EDN Design ideas 2009

January 2009

Digitally programmable-gain amplifier uses divergent-exponential curve
Circuit indicates ac-mains-fuse failure
Isolation MOSFET-driver IC gets improved power efficiency at lighter loads
Synthesize variable resistors with hyperbolic taper
Increase the range of memorized voltage for a sample-and-hold device
Inexpensive self-resetting circuit breaker requires few parts
Sinusoid generator uses dual-output current-controlled conveyors
Perform timing for microcontrollers without using timers

February 2009

Convert signals to proper logic levels
DDR-differential-clock source on SOC drives two DDR-memory chips
Flying capacitor and negative time constant make digitally programmable-gain instrumentation amplifier
MOSFET prevents battery damage
Voltage doubler improves accuracy
Digital controller compensates analog controller
Circuit provides constant-current load for testing batteries
MOSFET-based, analog circuit calculates square root
“Hippasian” nonlinear VFC stretches dynamic range
Decoder lights the way

March 2009

Microcontroller converts digital-temperature-sensor readings without floating-point arithmetic
Discrete-component buck converter drives HB LEDs
Drive a single-coil latching relay without an H-bridge circuit
Limit switches control dc-motor H bridge
Implement a clip-detection circuit for BTL Class D amplifiers
Buck converter uses low-side PWM IC
Isolated clock source acts as test generator
Class AB inverting amp uses two floating-amplifier cells
DPGA conditions signals with negative time constant
Instrumentation amplifier compensates system offset from single supply

April 2009

Twin-T power oscillators work as dc-biased ac sources
Diagnose LEDs by monitoring the switch-mode duty cycle
Single pin controls relay, intermittent buzzer, and status LED
Simple two-transistor circuit lights LEDs
Simple method uses PSpice for Thevenin-equivalent circuits
DAC and flip-flops form constant-current source
Convert negative inputs to positive outputs

May 2009
CMOS-NAND gates control sump pump
Use an LED to sense and emit light
Two instrumentation amps make accurate voltage-to-current source
Simple circuit indicates health of lithium-ion batteries
Current-sense monitor and MOSFET boost output current
Multiplexed, programmable-gain, track-and-hold amplifier has instrumentation inputs
Simple circuit smoothly drives stepper motors
Excel spreadsheet yields RLC best-fit calculator
Automatically turn secondary lamp on or off

June 2009
Fast 10-line-to-one-line data selector/multiplexer comprises only two ICs
Implement a simple digital-serial NRZ data-recovery algorithm in an FPGA
LED strobe has independent delay and duration
Cancel sensor-wiring error with bias-current modulation
Simple FSK modulator enables data transmission over low-speed link
Create a swept-sine function in LabView with just one virtual instrument
Charlieplexing at high duty cycle
Serial port tests digital circuits
DAC calibrates 4- to 20-mA output current
Alarm tells you to close the refrigerator door

July 2009
Illumination ring provides focused intensities
Digital variable resistor compensates voltage regulator
Hot-swap switch provides easy thermal protection
Add headphones to a Class D amplifier
Circuit eases power-sequence testing
Quasiresonant flyback converter easily charges energy-storage capacitors
First-event detector has automatic-reset function
Signal-powered linear optocoupler provides isolated control signal
Dark-activated switch needs only three components

August 2009
High-speed op amp enables IR-proximity sensing
Set your lights to music
Current limiter allows large USB bypass capacitance
High-speed pulse modulator retains signal envelope
Triac tester allows for manual or automatic operation
Handheld DMM copes with logic nanosecond-pulse-width waveforms
Build a simple complementary-bracket-pulse generator
Power-miserly voltage reference needs just one pin

September 2009
Turn a set/reset latch into an astable/monostable multivibrator
555 timer eliminates LED driver’s need for microprocessor control
Smart photoresistor timer needs few components
High-performance adder uses instrumentation amplifiers
Nonvolatile standby/on switch remembers its state
Missing pulse detects position or produces a delay
Emulate SPI signals with a digital-I/O card
Resistive DAC and op amp form hybrid divider
Connect two buttons with just two wires

October 2009
Unused port adds a PWM/analog channel to a microcontroller
Capacitance meter uses PLL for high accuracy
Resistor compensates for instrumentation-amp gain drift
Astable multivibrator gets hysteresis from positive-feedback stage
Class B amplifier has automatic bias
Cable tester uses LEDs to find faults
Dual-coil relay driver uses only two MOSFETs

November 2009
Negative-to-negative switch-mode converter offers high current and high efficiency
ADC for programmable logic uses one capacitor
Use two phases to cut current and improve EMI
Fader switch uses inexpensive controller
Inspect solar cells without a microscope
Solar-powered sensor controls traffic
Self-oscillating H bridge lights white LED from one cell
Low-cost LCD-bias generator uses main microcontroller as control IC

December 2009
Precision tilt/fall detector consumes less than 1.5 mW
Reset an SOC only when power is ready
Circuit provides simpler power-supply-sequence testing
Inexpensive power switch includes submicrosecond circuit breaker
Create a DAC from a microcontroller's ADC
Compact, four-quadrant lock-in amplifier generates two analog outputs
Eight-function remote uses one button, no microcode
Doorbell transformer acts as simple water-leak detector
Inverted regulator increases choice and reduces complexity
Debug a microcontroller-to-FPGA interface from the FPGA side

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AND FRAN GRANVILLE

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Digitally programmable-gain amplifier uses divergent-exponential curve

W Stephen Woodward, Chapel Hill, NC

DPGAs (digitally programmable-gain amplifiers) are handy signal-processing components whenever ADCs must acquire signals with a wide dynamic range. Without the ability to accommodate input-signal amplitude to match and efficiently use ADC span, low-level inputs may not be digitized with adequate resolution, and high-level inputs may overrange the ADC and be lost altogether.

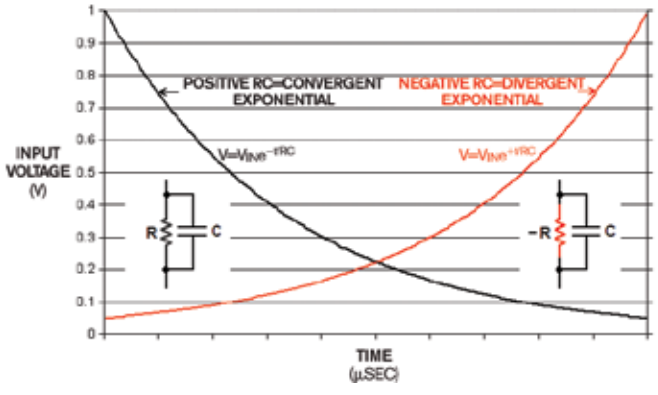

Figure 1 The behavior of the RC topology is still simple when you replace R with an active circuit that synthesizes a negative resistance.

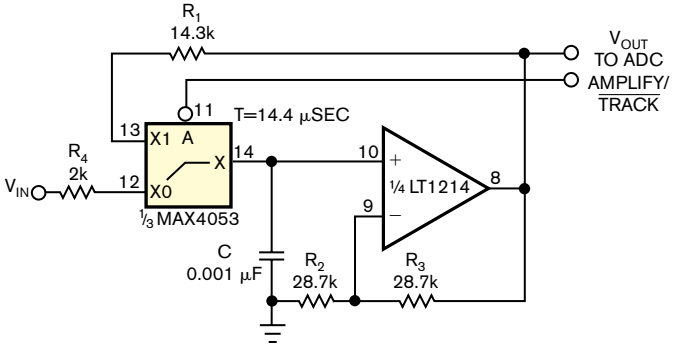

Figure 2 The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology.

DIs Inside

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Currently available DPGA designs typically incorporate a multiplying DAC into an op-amp-feedback loop, so that the input code to the multiplying DAC sets the amplifier's closed-loop gain. Several available monolithic DPGAs, such as Linear Technology's (www.linear.com) LTC6910 and National Semiconductor's (www.national.com) LMP8100, employ this topology. But the DPGA's digital-gain-control bits are sometimes inconvenient to provide, and these devices' output span may be inadequate, for example, to interface to ±10V ADC-input spans. Also, the resolution of these devices' available gain settings is usually coarse—for example, 2-to-1 per gain step—and their power consumption is sometimes large. In contrast, this Design Idea describes a new DPGA that employs the concept of the divergent-exponential curve.

No waveform is simpler or more familiar than the $e^{-t/RC}$-convergent exponential—the asymptotic discharge to zero of an elementary RC circuit initially charged to the input voltage, V_{IN}, in which $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V_{IN}/4$ at $t=2T$,

$V_{IN}/8$ at 3T, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). Replacing R with −R makes the RC time constant negative: −RC and the waveform function yield the divergent exponential, $V_{IN}\times e^{+t/RC}$. Then, instead of converging to zero, the waveform diverges theoretically to infinity, and $V=2V_{IN}$ at t=T, $4V_{IN}$ at 2T, $8V_{IN}$ at 3T, and so forth. Therefore, no matter how small the input voltage might be, you can amplify it as much as you desire to any voltage by simply waiting the right amount of time=$t=\log_2(V/V_{IN})T$ after starting the negative discharge.

The divergent-exponential and negative time constants are the core concepts of the DENT (divergent-exponential-negative-time-constant) DPGA topology (**Figure 2**). When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant: $-(R_1+R_{ON})(C+C_{STRAY})=-14.4$ µsec, where R_{ON} is the on-resistance of the CMOS switch, and C_{STRAY} is the parasitic capacitance surrounding C (**Figure 3**). It also creates a diverging exponential: $V_{OUT}(t)=V_{IN}\times 2^{(t/10\ \mu sec+1)}$. Thus, gain=$2^{(t/10\ \mu sec+1)}$. The 1-µsec timing resolution in the amplify-control bit provides 1.07-to-1=0.6 dB=33 steps/decade gain-programming resolution. **Figure 4** graphs the voltage gain versus the time elapsed since the track/amplify-logic transition.

Unlike monolithic PGAs, DENT uses discrete components, such as op amps and switches, so it can easily accommodate parameters such as I/O-voltage spans—negative inputs and 10V amplitudes—by choosing appropriate parts and power supplies. The accuracy and repeatability of the timing of exponential generation, ADC sampling, and RC-time-constant stability limit the practical performance of the amplifier in gain-programming accuracy and jitter. In the sample circuit, with T=14.4 µsec, 1 nsec of amplify-timing error or jitter equates to 0.007% of gain-programming error. Fortunately, the near ubiquity of programmable timer/counter hardware in popular microcontroller and data-acquisition peripherals usually makes the digital generation of a precisely repeatable amplify/track control an easy matter. On the analog side, possibilities exist for self-calibration algorithms that preserve gain-setting accuracy and relax RC-component-precision requirements, but they lie beyond the scope of this Design Idea. EDN

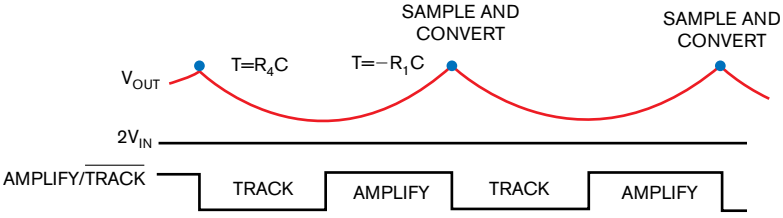

Figure 3 When the amplify/track-control bit goes to logic one, the two-times-noninverting gain of the op-amp follower creates a negative time constant.

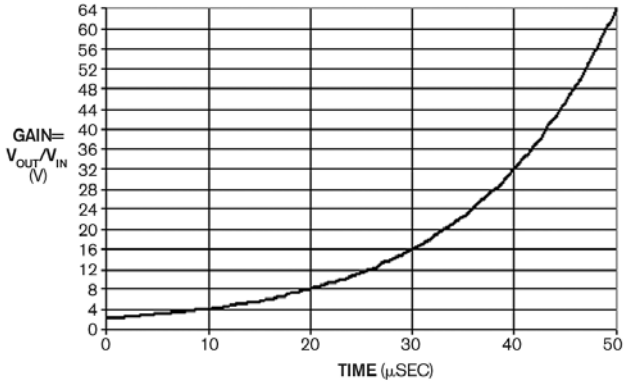

Figure 4 This graph shows the voltage gain versus the time elapsed since the track/amplify-logic transition.

Circuit indicates ac-mains-fuse failure

By Vladimir Oleynik, Moscow, Russia

Fuses are essential parts of power-distribution systems because they prevent fire or damage to electronic equipment. Fuses have the disadvantage of requiring replacement after every burnout, but they have the advantages of being inexpensive and widely available. It is difficult to determine the failure time of fuses with ceramic or sand-filled bodies to prevent arcing. This Design Idea presents a simple circuit that solves this problem (**Figure 1**). It visually and audibly indicates ac-mains-fuse failure; in most cases, audible indication is sufficient. The circuit works with a range of loads, and you can change its components to adapt to particular ac mains and load specifications.

When a fuse is in good order, the indication circuit is off because the fuse shunts it. When a fuse burns out, the indication circuit starts working. Capacitor C_1 reduces the ac-mains volt-

age, and bridge diode D_1 rectifies the ac voltage. Resistor R_1 limits inrush current when capacitor C_1 is discharged. Zener diode D_2 and capacitor C_2 form a dc voltage to operate a buzzer- and blinking-LED network. The blinking LED flashes, and buzzer B_1, which has a built-in generator, sounds.

Like most other simple circuits, this circuit also has a disadvantage: It is incompatible with some load-power and ac-mains-voltage values. When a fuse burns out, the load stays connected to the ac mains, and the ac voltage divides between the circuit and the load. When the load is highly resistive or the ac-mains voltage is 110V rather than 220V, the circuit's operating voltage may be too low to drive the circuit. In that case, decrease the value of capacitor C_1 to 47 or 68 nF, after which the circuit's resistance rises. With the component values in **Figure 1**, the tested circuit operated with resistive loads of 20 to 200W. With higher-power loads, the circuit operates well because, with higher load-power values, the circuit's load resistance is lower. EDN

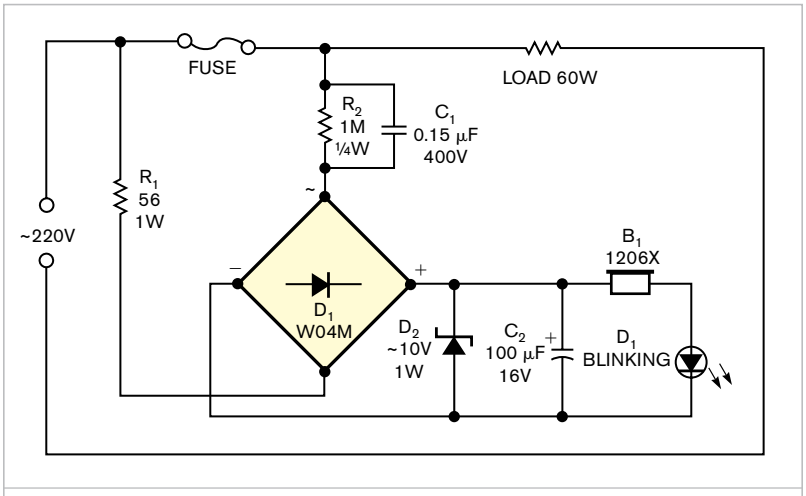

Figure 1 This circuit visually and audibly indicates ac-mains-fuse failure.

Isolation MOSFET-driver IC gets improved power efficiency at lighter loads

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Many modern power MOSFETs reach low values of on-resistance at 5V even when the gate-to-source voltage is 5V. For heavy-duty power MOSFETS and, especially, IGBTs (insulated-gate bipolar transistors), however, engineers prefer gate-to-source voltages of 12 to 15V because the on-resistance of those power switches further decreases at higher gate-to-source voltages. The 17A-rated IRFR024 power MOSFET from International Rectifier (www.irf.com), for example, has an on-resistance of 0.075Ω (**Reference 1**). When the gate-to-source voltage is 12V, the device's on-resistance drops to 41% of its value compared to a case of a gate-to-source voltage of 5V. At a switching current of 10A, the device dissipates 6W less when the gate-to-source voltage is 12V.

IC_1, an Analog Devices (www.analog.com) ADuM5230 IC isolation driver, can boost a 5V input to a level that's high enough to drive a MOSFET's on-resistance to a low value, minimizing power dissipation (**Figure 1**). At low switching frequencies, however, the IC's high-side, internal 18V clamping dissipates the energy that the IC draws from the low-side 5V supply (**Reference 2**).

The ADuM5230's output is, however, unregulated. Fortunately, this IC has an adjustment pin that you can use to control the duty cycle of the device's internal PWM (pulse-width modulator) to reduce the duty cycle from a value of 1 to approximately 0.1. The default duty cycle has the value of 0.55 when the adjust pin is open. The lowest value of duty cycle occurs when connecting the adjust pin to the 5V supply. IC_2, an ASSR-1219 advanced photo-MOSFET device from Avago Technologies (www.avagotech.com), controls the voltage at the adjust pin. The photo-MOSFET has 0V saturation voltage between its output terminals. As a classical optocoupler has a bipolar phototransistor, using it as IC_2 would be less suitable in this case. A bipolar phototransistor has a saturation voltage of 0.4V, and, further, the CTR (current-transfer ratio) of a common optocoupler would decrease significantly when operating close to output saturation. Pulling the voltage at the adjustment pin to the external voltage-supply level comes into account when the high-side output of IC_1 has light or negligible loading.

At some point, V_{ISO}, the high-side output voltage of IC_1, will exceed the value of approximately $V_Z(I_F)+V_{FLED}\sim13.5V$, where $V_Z(I_F)$ is the voltage of zener diode D_1 at I_F, the forward current of D_2, and V_{FLED} is the minimum forward voltage at D_2, the LED of IC_2. IC_1 exceeds this value, current starts to flow through the D_2, and the MOSFET at the output of IC_2 becomes conductive. The manufacturer of IC_2 designed it for on/off operation and recommends a forward current of at least 0.5 mA (**Reference 3**).

At signal-level loading of the MOSFET at the output of IC_2, a few tens of microamperes of forward current through the LED cause the photo MOSFET's on-resistance to change

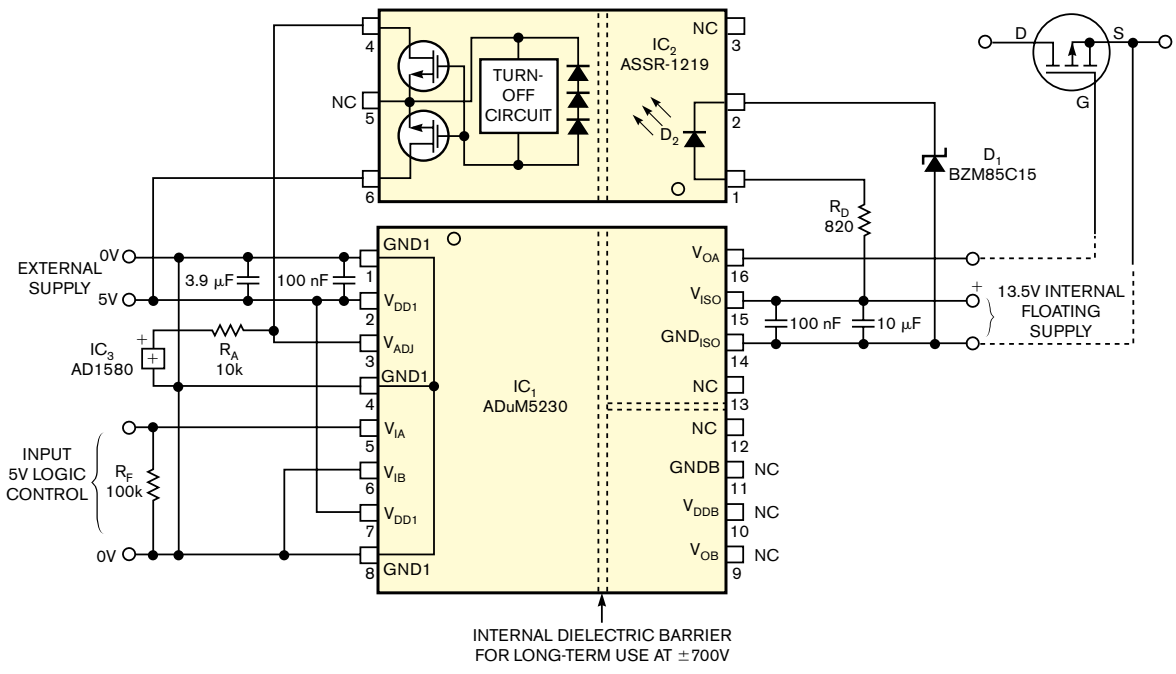

Figure 1 Connecting optical feedback by opto-MOSFET IC_2 in the power-MOSFET-driver IC_1 stabilizes the high-side output voltage to 13.5V at values of loading current down to 3.7 mA. The power efficiency of the circuit increases for a loading current of less than 7 mA.

from an almost-infinite value to a value of kilohms. The voltage level at the adjust pin then increases, and the duty factor of both the PWM in IC_1 decreases. This action establishes an isolated negative-voltage feedback. Thus, the temperatures of both the MOSFET and the LED in IC_2 have little effect on the properties of the circuit. At lighter loads, the current drain of the 5V supply is much lower than that of IC_1 with its adjust pin open.

Under test, the default supply current of the unloaded IC_1 was approximately 94.6 mA. This value decreases to 31.7 mA with the feedback in the circuit. At heavy loading, the high-side output current of IC_1 rises to approximately 20 mA, and the duty factor rises automatically to a proper value that's higher than at the default supply current. Thus, the output voltage is roughly 13.5V within the range of approximately 3.7 to 22.6 mA. The power efficiency of the circuit is 20% or greater. At an output current of 4.5 mA, the power efficiency is 20.5%, and the power efficiency for IC_1 is approximately 15%. At a current of 3.7 mA, the circuit reaches 20% efficiency, a value that's considerably higher than the 13% in IC_1 with its adjust pin open. EDN

REFERENCES

1 "IRFR/U024 HEXFET Power MOSFET," International Rectifier, www.irf.com/product-info/datasheets/data/irfr024n.pdf.

2 "ADuM5230, Isolated Half-Bridge Driver with Integrated High-Side Supply," Analog Devices Inc, 2008, www.analog.com/static/imported-files/data_sheets/ADuM5230.pdf.

3 "ASSR-1218, ASSR-1219 and ASSR-1228, Form A, Solid State Relay (Photo MOSFET) (60V/0.2A/10Ω)," Avago Technologies, July 18, 2007, www.avagotech.com/docs/AV02-0173EN.

Synthesize variable resistors with hyperbolic taper

TL Flaig, Clinton, WA

In adjustable, frequency-selective RC networks, the reciprocal of an RC product, $\omega_C=1/RC$, determines the corner frequencies of the network. If the adjustable elements are potentiometers with a linear-control characteristic—that is, taper—$R(\alpha)=\alpha R_P$, where α is the normalized wiper position, $0\leq\alpha\leq1$, and R_P is the potentiometer's end-to-end resistance, then the corner frequencies are reciprocal functions of the potentiometer's wiper position, and the frequency scale compresses at the high end of the adjustment range. This situation is usually undesirable because it complicates adjustment of the network at the high

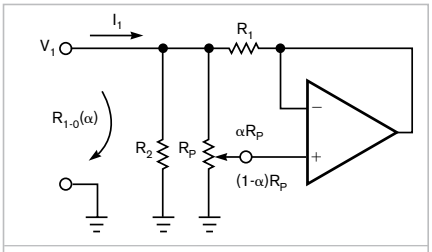

Figure 1 This simple circuit synthesizes a grounded variable resistance with a hyperbolic-control characteristic.

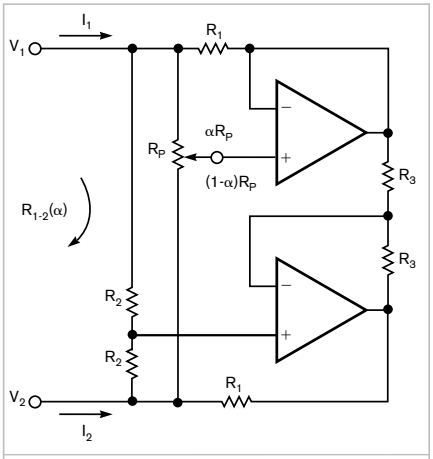

Figure 2 You can realize a floating variable resistance, with hyperbolic taper, with this circuit. Note that fixed resistors with the same number are matched pairs.

end. To make the frequency scale linear requires a control element with a hyperbolic taper—that is, something in the form $R(\alpha)=R_P/(A+\alpha B)$. Such variable resistances are not generally available from manufacturers, but you can synthesize them using a linear taper potentiometer and a few other components.

Figure 1 shows a simple circuit for producing a ground-referenced variable resistance having the desired hyperbolic-control characteristic. Analysis of this circuit yields the following relationship between the control setting and the resistance from Node 1 to ground: $R_{1\text{-}0}(\alpha)=R_1R_2R_P/(R_1R_2+R_1R_P+\alpha R_2R_P)0\leq\alpha\leq1$. If you use this resistance in series or in parallel with a capacitor, the resulting corner frequency will be a linear function of α: $\omega_C=(R_1R_2+R_1R_P+\alpha R_2R_P)/R_1R_2R_PC$. The minimum and maximum values for $R_{1\text{-}0}$ are $R_{1\text{-}0MIN}=R_1R_2R_P/(R_1R_2+R_1R_P+R_2R_P)$ and $R_{1\text{-}0MAX}=R_2R_P/(R_2+R_P)$.

To design this circuit for specific values of $R_{1\text{-}0MIN}$ and $R_{1\text{-}0MAX}$, choose $R_P>R_{1\text{-}0MAX}$ and then compute $R_1=R_{1\text{-}0MAX}R_{1\text{-}0MIN}/(R_{1\text{-}0MAX}-R_{1\text{-}0MIN})$ and $R_2=R_PR_{1\text{-}0MAX}/(R_P-R_{1\text{-}0MAX})$.

You can extend the basic circuit of **Figure 1** to produce a floating variable resistance with hyperbolic taper (**Figure 2**). The value of the floating resistance between nodes 1 and 2 is $R_{1\text{-}2}(\alpha)=2R_1R_2R_P/(2R_1R_2+R_1R_P+2\alpha R_2R_P)0\leq\alpha\leq1$, and the minimum and maximum values for $R_{1\text{-}2}$ are $R_{1\text{-}2MIN}=2R_1R_2R_P/(2R_1R_2+R_1R_P+2R_2R_P)$ and $R_{1\text{-}2MAX}=2R_2R_P/(2R_2+R_P)$. To design the circuit of **Figure 2** for specific values of $R_{1\text{-}2MIN}$ and $R_{1\text{-}2MAX}$, choose $R_P>R_{1\text{-}2MAX}$ and then compute $R_1=R_{1\text{-}2MAX}R_{1\text{-}2MIN}/(R_{1\text{-}2MAX}-R_{1\text{-}2MIN})$ and $R_2=\frac{1}{2}R_PR_{1\text{-}2MAX}/(R_P-R_{1\text{-}2MAX})$. Note that the value of the R_3 resistors does not directly affect the value of $R_{1\text{-}2}(\alpha)$. You should choose resistors that are large enough to not excessively load the op-amp outputs.

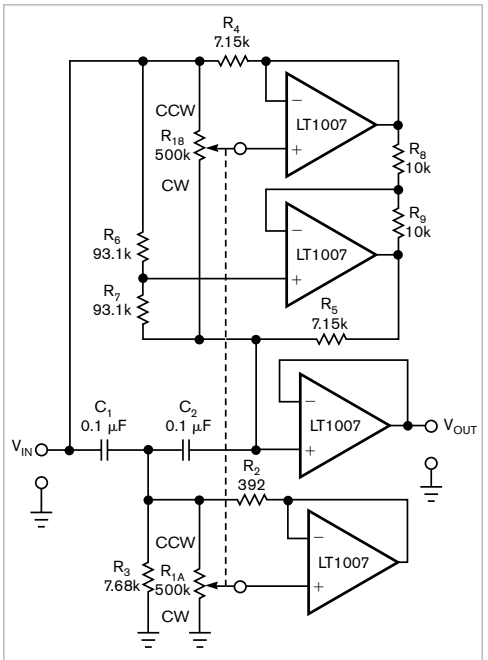

Figure 3 The basic circuits of figures 1 and 2 have been used in the design of a bridged-T notch filter with a variable notch center frequency and a linear frequency scale.

Figure 3 illustrates the application of the circuits in **figures 1** and **2** to the design of an adjustable bridged-T notch filter with a linear frequency scale. The filter has a notch center frequency that is adjustable from 50 to 1000 Hz and a notch depth of −20 dB. These requirements and the choice of 0.1-µF capacitors for C_1 and C_2 dictate that $R_{1\text{-}0}$ varies from 375 to 7503Ω and that $R_{1\text{-}2}$ varies from 6752 to 135,047Ω. (A side benefit of using this technique is that it frees the designer from the restrictions of the limited number of standard end-to-end resistance values that potentiometer manufacturers offer.)

Figure 4 plots the Spice-simulated notch center frequency for the circuit of **Figure 3** against the normalized wiper position. The notch center frequency is a linear function of the control position. EDN

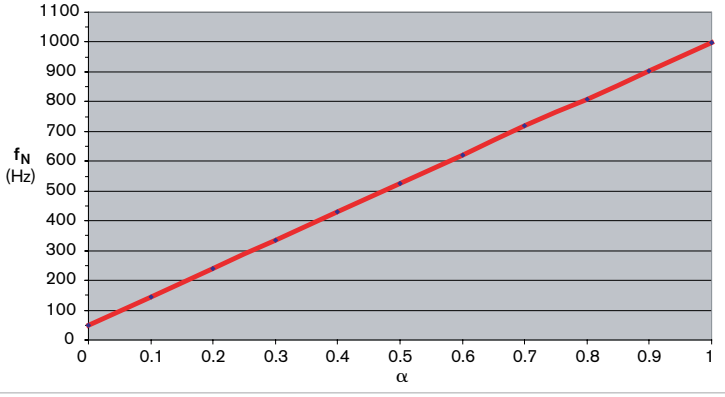

Figure 4 The Spice-simulated notch center frequency for the circuit of Figure 3 versus the normalized wiper position shows that the notch center frequency is a linear function of the control position.

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READERS SOLVE DESIGN PROBLEMS

Increase the range of memorized voltage for a sample-and-hold device

Yakov Velikson, Lexington, MA

Sample-and-hold devices find use in front of ADCs. The basic sample-and-hold circuit comprises two op amps, A_1 and A_2; a switch, S_1; and a capacitor, C_1 (**Figure 1**). For many low-power op amps, the values of the input and output voltages can be only ±10 to ±14V using a standard ±15V power supply. Enabling these devices to handle greater voltage can significantly improve the resolution of an ADC.

You can increase the memorized voltage that amplifiers A_1 and A_2 can reach by using a variable power supply (**references 1** and **2**). This approach places additional voltage requirements on S_1, however. To continue using switches with the same range as the original, you must add two switches and independent control-logic blocks, CL_1 and CL_2, for switches S_1, S_2, and S_3 (**Figure 2**). The two parts of the circuit may have independent power supplies. You apply the same variable voltages to amplifiers A_1 and A_2 as you do to control-logic blocks CL_1 and CL_2, respectively. When S_1 and S_3 are closed, S_2 is open, and vice versa.

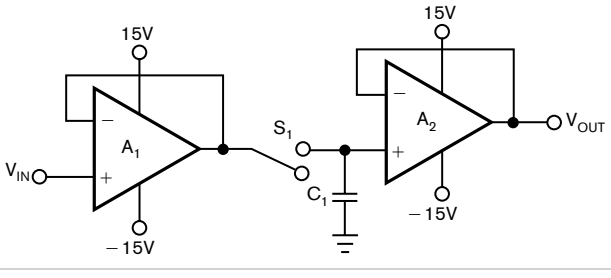

Figure 1 A basic sample-and-hold circuit comprises two op amps, a switch, and a capacitor.

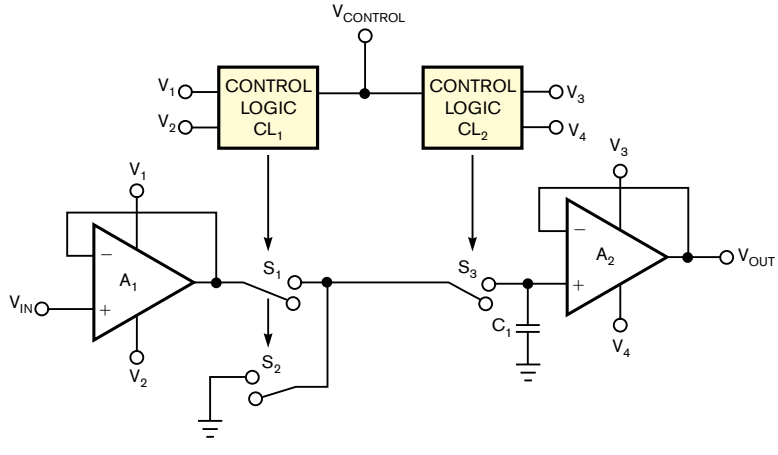

Figure 2 To continue using switches with the same voltage range as that of Figure 1, you must add two switches and two independent control-logic blocks.

The resulting circuit keeps the voltages connected to the gate and substrate for the MOS transistors of each switch within the desired 30V range (**Figure 3**). (You derive this value from the sum of absolute-voltage values: $|V_1|+|V_2|$ and $|V_3|=|V_4|$.) Voltages V_1 and $-V_2$ connect to amplifier A_1, control-logic block CL_1, and the substrates of the transistors of switches S_1 and S_2. Voltages V_3 and $-V_4$ connect to amplifier A_2, control-logic block CL_2, and the substrates of the transistors of switch S_3.

You create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8, which connect to the 30 and the −30V power supplies and the output of amplifier follower A_1 (**Figure 3**). Transistors Q_1 and Q_2 create the change to the power supply of amplifier A_1. Volt-

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ages V_1 and V_2 also supply power to control-logic block CL_1 and the substrates of the transistors of switches S_1 and S_2. CL_1 comprises transistors Q_{11}, Q_{12}, Q_{15}, and Q_{16}. It creates a control signal for gates Q_5 and Q_6 of switch S_1 and the inverse signal for gates Q_8 and Q_9 of S_2.

Resistor dividers R_9 and R_{10} and R_{11} and R_{12} connect to the 30 and the −30V power supplies, and the output of amplifier follower A_2 creates the changing voltages V_3 and V_4. Transistors Q_3 and Q_4 create the change to the power supply of amplifier A_2. Voltages V_3 and V_4 also supply power to control-logic block CL_2 and the substrates of the transistors of switch S_3. CL_2 is made up of transistors Q_{13}, Q_{14}, Q_{17}, and Q_{18}. It creates a control signal for gates Q_7 and Q_{10} of switch S_3. Transistors Q_5 through Q_{10} and Q_{11} through Q_{18} of CL_1 and CL_2, respectively, are complementary pairs of MOS logic transistors. EDN

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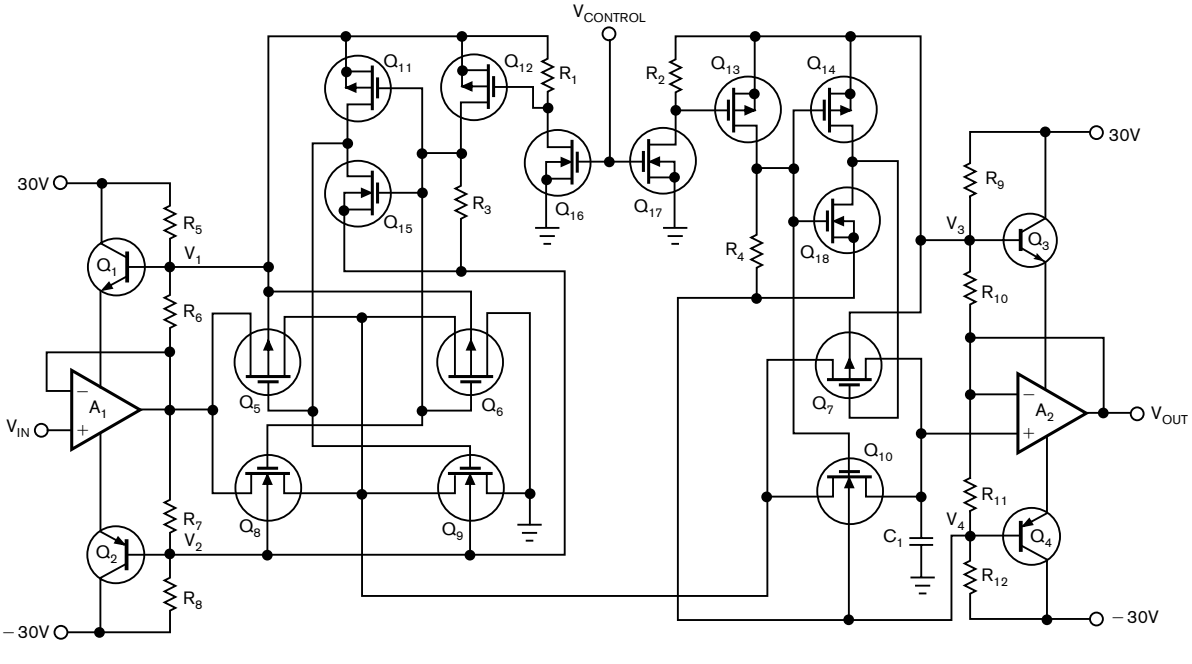

Figure 3 You can create the changing voltages of V_1 and V_2 using resistor dividers R_5 and R_6 and R_7 and R_8.

Inexpensive self-resetting circuit breaker requires few parts

Anthony H Smith, Scitech, Bedfordshire, England

Most readers are familiar with the current-limiting circuit in **Figure 1**, in which the load current, I_L, is limited to a value of $I_L \approx V_{BE}/R_S$, where V_{BE} is the base-to-emitter voltage and R_S is the sense resistance. Under normal conditions, in which the base-to-emitter voltage is too small to bias Q_1 on, P-channel MOSFET Q_2's gate resistor, R_G, biases Q_2 fully on, and only the load resistance, R_L, and the load voltage, V_L, determine the load current. However, if the load current increases to a point at which the base-to-emitter voltage is approximately 0.7V, Q_1 starts to conduct and reduces Q_2's gate-to-source voltage, V_{GS}, to a level that holds the load current roughly constant at a value you derive from $I_{LMAXIMUM} \approx 0.7V/R_S$.

This linear current limiter is effective for applications in which the maximum load current, the supply voltage, or both are relatively small. However, the power that the circuit's pass transistor, Q_2, dissipates limits the circuit's applicability. For example, if the maximum load current is 200 mA and the supply voltage, V_S, is 24V, a short circuit across the load would dissipate almost 5W into Q_2. Q_2 must handle this power with adequate margin, and additional heat-sinking may be necessary to keep its junction temperature at a safe level. Using larger values of

maximum load current, supply voltage, or both exacerbates this problem. In many applications, the cost, size, and weight of the components necessary to handle the short-circuit power dissipation may be prohibitive.

However, by adding a few inexpensive components, you can adapt the circuit to provide effective current limiting with none of the power-dissipation headaches. The resulting circuit functions as a self-resetting circuit breaker (**Figure 2a**). Again, Q_1 and R_S provide a current-monitoring function in which the sense voltage $V_{SENSE}=I_L \times R_S$. In this circuit, however, Q_2 is either fully on or fully off and never biases into its linear region. Because Q_1's base current is normally small, the voltage drop across base resistor R_B is also small, such that the base-to-emitter voltage is approximately equal to the sense voltage.

To understand how the circuit works, assume that the load current is initially low and the base-to-emitter voltage is less than 0.7V. Under these conditions, Q_1 is off and timing capacitor C_1 remains uncharged such that V_{IN}, the voltage at the input of Schmitt inverter IC_1, is 0V. Thus, IC_1's output is approximately 5V, biasing Q_3 on, which in turn provides gate bias for Q_2 through R_4, allowing current to flow from the supply voltage into the load through the sense resistor and Q_2's on-resistance.

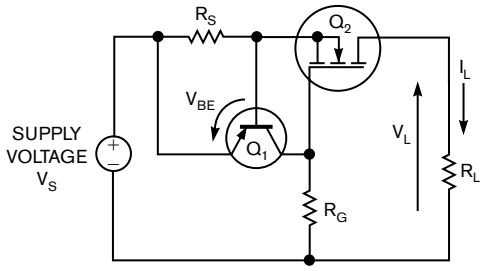

Figure 1 A conventional two-transistor current limiter prevents excessive current from reaching the load.

If a fault now causes the load current to increase to a level at which the base-to-emitter voltage is approximately 0.7V, Q_1 turns on and its collector current rapidly charges C_1. The input voltage now quickly rises toward the Schmitt inverter's upper threshold voltage, V_{TU}, at which point IC_1's output goes low, turning off Q_3 and Q_2. The load current now falls to 0A and the base-to-emitter voltage falls to 0V, thereby causing Q_1 to turn off. C_1 now begins to discharge through R_1 and R_2, and the input voltage slowly falls toward the Schmitt inverter's lower threshold voltage, V_{TL}. At this point, IC_1's output again goes high, Q_3 and Q_2 turn on, the circuit breaker resets itself, and the process repeats until you remove the fault.

The circuit's waveforms show the relationship between the input voltage and the load voltage (**Figure 2b**). Because load current flows into Q_2 only during the on-time, the average power it dissipates is directly proportional to the duty cycle: $P_{AVG} \propto t_{ON}/(t_{ON}+t_{OFF})$, where P_{AVG} is the average power in watts, t_{ON} is the on-time, and t_{OFF} is the off-time. Provided that C_1, R_1, and R_2 set a large enough time constant, the off-time will normally be much greater than the on-time, and the resulting power that Q_2 dissipates will be low. Like the linear-current limiter, the sense resistor sets the circuit breaker's current limit: $I_{LMAXIMUM} \approx 0.7V/R_S$ (A).

R_1 and R_2 form a potential divider that ensures that the input voltage can never exceed IC_1's maximum input voltage. Select values such that the input voltage is 5V or less when Q_1 is fully on, where the voltage of C_1 is roughly equal to the supply voltage. Also, choose values that are large enough to provide a large time constant without requiring an excessively large value of C_1. The selection of transistor Q_1 isn't critical, but you should select a device with good current gain and make sure that its maximum collector-to-emitter voltage is greater than the supply voltage. When choosing a P-channel MOSFET for Q_2, re-

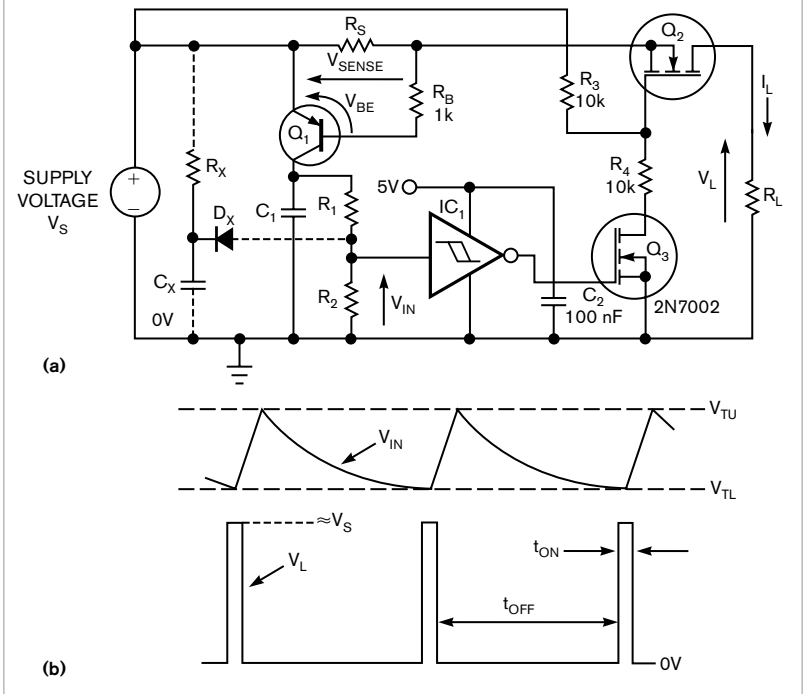

Figure 2 Adding a few components turns the current-limiting circuit into a pulser that reduces heat in the pass transistor, Q_2 (a). The circuit's waveforms show the relationship between the input voltage and the load voltage (b).

member that it must withstand the full supply voltage when you bias it off, so make sure that the maximum drain-to-source voltage is greater than the supply voltage. When choosing a value for the sense resistor, ensure that the base-to-emitter voltage is less than 0.5V at the maximum normal value of the load current.

Loads such as filament bulbs, capacitive loads, and motors that exhibit a large inrush current can cause the circuit breaker to trip on power-up. You can avoid these problems by adding capacitor C_X, diode D_X, and resistor R_X. On power-up, C_X is initially uncharged and pulls the input voltage toward 0V through D_X. This action prevents the circuit breaker from tripping until the inrush current subsides. C_X and R_X determine a delay, after which the voltage on C_X eventually rises to the supply voltage, D_X becomes reverse biased, and the circuit breaker is then free to respond to overcurrent faults. Be prepared to experiment with the values of C_X and R_X to get the right delay time. Values of 10 µF and 1 MΩ, respectively, are good starting points. EDN

Sinusoid generator uses dual-output current-controlled conveyors

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Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption. Hence, designers employ several implementations of current mode in these devices for realizing various functions. A previous Design Idea introduced a second-generation dual-output current-controlled conveyor to create oscillators (**Reference 1**). Unfortunately, these circuits aren't available as ICs, but you build them from discrete components. **Figure 1** illustrates an active building block of such a circuit, which the following **equations** characterize: $I_Y=0$, $V_X=V_Y+I_XR_X$, $I_{Z+}=I_X$, and $I_{Z-}=-I_X$. You can express the parasitic resistance at terminal X as $R_X=V_T/2I_B$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades. **Figure 2** shows the bipolar implementation of the circuit.

The circuit provides an extra degree of freedom in the sense that the control over the frequency of oscillation can be through both current and voltage. The circuit in the previous Design Idea provides various advantages, it this new circuit not only retains all those essential advantages, it also provides an extra feature of voltage controllability of frequency of oscillation.

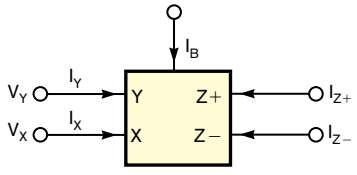

Figure 1 Second-generation current conveyors feature wide signal bandwidth, linearity, wide dynamic range, simple circuitry, and low power consumption.

Additionally, you can control the condition of oscillation using the conveyors' bias currents.

Figure 3 shows the proposed sinusoid-oscillator circuit. You can obtain the characteristic **equation** for the circuits as follows: $S_2C_1C_2R_{X1}R_{X2}+SC_2R_{X2}-SC_2R_{X1}+K=0$,

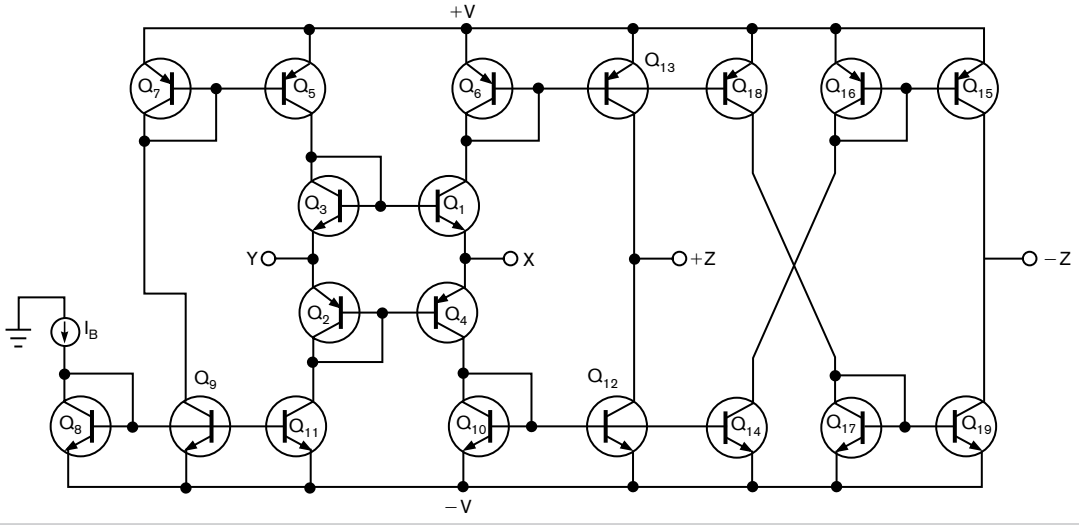

Figure 2 A current-controlled circuit uses no internal resistors or capacitors.

where K is the voltage multiplier. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360°—the required condition for oscillation is $R_{X1}=R_{X2}$, and the frequency of oscillation is $f=1/2\pi\sqrt{k/(C_1C_2R_{X1}R_{X2})}$.

Clearly, you can use the gain buffer to vary the frequency of oscillation, which is the area in which this circuit differs from the earlier Design Idea. You can use both current and voltage to control the voltage multiplier. The circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4} (**Figure 4**). For voltage control over K, you can use another circuit simply by using a noninverting op amp and replacing the resistors with MOSFETs working in that triode region. That approach simulates voltage-controlled resistors.

The circuit in **Figure 2** underwent testing with a PR100N PNP transistor and an NPN NP100N transistor of the bipolar arrays ALA400 and a dc supply of ±3V (**Reference 2**).

The circuit requires only two current-controlled conveyors, two grounded capacitors, and a voltage multiplier; it requires no floating capacitors and no external resistors, which makes the circuit's power consumption lower than that of RC oscillators. For a conventional bipolar-transconductance operational amplifier, the transconductance, g_m, is $I_B/2V_T$. Comparing this figure with the equivalent value of I_B, the transconductance of the bipolar-transconductance op amp is four times less than that of a dual-output current-controlled conveyor. Thus, the power consumption of the current-controlled-conveyor-based circuit is about four times less per active device than that of the op-amp-based circuit. The sensitivity study shows that $S^{\omega C}_{K;RX1;RX2;C1;C2}=-½$; ωc sensitivities are hence less than unity, which is an attractive feature of this circuit. Remember that creating an accurate oscillator model requires modeling equations to be nonlinear, and meeting the Barkhausen criteria is a necessary condition for oscillation. Oscillator circuits may latch up and never oscillate even if you satisfy the Barkhausen criteria.EDN

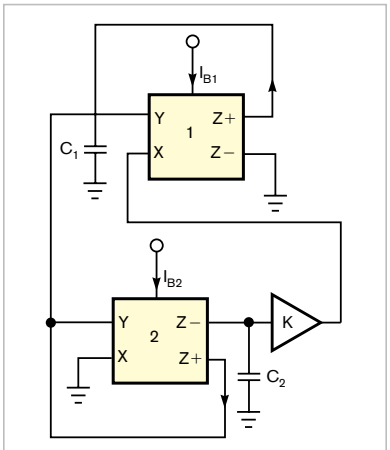

Figure 3 This configuration creates an oscillator from two current-controlled conveyor circuits.

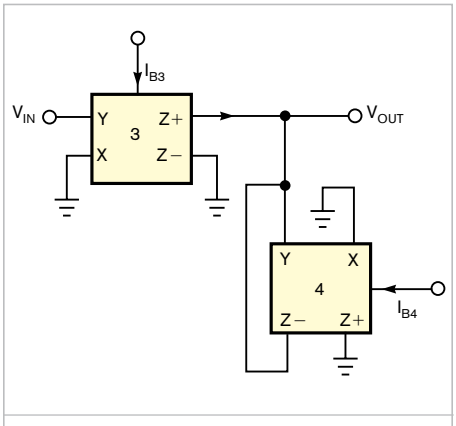

Figure 4 This circuit lets you vary the voltage multiplier by adjusting bias currents I_{B3} or I_{B4}.

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Perform timing for microcontrollers without using timers

Ganeshkumar Krishnamoorthy, NTERA Ltd, Dublin, Ireland

Microcontrollers now find use in every walk of life. Their peripherals vary from the general-purpose I/Os to the USB interface, making them versatile for a range of products. Timing is one key part of a typical microcontroller application. Low-cost microcontrollers have one or two built-in timers and often also have a watchdog timer. Sometimes, the design requires more timers without a significant cost increase. Software timers are not suitable for time-critical application because the controller is fully occupied. The circuit in this Design Idea uses the I/O "interrupt-on-change" feature that is common in most microcontrollers to implement a medium-precision, long-period timer with low additional cost.

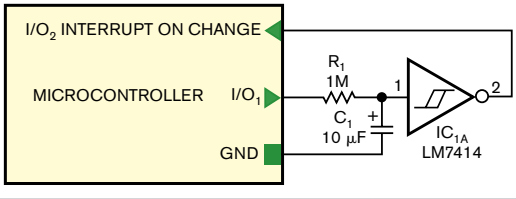

Figure 1 The RC filter along with I/O_2's interrupt-on-change feature provides a simple and cost-effective approach for a variety of time-scale measurements from microseconds to minutes.

The circuit in **Figure 1** uses I/O_1, a typical I/O pin, to drive an RC filter. The circuit feeds the output of the RC filter to a Schmitt-trigger inverter whose

output goes back to I/O_2, which has the interrupt-on-change feature. After power-up, I/O_1 is low and the output of the Schmitt-trigger inverter is high. After initialization, I/O_1 goes high. Capacitor C_1 charges up with the time constant R_1C_1. Once it reaches logic-high voltage, the output of the Schmitt-trigger inverter goes low and triggers an interrupt on I/O_2. In the ISR (interrupt-service routine), a counter increments, driving I/O_1 low. Now, C_1 discharges through R_1. The voltage reaches logic low, again triggering an interrupt. As the cycle repeats, the value in the counter indicates time=counter×R_1C_1. The Schmitt-trigger inverter serves as a debouncer.

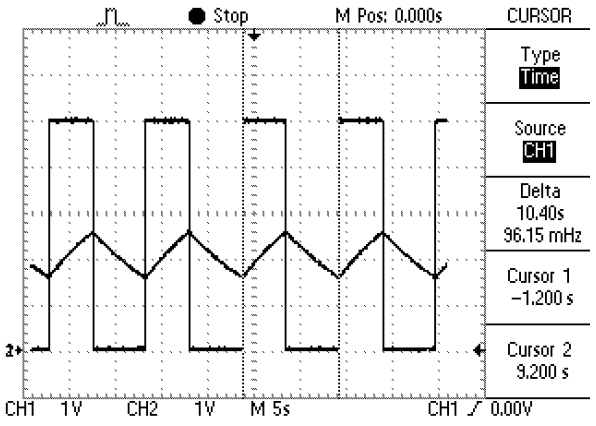

Figure 2 Channel 1 shows I/O_1's waveform, and Channel 2 shows the capacitor's charging/discharging waveform. The time period of the waveform is 10.4 sec.

Listing 1, which is available in the Web version of this Design Idea at www.edn.com/090122dia, includes the software routine for the ATMEGA64 microcontroller from Atmel (www.atmel.com). In the **listing**, Port D, Pin 5 plays the role of I/O_1 and Pin 3, whose alternate function is INT3, plays the role of I/O_2 in **Figure 1**. The trigger-edge interrupt in this case changes from falling-rising-falling edge in a cycle. Most microcontrollers don't require this feature because any logic change will trigger an interrupt. **Figure 2** shows the timing waveform of the circuit with the ATMEGA64 and the 74HC14.

The circuit's advantages are its low cost, a microcontroller-clock-independent time period, and the ability to achieve time periods of minutes to hours by tuning resistance and capacitance. For example, with a resistance of 10 MΩ, a capacitance of 10 μF, and a 16-bit register as a counter, you can achieve a maximum count of 75.85 days. EDN

ACKNOWLEDGMENT

This work is part of a system design in a project funded by the European Union under the Marie Curie Project.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Convert signals to proper logic levels

Abel Raynus, Armatron International Inc, Malden, MA

When designing a test station incorporating a microcontroller, you often face voltages in the test that exceed the maximum input level permitted for the microcontroller. For example, if a microcontroller uses a 5V power supply, then the maximum input signal should also be 5V. When a test voltage exceeds 5V, you might think to reduce the voltage with a voltage divider. A voltage divider can influence the DUT (device under test), however. So, a signal conditioner needs high input impedance. Also, the signal conditioner's output signals should match the logic levels of the microcontroller despite some fluctuation of the measured signal. It allows you to use the regular microcontroller-input pins instead of ADC ones.

Engineers often use a noninverting op amp to bring signal voltages in line. However, most op amps have differential-input-voltage ranges matching their power-supply voltages. Thus, you need one more power-supply voltage with a higher voltage and several extra resistors to lower the op amp's output to the microcontroller level. Moreover, the output will follow the measured input-signal variations, so it needs analog-to-digital conversion in the microcontroller.

A better approach is to use a small-signal MOSFET in the voltage-repeater configuration (**Figure 1**). You can use the BS107A from On Semiconductor (www.onsemi.com) for this task. You can consider the gate-to-source area of the MOSFET as a capacitor with a value of approximately 60 pF. To discharge it in the absence of the DUT, connect a resistor of ap-

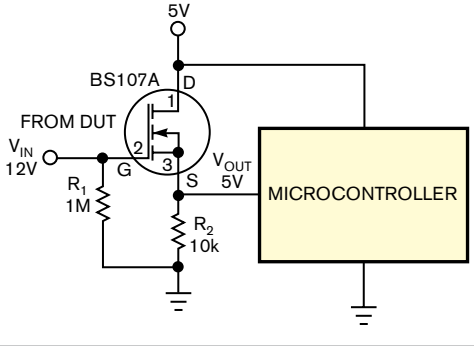

Figure 1 You can use a small-signal MOSFET to provide overvoltage-signal conditioning.

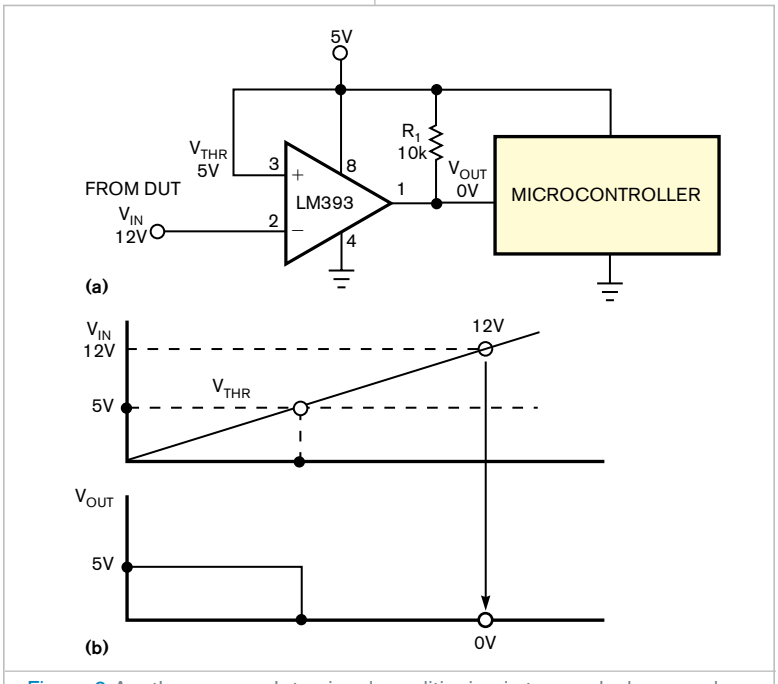

Figure 2 Another approach to signal conditioning is to use dual- or quad-voltage comparators (a). The 5V power-supply voltage acts as the positive-threshold voltage. The output is 5V for input signals lower than this level. If the input signal exceeds 5V, the output voltage drops to 0V (b).

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proximately 1 MΩ between the gate and ground. Also, the input voltage should be more than the MOSFET's gate-threshold voltage, V_{THR}, of 3V dc but less than the maximum rated gate-to-source voltage, V_{GS}, of 20V dc. In this **figure**, the output voltage never exceeds the power-supply voltage, and variations of the input voltage have no effect on output as long as they happen in the saturation region. A drawback of this approach is that you must use as many transistors as the number of test-points in the DUT.

Another good option is to use any dual- or quad-voltage comparator. You can use an LM393 from National Semiconductor (www.national.com) because it's inexpensive and widely available. **Figure 2** shows a simple configuration with few components. The 5V power-supply voltage acts as the positive-threshold voltage. The output is 5V for input signals lower than this level. If the input signal exceeds 5V, the output voltage drops to 0V. Resistor R_1 connects an open collector of the LM393 to the supply voltage.

Sometimes, a zero-output signal is undesirable. A missing power-supply voltage, a bad solder joint, or a broken wire in the test fixture could cause this zero-output signal. Use a logic high level when the signal under test is present and logic low when it's absent. At first glance, it seems that just switching the comparator pins of the input and the threshold voltages provides an acceptable approach. However, that assumption is invalid because the positive input voltage may exceed the power-supply level only as long as the other voltage remains within the common-mode range. The upper limit of common-mode input voltage for the LM393 is 1.5V less than the power-supply voltage, or 3.5V. Thus, you should use the voltage divider comprising R_2 and R_3 for the threshold voltage (**Figure 3**).EDN

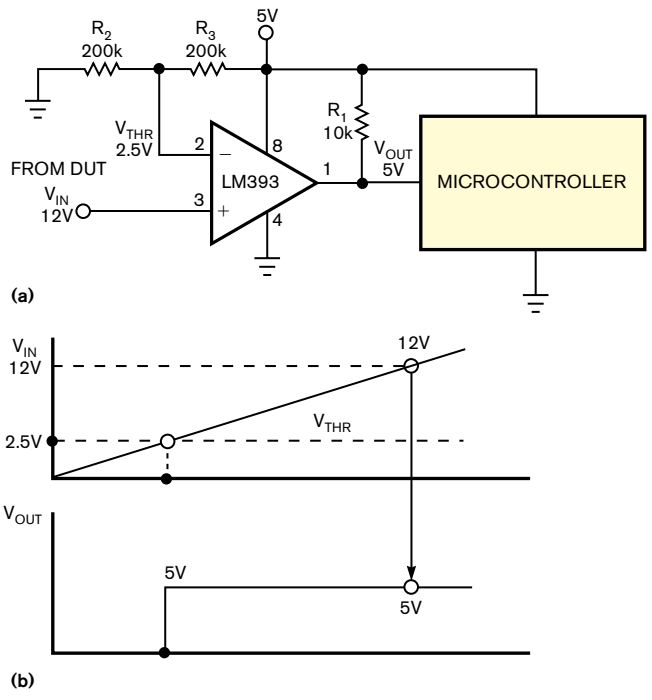

Figure 3 Use the voltage divider comprising R_2 and R_3 for the threshold voltage.

DDR-differential-clock source on SOC drives two DDR-memory chips

Goh Ban Hok, Infineon Technologies, Singapore

Many system engineers assume that a differential-clock source should drive just one chip. If a system design requires driving two DDR-memory chips, however, the design would inevitably need a differential-clock buffer. This Design Idea describes a circuit that drives two DDR chips without a clock-source buffer yet does not sacrifice much of the signal integrity.

The cost-saving nature of an SOC (system-on-chip) design dictates the need for fewer pins. Such designs typically have only one pair of differential signals available for external-memory-chip connection. When the system design requires more than one DDR chip, designers typically use a clock buffer.

Figure 1 shows an SOC with an embedded DDR controller, which connects the SOC's differential clock to two DDR-memory chips. Differential signals CLK and CLK− from SOC chip IC_1 connect to series resistors R_1 and R_2, respectively. The differential traces then connect to DDR-memory chips IC_2 and IC_3 with a 120Ω termination resistor near IC_2.

Figure 2 shows the equivalent PCB (printed-circuit-board) layout. The PCB comprises a four-layer FR4 material with a ground plane under differential lines CLK and CLK−. The CLK and CLK− signals are routed close to each other and pass through series resistors R_1 and R_2, which are also placed close to each other, to provide proper termination. The closely spaced differential signals connect to

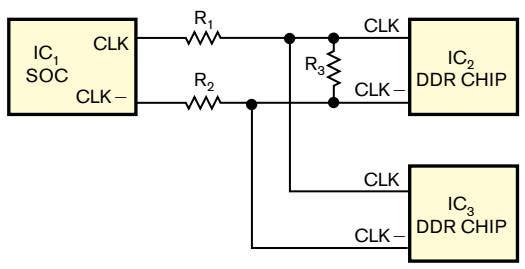

Figure 1 This circuit for an SOC-differential-clock source drives two DDR chips.

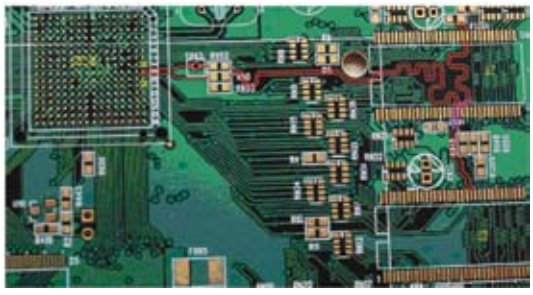

Figure 2 The bare PCB shows the differential-signal traces from the SOC to IC_1 and IC_2.

IC_2 with the 120Ω termination resistor, R_3. The bottom-layer traces are necessary to connect the differential signals to IC_3. The total length of the differential pair is approximately 2.5 in. from the SOC chip to the DDR chips.

The SOC provides DDR differential clocking. With various values for R_1, R_2, and R_3, the best results occur when R_1 and R_2 are 0Ω and R_3 is unconnected. Figures 3 through 7, which are available with the Web version of this Design Idea at www.edn.com/090205dia, show various waveforms for the signals. EDN

Flying capacitor and negative time constant make digitally programmable-gain instrumentation amplifier

W Stephen Woodward, Chapel Hill, NC

Numerous and evil are the forces of darkness that conspire to frustrate accurate analog-to-digital conversion of wide-dynamic-range analog signals. Among these gremlins lurk common-mode-voltage noise and signal amplitudes too variable to fully use ADC-input span and conversion resolution. Proven charms against common-mode noise are differential inputs, and you can exorcise variable signal amplitudes by implementing digitally programmable gain. DPGIAs (digitally programmable-gain instrumentation amplifiers) combine both useful features (**Figure 1**).

Microcircuit—even monolithic—DPGIAs, such as the Linear Technology (www.linear.com) LTC6915, are available. But this Design Idea describes a DDENT (differential-divergent-exponential-negative-time-constant) DPGIA employing the concepts of the "flying"-capacitor differential input and the DDENT curve, which provide an interesting alternative.

You control DDENT operation with the amplify/$\overline{\text{track}}$-bit mode. Track mode connects flying-capacitor C to the positive and negative differential-input terminals, which acquire the input voltage, V_{IN}. The transition to the amplify mode isolates C from the input and initiates regenerative negative-time-constant exponential amplification of the input voltage. From that point (**Reference 1**) until the moment when a connected ADC ultimately samples and converts the

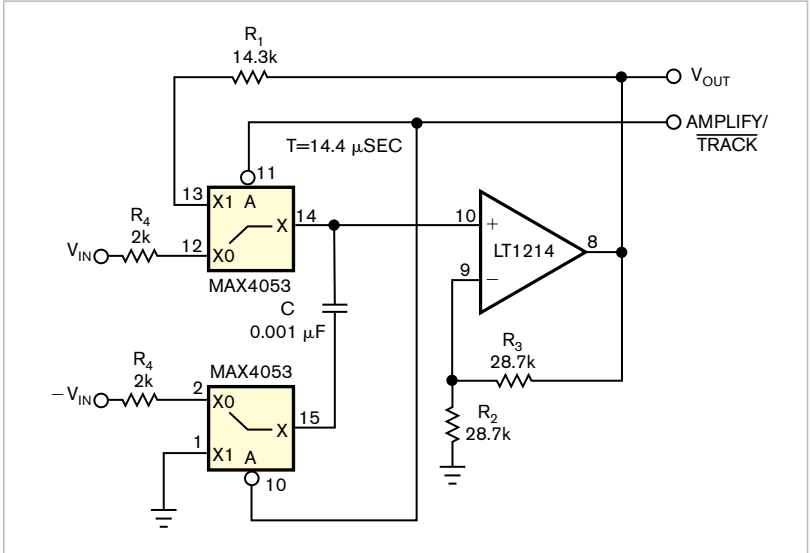

Figure 1 The behavior of the RC topology is still simple when you replace the resistors with an active circuit that synthesizes a negative resistance.

output voltage, V_{OUT}/V_{IN} is a divergent exponential function of time: gain$=2^{(t/10\ \mu sec+1)}$.

Building on the assets of that earlier design, this new circuit features CMR (common-mode rejection) that neither resistor-network matching nor the CMR of the op amp limits. Stray-capacitance issues impose the only limits, but you can minimize these issues with careful circuit layout. The circuit has rail-to-rail inputs, virtually unlimited programmable gain, and gain-set resolution that only the resolution of the amplify-interval timing limits. The circuit also has settling time 10 to 100 times faster than that of the exemplary LTC6915 and ±10V output-amplitude capability—two to four times greater than that of monolithic DPGIAs. Besides the inherent dc accuracy of the op amp you choose, the accuracy and repeatability of the timing of exponential generation, ADC sampling, and RC-time-constant stability are the only limits on the amplifier's signal-processing performance and precision. In the sample circuit, in which T=14.4 µsec, 1 nsec of amplify-timing error or jitter equates to 0.007% of gain-programming error. EDN

THIS NEW CIRCUIT FEATURES CMR THAT NEITHER RESISTOR-NETWORK MATCHING NOR THE CMR OF THE OP AMP LIMITS.

REFERENCE

1 Woodward, W Stephen, "Digitally programmable-gain amplifier uses divergent-exponential curve," *EDN*, Jan 8, 2009, pg 49, www.edn.com/article/CA6625454.

MOSFET prevents battery damage

Santosh Bhandarkar, Wep Peripherals, Mysore, India

Sealed-lead-acid batteries, which find wide use in power-electronics products, such as UPS (uninterruptible-power supplies), inverters, and emergency lamps, supply power to the load whenever utility power is unavailable. When you restore utility power, a charger supplies the power to the load and charges the batteries (**Figure 1**).

You can add a diode to protect a load from current resulting from a reverse-connected battery. The diode, however, won't protect a reverse-connected battery from the charger circuit. If the charger is on, a potentially dangerous current can flow into a reverse-connected battery. The battery voltage, which normally opposes the charging voltage, now aids it, which lets a higher current flow into the battery.

If you add an N-channel MOSFET to the circuit, you can protect the battery from this damaging condition (**Figure 2**). The MOSFET conducts only when the battery is correctly connected, which lets the battery charge or discharge. In this condition, the transistor gets forward-biased, which switches on the MOSFET. If the battery is reverse-connected, the transistor and MOSFET turn off, thus preventing current flow. This simple circuit provides reverse-battery protection in both charger and battery paths, thereby protecting the battery, the charger, and the load. You can use a microcontroller to measure battery current and make a decision on appropriate action, as well. EDN

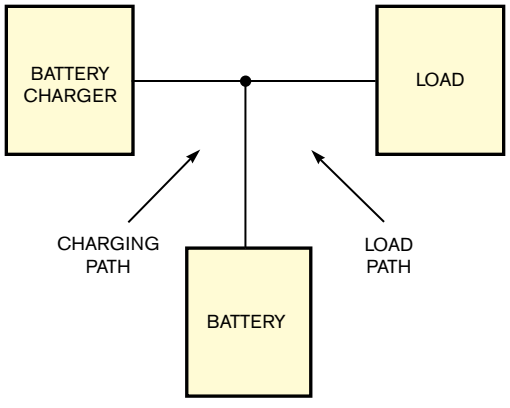

Figure 1 Batteries provide power to a load when utility power is off.

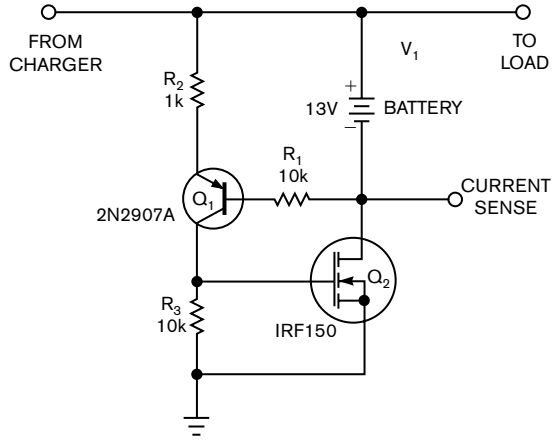

Figure 2 MOSFET Q_2 protects the battery from excessive current.

Voltage doubler improves accuracy

S Chekcheyev, Tiraspol, Moldova

The voltage doubler in **Figure 1** provides more accurate voltage doubling than does the conventional voltage doubler in **Figure 2** because it uses transistors instead of diodes. You can express the output voltage of the conventional doubler as $V_{OUTDC}=2V_{INAC}-2V_D$, where V_{OUTDC} is the output dc voltage, V_{INAC} is the amplitude of the input ac voltage, and V_D is the voltage across the forward-biased diodes. The error of the conventional voltage doubler is $2V_D$. Transistors Q_1 and Q_2 in **Figure 1** are saturated during the positive and the negative half-cycles, respectively, of the input ac voltage. The operation of the saturated transistors is similar to the operation of the forward-biased diodes in **Figure 2**. The collector-emitter voltage of the saturated bipolar transistors, however, is substantially smaller than the voltage across the forward-biased diodes. Thus, the error of doubling decreases.

Transistors Q_1 and Q_2 are reverse-biased during the negative and the positive half-cycles, respectively. The reverse beta of the bipolar transistors is small; consequently, the operation of the reversed transistors in **Figure 1** is similar to the operation of the reverse-biased diodes in **Figure 2**. Both circuits underwent tests with a resistive load of 10 kΩ and a 50-Hz, 2V-amplitude sinusoidal signal applied to the input. The measured output voltage of the conventional voltage doubler was 2.8V, and the error of doubling was 2×2V−2.8V=1.2V. The measured output voltage of the proposed voltage doubler was 3.8V, and the error of doubling was 2×2V−3.8V=0.2V. EDN

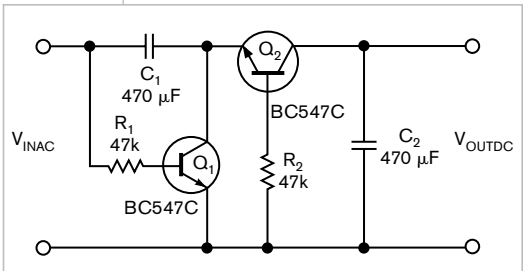

Figure 1 An improved voltage doubler uses transistors for better accuracy.

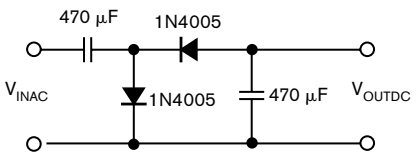

Figure 2 A conventional voltage doubler uses diodes.

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designideas

READERS SOLVE DESIGN PROBLEMS

Digital controller compensates analog controller

David Caldwell, Flextek Electronics, Carlsbad, CA

Emerging digital ICs for power control lack basic features, such as the built-in gate drive and current limiting, that you would normally find in analog ICs. Digital-power controllers generally have only PWM (pulse-width-modulated)-logic output, and discrete gate drivers rarely include current limiting. In addition, most protected FETs work only in low-frequency, low-side applications.

The LM3485 IC from National Semiconductor (www.national.com) includes high-side gate drive with current limiting (**Reference 1**). However, the hysteretic-control scheme of this analog IC is likely to yield questionable performance in some applications due to variable switching frequency and overshoot, as well as an inability to regulate feedback below the 1.24V reference. A traditional PID (proportional-integral-differential)-control scheme can get around these limitations but adds considerable complexity.

The CLZD010 CLOZD (Caldwell-

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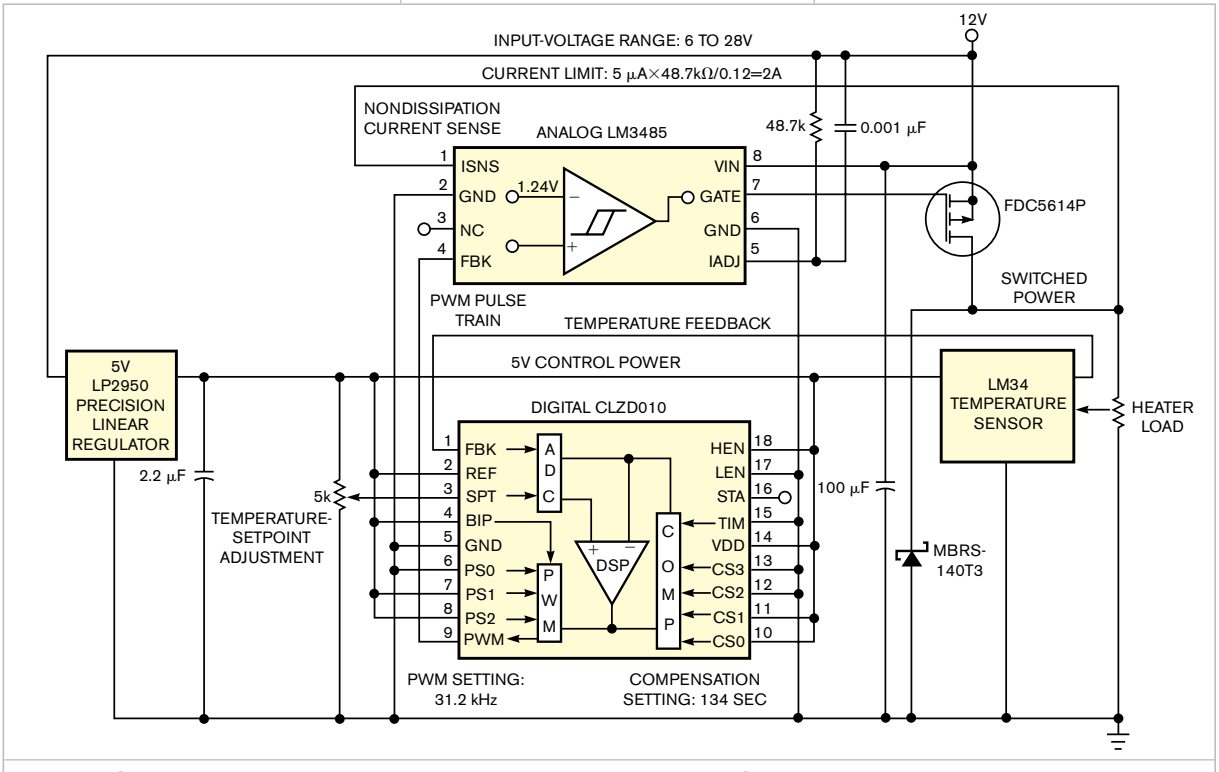

Figure 1 Combine the simple and robust closed-loop control of the digital CLZD010 with the current-limited high-side gate drive of the analog LM3485 for the best of both worlds.

loop-optimization-in-Z-domain) controller-chip IC from Flextek Electronics (www.flex-tek.com) both broadens and simplifies control applications though the embedded intelligence of a digital device (**Reference 2**). A single time-domain compensator replaces the three frequency-domain PID parameters, eliminating complex stability analysis. The circuit requires no PC interface because you inspect the open-loop response and then use pin settings to configure the closed-loop compensation. However, the PWM output is only a logic-level driver.

Combine the simple and robust closed-loop control of the digital CLZD010 with the current-limited high-side gate drive of the analog LM3485 for the best of both worlds (**Figure 1**). The PWM-logic level of the digital IC overrides the hysteretic comparator of the analog IC to switch the FET. A second comparator at ISNS, Pin 1 in the LM3485, turns off the FET if the voltage across it exceeds a predetermined value during conduction to limit current.

In the thermal-response example (**Figure 2a**), the circuit takes about three minutes for the open-loop temperature to reach roughly two-thirds of its final value, so closed-loop compensation, at 134 seconds, is slightly faster in **Figure 1**. The resultant closed-loop temperature quickly nears its final value due to maximum drive; voltage then decreases to allow the temperature to settle at the setpoint without overshoot (**Figure 2b**). You can use this basic circuit combination to satisfy a broad range of applications in multiple industries. EDN

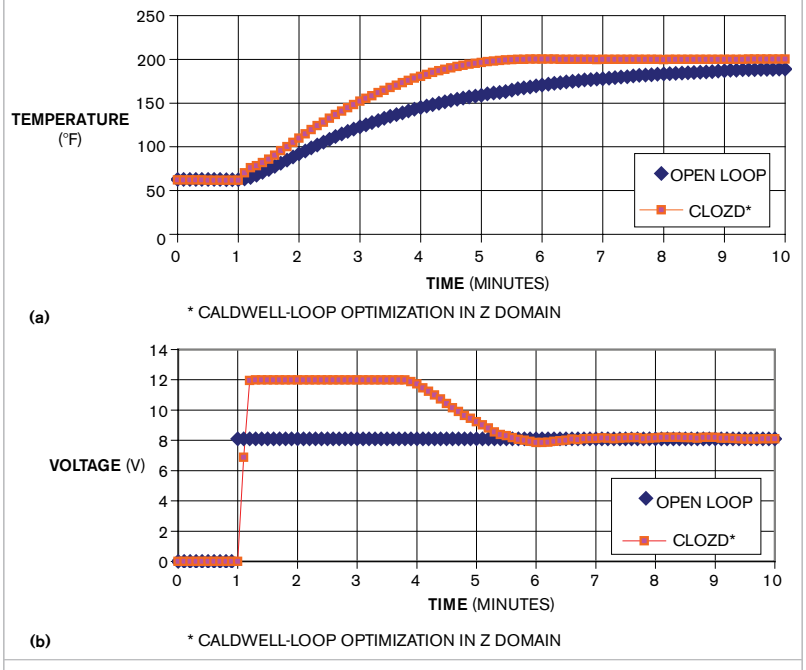

Figure 2 In the thermal-response example (a), the circuit takes about three minutes for the open-loop temperature to reach roughly two-thirds of its final value. The resultant closed-loop temperature quickly nears its final value due to maximum drive; voltage then decreases to allow the temperature to settle at the setpoint without overshoot (b).

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1 "LM3485 Hysteretic PFET Buck Controller," National Semiconductor, September 2004, www.national.com/ds/LM/LM3485.pdf.
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Circuit provides constant-current load for testing batteries

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Suppose that you need to test a 1.5V, AA-size alkaline battery. You can apply a short circuit and measure current, or you can measure open-circuit voltage, but neither method properly tests the battery. A suitable test current of approximately 250 mA gives you a more reasonable test. You can use a 6Ω resistive load at 1.5V, which produces an output voltage of 1.46V at an ambient temperature of 25°C if the battery is in excellent condition. A poor battery might produce less than 1.2V. Given the load, the output current at 1.2V will be 200 mA instead of 250 mA. The battery will have just 80% of a full load current. Instead, you can use the circuit in **Figure 1** to produce a constant-current load.

The circuit uses a 9V battery and a voltage regulator to produce a steady power-supply voltage of 5V. From that voltage, the circuit produces a constant sink current, which is independent of the battery's output voltage, using IC_1, IC_2, and Q_3. Your choice of current depends on battery size. You calculate the sink current of this circuit as $I_{TEST} = 1/R_{19} \times [V_{CC} \times R_{18}/(R_4+R_{18})]$, where I_{TEST} is the current you are testing and V_{CC} is the voltage of resistive divider R_4 and R_{18}.The voltage across R_{19} should range from 0.3 to 0.85V for AAA and AA batteries. Transistor Q_3 should be in its active region. Resistor R_{14} limits Q_3's base current to a safe level.

A suitable choice for the operational amplifier, IC_2, is also important. You should use a single-supply op amp with a rail-to-rail input and a rail-to-rail output, such as Analog Devices' (www.

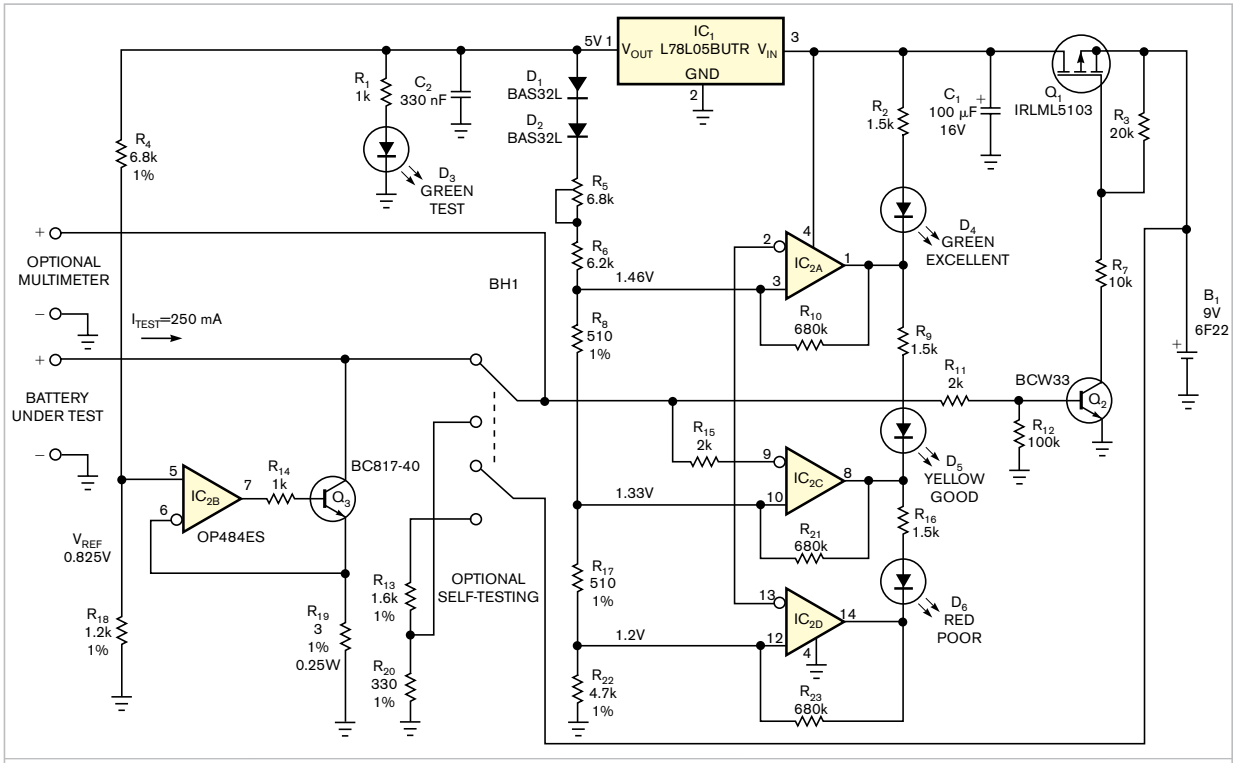

Figure 1 A tester of AA- or AAA-sized batteries uses constant-current load.

TABLE 1 VOLTAGE RANGES FOR LEDs

Condition	Battery voltage[1] (V)	D_2	D_4	D_5	D_6	D_3
Excellent	>1.46	Yes	Yes	No	No	Yes
Good	>1.33	Yes	No	Yes	No	Yes
Poor	>1.2	Yes	No	No	Yes	Yes
Bad	>1[2]	Yes	No	No	No	Yes
Unable to test	>12	No	No	No	No	No

[1]Ambient temperature is 25°C.
[2]This estimated value can be less.

analog.com) OP484ES or OP496GS.

When you connect the battery under test, Q_2 turns on, which then turns on Q_1, applying voltage from the 9V battery to the regulator. That action lights D_3, indicating that the battery under test has enough voltage to be tested. LEDs D_4, D_5, and D_6 indicate the battery's condition. **Table 1** shows the voltage ranges necessary for these LEDs to light.

Op amps IC_{2A}, IC_{2C}, and IC_{2D} work as comparators with some hysteresis for operational stability. The resistive divider comprising R_5, R_6, R_8, R_{17}, and R_{22} sets the voltage levels. Diodes D_1 and D_2 are optional but are useful when you need to operate the circuit outdoors, where temperatures vary widely. Resistor R_{15} protects the inputs of IC_{2A}, IC_{2C}, and IC_{2D}.

When you connect a battery to test, you should test it for at least 5 seconds. LED D_3 shines if the battery is in relatively normal condition. In this case, switch Q_1 applies power to the battery tester. The sink-current generator comprising IC_{2A} and Q_3 loads the battery under test, and the resistor-divider network sets the comparator voltages.

You can add an optional self-testing button for checking the 9V battery to ensure that it has enough voltage to drive the circuit. You can also connect a digital multimeter to the multimeter terminals if you need a more accurate measurement. You can use a suitable rotary switch or a variable resistor and change the value of the test current by changing the value of R_4 to test another type or size of battery. EDN

MOSFET-based, analog circuit calculates square root

Abhirup Lahiri, Netaji Subhas Institute of Technology, New Delhi, India

Square-root-calculating circuits find wide use in instrumentation and measurement systems for such tasks as calculating the rms (root-mean-square) value of an arbitrary waveform, for example. Hence, designers need an effective analog square-root calculator. Because manufacturers do much of the IC fabrication in MOS technology, a MOSFET-based, analog square-root calculator seems appropri-

ate. This Design Idea describes such a circuit, which uses only MOSFETs to provide the square-root function (**Figure 1**). The design is simple and versatile and can provide the output as the square root of the difference of two voltages.

The circuit uses the nested connection of MOSFETs Q_1 and Q_2. Q_2 works in the saturation region as it is diode-connected, forcing Q_1 to work in the triode region. All other MOSFETs work in the triode region. The first part of the circuit, comprising Q_3, Q_4, Q_5, and Q_6, creating the current I_{O1}, is basically a MOS-resistive circuit. The essential **equation** governing the circuit operation is:

$$V_O = \left(\sqrt{\frac{1}{K_2}} - \sqrt{\frac{1}{K_1}}\right)\sqrt{I_{O1}},$$

where K_1 and K_2 represent the aspect ratios of transistors Q_1 and Q_2, respectively: $K_1 = (\mu C_{OX} W)/2L_1$, where $I = K_1 = K_2$. The MOSFETs creating the MOS-resistive circuit and hence responsible for the current creation are identical, having the same aspect ratio and threshold voltage. The current relates to inputs V_1 and V_2, as the following **equation** shows: $I_{O1} = G(V_1 - V_2)$, where $G = 2K(V_A - V_B)$ and represents the conductance of the MOS-resistive circuit—$k = (\mu C_{OX} W)/2L$—of the identical transistors forming the MOS-resistive circuit, and V_A and V_B are control voltages applied to the gate of the MOSFETs that are working in the triode. This approach provides the advantage of voltage controllability of the output; hence, the square-rooting function is voltage-controllable.

The following **equation** gives the output voltage:

$$V_O = 2\left(\sqrt{\frac{1}{K_1} + \frac{1}{K_2}} - \sqrt{\frac{1}{K_2}}\right) \times$$

$$\sqrt{K(V_A - V_B)(V_1 - V_2)}.$$

It is evident from this equation that the output voltage, V_O, is the square root of the difference of input voltages V_1 and V_2. If you ground V_2, then the output voltage is proportional to the square root of input voltage V_1. As noted, control voltages V_A and V_B can vary the proportionality constant. Hence, you have devised a new all-MOSFET-based, voltage-controllable analog square-root calculator.

You can test the circuit using a variety of commercially available MOSFETs, such as the 2SK1228, which is available from many sources; the buffer can be a MOSFET-based op-amp buffer, such as the BUF04701 from Texas Instruments (www.ti.com). For the operation of the circuit to be in accordance with the output-voltage **equation**, the four MOSFETs you use to create the MOS-resistive circuit should be identical and should work in the triode region, for which inputs V_1 and V_2 should be less than $V_A - V_{TH}$ and $V_B - V_{TH}$, respectively. The MOSFETs in the current mirror, Q_7 and Q_8, should be identical, and the diode-connected MOSFETs, Q_1 and Q_2, should be different and have different aspect ratios. You can test the circuit onboard using commercially available ICs, or you can simulate it on a computer using any standard version of Spice. The supply voltage must be in accordance with the selected components. EDN

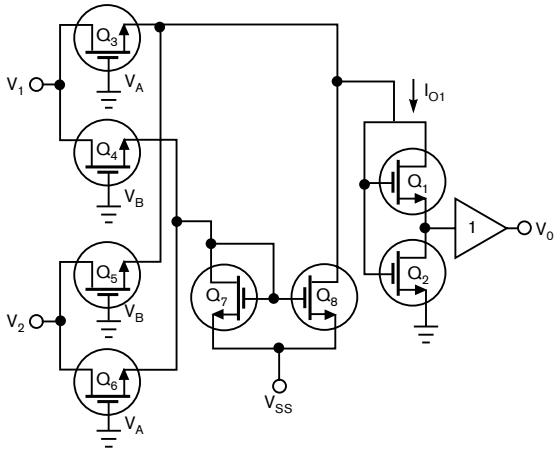

Figure 1 This circuit uses only MOSFETs to provide the square-rooting function.

"Hippasian" nonlinear VFC stretches dynamic range

W Stephen Woodward, Chapel Hill, NC

Hippasus of Metapontum was a Greek philosopher who lived approximately 500 BC. A disciple of Pythagoras, Hippasus discovered some interesting properties of square roots. This Design Idea describes a VFC (voltage-to-frequency converter) that also uses an interesting property of square roots: their ability to extend VFC dynamic range by orders of magnitude (**Figure 1**).

Linear VFCs are one of the oldest types of ADCs, and their simplicity and noise rejection preserve their popularity. However, their Achilles' heel is the direct proportionality between dynamic range and conversion time. Because the voltage resolution of linear VFC conversion is equal to the full-scale voltage reference, V_{REF}, divided by full-scale frequency, f_{FS}, multiplied by the counting interval, large dynamic range is inevitably associated with long counting intervals and slow conversion, even when clever VFC design provides for fast full-scale frequency.

For example: If you use a 3-MHz VFC-based ADC, such as Analog Devices' (www.analog.com) AD7742 with a 2.5V reference voltage in a design that requires 1-mV resolution, then

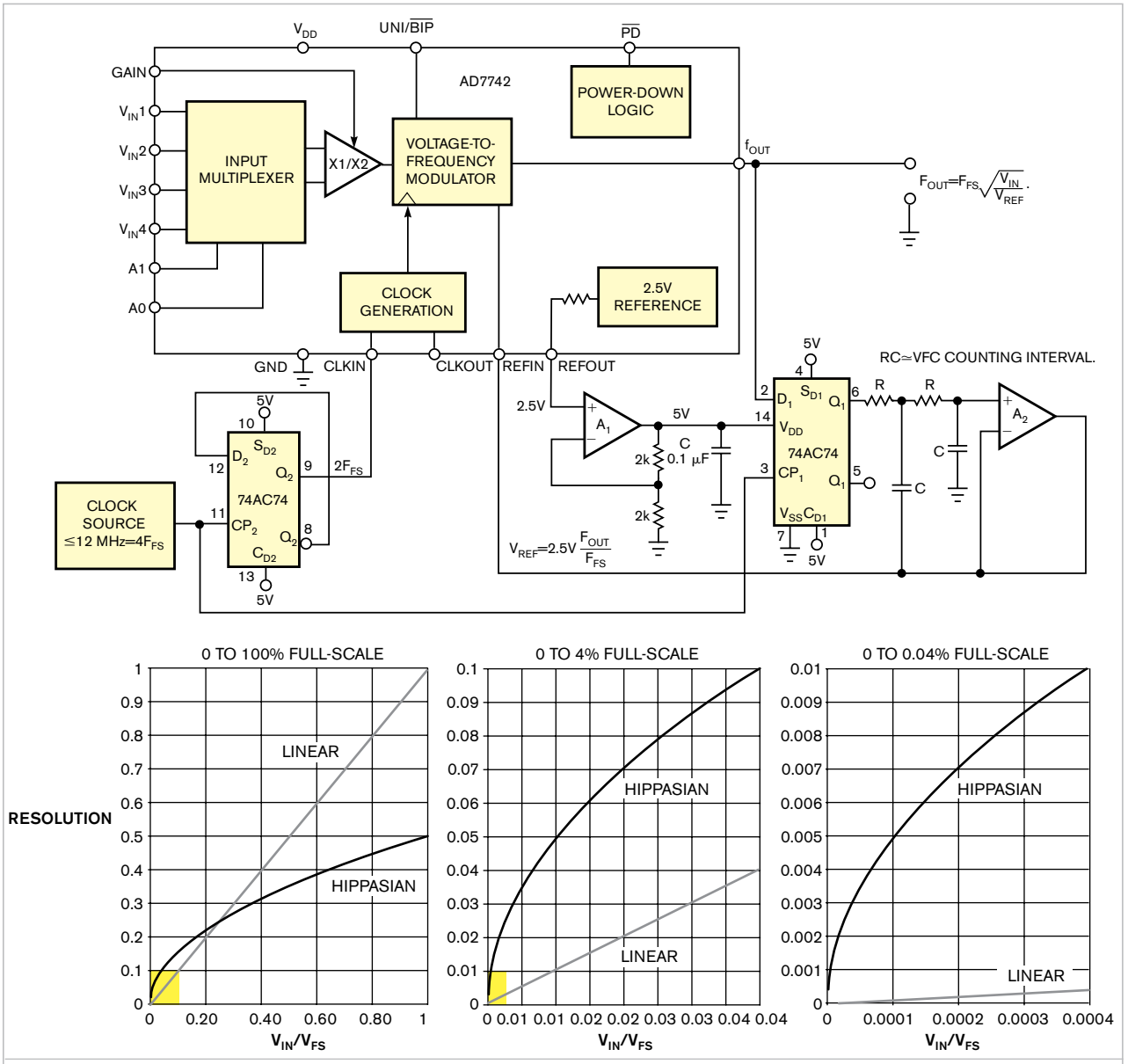

Figure 1 This nonlinear, wide-dynamic-range voltage-to-frequency converter exhibits 25-times improvement in counting time over other approaches.

you would need a minimum counting interval of 2.5/1 mV/3 MHz=2500/3 MHz=833 µsec. That counting interval yields only 1200 conversions per second, which for many applications is inconveniently slow.

The "Hippasian" VFC avoids this problem with a semiparabolic-transfer function instead of a linear one. It works by substituting V_{REF2}, which, instead of the constant V_{REF} of a linear VFC, is proportional to the output frequency. Then, $V_{REF2}=V_{REF}\times f_{OUT}/f_{FS}$, $f_{OUT}=V_{IN}\times f_{FS}/V_{REF2}=V_{IN}\times f_{FS}/(V_{REF}\times f_{OUT}/f_{FS})$, $(f_{OUT}/f_{FS})^2=V_{IN}/V_{REF}$, and $f_{OUT}=f_{FS}\times(V_{IN}/V_{REF})^{1/2}$.

Generating the dynamic, output-frequency-proportional reference voltage is the job of op amps A_1, which boosts the VFC's internal 2.5V reference to power flip-flop Q_1, and Q_1 and A_2, which compose a high-performance frequency-to-voltage converter. The accuracy of the reference voltage depends on precise 50-to-50 symmetry of the VFC's input-clock reference. Flip-flop Q_2 guarantees this symmetry.

The effect on conversion resolution of low-level signals is dramatic. To return to the example of a 2.5V full-scale, 1-mV-conversion resolution, which requires a 2500-count, 833-µsec conversion interval with a linear 3-MHz VFC, the Hippasian version needs only 100 counts and 33 µsec—a 25-fold improvement. Software linearization of the Hippasian VFC conversion is easy, requiring only one multiplication. EDN

Decoder lights the way

Jean-Bernard Guiot, Mulhouse, France

To display the status of two digital outputs, you can simply connect an LED and its resistor on each output. You must, however, interpret, or "decode," the displayed binary code. In addition, when no LED lights, users have no way of knowing whether it means that both outputs are off, that the power is off, or that a malfunction has occurred. In some applications, including industrial and medical settings, an indicator sending an ambiguous signal would be unacceptable. This Design Idea describes a simple circuit that resolves this problem by displaying four states on four LEDs (**Figure 1**). The operator need not understand binary coding, and, if no or more than one LED lights, it can mean only "no power" or "default."

The circuit works in the following way: If both inputs A and B are low, Q_1 allows current to pass through D_1 and resistor R_2 to A; only D_1 will light. Symmetrically, if both inputs A and B are high, Q_2 passes, and the current can pass from A through R_4, Q_2, and D_4; only D_4 will light. If both inputs are on different levels, only D_2 or D_3 will light. **Table 1** shows the possibilities; all other displays point to a default, such as a bad connection, a no-power condition, or a malfunction.

A totem-pole output that can sink and source the current for one LED must drive the A and B inputs. Resistors R_2, R_3, and R_4 are for applying a 12-mA LED current if the power supply is 5V. No component is critical. For example, you can use generic transistors, such as the NPN 2N3904 and the PNP 2N3906. You can even use transistors with integrated base resistors, further reducing the component count. EDN

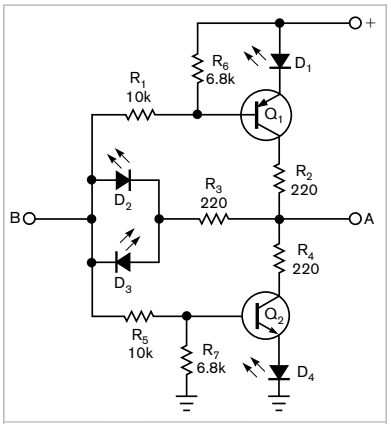

Figure 1 This simple circuit displays four states on four LEDs.

TABLE 1 LED-LIGHTING POSSIBILITIES

IN		LED			
A	B	1	2	3	4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Microcontroller converts digital-temperature-sensor readings without floating-point arithmetic

Jordan Dimitrov, Toronto, ON, Canada

Digital temperature sensors combine a sensor, an ADC, and a serial interface in a single chip. They feature wide enough measurement range, good accuracy and resolution, no need of external parts, easy interface to microcontrollers, small size, and low price. In a review of 10 digital sensors from seven companies, all parts deliver signed-number data in two's-complement format. They feature temperature ranges of −25 to +85 or −40 to +125°C, accuracy of 0.5 to 2 or 2 to 4°C, and output data of 9 to 13 bits with 0.5 to 0.0312°C resolution. The devices' conversion time is 26 to 750 msec, and they use an SPI (serial-peripheral interface), an I²C (inter-integrated-circuit), or a 1-Wire interface. Power supplies are 1.5 to 3.6 or 3 to 5.5V, and prices range from 80 cents to $2.10 (1000).

These sensors connect to microcontrollers; hence, size, speed, and time to develop firmware are also important. The standard approach is to use a high-level language and a compiler. Development time is short, and performing even complex calculations is not a problem. However, compilers produce machine code that occupies more memory and runs at lower speed than code from an assembler. Also, compiler IDEs (integrated development environments) cost hundreds of dollars, whereas many companies offer free assembly-language IDEs. If you work on a tight budget or memory-space allotment, assembly language is the better option. The problem is to find a simple way to avoid the necessary floating-point calculations to convert sensor data into human-understandable format, both in Celsius and Fahrenheit. This Design Idea presents an effective approach.

Consider the TMP121 sensor from Texas Instruments (www.ti.com). It provides 13-bit data in a 16-bit frame with resolution of 0.0625°C/bit. Hence, the transfer function is $t_C=0.0625\times N_S$, where t_C is the temperature in degrees Celsius and N_S is the sensor data after you remove the three meaningless least-significant bits. You can easily rearrange the above **equation** to:

$$t_C=\frac{5}{80}\times N_S=\left(\frac{N_S}{2}+\frac{N_S}{8}\right)\times\frac{1}{10}. \quad (1)$$

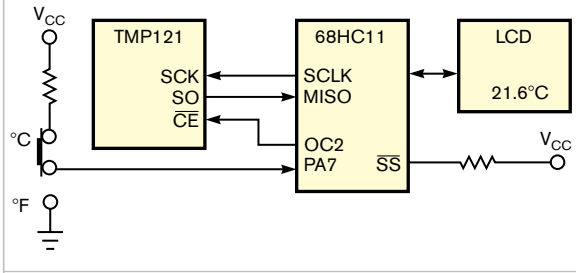

Figure 1 A small system uses a 68HC11 microcontroller to read a switch and a sensor, to convert data, and to display temperature.

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To get readings in degrees Fahrenheit, use the following **equation**, which converts degrees Celsius into degrees Fahrenheit: $t_F=[(9/5)\times t_C+32]$. Replacing t_C from the above **equations** yields:

$$t_F=\frac{9}{5}\times\frac{5}{80}\times N_S+32=\left(N_S+\frac{N_S}{8}+320\right)\times\frac{1}{10}. \quad (2)$$

The benefit of **equations 1** and **2** is that you can perform the calculations with integer arithmetic only. They require divisions by powers of two, which you can replace with shifts, and division by 10, which you perform by introducing a decimal point in the display.

The circuit underwent testing with the popular 68HC11 microcontroller from Motorola (www.motorola.com, **Figure 1**). Besides a sensor and a controller, it includes a unit-selection switch and a dot-matrix LCD. The display resolution is 0.1°. The core of the supporting firmware is an endless loop in which the 68HC11 uses an output-compare function to generate a square-wave signal with a

period of 1 sec and a duty cycle of 50%. The OC2 signal connects to the $\overline{CE}$ input of the sensor and controls its operation: When $\overline{CE}$ is high, the sensor measures temperature. The HC11 does nothing except display M on the LCD. When $\overline{CE}$ becomes low, the last measurement latches in a shift register inside the sensor. The HC11 deletes M from the display, reads the switch and the sensor, manipulates the data, and displays the temperature.

Equations 1 and **2** provide the basis for two source codes. **Listing 1**, available at www.edn.com/090305dia, generates machine code of 981 bytes. **Listing 2**, also available at www.edn.com/090305dia, generates machine code of 392 bytes. Despite the C-language approach with integer arithmetic, it needs 2.5 times more memory to do the job. The ratio is well above 10 if the C code goes with equations that need floating-point arithmetic. The benefit is clear: Modified **equations 1** and **2** and assembly-language programming let you select a microcontroller with less memory and reduce the price of your design. EDN

Discrete-component buck converter drives HB LEDs

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HB (high-brightness) LEDs require a large amount of current to operate. When driving HB LEDs from a voltage source, you can set the required current with a suitable series resistor. If the voltage source is a battery, then, as the battery drains, the LED's intensity decreases. Also, a series resistance has the disadvantage of power loss through the resistor. A better option is to use a suitable dc/dc converter. If the LED's turn-on voltage is lower than the battery voltage, as would be the case with a 6V sealed-lead-acid battery, then you can use a buck converter (**references 1** and **2**). You can build a simple buck converter using only discrete components. It requires two bipolar transistors, a P-channel MOSFET, an inductor, a Schottky diode, and a few resistors (**Figure 1**).

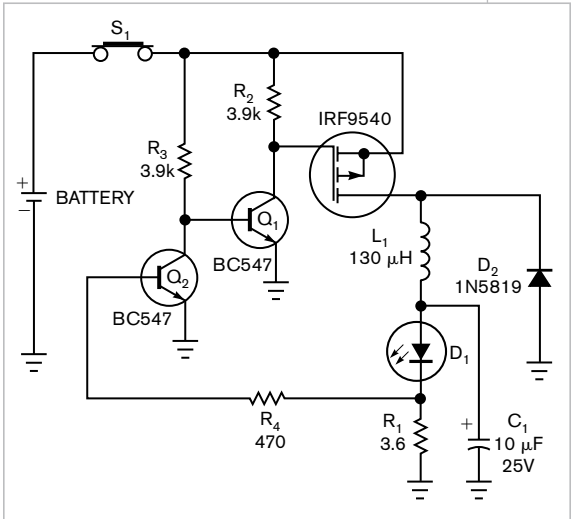

Figure 1 A buck converter provides current sufficient to drive a high-brightness LED.

When you switch on the battery voltage, the voltage across R_1, the resistor in series with the HB LED, is 0V. Thus, transistor Q_2 is off, and Q_1 is in saturation. The saturated state of Q_1 switches on the MOSFET, thereby applying the battery voltage to the LED through the inductor. As the current through resistor R_1 increases, it turns on Q_2, which turns off Q_1 and thus turns off the MOSFET. During the MOSFET's off state, the inductor continues to supply current to the LED through Schottky diode D_2. The HB LED is a 1W, white Lumiled (www.philipslumileds.com) LED. Resistor R_1 helps control the LED's

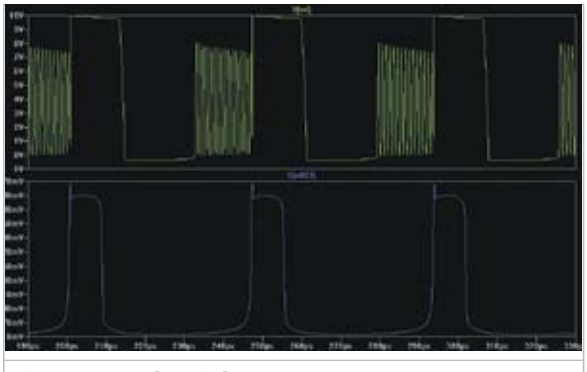

Figure 2 In a SwitchCAD simulation, the upper trace is the MOSFET-drain voltage, and the lower trace is the base voltage of Q_1.

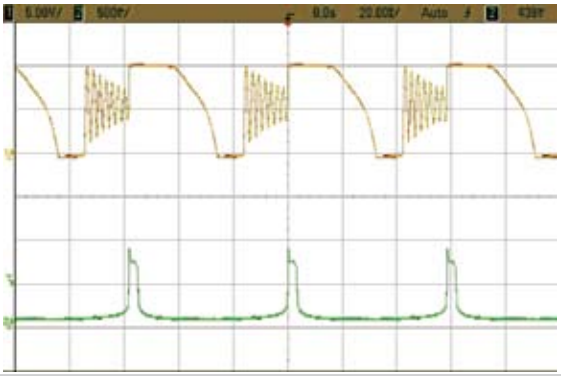

Figure 3 In an oscilloscope screenshot, the upper trace is the MOSFET-drain voltage; the lower trace is Q_1's base voltage.

intensity. Using a larger value for R_1 reduces the intensity.

The SwitchCAD-III software, which is available as a free download from Linear Technology (www.linear.com), simulated the circuit; the simulated MOSFET was an International Rectifier (www.irf.com) IRF9Z24S instead of an IRF9540 because the model for IRF9540 is not available in SwitchCAD-III. **Figure 2** plots the MOSFET-drain waveform and the voltage at Q_1's base. The circuit was wired on a prototyping board and tested for various supply voltages. **Figure 3** shows oscilloscope screenshots for the MOSFET-drain voltage and the voltage at the base of Q_1. They fairly well match the simulated waveform. Conversion efficiencies were 60 to 95% for supply voltages of 6 to 10V. EDN

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2 Gadre, Dhananjay V, "Buck regulator controls white LED with optical feedback," *EDN*, Oct 25, 2007, pg 72, www.edn.com/article/CA6491146.

Drive a single-coil latching relay without an H-bridge circuit

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Single-coil latching relays find use in signal-routing, audio, and automotive systems. To maximize their usefulness and cut power consumption, these coil currents must flow in both directions. Current flowing from the latching relay's positive pin to the negative pin causes it to latch in its reset position. Current flowing from the negative pin to the positive pin latches the relay in its set position. The relay maintains its position even when you remove the coil current, which saves power after the relay latches.

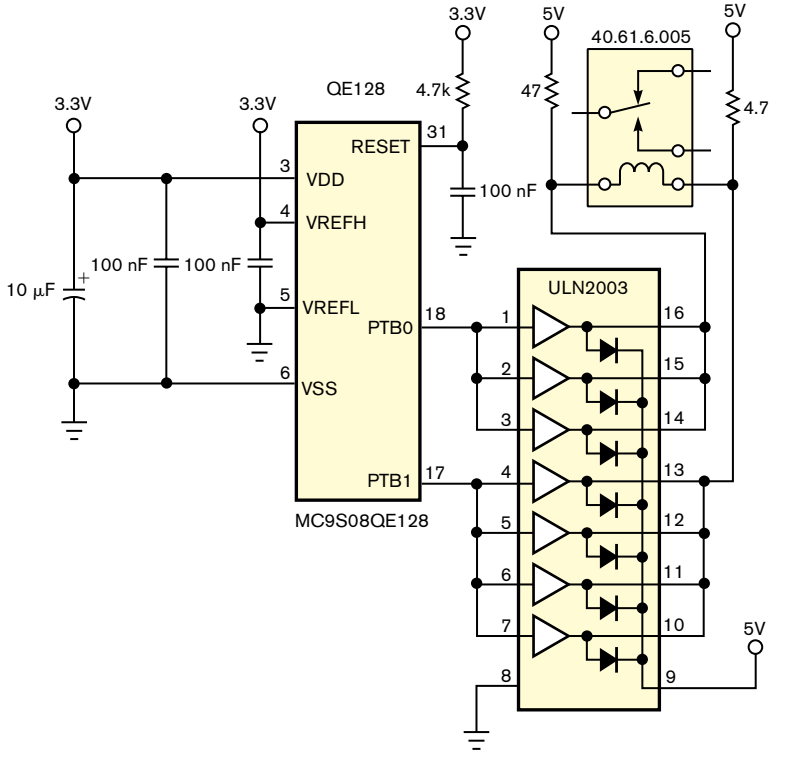

Figure 1 You can drive a single-coil latching relay without an H-bridge circuit, greatly simplifying hardware design and making the most of the low-power-consumption features inherent to latching relays in portable-system applications.

Latching relays have advantages over classic relays because, as soon as the relay switches, it remains in that position without consuming energy. Thus, no current consumption means less heat, smaller heat sinks, and a dramatic increase in battery life for portable devices. In some cases, the use of a latching relay lets your greatly simplify a circuit.

Although latching relays boast significant advantages over classic relays, their use appears limited to niche applications because they require more attention to design details. In general, a latching relay's drive circuit is slightly more complex than that of a classic relay. The traditional approach to driving a latching relay is to use an H-bridge circuit, which can be costly and difficult to handle. In addition, you must design a demagnetization circuit using a special resistor to limit the current in compliance with the manufacturer's specifications.

Figure 1 shows a simple circuit using the MC9S08QE128 microcontroller from Freescale (www.freescale.com) to drive a Finder (www.findernet.com) 40.61.6.005 single-coil latching relay with a standard ULN2003 Darlington driver with open-drain outputs and inductive-kickback protection. Clamping diodes on each ULN2003 output pin catch high-voltage transients that occur when you interrupt the coil current. Because demagnetization uses low-value resistors, you

must wire at least two open-drain buffers of the ULN2003 to both endings of the relay coil to ensure enough current when the microcontroller pulls down.

Listing 1, which is available in the Web version of this Design Idea at www.edn.com/090305dib, shows the software procedure to latch the relay to its set or reset position by turning on the corresponding microcontroller output for at least 50 msec. The current flows into the ULN2003 open-drain output and latches the relay to its set or reset position, according to the direction of the coil current. As soon as the relay latches, drive the corresponding microcontroller output low to turn off the ULN2003 open-drain buffer to ensure the lowest power consumption. You must, however, take into account the set/reset timing. Pull the microcontroller output low only after the required time has elapsed. Waiting ensures that the relay will properly latch to its intended position. EDN

Limit switches control dc-motor H bridge

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You use limit switches to switch off a motor if it reaches one of its two end positions. Even if you build a microprocessor-based motor controller, you should switch off a motor with hardware by building a safety interlock. Such a circuit works by inhibiting movement in one direction but allowing movement in the other direction when the motor retracts from its end position. **Figure 1** shows the circuit with mechanical switches. However, this ancient mechanical approach may be unsuitable in some cases because the motor cur-

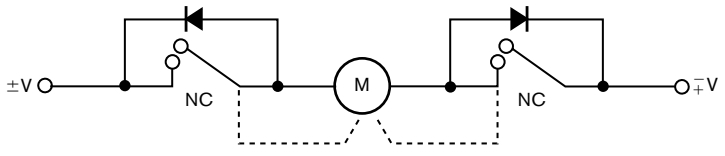

Figure 1 This circuit works by inhibiting movement in one direction but allowing movement in the other direction when the motor retracts from its end position.

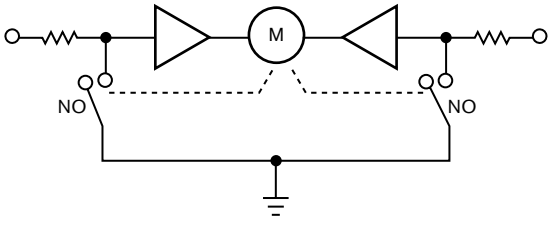

Figure 2 This circuit shortens one input of the H bridge to ground so that movement is possible only in the other direction by turning on the other input.

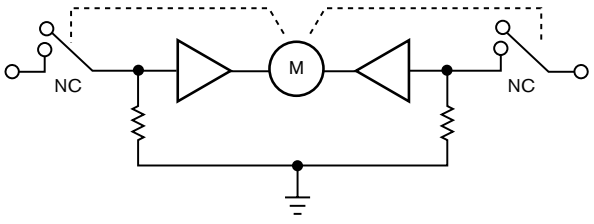

Figure 3 This circuit interrupts the connection to the driving circuit of one input and sets the input to low using a pull-down resistor.

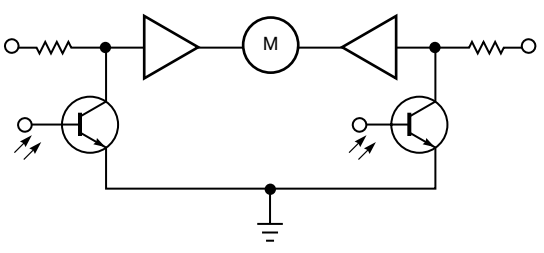

Figure 4 This circuit is the same as that in Figure 3, and it works with phototransistors without modification.

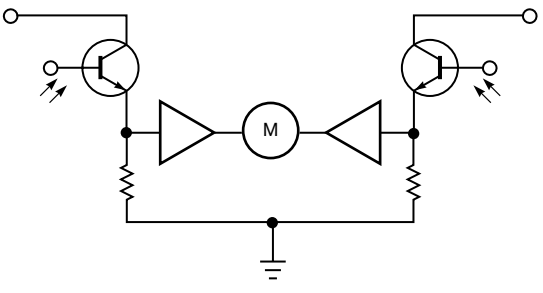

Figure 5 This circuit is the same as that in Figure 4; the value of the resistors depends on the parts you use.

rent may be too high, or the switches may be closing switches or light barriers.

If you use an H bridge to drive the motor, you can achieve the same operation in a more versatile way. The circuit in **Figure 2** shortens one input of the H bridge to ground so that movement is possible only in the other direction by turning on the other input. If the switches are opening at the end positions, the circuit in **Figure 3** interrupts the connection to the driving circuit of one input and sets the input to low using a pulldown resistor. The same circuit works with phototransistors without modification (**figures 4** and **5**). The value of the resistors depends on the parts you use; a value of 10 kΩ should work in most designs. EDN

Implement a clip-detection circuit for BTL Class D amplifiers

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Clip detection is a convenient feature in Class AB amplifiers. It produces a signal from a clip-detection pin that drives an automatic volume control, which reduces gain compression and distortion when the amplifier is overdriven. Class AB amplifiers, such as the STMicroelectronics (www.st.com) TDA7293, TDA7396, STA7360, and STA540 and the Toshiba (www.toshiba.com) TA8275 and TB29xx, have on-chip clip-detection circuits. Newer Class D automotive amplifiers, such as the four-channel STMicroelectronics TDA7454 and the Texas Instruments (www.ti.com) TAS5414/5424, have on-chip clip-detection circuits, but these ICs use a common clip-detection pin, comprising hardware ORed inside the IC, for all four channels. Other Class D amplifiers lack the clip-detection feature altogether, but you can implement it with external components.

An analog-input Class D amplifier comprises PWM (pulse-width-modulation) logic, gate-drive circuits, and a power stage. The PWM logic transforms the analog-input signal into a PWM signal. The power stage with

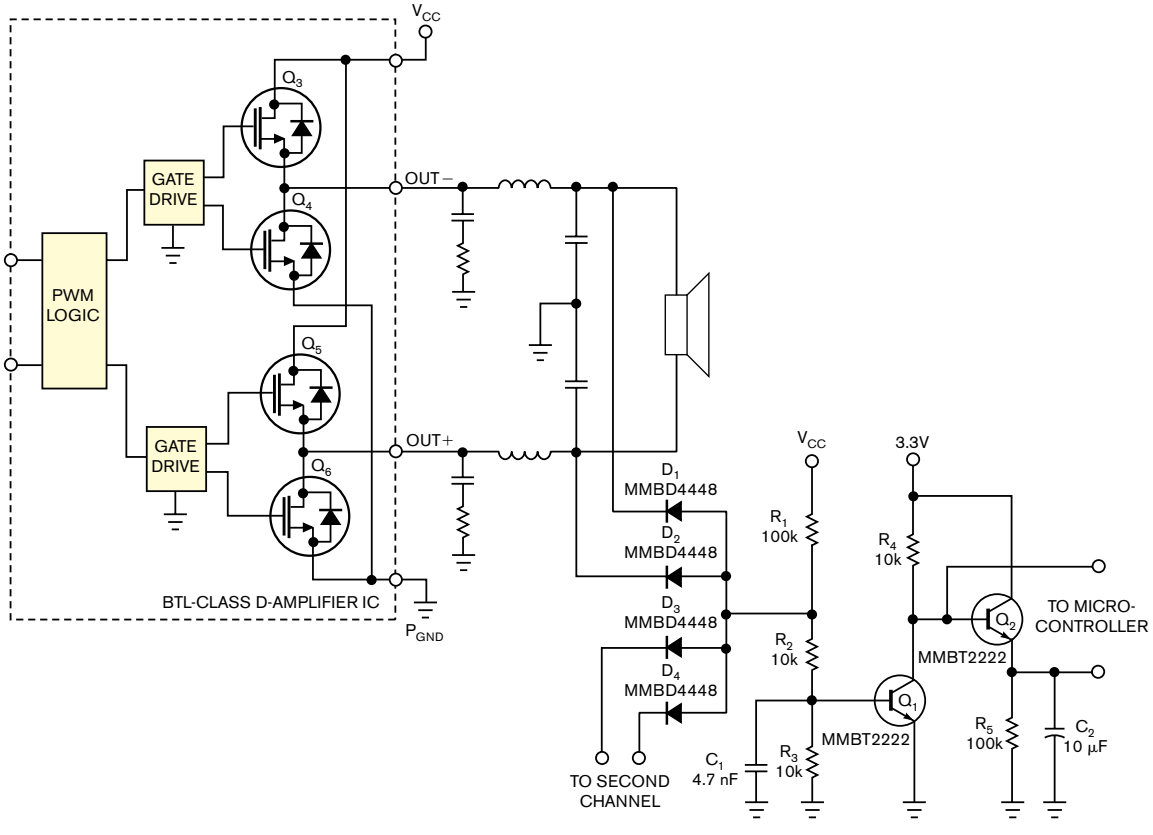

Figure 1 Adding several components to the BTL-Class D-amplifier IC provides a clip-detection function. A peak detector, comprising Q_2, R_5, and C_2, is optional.

the gate drivers transforms the low-power PWM signal into a high-voltage, high-current PWM sequence. A BTL (bridge-tied-load) amplifier basically comprises two gate-drive circuits and two power stages, which the same PWM signal drives. The signal directly drives one gate-drive circuit and phase-inverts the other. In theory, a BTL amplifier can produce four times more power into the same load than a single-ended amplifier.

Figure 1 illustrates the implementation of an external clip-detection circuit to a BTL-Class D-amplifier IC. The voltage swing on each output is symmetrical and is within the range of voltage drop on the on-resistance of MOSFET Q_6 to the common-collector voltage, V_{CC}, minus the voltage drop on the on-resistance of MOSFET Q_3. When the output voltage reaches a certain threshold, Q_1 turns off. The component values of R_1, R_2, and R_3 and the voltage drop across diodes D_1 through D_4 set this threshold, which is 0.5V with respect to power ground, P_{GND}, for the given component values. A positive-going pulse appears on the collector of Q_1 whenever the output voltage is below the threshold with respect to power ground. This pulse alerts the host microcontroller to the existence of clipping (**Figure 2**). Capacitor C_1 filters the residual of the switching- and high-frequency content of the audio signal.

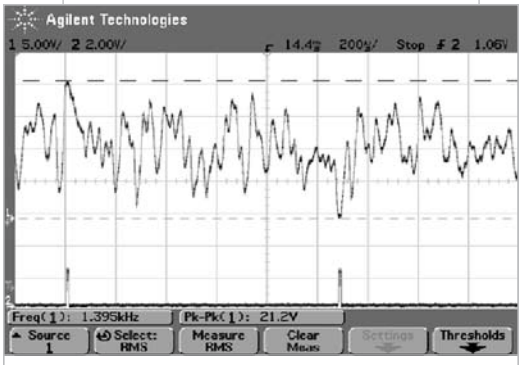

Figure 2 A positive-going pulse appears on the collector of Q_1 whenever the output voltage is below the threshold with respect to power ground.

A simple application involves filtering and integrating the pulses with further automatic reduction and restoration of the volume setting using the microcontroller's driven-volume control to counteract the clipping distortion. You can also implement more sophisticated algorithms (**Reference 1**). A suitable peak detector comprising Q_2, R_5, and C_2 allows the circuit to hold the short clipping pulses for a longer time. You can add LED circuitry to provide a visual clipping indication. EDN

REFERENCE

1 Person, Andrew P, and James P Muccioli, "Adjustable Clip Detection System," US Patent, 5,453,716, Sept 26, 1995, US Patent Office, http://patft.uspto.gov.

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READERS SOLVE DESIGN PROBLEMS

Buck converter uses low-side PWM IC

L Haachitaba Mweene, PhD, National Semiconductor Corp, Richardson, TX

The most common switching-power topology is a buck converter, which efficiently transforms high voltages to low voltages. **Figure 1** shows a typical buck converter in which the N-channel MOSFET, Q_1, needs a floating-gate drive signal. The floating-gate drive is part of the PWM (pulse-width-modulation) controller IC. Q_1 can be either N or P channel, depending on the controller's design. Unfortunately, the IC's voltage rating must be as high as the input voltage, which places a limit on the maximum voltage it can process.

The circuit in **Figure 2** uses a simple voltage-level shifter that lets a buck converter control a pass transistor with a low-side IC that has a ground-referenced gate drive. Because the level-shifting circuit in the PWM IC does not have to tolerate high voltages, you can implement a converter with an arbitrarily high input voltage.

PWM ICs with low-side gate drivers can power N-channel MOSFETs that are on when they have a positive gate-to-source voltage. The circuit in **Figure 2** uses a P-channel device as the high-side MOSFET; it's on when its gate-to-source voltage is negative. Therefore, you must invert the control signal from the PWM controller. A MOSFET totem-pole configuration comprising Q_2 and Q_3 will work, although you can also use an inverting-gate driver.

Capacitor C_2 performs the level-shifting. It must have a value large enough to maintain its charge at the switching frequency but small enough for its voltage to follow variations in the input voltage. Resistor R_1 and P-channel MOSFET Q_3 charge C_2 to a voltage of $V_C = V_{IN} - V_{CC}$, where V_C is C_2's voltage, V_{IN} is the input voltage, and V_{CC} is the supply voltage of the Q_2 and Q_3 totem-pole configuration and the PWM IC. The supply voltage must be less than zener diode D_2's breakdown voltage. Otherwise, current will flow through D_2 and C_2 whenever Q_2 is on, which lowers efficiency. D_2 limits C_2's voltage to the value in the above **equation**. When Q_3 is on, D_2 becomes forward-biased if the voltage attempts to increase. This circuit applies a 0V voltage between Q_1's gate and source when Q_3 is on, and it applies $-V_{CC}$ when Q_2 is on.

Resistor R_1 also ensures that Q_1's gate-to-source capacitance discharges, which keeps Q_1 off when the totem pole's output

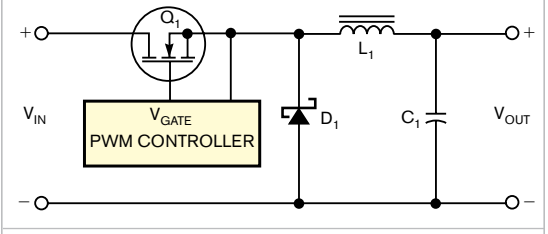

Figure 1 A basic buck converter uses a PWM controller and a MOSFET.

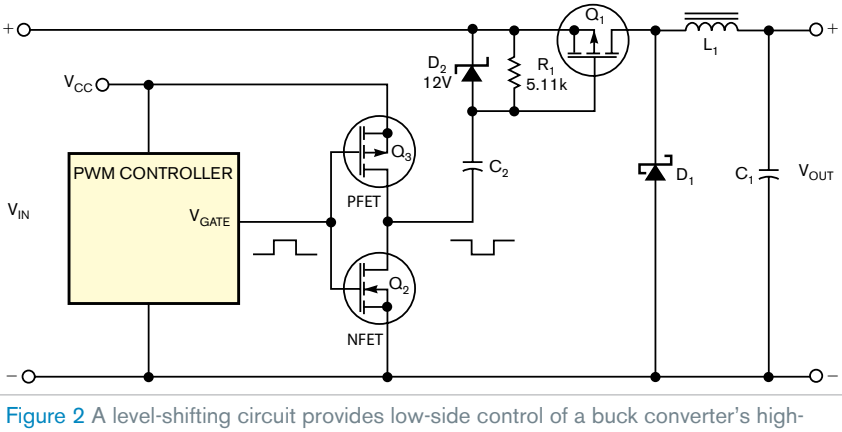

Figure 2 A level-shifting circuit provides low-side control of a buck converter's high-side FET.

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voltage is high. Diode D_2 limits Q_1's gate-to-source voltage to 12V regardless of the circuit's input voltage. Capacitor C_2 is transparent to Q_1's gate-drive pulse, so the circuit's gate-driving capability is just as good as that of the totem-pole circuit itself. The level shifting, therefore, imposes no limitation on the size of the MOSFET that the circuit can drive.

Figure 3 shows a practical buck converter employing this scheme. The converter's input voltage is 18 to 45V, and its output voltage is 12V at a 1.5A output current. The converter uses National Semiconductor's (www.national.com) LM5020-1 flyback/boost/forward/SEPIC (single-ended-primary-inductance-converter) PWM-controller IC.

The **figure** retains the component designators from the previous **figures** but adds functions such as input-voltage filtering in C_9; input-undervoltage lockout in R_2 and R_7; soft-start capability in C_3; switching-frequency-setting ability in 12.7-kΩ R_3 for 500 kHz; feedback compensation in C_7, C_8, and R_6; and output-voltage setting in R_9 and R_{10}.

The LM5020-1 provides current-mode control, but, in this circuit, it implements voltage-mode control. An internal sawtooth-current source with a peak value of 50 µA, which adds slope compensation to a current signal, serves as a voltage ramp. This current flows through 5.11-kΩ resistor R_4 and an internal 2-kΩ resistor to generate a ramp with a peak-to-peak voltage of 50 µA×(2 kΩ+5.11 kΩ)≃300 mV at the CS pin, Pin 8. The COMP pin, Pin 3, compares this sawtooth to the output error voltage at the COMP pin, which generates the right duty-ratio signal for Q_1.

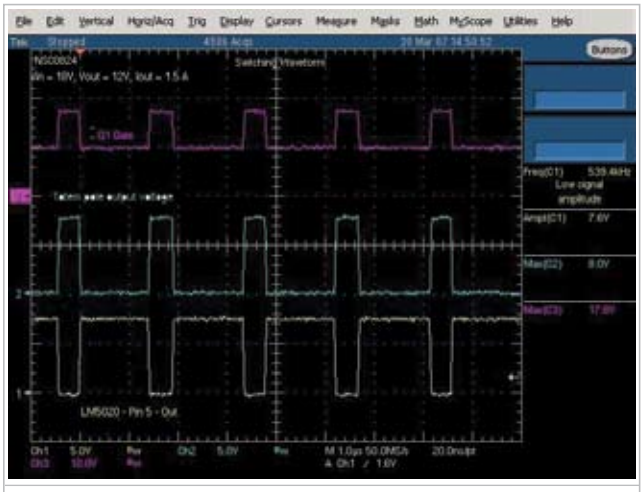

Figure 4 Voltage waveforms in the buck-converter circuit of Figure 3 show clean voltages with short rise and fall times.

Figure 4 shows the circuit's switching waveforms. Oscilloscope channel 1 (bottom trace) shows the gate-drive signal that the LM5020-1 generates. Channel 2 (middle trace) shows the corresponding totem-pole output voltage. Channel 3 (top trace) shows the level-shifted totem-pole output voltage between the source and the gate of Q_1. The peak value of Q_1's gate-to-source voltage equals the input voltage, and its amplitude is about 8V, the value of the supply signal that the LM5020-1 internally generates. All the waveforms are clean and have short rise and fall times. The full-load efficiency of the circuit is 86 and 83% at input voltages of 18 and 45V, respectively. EDN

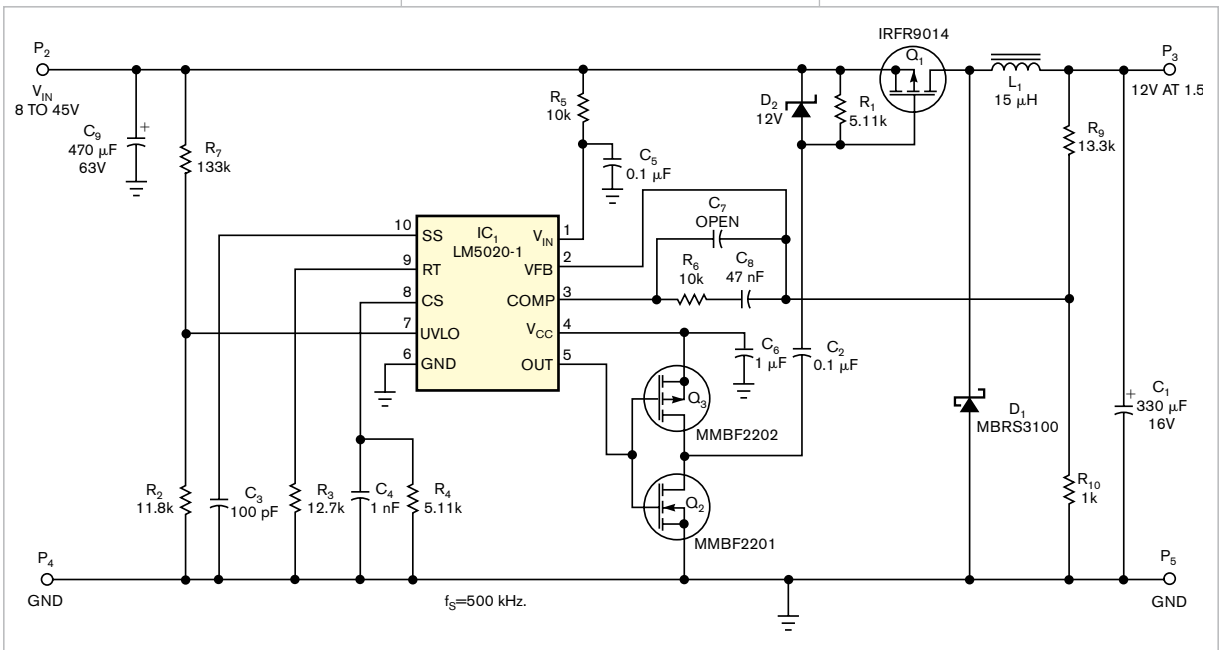

Figure 3 An alternative buck converter uses a low-side PWM IC to control MOSFET Q_1.

Isolated clock source acts as test generator

Daniele Danieli, Eurocom-Pro, Venice, Italy

Circuits such as PLL synthesizers, high-dynamic-range ADCs, and timing-sensitive digital networks require stable and spurious-free clocks. Testing these circuits is a difficult task when you use a master oscillator, even if the signal theoretically matches the application's phase noise and spurious responses. Variable clock-line loads, typical conditions in circuits under functional evaluation, and power-supply-line interferences, again typical in open-board environments on lab desktops, can degrade signal purity with jitter or unpredictable phase steps.

You can insulate an oscillator from a load requiring a special high reverse-attenuation-buffer stage, but it is more difficult to implement this insulation at frequencies of 10 MHz and more. This Design Idea describes a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

The circuit uses a quartz-oscillator stage with two NPN transistors in a conventional scheme (**Figure 1**). You select components C_3 and C_4 relative to the frequency; for 15- to 30-MHz frequencies, the corresponding values are 220 and 100 pF, respectively. You can scale up these values for lower frequencies. You can also substitute this stage with other equivalent circuits. A level-shift follower uses PNP transistor Q_3; a TTL-compatible signal at the output is available. You select resistor R_7 for the best pulse response; a value of 22Ω is adequate for most applications; however, you can omit the resistor if necessary.

You now apply a logic-level signal to the input pin of a high-speed CMOS optocoupler, IC_2. This design uses an HCLP-7101 type that operates at frequencies as high as 40 MHz, but new devices, such as the HCPL-77xx in SMD packages, are fully compatible. These optocouplers have input-to-output capacitance of less than 1 pF, and they have separate supply pins. If you do not use common grounds, as in the **figure**, you establish an optimized ultralow-power coupling, which provides effective isolation from load conditions and EMI (electromagnetic interference) that otherwise might modulate the incoming signal.

Note that the left side of the circuit, comprising an oscillator and the input half of the optocoupler, uses a dedicated battery to obtain the 5V supply voltage. On the right side, comprising the output half of the optocoupler, all lines directly connect to the board under test with relatively long cables; thus, they cause no disadvantages in the oscillator stage. You can use any optocoupler of adequate bandwidth as long as you pay attention to the correct power-supply voltage and the logic-level compatibility of IC_2. EDN

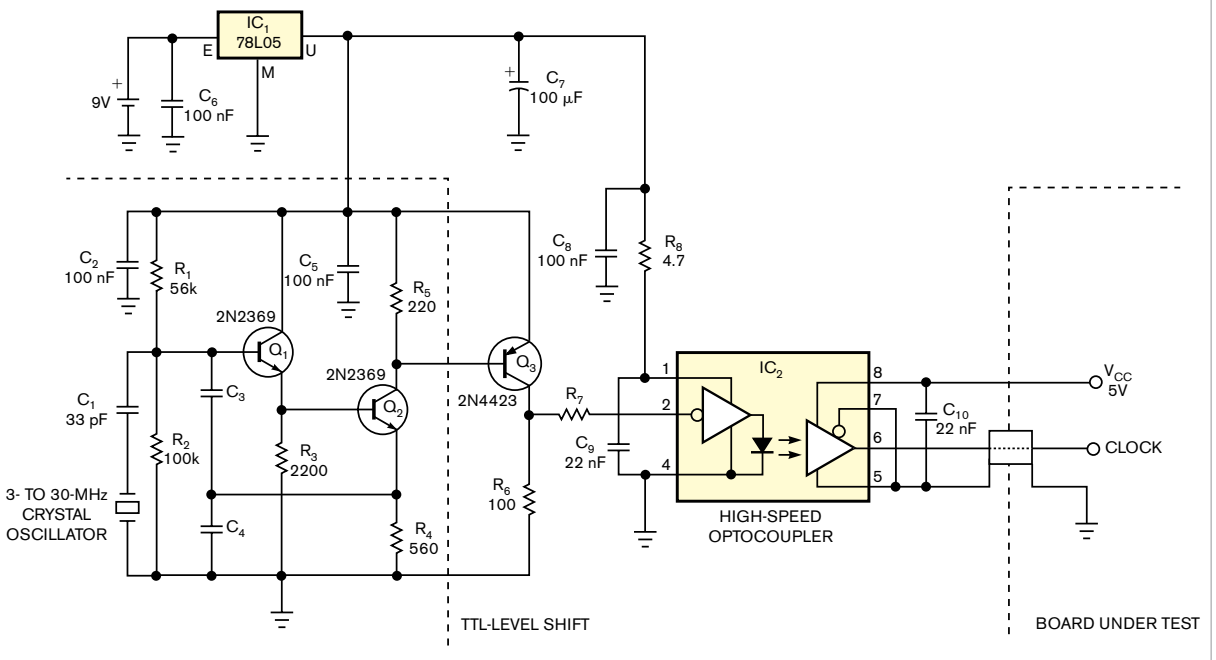

Figure 1 This circuit provides a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

Class AB inverting amp uses two floating-amplifier cells

Joseph Wee Ting, Institute of Atomic and Molecular Sciences, Sinica Academy, Taipei, Taiwan

Transistors often find use as three-pin amplifier devices, in which the input and the output share one pin. Thus, the input and the output must have the same voltage at this pin. On the other hand, a four-pin amplifier could isolate the circuit's input and output. Using optoisolators, you can design a four-pin Class AB amplifier. Although the output voltage of an optoisolator curtails its usefulness, you can add discrete transistors to form an isolated amplifier.

Figure 1 shows an example of a simple, 1-kV-p-p Class AB inverting amplifier that uses two identical floating-amplifier cells. The frequency response is dc to 20 kHz at full gain. You can achieve higher frequencies but at lower gains. The ratio of resistors R_2 and R_1 sets the gain. This circuit eliminates the need for many voltage-shifting components, which are typical of a standard circuit design. The positive and the negative cells are driven out of phase. The 15V and −15V and re-

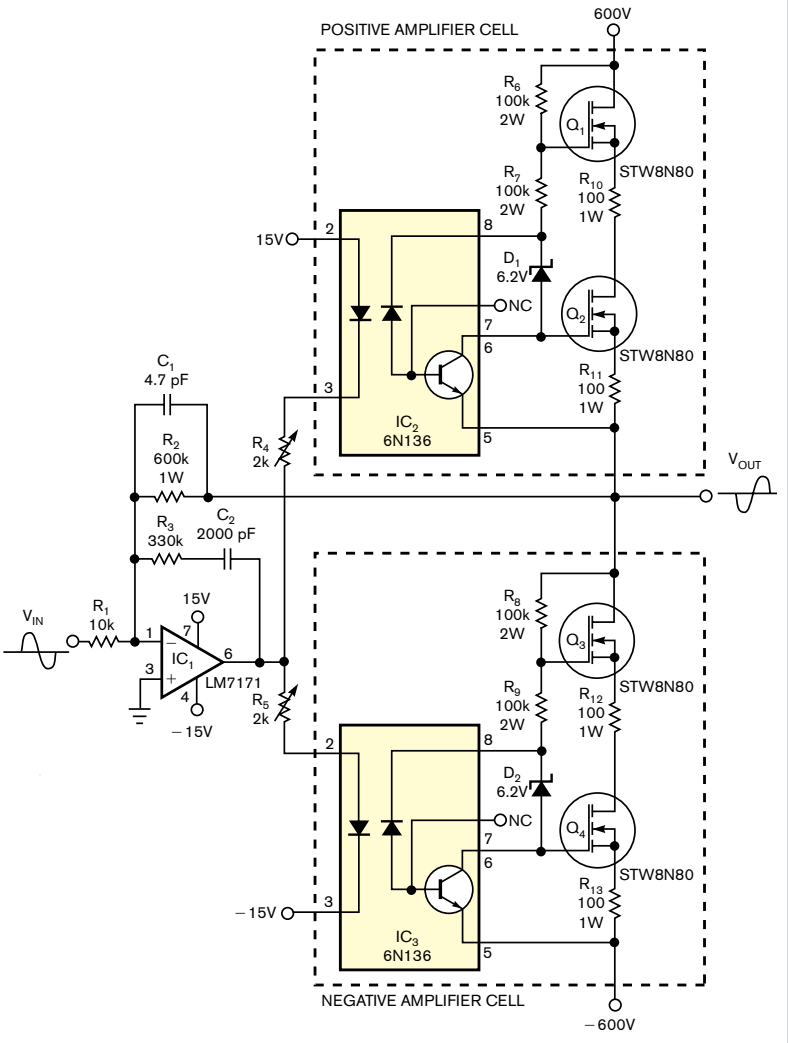

Figure 1 Transistors boost the output voltage and current of optoisolators, making an isolated amplifier output.

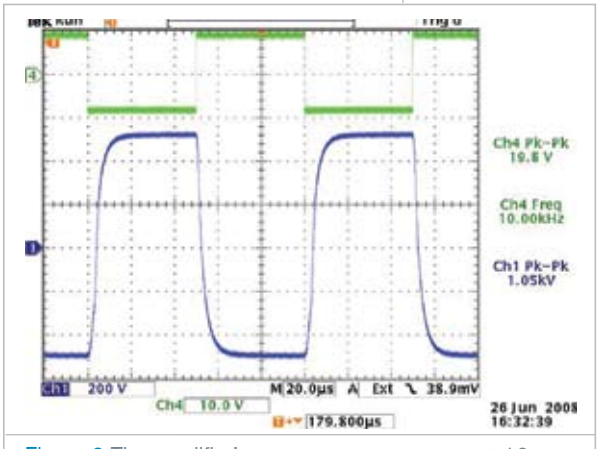

Figure 2 The amplifier's square-wave response at 10 kHz shows some high-frequency cutoff.

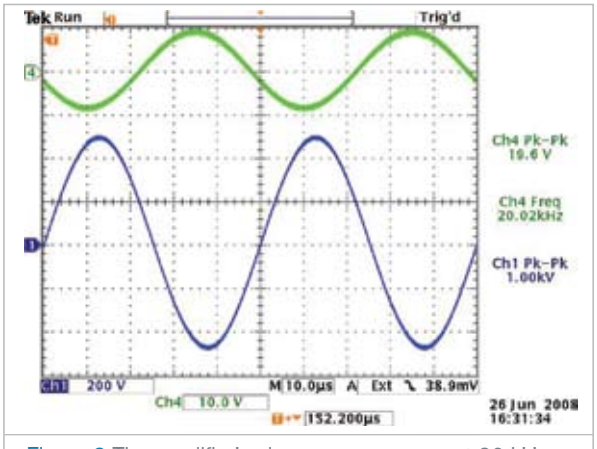

Figure 3 The amplifier's sine-wave response at 20 kHz shows a clean output signal.

sistors R_4 and R_5 provide the necessary bias to guarantee that the output transistors are always on. Careful trimming of R_4 and R_5 can remove the output crossover distortion. Zener diodes D_1 and D_2 keep the optoisolator photodiodes back-biased at 6.2V. Resistors R_{10}, R_{11}, R_{12}, and R_{13} supply some negative feedback to the output transistors. You must mount the four STW8N80 N-channel MOSFETs on suitable heat sinks to keep them cool. The circuit requires no active short-circuit protection. One pair of 125-mA currents across the high-voltage supply lines is sufficient to safeguard the circuit from destruction.

Figure 2 shows the square response at 10 kHz. There are no overshoots or undershoots, and the rising edge is almost antisymmetric with respect to the trailing edge. **Figure 3** shows the sine-wave response at 20 kHz. Both outputs are 1 kV p-p. EDN

DPGA conditions signals with negative time constant

W Stephen Woodward, Chapel Hill, NC

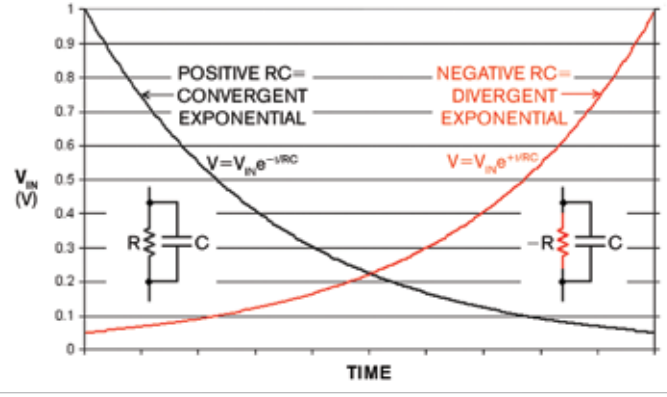

Figure 1 A negative time constant causes voltage to increase exponentially over time.

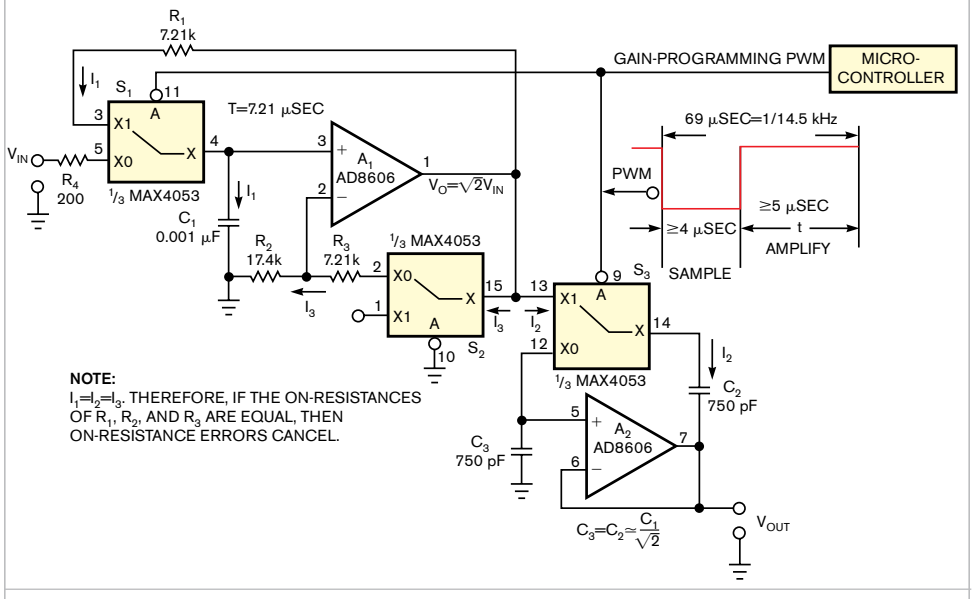

Figure 2 Positive feedback from amplifier A_1 causes C_1 to increase in voltage, which exponentially amplifies the input voltage.

DPGAs (digitally programmable-gain amplifiers) amplify or attenuate analog signals, which maximizes an ADC's dynamic range. Most monolithic DPGAs, such as the Linear Technology (www.linear.com) LTC6910 and the National Semiconductor (www.national.com) LPM8100, use a multiplying DAC in an op amp's feedback loop so that the DAC's input code sets the amplifier's closed-loop gain. Instead of using a monolithic DPGA, you can use two op amps and three analog switches to build a DPGA employing negative time constants.

You're no doubt familiar with the $e^{-t/RC}$ convergent exponential in which a capacitor in an RC circuit asymptotically discharges to zero. For input voltage, $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V=V_{IN}/4$ at $t=2T$, $V=V_{IN}/8$ at $t=3T$, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). If you replace resistor R with −R, you create a positive RC time constant. Thus, you create a divergent exponential, $V_{IN}e^{+t/RC}$.

Instead of converging to zero, the waveform theoretically diverges to infinity, and $V=2V_{IN}$ when $t=T$, $V=4V_{IN}$ at $t=2T$, $V=8V_{IN}$ at $t=3T$, and so forth. Therefore, you can amplify the in-

put voltage by simply waiting the right amount of time ($t=\log_2(V/V_{IN})T$) after starting the negative discharge. The divergent exponential and the negative time constant are the core concepts of the circuit in **Figure 2**.

You can program the amplifier's gain with a PWM (pulse-width-modulation) signal from a microcontroller or another circuit. When the PWM signal goes to logic zero, sample-and-hold capacitor C_1 charges to V_{IN}. When the PWM signal cycles to logic one, op amp A_1 drives the R_1C_1 positive-feedback loop, creating a negative time constant. The resulting divergent exponential rise of C_1's charge continues as long as the PWM signal remains at logic one. That situation creates a net voltage gain of:

$$V_{OUT}(t)=V_{IN}2^{(t/10\ \mu sec+0.5)}.$$

THE NEAR-UBIQUITY OF PROGRAMMABLE-TIMER/COUNTER HARDWARE MAKES IT EASY TO DIGITALLY GENERATE A HIGHLY REPEATABLE PWM-CONTROL SIGNAL.

Thus, gain$=2^{(t/10\ \mu sec+0.5)}$ and log(gain)$=3+0.6$ dB/μsec. At the end of the amplification cycle, when PWM returns to logic zero, amplifier A_2 captures and holds the amplified input voltage.

The logarithmic relationship between gain and timing provides excellent gain resolution even when a PWM signal has just 8 bits of resolution and its programmable gain has a range greater than 0.2 dB/LSB step. (To view the log and linear plots of gain versus time using the amplify phase, go to the Web version of this Design Idea at www.edn.com/090319dia.)

The accuracy and repeatability of the timing of the exponential signal, the ADC sampling, the jitter, and the RC-time-constant stability all limit the amplifier's gain-programming accuracy. In **Figure 2**, 1 nsec of timing error, or jitter, produces 0.007% of gain-programming error. Fortunately, the near-ubiquity of programmable-timer/counter hardware in microcontrollers and data-acquisition systems usually makes it easy to digitally generate a highly repeatable PWM-control signal. EDN

Instrumentation amplifier compensates system offset from single supply

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

Many integrated instrumentation amplifiers have architectures that permit offset compensation. The reference terminal's voltage, V_{REF}, adds in phase to the output to yield a gain of one. As a result, you can reset the output offset voltage by applying to the V_{REF} input a correction voltage of equal value but of opposite polarity. If the instrumentation amp operates from a dual-supply voltage, you can easily provide both positive- and negative-correction voltage. However, some instrumentation amps operate from a single supply—for example, in a battery-powered application—to amplify a signal source or a sensor that introduces a positive offset voltage. A sensor such as the AD590 from Analog Devices (www.analog.com), for example, produces an output current proportional to absolute temperature, and you should calibrate it at the lower reference temperature. In this case, the output swing of the instrumentation amp decreases, especially with high gain. To prevent this effect, you must apply a negative-correction voltage, which you generate from the positive power supply. In precision applications, the application of such a voltage may cause a problem.

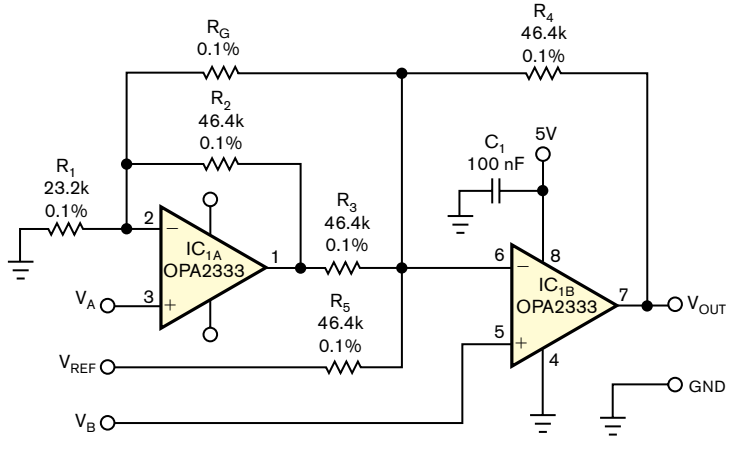

Figure 1 You can build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input.

This Design Idea shows you how to build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input. The circuit in **Figure 1** employs the dual high-precision OPA2333 op amp from Texas Instruments (www.ti.com). This op amp can

operate from a 1.8 to 5.5V supply and uses a proprietary autocalibration technique to simultaneously provide a maximum offset voltage of 10 µV and near-zero drift over time and temperature. It also offers high-impedance inputs that have a common-mode range 100 mV beyond the supply rails and rail-to-rail output that swings within 50 mV of the rails. Applying the superposition of the effects to the circuit in **Figure 1** yields the following **equation**:

$$V_O = V_B\left[\left(1+\frac{R_4}{R_3\|R_5\|R_G}\right)+\left(\frac{R_4}{R_3}\right)\left(\frac{R_2}{R_G}\right)\right]-V_A\left[\left(1+\frac{R_2}{R_1\|R_G}\right)\left(\frac{R_4}{R_3}\right)+\left(\frac{R_4}{R_G}\right)\right]-V_{REF}\left(\frac{R_4}{R_5}\right).$$

To achieve equal gain for both the V_B and the V_A inputs, resistors R_2, R_3, R_4, and R_5 must have equal values that are double the value of R_1. Using the resistor values in **Figure 1**, you obtain the following simplified **equation**:

$$V_O = \left(3+\frac{92.8\ k\Omega}{R_G}\right)(V_B-V_A)-V_{REF}.$$

The amplifier's differential gain is $3+(92.8\ k\Omega/R_G)$, and the reference voltage is added, inverted together with the output signal. Resistor R_G sets the gain, and, if you do not connect R_G, the gain assumes the minimum value, which is three; decreasing the value of R_G to 93Ω increases the gain to 1000.

The V_{REF} input requires a low-impedance connection to preserve a good CMRR (common-mode-rejection ratio); otherwise, you can use an op-amp buffer for better CMRR, which depends mainly on resistor-ratio matching. In this implementation, to preserve an acceptable CMRR, you must use precision film resistors. Analyzing the circuit, you can calculate the worst-case CMRR at low frequency. With R_2, R_3, R_4, and R_5 all of equal value and double that of R_1 and with all the resistors having equal tolerance, you obtain:

$$CMRR = \frac{3+\frac{2R}{R_G}}{6\left(\frac{\Delta R}{R}\right)},$$

where ΔR/R is the resistor's tolerance. If the tolerance is 0.1% and with the minimum differential gain, which is three, you obtain a CMRR of at least 54 dB. With a differential gain of 100, you obtain a CMRR of at least 84 dB.

The V_{REF} input can reduce the system offset to the lower output-swing limit but does not reset it completely because, in that case, the output voltage would be unable to reach the single-supply ground. If you want instead to reset the output offset, you can subtract this value using an ADC with differential inputs (**Reference 1**). EDN

REFERENCE

1 Bruno, Luca, "Circuit compensates system offset of a load-cell-based balance," *EDN*, Aug 16, 2007, pg 71, www.edn.com/article/CA6466208.

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READERS SOLVE DESIGN PROBLEMS

Twin-T power oscillators work as dc-biased ac sources

Tiger Zhou and Robert Dobkin, Linear Technology, Milpitas, CA

AC test equipment often needs a low-distortion signal source to excite the device under test. The common practice is to use a signal generator to produce a low-distortion reference, which you feed to a power amplifier to drive the device under test. This Design Idea suggests a less cumbersome alternative.

Figure 1 shows an oscillator that generates a low-distortion sinusoidal signal with power-driving capability. The power oscillator consists of two major parts: a twin-T network and a high-power low-dropout regulator. The twin-T network has two T-type filters in parallel: one lowpass filter and one highpass filter. The twin-T network is highly frequency-selective as a notch filter. The low-dropout regulator amplifies the signal and drives the load. The regulator in this circuit incorporates a current-reference voltage-follower architecture. It is unity gain from the Set to the Out pins, and the current reference is a precision 10-µA current source. The R_{SET} resistor on the Set pin programs the output-dc level. By connecting a twin-T network between the Out and the Set pins, the resulting notch filter attenuates both high- and low-frequency content, allowing the center frequency to freely pass through. The resistors and capacitors program the center frequency, f_0: $f_0=1/(2\pi RC)$.

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Small-signal analysis of the twin-T network indicates that the gain is maximum at the center frequency. The twin-T oscillator's maximum gain increases from one to 1.1 when the K factor increases from two to five (**Fig-**

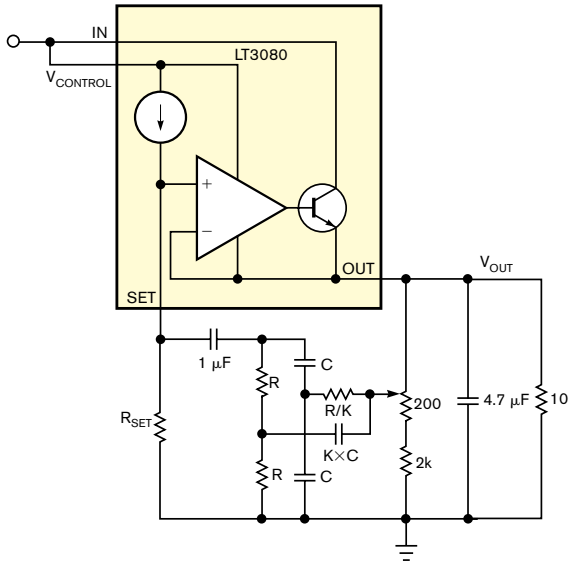

Figure 1 This oscillator generates a low-distortion sinusoidal signal with power-driving ability.

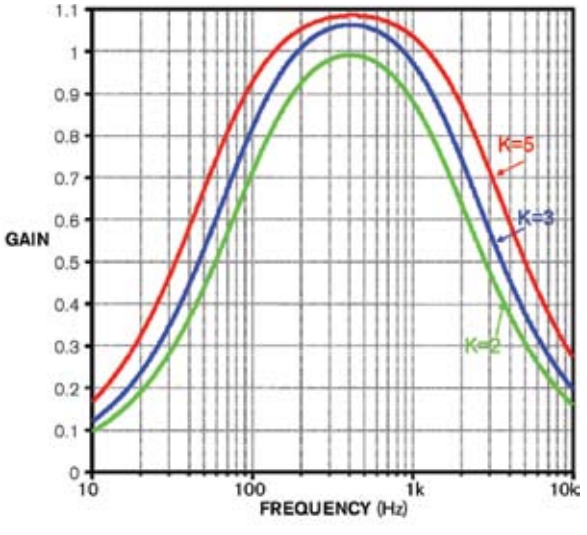

Figure 2 The twin-T network's gain changes with the value of K from Figure 1.

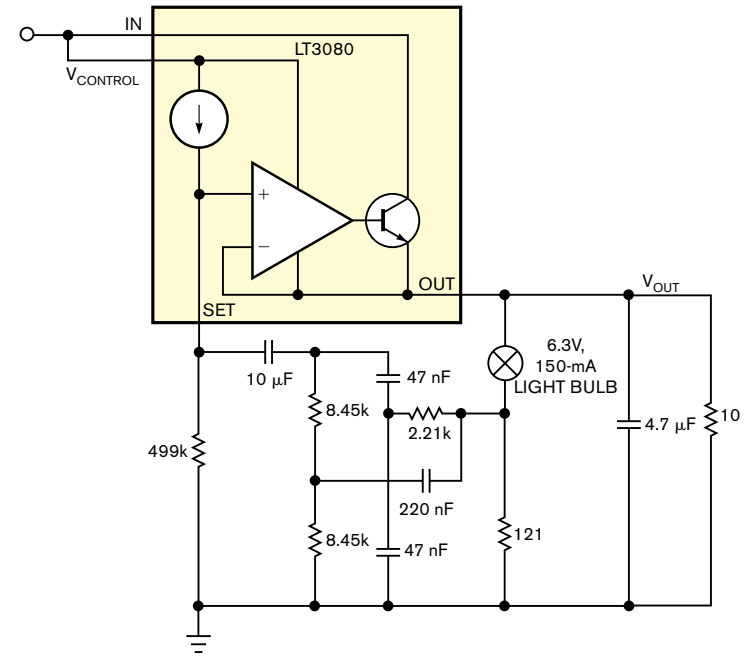

Figure 3 To automatically control the gain, you can replace the potentiometer with a light bulb.

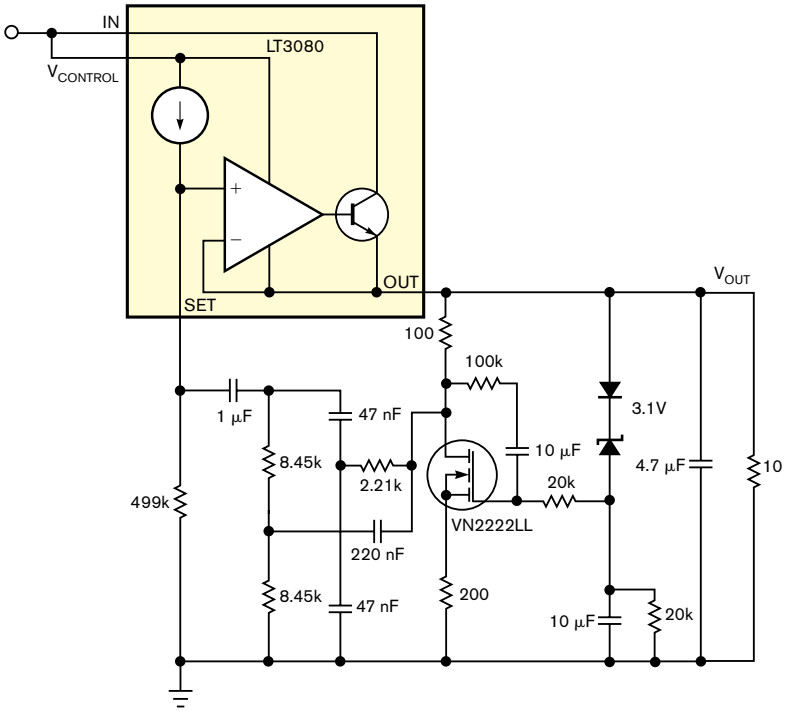

Figure 4 You can automatically control the gain by replacing the potentiometer with a variable-resistance MOSFET.

ure 2). The maximum gain decreases when the K factor is larger than five. Therefore, select a K factor of three to five for a gain larger than unity gain. The loop gain must be unity to maintain a steady oscillation. Thus, you need a potentiometer to tune the loop gain to control the oscillation amplitude.

The twin-T oscillator can drive inductive, capacitive, or resistive loads. The low-dropout regulator's current limit, which is 1.1A for the Linear Technology (www.linear.com) LT3080, is the only limit on the oscillator's drive capability. The load characteristics limit the maximum programmable frequency. For example, a 10Ω resistive load with a 4.7-µF output capacitor causes a 7% THD (total harmonic distortion) at a frequency higher than 8 kHz, although THD is 0.1% at 400 Hz in the circuit of **Figure 3**. The twin-T oscillator has the same performance in line and load regulation as the LT3080. It also works in a wide temperature range.

To automatically tune the gain, you can replace the potentiometer with a light bulb (**Figure 3**) or a voltage-modulated resistive MOSFET (**Figure 4**). The light bulb's resistance increases with the oscillation amplitude due to a self-heating effect, so it servos the loop gain to maintain the oscillation. In **Figure 4**, by detecting the peak voltage using a zener diode, the MOSFET resistance decreases when the oscillation amplitude is high. The loop gain also decreases to maintain the oscillation.

Figure 5 shows the test waveform of the twin-T oscillator using a light bulb. The output is tuned to a 4V-p-p voltage with 5V-dc bias voltage (**Figure 6**). The twin-T oscillator has a 400-Hz frequency and 0.1% THD. The most significant harmonic contribution is from the second harmonic at less than 4 mV p-p. **Figure 6** shows the test waveform of the twin-T oscillator using the MOSFET. The THD is 1% with a 40-mV-p-p second harmonic.

Start-up is another important aspect of the oscillator. Both circuits exhibit no low-frequency swing, which is common to other types of oscillators. The waveforms in **figures 7** and **8** exhibit little overshoot. The oscilla-

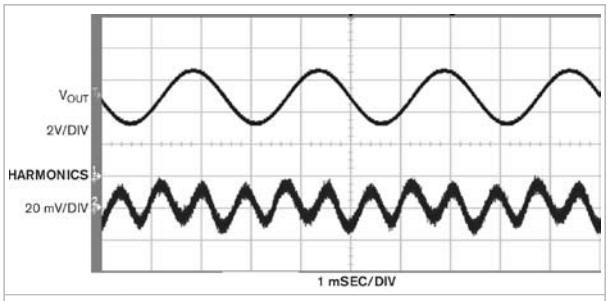

Figure 5 The test waveform for the oscillator in Figure 3 shows low distortion at a THD of 0.1%.

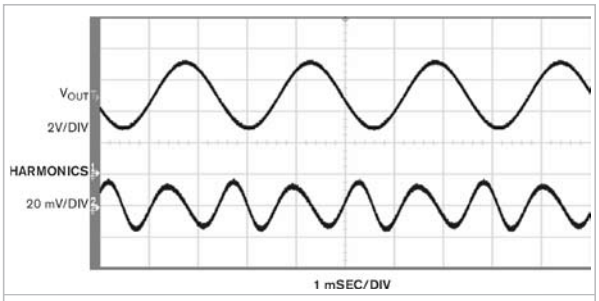

Figure 6 The test waveform for the oscillator in Figure 4 shows low distortion with a THD of 1%.

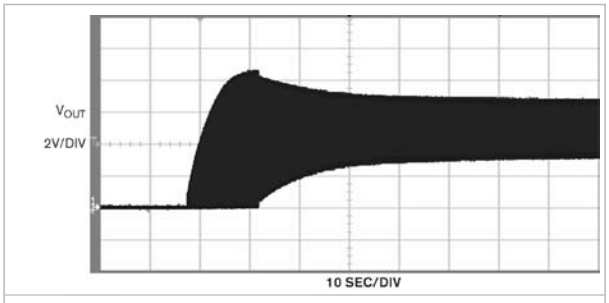

Figure 7 The waveform for the circuit in Figure 3 shows a slow start-up of the light-bulb oscillator.

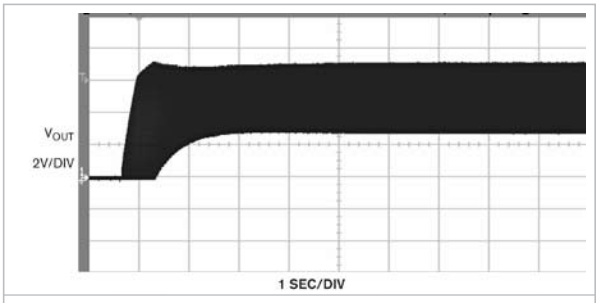

Figure 8 The waveform for the circuit in Figure 4 shows a quick start-up of the MOSFET oscillator.

tor using the MOSFET stabilizes faster than the one using the light bulb because the light bulb has a long thermal constant due to the heating effect. You can use the simple circuit as a dc-biased ac source in applications requiring low distortion and power-driving capability. EDN

ACKNOWLEDGMENT

The authors wish to thank Tony Bonte, Mitchell Lee, Jim Williams, and Todd Owen for fruitful discussions.

Diagnose LEDs by monitoring the switch-mode duty cycle

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Engineers often monitor the forward voltage, V_F, of HB LEDs (high-brightness light-emitting diodes) to assess the LEDs' health. Big changes in forward voltage can indicate deterioration or even a complete failure of one or more LEDs connected in series. For several LEDs in series, the sum of their forward voltages can reach 40V or more, and, if you do not reference that voltage to ground, it requires a differential measurement. In addition to the challenges of high voltage and differential measurement, HB LEDs are often dimmed using PWM (pulse-width modulation). If so, you can't measure forward voltage during the low portion of the PWM duty cycle when the LEDs are unlit and the forward voltage is not present. For a hysteretic buck-LED driver driving three LEDs in series (**Figure 1**), you must measure the anode and cathode voltages of the string when the Dim pin is high.

To avoid the need for a differential high-voltage measurement, you can take the indirect approach of measuring the duty cycle at the driver pin, DRV. For this LED driver, a first-order estimate of forward voltage for

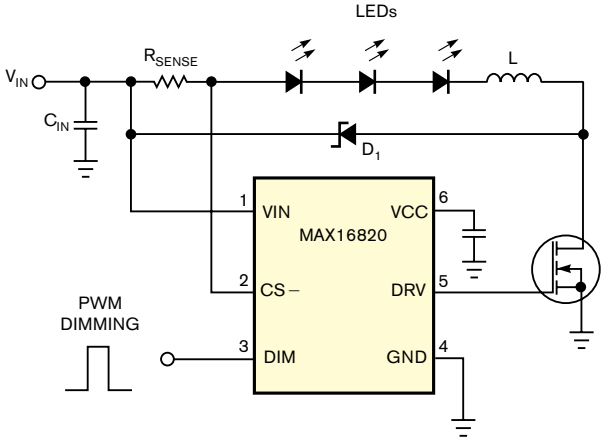

Figure 1 For a hysteretic buck-LED driver driving three LEDs in series, you must measure the anode and cathode voltages of the string when the Dim pin is high.

the LED string is $V_F=D\times V_{IN}$, where D is an internal duty cycle that the IC's switch-mode section produces; do not confuse this duty cycle with that at the Dim pin. You reference the driver signal to ground and limit it to the power-supply voltage, V_{CC}, at 5V. That condition allows the use of low-voltage ADCs or comparators, which the LED driver's V_{CC} output, a maximum of 10 mA, can power.

Figure 2 shows how to detect a short-circuited LED with the aid of a comparator. Filter R_1C_1 converts the ac PWM signal at the driver to a dc voltage, V_D, proportional to $D\times V_{CC}$. You should sample V_D when its value is greater than perhaps 90% of its steady-state value; this sampling requires a period of at least $2.3R_1C_1$. Because the comparator's LE (latch enable) latches the output when LE is low, LE should assert not earlier than $2.3R_1C_1$ after the Dim pin goes high. R_2, C_2, and D_2 ensure that LE deasserts immediately after the Dim pin goes low. The value of R_2C_2 is higher than that of R_1C_1, so the comparator enables when the input signal reaches at least 90% of its steady-state value. D_2 immediately discharges C_2 after the Dim pin goes low, which latches the output as soon as the LEDs turn off.

Because the reference voltage is lower than $D\times V_{IN}$, the comparator output is normally low. If an LED fails shorted, its forward voltage drops and causes the duty cycle at the driver to drop. V_D then drops below the reference, causing the comparator's output to go high, indicating a shorted LED. Because the output latches when the Dim pin goes low, the error signal remains asserted even when the LEDs are off. **Figure 3** shows the filtered Dim pin and driver signals for normal operation versus a shorted-LED condition.

For a system with an input voltage of 12V and three LEDs in series, in which the forward voltage is approximately 3V per LED (**Figure 3a**), the filtered driver signal (green) stabilizes at approximately $D\times V_{CC}=(9V/12V)5V=3.75V$. The comparator latches when the filtered Dim signal (yellow) goes lower than 2.5V, so the comparator begins interpreting the filtered driver signal after approximately 100 µsec. Clearly, V_D is higher than the threshold-reference voltage (red) when the comparator is active. After one of the LEDs shorts out (**Figure 3b**), V_D stabilizes at approximately $(6V/12V)5V=2.5V$ and no longer exceeds the threshold. That condition causes the comparator's output to go high, indicating that one of the LEDs has become a short circuit.

The choice of filter constants R_1C_1 and R_2C_2 depends on several parameters. The cutoff frequency should be low enough to properly filter the driver signal yet small enough to allow the filtered signal to stabilize near the steady-state value achievable within the shortest dimming pulse. You can easily adjust this circuit to detect open-circuit LEDs. When an LED breaks and stops conducting current, the driver's duty cycle goes to 100% when the Dim pin is high. If you then swap the comparator-input connections and put the reference voltage slightly below V_{CC}, the comparator output goes high in response to an open LED. EDN

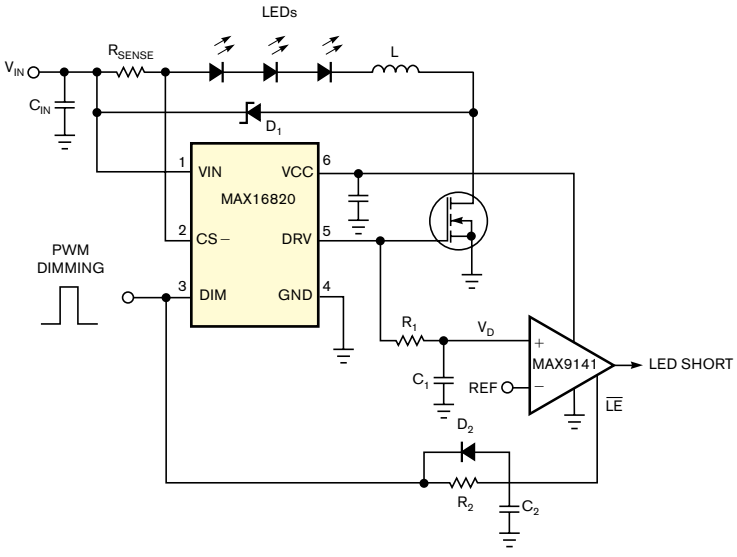

Figure 2 Adding this comparator circuit to the Figure 1 circuit provides detection of shorted LEDs.

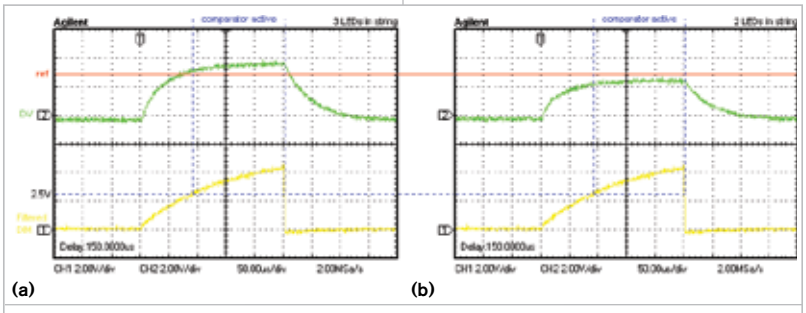

Figure 3 For a system with an input voltage of 12V and three LEDs in series, in which the forward voltage is approximately 3V per LED (a), the filtered driver signal (green) stabilizes at approximately $D\times V_{CC}=(9V/12V)5V=3.75V$. The comparator latches when the filtered Dim signal (yellow) goes lower than 2.5V, so the comparator begins interpreting the filtered driver signal after approximately 100 µsec. Clearly, V_D is higher than the threshold reference voltage (red) when the comparator is active. After one of the LEDs shorts out (b), V_D stabilizes at approximately $(6V/12V)5V=2.5V$ and no longer exceeds the threshold.

Single pin controls relay, intermittent buzzer, and status LED

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Switching applications involving controlling devices or appliances using digital-I/O lines through a relay often need to indicate the change of state of the I/O line and, hence, the connected device. This indication could be in the form of a buzzer that turns on for a few seconds every time the line changes state. Designers generally employ an additional I/O pin to trigger the buzzer whenever the state of the primary I/O line changes. This Design Idea discusses a circuit that controls a device through a relay and an intermittent buzzer with only one digital-I/O pin.

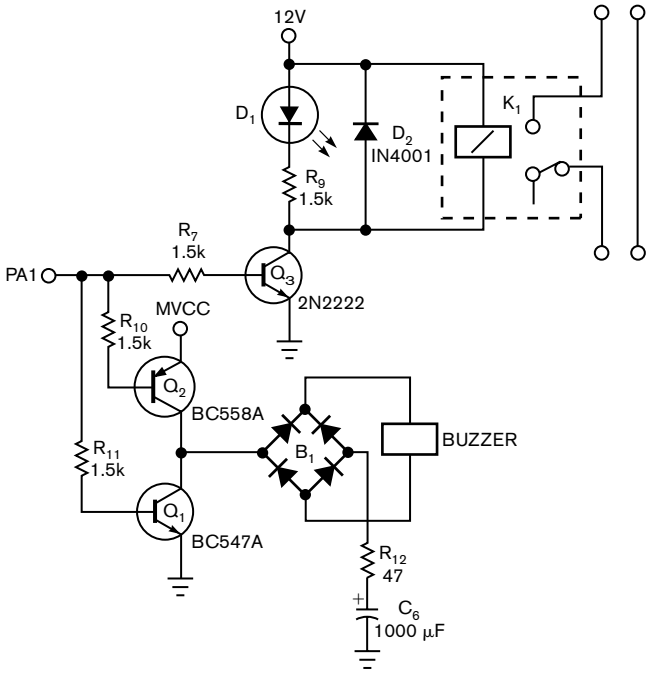

Figure 1 This circuit controls a device through a relay and an intermittent buzzer with only one digital-I/O pin.

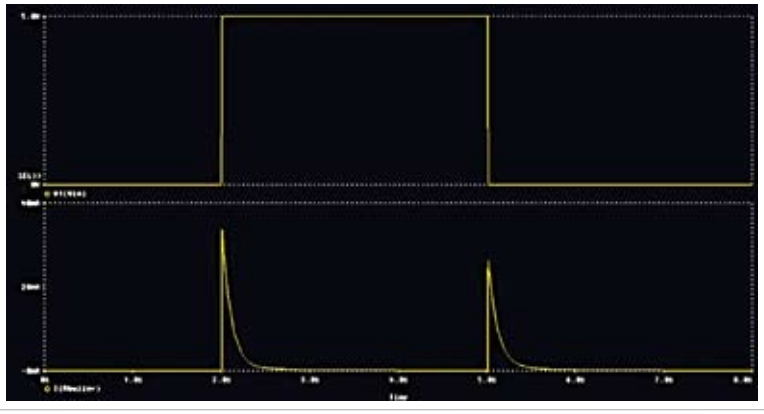

Figure 2 A Spice simulation of the buzzer circuit replaces the buzzer with 50Ω resistance and plots the current through the buzzer and the status of the I/O line.

Pin PA1 of the digital device controls a relay, which switches an appliance on and off (**Figure 1**). NPN transistor Q_3 activates the relay coil when the I/O line is in the high state. Status LED D_1 connects in parallel to the relay coil and turns on when the I/O line is high and off when the line is low.

The buzzer remains on for a small amount of time when the relay changes state. You accomplish this task by employing a push-pull-inverter topology using complementary BJTs (bipolar-junction transistors) NPN Q_1 and PNP Q_2. The output of this stage connects to a bridge rectifier with a buzzer as a load because buzzers usually are unidirectional. The bridge rectifier connects in series both with resistor R_{12} to regulate the maximum current through the buzzer and with capacitor C_1 to ensure that the buzzer "fades off." When the line is low, transistor Q_2 is on, the capacitor charges to a positive voltage, and the buzzer operates until the current through it is sufficient. When the line goes high, transistor Q_1 switches on, the capacitor discharges to approximately 0V, and the buzzer operates again for a short duration. The on-time of the buzzer depends on the values of R_{EQ}, the series combination of R_{12} and the buzzer resistance, and C_6. To change the time constant and hence the on-time of the buzzer, you should change the value of the capacitor rather than that of the resistor. You can also design this circuit using only one BJT instead of two, but the transistor would always draw some current at steady state.

This topology is useful when no separate I/O lines are available for controlling the buzzer. You can also employ this topology to indicate the change of state of any input stage directly by connecting it to the given circuit or through a buffer. **Figure 2** shows a Spice simulation of the buzzer circuit. This simulation replaces the buzzer with 50Ω resistance and plots the current through the buzzer along with the status of the I/O line. EDN

Simple two-transistor circuit lights LEDs

Barry A Tigner, Michigan State University, East Lansing, MI

A previous Design Idea describes a circuit that uses an astable multivibrator to drive an LED (**Reference 1**). The circuit in **Figure 1** uses a simpler alternative approach. The circuit uses a 2N3904 NPN transistor and a 2N3906 PNP transistor, which operate as a high-gain amplifier.

The 1-MΩ resistor supplies bias current. The 1-kΩ resistor helps linearize the oscillator waveform into one that is close to a square wave with about a 50-to-50 duty cycle. The capacitor supplies positive feedback from the output of the amplifier to the noninverting input. The frequency of oscillation depends mostly on the RC constant of the feedback capacitor and the input-stage impedance. The circuit oscillates at 91 kHz with a 48% duty cycle. You can use almost any common NPN or PNP transistors, as long as they have moderate forward-current gain of 50 or more and can handle 100-mA collector currents.

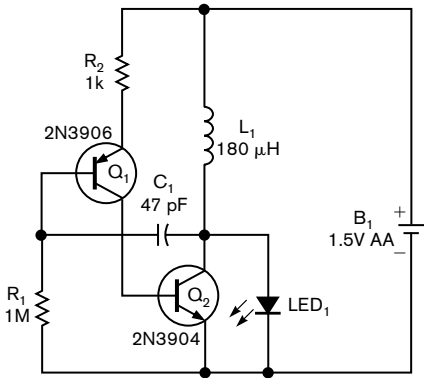

Figure 1 This two-transistor circuit operates as a high-gain amplifier to light LEDs.

The LED connects across the output transistor because this approach lets the inductive kickback voltage add to the battery-supply voltage and makes the LED brighter. This circuit operates well from approximately 0.8 to 1.6V, which is the useful range of an alkaline battery. The LED-light output decreases as the supply voltage decreases from 1.6 to 0.8V. EDN

REFERENCE

1 Bruno, Luca, "Astable multivibrator lights LED from a single cell," *EDN*, Aug 21, 2008, pg 53, www.edn.com/article/CA6586223.

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READERS SOLVE DESIGN PROBLEMS

Simple method uses PSpice for Thevenin-equivalent circuits

David Karpaty, Analog Devices Inc, Wilmington, MA

Thevenin- and Norton-equivalent circuits, among the most fundamental circuit-analysis theorems, can be useful for determining a load resistance for maximum power transfer, simplifying circuit models, and a variety of other analysis techniques. Unfortunately, calculating the Thevenin voltage and resistance can become difficult as circuit complexity increases. **Figures 1**, **2**, and **3** illustrate a simple method for obtaining the Thevenin voltage and resistance—and, subsequently, the Norton equivalence—with the aid of simulation. First, you choose an arbitrary load resistance, R_{LOAD}—2 kΩ in this example—and run the simulation to get the current through the load resistance. Next, you remove the load resistance and simulate the open-circuit voltage across nodes A and B to obtain the Thevenin voltage. You obtain the Thevenin resistance from those two values.

The Thevenin-equivalent circuit must produce the same current through the load. The total resistance in the Thevenin circuit is $R_{TOTAL}=(V_{TH}/I_{LOAD})=(374.095\ mV/60.301\ \mu A)\simeq 6.203\ k\Omega$, where R_{TOTAL} is the total resistance. Therefore, the Thevenin resistance is simply $[(V_{TH}/I_{LOAD})-R_{LOAD}]=(R_{TOTAL}-R_{LOAD})=6.203\ k\Omega-2\ k\Omega\simeq 4.203\ k\Omega$, where V_{TH} is the Thevenin voltage and I_{LOAD} is the load current.

Figure 4 shows the Thevenin-equivalent circuit, and **Figure 5** shows the Norton-equivalent circuit. Note that, because the net current through the load flows to the left, the positive Thevenin terminal is grounded.

Without the aid of simulation, you can calculate $V_{THEVENIN}$ and $R_{THEVENIN}$ as follows. The array for the loop currents in **Figure 2**, assuming a clockwise current flow in each loop, gives the current through the load resistance (**Equation 1**).

$$\begin{bmatrix} +(6k)I_1 & -(2k)I_2 & -(0)I_3 & -(2k)I_4 & -(0)I_5 & -(0)I_6 \\ -(2k)I_1 & +(9.5k)I_2 & -(2k)I_3 & -(0)I_4 & -(2k)I_5 & -(0)I_6 \\ -(0)I_1 & -(2k)I_2 & +(15k)I_3 & -(0)I_4 & -(0)I_5 & -(3)I_6 \\ -(2k)I_1 & -(0)I_2 & -(0)I_3 & +(4k)I_4 & -(2k)I_5 & -(0)I_6 \\ -(0)I_1 & -(2k)I_2 & -(0)I_3 & -(2k)I_4 & +(14k)I_5 & -(2k)I_6 \\ -(0)I_1 & -(0)I_2 & -(3k)I_3 & -(0)I_4 & -(2k)I_5 & +(17k)I_6 \end{bmatrix} \begin{bmatrix} 1V \\ 0V \\ 0V \\ 5V \\ -2V \\ 2V \end{bmatrix} \quad (1)$$

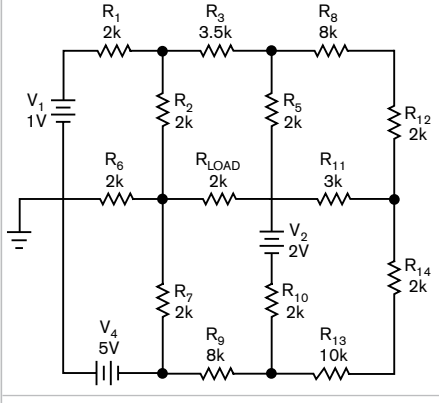

Figure 1 To calculate Thevenin-equivalent circuits, you first choose a load resistance—2 kΩ in this circuit.

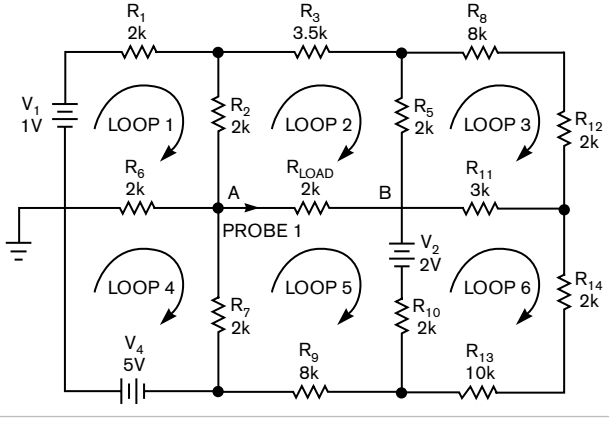

Figure 2 The simulation for current through the load resistance yields −60.3 μA.

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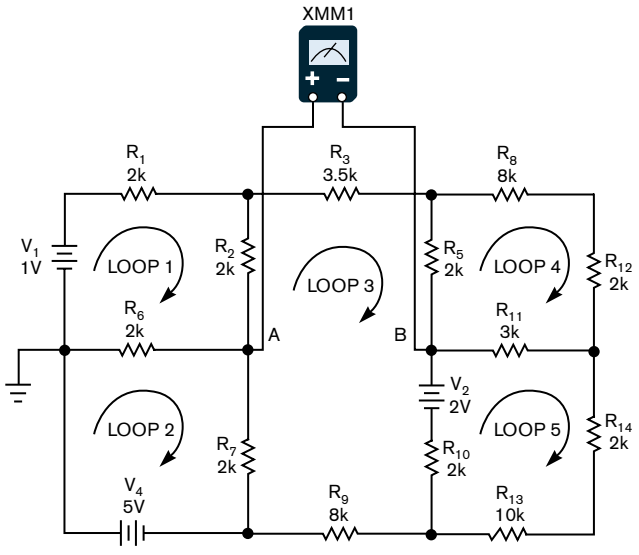

Figure 3 The simulation for the open-circuit voltage yields approximately −374 mV.

From **Equation 1**, you can calculate I_2 and I_5: $I_2 \simeq 217.77\ \mu A$, and $I_5 \simeq 157.47\ \mu A$. Thus, $I_2 - I_5 \simeq 60.3\ \mu A$, assuming a leftward flow through the load resistor.

You calculate the array for the loop currents in **Figure 3** without the load resistance, as **Equation 2** shows. From **Equation 2**, you can calculate the following currents: $I_1 \simeq 807.92\ \mu A$, $I_2 \simeq 1.744$ mA, $I_3 \simeq 179.87\ \mu A$, $I_4 \simeq 53.64\ \mu A$, and $I_5 \simeq 148.27\ \mu A$.

$$\begin{bmatrix} +(6k)I_1 & -(2k)I_2 & -(2k)I_3 & -(0)I_4 & -(0)I_5 \\ -(2k)I_1 & +(4k)I_2 & -(2k)I_3 & -(0)I_4 & -(0)I_5 \\ -(2k)I_1 & -(2k)I_2 & +(19.5k)I_3 & -(2k)I_4 & -(2k)I_5 \\ -(0)I_1 & -(0)I_2 & -(2k)I_3 & +(15k)I_4 & -(3k)I_5 \\ -(0)I_1 & -(0)I_2 & -(2k)I_3 & -(3k)I_4 & +(14k)I_5 \end{bmatrix} \begin{bmatrix} 1V \\ 5V \\ -2V \\ 0V \\ 2V \end{bmatrix}. \quad (2)$$

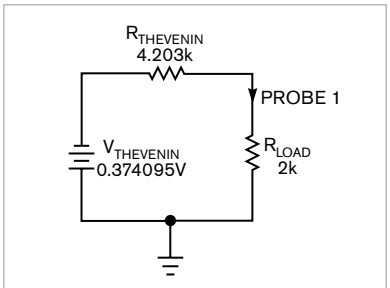

Figure 4 In the Thevenin-equivalent circuit, current flows to the left, so the $V_{THEVENIN}$ terminal is grounded.

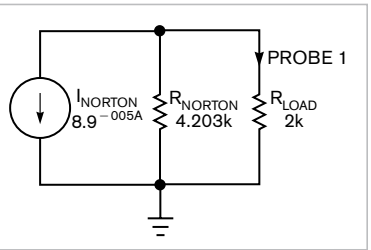

Figure 5 In the Norton-equivalent circuit, R_{NORTON} is 4.203 kΩ.

Thus, $V_A = -V_4 + [(I_2 - I_3) \times R_7] \simeq -1.8719$V, where the net current flows downward. Further, $V_B = [(-V_4 + (I_3 \times R_9)) + ((I_3 - I_5) \times R_{10}) + V_2] \simeq -1.498$V, where the net current in R_{10} flows downward. Thus, $V_{THEVENIN} = V_A - V_B \simeq -374$ mV, and you can calculate $R_{THEVENIN}$ according to the previous description. EDN

DAC and flip-flops form constant-current source

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The Analog Devices (www.analog.com) AD5422 16-bit serial-input DAC lets you program for a voltage output or a current output. To communicate with the DAC and produce a variable output, you need a data SERDES (serializer/deserializer). If your design needs a constant 4-mA output, however, you can program the device with two flip-flops and test it with S_1, a mechanical pushbutton switch (**Figure 1**).

The AD5422's programming uses a 24-bit word in which the upper eight bits form an address for a control register and the lower 16 bits set the DAC's output range, slew-rate step, and slew-rate clock (**Table 1**, pg 52). Programming a 24-bit 0101 ... 01 pattern into the AD5422 sets it to the bottom of the simultaneously selected current range, 4 to 20 mA at the output-current pin (Pin 19). The AD5422's internal shift-register data moves into the data register at every low-to-high transition of the latch signal (Pin 7). The device interprets this alternating bit sequence as a control command during the 23rd time you press and release the switch after IC_1's power-up. After that sequence, the SCLK signal can remain idle (**Figure 2**).

Flip-flop FF_1, configured as a familiar divide-by-two counter, produces the desired alternating sequence. Manually pressing and releasing the pushbutton switch, you cause the generation of an SCLK signal. You must use a debounc-

er because the circuit requires a clean logic signal for SCLK with level transitions that do not exceed a few 10s of nanoseconds. FF_2 acts as an asynchronous set/reset flip-flop that debounces the signal from the button.

For the circuit to work properly, the active low-to-high transition of the latch signal must occur at least 13 nsec after the low-to-high transition of SCLK. You can fulfill this requirement by using the SN74HC74-class flip-flop. The Q output of FF_1 in IC_2 connects to the SDIN input of IC_1. The level transitions at the SDIN input must have preset and hold times of at least 5 nsec with respect to low-to-high transitions of the SCLK signal. You can derive the supply voltage of 5V for the pull-up resistor at the $\overline{FAULT}$ output of IC_1 (Pin 3) for IC_2 from the AD5422's precision 5V reference. The tiny current surges due to loads appear at the initializing state, at clocking in the control word to IC_1, or in a faulty state when the open-drain $\overline{FAULT}$ output of IC_1 is active. Fortunately, either the output current (Pin 19) is not yet flowing, or an overtemperature condition or an excessive value of the load resistor causes external damage to the precision of this current. In either case, the external loading of the internal reference

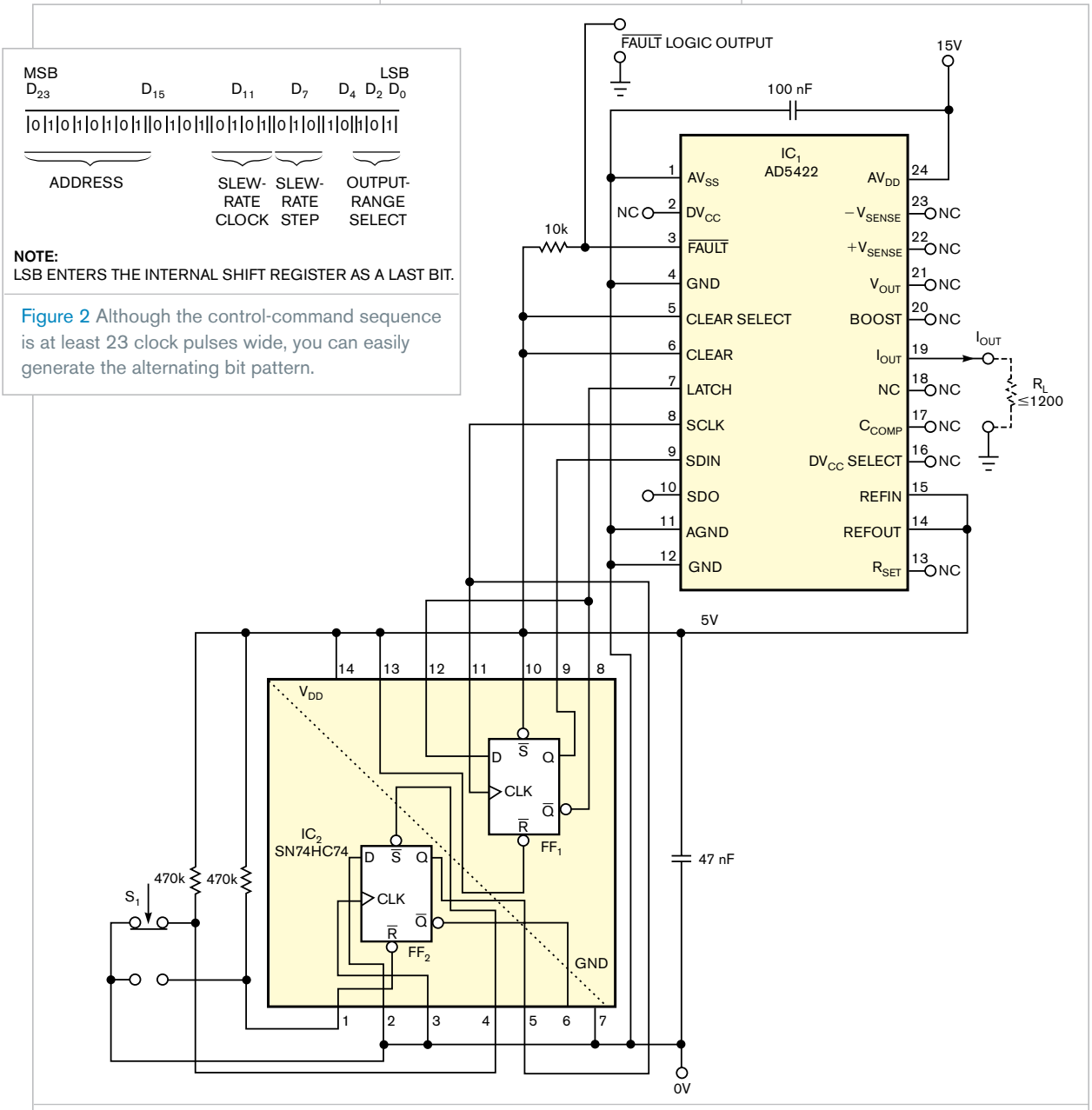

Figure 2 Although the control-command sequence is at least 23 clock pulses wide, you can easily generate the alternating bit pattern.

Figure 1 After you press and release S_1 23 times, the DAC produces a constant-4-mA-current output.

source, which is no more than a few 10s of microamperes, is harmless to the precision of the reference source.

By connecting a high-precision, 100Ω resistor between the I_{OUT} pin and ground and generating 23 clock pulses, you can measure a voltage of 0.400xV on this resistor, where x≤4, confirming the high-precision, constantly flowing current of 4 mA. The actual full-scale-range error of IC_1 is far below its guaranteed worst-case value of ±0.3% full-scale-range error (**Reference 1**). Hence, you must divide the observed relative error of the 4-mA current, with a value not exceeding 0.1%, by four because the current scale is 20 mA−4 mA=16 mA. The total full-scale-range error of the DAC in this case is thus less than 0.1%/4, or 0. 025%. By using the constant-current source employing a monolithic DAC, you get high resolution, negligible sensitivity to temperature, immunity to supply-voltage variations, and high initial accuracy. Current-output DACs also exhibit output resistance in the 10s of megohms.

This circuit uses S_1 to generate the SCLK signal for testing purposes only. For power-on-the-go applications, you can use a free-running clock with a frequency as high as 200 kHz. You can supply the pull-up resistor at the $\overline{FAULT}$ output and IC_2 from the AD5422's DV_{CC} pin. EDN

TABLE 1 EFFECTS OF THE SINGLE BITS OF THE CONTROL COMMAND

$D_2D_1D_0$=101	Selects 4- to 20-mA current range
D_3=0	Disables daisy-chain operation
D_4=1	Enables slew-rate control
D_7 to D_5=101	Selects slew-rate size of 4 LSB
D_{11} to D_8=0101	Selects slew-rate update-clock frequency of 69.444 kHz
D_{12}=1	Enables outputs
D_{13}=0	Deactivates external-resistor pin
D_{14}=1	Increases output voltage by 10%
D_{15}=0	Concerns only the voltage output

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1 "Single Channel, 12/16-Bit, Serial Input, Current Source and Voltage Output DACs, AD5412/AD5422," Analog Devices, 2008, www.analog.com/static/imported_files/data_sheets/AD5412_AD5422.pdf.

Convert negative inputs to positive outputs

Shane Chang and Budge Ing, Maxim Integrated Products, Sunnyvale, CA

You can obtain a precise, positive-output voltage from a negative-voltage supply with a boost converter and a linear regulator. The input and output capabilities of the circuit in **Figure 1** depend on the allowable I/O voltages of IC_1 and IC_2. In this case, IC_1 and IC_2 convert a −5V input voltage to a 3.3V output voltage.

IC_1 is a boost converter that accepts −5V when its V_{CC} pin connects to common ground—that is, the ground of the negative-power-supply input. Voltage divider R_1/R_2 at IC_1's output provides feedback that sets the output voltage 10.5V above IC_1's ground pin. With the feedback-threshold voltage factory-set to 1.226V, you can choose values for R_1 and R_2 using this **equation**: $(1.226V/R_2)\times(R_1+R_2)=10.5V$. Current through R_1 and R_2 should be at least 2 µA. The IC_1 output, which is IC_2's input, is 10.5V higher than −5V, which is 5.5V with respect to common ground.

IC_2, a linear regulator whose ground pin connects to the common ground, accepts input voltages as high as 6.5V. Its output is factory-set at 3.3V. **Figure 2** shows the output voltage versus the output current for the circuit in **Figure 1** with input voltages of −4.5, −5, and −5.5V. EDN

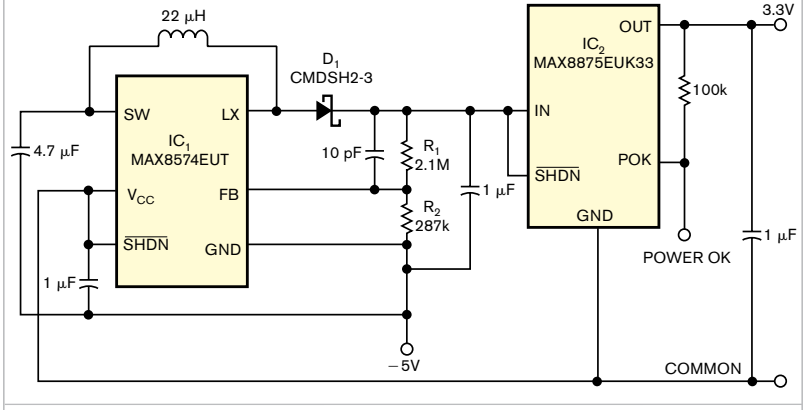

Figure 1 A two-IC circuit converts a −5V input to a 3.3V output.

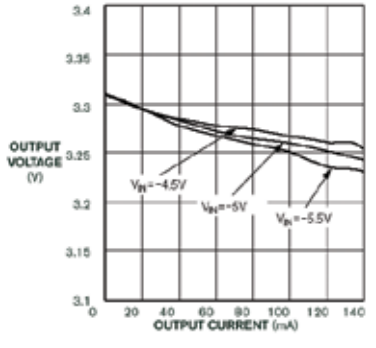

Figure 2 The circuit's output voltage drops as current increases. Plots indicate source voltages of −4.5, −5, and −5.5V.

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CMOS-NAND gates control sump pump

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With just a few NAND gates, you can control sump pumps and other pumps that keep your basement from flooding and maintain water levels in tanks. The circuit in **Figure 1** receives 12V signals from L_1, the lower water level, and L_2, the upper level, of an underground tank. You adjust the gap between these two levels to avoid short cycling of the pump. When the water level touches the maximum level of L_2, the pump switches on to fill up the overhead tank. When the water level falls below the low level of L_1, the pump switches off.

When the tank is empty, sensors L_1 and L_2 and Gate D are at low levels because the outputs of gates B and A are high. When the water level rises and shorts 12V through L_1, the gate outputs remain the same. When the water level further rises and shorts 12V with L_2, then the output of Gate A becomes low, which forces Gate D to a high level. That action, in turn, latches Gate B's output low. A low output on Gate B pulls down the SSR (solid-state relay), which turns on the sump pump (**Reference 1**). Simultaneously, the high output of Gate D turns on the gated oscillator and sounds the piezoelectric buzzer.

When the water level lowers below level L_2, the pump remains on because of the latched B and D gates. If the water level falls below sensor level L_1, the output of Gate B becomes high, which turns off the pump. This action

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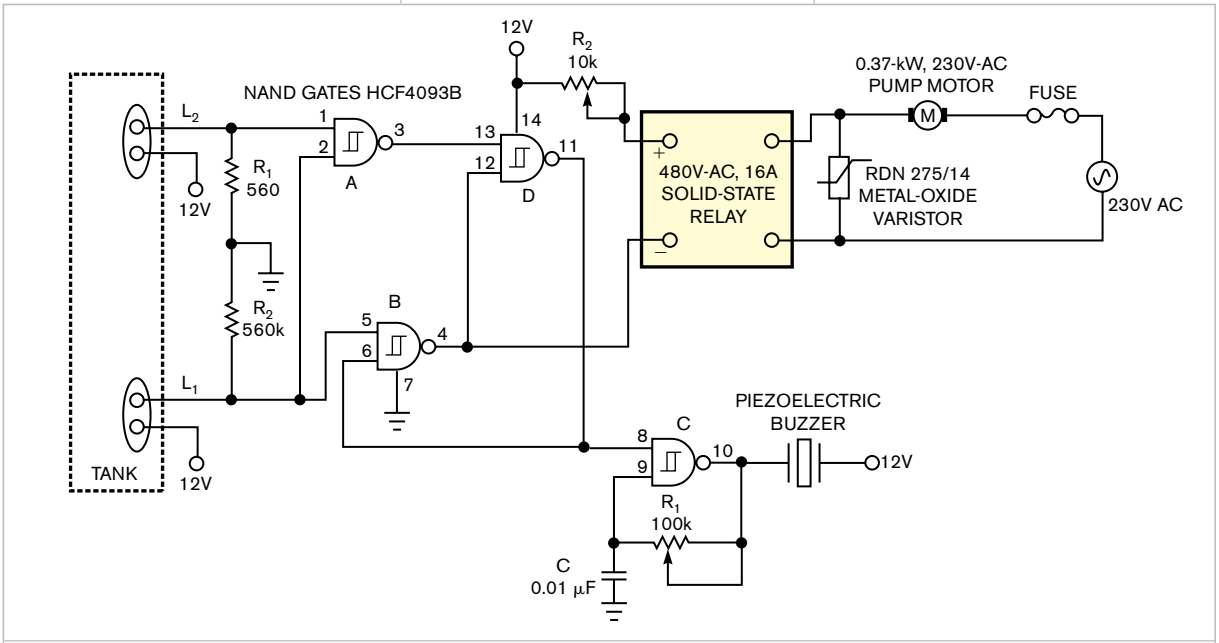

Figure 1 A sump-pump controller uses a quad-NAND gate to drive a solid-state relay.

makes the output of Gate D go to a low level, which stops the oscillator and thus the piezoelectric buzzer.

The circuit uses HCF4093B Schmitt-trigger-input NAND gates to square the slow signals. The input resistor, R_1, has a value of 560 kΩ. Checking the circuit with a glass of filtered water shows an improved conductivity for ground water. Raising the value of the input resistor to a higher value is also not objectionable after you account for pickup and the voltage drop across the resistor due to the input leakage current.

The solid-state relay may have back-to-back connected SCRs (silicon-controlled rectifiers), random turn-on, and snubber circuitry to handle the motor load (**Reference 2**). Choose an SSR with a voltage rating that is double the working voltage and five to 10 times the current rating of the motor for withstanding dV/dt and the surge current. You should also use fast-blow fuses or semiconductor fuses with less than the I^2t rating of the SSR, where I is the current and t is the duration of current flow in seconds. Choose appropriate SSRs for different ratings of pump motors.

THE PARALLEL SENSOR WIRES AVOID THE CHANCE OF A MOISTURE INTERFACE BETWEEN THE WIRES WHEN THE WATER LEVEL FALLS BELOW THE SENSORS.

This circuit uses sheathed, single-strand, thick-gauge, edge-stripped copper wires as sensors. You can connect the sensor wires in two-way porcelain connecters, which you house in a box and place at the top of the tank. The parallel sensor wires avoid the chance of a moisture interface between the wires when the water level falls below the sensors. You can also use any other high-conductivity and noncorrosive wire material in some configurations. The power supply is floating.

With few modifications, the circuit in **Figure 2** can perform a slightly different function. Assume that you have a tank in which you want to maintain a level of water or any conductive liquid. Mount sensors L_1 and L_2 in the tank the same as those in **Figure 1**. Switching on the power supply causes the pump to begin to fill up the liquid in the tank. When the level reaches L_2, the pump turns off. The pump remains off until the level falls to L_1. When the level falls below L_1, the pump again starts filling the tank until it reaches L_2. The piezoelectric buzzer announces that the pump is running.

You can also control pumps with three-phase motors using a three-phase SSR or adding one appropriately rated single-phase SSR to this circuit. In this case, you can connect the inputs of the two SSRs in series. One SSR on each phase controls two of the phases, and you directly connect the third phase. EDN

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2 "Single-phase SSRs," ERI Solid State Relays, 2007, www.electronicrelaysindia.com/prod_001sjk_3.html.

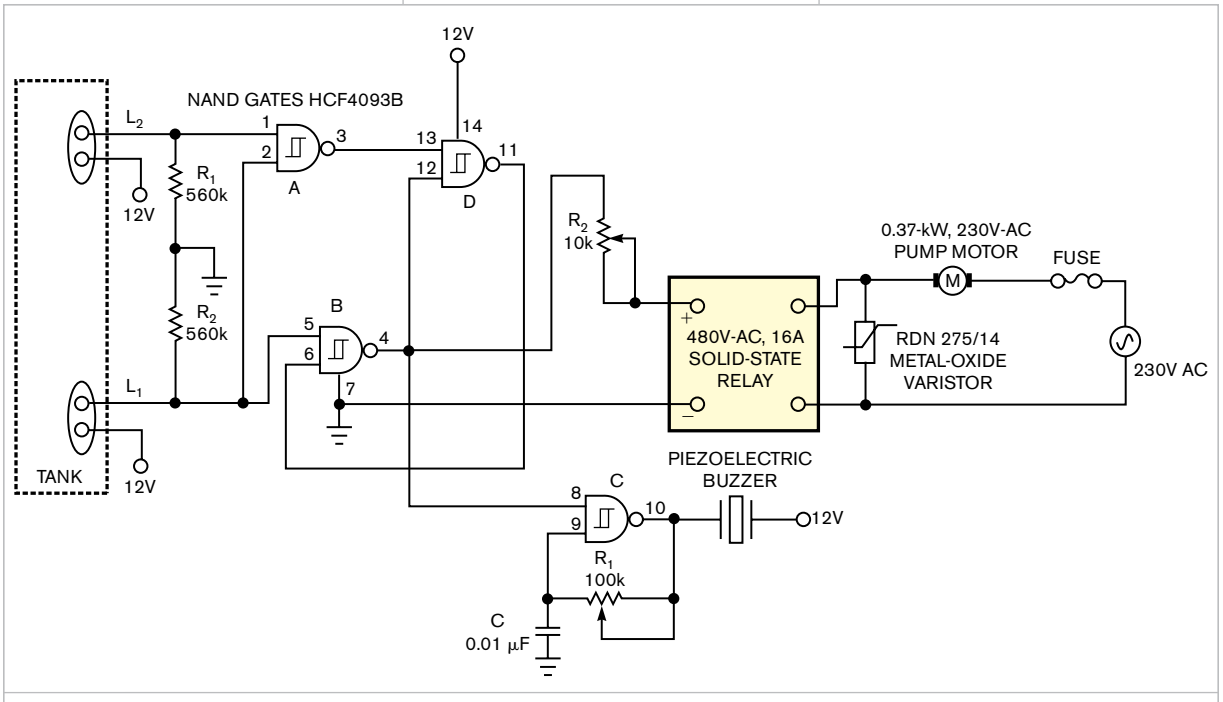

Figure 2 Connecting the potentiometer to NAND Gate B creates a water-level controller.

Use an LED to sense and emit light

Rafael Camarota, Altera Corp, San Jose, CA

LEDs in portable devices often show power status, battery status, or Bluetooth-connection activity. LEDs can be major factors in determining battery life because their intensity is directly proportional to power drain. Using a simple circuit, the MAX IIZ CPLD from Altera (www.altera.com) can measure the analog-light level of its environment and then drive an LED at a proportional analog intensity level. A single LED can both sense and emit light with the same LED and bias resistor. The circuit in **Figure 1** requires only 45 logic elements, and the programmability of the CPLD makes it easy to quickly adjust the parameters of the circuit to the characteristics of any LED.

You can reduce the power consumption of a flashing LED by increasing the flash period, decreasing the flash pulse width, or decreasing intensity. Controlling the LED intensity based on ambient light reduces LED energy usage by more than 47% without affecting appearance. **Figure 1** shows a circuit that uses an Altera EMP240ZM100C7N CPLD, LED, resistor, and clock source to blink an LED with an intensity proportional to ambient light. The circuit comprises a PWM (pulse-width modulator) for driving the LED, a light-intensity-measurement block, and a controlling state machine and timer.

The state machine includes one hot state comprising an 8-bit shift register initialized to the 00000001 binary. The carryout of Count 12, a 12-bit counter, generates an 8-Hz enable signal for state machine Shift 8. Thus, each of the eight states of the state machine is active for 125 msec. In State 0, the reset state, PWM Count 4 block and light-measurement block Count 8 are reset. State 1 is the light-intensity-measurement state, which enables a frequency counter, Count 8. Enabled for 125 msec, Count 8 counts the cy-

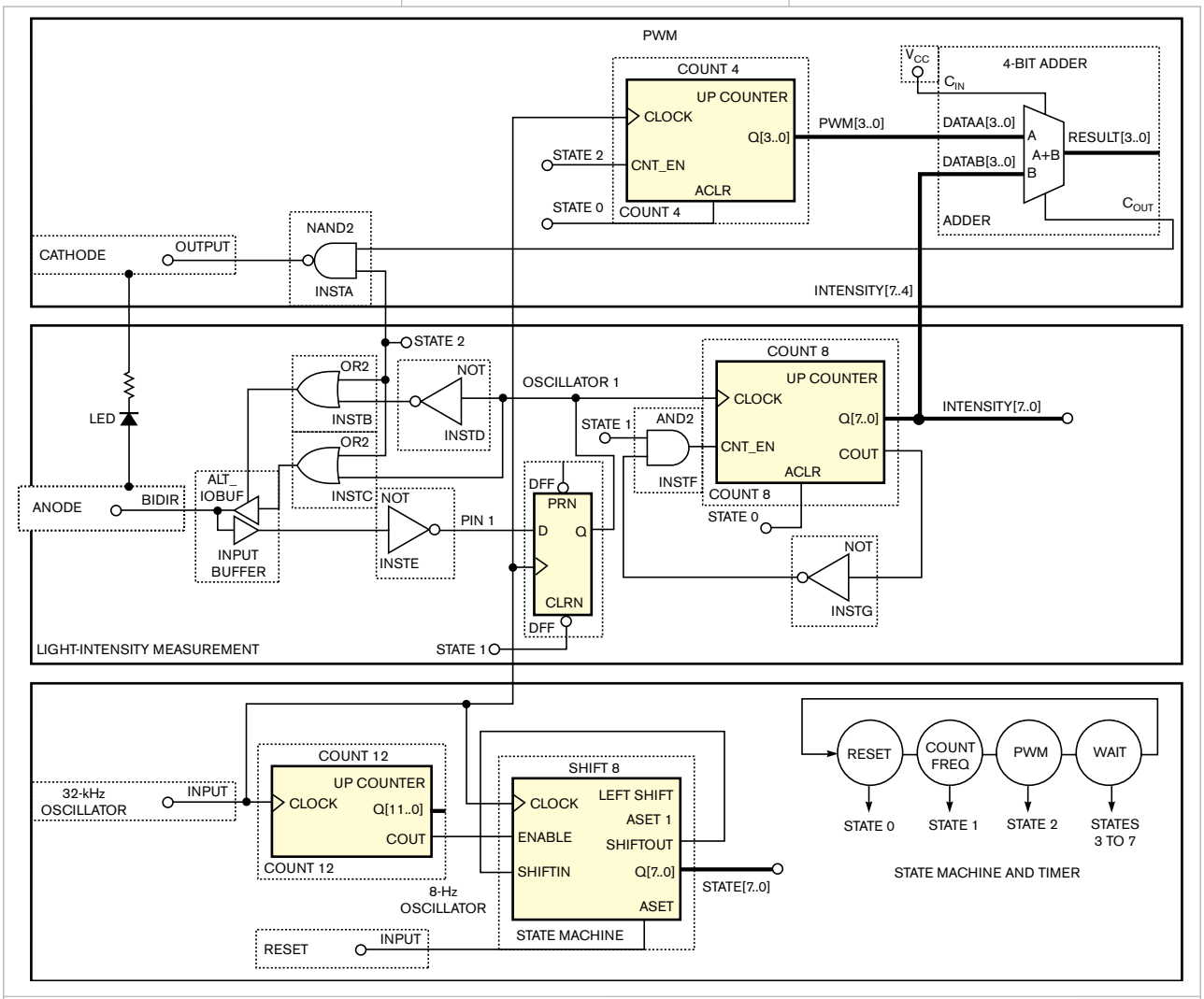

Figure 1 This simple MAX IIZ circuit uses an LED as an emitter and a sensor.

cles exiting the light sensor. The circuit senses the light by biasing the LED and current-limiting resistor such that the cathode lead of the LED is at logic one. The anode connects to a relaxation oscillator that starts with anode at logic zero. The LED pulls up the anode in proportion to the amount of light hitting the LED. The reverse-biased LED acts as a solar cell with output current proportional to light. Once the slow-rising anode signal reaches the threshold of the input buffer, the Pin 1 signal becomes a zero, and the D flip-flop, DFF, toggles to zero and drives the anode signal to zero, making Pin 1 a logic one and tristating the input buffer on the next clock cycle, allowing the anode signal to rise again.

The frequency of Oscillator 1 is proportional to light intensity, with typical frequency for bright light of approximately 2000 Hz. The Oscillator 1 signal drives the clock of Count 8. Count 8 resets in State 0 and then is enabled in State 1 for 125 msec. In bright light, Count 8 might count to 250 at the end of the measurement, and, in low light, it might count to only 16. The counter's C_{OUT} signal feeds back to the enable so that the count will saturate at a count of 255 and prevent high-intensity light from wrapping the counter back to zero and taking a false measurement.

State 2 is the LED's blinking state. This state blinks the LED for 125 msec at an intensity that a PWM controls. In State 2, the cathode and anode pins are bias to the emitter mode. The emitter mode forces the anode signal to V_{CC}. The cathode node connects to the PWM output. A logic zero on the cathode node lights the LED, and a logic one turns it off. The cathode signal is the inverted form of the PWM output.

In this example, the PWM is a 4-bit-resolution PWM, but you can use more or fewer bits. The PWM comprises binary counter Count 4 and a binary, 4-bit adder. The Count 4 counter is enabled in State 2, and the cycling output connects to the A input of the 4-bit adder. The B input of the adder connects to the four MSBs (most significant bits) of the light-sensor-frequency counter. The carryout of the adder is the PWM output. The carry-in of the adder is a constant logic one.

The following examples show how the PWM works:

- A logic zero from the intensity measurement results in a logic zero at carryout when Count 4 is zero through 14 and a logic one when Count 4 is 15. This 6.25% duty cycle is a very low-intensity level.
- A value of seven from the intensity measurement results in a logic zero at carryout when Count 4 is zero to seven and a logic one when Count 4 is eight to 15. This 50% duty cycle is a medium-intensity level.
- A 15 from the intensity measurement results in no logic zero at carryout for any Count 4 value and a logic one when Count 4 is zero through 15. This 100% duty cycle is a full-intensity level.

The only function of states 3 to 7 is to wait for the next LED-flash cycle. You can add or remove states to change the flash rate. EDN

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Two instrumentation amps make accurate voltage-to-current source

Frank Ciarlone, Analog Devices, Wilmington, MA

Many designs require precise voltage-controlled current sources, especially in the presence of variable loads. Common approaches, which use a few op amps and a handful of passive components, have inherent errors due to nonideal component characteristics, such as finite open-loop gain, common-mode rejection, bias current, and offset voltage. Designs using operational amplifiers may require precision resistors to set gain and additional capacitors for stability. In addition, some circuit designs provide currents that are not directly proportional to the input voltage. The voltage-to-current converter in **Figure 1**, for example, relies on the fact that the collector current is approximately equal to the emitter current and provides current in only one direction.

With two instrumentation amplifiers and two transistors, you can build a 0.01%-accurate voltage-controlled current source (**Figure 2**). This current source features a ±10V input-voltage swing that is directly proportional to the output current. It maintains high accuracy, even while delivering as much as 90 mA of output current. The AD620 low-power, low-drift instrumentation amplifiers from Analog Devices (www.analog.com) provide circuit control and error correction but are not part of the output circuit. Thus, you can substitute higher-power transistors for Q_1 and Q_2 to achieve higher output currents. You can configure the instrumentation amplifiers for any gain of one to 10,000 to accommodate input signals lower than 1 mV. Simply connect a resistor across the inputs of both IC_1 and IC_2 to achieve the desired gain.

The first instrumentation amplifier, IC_1, controls the base voltage of the push-pull output stage. The resistors

and diodes provide bias to Q_1 and Q_2 to eliminate crossover distortion. IC_2 provides error correction and accounts for deltas in the base-to-emitter voltage. The error voltage, which you measure differentially from the D_1/D_2 junction to the output voltage, feeds into the reference pin of IC_1, summing it with the input voltage. The result is an output current that is directly proportional to the input voltage. This circuit achieves a 0.01% typical dc accuracy across a ±10V input span and 1.5% typical ac accuracy at 1 kHz with an output voltage of ±5V p-p.

The **equations** for calculating the output current are:

$$V_{OUT_{IC1}} = \left[\left(V^{+}_{IC1} - V^{-}_{IC1}\right)A_{IC1} + V_{REF_{IC1}}\right].$$

$$V_{REF_{IC1}} = V_{OUT_{IC2}} = \left(V^{+}_{IC2} - V^{-}_{IC2}\right)A_{IC2} + V_{REF_{IC2}}.$$

$$V_{OUT} = V_{OUT_{IC1}} = \left(V^{+}_{IC1} - V^{-}_{IC1}\right)A_{IC1} + \left(V^{+}_{IC2} - V^{-}_{IC2}\right)A_{IC2} + V_{REF_{IC2}},$$

where

$$V^{+}_{IC1} = V_{IN},\ V^{-}_{IC1} = 0;\ A_{IC1} = A_{IC2} = 1;\ V_{REF_{IC2}} = 0.$$

Therefore,

$$V_{OUT} = V^{+}_{IC1} + \left(V^{+}_{IC2} - V^{-}_{IC2}\right),$$

or

$$I_{OUT} = \frac{V_{IN}}{R_L}.$$

This circuit provides a wide output range, as well as output current that is directly proportional to the input voltage and high linearity and precision (**Figure 3**).EDN

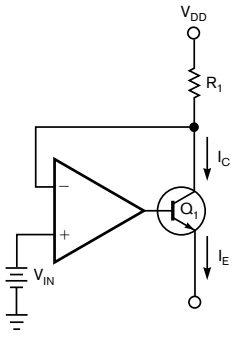

Figure 1 The voltage-to-current converter relies on the fact that the collector current is approximately equal to the emitter current and provides current in only one direction.

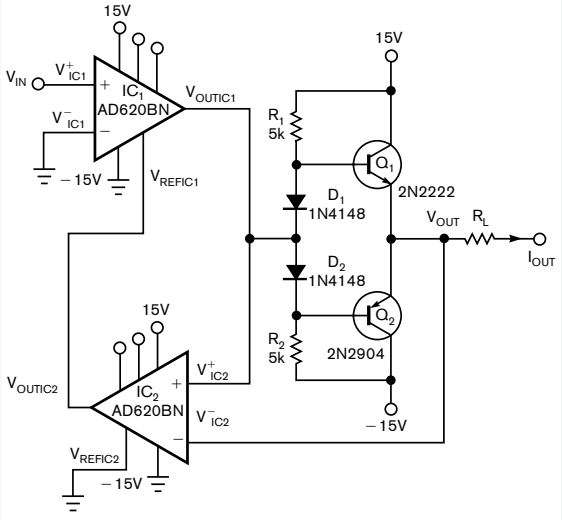

Figure 2 This handy voltage-to-current converter delivers high accuracy over a range of conditions.

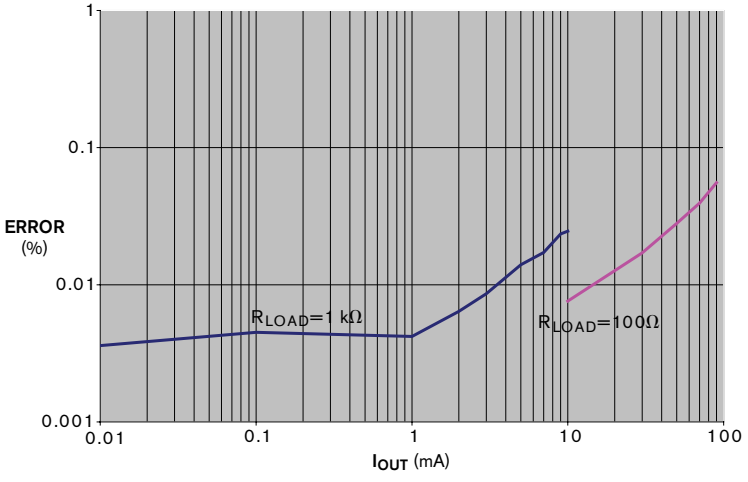

Figure 3 The circuit in Figure 2 provides a wide output range, output current that is directly proportional to the input voltage, and high linearity and precision.

Simple circuit indicates health of lithium-ion batteries

Fritz Weld, Friedberg, Germany

Lithium-ion batteries are sensitive to bad treatment. Fire, explosions, and other hazardous condition may occur when you charge the cell below the margin that the manufacturer defines. Modern battery chargers can manage the hazardous conditions and deny operation when illegal situations occur. This fact doesn't mean, however, that all cells are bad. In most cases, you can replace the discharged battery and increase your device's lifetime. **Figure 1** shows the circuit for testing battery packs.

When the supply voltage is lower than 2.6V, no current drives the base of the transistor. LED_1 lights up, and

LED_2 is off. When the voltage exceeds 2.6V, the transistor begins to short LED_1, turning it off and lighting LED_2. This condition indicates that the battery is below the allowed limit for recharging. The voltage margins highly depend on the type or color of the chosen LEDs. A standard red LED has a forward voltage of 1.7V; a green LED, about 2.1 or 2.2V. The circuit in this design uses red LEDs with forward voltages of approximately 1.6V at 2 mA. Other LEDs may require a simple redesign, mostly resulting in the requirement for a Schottky diode instead of the 1N4148 in this circuit. Even white or blue LEDs with 3V or more forward voltage make sense for certain applications.

Lower-value resistors increase the brightness of the LEDs but increase the supply current, as well. **Table 1** shows how this indicator provides three states of operation. Although this simple device draws little current, you cannot expect a long battery life if you use the device as a permanent display, especially when it is in storage. Although a fully charged 32-Ahr cell will expire after about a year, an empty battery of the same size but slightly higher than the allowed margin for charging will expire after one or two days.

You can build an array of indicators in one test module. By connecting to the measuring/balancing port of the pack, you can easily inspect a whole pack with one view. Adding zener diodes in series to the LEDs also makes this circuit a simple indicator for higher voltage levels. EDN

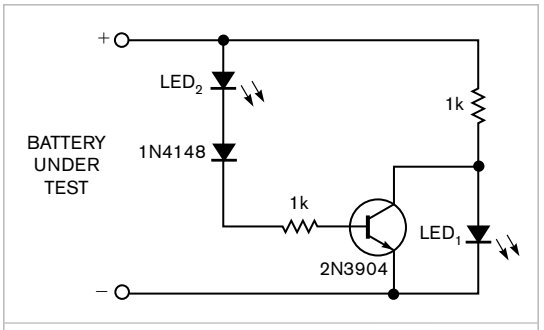

Figure 1 LEDs indicate the health of a battery based on its voltage.

TABLE 1 POSSIBLE LED CONDITIONS FOR BATTERY VOLTAGES

LED_1	LED_2	Indication	Condition
Off	Off	0 to 1.6V	Battery is empty, defective, or unusable.
On	Off	1.7 to 2.5V	Battery is below allowed limit for recharging.
Off	On	More than 2.6V	Battery is OK and can be charged.

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READERS SOLVE DESIGN PROBLEMS

Current-sense monitor and MOSFET boost output current

Gyula Diószegi and János Nagy, Divelex Ltd, Budapest, Hungary

A previous Design Idea describes a programmable current source that used a three-terminal National Semiconductor (www.national.com) LM317 adjustable regulator (**Reference 1**). Although that circuit lets you program the output current, the load current flowed through the BCD (binary-coded-decimal) switches. However, you may find it difficult to purchase BCD switches that can handle more than 25 mA, limiting the circuit's output current. By applying the simple, four-pin Zetex (www.zetex.com) ZXCT1010 current-sense-monitor chip, you can boost current because it doesn't flow through BCD switches (**Figure 1**). The load current results in a voltage on the sense resistor R_{SENSE}. The voltage on R_1, the 100Ω resistor, is the same as that on R_{SENSE}, generating an output current on R_1: $I_{OUT}\times100=I_{LOAD}\times R_{SENSE}$, and $V_{OUT}= I_{OUT}\times R_{OUT}$, where I_{OUT} is the output current, I_{LOAD} is the load current, and V_{OUT} is the output voltage. You can apply the output voltage as a control voltage to regulate the load current.

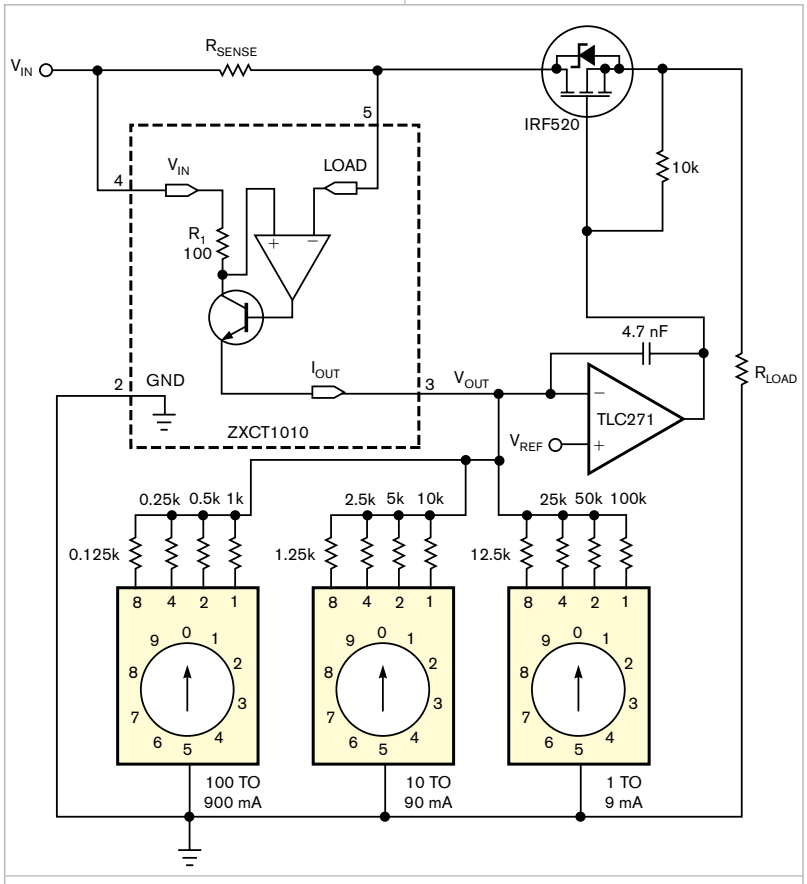

Figure 1 Passing current through a MOSFET and regulating it with a current-sense monitor bypasses the BCD switches, letting you increase load current.

One application for this circuit would be to refill accumulators in portable devices. In this case, the circuit works at 18V. The Fairchild Semiconductor (www.fairchildsemi.com) IRF520 is an N-channel, power-MOSFET chip in an aluminum heat sink with as much as 9.2A current and 0.27Ω drain-to-source resistance to connect the load current. An op amp controls the IRF520 in the feedback of the load current. In this application, the maximum output current is 1A, and the value of the sense resistor is 0.1Ω. The PCB (printed-circuit board) can also have this small resistance value, which you calculate using

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the cuprum material's 35-micron-thick layer. The BCD switches are in parallel and connect from 125Ω to 100 kΩ to adjust the output voltage on the op amp's negative input. The equations to calculate resistor values are: $V_{SENSE}=R_{SENSE}\times I_{LOAD}$, $I_{OUT}=R_{SENSE}\times I_{LOAD}/100$, and $R_0=V_{REF}\times 100/(R_{SENSE}\times I_{LOAD})$. If you choose a value of 0.1Ω for the sense resistor and a value of 0.1V for the reference voltage, the **equation** becomes $R_0=100/I_{LOAD}$.

Applying this **equation**, you can calculate the four weighting resistors of the three BCD switches, which you can determine when the current flows through only that resistor. For currents of 800, 400, 200, 100, 80, 40, 20, 10, 8, 4, 2, and 1 mA, the corresponding resistances would be 0.125, 0.25, 0.5, 1, 1.25, 2.5, 5, 10, 12.5, 25, 50, and 100 kΩ. If the load current is 1A, then the output current is only 1 mA, and, if the load current is 1 mA, then the output current is only 1 µA. Note that the IRF520's surface is on the drain potential. EDN

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1 Guy, John, "Programmable current source requires no power supply," *EDN*, June 12, 2008, pg 70, www.edn.com/article/CA6566536.

Multiplexed, programmable-gain, track-and-hold amplifier has instrumentation inputs

W Stephen Woodward, Chapel Hill, NC

ADCs need adequate signal-acquisition analog interfaces to perform at their best. The classic general-purpose ADC front end includes multiple channels of differential input, digitally programmable gain, and track-and-hold capability. This Design Idea presents a new, complete, high-performance, low-parts-count ADC front end that implements the standard ensemble of functions (**Figure 1**). However, it also incorporates the concepts of the flying-capacitor differential input and the divergent-exponential negative-time constant that an earlier Design Idea describes (**Reference 1**). This Design Idea adds to that circuit multiplexed inputs and a versatile track-and-hold function.

The multiplexer address and the state of the hold-mode bit control signal acquisition and conditioning. With a hold state of zero and the multiplexer's address equal to the selected input channel, the flying capacitor, C_1, connects to the positive and negative differential-input terminals, which acquire the input voltage. Moving the hold state to one isolates C_1 from the input. Then, the multiplexer's address becomes zero, and the hold state returns to zero, initiating regenerative negative-time-constant exponential amplification of the input voltage. From that point until the point when hold reasserts and a connected ADC samples and converts the output voltage, the input voltage and the output voltage are divergent exponential functions of time, with a gain equal to $2^{(1+t/10\ \mu sec)}$.

Building on the assets of that earlier design, this new circuit has the desirable features of multiple instrumentation-style differential inputs. Also, neither resistor matching nor the CMR (common-mode rejection) of the op amp limits the circuit's CMR. Stray-capacitance issues do have an effect on CMR, but you can minimize this capacitance by careful circuit layout. The circuit also has rail-to-rail inputs and virtually unlimited programmable gain. Further,

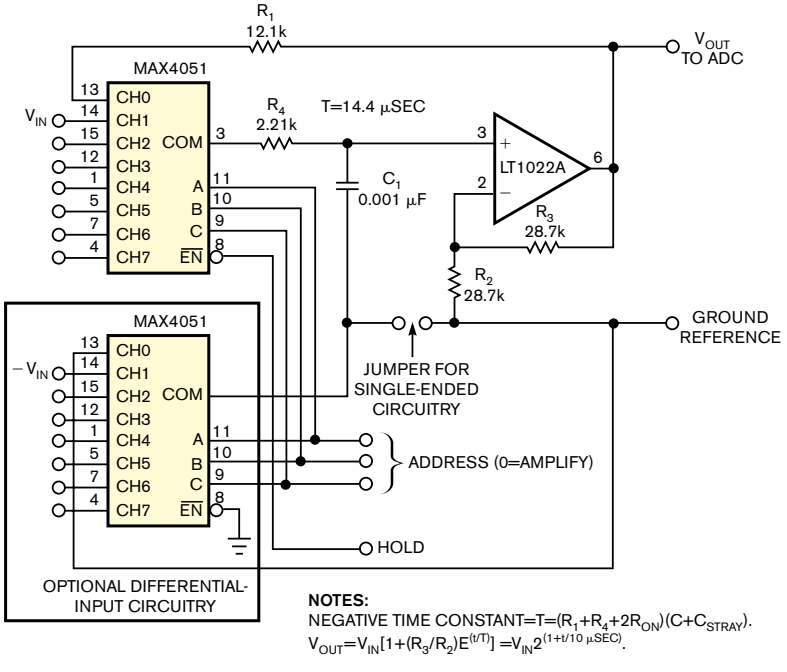

Figure 1 This high-performance, low-parts-count ADC front end implements the standard ensemble of functions.

only the resolution of the amplify interval's timing limits gain-set resolution (**figures 2** and **3**). This circuit also has ±10V output-amplitude capability—two to four times greater than that of monolithic digitally programmable-gain instrumentation amplifiers.

The inherent noise and dc accuracy of the chosen op amp, the accuracy and repeatability of the timing of exponential generation, ADC sampling resolution, and RC-time-constant stability are the main limits on signal-processing performance and the amplifier's precision—for example, its gain-programming accuracy, dc error, noise, and jitter. In the circuit, 1 nsec of the amplify-interval timing error or jitter equates to 0.007% of gain-programming error. EDN

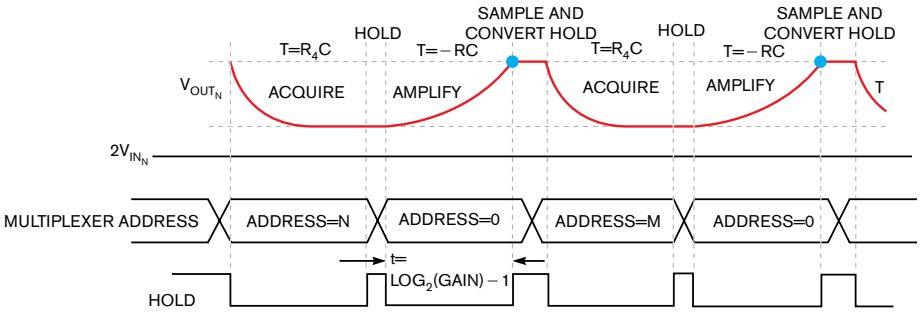

Figure 2 Only the resolution of the amplify interval's timing limits gain-set resolution.

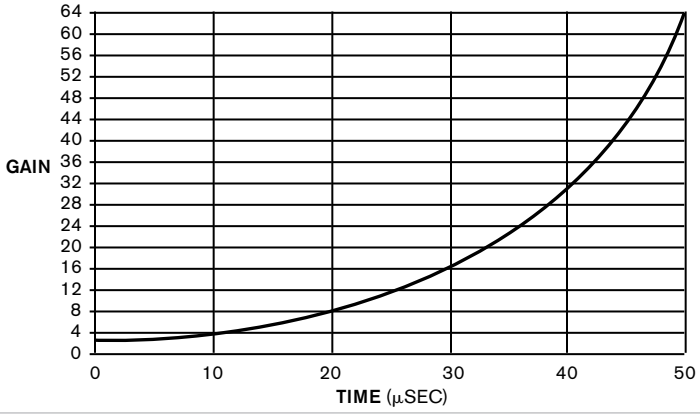

Figure 3 This graph of input- and output-voltage gain shows the time elapsed since the track/amplify-logic transition.

REFERENCE

1 Woodward, W Stephen, "Flying capacitor and negative time constant make digitally programmable-gain instrumentation amplifier," *EDN*, Feb 5, 2009, pg 48, www.edn.com/article/CA6632372.

Simple circuit smoothly drives stepper motors

Uwe Schüler, Institute of Physiology, Tübingen, Germany

The circuit in this Design Idea drives low-power, unipolar stepper motors using only a shift register, a few resistors, and low-power transistors. Adding an inexpensive 4053 analog switch allows bidirectional switching. Compared with other simple stepper-motor-drive circuits, it has better-than-half-step characteristics (**Figure 1**).

After power-up, all shift-register outputs are in a zero state. Pin QP3 feeds back to the serial input through an inverter—transistor Q_5 in **Figure 2** and analog-switch IC_2 in **Figure 3**. The circuit generates a sequence of four ones and then four zeros. You can use this pattern to drive, for example, NPN transistors with emitters that tie to ground and collectors that tie to the stepper-motor coils. However,

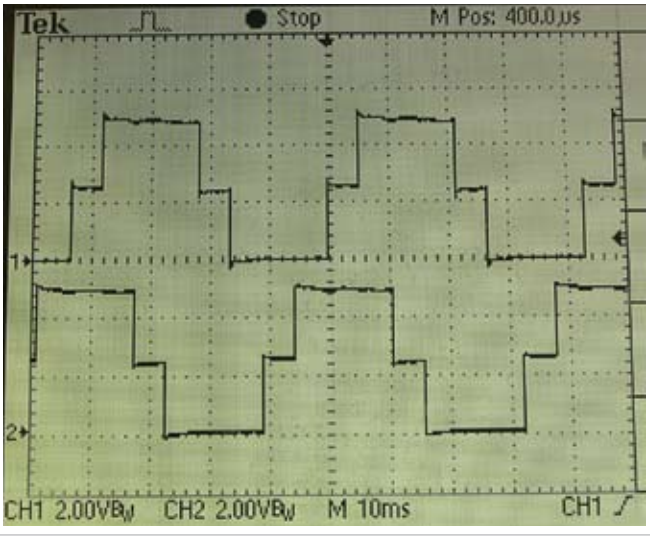

Figure 1 An oscilloscope snapshot shows the base voltages of Q_1 and Q_2 in figures 2 and 3.

to achieve smoother drive characteristics, the shift-register outputs drive four simple DACs, each comprising two identical resistors.

These DACs can generate output voltages of 0, 2.5, and 5V to drive four emitter followers. A snapshot from an oscilloscope shows the base voltages of Q_1 and Q_2 (**Figure 1**). They come close to a quarter-step drive pattern. The circuit can use almost any 8-bit shift register. EDN

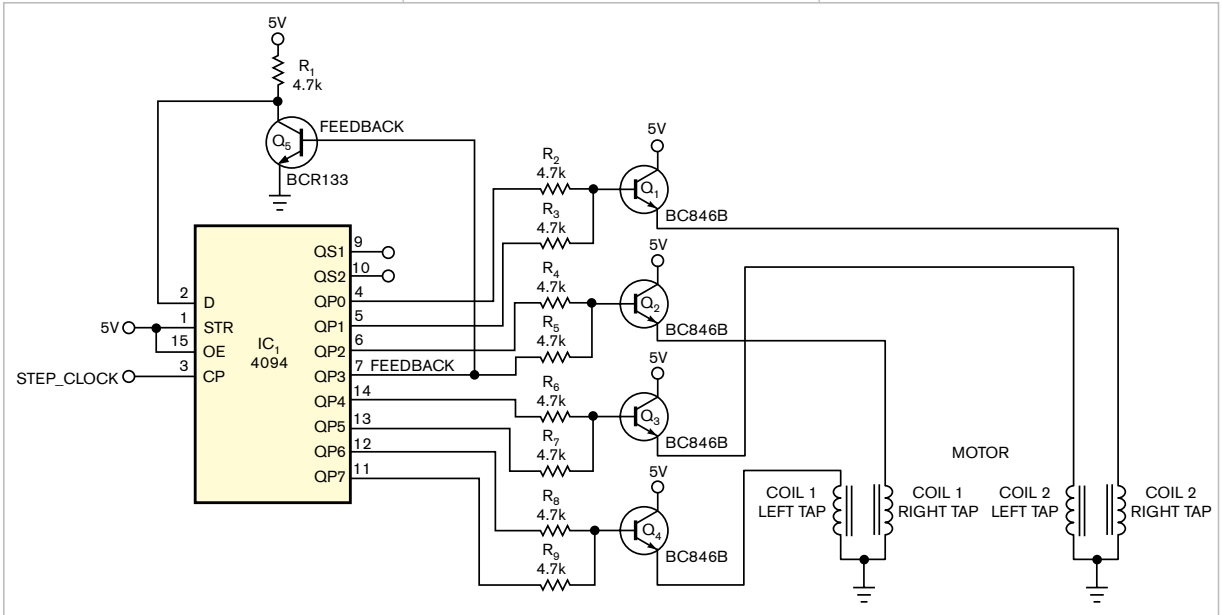

Figure 2 This circuit drives low-power, unipolar stepper motors using only shift-register IC_1 and a few resistors and transistors.

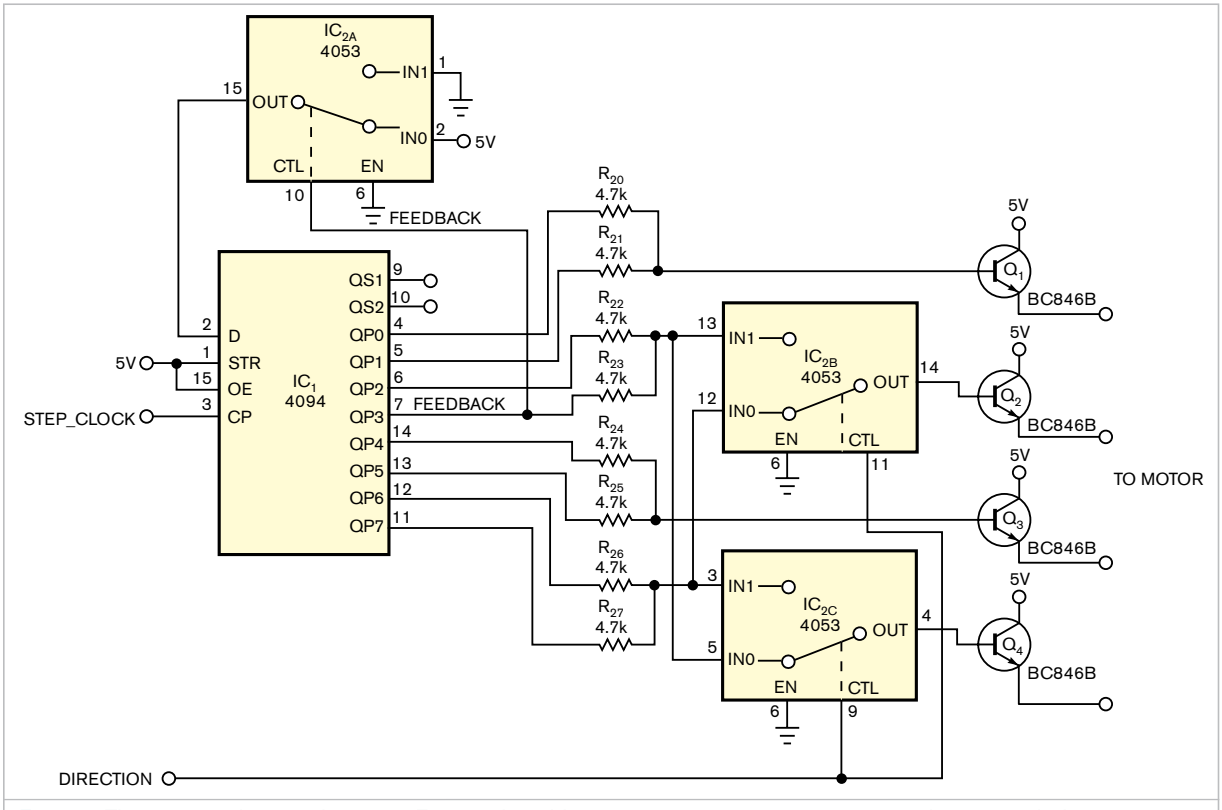

Figure 3 This circuit enhances the one in Figure 2 by adding an inexpensive 4053 analog switch, allowing bidirectional switching.

Excel spreadsheet yields RLC best-fit calculator

Alexander Bell, PhD, Infosoft International Inc, New York, NY

Commercial off-the-shelf software such as Microsoft (www.microsoft.com) Excel lets you automate engineering functions (**references 1** through **3**). This Design Idea explains how you can use Excel to calculate the values of two passive components—resistors, inductors, or capacitors—from the standard E-Series, which comprises E6, E12, E24, E48, E96, and E192, that you can use in circuits such as filters. The application's results depend on whether you select a parallel- or a series-connected topology.

Figure 1 In the user interface, you enter the user-defined functions FitR 1234, P, or E192 into any cell of the Excel worksheet.

The calculations appear in an Excel spreadsheet that you can download from the online version of this Design Idea at www.edn.com/090528dia. The VBA (Visual Basic for Applications) source code for this project resides in a single code module (**Listing 1**, which is also available with the online version of this article). It contains three main public functions, FitR(), FitL(), and FitC(), and several private auxiliary functions. The key algorithm loops through the range of values, trying to find the best fit for the target. There is an inner loop for the first value of RLC and an outer loop for the second one.

Figure 1 shows the user interface. You can enter the user-defined functions FitR 1234, P, or E192 into any cell of the Excel worksheet. The cells accept four arguments and return a text string containing the best-fit values, R_1 and R_2 in this case, and the relative error of approximation. **Table 1** shows the functions' parameter list. For better readability, the spreadsheet returns the values of R_1 and R_2 in commonly used electrical-engineering format by applying a scientific-to-engineering format-conversion function, E2BOM().

The computation engine for electrical resistance and inductance components uses the same formulas: a simple sum of the resistance for the series connection and a sum of conductance for parallel topology, whereas, in the case of the capacitors, the formula is vice versa. You can also fine-tune the functions by changing the constant values corresponding to the upper and lower search limits (**Listing 1**). Thus, you can extend the search range and increase the accuracy, although this process requires more computation time. If you use Microsoft Office 2007, you must contend with an increased security level and set the proper permission level to run the VBA content of the Excel workbook.

This approach is essentially a desktop application, extending the functions of the popular Excel application. You can install the application on either a computer or a network. To further extend its accessibility and bring it to the global level, you should consider an online Web application. The modern RIA (rich-Internet-application) concept and corresponding development tools, available on the market, let you build Web applications with the level of interactivity and responsiveness close to those of the desktop application. A Web-based application provides for easy implementation and maintenance. The user needs only a Web browser. Web applications are essentially platform-independent and globally accessible. Web-based applications of the RLC calculator don't require the user's machine to have MS Office. You can also place the application in password-protected directories from which you can control access to them. A demo version of an online RLC best-fit calculator incorporates the latest set of Microsoft technologies, such as ASP.NET, C#, and Ajax, providing a rich user experience with high interactivity and responsiveness (**Reference 4**). EDN

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2 Bell, Alexander, "Simplify computer-aided engineering with scientific-to-engineering conversion," *EDN*, Sept 30, 2004, pg 94, www.edn.com/article/CA454644.
3 Bell, Alexander, "Voice feedback enhances engineering calculator," *EDN*, July 11, 2002, pg 108, www.edn.com/article/CA231578.
4 Bell, Alexander, "Best Fit RLC Calculator," www.alexanderbell.us/RLC/RLC.aspx.

TABLE 1 FUNCTIONS FITR(), FITL(), AND FITC() PARAMETER LIST

No.	Parameter	Description	Required
1	R	Target value	Yes
2	ParSer	Topology: parallel or serial connection	Yes
3	ESeries	Standard series: E6, E12, E24, E48, E96, or E192	No: Default value is E24
4	ExtSearch	Flag to use preferred search limit or extended	No: Default is preferred search range

Automatically turn secondary lamp on or off

Vladimir Oleynik, Moscow, Russia

You may sometimes need to turn on a secondary device, such as a lamp or an alarm, when a device that is normally on loses power. You can build a simple circuit using just a transformer and a relay for this purpose. In the circuit, a primary load is in series with an ac-mains transformer (**Figure 1**). The transformer connects in an unusual way. Its usual secondary low-voltage winding is Winding 1, and its primary ac-mains winding is Winding 2. Under these conditions, the main lamp's voltage is slightly less than during its ordinary operation—the ac-mains voltage minus the voltage drop over Winding 1. That situation is acceptable in most cases because the lower voltage doesn't greatly affect the operation of the load—that is, the luminosity of the main lamp. Select Winding 1 to match the main load's current needs. In this circuit, a 220V, 50-Hz ac voltage appears at Winding 2.

Connect a relay to Winding 2 so that the secondary loss connects to the relay's NC (normally closed) terminal. Use a relay with a winding that can operate at 220V, 50 Hz for your ac-mains voltage. For example, you can use a TR91-220VAC-SC-C relay from Tai-Shing Electronics Components Corp (www.tai-shing.com.tw). This relay's coil operates at a 220V, 50-Hz, SPDT (single-pole/double-throw) commutation of 240V ac under a 40A load.

Using an SPDT relay adds flexibility in controlling the spare load. It lets you switch a load on or off with no need for additional electronic components. In the **figure**, a spare lamp turns on when the main lamp burns out because the secondary load connects to the relay's NC contact.

Select a transformer whose secondary winding (Winding 1 in the **figure**) has a low-rated voltage that provides sufficient current for the main load—the lamp. Match the relay's rated coil voltage to the ac-mains voltage and frequency specifications. EDN

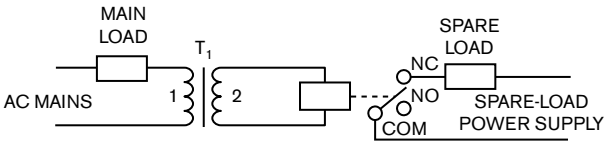

Figure 1 A transformer and a relay are all you need to control a secondary load should the main load fail.

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Fast 10-line-to-one-line data selector/multiplexer comprises only two ICs

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When dealing with logic operations over BCD (binary-coded-decimal) numbers, you often need a 10-line-to-one-line data selector/multiplexer. In the past, you could use the famous 16-line-to-one-line 74150 multiplexer IC. Nowadays, however, when you look at the Web sites of the renowned semiconductor houses for the 150 and similar 16-to-one multiplexers, such as the 250, the 850, or the 851, you find that vendors have labeled them obsolete or no longer available. On the other hand, the eight-line-to-one-line multiplexers not only have survived but also are parts of advanced logic families, such as HC (high-speed CMOS) and AC (advanced CMOS).

The circuit in **Figure 1**, a 10-line-to-one-line data selector/multiplexer, comprises two eight-to-one multiplexers, IC_1 and IC_2. The A, B, and C bits of the address input of IC_1 connect to corresponding address bits—A, B, C, and D—of the main address input. The eight data inputs, D0 to D7, of the circuit are identical to the equally denoted data inputs of IC_1.

Whenever the main address is a binary-coded eight or nine, when A, B, C, and D=eight, the data input, D4 of IC_2, is active. When A, B, C, and D=nine, D5 of IC_2 is active. This shift in addressing of IC_2's data inputs is due to the IC's modified addressing: Address bit C connects to the MSB (most-significant bit) D of the main address input. The A and B are common to IC_1 and IC_2, respectively. To unite their outputs without using any additional logic, you must connect the noninverting output, Y, of IC_1 to data inputs D0 through D3 of IC_2. The eight lowest values, zero through seven, of the address always activate a signal of D0 through D3 in

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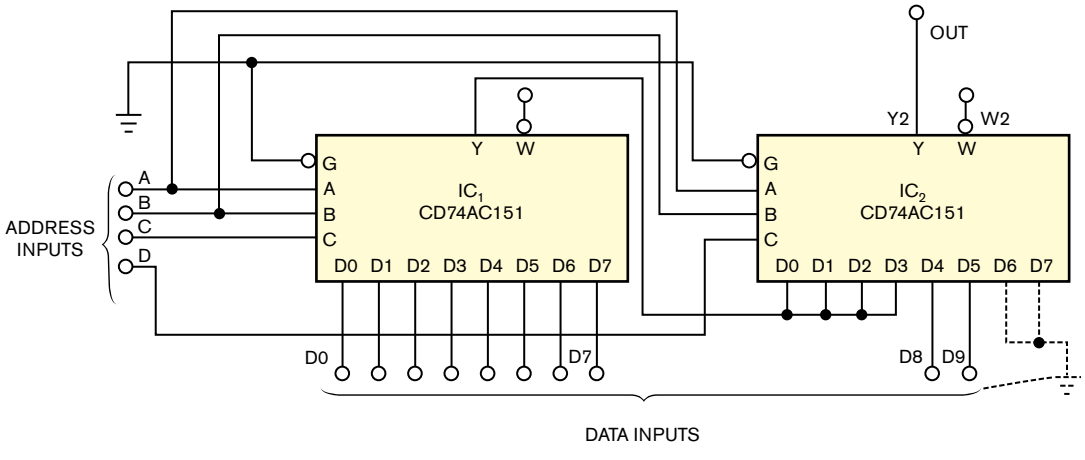

Figure 1 The maximum worst-case propagation delay of this 10-line-to-one-line data selector/multiplexer is 27 nsec, whereas the typical value is only 6.8 nsec. The circuit can also serve as a 12-to-one multiplexer.

IC_2. The output signal of IC_1 passes through one of these data inputs to the main output, Y2. If necessary, you can also use the W2 inverting output. Although the propagation delay from D0 through D7 to Y2 output is twice that from D8 and D9 to Y2, it is still less than 2×13.5 nsec=27 nsec for the CD74AC151 with a 5V supply. The typical delay is only 6.8 nsec.

Note that you can also use the circuit as a 12-line-to-one-line data selector/multiplexer by using the remaining data inputs, D6 and D7 of IC_2, which are idle in this circuit. In such a case, you attribute another notation of D10 to the D6 input of IC_2, and D11 holds for D7 one. Simultaneously, you must code the A, B, C, and D address in duodecimal code and, eventually, hexadecimal code, instead of BCD. EDN

Implement a simple digital-serial NRZ data-recovery algorithm in an FPGA

Jef Thoné and Bob Puers, ESAT-MICAS,
Katholieke Universiteit Leuven, Leuven, Belgium

Serial-data links embed clocks in their data streams, and those clocks must be recovered at the receiver end. This Design Idea describes a data/clock-recovery algorithm for an NRZ (nonreturn-to-zero), 1.5-Mbps data stream in a Xilinx (www.xilinx.com) Spartan XC3S200 FPGA. The algorithm employs a modified data-recovery application note (**Reference 1**). The application note uses the DCM (digital-clock manager) on the Xilinx Spartan and Virtex models, but this application uses a simplified algorithm that compares the data edges, if any, with internally generated clock edges, dynamically changing the data-input-to-data-output delay. The simplified algorithm allows integration in smaller CPLDs or FPGAs that lack a DCM (**Figure 1**).

The algorithm uses a 3-bit, free-running counter to generate the output clock, an 8-bit shift register to sample the serial data, seven XOR ports for edge detection, a 7-to-1 multiplexer with decoding for multiplexing the right-shift-register bit to the output, and some buffering registers. The algorithm runs at eight times the serial-data-stream speed, without a known phase relationship between both. It clocks the data into the shift register, which implies that, after eight clock cycles, the shift register will contain a rising edge; a falling edge; or, when the input data remains the same, no edge. The multiplexer does not take into account cases in which the shift register contains no edges or more than one edge.

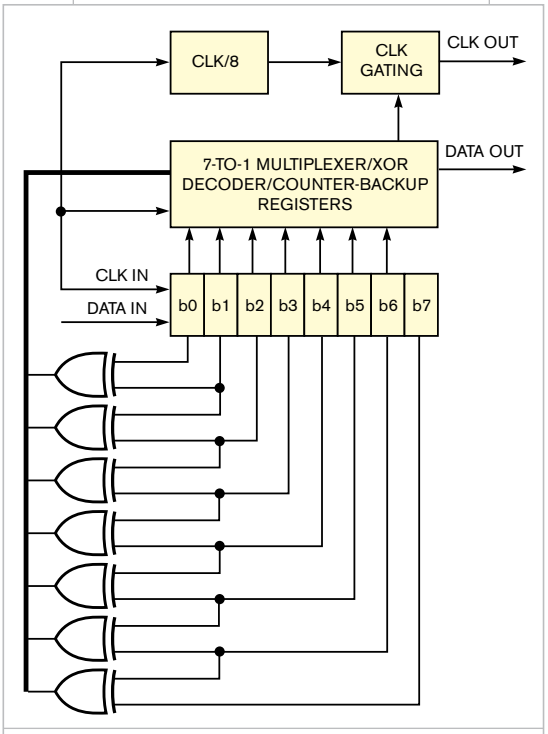

Figure 1 A clock-recovery circuit in an FPGA recovers data in a 1.5-Mbps data stream.

The edge location is checked in the shift register using the XOR-port array, which compares shift-register bit 0 with bit 1, bit 1 with bit 2, and so on. Depending on the output of the XOR array, showing where the edge occurs, a certain bit of the shift register multiplexes to the output. This action ensures that the output clock always toggles around the middle of the output-data bits.

When there are slight differences in clock speed and serial-input-data speed—for example, in the case of clock jitter or clock tolerances—the data-input phase continuously changes with regard to the output-clock phase as the algorithm tries to track the input-data phase. In this case, the multiplexer has an overflow, which happens when shift-register bit 7 multiplexes to the output, the next bit is

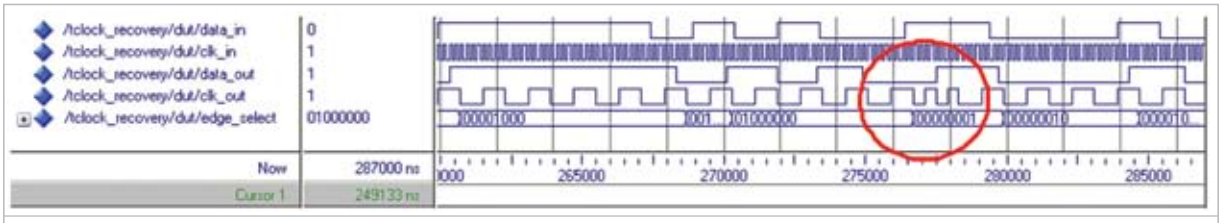

Figure 2 Doubling a clock output prevents a backward phase jump.

shift-register bit 1, or vice versa.

If bit 7 is output first—that is, the signal edge_select is 0100 0000—and the next selected bit is bit 1, with an edge_select of 0000 0001, a sudden phase jump in output data occurs. This phase jump is −360°×7/8, or −315°. Because the next input-data bit already had shifted in completely in the shift register, you need to employ a double-output clock once, so that the register doesn't miss a data bit (circled area in **Figure 2**).

When bit 1 is output, with an edge_select of 0000 0001, and the multiplexer jumps to bit 7, with an edge select of 0100 0000, a sudden phase jump in output data of 360°×7/8, or 315°, occurs. Because the shift-register data bit 7 is a delayed version of the last clocked bit, b1, the output clock must be stalled for one cycle. Otherwise, one bit too many will clock at the output (circled area in **Figure 3**). You can solve the overflow-phase jumps by gating the output clock using combinatorial logic. EDN

REFERENCE

1 Sawyer, Nick, "Data Recovery," Xilinx Application Note XAPP224, Version 2.5, July 11, 2005, www.xilinx.com/support/documentation/application_notes/xapp224.pdf.

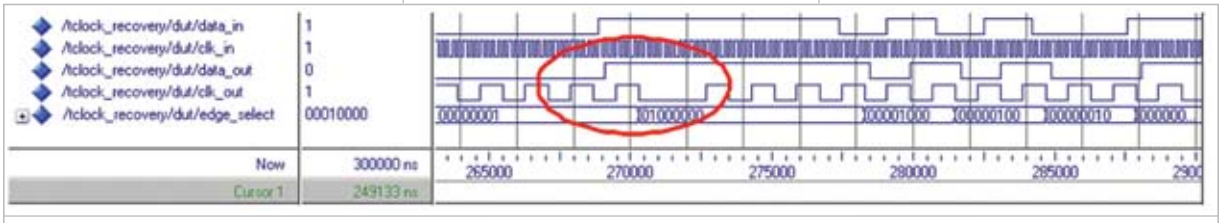

Figure 3 Stalling the output clock prevents a forward phase jump.

LED strobe has independent delay and duration

Michael C Page, Chelmsford, MA

The circuit in **Figure 1** is not complex, but it saved the day in an application involving visual inspection of the spray pattern of fuel injectors for quality and consistency. In this application, xenon strobe lights did not work because they take up too much space, and the light they emit is too intense. With a bank of six injectors with isolation panels, the reflection off a person's shirt or the wall behind him would interfere with the visual inspection. So the application instead used white HB LEDs (high-brightness light-emitting diodes) on "gooseneck"-type stands for adjustability in the chamber sections. Although the applica-

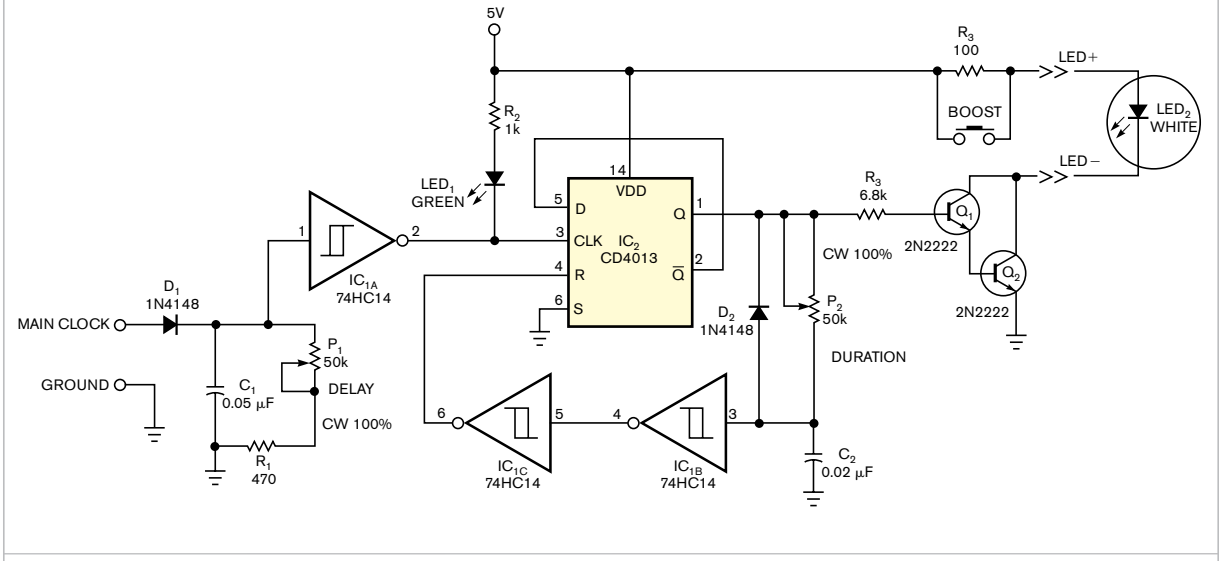

Figure 1 This circuit employs HB LEDs for a visual-inspection application.

tion could have used the trusty old 555 timer, the delay and duration duty-cycle controls interact, which is an awkward situation.

The circuit in **Figure 1** shows the main-clock input; the delay and duration potentiometers, P_1 and P_2; and the HB-LED output. The circuit also includes an onboard general-purpose LED for bench testing to indicate an input signal, although, when the circuit is operating at high speeds, this LED is useless. The main-clock input is a 5V pulse of approximately 30 µsec coming from the fuel-pump index. Delay potentiometer P_1 adjusts the on-time delay of the LED from about 40 µsec to 2 msec, and duration potentiometer P_2 adjusts the LED-on, or flash, time with a range of approximately 15 µsec to 15 msec.

The circuit applies a 5V pulse, the main clock, to diode D_1 and capacitor C_1 to form a peak-hold circuit. C_1 then discharges at a rate that P_1 sets. Schmitt trigger IC_{1A} monitors C_1's voltage, and, when it reaches the low threshold of IC_{1A}, it outputs a high level to IC_2's clock input, setting the Q output high. With IC_2's Q output high, the Darlington-transistor pair comprising Q_1 and Q_2 turns on, driving the output to the HB LED low at the output, lighting the LED. At this time, capacitor C_2 charges at a rate that P_2 sets. When this voltage reaches the upper threshold of IC_{1B}, IC_{1C}'s output switches to high, resetting flip-flop IC_2's output back to low and turning off the HB LED. The circuit is now ready for another round. Diode D_2 ensures a complete discharge of capacitor C_2 for repeatability when you reset the Q output of IC_2 to low. Because IC_2 requires an active-high signal, you can omit IC_{1B} and IC_{1C}, but you should use a Schmitt trigger following an RC circuit for repeatability, especially on slow capacitor-charge/discharge times.

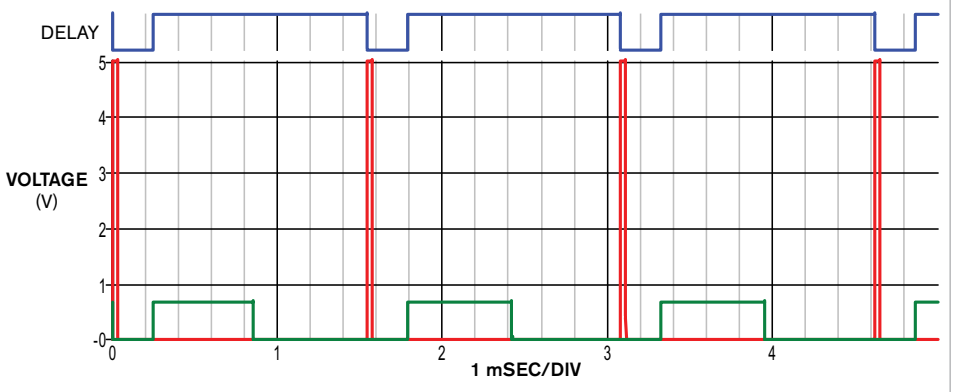

Figure 2 With a main-clock input of 650 Hz, the delay is approximately 250 µsec, with P_1 at 10%, and the duration is approximately 600 µsec, with P_2 at 75%. The top trace (blue) represents the strobe delay, the lower trace (green) represents Q_1's base duration, and the 5V trace (red) represents the main clock.

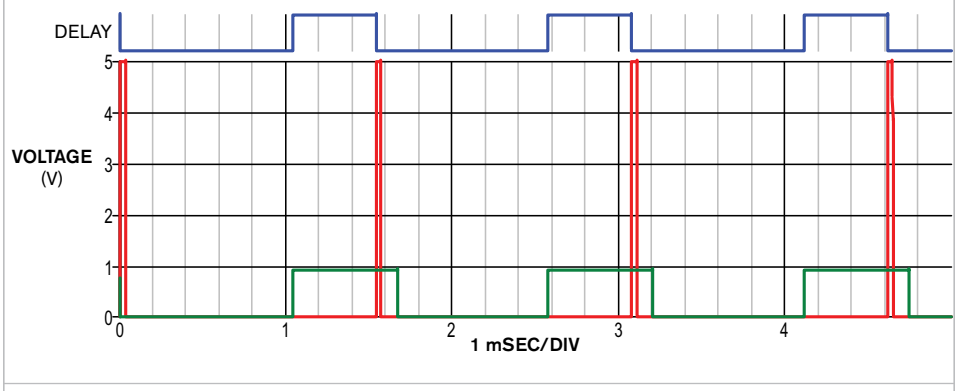

Figure 3 An adjustment change of delay occurs with the same duration as in Figure 2. The top trace (blue) represents the strobe delay, the lower trace (green) represents Q_1's base duration, and the 5V trace (red) represents the main clock.

Figure 2 shows the results of the circuit running with a main-clock input of 650 Hz and a delay of approximately 250 µsec, with P_1 at 10%, and a duration of approximately 600 µsec, with P_2 at 75%. **Figure 3** shows an adjusted change of delay with the same duration setting as in **Figure 2**. The new flash period overlaps the following fluid burst. You could, depending on the injector nozzle, see the end of one fuel burst of calibration fluid and the start of another in the chamber during the same flash period without encountering an error. The circuit also has a boost switch for a momentary intensity increase; otherwise, R_3 normally limits the current to approximately 40 mA. When you press the boost switch, the Darlington pair, two 2N2222 transistors with current of approximately 400 mA, still limits the current, but long-term use of the switch will shorten the LEDs' life. You should tailor the values of C_1, C_2, P_1, and P_2 to the application. Calculations will vary depending on the logic family you use, but, generally, $T=0.7\times R\times C$, where T is the time in seconds, R is the resistance, and C is the capacitance. EDN

Cancel sensor-wiring error with bias-current modulation

W Stephen Woodward, Chapel Hill, NC

The approximately −2-mV/°C temperature coefficient of diode junctions is a popular means of temperature measurement, especially in cryogenic applications (**Figure 1**). Diode temperature sensors are compact, stable, robust, sensitive, and inexpensive, and, unlike thermocouples, they require no reference junction. All of these benefits help explain the durable popularity of this—to use the polite term—"mature" technology.

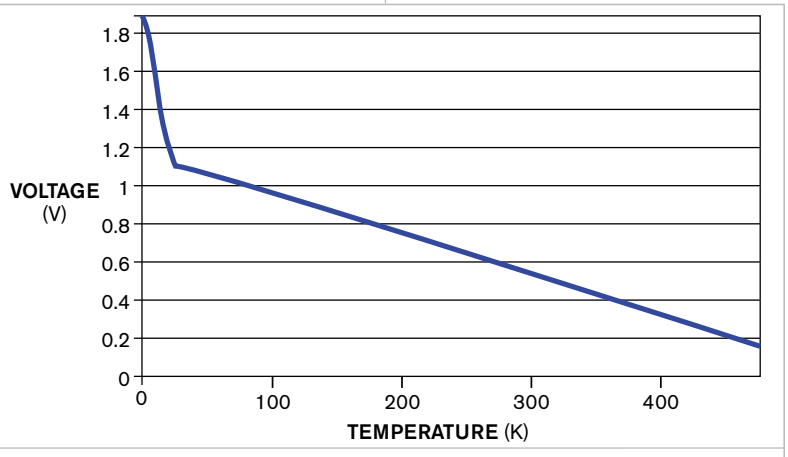

Figure 1 The typical −2-mV/°C-voltage-versus-temperature coefficient of diode sensors is large and nearly constant over a wide range of temperatures.

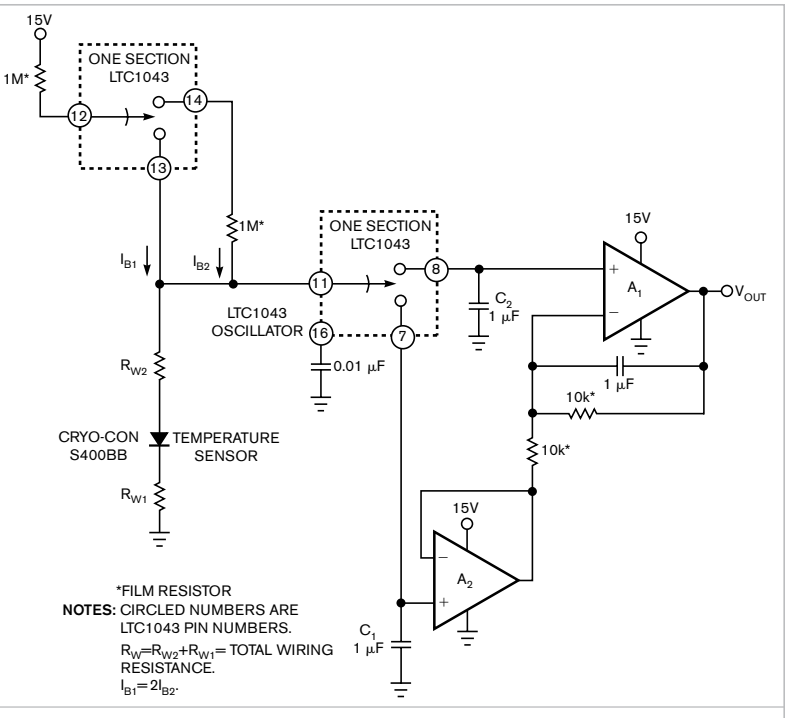

Figure 2 This circuit cancels the wiring-resistance error inherent in diode temperature sensors and requires only two conductors in the sensor cable.

A complicating factor and potential error source affecting these sensors arises from their need for bias-current excitation, however. The resulting contribution of ohmic IR (current/resistance)-voltage drop in the wiring and the connectors' resistance to the sensor's output voltage create spurious and temperature-sensitive voltage offsets. These offsets can introduce unacceptably large measurement error. This situation is especially likely when you use small and, therefore, high-resistance-gauge wire for sensor cabling, such as in cryogenic applications. In those cases, designers prefer exceptionally fine-gauge wire to minimize thermal conductivity and leakage.

The usual solution to the IR problem is to employ four-wire "Kelvin"-interconnection topologies, in which one pair of conductors carries the sensor's bias current and a separate, independent pair differentially senses the sensor's output voltage. This approach prevents corruption of the sensed voltage by IR drop in the bias pair. This traditional fix works well but complicates the wiring and doubles undesirable thermal leakage due to the extra wires, thus defeating much of the point of using fine-gauge cabling in the first place.

Figure 2 illustrates a circuit that implements a different approach. It cancels the wiring-resistance error and needs only two conductors in the sensor cable. It takes advantage of the fact that IR-voltage drop is directly proportional to current, but the sensor voltage is mostly constant. It works by alternating the magnitude of the excitation current, I_B, between two values, I_{B1} and I_{B2}, where $I_{B1}=2I_{B2}$. The ac component of the resulting signal is thus approximately I_BR_W, where R_W is the total wiring resistance plus a minor contribution from nonzero sensor impedance.

The clock for both I_{B1}/I_{B2} excitation modulation and synchronous demodulation of the resulting response is the internal oscillator of the LTC1043, which you set to approximately 500

Hz by connecting the external 0.01-µF capacitor to Pin 16. The resulting toggling of the excitation ballast resistance between 1M and 1M+1M=2M creates the 2-to-1 current modulation and an ac-signal component proportional to wiring resistance: I_BR_W.

The other side of the LTC1043 synchronously rectifies the I_BR_W ac component, storing the $I_{B1}R_W=V_{C1}$ phase on C_1 and the $I_{B2}R_W=V_{C2}$ phase on C_2. Op amp A_2 buffers V_{C1} and inputs it to the resistor network and A_1, which subtracts it from the average sensor signal, producing an output voltage independent of cabling-resistance offset. One downside of the technique is that, due to sensor-impedance effects on the order of 20 mV, the thermometric diode usually requires custom temperature calibration. EDN

Simple FSK modulator enables data transmission over low-speed link

Israel Schleicher, Prescott Valley, AZ

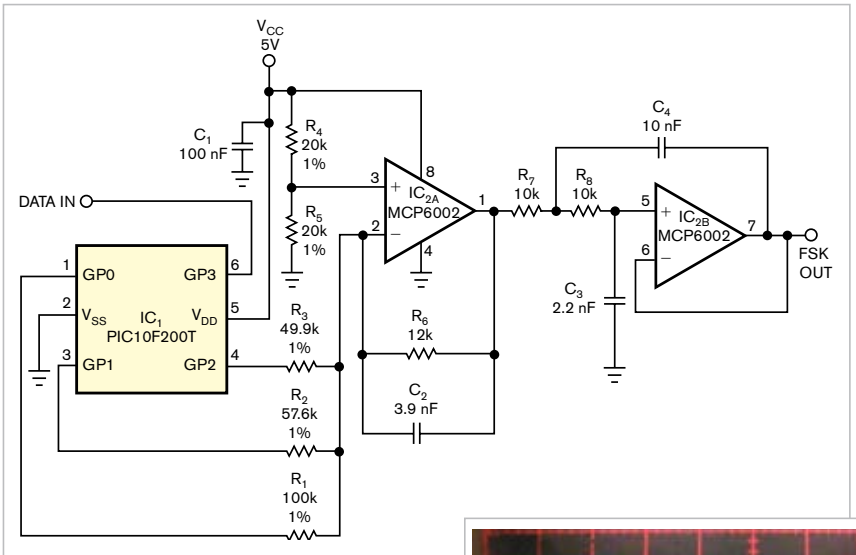

Figure 1 This microcontroller-based circuit generates Bell 202-compatible FSK modulation.

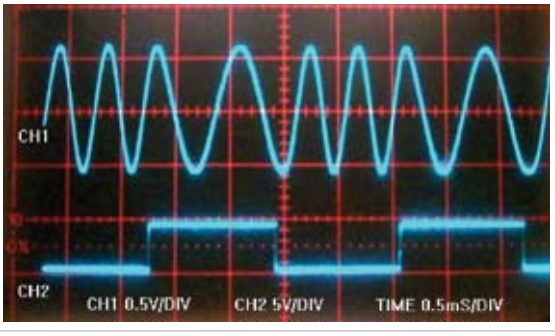

Figure 2 The FSK modulator's output changes frequency based on a digital input.

FSK (frequency-shift keying) is a type of signal modulation for transmitting digital data over an analog communication link. An FSK modulator comprises a digitally controlled sine-wave generator whose frequency shifts between two predetermined frequencies in response to the two logic levels of the digital data. The circuit in **Figure 1** generates a sine wave by continuously sampling a single sine cycle. The output of IC_{2A} is proportional to the currents through R_1, R_2, and R_3. These resistors connect together at one end to the inverting input of IC_{2A}, which is biased at $V_{CC}/2$. The outputs GP0, GP1, and GP2 of microcontroller IC_1 produce nonoverlapping pulse trains. When you set either output high or low, the others are off—that is, at high impedance. When you set an output high, the voltage across the resistor that connects to it is $V_{CC}/2$. When you set the output low, the voltage across the resistor is $-V_{CC}/2$.

Select the values of R_1, R_2, and R_3 so that the current pulses have magnitudes proportional to samples of sin 30, 60, and 90°, respectively. Setting all the outputs of IC_1 to off produces the sample of sin(0°), and no current flows through the resistors. Thus, starting with all outputs of IC_1 at off and consecutively and periodically setting GP0, GP1, and GP2 to high and then, in reverse order, setting GP1 and GP0 high again generates the positive half of a sine wave. Repeating the process but setting the outputs to low generates the negative half of the waveform.

This scheme produces a sampled sine waveform with 12 samples per cycle. In addition to the desired frequency component, f_0, this waveform contains higher-frequency components at $(12k+1)f_0$ and $(12k-1)f_0$, k=1,2,3, and so forth. The lowpass filter comprising IC_{2B}, R_7, R_8, C_3, and C_4 easily filters out these undesired components of smaller amplitude. **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com/090611dia, is the assembly-program code that implements the Bell 202 FSK standard. When the control input Data In is high, the output frequency is 1200 Hz; when the control is low, the output frequency is 2200 Hz. The transition from one frequency to the other occurs in a manner that retains phase continuity. **Figure 2** shows the FSK-modulator output (CH1) in response to a modulating signal (CH2). EDN

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Create a swept-sine function in LabView with just one virtual instrument

Sean McPeak, University of California—San Diego

Swept sine waves are useful when you want to test a product over a wide frequency range. A large research project included the requirement to determine wave propagation in the open ocean. This application required the generation of a swept sine wave to drive an acoustic transducer. Although many waveform generators have a built-in function for this requirement, you must program it yourself if you want to implement a swept sine with a multifunction data-acquisition card. You can create a swept-sine function in National Instruments' (www.ni.com) LabView with just one VI (virtual instrument). Using this function, you can control start and stop frequencies, sample rate, and the overall duration of the sweep (**Figure 1**).

The LabView software calculates an array of numbers that represent the swept-sine-wave time series at each sample point as the frequency either increases or decreases, depending on the direction of the sweep. You must handle the frequency change of the output on a point-by-point basis. The basic form of the **equation** is $Y(I)=V\times\sin((A\times I^2)/2+B\times I)$, where Y(I) is the amplitude of the swept sine wave as a function of the sample point, I is the integer that steps through the time series, V is the peak voltage, and A and B are variables. You define A as $2\times\pi(f_{STOP}-f_{START})/N$, and you define B as $2\times\pi f_{START}$, where N is the number of samples, f_{START} is the normalized start frequency, and f_{STOP} is the normalized stop frequency. To normalize the start and stop frequencies, you must change the unit to cycles per sample. You accomplish this task by dividing the f_1 and f_2 frequencies in hertz by the sample rate. You determine the sample rate by deciding how smooth of a transition you want to represent your swept sine wave. A good rule of thumb is to have at least 10 samples/cycle at the high-

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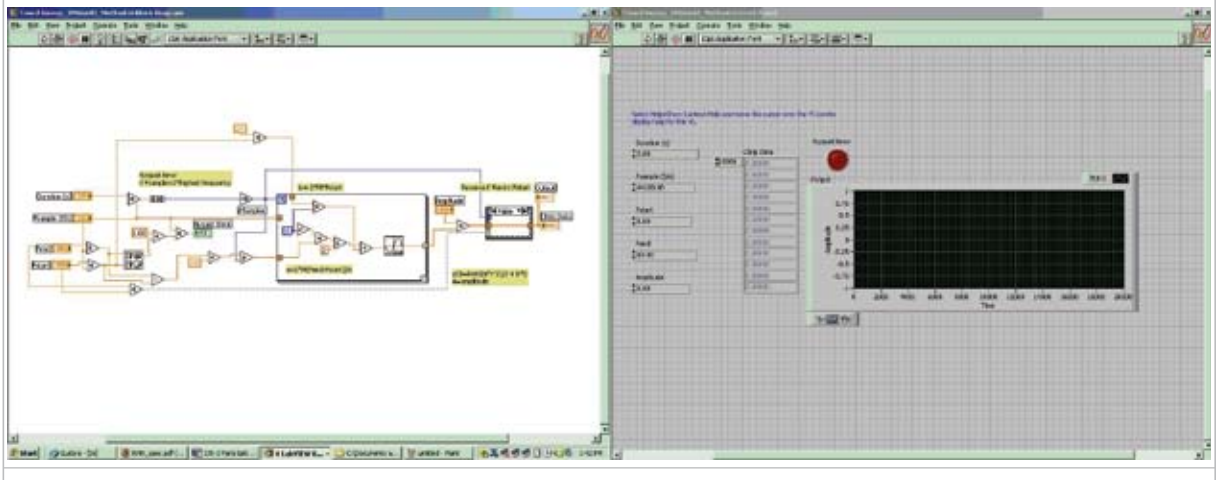

Figure 1 With just one LabView virtual instrument, you can control start and stop frequencies, sample rate, and the overall duration of the sweep.

est frequency. When setting the sample rate, you need to take into account the overall frequency span you are sweeping and the duration of the sweep itself. It is also helpful to compare the results and performance of the LabView data-acquisition-system implementation of the swept sine wave with those of an AWG (arbitrary-waveform generator).

You use two methods of comparison. First, you compare the output of both the data-acquisition and the AWG swept sine wave on a spectrum analyzer. Second, you run them both through an audio-amplifier/speaker system and simply listen to the output. This method is useful in determining sweep rate, duration, and stop and start frequencies. This type of comparison is valid only if the frequencies involved are in the audible range. The LabView VI employs simple array manipulation and uses a "for" loop. The input duration is in seconds, the sample frequency is in samples per second, and the starting and ending frequencies are in hertz. Dividing the sample rate immediately converts the start and end frequencies to cycles per sample. A maximum/minimum block takes the normalized ending and starting frequencies as its inputs and uses the maximum output of the input pair. You use this method to determine whether your design meets the Nyquist criteria, given the sample rate and highest frequency you require.

This approach drives a simple Boolean variable to alert the user about whether the design meets the Nyquist criteria. You set the "for" loop to run for the total number of samples you want to calculate. You determine this value by multiplying the duration in seconds by the sample rate in samples per second. To guarantee that the loop processes all of the generated samples, you must add one, because the loop stops at N−1.

You implement the output function in the "for" loop with simple algebraic operators and the sine block. The output is an array that reaches the perimeter of the "for" loop. It is important to enable indexing at this node. This action allows the circuit to individually handle each element in the array at the output of the "for" loop. You can also add a simple gain stage to set the peak-to-peak value to whatever point you want. Finally, you use the "rotate-1D-array-block" case structure to flip the array if the ending frequency is lower than the starting frequency. This approach handles cases in which you want a frequency sweep that starts out in a higher frequency and descends to a lower frequency.

You can easily modify and expand this simple program. One idea would be to use the output array, which is nothing more than the time series representing a predescribed frequency sweep, to feed a loop that would drive a data-acquisition module. The output of the module should accurately represent the frequency sweep, as long as the module's output sample rate is the same as the sample rate you use for generating the frequency-sweep time series. You should then be able to track the output samples and, when they are complete, reverse the frequency-sweep array. You then again feed this new flipped array to the data-acquisition module. Depending on the maximum and minimum frequencies, sweep duration, and sample rate you use, it may be difficult to flip the array and configure the module quickly enough to not miss a sample. In that case, you can prefill a frequency-sweep array for a set number of passes.

These modifications allow the sweep to continue back and forth for a set period. Another improvement would be to add some real-time FFT (fast-Fourier-transform) capability so that the user can see the sweep in the frequency domain. This approach also adds an increased level of insurance that the circuit properly meets the sweep definition. EDN

Charlieplexing at high duty cycle

Luke Sangalli, Digital Designs, Melbourne, Australia

A few articles have recently appeared describing novel ways to increase the number of LEDs a microprocessor can drive with a limited number of pins (**Reference 1**). The standard multiplexing technique made popular by multidigit seven-segment displays has, in pin-scarce designs, given way to "Charlieplexing."

Charlie Allen devised this technique while working at Maxim (www.maxim-ic.com), which has since introduced ICs using the technique (**Reference 2**). Allen used the high-impedance third input state available to most microprocessors for turning off LEDs in a matrix; the LEDs' respective microprocessor pins' high or low states individually turn on these LEDs. Using this method, you can drive nine seven-segment LED displays using only nine microprocessor pins rather than the usual 17. For N pins, you can individually address N×(N−1) LEDs using Charlieplexing.

One of the gripes people often level at Charlieplexing regards its poor duty cycle. A previous Design Idea com-

TABLE 1 NO. OF LEDs AND DUTY CYCLES

No. of pins	No. of LEDs	Charlieplexing duty cycle (%)	Standard multiplexing duty cycle (%)/no. of pins
Three	Six	33.3	50/five
Four	12	25	33/seven
Five	20	20	25/nine
Six	30	16.6	20/11
Seven	42	14.2	16.6/13
Eight	56	12.5	14.2/15
Nine	72	11.1	12.5/17
10	90	10	11.1/19

pares the standard multiplexing method with Charlieplexing (**Reference 3**). Using Charlieplexing, the maximum duty cycle for a 20-LED display is only 5%. The poor duty-cycle figure is due not to the method, however, but rather to the driving capability of the microprocessor and the parasitic-leakage paths. A single pin cannot usually sink the current a number of LEDs require to effectively light up, so these designs often require one source pin and one sink pin to light only one LED at any time. However, adding a transistor or two resistors allows you to circumvent these issues.

If you rearrange the LEDs in the familiar cross-point array and add a transistor to each column to carry the common current, you'll see the duty cycle of the Charlieplexing method does not differ much from standard multiplexing (**Figure 1**). For a 20-LED, five-column matrix, each LED remains on for 20% of the time compared with 25% for standard multiplexing, but now using only five pins instead of nine (**Table 1**).

BY THE TIME YOU GET TO 90 LEDs, THE PCB REAL ESTATE AND COST OF THE 10 TRANSISTOR/ RESISTOR SETS PALE IN COMPARISON TO THE DISPLAY ITSELF.

One of the drawbacks of adding the transistor and resistors to each column is that you need additional components to achieve a reasonable LED brightness when a large number of LEDs is involved. This approach, however, is a better alternative to using a costly IC and no worse than standard multiplexing or "Gugaplexing," which also requires additional transistors and resistors. From a cost and benefits point of view, consider that, by the time you get to 90 LEDs, the PCB (printed-circuit-board) real estate and cost of the additional 10 transistor/resistor sets pale in comparison to the display itself.

Examining the circuit in detail, you'll notice that it has five microprocessor pins, P_1 through P_5, available, for a total of $N\times(N-1)=20$ LEDs. When P_3, for example, is high, the emitter of Q_3 is at approximately 4.4V, and you can turn off D_{13}, D_{23}, D_{43}, or D_{53} if you make P_1, P_2, P_3, or P_5 low. Any pin that you set to input, or high impedance, alternatively turns off the corresponding LED. When P_1 and P_4 are low, P_3 is high, and P_2 and P_5 are in high-impedance states. With P_3 high, transistor Q_3 biases on, all the other transistor bases are either low, which ensures that no current will flow, or high-impedance, which supplies no current into the base to allow the transistor to conduct. All the diodes in the third column can turn on, but only D_{13} and D_{43} have a path directly to ground through P_1 and P_4, which are low and through the 100Ω current-limiting resistors.

D_{23} and D_{53} connect to the high-impedance input pins and can conduct only through the 100Ω resistors attempting to turn on Q_2 and Q_5. Because of their forward-voltage drop—typically, 2.2V—the emitters of Q_2 and Q_5 will be less than 1.6V, as the following **equation** shows: $5V_{CC}-0.6V\ (Q_3)-2.2V\ (D_{23}\text{ or }D_{53})-0.6V\ (Q_3\text{ or }Q_5)-I_{LED}\times100\Omega<1.6V$, where I_{LED} is the current of the LEDs. This scenario does not allow any LED in Column 2 or Column 5 to light up to any level that would have an undesirable effect. EDN

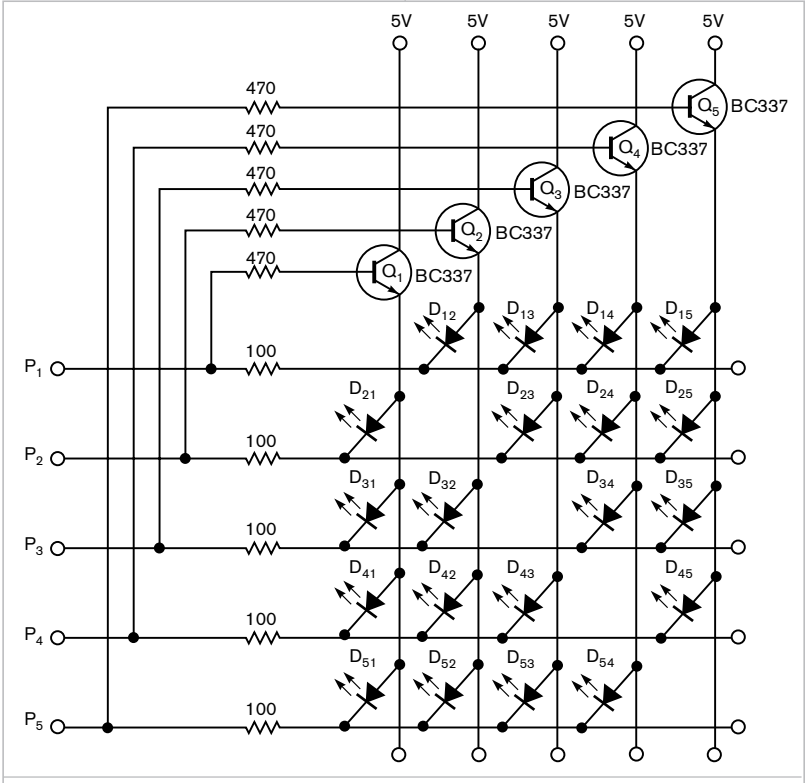

Figure 1 Arranging LEDs in a cross-point array and adding a transistor to each column show that the duty cycle of Charlieplexing is similar to that of standard multiplexing.

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2 "Charlieplexing–Reduced Pin-Count LED Display Multiplexing," Application Note 1880, Maxim, Feb 10, 2003, http://pdfserv.maxim-ic.com/en/an/AN1880.pdf.

3 Gupta, Saurabh, and Dhananjay V Gadre, "Multiplexing technique yields a reduced-pin-count LED display," *EDN*, Oct 16, 2008, pg 68, www.edn.com/article/CA6602447.

Serial port tests digital circuits

Yury Magda, Cherkassy, Ukraine

A PC's serial port provides signal lines that you can use to read voltage levels of digital circuits. You can use the port to test digital TTL (transistor-to-transistor-logic)-level circuits. You just need to convert the TTL levels to RS-232 voltages, and you can add a multiplexer to increase the number of signals that the serial port can sense.

The circuit in **Figure 1** uses a MAX232 IC from Maxim (www.maxim-ic.com) to convert RS-232 voltage levels to TTL levels (**Reference 1**). A 74HC4051 from Texas Instruments (www.ti.com) lets you select any of four digital inputs and route them to the serial port (**Reference 2**). **Listing 1**, which is available with the online version of this Design Idea at www.edn.com/090625dia, lets you control the RTS (ready-to-send) and DTR (data-terminal-ready) pins in the serial port that selects the signal under test. The CTS (clear-to-send) pin then reads the signal under test into the PC.

The four digital-input signals, A0 through A3, from your device under test connect to the first four inputs, X0 through X3, of the multiplexer. Only one of those signals can pass through to the X output, Pin 3, at a time. By setting the appropriate binary code on the serial port's RTS and DTR lines, you can select the signal to pass through the multiplexer (**Table 1**).

The PC software, running on Windows XP, sequentially sets those binary combinations on the port's RTS and DTR lines and reads the digital signal on the CTS line. The software then reads the status of the selected bit and displays it when you press the "check-status" button (**Figure 2**). The code is written in Microsoft C# 2008, but it will run on the 2005 version, as well.

To create the application, select the "Windows Form Application" from the templates in the project wizard. Place the text-box, label, and button components on the project's main form and assign titles for them. You should place the serial-port component on the design area of the project. Then, set the appropriate parameters for the serial-port component, including the port number, baud rate, data bits, parity, and stop bits.

When you build the circuit, follow all precautions concerning the MAX232 and 74HC4051 wiring according to the manufacturers' data sheets. Place bypass capacitors as close as possible to the IC's power and ground. You can replace the MAX232 with a MAX225 or MAX233. EDN

TABLE 1 INPUT SELECTION

Signal to X pin	RTS bit	DTR bit
A0	0	0
A1	1	0
A2	0	1
A3	1	1

REFERENCES

1 "MAX220-MAX249 +5V-Powered, Multichannel RS-232 Drivers/Receivers," Maxim, January 2006, http://datasheets.maxim-ic.com/en/ds/MAX220-MAX249.pdf.

2 "CD54/74HC4051, CD54/74HCT4051, CD54/74HC4052, CD74HCT4052, CD54/74HC4053, CD74HCT4053 High-Speed CMOS Logic Analog Multiplexers/Demultiplexers," Texas Instruments, 2004, http://focus.ti.com/lit/ds/symlink/cd74hct4053.pdf.

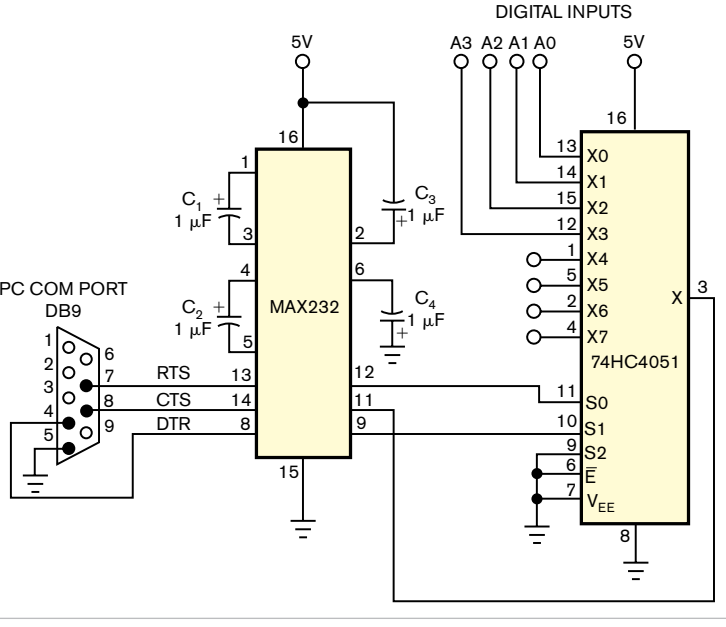

Figure 1 This circuit lets you pass up to four TTL-level signals to an RS-232 port to read their status.

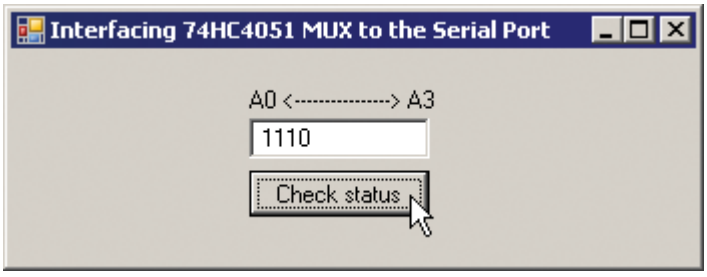

Figure 2 A main window of the running application shows that input lines A0–A2 have high logic levels and A3 has a low logic level.

DAC calibrates 4- to 20-mA output current

Ronald Moradkhan and Steven Lau,
Maxim Integrated Products, Sunnyvale, CA

Industrial controls make heavy use of 4- to 20-mA current loops to transmit process measurements because current loops retain information in the presence of noise and changes in loop voltage. The loop circuit requires proper calibration to ensure accurate readings. The circuit in **Figure 1** calibrates the loop by generating a current in response to a control voltage:

$$I_{OUT} = \frac{V_{CONTROL}}{R_{SENSE} \times K_{CSA}},$$

where I_{OUT} is the output current, $V_{CONTROL}$ is the control voltage, R_{SENSE} is the sense resistance, and K_{CSA} is the gain of the current-sense amplifier—20 in this case. The circuit comprises IC_2, a Maxim (www.maxim-ic.com) MAX5304 DAC; IC_3, a MAX4376T current-sense amplifier; IC_4, a MAX420 op amp; and Q_1, an N-channel IRFL4105 MOSFET. The op amp lets the control voltage set the output current because it forces the voltage on the negative input equal to that on its positive input. The output current depends on the value of the sense resistor, the gain of the current-sense amplifier, and the control voltage.

The DAC provides the control voltage that lets you automate the calibration procedure. By selecting the right value for the sense resistor and by using a suitable resistor divider for R_1 and R_2 at the output of the DAC, you can adjust the circuit's output to 4 mA when the DAC's digital input is zero-scale and 20 mA when the digital input is full-scale. **Figure 1** shows the component values you need to achieve that condition.

With a zero-scale digital input, the DAC output is 0V and the resistor divider produces 0.6V at the op amp's positive input, forcing the output current to 4 mA. With a full-scale digital input, both the DAC output and the midpoint of the resistor divider are at the 3V reference voltage, forcing the output current to 20 mA. A transfer curve relates the output current to the control voltage (**Figure 2**).EDN

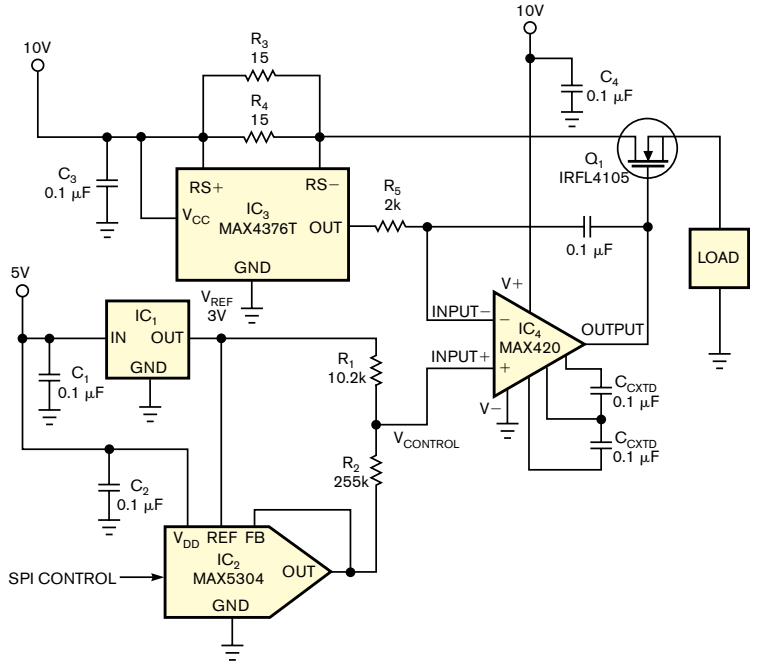

Figure 1 This DAC-controlled 4- to 20-mA transmitter allows digital control of the loop current.

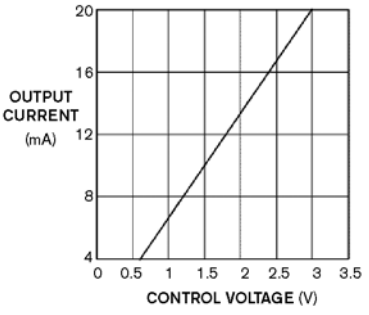

Figure 2 The circuit in Figure 1 produces a linear output current versus digital control voltage.

Alarm tells you to close the refrigerator door

Boris Khaykin, TRW Automotive, Livonia, MI

The circuit in **Figure 1** is a simpler and safer device than a similar one I recently read about (**Reference 1**). A few years ago, I built the circuit that this Design Idea describes, and the gadget still operates with the original 9V battery. The circuit operates by sensing a decrease in resistance of photocell PC_1 that results from light in the refrigerator when its door is open. A counter is in a reset state when PC_1 is in the dark, and its resis-

tance is greater than 30 kΩ. Usually, the dark resistance is greater than 200 kΩ, and current consumption at this state is less than 40 μA. Oscillator-counter IC_1 starts counting when PC_1's resistance is lower than 15 kΩ—that is, when the light bulb in the refrigerator is on. Then, in 20 seconds, it turns on a buzzer for 20 seconds or until someone closes the door. The current at this state is approximately 2.5 mA.

You can use almost any photocell, such as the Jameco (www.jameco.com) 202403 CDS0018001 with 200-kΩ dark and 3-kΩ light resistance. This circuit uses a RadioShack (www.radioshack.com) 273-074 buzzer. You can use any similar piezoelectric buzzer with an operating dc voltage of 1.5 to 15V. V_1 can be as low as 3V. The trade-off is that using a voltage this low gives you longer battery life but lower volume of sound. EDN

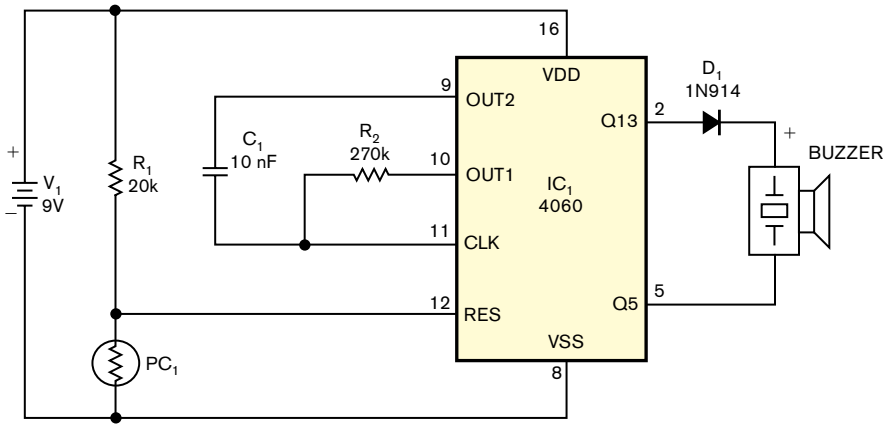

Figure 1 This gadget, placed inside a refrigerator, sounds an alarm when the refrigerator door is open for more than 20 seconds.

REFERENCE

1 Babu, TA, "Alarm Sounds When Refrigerator Door Remains Open Too Long," *Electronic Design*, March 26, 2009, pg 46, http://electronicdesign.com/Articles/ArticleID/20806/20806.html.

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READERS SOLVE DESIGN PROBLEMS

Illumination ring provides focused intensities

William Grill, Honeywell Aerospace, Olathe, KS

If you use a camera-based inspection or soldering fixture, you need to see images in a small area. Often, side lighting produces shadows on an image that result in contrasting colors and poor quality. Thus, your monitor views may be difficult to clearly see or interpret. Centering a light ring on the image provides illumination on all sides of the object and may illuminate everything you need to see. In a camera application for controlling a light ring, this implementation not only controls the light, but also enables you to direct the light intensity by maintaining two levels of control. It also lets you maintain and rotate the second-tier levels about the illuminated object.

Based on a seven-LED set, you select three consecutive LEDs; the second-tier settings will define the three LEDs' intensities (**Figure 1**). The remaining displays are maintained at a base-tier-intensity setting. Using four pushbutton switches, the Microchip (www.microchip.com) 16F505 rotates, distributes, and provides PWM (pulse-width-modulation) control of these two power tiers across the seven LEDs. Two of the buttons increase or decrease intensity, or they group or ungroup the tier-intensity settings; the other two buttons rotate the resulting second-tier display clockwise or counterclockwise.

The implementation uses just a few parts, exploiting the controller to provide light level, state maintenance, and PWM control. The application debounces the buttons and indexes the intensity controls. An eighth LED indicates tier-grouped or -ungrouped

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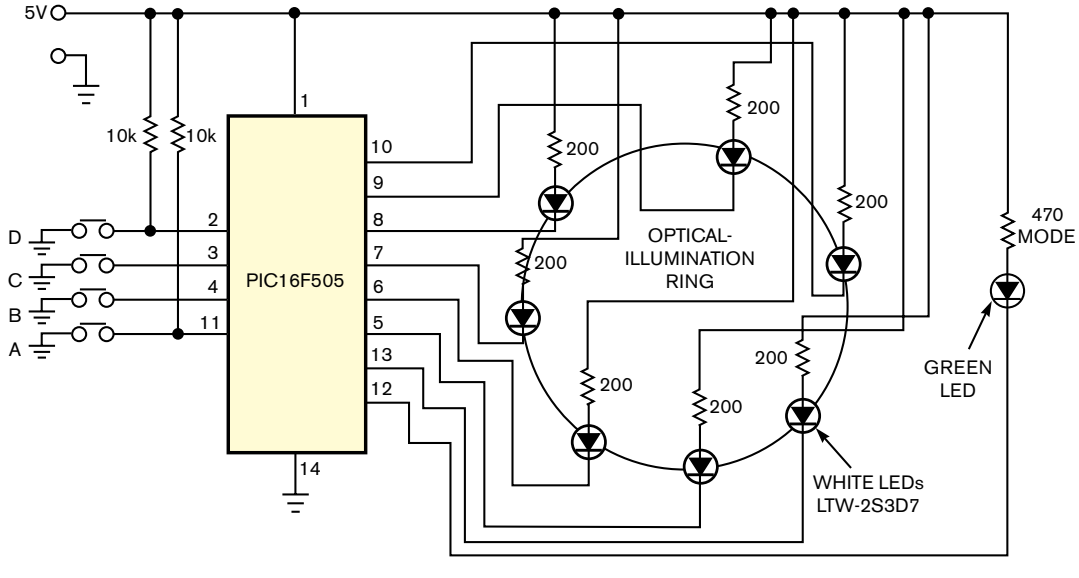

Figure 1 An LED illumination ring provides directed light intensity.

mode. When you group the tiers together, their intensity-setting indexing is common, but their register limits remain independent. You can download **Listing 1**, the assembly code for the circuit, from the online version of this Design Idea at www.edn.com/090709dia.

The controller provides a PWM period of approximately 7.5 msec to all the LEDs. It also controls each LED's duty cycle, according to the registered levels the button sets, in defined and maintained register masks and intensity values. The controller provides six bits of intensity, corresponding to 64 levels of resolution, although 8-bit resolution is available. The operating voltage is 5V. You can reconfigure the controller, the display, and their limiting resistors to operate at voltages as low as approximately 3.1V. High-millicandle, white, 5-mm, T1¾ through-hole LEDs provide the light source. The controller provides about 8 mA of current to each of the LEDs. By constraining the total power, surface-mount or other LED configurations are possible.

You can lay out the four momentary-action pushbutton switches for operation by the left or the right hand. With one representing the pushbuttons' asserted position, the controller's coded sequences provide the button-control functions found in **Table 1**.EDN

TABLE 1 PUSHBUTTON-CONTROL FUNCTIONS

A	B		C	D	
1	1	No function	1	1	Alternate between common-tier mode and second-tier mode
1	0	Select second-tier mode, rotate Tier 2 LEDs counterclockwise	1	0	Increment all or second tier if in second-tier mode with autoindexing
0	1	Select second-tier mode, rotate Tier 2 LEDs clockwise	0	1	Decrement all or second tier if in second-tier mode with autoindexing
0	0	No function	0	0	No function

Digital variable resistor compensates voltage regulator

Jason Andrews, Maxim Integrated Products Inc, Dallas, TX

A variable resistor that integrates a programmable, temperature-indexed look-up table can compensate for the temperature drift of a voltage regulator. In this case, the look-up table can change the resistance every 2°C over a range of −40 to +102°C, thereby nulling any regulator-output changes that would otherwise occur because of temperature. A typical regulator circuit comprises a regulating element, a feedback-resistor divider, and capacitors to provide filtering and regulation against transients and load-switching conditions (**Figure 1**). The ratio of the two feedback-divider resistors sets the regulator-output voltage. The regulator can generate either a preset 3.3V or any user-defined output within its operating range.

For most regulator circuits, the output voltage varies slightly with temperature, from 97.6 to 101.5% of nominal in this circuit. These numbers are respectable, but you can improve them. First, incorporate a digitally controlled variable resistor, such as a DS1859, into the regulator circuit of **Figure 1** by placing it in parallel with R_2 (**Figure 2**). A temperature-indexed look-up table in an internal nonvolatile memory controls the 50-kΩ digital resistor, allowing you to program a different resistance value for each 2°C window.

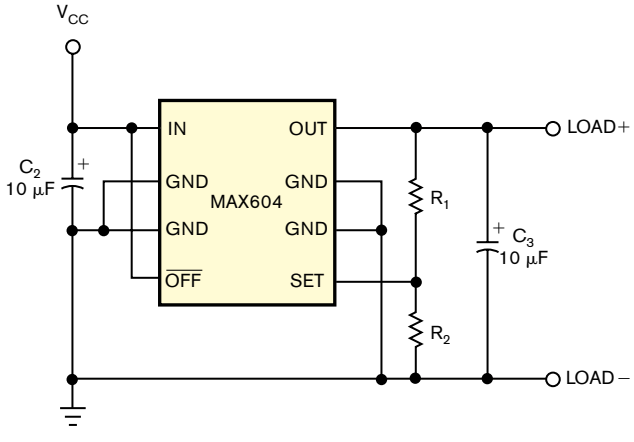

Figure 1 A typical voltage regulator lets you set the regulated output level by adjusting the R_1/R_2 divider.

You can program the look-up table to provide any resistance-versus-temperature profile. In this example, the look-up table flattens the regulator's normal curve over temperature. These look-up tables, therefore, provide a positive resistance slope with respect to temperature. The resistor has 256 programmable resistance settings of 0 to 255 decimal, and each one accounts

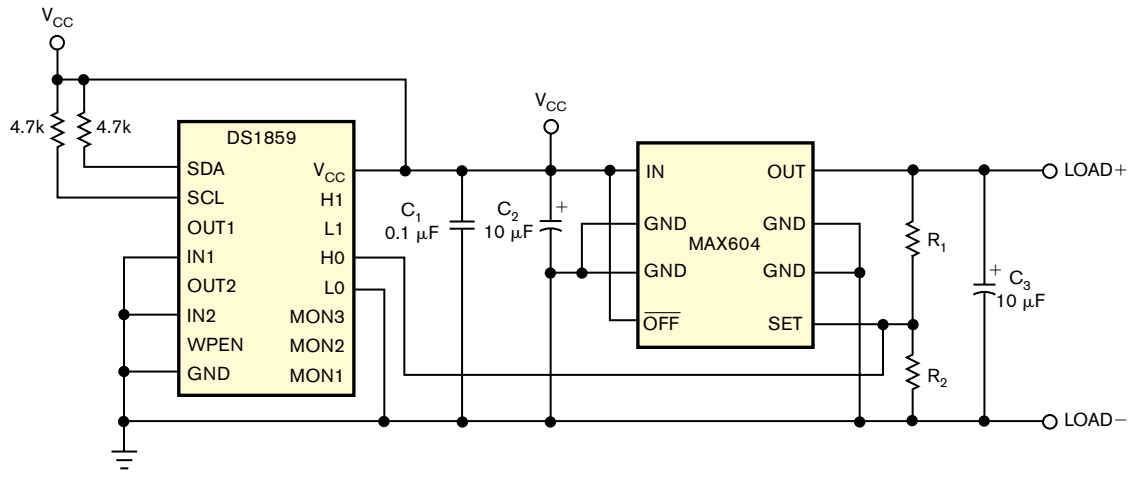

Figure 2 Connecting one-half of a dual variable resistor in parallel with R_2 to the circuit in Figure 1 lets you temperature-compensate the regulated output voltage.

for approximately 192Ω. In this example, the look-up table was programmed with a setting of 143 decimal at −40°C. The settings were incremented by one for every 4 to 6°C change in temperature, resulting in a value of 152 decimal for ambient and 158 decimal for +85°C.

As illustrated in **Figure 3**, the result of this regulated performance over temperature is a drastic increase in precision: The variation from −45 to +85°C is now only ±2 mV. For comparison, note the response of the standard regulator circuit in **Figure 1** (the black curve). The digital-resistor IC of **Figure 2** includes three ADC inputs for monitoring external voltages. An alternative, the DS1847 dual variable resistor, offers similar performance without the ADC monitors and at lower cost. EDN

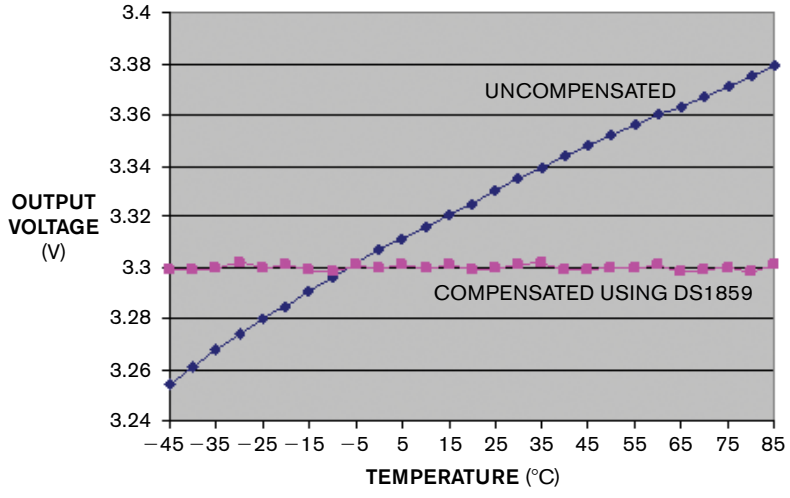

Figure 3 These curves compare regulated outputs versus temperature for the Figure 1 circuit (black) and the compensated Figure 2 circuit (pink).

Hot-swap switch provides easy thermal protection

Donald Schelle, National Semiconductor Corp, Santa Clara, CA

It is often difficult to design an effective thermal-management scheme that minimizes the risk of meltdown or fire. System orientation, placement, or both complicate matters by generating hot spots at varying locations on a PCB (printed-circuit board). A hot-swap switch and carefully placed temperature sensors mitigate thermal issues by disconnecting system power when a temperature exceeds a safe limit. The circuit in **Figure 1** uses a hot-swap switch to monitor overvoltage, undervoltage, and overcurrent conditions. When the ambient temperature exceeds a preset threshold, a carefully placed temperature sensor, IC_1, forces the hot-swap controller, IC_2, to disconnect system power. You can use multiple tempera-

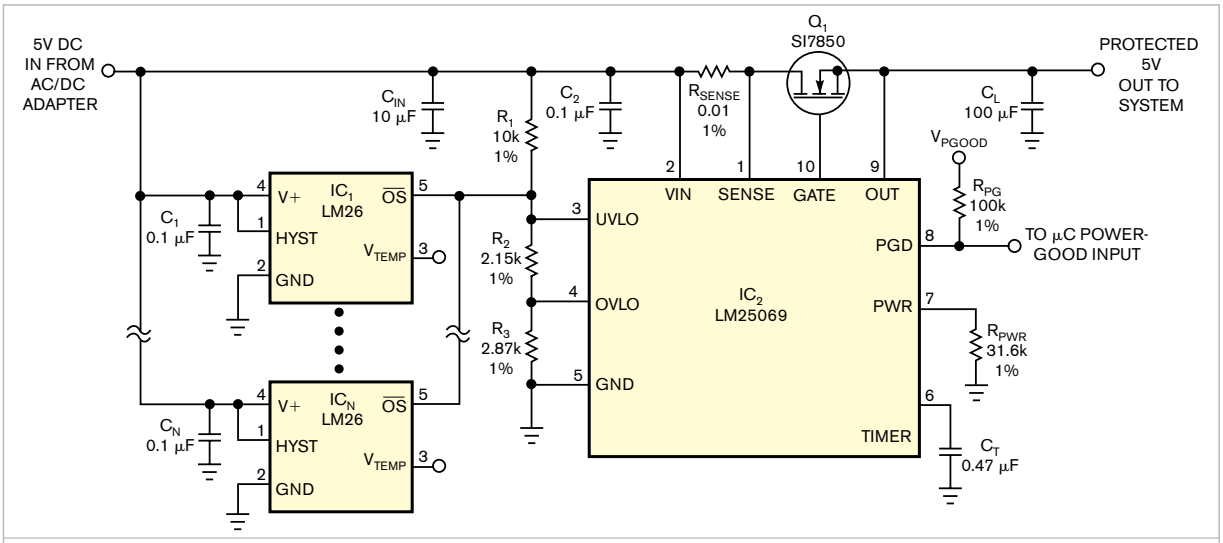

Figure 1 Carefully placed low-cost temperature sensors disconnect system power when an overtemperature thermal event occurs.

ture switches to isolate hot spots when you mount the system in varying orientations. The circuit requires neither a microcontroller nor a costly temperature-monitoring IC. Thermal events cut power to the system using a robust, nondestructive technique.

In a typical overtemperature condition (**Figure 2**), a thermal event (upper trace) causes the LM26 to trip, forcing the LM25069 to disconnect power from the system (middle and lower traces). When the system temperature decreases below the LM26's trip point, system power returns. Incorrect placement or orientation can cause overtemperature events, forcing the system to turn on and off like clockwork; support personnel can easily diagnose this symptom. Inexpensive temperature sensors and an innovative power-limiting hot-swap controller reduce the cost of this circuit to approximately $2 in low-volume applications. EDN

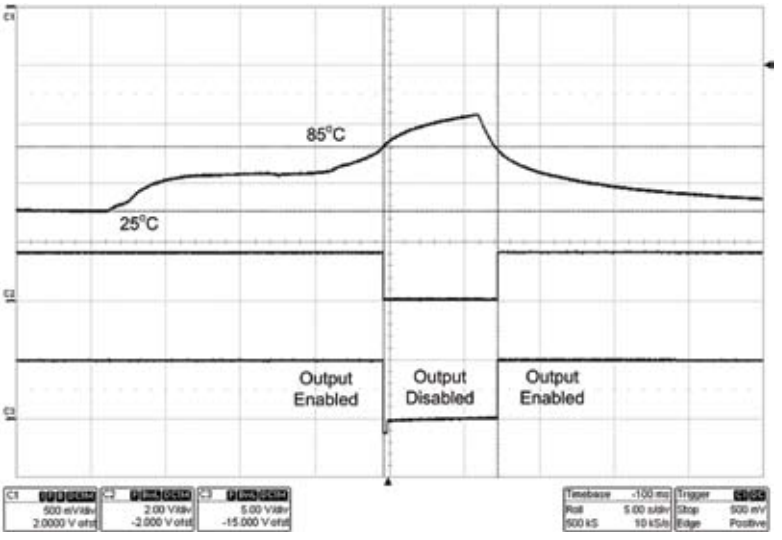

Figure 2 As the temperature rises above the threshold (top trace), the output of the temperature sensor (middle trace) goes low, forcing the hot-swap switch to disconnect power (bottom trace) from the circuit.

Add headphones to a Class D amplifier

Hiroshi Fukushima, Technical Research Center,
D&M Holdings Inc, Kawasaki City, Kanagawa, Japan

The MAX9704 from Maxim (www.maxim-ic.com) is a small and efficient Class D audio power amplifier. Its fully balanced inputs and Class D outputs make it a convenient chip to directly drive speakers. Sometimes, though, you want to have a headphone output to keep the office environment. Class D power amplifiers usually have fully balanced, bridged outputs on each channel. If the amplifier drives separate speakers, you can use an attenuator circuit (**Figure 1**). A problem arises, however, with grounded headphones: Stereo headphones use three-pole plugs with which the negative side of each speaker connects to a common ground. Thus, you may think that you can't directly connect head-

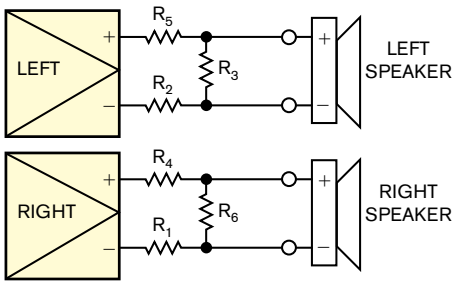

Figure 1 A Class D amplifier has separate drivers for each speaker.

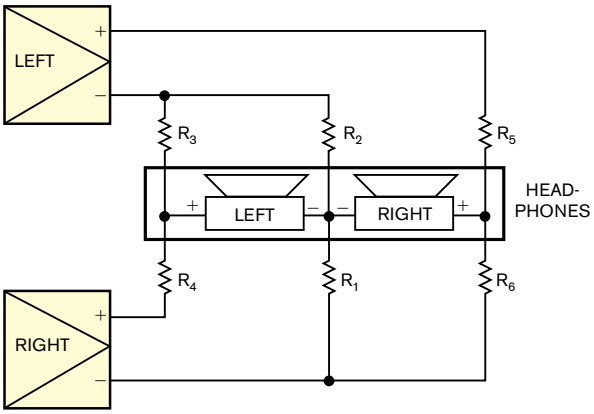

Figure 3 This speaker configuration lets you connect headphones with a common ground to a Class D amplifier.

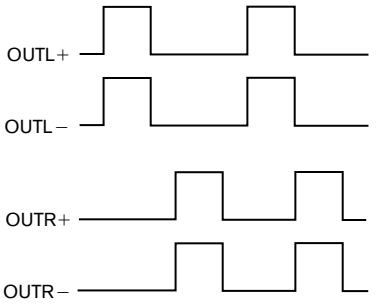

Figure 2 The MAX9704 applies power to one channel at a time.

phones to a Class D amplifier without using a transformer.

To solve the problem, look at the output waveform of the MAX9704 as it swings (**Figure 2**). Each channel output alternates between high and low. You can take advantage of the fact that the channels aren't on at the same time by configuring your circuit like the one in **Figure 3**.

Figure 4 shows the circuit details. Because the MAX9704 alternates the outputs of each channel, the R_3/R_6 combination doesn't affect the channel's drivers. Resistors R_3 and R_2 connect to the left output terminal. Resistors R_4 and R_1 connect to the right output terminal. The inactive channel's output voltage must be the same voltage, which means that R_4, R_1, and R_6 connect to the same voltage when the left-channel output is active. R_3, R_1, and R_5 connect to the same voltage when the right-channel output is active. The values of R_1 and R_2 affect how much crosstalk you get between channels. The values in **Figure 4** provide sufficient channel separation. EDN

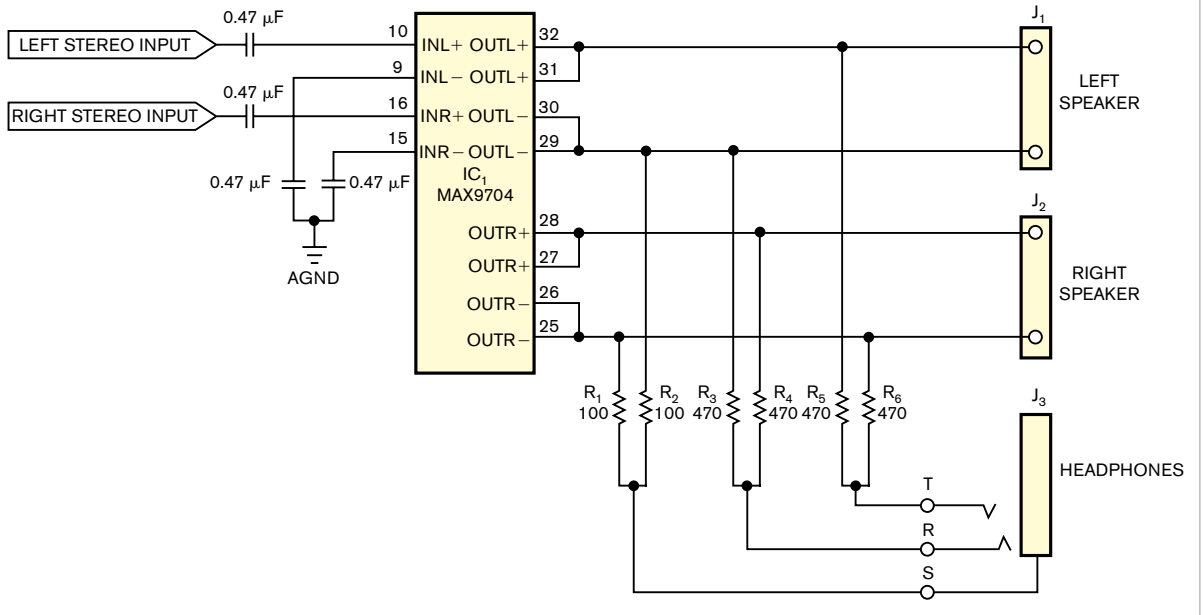

Figure 4 With the resistors in place, you can connect headphones to the MAX9704 amplifier.

Circuit eases power-sequence testing

Goh Ban Hok, Infineon Technologies Asia Pacific Ltd, Singapore

Systems on chip (SOCs) normally require one power supply for the core and another for I/O. To properly apply power to the device, you often need one supply to apply power before the other. The circuit in **Figure 1** lets you test the power sequencing of the SOC. Two TPS75501 linear regulators, IC_3 and IC_4, generate two power supplies. The TPS75501 adjustable regulator provides output voltages of 1.22 to 5V from a maximum input of 6V. The circuit uses 5V as the input source, and it can supply as much as 5A. The SOC requires 3.3 and 1.5V. The following **equations** describe how to set the voltages. $V_{OUT1}=V_{REF}\ (1+R_4/R_5)$ for IC_3, and $V_{OUT2}=V_{REF}(1+R_6/R_7)$ for IC_4. The reference voltage is 1.22V.

In the circuit, R_5 and R_7 are 30 kΩ. Variable resistor R_4 is 7 kΩ for the 1.5V supply, and R_6 is 50 kΩ for the 3.3V supply. Green LED D_2 lights when the 3.3V supply is present, and red LED D_1 lights for the input-supply voltage. Pin 1 of the TPS75501 is the enable pin. When low, it enables the output voltage at Pin 4. Switch S_2 selects the sequence of the power supplies. IC_1 is a 555 timer operating as a monostable circuit. It provides the delay between the two power supplies. You can adjust the delay by using the time constant of R_3 and C_3: Delay=$1.1\times R_3C_3$.

C_3 is 33 µF and R_3 is 11 kΩ for a 400-msec delay between powering the two supplies. The timer triggers with a negative pulse at Pin 2 of IC_1. It produces a positive pulse at Pin 3 of IC_1. The output becomes inverted at IC_{2A} before passing to IC_6's Pin 11. IC_5 and IC_6 are the latched circuits. The set pin, S, connects to the 5V supply, and the reset pin, R, connects through resistors R_2 and R_{10} and capacitors C_4 and C_7 to ensure that the Q output is high during the initial power-up stage. Regulators IC_3 and IC_4 are initially off.

When analog switch S_2 is in the on position, the sequence of the 1.5V power supply starts first, and the 3.3V supply follows. To start the power-sequence testing, press and release trigger switch S_1 to momentarily produce

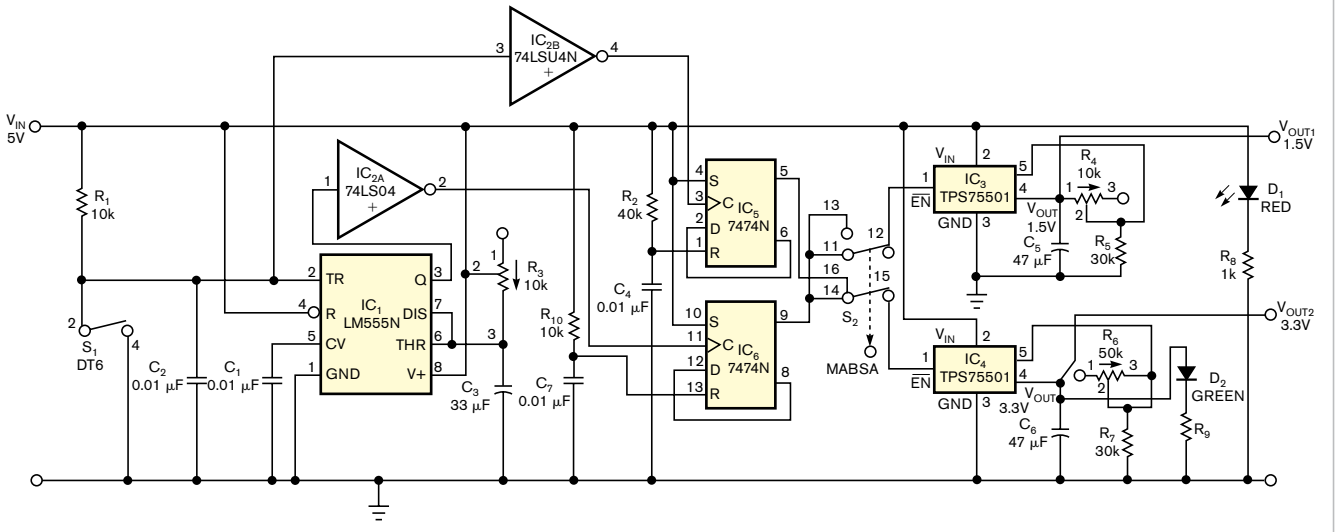

Figure 1 A configurable sequencing circuit uses a 555 timer to delay one power supply.

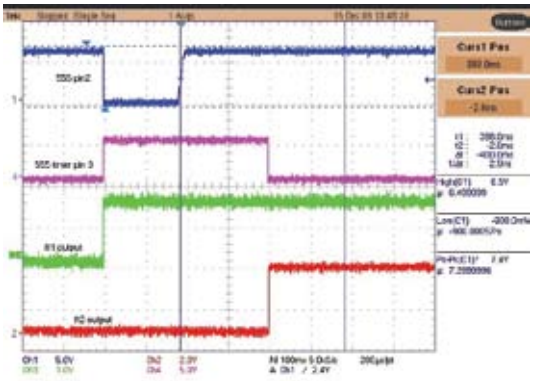

Figure 2 The 1.5V power supply (green trace) comes on first, and the 3.3V supply (red trace) and 555 timer follow.

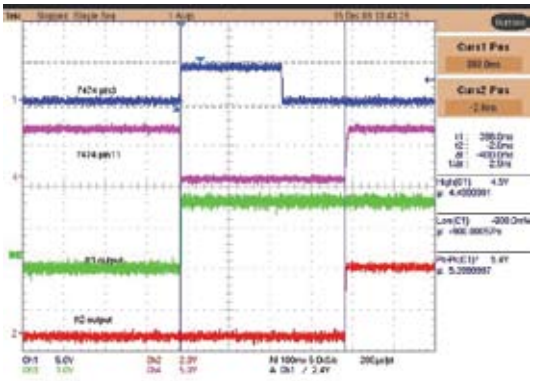

Figure 3 The 1.5V power supply (green trace) comes on first, and the 3.3V supply (red trace) and 7474 latch-circuit input follow.

a low pulse. This pulse triggers the 555 timer, IC_1, which produces a positive pulse. This pulse in turn produces a delay before enabling IC_4's power 3.3V supply. When you press and release S_1, another signal goes to inverter IC_{2B} before passing to the latch pin, Pin 3 of IC_5. There is no delay for the 1.5V regulator that connects to this pin. It enables IC_3's 1.5V power supply. Because IC_3's enable pin immediately receives the enable signal, it produces the 1.5V without delay. IC_4's enable pin, which receives a signal after the delay by the 555 timer, later produces the 3.3V, thus achieving the power sequence. The 1.5V power supply comes first when you press S_1, and the 3.3V power supply comes on only after the 555 timer delay (**figures 2** and **3**).

Switch S_2 connects to pins 13 and 16. When S_2 is off, the power sequence changes. In this case, the 3.3V supply powers up first, and the 1.5V supply follows (**figures 4** and **5**). When you press S_1, the 3.3V power supply comes first, and the 1.5V supply follows after the 555 timer delay. EDN

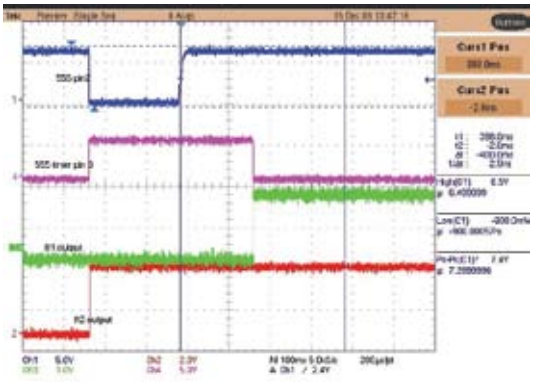

Figure 4 The 3.3V power supply (red trace) comes on first, and the1.5V supply (green trace) and 555 timer follow.

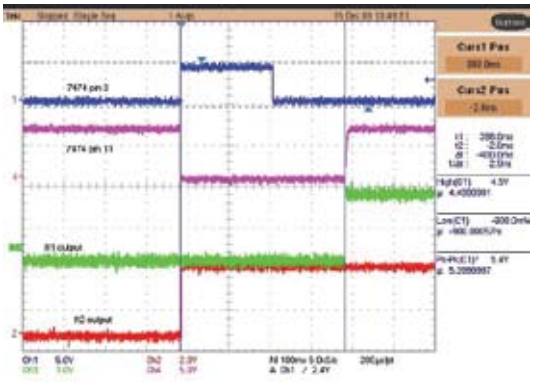

Figure 5 The 3.3V power supply (red trace) comes on first, and the 1.5V supply (green trace) and 7474 latch-circuit input follow.

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READERS SOLVE DESIGN PROBLEMS

Quasiresonant flyback converter easily charges energy-storage capacitors

Todor Arsenov, Toronto, ON, Canada

Designers often use chargers with flyback topologies to quickly charge energy-storage capacitors (**references 1** and **2**). In a flyback topology, the energy transfer takes place only when the charger's power MOSFET is off, which effectively isolates the power switch from the load, comprising high-energy storage-capacitor banks. Thus, the voltage levels on the circuit transformer's secondary can vary from zero to a predetermined value and corresponding energy level without any significant stress on the components on the primary side of the transformer.

The classical flyback capacitor charger operates in CCM (continuous-conduction mode). Flat-topped, short-duration current pulses on the transformer's secondary charge the storage capacitors (**Reference 3**). Unfortunately, this charging strategy requires complex control circuitry to limit both the secondary current and the capacitor voltage. Most circuits use a specialized PWM (pulse-width-modulation)-controller IC, which increases the overall cost of the charger. Another disadvantage of the CCM is the small portion of energy that accumulates during the on-time of MOSFET conduction:

$$\Delta W = \frac{1}{2} \times (L_P \times I_{P_{PK}}^2 - L_P \times I_{P_{OFFSET}}^2),$$

where $I_{P_{OFFSET}}^2$ signifies the initial nonzero primary current at the beginning

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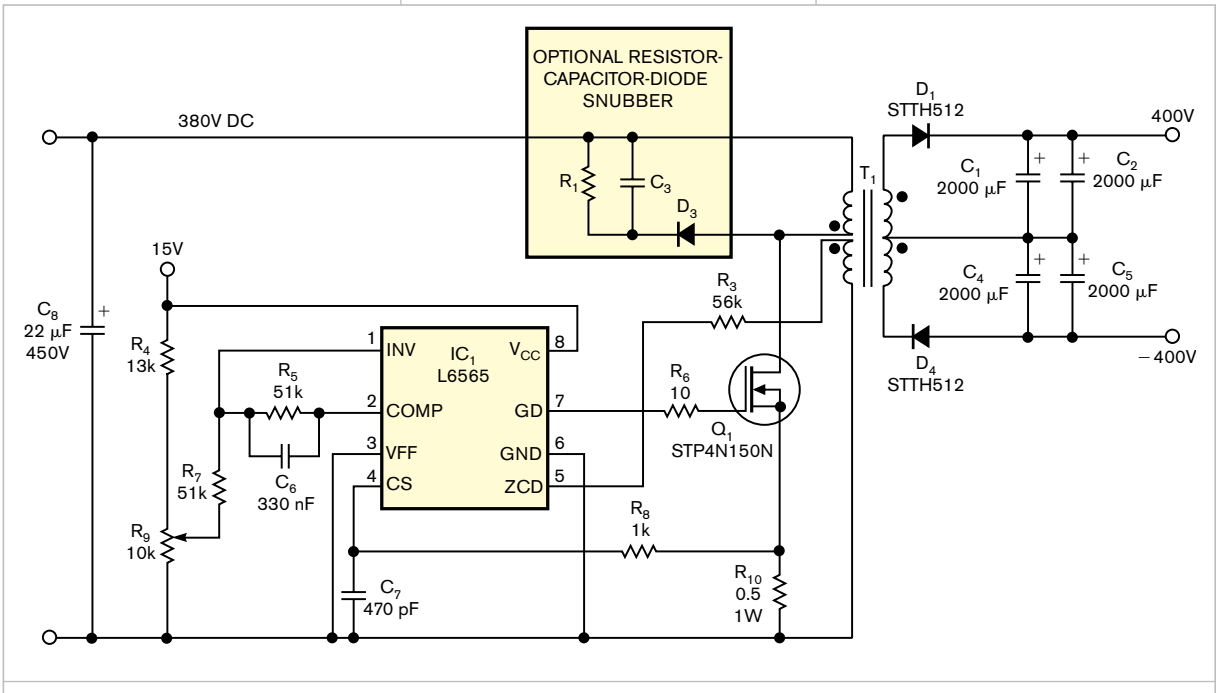

Figure 1 A flyback capacitor charger uses BCM operation.

of the on-time interval.

Only this limited portion of energy transfers from the primary to the secondary sides and enters the storage capacitor. Therefore, you can considerably increase the amount of energy transferable to the capacitive load if the converter can operate in BCM (boundary-conduction mode). The secondary current becomes zero, the power MOSFET turns on, and the primary current builds from zero. Thus, a bigger portion of energy accumulates during every consecutive on-time interval:

$$\Delta W = \frac{1}{2} \times L_P \times I_{P_{PK}}^2 .$$

With all other conditions equal, BCM operation ensures faster accumulation of a predetermined amount of energy because of the bigger stored portions of energy during the on-time intervals. Many converter circuits that operate using BCM incorporate PWM controllers that implement BCM operation for capacitor charging. These circuits often use Maxim (www.maxim-ic.com) MAX8622 or Linear Technology (www.linear.com) LT3468 ICs. These ICs are specialized devices to accommodate BCM operation.

You can, however, implement flyback BCM operation without these specialized parts. Manufacturers implement BCM in the variable-frequency versions of flyback converters, which are quasiresonant, ZVS (zero-voltage-switching) converters that commonly find use in TV SMPS (switched-mode-power supplies). For example, you can use the STMicroelectronics (www.st.com) quasiresonant-SMPS-controller L6565 to build a flyback capacitor charger working in BCM (**Reference 4**). Doing so eliminates the need for using a specialized chip for capacitor chargers.

Figure 1 shows the power stage of a charger using the ST L6565. It achieves the BCM using a second primary winding on T_1 that feeds the transformer-sensing input at the ZCD pin of the L6565. The voltage of this winding is a scaled-down replica of the drain-to-source voltage of power MOSFET Q_1. When the circuit interrupts the secondary current—indicating full demagnetization of T_1—it detects the minimum of the first valley of ringing, and the L6565 turns on the MOSFET. This action eliminates the idling and zero-phase-time intervals, thus establishing BCM. The elimination of the zero-phase-time intervals greatly reduces the charging time of the storage capacitors.

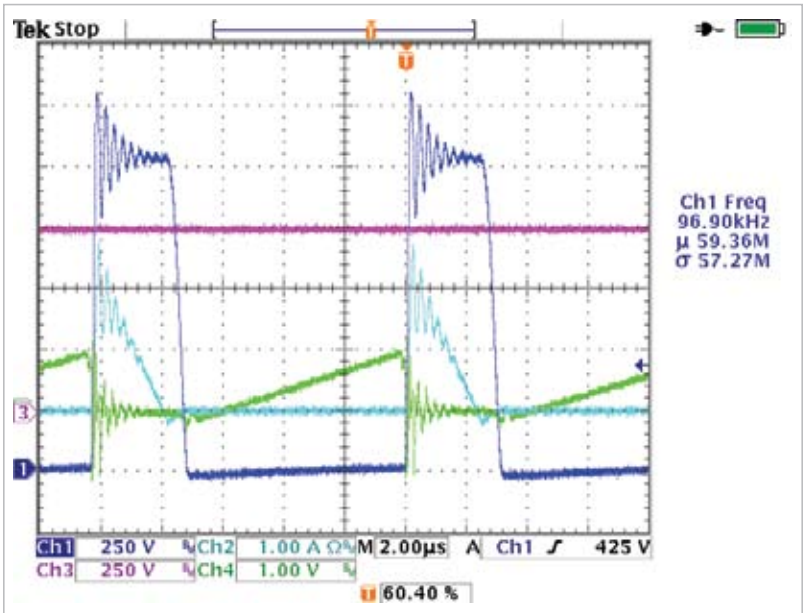

Figure 2 When the secondary current reaches 0A, the MOSFET turns on, and the primary current increases from 0A.

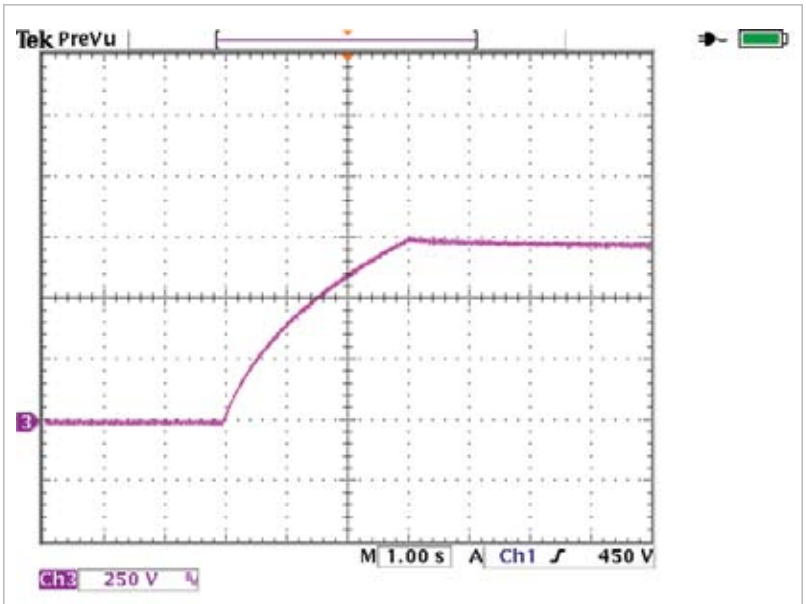

Figure 3 The output-capacitor voltage reaches its full level in about 3 seconds.

At the beginning of the charging sequence, the output voltage is low because of the large capacitance values. The secondary current decreases slowly. The reflected voltage on the primary side is too low to trigger the ZCD pin of the L6565. Thus, the L6565's

initial starting timer sets the switching frequency to 2.5 kHz at the start of charging. The output voltage across the storage capacitors increases to a point at which the switching frequency becomes variable because of the demagnetization of the transformer core. **Figure 2** shows that, as soon as the secondary current (Channel 2) becomes 0A, the power MOSFET turns on, and the drain-to-source voltage decreases (Channel 1). At that time, the primary current again increases (Channel 4). At the output voltage close to full charge, the switching frequency is approximately 100 kHz. **Figure 3** shows the total voltage of 750V across C_1, C_2, C_4, and C_5 within a 3-second charging time.

The waveforms in **figures 2** and **3** are evaluation measurements of a prototype capacitive charger using the L6565 and power MOSFET STP4N150. A low-power PFC (power-factor-correction) stage, using transition-mode-PFC controller L6562, delivers the input-bus voltage of 380V dc. This configuration ensures not only the dc-voltage bus for the power stage of the charger, but also a high power factor during the charging phase. EDN

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First-event detector has automatic-reset function

Vasil Borodai, Zaporozhje, Ukraine

The circuit in **Figure 1** lets you indicate which game player presses a button first. Each button has a corresponding LED that indicates the pressing of the button. All other LEDs remain locked out until someone presses a reset button. When a player presses a pushbutton, the corresponding optoisolator turns on, which illuminates the appropriate indicator LED. The LED remains on after the player releases the pushbutton. The voltage at Point A pulls down to nearly 3.7V, which you determine by adding the forward voltage of the optoisolator's internal LED, the phototransistor's voltage, and the LED's voltage: 1.3+0.6+1.8V=3.7V. The green LED then turns off.

Beginning at time T_1 (**Figure 2**), no other player can change the situation by pressing a pushbutton because switching on any other optoisolator requires a voltage exceeding 3.9V. Resistor R_1 depends on V_{PS} such that $R_1=(V_{PS}-V_{D1})/I_{OPTOLED}$, where V_{PS} is the power-supply voltage, V_{D1} is the voltage of diode D_1, and $I_{OPTOLED}$ is the current of the optoisolator LED. Thus, for a 9V power supply, R_1 has a value of 1.5 kΩ. When a player presses the reset button, the player LEDs turn off, and the green LED illuminates. The voltage at Point A returns to 9.2V (time T_2 in **Figure 2**).

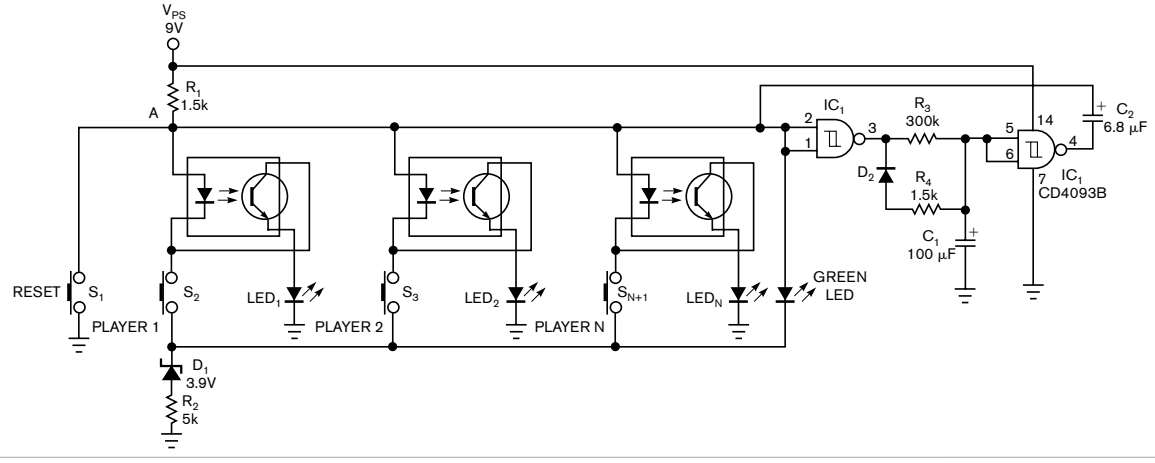

Figure 1 This circuit lets you indicate which game player presses a button first.

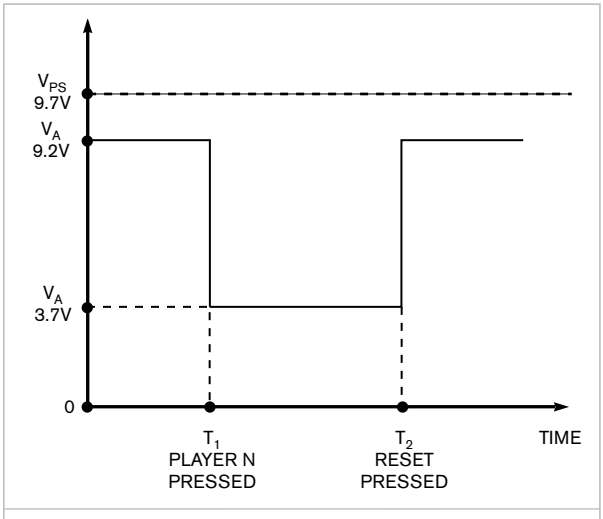

Figure 2 When a player presses the reset button, the player LEDs turn off, and the green LED illuminates. The voltage at Point A returns to 9.2V.

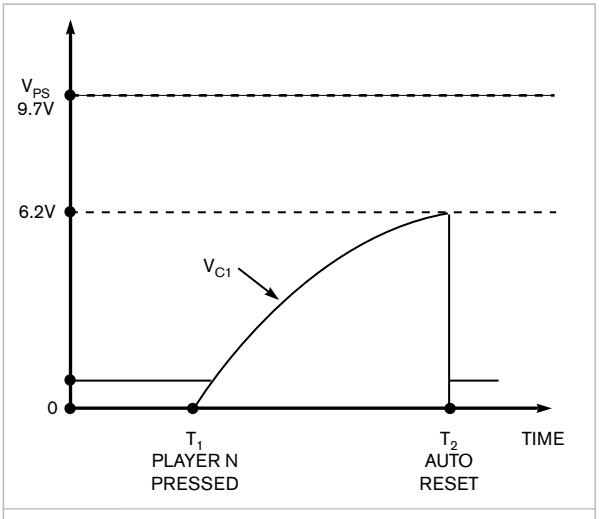

Figure 3 When Point A drops to 3.7V, the inputs at IC_1, pins 1 and 2, go low, and the output at Pin 3 goes high, charging C_1.

You can also add an auto-reset feature to the circuit. When Point A drops to 3.7V (time T_1 in **Figure 3**), the inputs at IC_1, pins 1 and 2, go low, and the output at Pin 3 goes high, charging C_1. After about 30 seconds (time T_2 in **Figure 3**), C_1 has enough voltage to force IC_1's Pin 4 low. R_3 and C_1 determine the charging time. A pulse of current flows through C_2, which forces the voltage at Point A to nearly 2V. That action momentarily interrupts the current in any optoisolator LED. As a result, the circuit automatically resets, and the green LED lights. IC_1's Pin 3 goes low, which discharges C_2 through R_2, resetting the circuit to its original state. EDN

Signal-powered linear optocoupler provides isolated control signal

Mitja Rihtarsic, Škofja Loka, Slovenia

The circuit in **Figure 1** provides an isolated control voltage, such as 0 to 10V. In the low part of the range, 0V to approximately 2V, the controlled device is off. Therefore, the upper part of the range must be as linear as possible. You can meet this requirement using a linear optocoupler, such as Vishay's (www.vishay.com) IL300 or Avago Technologies' (www.avagotech.com) HCNR200 or HCNR201.

These optocouplers each comprise an LED and a photodiode on the transmitting side and an identical photodiode on the receiving side. Because of this construction, the emitted light from the LED should cause the same current to flow in both photodiodes. The current through the photodiode on the receiving side, feedforward current I_{FF}, is the output current, and you must set this current in proportion to the transmitted signal voltage, V_1. This current equals the feedback current, I_{FB}, through the transmitter-side photodiode. A feedback loop around the emitting side of the optocoupler keeps the feedback current in proportion to the transmitted signal. When the feedforward current and the feedback current are equal, the output current is proportional to the transmitted signal.

The hidden cost, however, is a power supply. You need some power on both

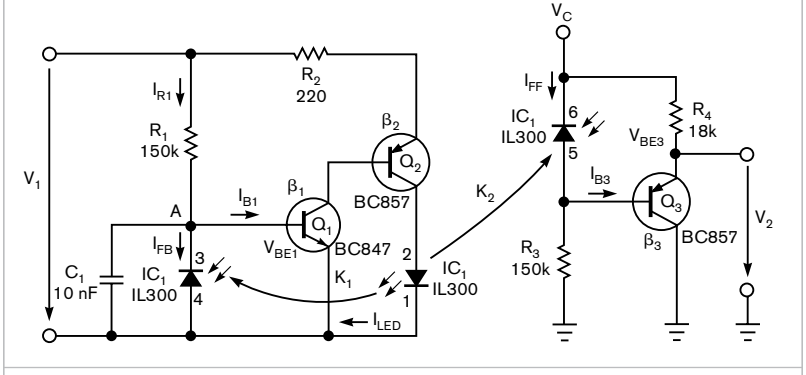

Figure 1 Optocoupler IC_1 isolates the control circuit's input and output.

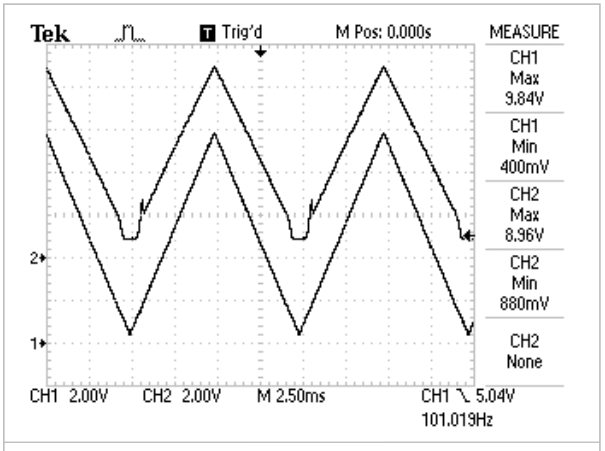

Figure 2 The output voltage (upper trace) turns off when the input voltage (lower trace) gets too low.

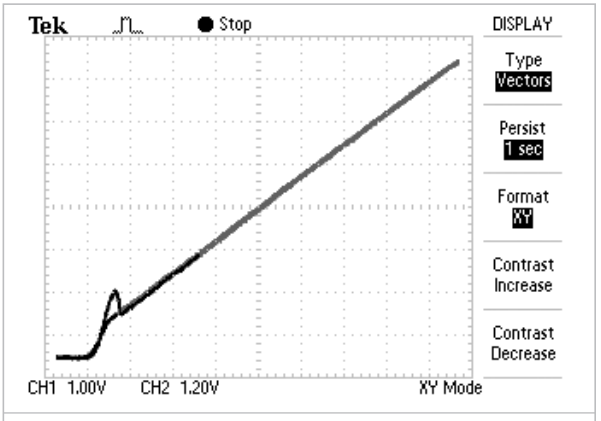

Figure 3 An XY plot of the circuit's input and output voltages shows linearity once the input voltage is high enough to power the circuit.

sides of the signal path. The circuit in this Design Idea uses power from signal voltage V_1 to supply a feedback loop in the transmitting side similar to the way some circuits in a 4- to 20-mA loop get power from the loop current. Both photodiodes operate in reverse-biased, photoconductive mode. The currents through them are proportional to incident-light flux, which feedback gain K_1 and forward gain K_2 describe.

$$K_1 = \frac{I_{FB}}{I_{LED}}, \quad (1)$$

where I_{LED} is the LED's current, and

$$K_2 = \frac{I_{FF}}{I_{LED}}. \quad (2)$$

A description of the circuit begins with a sum of the dc currents at Node A.

$$\frac{V_1 - V_{BE1}}{R_1} = I_{FB} + I_{B1}. \quad (3)$$

The gains of both transistors amplify current I_{B1} into the base of Q_1. The amplified current then flows through the LED.

$$I_{LED} = \beta_1\beta_2 \times I_{B1}. \quad (4)$$

Equations 1 through **4** yield the output feedforward current:

$$I_{FF} = (V_1 - V_{BE1}) \times \frac{1}{R_1} \times \frac{K_2\beta_1\beta_2}{K_1\beta_1\beta_2 + 1}. \quad (5)$$

When the product of feedback gain K_1 and transistor gains β_1 and β_2 is much greater than one, you can cancel out the transistors' gains, yielding a characteristic that is linear:

$$I_{FF} = (V_1 - V_{BE1}) \times \frac{1}{R_1} \times \frac{K_2}{K_1}; K_2\beta_1\beta_2 >> 1. \quad (6)$$

The ratio of feedback gain K_1 and forward gain K_2 is transfer gain K_3. Because K_1 and K_2 are similar, K_3 is approximately one. In reality, K_3 may deviate, but it changes less than K_1 or K_2 alone:

$$K_3 = \frac{K_2}{K_1}. \quad (7)$$

Equation 6 subtracts the base-to-emitter voltage from the input voltage. Although the base-to-emitter voltage is not constant, it is desirable to remove it. You accomplish this task using the emitter follower in the receiving circuit. The output voltage, V_2, is a sum of voltage across R_3 and the base-to-emitter voltage of Q_3.

$$V_2 = (I_{FF} + I_{B3}) \times R_3 + V_{BE3}. \quad (8)$$

You can use a different **equation** to yield the feedforward output current:

$$I_{FF} = \left((V_1 - V_{BE1}) \times \frac{1}{R_1} - I_{B1}\right) \times K_3. \quad (9)$$

You can rearrange **equations 8** and **9** as:

$$V_2 = V_1\frac{R_3}{R_1}K_3 + \left(V_{BE3} - V_{BE1}\frac{R_3}{R_1}K_3\right) + R_3(I_{B3} - I_{B1}K_3). \quad (10)$$

In the first term in **Equation 10**, the ratio of resistors R_3 and R_1 is approximately 1-to-1. You must be careful with the transfer gain, K_3, which is the reason that K_3 remains in **Equation 11**.

$$V_2 \approx K_3 \times V_1. \quad (11)$$

When K_3 is one, voltages V_{BE1} and V_{BE3} cancel each other to some degree. Therefore, **Equation 11** omits the second term in **Equation 10**. Base current I_{B3} depends on resistor R_4 and the output load. When you can set both base currents to be equal, the last term would cancel out, too. The values of resistor R_2 and capacitor C_1 must be small enough so that transistors Q_1 and Q_2 don't saturate. C_1 enhances stability.

Figure 2 shows the necessary voltage for the circuit to begin operation. The output voltage (upper trace) has flatness at its lowest voltages as opposed to the input voltage (lower trace). **Figure 3** shows the two signals' linearity. Dividing the measured maximum of voltages V_1 and V_2 yields 0.91V. A test circuit uses an IL300, which has a gain of 0.851 to 0.955. The measurement meets the requirements of **Equation 11** despite the **equation**'s simplifications. EDN

Dark-activated switch needs only three components

Abel Raynus, Armitron International, Malden, MA

Assume that you have a device that receives its power from the main 120 or 220V-ac line and you need to add a switch between the ac line and the device so that the device works only when it is dark. Although you may think this task would be trivial, it is difficult to find a workable approach because most of the published schematics need 6 to 12V-dc power supplies and relays. Several off-the-shelf dark-activated switches, such as devices from Suns International (www.suns-usa.com), are available, but they're expensive for a consumer product. After looking at products from dozens of Web sites, you may decide to make your own. The solution is simple and inexpensive.

The circuit in **Figure 1** employs an internally triggered triac, which Teccor Electronics (www.teccor.com) originally developed. The primary purpose of any triac is bidirectional-ac switching. The Quadrac triac has a built-in triggering device with the threshold-voltage level of approximately 40V. To achieve this level, the circuit uses a voltage divider comprising a photocell and resistor R_1. When you light the photocell, its voltage drop is lower than the triggering level of the threshold voltage, and Q_1 is locked, so the load disconnects from the ac line. When it becomes dark, the peak voltage amplitude on the photocell increases to 40V, opening Q_1 and making the load connect to the power line.

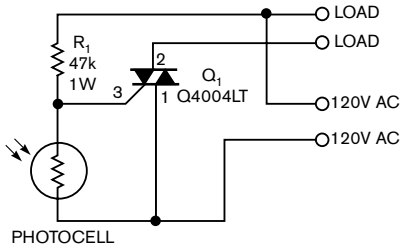

Figure 1 This dark-activated switch needs only a photocell, a resistor, and a triac to switch between the ac line and the device.

The choice of Q_1 depends on the load current and ac-line voltage. This circuit uses the Q4004LT from Littelfuse (www.littelfuse.com) with a maximum current of 4A rms and a voltage of 400V. You can use any photocell, but this circuit uses an off-the-shelf model and accordingly uses a value of 47 kΩ for R_1 to achieve reliable switching. For an inductive load, add a 100Ω resistor in series with a 0.1-μF capacitor between pins 1 and 2 of Q_1. EDN

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READERS SOLVE DESIGN PROBLEMS

High-speed op amp enables IR-proximity sensing

Arpit Mehta, Maxim Integrated Products Inc, Sunnyvale, CA

IR (infrared)-proximity sensors can sense the presence of an object, its distance from a reference, or both. Applications include speed detection, sensing of the hand in automatic faucets, automatic counting or detection of objects on conveyer belts, and paper-edge detection in printers. The latest-generation smartphones, for example, can turn off the LCD touchscreen to prevent the accidental activation of buttons when you press the screen against your chin or your ear.

To sense an object, a proximity sensor transmits IR pulses toward the object and then "listens" to detect any pulses that reflect back. An IR LED transmits the IR signals, and an IR photodetector detects the reflected signal. The strength of this reflected signal is inversely proportional to the distance of the object from the IR transceiver. Because the reflected IR signal is stronger when the object is close, you can calibrate the output of the photodiode detector to determine the exact trigger distance of an object. The trigger distance indicates the threshold for making a decision on whether an object is present.

The photodiode detects IR not only that the object reflects, but also from the ambient conditions. You must filter out this IR noise to prevent false detections. A common method is to modulate the LED's IR signal with a convenient frequency and then detect only the IR with that modulation, which identifies it as a reflection from the object.

This Design Idea describes an IR-proximity sensor with simple transmitter and receiver sections (**Figure 1**). The transmitter consists of an Everlight (www.everlight.com) 940-nm IR11-21C IR LED, which turns on and off using a 10-kHz oscillator frequency. By varying the LED's current, you control the level of transmitted power and, hence, the detection range. To save power, the transmitting pulses have a typical duty cycle of only 10%.

The receiver circuit demodulates and amplifies the IR signals that the Everlight PD15-22C photodiode detects; the photodiode's peak sensitivity occurs at 940 nm. The photodiode output ac couples to the op amp's noninverting input. This coupling allows the 10-kHz signal to pass, but the coupling capacitor sets a 300-Hz cutoff frequency that prevents dc noise and background IR from reaching the amplifier.

Low noise, high bandwidth, and rail-to-rail-I/O capability make the op amp a good choice for demodulation and amplification in this circuit. In addition, its RF immunity prevents the annoying 217-Hz audio buzz that you commonly find in GSM (global-system-for-mobile)-communications cell phones. For the IR receiver, the op amp acts as a gain-of-100, second-order bandpass fil-

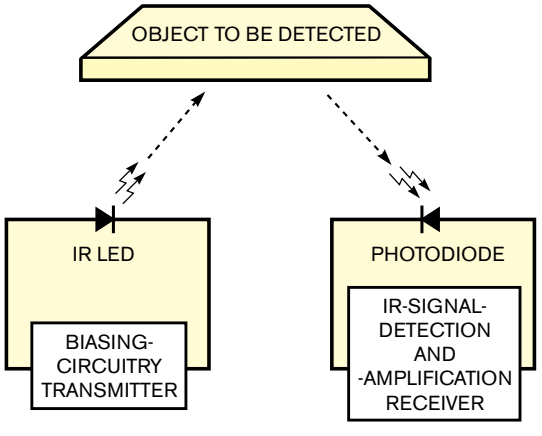

Figure 1 An IR-proximity sensor detects an object by receiving reflected light.

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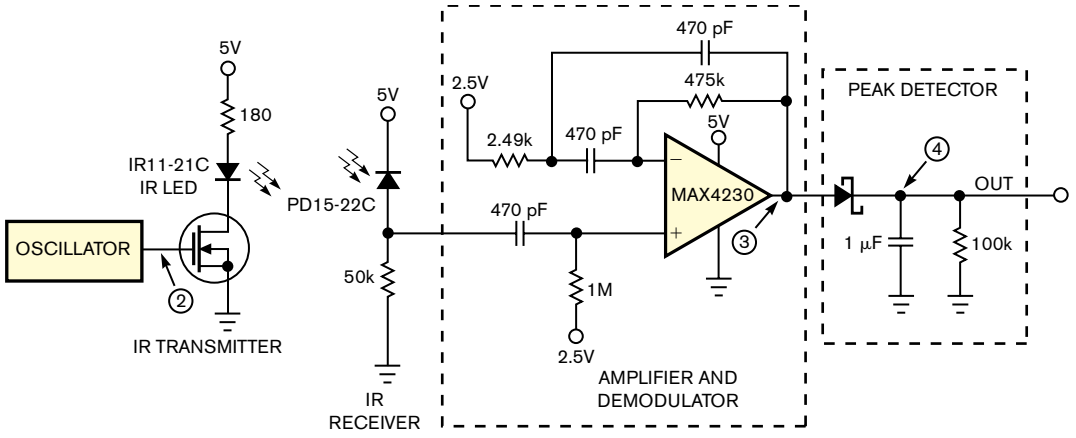

Figure 2 An IR transceiver detects the presence of an object and provides an approximate distance from the transceiver.

ter with a center frequency of 10 kHz. Thus, the op amp amplifies the incoming IR signals and demodulates them with a bandpass filter.

With no input IR signal present, the op amp is biased at 2.5V. With a 10-kHz IR signal incident, its output varies around 2.5V with a dynamic range of 5V. The output drives a simple diode detector, which rectifies the 10-kHz signal and provides a dc signal proportional to its amplitude. This analog-output signal is proportional to the distance of the object from the IR transmitter. You can use it as is or feed it to an ADC for further processing.

Figure 2 shows circuit operation at three nodes for objects at 1.2 and 1.4 in. from the IR transceiver. The circled numbers in **Figure 2** refer to the oscilloscope traces in **Figure 3**.EDN

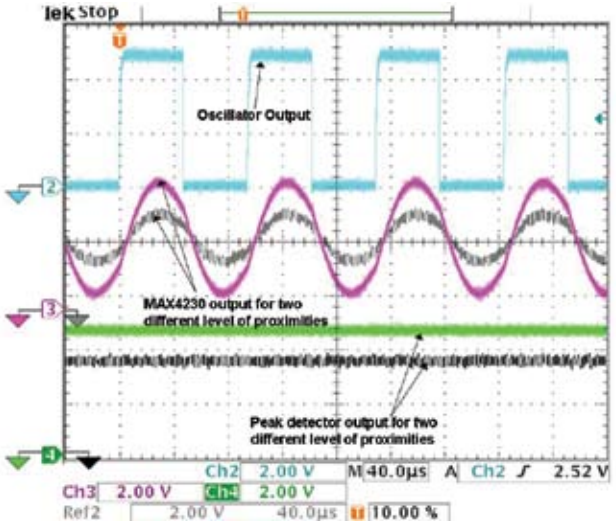

Figure 3 Different distances produce received waveforms of different amplitudes.

Set your lights to music

Hanif Saeed, Maxim Integrated Products Inc, Sunnyvale, CA

As one of many ways you can implement a light show, the circuit in this Design Idea selectively activates various subsets in a group of six strings of lights, causing them to flash on and off according to the level and tempo of music you are playing. The stand-alone circuit requires no microcontroller, no software, and no trimming (**Figure 1**). You apply the audio signal you want to display to IC_1, a 12-bit ADC. The signal ranges from 0 to 2.048V, causing the first string of lights to come on at 2 mV. Although the circuit controls six ac outlets, you can expand it to control 12 outlets.

A short positive pulse at the CNVST pin of IC_1 triggers it to initiate a conversion, which the SCLK signal clocks. Its output (DOUT), which the rising edges of SCLK clock, comprises four leading zeros followed by the 12-bit conversion result, MSB (most-significant bit) first. Thus, one conversion requires 16 clock pulses at SCLK.

A vertical stack of six switched outlets, in which the top outlet represents the MSB, powers the display. You might, for example, plug a separate string of lights into each outlet. During operation, the circuit scans each conversion result as it is generated (MSB

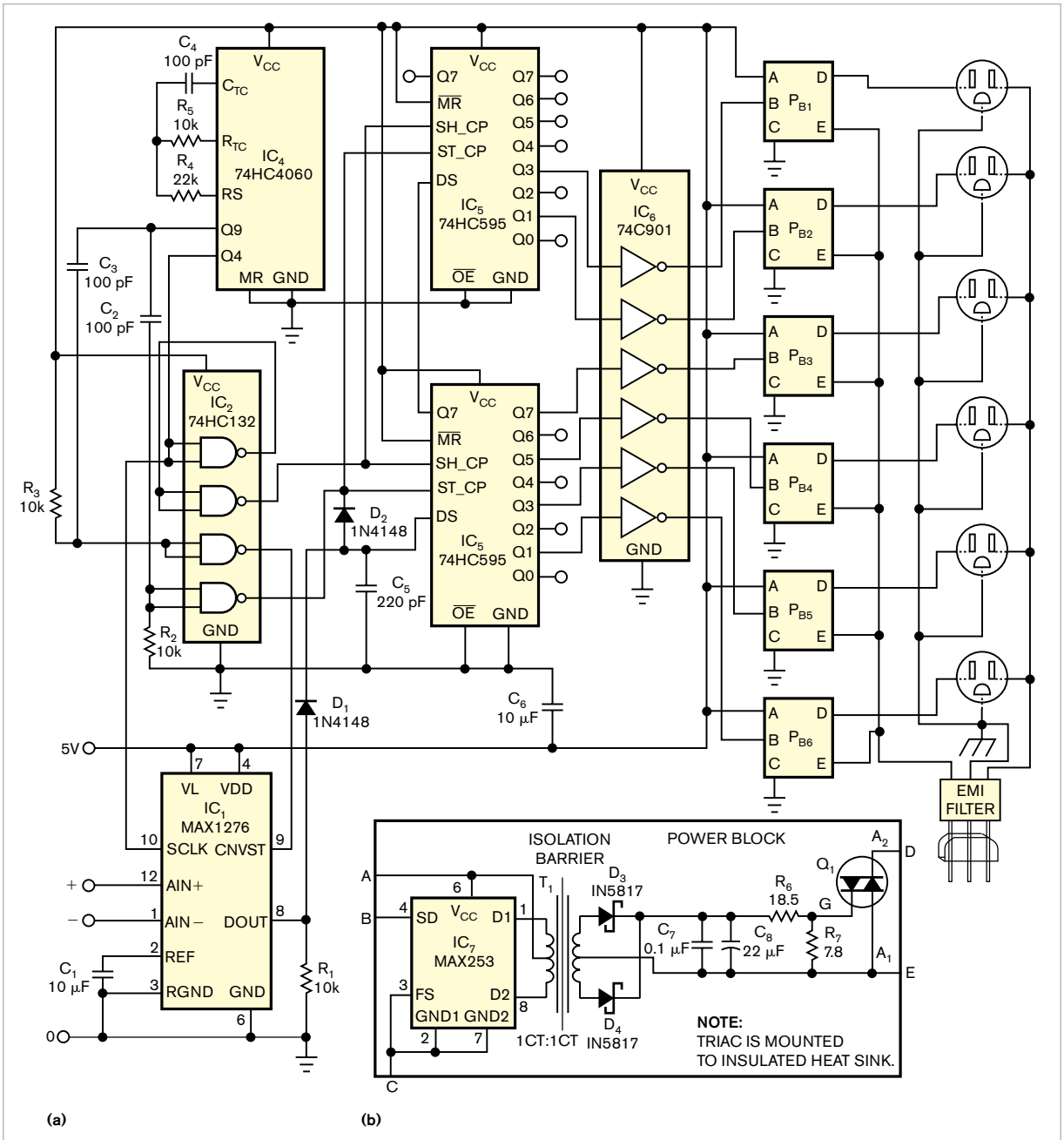

Figure 1 Driven by a 0 to 2.048V music signal at pins 12 and 1 of IC_1, this circuit activates the six ac outlets according to the music amplitude, in a logarithmic thermometer-code format (a). The power block (b) represents each of the power blocks, PB_1 through PB_6.

first, as described previously) and notes the first bit to assume a value of one. It then turns on the corresponding outlet and all those below it in the stack. The result is a logarithmic column, in which the change of input voltage necessary to move the column one step up or down (a 12.04-dB increment) is either quadruple or one-fourth the immediate value. Although the number of steps available equals the ADC's resolution of 12 bits, this circuit uses only every other one to drive the six outlets.

At DOUT, the first output bit with a value of one charges C_5 through D_1 to the logic-one level. The voltage on C_5 connects to the data input (DS) of the first of two cascaded 74HC595 ICs, which together form a 16-bit shift register. The signal that clocks the ADC, slightly delayed, also clocks this shift

register through the NAND gates in IC_2 and thereby inserts into the shift register the value present at its input. At the end of a conversion, the voltage stored on C_5 forces to one all the bits following the first one that exhibits a value of one.

At the completion of each conversion, a negative pulse applied to the ST_CP inputs of both 74HC595 ICs transfers these shift-register contents to a parallel-output register, IC_6. The same pulse discharges the storage capacitor through diode D_2, leaving the circuit ready for the next conversion scan. The parallel-register outputs then serve as drivers for the 12-bit logarithmic column, with the MSB driving the top outlet.

IC_4, a 74HC4060, serves as a clock and timing-sequence generator, and IC_2, a 74HC132, provides some necessary glue logic. For each connected 74HC595 output, the signal, which IC_6 inverts, activates the corresponding MAX253 transformer driver, IC_7 in one of the six power blocks. A 1-to-1 transformer isolates this driver signal, which then triggers solid-state TRIAC (triode for alternating current), Q_1, to its on state. For the component values in the **figure**, the circuit has a display-sampling rate of about 2.5 kHz and uses the 12th, 10th, eighth, sixth, fourth, and second bits to control the six outlets. The resulting light show adds an extra dazzle to the music you are playing.

This circuit operates at lethal voltages and requires proper handling. Note that the transformer must withstand a line level of 120V ac. It operates with incandescent light bulbs; you should not use any other type of light bulb. Even though the outlets are standard 120V-ac outputs for use with commercial incandescent lights, fast switching in the TRIACs makes them unsuitable for driving other types of loads, such as appliances, electronics, or ac adapters. Transformer T_1 is a TGM-350NA from Halo Electronics Inc (www.haloelectronics.com), and TRIAC Q_1 is a T1235-T from STMicroelectronics (www.st.com). For a video of this circuit in action, go to www.edn.com/090806dia. EDN

Current limiter allows large USB bypass capacitance

Daniel Morris, Group IV Technology, Renton, WA

The USB (Universal Serial Bus) specification requires a connected USB device to present a load to the host or hub of no greater than 10 µF in parallel with 44Ω, including the effects of any bypass capacitance visible through the device's voltage regulator. This limit avoids excessive voltage drop at the device as inrush current charges its capacitance. Occasionally, a bus-powered device needs more than 10-µF bypass capacitance to provide an adequate reservoir for current spikes. The circuit in this Design Idea repurposes a Linear Technology (www.linear.com) LTC6102 precision current-sense amplifier, IC_1, to limit inrush current below the specified maximum, allowing the device to use more capacitance when necessary.

The LTC6102 usually translates the voltage across a current-sense resistor to a larger ground-referenced voltage in an output resistor. The part features an amplifier with low offset voltage, letting you use low-value sense resistors. In the usual circuit configuration, output current flows through an onboard FET whose source connection connects to a force pin separate from the amplifier input pin to minimize errors across trace and pin resistances.

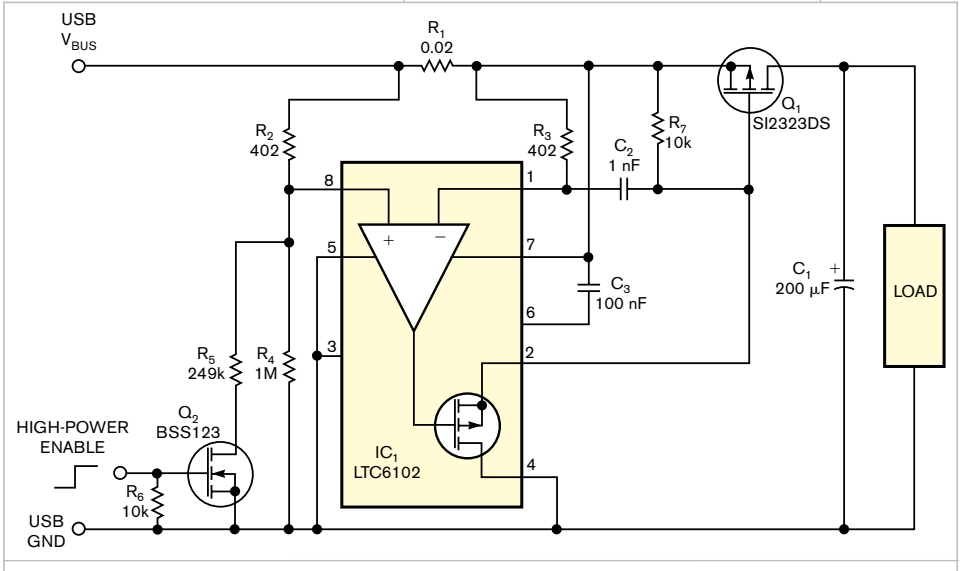

Figure 1 This circuit limits USB-device current both at connection and after configuration.

This circuit grounds the LTC6102's output pin and uses the onboard FET as a source follower to drive the gate of an external current-limiting FET (**Figure 1**). The feedback loop around the LTC6102 maintains equal voltages at the positive and negative inputs of the amplifier, pins 8 and 1 of IC_1. Resistor divider R_2/R_4 sets the positive input of the amplifier, IC_1's Pin

8, approximately 2 mV below the 5V USB-voltage rail. With Q_1 initially off at device connection, the negative amplifier input, IC_1's Pin 1, is higher than the positive input, causing the amplifier's output to go low. As the amplifier's output drops, the onboard FET follows, pulling the gate of Q_1 low and turning it on. Current increases in Q_1 until the voltage drop across sense resistor R_1 matches the drop across resistor R_2.

Resistor R_3 and capacitor C_2 compensate the feedback loop against oscillation and slow the turn-on of Q_1, preventing an initial current spike when the device connects to the bus. Capacitor C_3 bypasses a regulator on IC_1. Resistor R_7 meets the allowed maximum 1-mA current through the FET on IC_1. Q_1 turns on at a gate voltage low enough that it does not exceed the input range of 4V positive voltage to IC_1's Pin 7 to Pin 2.

Instead of the large capacitive load of C_1, the circuit presents a resistive load to the USB host equal to $R_1(R_2+R_4)/R_4=49.8\Omega$, lighter than the 44Ω maximum requirement. After C_1 charges, the circuit continues to limit current below the 100-mA maximum permitted to a low-power USB device. Upon configuration, the device can raise the current limit to the 500-mA maximum permitted to a high-power device by turning on FET Q_2 to place R_5 in parallel with R_4, increasing the voltage maintained across sense resistor R_1.EDN

High-speed pulse modulator retains signal envelope

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The circuit in **Figure 1** enables you to convert an arbitrary, relatively slowly varying voltage waveform to a new waveform in which the instantaneous values of the original waveform alternate with positive and negative signs. The new waveform retains information about the original waveform, and its mean value approaches zero. This situation holds true for any input waveform, even a dc voltage. The nearly zero dc component of the output of the circuit in conjunction with the upconversion of the frequency band lets the modulated waveform pass easily through a transformer (**Figure 2**).

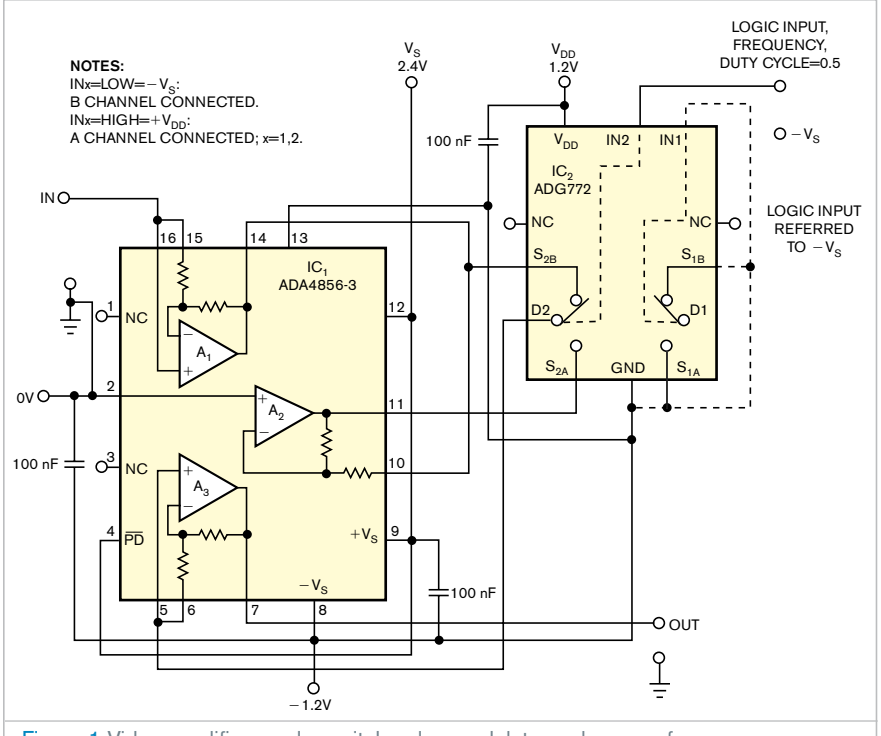

Figure 1 Video amplifiers and a switch pulse-modulate analog waveforms.

The circuit uses just one and one-half ICs from Analog Devices (www.analog.com). IC_1 is a triple video amplifier, the ADA4856-3 with a gain of two (**Reference 1**). Amplifier A_1 acts as a voltage follower, which gives a maximally smooth and flat frequency response. Amplifier A_2 acts as an inverter, having a voltage gain of negative one, and A_3 serves as an impedance converter with a voltage gain of one.

IC_2, an ADG772 high-speed 2-to-1 multiplexer (**Reference 2**), alternately switches the outputs of A_1 and of A_2 to the input of A_3. You must keep the duty cycle of IC_2's logic-control signal, IN2, close to 0.5 to ensure the "zero" mean value of the output voltage, even at a nonzero input voltage. At a modulation rate, or the frequency of the logic-control signal, of approximately 6 MHz, the output voltage's dc component shifts negligibly only from the low-frequency mean-offset voltage of the circuit, which is less than 4 mV.

Experiments have confirmed this value for an input voltage of 0V and for the precise reference dc voltage of 0.8188V. At a frequency of 60 MHz, the dc component of the output voltage remains at about 4 mV for an input voltage of 0V and rises to approximately 175 mV for an input voltage of 0.8188V. This result is still remarkable because the ADG772 is a BBM (break-before-make) type of multiplex-

er/switch. During time interval t_{BBM}, which is typically 5 nsec, both the S_{2A} and S_{2B} switches are temporarily off. Thus, the corresponding switch is on for approximately 8.2 nsec within a half-period of a 60-MHz control signal, yielding an on-state duration of only 3.2 nsec. An eventual 320-psec difference of the turn-on times of switches S_{2A} and S_{2B} would cause a shift in the dc component of 81.88 mV. The corresponding dc components of output voltages for an input voltage of 0V and an input voltage of 0.8188V differ by about 175 mV as a result of the difference in turn-on times of S_{1A} and S_{1B}. You can estimate this difference using the following **equation**:

$$320\ \text{psec} \times \frac{175\ \text{mV}}{81.88\ \text{mV}} \cong 684\ \text{psec}.$$

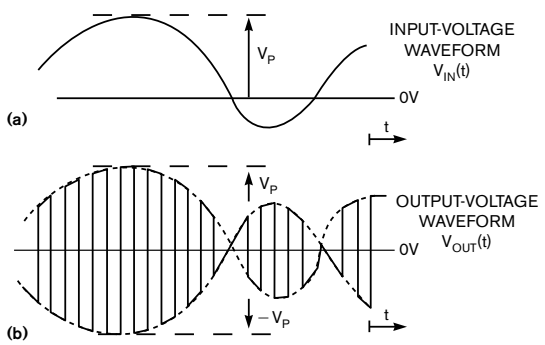

Figure 2 The pulse-modulated waveform can pass through a transformer, providing signal isolation. Comparing the input waveform, $V_{IN}(t)$ (a) with the output waveform, $V_{OUT}(t)$ (b) shows that the frequency spectrum of the output waveform upconverts while its dc component becomes zero.

Thus, this application calls for an analog multiplexer having the speed and bandwidth of the ADG772, and it should operate as an MBB (make-before-break) type. At a switching rate of 60 MHz, the channels of such a multiplexer will conduct almost three times longer, and the difference in turn-on times of the A and B channels will be less significant. To prevent short overloading of amplifiers A_1 and A_2, you can place SMD resistors of about 20Ω to the outputs of A_1 and A_2 when using an MBB multiplexer. EDN

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2 "ADG772: CMOS Low Power Dual 2:1 Mux/Demux USB 2.0 (480 Mbps)/USB 1.1 (12 Mbps)," Analog Devices, 2007 to 2008, www.analog.com/en/switchesmultiplexers/analog-switches/adg772/products/product.html.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Triac tester allows for manual or automatic operation

Abel Raynus, Armatron International, Malden, MA

Triacs are bidirectional ac switches that can control loads with currents as high as 25A rms at voltages as high as 600V. They find wide use in motor-speed, heater, and incandescent-lamp controls. Logic triacs are especially attractive for microcontroller-driven devices. You can activate a triac directly from microcontroller-output ports because of the triac's trigger current of only 3 to 10 mA. As with any electronic device, triacs can have some internal problems that you can detect before using them in a design.

Figure 1 shows a simple and inexpensive test fixture that tests the L2004F31, L2004F61, L2004L1, and L4004V6TP triacs from Littelfuse (www.littelfuse.com), but you can use it to test any other leaded triac because all the standard packages, including TO-220AB, TO-202AB, TO-251, and IPak, have the same pin layout. An IC socket provides easy insertion of a triac under test. You can also apply this idea to SMDs (surface-mount devices), provided that you can find or create an appropriate test socket. Polarity switch S_1, a DPDT (double-pole/double-throw) device, lets you check conductivity in both directions. Trigger switch S_2, a momentary SPST (single-pole/single-throw) pushbutton device, activates the triac under test by connecting the gate (Pin 3) with MT_2 (Pin 2) through resistor R_2 (**Figure 1**).

The test takes less than 5 seconds and comprises four steps (**Table 1**). An LED indicates the result of each step to the test operator. A triac is good if

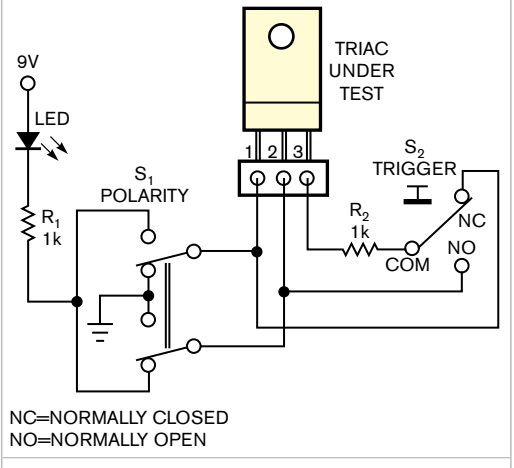

Figure 1 A triac tester uses a switch to reverse the polarity of the test signal.

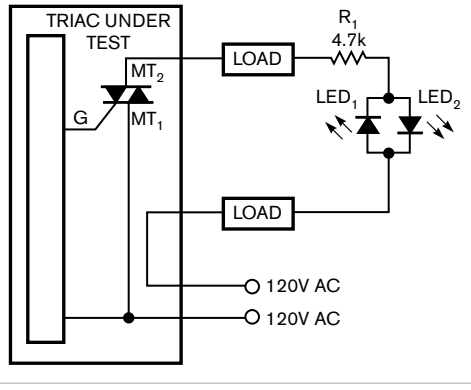

Figure 2 With a resistive load, the tester uses two LEDs to indicate pass and fail in both directions.

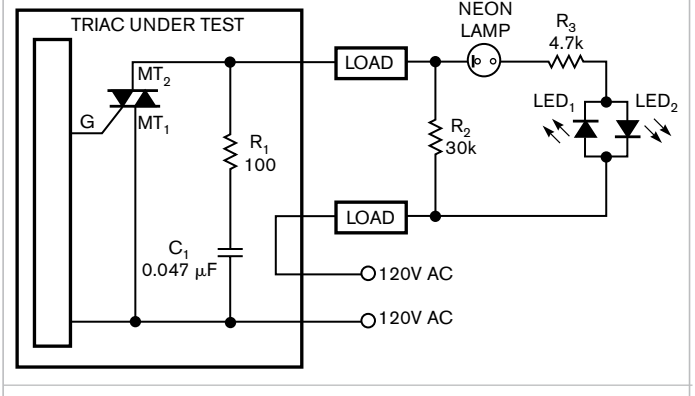

Figure 3 For an inductive load, add a neon lamp to minimize leakage current.

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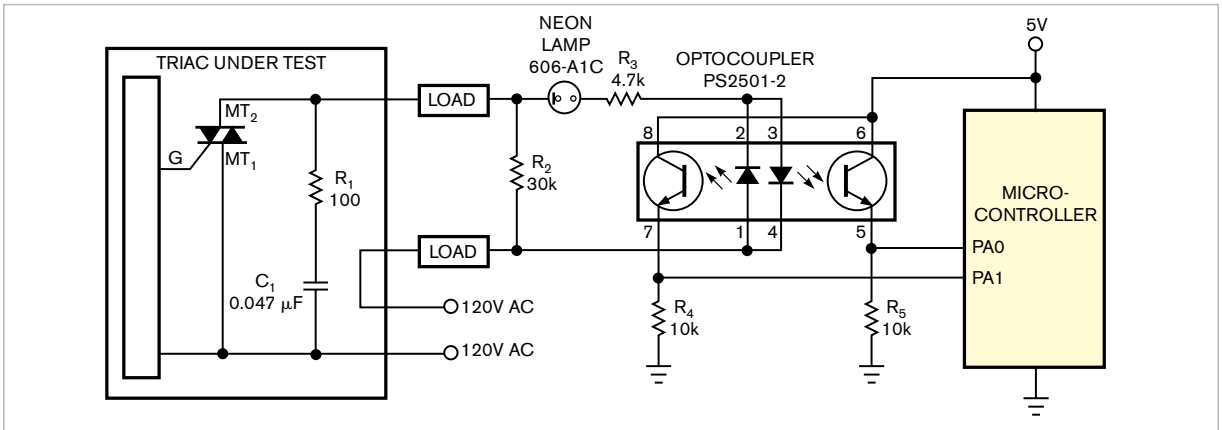

Figure 4 An optocoupler isolates the triac from ground.

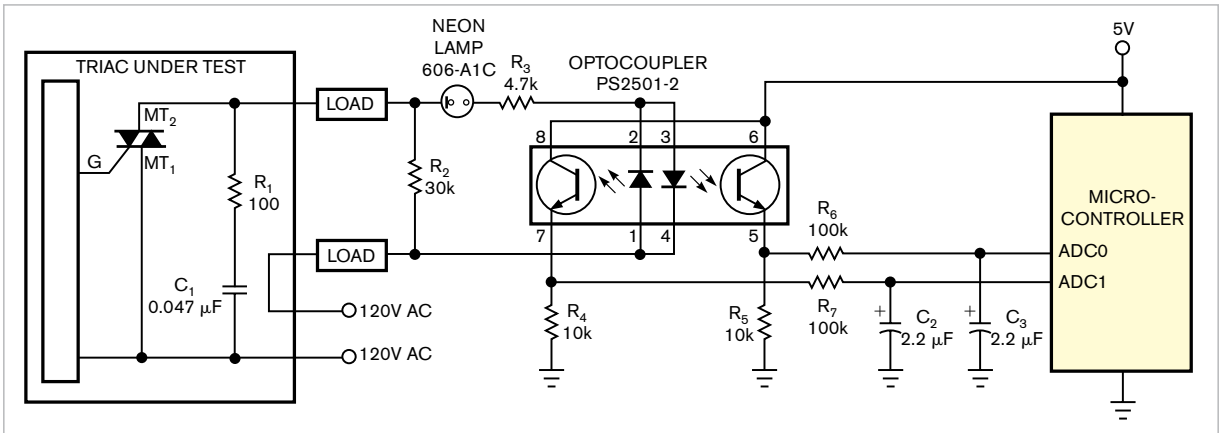

Figure 5 RC filters let you use PWM signals.

it passes all four tests. You should perform another triac test during manufacturing to ensure that there is no problem with the subassembly board and that the triac works properly. This test saves time and labor in case you detect a problem after assembling the entire product. You perform this test with the triac soldered into place on the board. You use the nominal power-supply voltage of 120/220V ac. The test should have minimal influence on the DUT and should use minimal time and labor. This test uses the triac tester in place of a load. The connection from the tester to the DUT can vary, and be sure to take some safety measures when connecting 120/220V ac.

You use a different test fixture for triacs that drive a resistive load, such as an incandescent lamp or a heater (**Figure 2**). Each LED checks conductivity in one direction. When the triac is closed, both LEDs should be off. When it is open, both LEDs should be on. In the case of an inductive load, such as a motor, use an RC snubber circuit comprising C_1 and R_1 in parallel with the triac (**Figure 3**). Unfortunately, the snubber circuit introduces a small current leakage into the test circuit even when the triac is closed. The circuit in **Figure 3** shows you how

TABLE 1 TEST FOR TRIACS

Step no.	Operations	LED status	Result
1	Insert triac under test into the socket; turn on power	Off	OK
		On	Shortage inside triac
2	Push and release trigger switch S_2	Off	Break inside triac
		Stays on	OK
		On but goes off after you release S_2	Bad "hold" function in triac
3	Move polarity switch S_1 into another position	Off	OK
		On	Shortage inside triac
4	Push and release trigger switch S_2	Off	Break inside triac
		On	OK
		On but goes off after you release S_2	Bad "hold" function in triac

to avoid this problem using resistor R_2 and a neon lamp with an ac breakdown voltage of 95V.

The indicators of the test result in **figures 1**, **2**, and **3** are LEDs. Sometimes, the triac test is part of a multitasking test system that checks other components or parameters of the whole device, which includes the triac. This test involves a sequence of measurements, and a system operator gets only one of two possible signals: pass or fail. These tests use a microcontroller-based system. Thus, all the interface signals should be in digital format: high or low.

You can also use analog signals by activating the microcontroller's ADCs. This approach is less preferable, however, because of the limited number of ADCs in low-end microcontrollers and more complicated software. Interfacing the triac under test with the microcontroller creates no problem if the triac's MT_1 pin is grounded. In most cases, MT_1 and MT_2 are isolated from the ground. When this scenario occurs, you can use an optocoupler, such as the PS2501-2 from California Eastern Laboratories (www.cel.com, **Figure 4**). It comprises two optically coupled isolators containing LEDs and NPN phototransistors with a maximum voltage of 80V.

If the triac output comprises a sequence of pulses, such as a PWM (pulse-width-modulated) signal for motor-speed or lamp-brightness control, then use a lowpass RC filter before the microcontroller's ADC inputs (**Figure 5**). The time constant of this filter, $\tau = R_6 \times C_2$, depends on the PWM signal period and duty cycle. The measurement in the chain of tests should start no earlier than $3-5\tau$. Using the microcontroller's ADC requires additional firmware. To avoid this requirement, you can compare the voltage after the filter with a reference voltage with a comparator, such as the LM393 from National Semiconductor (www.national.com), to produce a logic-high level for the microcontroller's input. **Reference 1** describes an alternative approach with minimal external components for the expense of the firmware complication. EDN

REFERENCE

1 Raynus, Abel, "Microcontroller detects pulses," *EDN*, July 24, 2008, pg 58, www.edn.com/article/CA6578137.

Handheld DMM copes with logic nanosecond-pulse-width waveforms

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When testing sequential-logic circuits, you may find that, although the repetition frequency of a logic signal is within the range of your DMM (digital multimeter), you can't measure it. The displayed frequency value is either dubious or chaotically changing in time. The DMM may also behave as if there were no signal. Any of these undesired states might appear when the duty cycle of the measured waveform is either close to zero or is approaching one—in other words, when the width of a pulse—high or low—is much narrower than the repetition period of these pulses. This problem occurs because you can't expect a DMM with an upper frequency limit of perhaps 200 kHz to measure 100-nsec-wide pulses, even if the repetition rate of these pulses is well below the upper limit of the DMM's frequency range—perhaps just 5 kHz. For a rough estimation of bandwidth for measuring at a pulse width of 100 nsec, consider this pulse to be a half-period of a square-wave signal. Use the following **equation** to calculate the required bandwidth:

$$B \approx \frac{1}{2T_W} = \frac{1}{2 \times 10^{-7}} = 5\ \text{MHz}.$$

This frequency is well beyond the bandwidth of most DMMs. The second cause of failing to measure the repetition rate of logic waveforms with too-low or too-high duty cycles lies in the internal ac coupling of the DMMs during frequency measuring. Due to this coupling, the decision threshold of an internal comparator, which you derive from the mean value of the measured waveform, is close to either the low or the high level of this waveform. In the case of narrow pulses, the operation of the internal comparator becomes ambiguous, and any noise in the measured waveform or that the comparator itself generates may cause an error.

You can address the problem by placing a binary divider between the source of a logic signal and the DMM. The binary divider comprises IC_1, a positive-edge-triggered, D-type flip-flop (**Figure 1**). The supply pin of IC_1 connects to the supply terminal of the tested logic

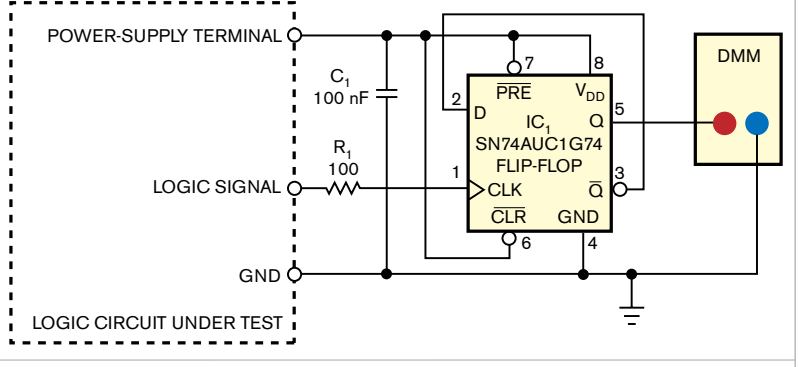

Figure 1 A binary divider turns low- or high-duty-cycle waveforms into square wave so that you can measure their frequencies.

circuit. Therefore, you can run the logic at any industry-standard supply voltage of 1.2, 1.5, 1.8, or 2.5V. In testing 3.3V logic, use an external 2.5V source to supply IC_1. The internal protective diodes at Pin 1 of IC_1, along with resistor R_1, reduce the voltage swing at Pin 1 to an acceptable level in such a case.

A square-wave signal is at the output of the binary divider (**Figure 2**). The DMM no longer sees nanosecond pulses at its measuring terminal. You have only to multiply the displayed frequency value by two to obtain the correct frequency. Due to relatively low values of R_1 and of the input capacitance, approximately 2.5 pF, at the clock input of the flip-flop, you need not worry about frequency compensation. The time constant of $R_1 \times C_{IN}$ is merely 0.25 nsec. The width of pulses—either low or high—at the input of the circuit can decrease to 1 nsec. EDN

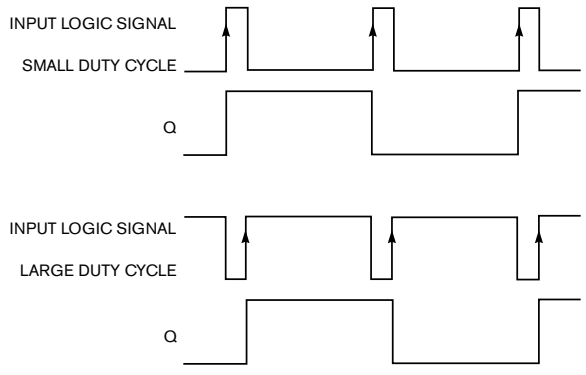

Figure 2 The flip-flop output, Q, produces a signal with a 50% duty cycle.

Build a simple complementary-bracket-pulse generator

Horst Koelzow, Global Thermoelectric, Calgary, AB, Canada

When building push-pull switching power converters or motor controllers, you often need alternating pulses with a small amount of dead time between them to minimize simultaneous conduction in output-switching devices. Switching controller ICs have this feature, but they usually operate within closed loops to minimize IC pin count. When optimizing switching output stages, you may need open-loop control. **Figure 1** shows how you can build such a generator with just two common ICs. As a bonus, both the overlapping, P-channel drive and the nonoverlapping, N-channel drive are available simultaneously.

The circuit's input, Pin 10 of IC_1, comes from clock generator IC_{2F}. A slightly delayed and inverted version occurs at IC_1's Pin 9 from IC_{2A}. IC_1 then decodes the original and delayed inputs to form the desired outputs (**Table 1**). Because IC_1 is an analog demultiplexer, you can set its outputs either active high or active low with pull-up or pull-down resistors. You determine the high or low inactive state by tying the X or Y pins to either the power-supply voltage or ground. Depending on the state of IC_{1A}'s A and B inputs, internal switches in IC_1 close between X and X0 to X and X3, as well as from Y and Y0 to Y and Y3. Buffers IC_{2B} through IC_{2E} buffer and invert the resulting outputs. You can use the remaining gate as a variable-frequency or variable-duty-cycle generator. You determine the dead time,

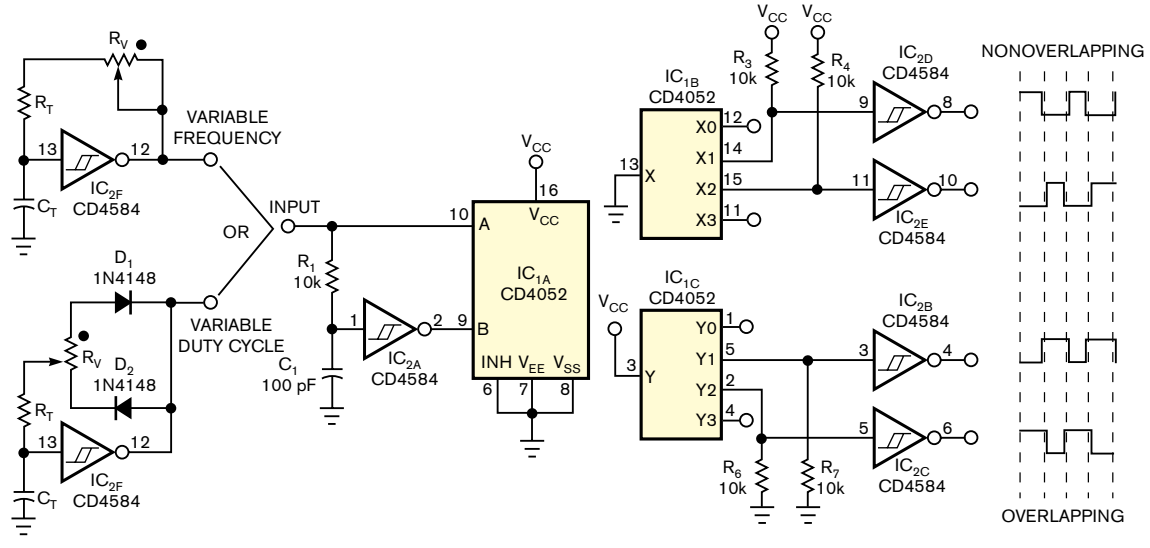

Figure 1 You can build a simple pulse generator with just two commonly available ICs.

which is independent of frequency or duty cycle, using the time constant of R_1 and C_1. Depending on output-device characteristics and switching frequency, output buffers may require an additional stage, or you can replace them with MOSFET-gate-driver devices. Supply voltage is not critical but should be high enough to guarantee that output devices fully turn on. In general, a higher supply voltage allows for higher-speed operation. The MC14xxx series of ICs is the same as the CD4xxx series. If you need higher-frequency operation at lower supply voltages, then use the 74HC4xxx-series devices. All of these ICs are available from a number of manufacturers, including Texas Instruments (www.ti.com, **Reference 1**) and On Semiconductor (www.onsemi.com, **Reference 2**). EDN

TABLE 1 ORIGINAL AND DELAYED INPUTS

Pin 9 (Input B)	Pin 10 (Input A)	Sequence
0	1	Phase A
1	1	Dead time
1	0	Phase B
0	0	Dead time

REFERENCES

1 "CD4051B, CD4052B, CD4053B," Texas Instruments, October 2003, http://focus.ti.com/lit/ds/symlink/cd4052b.pdf.

2 "Semiconductor and Integrated Circuit Devices," On Semiconductor, www.onsemi.com/pub_link/collateral/mc14584b-d.pdf.

Power-miserly voltage reference needs just one pin

Peter T Miller, Applied Inspirations LLC, Bethlehem, CT

The supply rail normally powers a microcontroller's voltage-reference source. In power-critical battery-operated applications, the constant drain, even of a few 10s of microamps, can be prohibitive. This situation requires adding a pin to turn the reference voltage on and off. By adding a 0.1-µF capacitor in parallel with the voltage reference and a simple bit of software that you can download from the online version of this Design Idea at www.edn.com/090820dia, you'll need just one pin to both power and read the reference voltage.

When you connect the voltage reference as in **Figure 1**, the software configures the Microchip (www.microchip.com) PIC chip's V_{REF} (reference-voltage) pin as a switched-on output. After approximately 300 µsec, the voltage across the capacitor stabilizes at 1.225V.

There is an initial overshoot when the ZXRE4041 powers up. The pin is then reconfigured as an analog input for the ADC's reference-voltage source. The reference voltage quickly drops by 20 mV in the next 50 µsec as the ZXRE4041 shuts down. With a 0.1-µF capacitor, the voltage then slowly drops 60 mV over 2 msec because of leakage. Although this delay is exponential, the rate is so slow that, for practical purposes, you can consider it linear for this short time window.

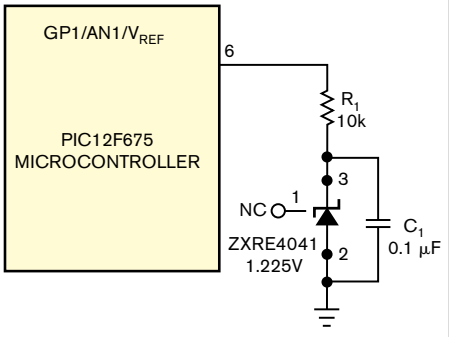

Figure 1 A voltage reference and a capacitor provide a reference voltage for a microcontroller.

You must also consider that the ADC also draws current through the 10-kΩ resistor during conversion, causing voltage drop. Although Microchip doesn't characterize this voltage drop in its documentation, tests consistently measured a drop of 80 mV for several devices, giving a calculated current of 6.67 µA. Using a conservative internal 4-MHz clock and allowing an ADC clock of frequency oscillation divided by 16 for operation at the minimum operating voltage, one conversion takes 45 µsec. This action slightly drains the capacitor, but this drainage appears to be only 2 or 3 mV. Calculations of initial watt-seconds minus watt-seconds used yield even lower values. Subtracting these fixed, repeatable losses from the initial steady-state 1.225V yields a new reference voltage of $1.225V_{REF}-0.020V$ shutdown drop -0.080 IR drop $=1.145V$.

Allowing 75 µsec to do the analog-to-digital conversion, store the value, and set up for the next conversion on another channel, 11 conversions will result in the last one's reference voltage being lower by 22.5 mV—that is, 10 conversions×75 µsec×(60 mV/2000 µsec). This error is only 1.9% compared with the first conversion's results.

If you just need an approximate voltage for a consumer product, for example, to warn of low battery voltage, you can use an LED instead of the ZXRE4041. Just change the value of R_1 to 300Ω to provide sufficient current to turn on the LED. Although LEDs lack the temperature stability of dedicated voltage-reference chips, the variation may be acceptable for the application because most consumer products find use within the comfort range of humans. If an LED is already part of the system, then the voltage-reference cost is only that of the software. Using this technique, an LED can now provide status-indicator, photodetector, and voltage-reference functions and enter a zero-power state using only software to reconfigure the changes. EDN

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READERS SOLVE DESIGN PROBLEMS

Turn a set/reset latch into an astable/monostable multivibrator

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

This Design Idea describes a simple way to form a reliable astable or monostable multivibrator from a set/reset latch. You may find it useful because it lets you minimize the number of standard digital ICs your design requires when absolute precision isn't an issue. You can use a set/reset latch either with active-low or active-high inputs, which you can build with two NAND or NOR logic gates. You can also use integrated set/reset latches or any type of flip-flop that comes with asynchronous preset and clear inputs because they have the same function as the set/reset inputs when the clock and data inputs are grounded. This method functions only with CMOS-logic families that offer the benefits of high input impedance; a quasi-ideal voltage-transfer characteristic with a threshold voltage, V_{TH}, typically equal to the drain-to-drain voltage, V_{DD}, divided by two; and low power consumption. This concept has undergone testing with a 74HC00 quad NAND, a 74HC02 quad NOR, a CD4001 quad NOR, a CD4011 quad NAND, and a CD4013 dual-D-type flip-flop.

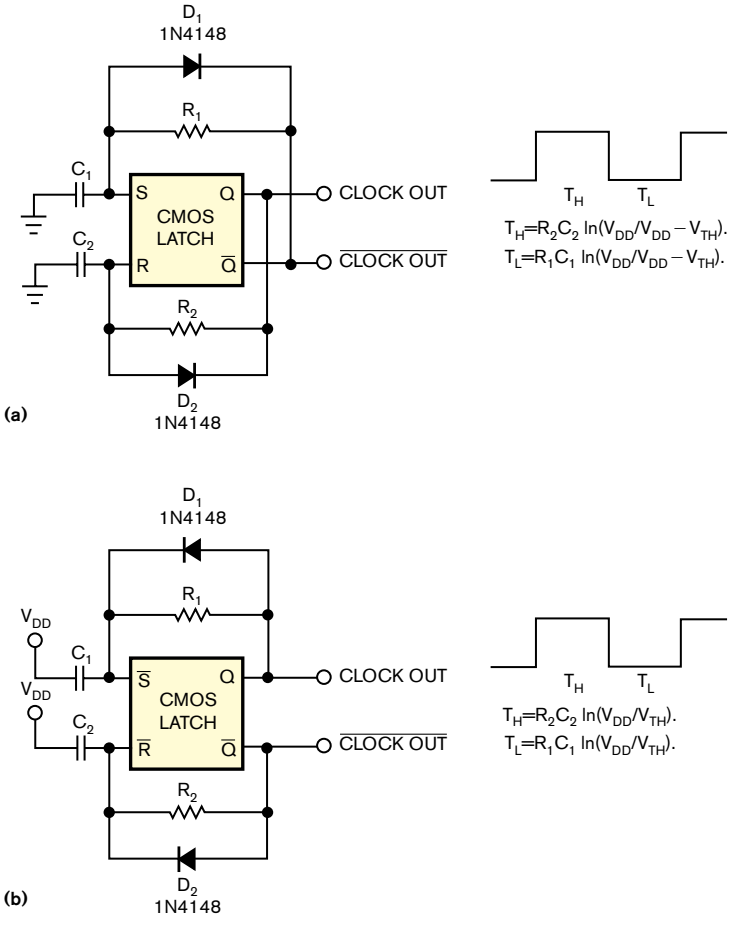

Figure 1 Capacitors that connect to ground or V_{DD} depend on active-high (a) or active-low (b) inputs.

Connecting two RC networks between the complementary outputs Q and $\overline{Q}$ and set and reset inputs enables astable operation (**Figure 1**). Due to complementary outputs, the circuit has no stable state, and it toggles continuously, generating an output clock. The time constants R_2C_2 and R_1C_1 set the high and low time periods, T_H and T_L, respectively, and also the duty cycle. Diodes D_1 and D_2 quickly discharge capacitors C_1 and C_2 so that, on the next

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cycle, they will recharge from 0V.

In monostable mode, connect one RC network (**Figure 2**), depending whether you need a positive-pulse or a negative-pulse trigger. When an input trigger pulse occurs, it sets the output pulse, T_W, which remains in this state until the RC network activates the reset pin. The RC time constant sets the output-pulse width. For correct operation, the trigger pulse must be shorter than the output pulse. Diode D_1 reduces recovery time.

The threshold voltage has the typical value $V_{DD}/2$, but it may change from 0.33 to 0.67 of V_{DD} for the CD4000 CMOS family. The parameters of the generated output signals of the circuits in **figures 1** and **2** present variations from unit to unit as a function of threshold-voltage shift. On the other hand, the threshold voltage presents good stability with supply voltage and temperature variations.

For best accuracy, the timing capacitors for both astable and monostable circuits should be nonpolarized, have low leakage, and be much larger than the inherent stray capacitance in the circuit, and the timing resistors for both astable and monostable circuits must be much larger than the CMOS on-resistance in series with them, which typically is hundreds of ohms. In addition, you must decouple the supply voltage for safety to prevent voltage spikes, which may disturb the circuits. EDN

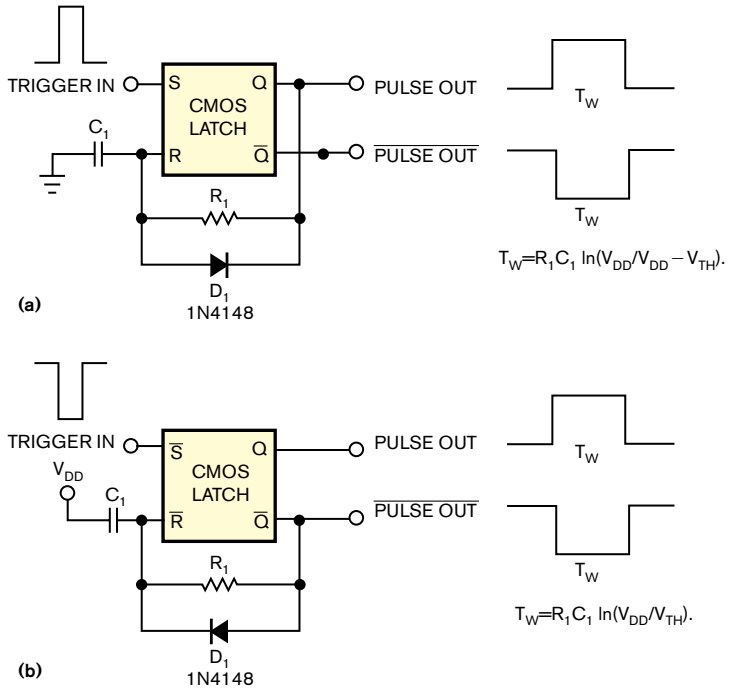

Figure 2 The leading edge of the trigger pulse depends on active-high (a) or active-low (b) inputs.

555 timer eliminates LED driver's need for microprocessor control

Michael Day, Texas Instruments, Dallas, TX

LEDs find their way into applications that range from high-end video displays to low-end lighting applications. Designers often need only some of the functions of a dedicated LED driver but can't afford the cost

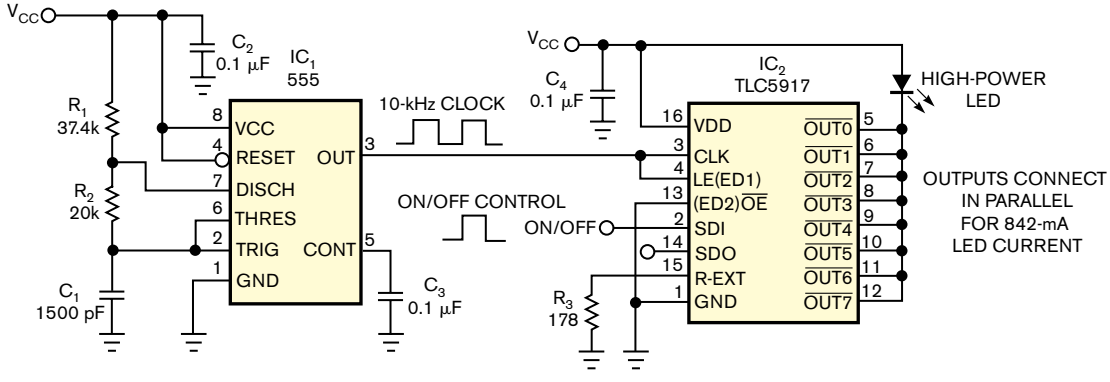

Figure 1 A 555 timer provides the necessary pulses for configuring an LED driver.

of the microprocessor to control them. Microprocessors typically control dedicated LED drivers, enabling features such as analog or PWM (pulse-width modulation) for LED-current control, independent control of each LED, and reading LED status and faults. If your design requires a constant-current LED, such as those in LED lighting or luminaires, then you may not need these advanced features. In these applications, a 555 timer can replace the microprocessor and still allow accurate control of LED current independently of input voltage, temperature, and LED forward-voltage drops.

IC_2, a TLC5917 dedicated LED driver, controls eight independent constant-current sinks (**Figure 1**). It normally requires a microprocessor to drive four digital-input signals. The command $\overline{OE}$ (output enable) enables and disables the IC. Data on the SDI (serial-data-input) pin clocks into the IC's input shift registers on the rising edge of the clock. The data in the shift registers transfers into internal on/off latches on the falling edge of the LE (latch).

Either the TLC5917 outputs can drive eight independent LEDs, or you can parallel its outputs to increase the current to drive one higher-power LED. Its internal current-setting registers have default values at start-up. These values, along with external current-setting resistor R_3, set the LED current. In this application, R_3 sets each output's current to 105 mA: $18.75V/R_3=18.75A/178\Omega$. Connecting all outputs in parallel yields 842 mA of LED current.

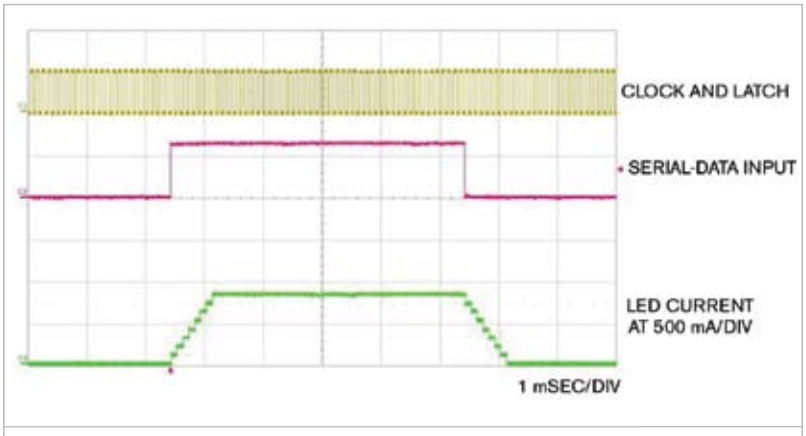

Figure 2 The LED current (lower trace) ramps up and down in eight steps.

At power-up, the internal on/off latches that turn each output on or off default to zero, so you must set these latches to one before the outputs turn on. The 555 timer replaces the microprocessor for this function. The clock and latch lines both connect to the 555 timer's square-wave output. At each rising edge of the clock, the SDI shifts into the TLC5917's input shift register. This data latches into the on/off latch at the falling edge of the latch signal. Because shifting the data and latching the data occur at different clock edges, the clock and latch pins can connect to the same input clock signal. Hard-wiring $\overline{OE}$ to ground permanently enables the IC. You can connect SDI to the power-supply voltage to automatically turn on the LED at power-up. This connection continuously clocks in ones to turn on all outputs. You can also connect SDI to a switch or a digital input to allow for LED on/off control. Then, SDI can pull to the power-supply voltage, which continuously clocks in all ones to turn on the outputs. Alternatively, it can pull to ground, which continuously clocks in all zeros to turn off the outputs.

The 555 timer's clock speed determines how fast the LEDs turn on and off. The LED current ramps from 0 to 100% in eight clock pulses as each falling edge of the latch pin latches the SDI data into another of the eight internal on/off latches, turning on or off another one of the eight outputs. **Figure 2** shows the resulting stair-stepped LED current increasing and decreasing with each successive falling edge of the latch. Even a relatively low clock speed of 10 kHz results in an off/on and on/off transition of only 0.8 msec, which the human eye perceives as instantaneous. You can achieve gradual turn-on and turn-off with low clock speeds. Setting the clock to 0.1 Hz gradually turns the LED on and off in 0.8 sec. EDN

Smart photoresistor timer needs few components

Abel Raynus, Armatron International Inc, Malden, MA

An application required a photo timer with some unusual functions. It had to switch on the load, a lamp, an hour after sunset. After working for three hours, the timer should turn the load off, which had to remain off until an operator manually reactivated the timer. The timer had to reside between the main 110/220V-ac line and the load. And, as with any other consumer product, it had to be cost-effective. You can achieve these goals by using a voltage comparator and dual timers with an RC-timing network, but an inexpensive, 8-bit microcontroller with a built-in ADC provides a more elegant approach. You can perform all the functions in firmware. **Listing 1**, which is available at www.edn.com/090903dia, contains downloadable source code.

Figure 1 shows the circuit, which uses an eight-pin MC68HC908QT2 microcontroller from Freescale Semi-

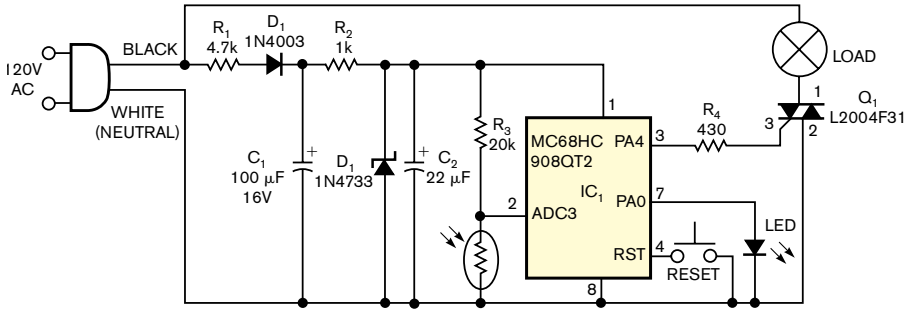

Figure 1 This circuit uses an eight-pin microcontroller and a logic switch to provide a smart photoresistor.

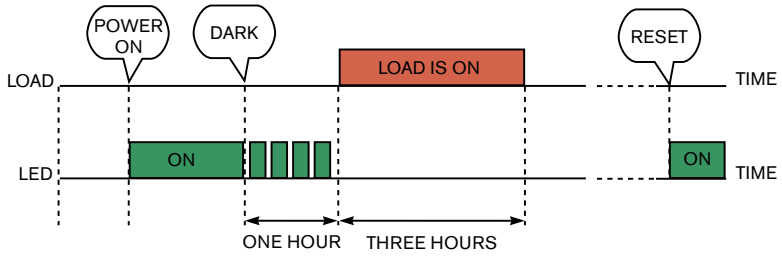

Figure 2 The LED is on when the timer is ready for work and waits for darkness. It blinks during the delay, and it is off when the timer waits for reactivation.

conductor (www.freescale.com). **Reference 1** describes a microcontroller's power supply. Q_1, an L2004F31 logic triac from Littelfuse (www.littelfuse.com), switches the load on and off; the type you use depends only on the load current and main voltage. The L2004F31 requires only 3 mA of dc-gate-trigger current, and it conducts 4A rms at 200V ac. The VT90N1 photoresistor from PerkinElmer (www.optoelectronics.perkinelmer.com) has a dark resistance of 200 kΩ, which drops in light to 10 kΩ or less. The LED indicates the status of the timer: It is on when the timer is ready for work and waits for darkness. It blinks during the delay, and it is off when the timer waits for reactivation (**Figure 2**). The W934GD5V LED from Kingbright (www.kingbright.com) has a built-in resistor that minimizes the number of necessary components. To reactivate the timer, press the pushbutton reset switch. All time delays are set in firmware, and you can easily change them. EDN

REFERENCE

1 Raynus, Abel, "AC line powers microcontroller-based fan-speed regulator," *EDN*, Nov 9, 2006, pg 128, www.edn.com/article/CA6387025.

High-performance adder uses instrumentation amplifiers

Moshe Gerstenhaber and Michael O'Sullivan,
Analog Devices, Wilmington, MA

As instrumentation amplifiers become less costly, they can provide improved performance in applications that operational amplifiers traditionally served. The op-amp adder in **Figure 1** has a few shortcomings. First, the inputs have low to medium input impedance, which the input resistor of each signal determines. This arrangement causes gain errors when the source impedance of the driving signal is large or requires the design of low-impedance driving sources. This circuit also has no common-mode-rejection capability, so inputs must be single-ended. The channel with the largest gain limits the performance of the entire system. Higher gain on one channel results in lower bandwidth, higher distortion, and increased system noise on all channels. To limit these effects, even low-performance adders require high-performance, high-bandwidth op amps.

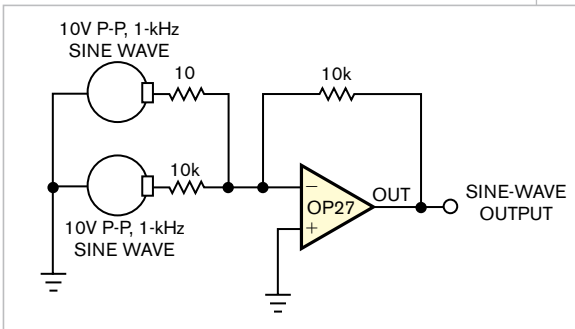

Figure 1 A typical adder configuration uses a single op amp.

The noise gain of this op-amp adder is $1+10{,}000/(10||10{,}000)$. The input signal with the highest gain and 10Ω input dominates the noise gain, but all inputs suffer increased offset voltage, gain error, noise,

and distortion. You can increase input impedance and improve common-mode rejection by using instrumentation amplifiers. The output voltage of an instrumentation amplifier is proportional to the voltage difference between the positive and the negative inputs. You can amplify this signal by connecting a resistor, R_{GAIN}, to the R_G pins (**Figure 2**). The output voltage is generated between the reference pin and the output pin. This arrangement allows you to use the reference pin to cascade multiple signals together in an adder configuration. You can set each instrumentation amplifier to a different gain.

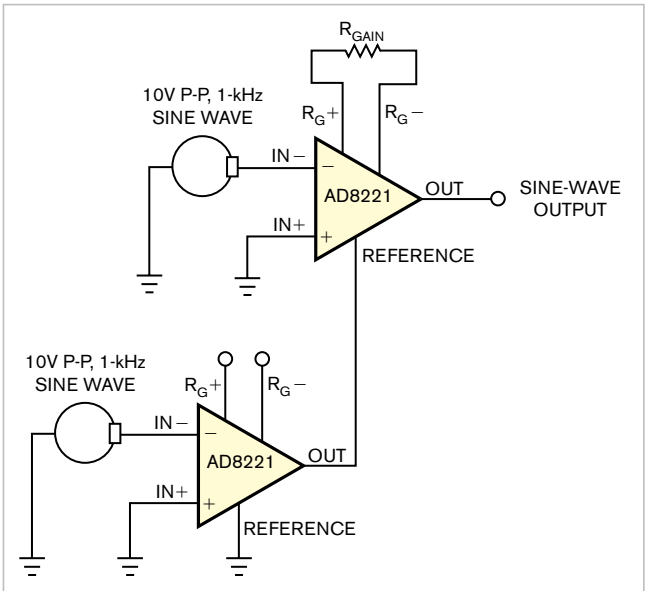

Figure 2 Two instrumentation amplifiers provide increased input impedance in this adder circuit.

This system has several advantages over the simple op-amp adder. For example, each input has extremely high input impedance and has independent common-mode rejection, which the instrumentation amp connected to that channel determines. The higher the channel gain, the higher the common-mode rejection, and the smaller the resulting error. You can also easily add or subtract signals by using the inverting or noninverting terminals of the instrumentation amplifier, and the amplifier enables the use of differential input signals if you wish. Further, the distortion, noise gain, and bandwidth of each signal are independent of the other signals, leading to lower offset voltage, gain error, noise, and distortion. **Figure 3**'s THD+N (total-harmonic-distortion-plus-noise) plot demonstrates five times less distortion for the instrumentation-amplifier adder than that of the op-amp adder, even though the instrumentation amplifier has 1-MHz bandwidth and operates at 1 mA, whereas the op amp has 8-MHz bandwidth and operates at 4.5 mA. EDN

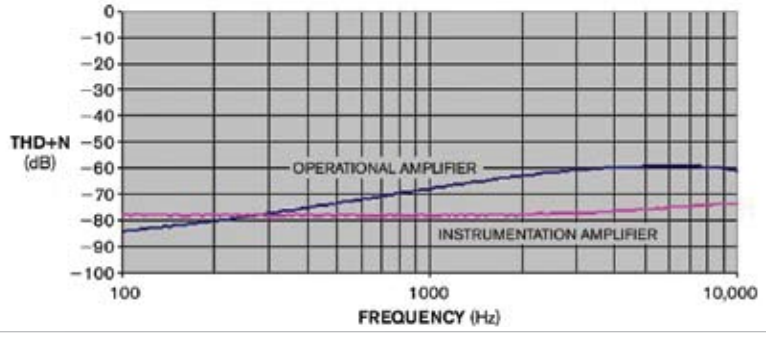

Figure 3 The instrumentation-amplifier configuration shows improved THD+N at frequencies greater than 300 Hz.

Nonvolatile standby/on switch remembers its state

Anatoly Andrusevich, Maxim Integrated Products Inc, Moscow

You can use the standby/on switch in **Figure 1** for industrial or telecom applications in which the circuitry must somehow "remember" its state—standby or on—after a power failure that occurs when no operator is present. An alternative approach uses a battery or a supercapacitor and a flip-flop. This approach is less reliable, however, because the circuit can lose its state if leakage current drains the battery. Another alternative involves the use of a microcontroller and EEPROM, but that approach requires software plus a provision for start-up time. Also, a stand-alone EEPROM for this application has an awkward interface.

You can use an electronically programmable voltage reference, IC_4, as a single-bit nonvolatile-memory cell. To remember the state of the standby/on switch, this circuit programs IC_4's output voltage high or low and can reprogram it at least 50,000 times. IC_1 is a low-dropout linear regulator with reset output and a wide input-voltage range that extends to 72V. A microprocessor supervisor, IC_2, debounces the standby/on pushbutton and supports the programming of IC_4 by increasing the pause length between pulses. IC_4's output drives IC_5, an inverter with Schmitt-trigger input, which in turn drives the gate of transistor Q_2 to control the main power supply.

Flip-flop IC_3 helps to change the standby/on state with each press of the control button. At the end of IC_4's programming cycle, a low-to-high edge at IC_3's clock input sets the flip-flop to its opposite state, thanks to the feedback from the inverter. IC_2's reset triggers this action at power-up to ensure that the switch is ready to change state. Transistor Q_{1B} and IC_1's reset output prevent the programming of incorrect states by blocking IC_4's adjust input during start-up and power-fail conditions.

You must block the effect of IC_2's power-up or -down reset pulse on IC_4's adjust input; C_2 therefore sets IC_1's reset time-out to be longer than IC_2's reset time-out. The threshold voltage of IC_2, 2.9V, is also lower than that of IC_1, 4.6V. The worst-case 1.32V input-threshold voltage of IC_5 guarantees the standby position at first power-on because the factory-preset output for IC_4 is only 1.2V. EDN

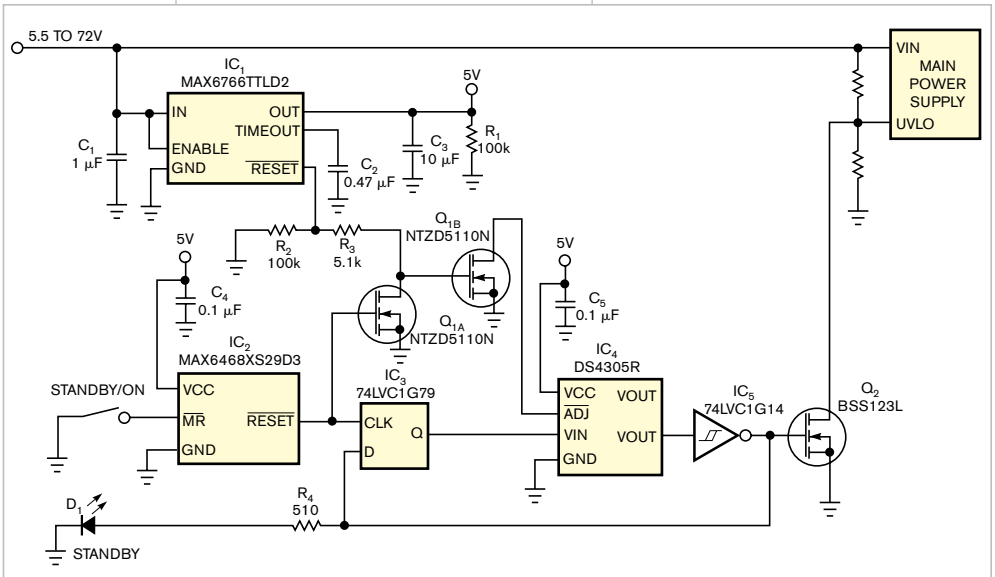

Figure 1 The circuit remembers its standby or on state if power fails with no operator present.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Missing pulse detects position or produces a delay

Michael C Page, Chelmsford, MA

Consider an application that needs a series of pulses to indicate position in which the lack of a pulse "indexes" the count. To achieve that goal, the application uses a rotating, 36-tooth sprocket with one missing tooth. Rotational speed ranges from 500 to 7000 rpm. The mechanism uses an inductive pickup to sense the sprocket's teeth. With one of the sprocket's 36 teeth missing, the detector senses 35 pulses, and then a pulse disappears.

Unfortunately, the mechanism frequently breaks down or simply breaks apart. Because the application uses this wheel just to trick the computer by simulating an operating engine, the application's designers replaced the rotating gear with a simulator circuit (**Figure 1**). Given the rotational speed and number of teeth, the maximum pulse frequency is 7000/60×36, or 4200 Hz. The circuit works well from single stepping to more than 1 MHz before starting to break down. The maximum frequency depends on the logic family and construction methods you use.

Figures 2 and **3** show the outputs running at 100 Hz and 1 MHz, respectively. At power-up, capacitor C_1 remains the same, which forces RST on

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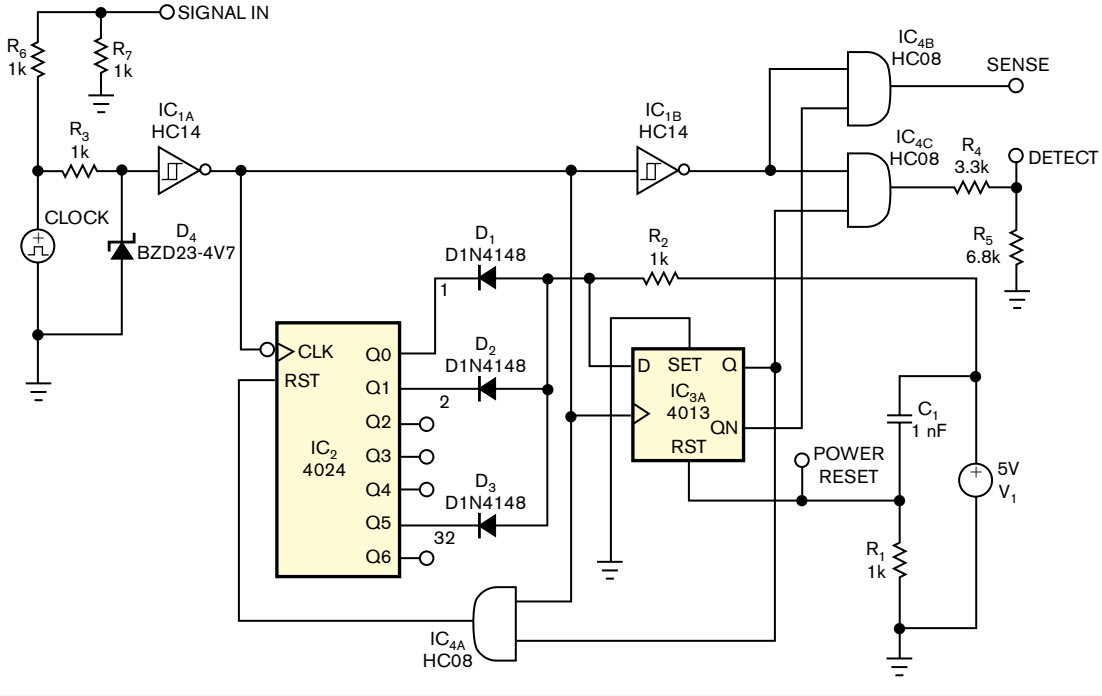

Figure 1 IC_2 combines with three diodes to produce a stream of 36 pulses before resetting.

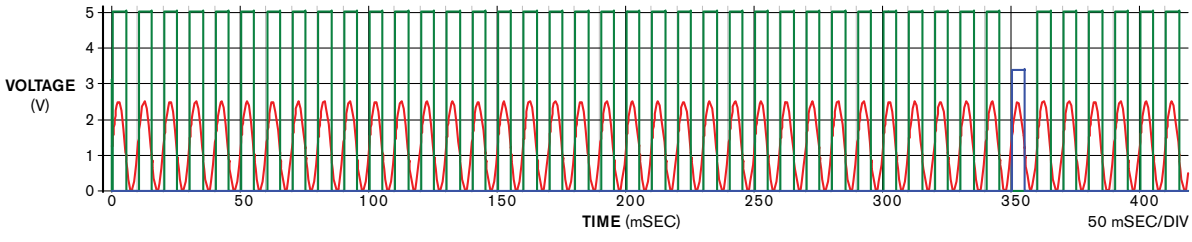

Figure 2 Operating at 100 Hz, the circuit signals include the clock-sine-wave signal (red), the sense-square-wave signal (green), and the detect signal (blue), which indicates the missing pulse.

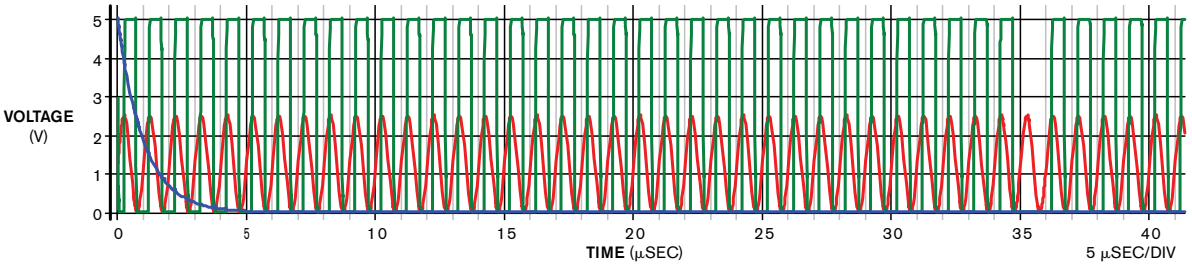

Figure 3 The pulse train at a clock frequency of 1 MHz still shows the missing 36th pulse along with the power-reset signal (blue).

IC_{3A} low. That action puts the D flip-flop into a known state. As C_1 charges through R_1, the voltage at the power reset falls, letting clock pulses set IC_{3A}'s outputs. You must keep the small value for the C_1/R_1 combination if you use a high input frequency with a low count rate. As **Figure 3** shows, the desired count must exceed the duration of the power reset. The values in **Figure 1** provide a time of approximately 0.66×1 kΩ (the value of R_1)×1 nF (the value of C_1), or 0.66 µsec, leaving a minimum count of approximately three at 1 MHz.

For the clock signal, the circuit uses a sine-wave signal with an amplitude of 5 to 10V from the system. The clock signal goes through R_3 to D_4 and IC_{1A} to produce a 5V square-wave signal. The signal goes to counter IC_2 and to one input of AND gate IC_{4B}. With the other input of IC_{4B} coming from IC_{3A}'s QN output, which is high from power reset at start-up, the input-pulse train passes through IC_{4B}, which simulates sprocket teeth at the sensor. Resistors R_6 and R_7 halve the clock-signal amplitude just to make the graphics clear at "signal in." Diodes D_1, D_2, and D_3 pull up to 5V through R_2 and form an AND gate to select the desired count. Counter IC_2's outputs are binary, so, for a 36-tooth sprocket with one missing tooth, outputs Q0, Q1, and Q5 correspond to 1+2+32=35.

You can produce any count as high as 128 by adding the appropriate diodes on the Q outputs on IC_2. In other words, you need to generate one missing pulse of 36 to simulate the 36-tooth sprocket. Thus, you select a count of 35; the circuit automatically adds a count of one due to the one-clock delay of the counter. Because you reset IC_2 at power-up, all outputs are low, keeping the D input of IC_{3A} low, with a count of zero.

THE CIRCUIT AUTOMATICALLY ADDS A COUNT OF ONE DUE TO THE ONE-CLOCK DELAY OF THE COUNTER.

As clock pulses continue into IC_2 and when outputs Q0, Q1, and Q5 are all high, with a count of 35, IC_{3A}'s D pin pulls high through R_2. On the next clock pulse, the Q output of IC_{3A} goes high and the QN output goes low, stopping the pulses from passing through IC_{4B}. This action indicates the missing tooth and produces the sense condition (the missing pulses in **figures 2** and **3**). Meanwhile, the Q output of IC_{3A}'s output goes high, yielding a single detect pulse at IC_{4C} through R_4 and R_5. On the next clock pulse, with IC_{3A}'s Q output high, IC_2 resets logic zero and is ready for the next count cycle. R_4 and R_5 halve the clock signal just to make the graphics clear at "detect."

The 4024 is an eight-stage binary-ripple counter. You can replace it with a 4040 counter to achieve a count of 2048, and you can cascade counters to get longer counts or delays. The 4040's pinout differs from that of the 4024, but their operation is identical. Some systems have an extra tooth instead of a missing tooth, and some have multiple missing teeth at odd locations around the sprocket, all waiting for replacement by this simple circuit. EDN

Emulate SPI signals with a digital-I/O card

Andy Street, Autoliv Electronics, Lowell, MA

A design-verification tester for millimeter-wave SOC (system-on-chip) devices needed to combine switching, electrical measurements, temperature measurement, a parallel-digital interface, and a serial-digital interface into one instrument. To minimize rack space, the circuit uses an Agilent Technologies (www.agilent.com) 34980A multifunction mainframe because its plug-in cards could support a force/sense dc matrix and multiplexed temperature measurements. The addition of an Agilent 34950A 64-bit digital-I/O card formed the basis of a system that could provide both an SPI (serial-peripheral-interface) bus and a simple parallel bus. The 34950A groups its I/O lines into two banks of four 8-bit channels. It provides 64 kbytes of memory per bank for pattern generation or signal capture. It also has three I/O lines per bank for handshaking.

YOU CAN STORE A MAXIMUM OF 32 TRACES IN THE PATTERN RAM PER BANK.

However, the card's handshake lines provide insufficient control for implementing SPI transactions. To get adequate control, you can emulate the SPI bus using three of the data-I/O lines.

Motorola (www.motorola.com) microcontrollers first used the SPI master-slave protocol. Today, it's become the control interface in a variety of ICs, including PLLs (phase-locked loops) and RF ASICs (**references 1** and **2**). The SPI bus uses the clock, SS (slave-select), MOSI (master-out/slave-in), and MISO (master-in/slave-out) lines. The clock line is a signal from the master to the slave. All SPI signals are synchronous with this clock. The SS line selects the slave for communication. The SPI specification defines four modes of operation, which effectively specify the clock edges for toggling and sampling and the clock-idle level. The specification makes no requirements on voltage levels or data rates, and many SPI implementations can clock in excess of 10 MHz. **Figure 1** shows a block and timing diagram of the 34950A's Bank 1, configured for synchronous, buffered output. H0 through H2 denote the handshake lines. The **figure** also shows an 8-bit SPI transaction for reference.

You cannot use the 34950A's handshake lines to emulate all modes of the SPI bus because the bus latches data on the falling edge of the clock, making the bus unsuitable for slaves that use the rising edge. Inverting the clock polarity is not a solution because you may lose the last data bit. Furthermore, if you write a number of transactions to a slave, you must store each transaction as a separate trace memory in the 34950A. Although each bank supports 64k×8 bits, you can store a maximum of 32 traces in the pattern RAM per bank, thereby limiting the number of SPI transactions. In addition, the card lacks a sequencer, so you cannot download a number of bit patterns and then play them in sequence. You must load each pattern into the I/O card's memory and then play each pattern under SCPI (standard commands for programmable instruments) from a host computer, slowing transactions.

Instead of using the handshake lines, this solution uses three da-

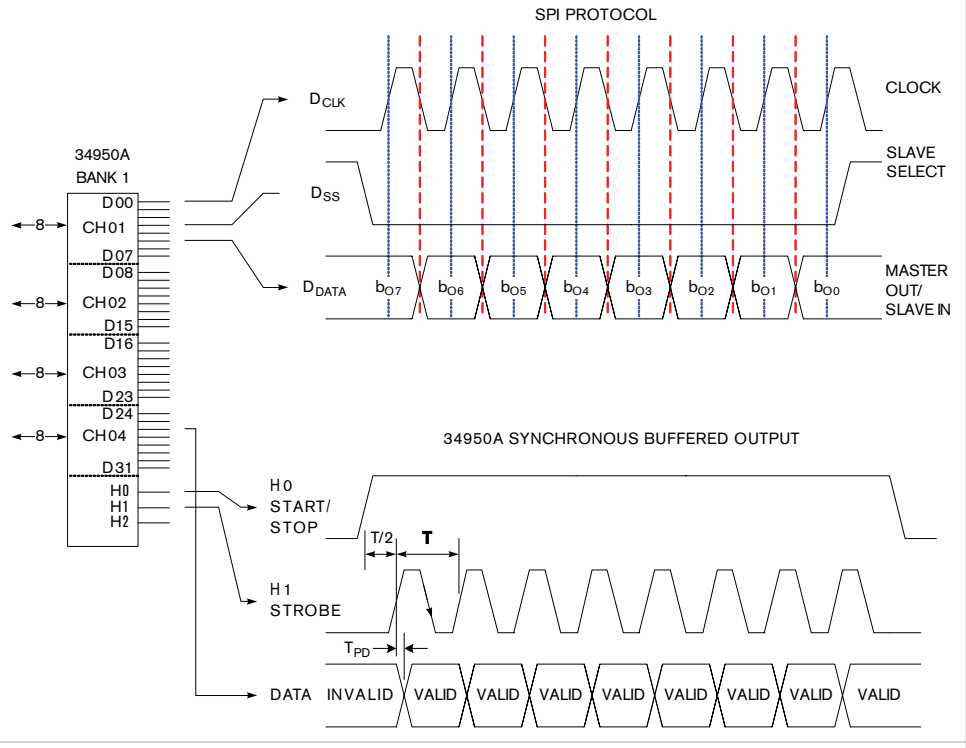

Figure 1 The 34950A synchronous buffered output uses the falling edge, making it unsuited to rising-edge SPI implementations.

ta-I/O lines to emulate the SPI clock, SS, and MOSI. The software driver for the I/O cards then has the responsibility of translating the data to be sent into an SPI-compatible bit stream. **Listing 1**, which is available at www.edn.com/090917dia, contains the algorithm in pseudocode, which translates a hexadecimal string, DH, of characters to an SPI signal. LD, LSS, and LCLK are integers to define which data outputs represent the MOSI, CLK, and SS, respectively.

Assuming a 24-bit register write with two bits of overhead for the SS prefix and postfix, the 64-kbyte memory can support more than 1000 SPI transactions. The approach has two additional advantages: The three lines that form the SPI bus are under software control, which provides cabling flexibility, and the implementation can support multiple slaves through the use of additional SS lines. **Figure 2** shows an MSO (mixed-signal-oscilloscope) screen that shows the SPI transaction. The SPI clock rate is 5 MHz, which the 34950A's internal 10-MHz clock limits. The different payload sizes correspond to writing data to 16- and 24-bit registers within the slave. EDN

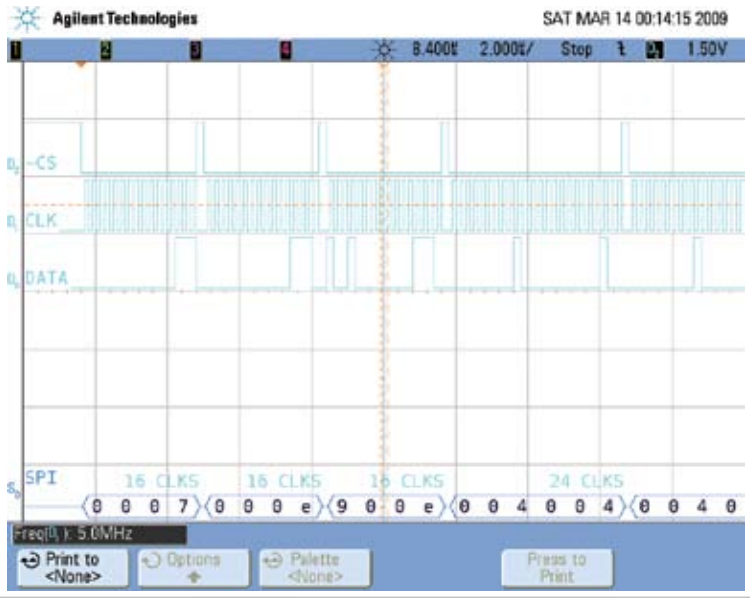

Figure 2 An MSO screen shows the SPI transactions using the digital-I/O lines.

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Resistive DAC and op amp form hybrid divider

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

A resistive DAC in a resistive-feedback loop of an op amp lets you create an analog-digital-analog divider. The resistance, R_{WA}, between the W and A terminals of the Analog Devices (www.analog.com) AD5293 (**Figure 1**) decreases linearly with increasing the digital-control data, D:

$$R_{WA}(D) = \frac{1024-D}{1024} \times R_{AB},$$

and the value of the R_{WB}, the resistance between the W and B terminals of the DAC, rises proportionally to D as

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB}.$$

R_{AB} is a constant value of resistance between the ends of the digital potentiometer. The circuit uses resistance R_{WA} as a feedback resistor, and resistance R_{WB} connects between the inverting input of the op amp and ground. The voltage gain of the noninverting amplifier becomes

$$A_V = 1 + \frac{R_{WA}}{R_{WB}} = \frac{1024}{D}.$$

The output voltage is

$$V_{OUT} = V_{IN} \times \frac{1024}{D}.$$

Both the input voltage and the digital-input data can be time variables, and the clock frequency for fetching digital-input data can be as high as 50 MHz.

The potentiometer's data sheet provides the ground-referred parasitic capacitances at the A, B, and W terminals of the potentiometer. Thorough measurement of the capacitances at these terminals provides enough data to determine capacitances between the terminals. An evaluation of the measured data shows that the direct capacitance between the A and W terminals at the midscale position of the wiper is just 2.4 pF:

$$C_{AW}(X = ½) \approx 2.4 \text{ pF}.$$

If you assume that the five segments of the potentiometer are ordered topologically into a chain, then the direct intercapacitance between the A and B ends of potentiometer is

$$C_{AB}(X = ½) \approx ½C_{AW}(X = ½) \approx 1.2 \text{ pF}.$$

The capacitance per segment of the five segments of the potentiometer is

$$C_{SEGM} \simeq 5C_{AB}(X = ½) \simeq 6\ pF,$$

where X=½ denotes the midscale of the resistive DAC.

The five-step distributed RC line of the potentiometer has a time constant of

$$\tau_{SEGM} = \frac{R_{AB}}{5} \times C_{SEGM} = R_{AB} \times C_{AB} = 24\ NSEC,$$

where R_{AB} is 20 kΩ. The ground-referred wiper capacitance, C_W, of 40 pF is much higher than the intercapacitances and creates a time constant:

$$\tau_W \simeq R_{WB} \times C_W.$$

The feedback network of the amplifier is frequency-compensated for $\tau_{SEGM} \simeq \tau_W$. Thus, you can calculate the value of R_{WB} as 600Ω, meaning that the voltage gain of the amplifier, A_v, is 32.3. For gains higher than 32.3, the effect of C_W becomes negligible, and you need not bother about amplifier stability. To suppress the derivative behavior of the amplifier for gain values of two to 32.3, you can add a 40-pF compensating capacitor in parallel to feed back part of the potentiometer. The amplifier thus has an integrating character for all gains down to a value of two.

You fetch the divisor, Y, which is a digital-data word, D, through a standard SPI (serial-peripheral interface). After power-on, you must initially neutralize the write-in protection of the resistive DAC. You have to first program the control bit C_1 to the value of one, whereas it is zero by default. You achieve this task by clocking in the word containing C_3, C_2, C_1, and C_0, which equals 0110, and you put the desired C_2 and C_1 values at data positions D_2 and D_1. After performing these steps, you change the wiper position in which the control bit is C_3, C_2, C_1, and C_0, which equals 0001, and the data bits, D_9 to D_0, represent the gain as 1024/D. EDN

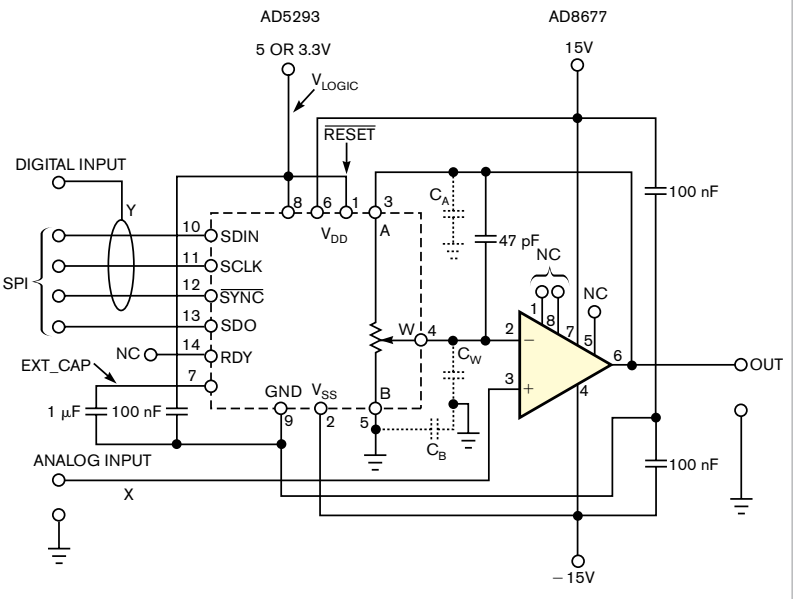

Figure 1 The resistive DAC-potentiometer forming the feedback for an op amp controls the op amp's gain as inversely proportional to the digital-input-data word. The circuit thus becomes a two-quadrant divider.

Connect two buttons with just two wires

Fikret Yilmaz, Mobil Elektronik, Istanbul, Turkey

Sometimes, you need to read the status of pushbuttons that are as much as 5m away from your electronic circuit. That task is easy if you have just one button. You simply design a constant-current source, connect the current line from your button, and measure the current in the line. If you press the button, current flows through it. Otherwise, current does not flow.

Problems occur, however, when you need to read two or more buttons. Several approaches to this problem are available. For example, you could use an RS-485 interface with two wires for communication and two for power. Alternatively, you could use a single-wire connection

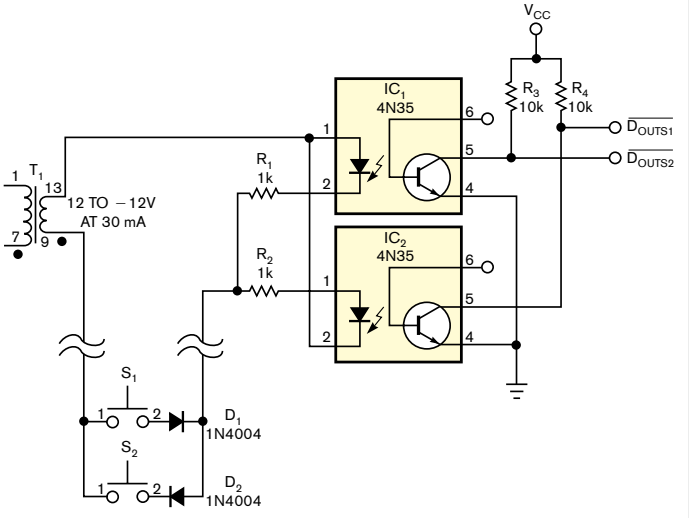

Figure 1 You can connect two buttons using diodes.

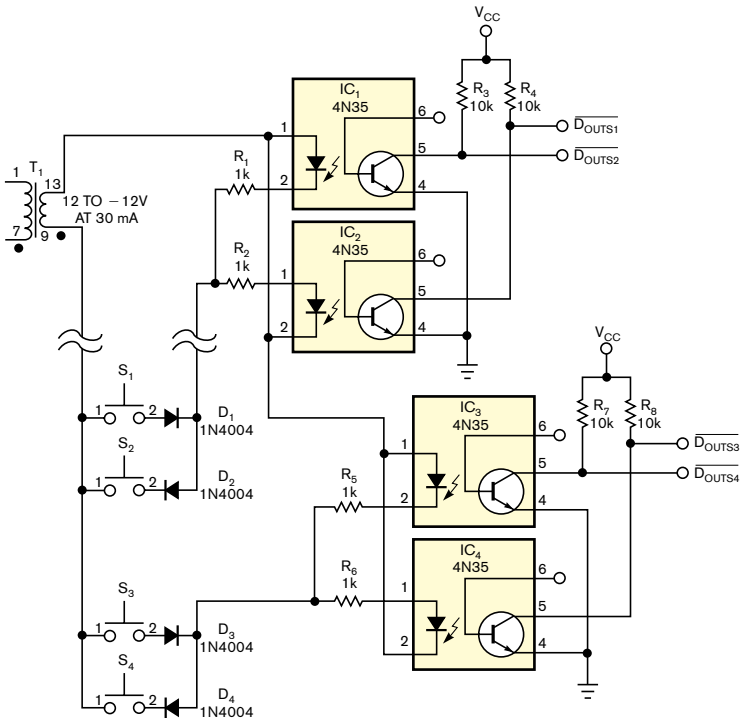

Figure 2 By adding a third wire, you can connect four pushbutton switches.

with one wire for communication and two for power. Another option is to use separate wires for each button. In that case, you would use one more wire than there are buttons. Finally, you could use a POE (power-over-Ethernet) approach, employing four wires for communication and power. All of these approaches require a button reader or a controller, which you must program, adding complexity and cost.

The circuit in **Figure 1** shows you how to connect two buttons using diodes. Because the diodes steer the current, the circuit needs just two wires. On a positive cycle from the transformer secondary and with switch S_2 closed, current flows through IC_1, R_2, and D_2. Thus, output $\overline{D_{OUTS2}}$ pulls low. Conversely, if S_1 closes on a negative cycle, then current flows through D_1 to R_1 and IC_2, which pulls $\overline{D_{OUTS1}}$ low. The circuit in **Figure 2** extends the concept to four pushbutton switches by adding a third wire. EDN

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designideas

READERS SOLVE DESIGN PROBLEMS

Unused port adds a PWM/analog channel to a microcontroller

Vishwas Vaidya, Tata Motors Ltd, Pune, India

Low-cost, 8-bit, single-chip microcontrollers are stingy when it comes to on-chip PWM (pulse-width-modulation) resources. The use of a PWM resource often forces a designer to sacrifice a capture/compare or timer channel because the PWM channel shares the same on-chip hardware. This Design Idea describes how you can use an on-chip unused synchronous serial port to generate PWM signals and convert them to a slow-moving analog signal (**Figure 1**). Many microcontroller-based stand-alone electronic units don't use the synchronous serial port. Thus, you can use the microcontroller's baud-rate generator and parallel-to-serial-converter blocks to generate bit patterns to form a 256-bit PWM pattern. You can then filter the PWM output with an RC filter to extract an analog signal (**Reference 1**). The synchronous communication is devoid of the start and stop bits of asynchronous mode, so the bit pattern can generate long periods of high or low level.

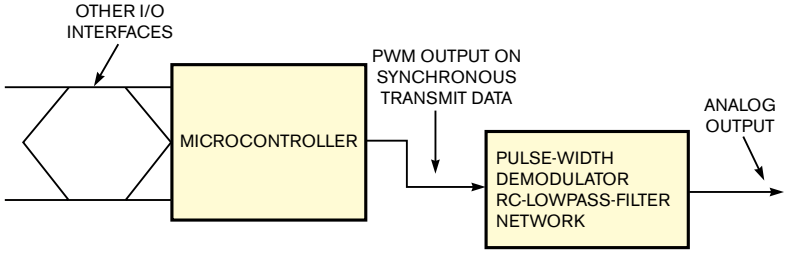
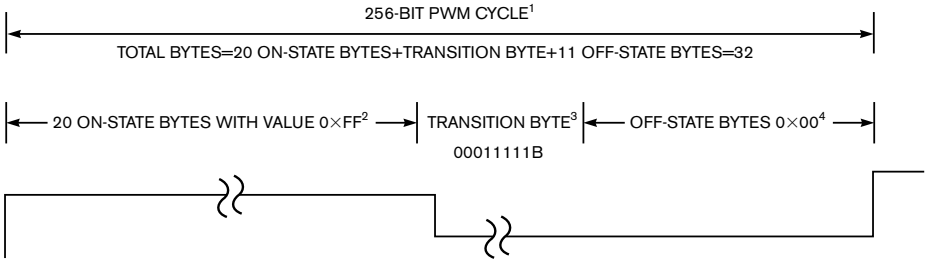


Figure 1 You can use an on-chip unused synchronous serial port to generate PWM signals and convert them to a slow-moving analog signal.



[1]RAW DATA=165; ON-STATE=5V; OFF-STATE=0V.
[2]NUMBER OF ON-STATE BYTES=165/8=20 (INTEGER DIVISION).
REMAINDER=165 – (8×20)=165 – 160=5.
[3]TRANSITION BYTE=00011111B=0×1F (NOTICE FIVE ONES FROM LSB SIDE).
[4]NUMBER OF OFF-STATE BYTES=TOTAL 32 BYTES – ONE TRANSITION BYTE – 20 ON-STATE BYTES=32 – 1 – 20=11 BYTES.
ANALOG OUTPUT AFTER LOWPASS FILTER=(165/256)×5=3.22V.

Figure 2 You can generate raw data with a decimal value of 165 using this concept.

You can generate raw data with a decimal value of 165 using this concept (**Figure 2**). A PWM-conversion cycle consists of generating 256 bits—that is, 32 bytes. The number of "on" bits corresponds to the value of the raw data to convert into PWM. Hence, for 165 bits as the raw data, 165 bits are on and 91

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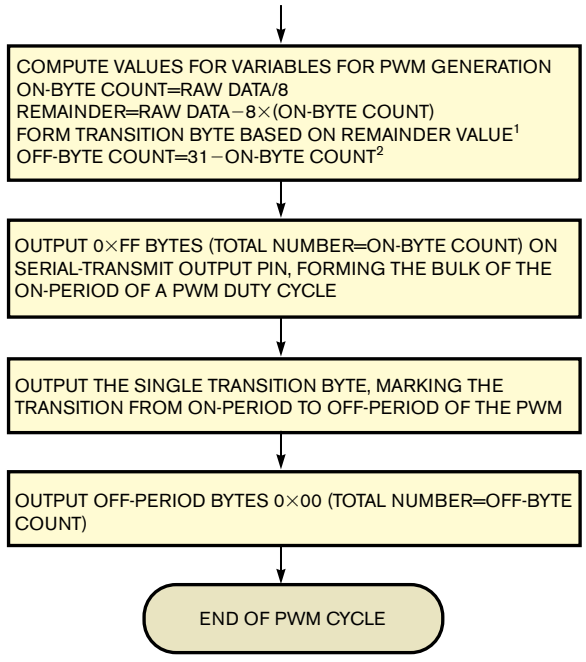


[1]TRANSITION BYTE CONSISTS OF A NUMBER OF ONE BITS STARTING FROM LSB. REMAINING BITS ARE ZERO. THE VALUE OF THE REMAINDER DECIDES THE NUMBER OF ONE BITS. IF THE REMAINDER IS THREE, THE TRANSITION BYTE IS 00000111B. FOR A REMAINDER OF FIVE, THE TRANSITION BYTE IS 00011111B. THE LSB TRANSMITS FIRST.

[2]FOR A SINGLE PWM CYCLE, TOTAL BITS=256 AND TOTAL BYTES=256/8=32. BECAUSE THE TRANSITION BYTE OCCUPIES 1 BYTE, THE OFF-BYTE COUNT=31 − ON-BYTE COUNT.

Figure 3 You can tailor the PWM frequency to your application by selecting a crystal, PLL, and baud rate.

bits are off. To generate a 165-bit on-period, the first 20 bytes—that is, 160 bits—transmit as 0×ff on-state bytes. The trick lies in judiciously composing the 21st, or transition, byte. This byte has some of its LSBs (least significant bits) as ones and the rest as zeros to form the required length of the on-period. In this case, the circuit needs five more on bits: 160+5=165. Hence, the transition byte should have a 00011111b pattern (byte=0×1f).

Figure 3 illustrates the process in flow-chart form. You can tailor the PWM frequency to your application by selecting a crystal, PLL (phase-locked loop), and baud rate. A simple RC filter can convert the PWM into a slow-moving analog value. Although this idea describes an 8-bit PWM, you can increase or decrease resolution by changing the total bits per PWM cycle. You correspondingly increase or decrease the conversion time.

Listing 1, which is available at www.edn.com/091008dia, provides a sample code for illustrating the concept. The code uses the Microchip (www.microchip.com) PIC18F4525, which has a 4-MHz crystal and 10-kHz baud rate for the synchronous serial communication, yielding 10,000/256=39.31 Hz of PWM frequency. You can filter it with a 0.1-sec RC filter, which is sufficient for slow-moving analog signals, such as speed setpoints for motion-control applications. By using a 20-MHz crystal, you can achieve synchronous serial baud rates greater than 1.5 MHz and PWM frequencies of a few kilohertz. EDN

REFERENCE

Mitchell, Mike, "Make a DAC with a microcontroller's PWM timer," *EDN*, Sept 5, 2002, pg 110, www.edn.com/article/CA240913.

Capacitance meter uses PLL for high accuracy

Jim McLucas, Broomfield, CO

An old *Electronics Designer's Casebook* described a circuit that provided capacitance measurements of 10 pF to 1 µF with 1% accuracy (**Reference 1**). A number of issues emerged with the circuit during testing, and this Design Idea describes an improved circuit. The meter circuit in **Figure 1** (pg 48) lets you measure capacitance from 10 pF to 10 µF with high accuracy. It needs no microprocessor; thus, it needs no code. Even in the 1- to 10-pF range, the circuit is accurate to about ±1 pF when reading values as low as 5 pF.

The circuit requires a high-input-impedance device to interface with the high-value resistors, R_6, R_8, R_9, and R_{10}, and a fast comparator to interface with the PLL (phase-locked loop). IC_1, an Analog Devices (www.analog.com) AD8033 op amp, does the job because of its 1000-GΩ input impedance and 1.7-pF input capacitance. It also has only 50 pA of input bias current over temperature. Its 80-MHz bandwidth and 80V/µsec slew rate are more than enough for this application. It can operate with just an 8V power supply. Unfortunately, the AD8033 is available only in surface-mount packages, which makes breadboarding somewhat tedious. IC_2, an Analog Devices ADCMP601 comparator, interfaces

with the AD8033 op amp and IC_3, a 74HC4606A PLL. The comparator has a typical propagation delay of only 4.3 nsec. It has built-in hysteresis and needs only a 5V supply. It is also available only in surface-mount packages.

The capacitance meter generates two signals; one of them lags the other by 60°. A 3-bit, self-correcting, divide-by-six twisted-ring counter comprising IC_6, IC_7, and IC_{13B} provides the lagging signal. The lagging signal connects to the COMP input of the PLL (Pin 3), and the other signal is applied to an RC circuit, which provides a 60° phase lag before it gets to the SIG input of the PLL (Pin 14). The PLL adjusts the frequency of its VCO (voltage-controlled oscillator) so that the two input signals are in phase. The resulting period of the VCO's output signal (Pin 4) is proportional to the measured capacitance.

On the low-capacitance range, signals with frequency F_O are applied to the PLL. On the high-capacitance range, the frequency is $F_O/1000$. IC_8 through IC_{10} provide the division, and S_2, IC_{4B} through IC_{4D}, IC_{5D}, IC_{5E}, and the associated components provide the high-capacitance/low-capacitance range switching. The VCO of the PLL runs at $6F_O$. The circuit divides this signal by three to provide an output with a period that's proportional to the measured capacitance. It provides the correct digits when you measure with a frequency counter that you set to measure the period. You can calculate F_O or $F_O/1000$ from $0.1505/R_XC_X$, where R_X is R_6, R_8, R_9, or R_{10}, depending on the selected range.

The 74HC4046A PLL can exhibit several problems. For example, it may not start when you apply power, or it may hang with the VCO running with the VCO-input pin (Pin 9) stuck high or low. The start-up circuitry, comprising IC_{13F}, Q_4, and associated components, applies a positive voltage of approximately 2V to the VCO's input, which forces the VCO to oscillate. After the VCO starts, D_4 becomes back-biased, which disconnects the start-up circuitry from the VCO's input pin. If the VCO is running but hung with its input stuck high or low, one-shot IC_{12A} detects that it's not phase-locked by responding to pulses from Pin 1 of IC_3. The one-shot then issues a 1.5-sec pulse that causes IC_{12B} to produce a 0.5-sec pulse that causes either a positive pulse at the inhibit pin or a low pulse at the VCO's input pin, depending upon whether the PLL is low or high. After the 0.5-sec pulse ends, the pulse from IC_{12A} continues for 1 sec, giving the PLL time to lock. LED D_7 indicates phase lock. If the PLL phase locks, all is well. If it does not, the IC_{12A}/IC_{12B} one-shots continue issuing pulses. Experiments determined these methods for recovering from the anomalous states. It's possible that the circuit won't always recover, but these methods have been effective on the test unit.

THE 74HC4046A PLL MAY NOT START WHEN YOU APPLY POWER.

The circuit applies the $6F_O$ signal, divided by three, to buffer IC_{5F}'s Pin 5. This action provides an output frequency whose period is proportional to the value of the measured capacitance. The output provides the correct digits without regard to the location of the decimal point. To determine the value of the unknown capacitance, observe the setting of S_1 and S_2.

You can calibrate the circuit by using a capacitance of a known value of approximately 1000 pF, with S_2 at the low-capacitance position and S_1 at the 100- to 1000-pF/0.1- to 1-µF position. Set R_{22} at its midposition, connect a frequency counter to Pin 6 of IC_{5F}, and set the meter to measure the period of the signal. Adjust R_{12} for a period whose digits agree with the known value of capacitance. Next, use a capacitance of approximately 100 pF and set S_1 to the 10- to 100-pF/0.01- to 0.1-µF position. Record the measured value of the capacitor. Then, using the same capacitance of approximately 100 pF, set S_1 to the 100- to 1000-pF/0.1- to 1-µF position and adjust R_{22} to get the same value as you obtained on the 10- to 100-pF/0.01- to 0.1-µF position. The R_{22}/C_{13} combination provides a small variable delay relative to the signal at Pin 14 of IC_3. This fine adjustment improves accuracy in the lower range.

Employing measurements made with the available equipment, which did not include an accurate, high-resolution capacitance meter, this meter is accurate to approximately ±2% over 100 pF to 10 µF (**Table 1**). The accuracy degrades over 10 to 100 pF because of the input capacitance of the op amp and the associated parasitic capacitance at IC_1's Pin 3. R_7 and C_6 provide some compensation at the 10- to 100-pF range for the inherent capacitance at that node. R_5 and C_5 provide compensation at the 1- to 10-pF range.

You can also measure the inherent capacitance and then subtract it from the reading on the two lower ranges. If you take this approach, omit R_5, R_7, C_5, and C_6 from the circuit. Then, with S_1 at the 1- to 10-pF range and S_2 at the low-capacitance position, you can measure the capacitance at that node with no external capacitance. The in-

(*continued on page 50*)

TABLE 1 CAPACITANCE MEASUREMENTS

Range	1 to 10 pF	10 to 100 pF	100 to 1000 pF	1000 to 10,000 pF	0.01 to 0.1 µF	0.1 to 1 µF	1 to 10 µF
Capacitance	5.24, 10.04	10.04, 23.22, 47.6, 102.68	102.68, 469.32, 1022.1	1022.1, 5226.9, 10,140	0.01014, 0.10052	0.10052, 1.034	1.034, 10.07
Measurement error (%)	−8.85, 2.89	6.37, −4.78, −3.68, −0.61	−0.86, −2.5, −0.7	−0.89, −1.28, 0	0.89, 0.88	2.27, −0.87	2.03, 1.24

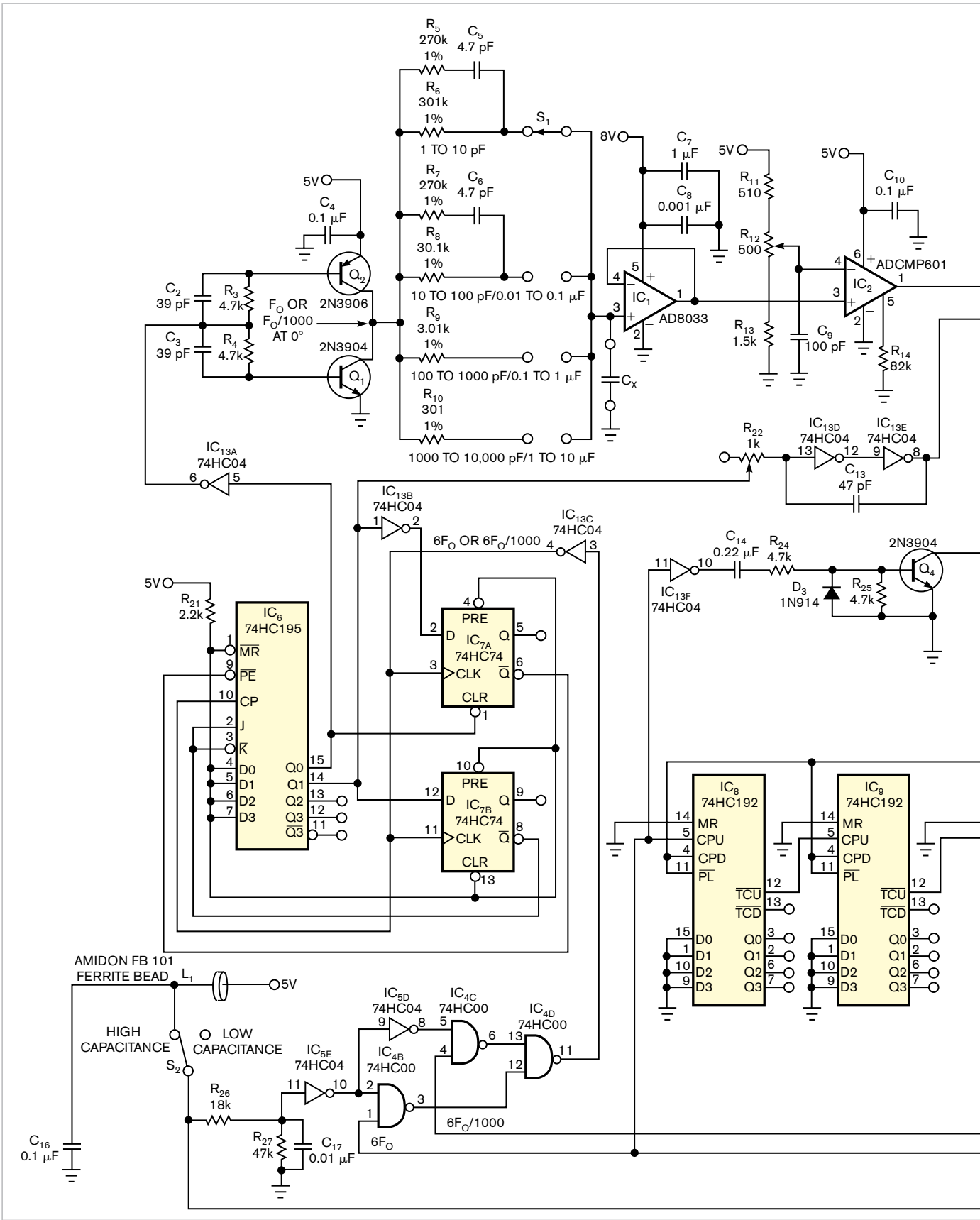
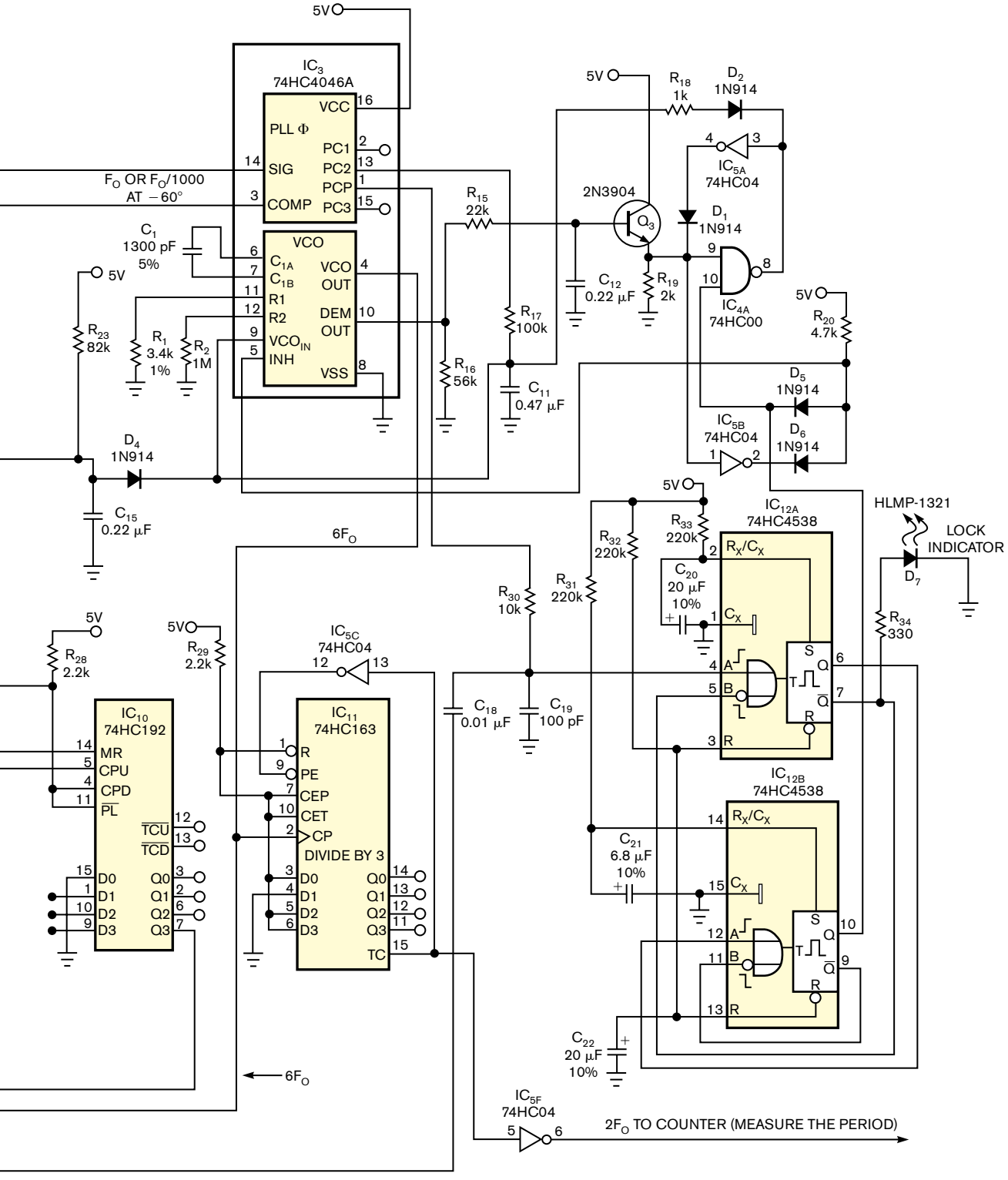


Figure 1 A capacitance meter connects to a frequency counter measuring pulse width to provide a capacitance measurement.


5V
IC3
74HC4046A
VCC
PLL Φ
PC1
PC2
PCP
PC3
SIG
COMP
VCO
VCO OUT
DEM OUT
VCOIN
INH
VSS
FO OR FO/1000
AT −60°
C1
1300 pF
5%
R23
82k
R1
3.4k
1%
R2
1M
R15
22k
R16
56k
R17
100k
C11
0.47 µF
R18
1k
D2
1N914
IC5A
74HC04
2N3904
Q3
D1
1N914
C12
0.22 µF
R19
2k
IC4A
74HC00
R20
4.7k
D5
1N914
IC5B
74HC04
D6
1N914
D4
1N914
C15
0.22 µF
6FO
R32
220k
R33
220k
IC12A
74HC4538
RX/CX
C20
20 µF
10%
CX
R31
220k
R30
10k
HLMP-1321
LOCK
INDICATOR
D7
R34
330
R28
2.2k
R29
2.2k
IC5C
74HC04
IC10
74HC192
MR
CPU
CPD
PL
TCU
TCD
D0
D1
D2
D3
Q0
Q1
Q2
Q3
IC11
74HC163
R
PE
CEP
CET
CP
DIVIDE BY 3
TC
C18
0.01 µF
C19
100 pF
IC12B
74HC4538
C21
6.8 µF
10%
C22
20 µF
10%
IC5F
74HC04
2FO TO COUNTER (MEASURE THE PERIOD)

(*continued from page 47*)
trinsic capacitance of the test circuit is 2.8 pF. Using this correction, the values you obtain on the lowest two ranges are accurate to approximately ±2%, or ±1 pF.

You must observe capacitor polarity when measuring electrolytic capacitors. Connect the negative end of the capacitor to the grounded terminal. Also, the circuit provides no overvoltage or ESD (electrostatic-discharge) protection, so be sure to discharge the capacitors before connecting them to the capacitance meter and use an ESD wrist strap to avoid damaging the circuit. For best results, you need accurate and stable 5 and 8V power supplies. Both supplies should be accurate to ±2%. You can raise the 8V supply to 9V and relax the accuracy to 5%. If you use a 9V battery to supply the 8V, you can let the voltage drop to about 7.9V before adversely affecting the performance of the meter. You must, however, maintain the 5V supply at a constant, accurate value. Note that all of the ICs except IC_1 have 0.1-µF bypass capacitors from their 5V pins to ground. EDN

REFERENCE

1 Pyle, Ronald E, "Phase-locked loop aids in measuring capacitance," *Electronics Designer's Casebook*, No. 4, pg 32.

Resistor compensates for instrumentation-amp gain drift

Kenneth Gustafsson, Karlskoga, Sweden

Some instrumentation amplifiers use external resistors to set their gain. Unfortunately, the lack of temperature-coefficient matching between the external and the internal resistors results in a high gain drift. If, however, another on-chip resistor is available, you can use it to compensate for gain drift as a result of temperature.

As an example, Analog Devices' (www.analog.com) AD8295 has a drift of as much as −50 ppm/°C, even if you use a zero-drift gain-setting resistor. In this Design Idea, you can compensate this drift with an extra zero-drift resistor in combination with an internal chip resistor.

The gain-set **equation** from the data sheet (**Reference 1**) is

$$\text{GAIN} = 1 + \frac{49{,}400}{R_G}.$$

From this gain-set **equation**, you can assume that the chip uses two 24.7-kΩ resistors with the external gain resistor, R_G, to set the amplifier's gain. The chip has two more 20-kΩ resistors. Because all of these chip resistors are of the same magnitude, they probably will have good temperature-coefficient matching, and you can use this matching for compensation. If the amplifier resistance, R_A, and the gain resistor are zero-drift resistors (**Figure 1**), then

$$\text{GAIN} = \left[1 + \frac{49{,}400\,(1+\Delta)}{R_G}\right]\left[1 + \frac{2 \times R_A}{20{,}000\,(1+\Delta)}\right],$$

where Δ is the drift of the internal matched resistors. If

$$\frac{49{,}400}{R_G} = \frac{R_A}{10{,}000},$$

then the first-order drift of the gain cancels, and the gain splits equally between the instrumentation amplifier and A_1. Solving for R_G and R_A yields

$$R_G = \frac{49{,}400}{\sqrt{\text{GAIN}} - 1};$$

$$R_A = 10{,}000\left(\sqrt{\text{GAIN}} - 1\right).$$

For gain greater than 100, the amplifier resistance becomes greater than 90 kΩ, which can be problematic. In this case, you can use A_1 in an inverting configuration with a gain of −1

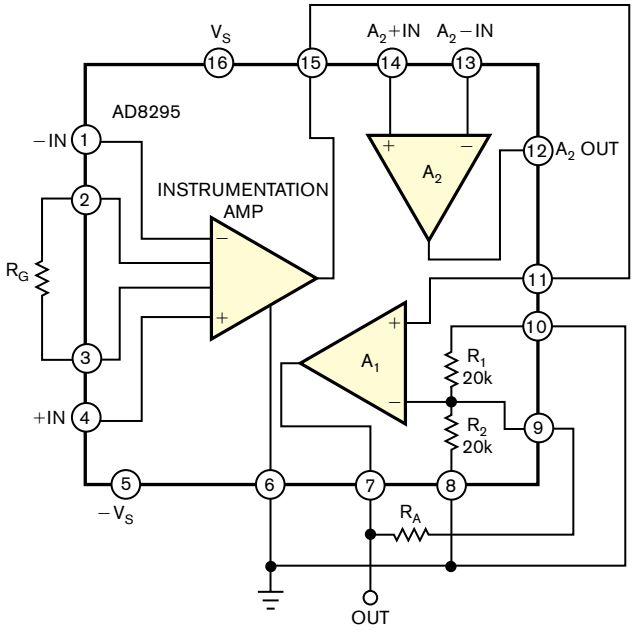


Figure 1 In this configuration, the first-order drift of the gain cancels, and the gain splits equally between the instrumentation amplifier and A_1.

(**Figure 2**). With an amplifier resistance of 10 kΩ,

$$GAIN = \left[1 + \frac{49{,}400\,(1+\Delta)}{R_G}\right]$$

$$\left[\frac{2 \times R_A}{20{,}000\,(1+\Delta)}\right] = \left[\frac{1}{(1+\Delta)} + \frac{49{,}400}{R_G}\right].$$

This case sizes R_G using a value from the data-sheet formula. If the gain is 50, the internal matching and the negative drift compensate the "49" part of the gain, and the "one" part is just the drift divided by 50 in the total gain, resulting in a typical figure of −1 ppm/°C. In both cases, the resulting gain temperature coefficient can be less than 5 ppm/°C, which is 10 times better than the original outcome. EDN

REFERENCE

1 "AD8295: Precision Instrumentation Amplifier with Signal Processing Amplifiers," Analog Devices, www.analog.com/en/amplifiers-and-comparators/instrumentation-amplifiers/ad8295/products/product.html.

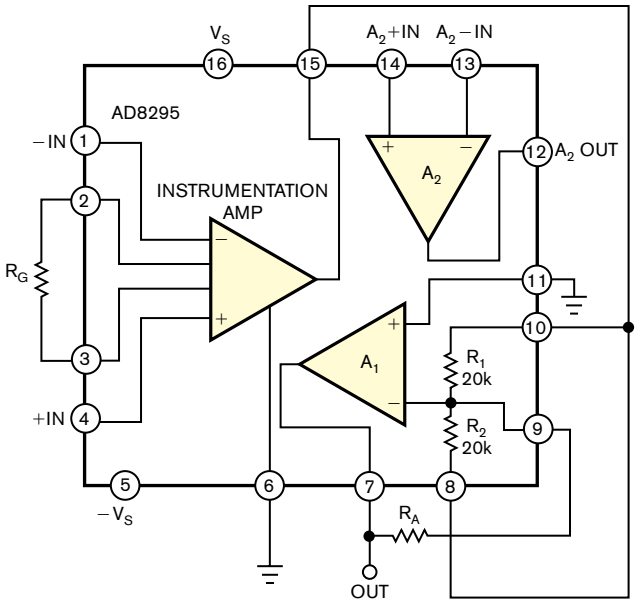


Figure 2 For gain greater than 100, the amplifier resistance becomes greater than 90 kΩ, in which case you can use A_1 in an inverting configuration with a gain of −1.

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designideas

READERS SOLVE DESIGN PROBLEMS

Astable multivibrator gets hysteresis from positive-feedback stage

Robert Larson, Seattle, WA

Many designs exist for logic-based astable multivibrators, one of the simplest being an RC feedback loop around a single inverting Schmitt trigger inverter (**Figure 1**). The output charges the capacitor to the upper switching threshold, at which point the output switches to its opposite state, the threshold switches to a different value, and the capacitor's charging current reverses direction. When the capacitor's voltage crosses the lower threshold, the output and threshold both toggle back to their original values, and the process repeats. The timing depends on both the RC time constant and the hysteresis resulting from the spread between the two threshold values (**Figure 2**). Unfortunately, although inverter manufacturers specify the hysteresis voltages in their data sheets, the devices have a fairly large range. In addition, they likely have some temperature dependence. These uncertainties make it difficult to design the circuit to have a predictable oscillating frequency.

A simple inverter, without the hysteresis to let it overshoot the nominal threshold, charges the capacitor to the threshold voltage and stops in its narrow linear region. At this point, the negative feedback from the inverting output to the input regulates the output to the threshold voltage. Adding another inverting stage injects hysteresis of a different form by means of positive feedback, which external passive

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TABLE 1 74VHC04 RESULTS

Resistance (kΩ)	Timing capacitance (pF)	Hysteresis capacitance (pF)	Expected results: Hysteresis voltage (V)	Expected results: Total time period (nsec)	Measured results: Hysteresis voltage (V)	Measured results: Total time period (nsec)	Total time differential (%)
10	470	100	0.88	3462	0.75	2930	18
10	470	220	1.59	6850	1.8	7340	−7
10	12,000	12,000	2.5	333,526	2.6	364,800	−9
0.3	220	220	2.5	221	1.75	240	−8
1	12,000	12,000	2.5	34,086	2.5	36,000	−5

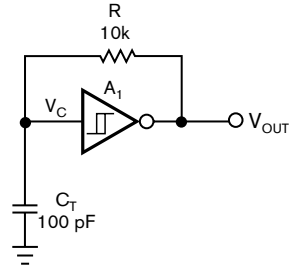

Figure 1 A basic astable multivibrator uses a Schmitt trigger and an RC network.

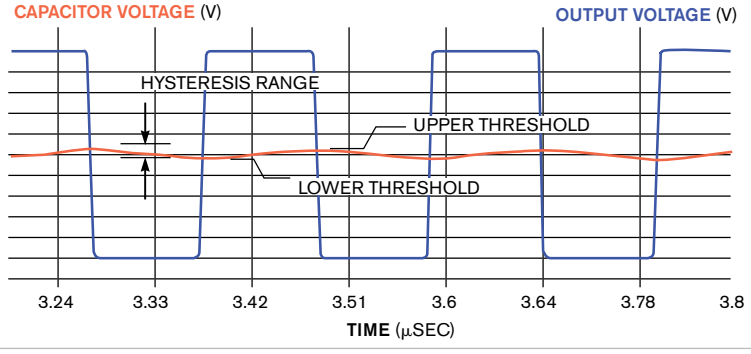

Figure 2 A part's hysteresis, in large part, determines switching thresholds.

parts determine (**Figure 3**).

Whenever Stage 1 crosses its threshold, the extra Stage 2 injects an additional charge through a feedback capacitor to make the timing capacitor's voltage jump past the threshold. The RC charging current reverses direction to get back to the threshold voltage. When it gets there, the hysteresis-injection circuit again jumps the voltage past the target so that the RC timing circuit must again reverse the charging current to seek the threshold voltage (**Figure 4**). This process continues endlessly at a fairly predictable rate. In the **equations**, C_T is the timing capacitor, C_H is the hysteresis capacitor, V_{THRESH} is the threshold voltage, V_{LOW} is the low output voltage, and V_{HIGH} is the high output voltage.

You can view the hysteresis-overshoot voltage, V_{HYST}, as the result of a capacitive voltage divider that timing capacitor C_T and hysteresis capacitor C_H form. When Stage 1 toggles Stage 2, its output jumps from a low value to a high value or from a high value to a low value by an amount of $V_{HIGH}-V_{LOW}$, and the voltage of the timing capacitor jumps by $V_{HYST}=(V_{HIGH}-V_{LOW})(C_H/(C_H+C_T))$. Second, the voltage of the timing capacitor relaxes back toward Stage 1's output voltage by drawing current through both the timing capacitor and the hysteresis capacitor.

Thus, the relaxation time constant is $R(C_T+C_H)$ and the relaxation voltage is either $V_{CT}=(V_{THRESH}+V_{HYST}-V_{LOW})\exp(-t/R(C_T+C_H))$ or $V_{CT}=(V_{HIGH}-(V_{THRESH}-V_{HYST}))\exp(-t/R(C_T+C_H))$, depending on which half-cycle is occurring. You calculate the time from $V_{THRESH}+V_{HYST}$ back to V_{THRESH} as $t_1=-R(C_T+C_H)\ln((V_{THRESH}-V_{LOW})/(V_{THRESH}+V_{HYST}-V_{LOW}))$. For the other half-cycle, $t_2=-R(C_T+C_H)\ln((V_{HIGH}-V_{THRESH})/(V_{HIGH}-V_{THRESH}+V_{HYST}))$.

You should add the total propagation time ($t_{PLH}+t_{PHL}$) through stages 1 and 2 to the total period. Unless you want the circuit to operate at its maximum frequency, these propagation times become insignificant. The period prediction then depends only on passive-component values and their tolerances, temperature, and aging coefficients. The series combination of C_T and C_H, however, presents a capacitive load to Stage 2. This load affects Stage 2's rise and fall times, the sum of which you must add to the total period, T.

In the case of CMOS parts, such as the 74VHC04 from Fairchild Semiconductor (www.fairchildsemi.com), rise and fall times depend on the output resistance of the part as well as on the external components. If you model the Stage 2 output as an RC circuit, you can estimate the 10 to 90% exponential rise and fall times as $t_{RISE2}=t_{FALL2}=2.2R_O(C_TC_H/(C_T+C_H))+t_O$, where t_{RISE2} is the rise time, t_{FALL2} is the fall time, R_O is the output resistance of the part—30Ω for the 74VHC04—and t_O is the no-load rise time—in this case, 4.5 nsec for the VHC04. Thus, the total period is $t_1+t_2+2(t_{PLH}+t_{PHL})+t_{RISE2}+t_{FALL2}$.

Also note that the timing depends on inverter output voltages and the location of the threshold voltage within that range. For example, a CMOS part whose outputs are close to the power rails is more predictable than a TTL (transistor-transistor-logic) part, and a 74HC part with a midpoint threshold voltage has a more symmetric output than an HCT part whose threshold voltage is offset for TTL interfacing.

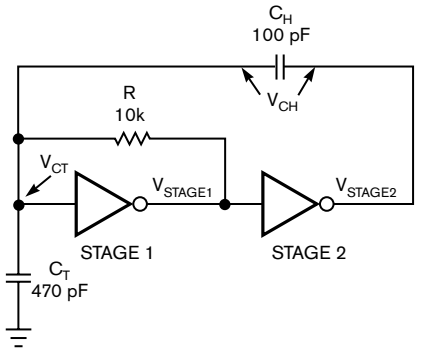

Figure 3 The addition of a positive-feedback stage provides hysteresis to a simple inverter stage.

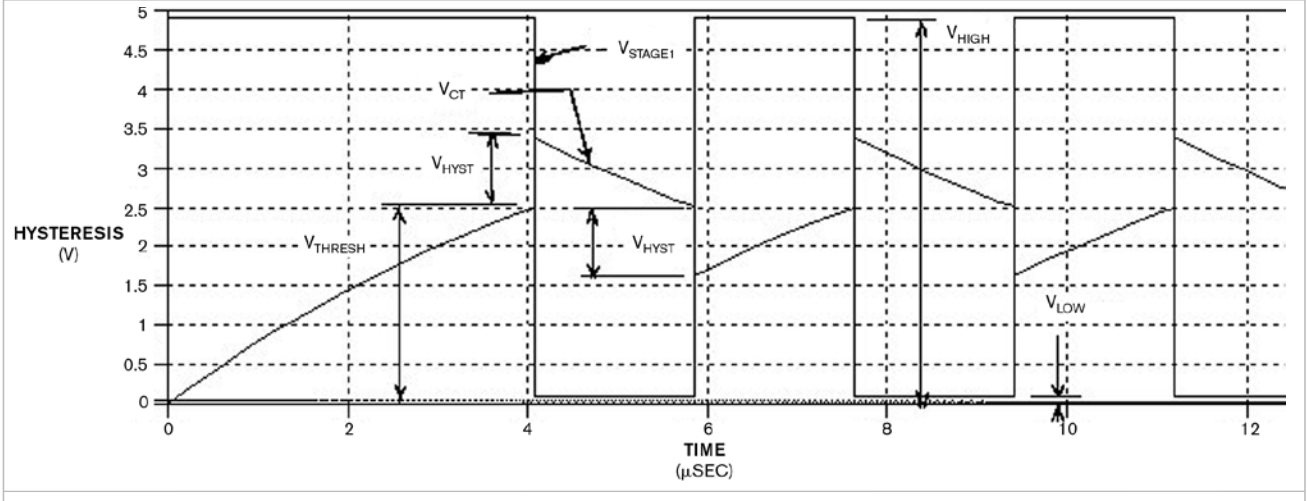

Figure 4 Hysteresis results from a charge burst from Stage 2 that jumps the timing-capacitor voltage past the switching threshold by a known, fixed amount.

For higher frequencies, you must use smaller resistor values, smaller timing-capacitor values, or both. For predictable results, the value of the timing capacitor should be no less than 10 times the inverter's input capacitance, which ranges from 3 to 10 pF for a typical CMOS, and R should not be so low that it significantly loads down the output. As a precaution, the value of the hysteresis capacitor should not exceed that of the timing capacitor so that it does not exceed the maximum input voltage on Stage 1. If the value of the hysteresis capacitor were much greater than that of the timing capacitor, then the threshold voltage and the hysteresis voltage would approach 7.5 and −2.5V, respectively. The 74VHC04 part proves the calculations using 5% resistors and 20% capacitors.

Table 1 summarizes the results, which are within the component tolerances. **Figure 5** shows a typical input and output plot.EDN

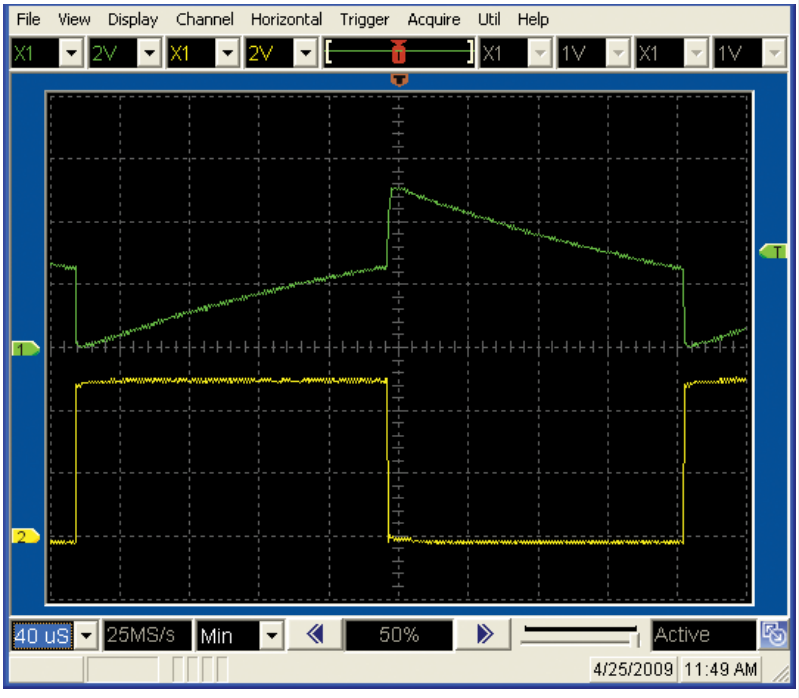

Figure 5 The circuit is well-behaved at low frequencies.

Class B amplifier has automatic bias

Pierre Corbeil, Paradox Innovation, Montreal, PQ, Canada

Class B amplifiers are prone to crossover distortion, which occurs in the output stage in which conduction transfers from one transistor to the other. To prevent crossover distortion, a bias current must flow in both transistors simultaneously. The bias current prevents both transistors from turning off in the transition region. Classic bias circuits keep a constant dc polarization voltage between the bases of the two transistors. Often manually adjusted, it keeps the two transistors on the edge of conduction when there is no signal present. Such a circuit is sensitive to temperature and needs some form of compensation to prevent thermal runaway, which can lead to failure. **Figure 1** shows an approach in which automatic bias eliminates the problem.

In this Class B amplifier, R_1 sets the bias current at idle mode with no signal. Emitter current for Q_3 is $(V_{CC}-V_{BIAS}-V_{BEQ3}-V_{BEQ1})/R_1$, where V_{CC} is the power-supply voltage, V_{BIAS} is the dc voltage on the emitters of Q_1 and Q_2, V_{BEQ3} is the base-to-emitter voltage of Q_3, and V_{BEQ1} is the base-to-emitter voltage of Q_1. Q_1 and Q_2 mirror this current because Q_1 and Q_3 share the same base current, as do Q_2 and Q_4. Assuming that the four transistors are perfectly matched, all of them have the same base current and the same collec-

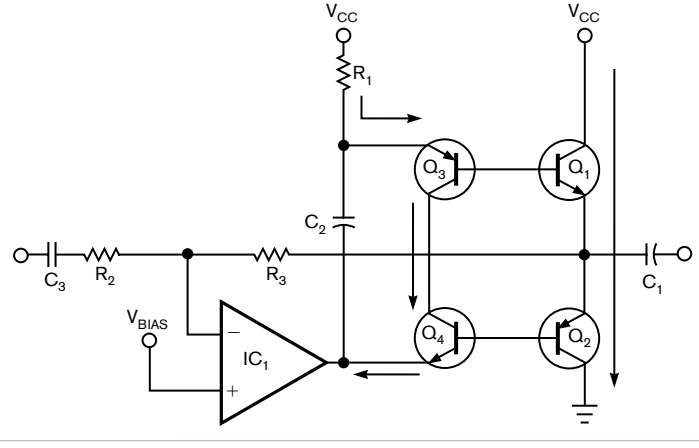

Figure 1 A bias current flows in the transistors that prevents Q_1 and Q_2 from being off simultaneously.

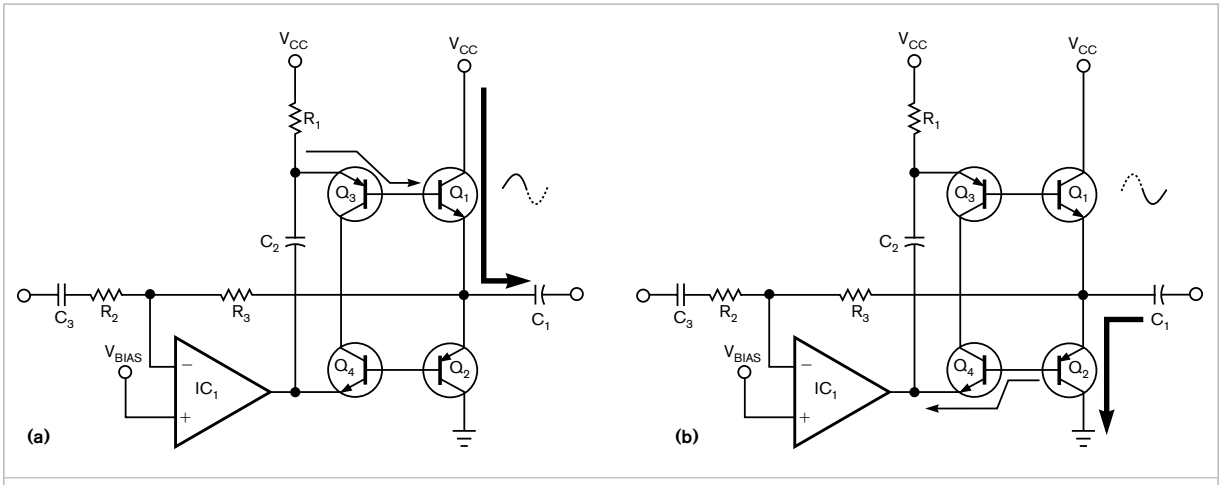

Figure 2 On a positive half-cycle, current flows from Q_1 through C_1 to a load (a). On a negative half-cycle, current flows through Q_2 (b).

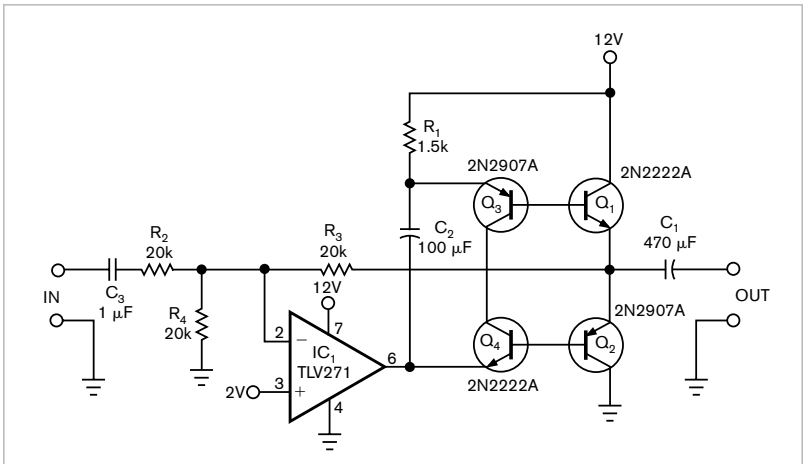

Figure 3 A typical application of this Class B circuit is a headphone amplifier.

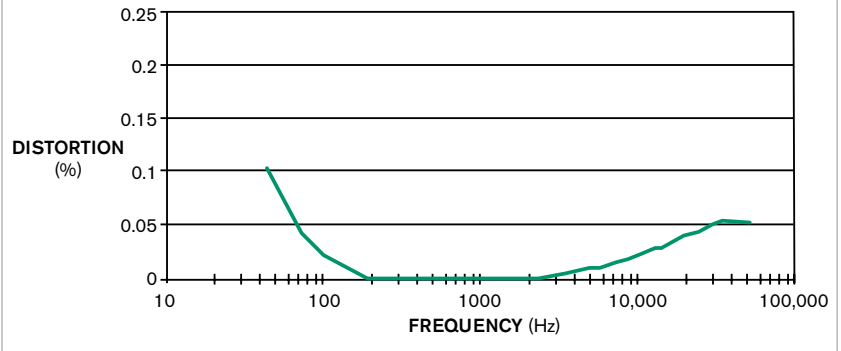

Figure 4 This graph shows distortion as measured on the circuit of Figure 3.

tor current, so the emitters of Q_1 and Q_2 precisely mirror the current in R_1. Transistor matching is unnecessary, however. With unmatched transistors, either Q_3 or Q_4 must operate in saturation, and, because the mirror effect depends on the transistors' current gain, h_{FE}, the difference between Q_1/Q_2 bias current and the current in R_1 can be significant. This circuit automatically adjusts the voltage on C_2 to compensate for temperature and the transistors' characteristics.

When a signal is present, the current gain is the h_{FE} of output transistor Q_1 or Q_2 (the same as for a classic Class B amplifier). On the positive part of the signal, Q_1 carries the load current. Because the base current increases, Q_3 enters saturation. On the negative part of the signal, Q_2 carries the load current and Q_4 saturates.

Figure 2 shows the ac-current path. The maximum average load current is the idle current in R_1 times the current gain of Q_1 times two. The op amp must be able to sink the base current of Q_2 (load current/h_{FE})+(($V_{CC}-V_{BE}\times4$)/R_1). A typical application of this Class B amplifier delivers 0.25W into 8Ω (**Figure 3**). **Figure 4** shows the total harmonic distortion over the 45-Hz to 50-kHz band—that is, 1V rms into 8Ω. EDN

Cable tester uses LEDs to find faults

Pavel Šádek, Apri, Rožnov pod Radhoštěm, Czech Republic

This Design Idea describes a simple cable-test machine that visually shows continuity issues on a 16-wire cable harness for ultrasonic-parking-aid systems. A subcontractor produces the harness in low volumes, making it impractical to use an automated tester. For simplicity, the test signal drives LEDs for a visual indication of continuity.

The circuit in **Figure 1** generates a binary number from zero to 15 (0000 to 1111). You can generate the numbers with a 555 timer and a binary counter, but this circuit uses a tiny, eight-pin microcontroller. A four-wire bus sends the digits to two four- to 16-line 74HC154 decoders, which generate active-low signals on their 16 lines. Inverting the outputs of the driver decoder with a 74HC04 inverter provides a drive signal for an LED and current-limiting resistor on each harness wire.

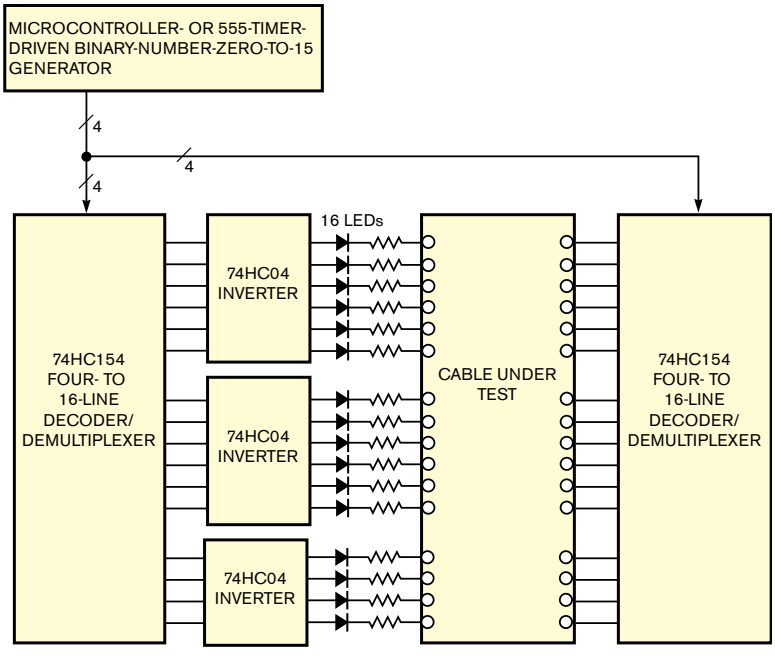

Figure 1 A pair of four- to 16-line demultiplexers selects cable-harness wires for testing.

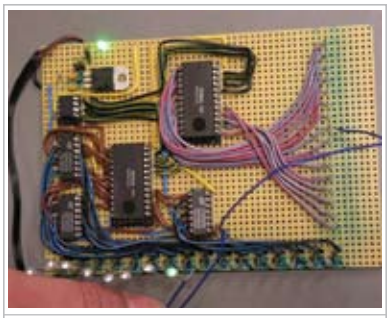

Figure 2 The cable-harness tester uses LEDs to indicate good connections.

The tester should produce one and only one illuminated LED for a good wire as the circuit scans the harness. If the scan is fast enough, all LEDs will all appear to be on, although each is on for just one-sixteenth of the time. **Figure 2** shows the completed circuit with eight LEDs, but it has room for 16 LEDs.

Broken wires in a harness, wrong wire positions, or other continuity failures lead directly to the turn-off of the corresponding LED. Swapped wires can also lead to the turn-off of two LEDs. Meanwhile, only one cathode is driven high, whereas the others are driven low, and only the cathode's anode is driven low, whereas the others are driven high. So only correctly connected wires could pass this test.

If you need to test harnesses with more that 16 wires, you can cascade additional decoders. You can also use a high-pin-count microcontroller in the same way. EDN

Dual-coil relay driver uses only two MOSFETs

Mehmet Efe Ozbek, PhD, Atlim University, Ankara, Turkey

Latching relays change their states when you apply a short voltage pulse to their coils. Because these relays require no continuous coil currents to keep their states, you can save considerable power in the driver circuit. In one type of latching relays, you can alternately energize dual coils to change the relay state. Simply apply voltage to one coil for the set state and to the other coil for the reset state. Applying a 25- to 50-msec-wide voltage pulse to the coils is sufficient for operating the relay. Many relays can operate with a continuous coil current, and some dual-coil relays have internal contacts that interrupt the coil current after it completes a state change. Continuous coil voltages can drive such relays if energy efficiency is not a big concern.

The need to differentially drive the coils results in crowded drive circuits for dual-coil relays. Drivers usually in-

clude logic elements to make sure to energize only one coil at a time. The design in **Figure 1** uses only two MOSFETs to drive a dual-coil RF relay. The Agilent Technologies (www.agilent.com) N1810UL RF switch has dual 24V coils and internal current-interrupting contacts.

When logic input is high, Q_1 conducts and changes the relay state by activating L_1. The states of the current-interrupting contacts also change. Meanwhile, Q_2 is off because Q_1 pulls down its gate, which avoids fighting between the coils. If you then apply a low signal to the logic input, Q_1 turns off and keeps the L_1 coil inactive. Because R_1 pulls up Q_2's gate, Q_2 turns on and energizes L_2. The 1N4007 diodes prevent inductive kickback. The idea is applicable to dual-coil relays with continuously rated coils or with current-interrupting contacts. In the absence of current-interruption contacts, L_1 can serve as a pullup, and R_1 therefore becomes redundant. EDN

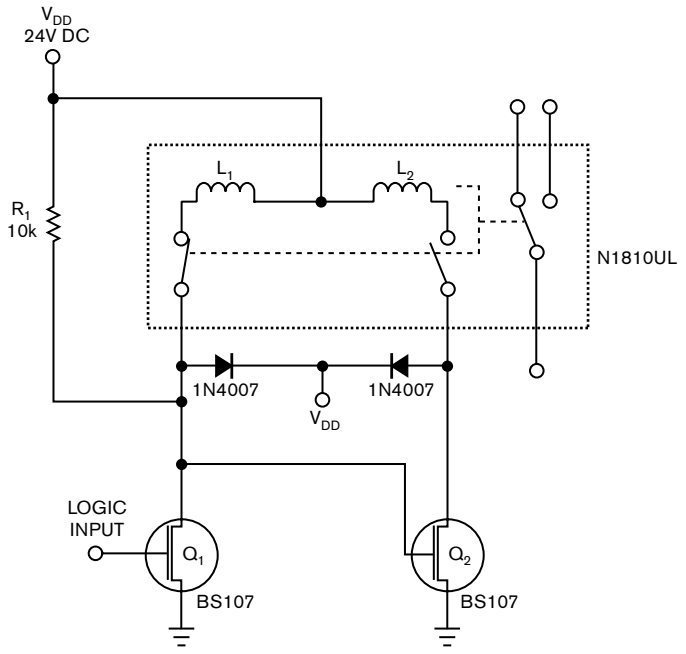

Figure 1 Using two MOSFETs to differentially drive a dual-coil latching relay eliminates the need for any logic components.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Negative-to-negative switch-mode converter offers high current and high efficiency

Budge Ing, Maxim Integrated Products Inc, Sunnyvale, CA

When converting a negative-output power supply to one with less-negative output, you must ensure that variations in input voltage don't affect the output voltage. All such supplies include an internal reference voltage that enables output-voltage regulation. You usually refer this reference to the most negative rail, which is ground. Thus, the output voltage of such a converter depends on the accuracy of its negative input supply voltage. The circuit in **Figure 1** lacks that limitation. Delivering output currents as high as 4A with efficiencies better than 90%, it generates a negative output with the help of an op amp and a switch-mode boost converter. Closed-loop feedback regulates the output voltage with respect to ground, the most positive rail,

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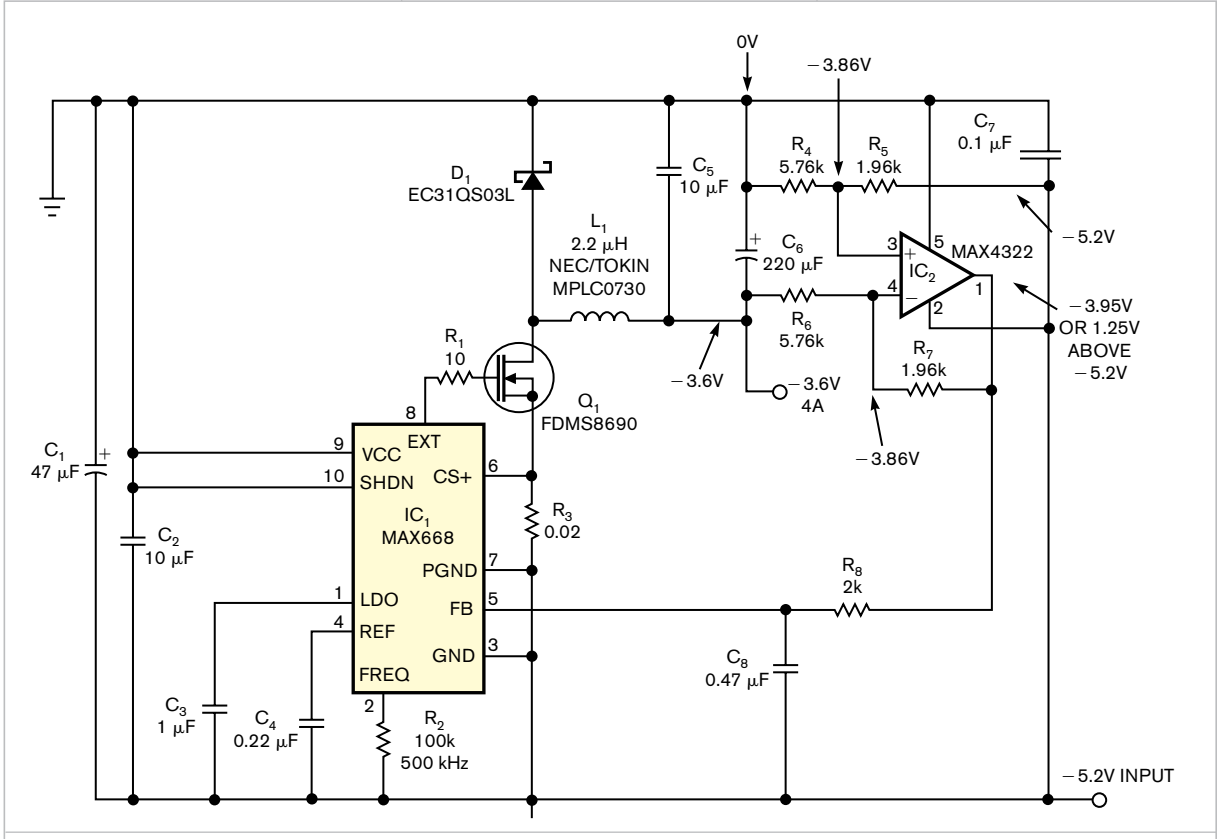

Figure 1 A switch-mode converter generates a regulated negative supply voltage from a more-negative input voltage.

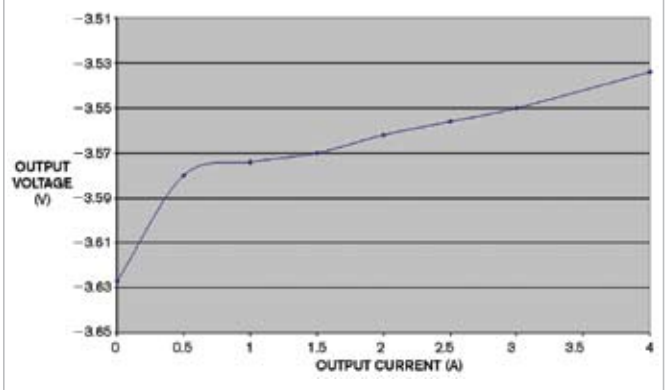

Figure 2 Output voltage for the circuit in Figure 1 varies with output current.

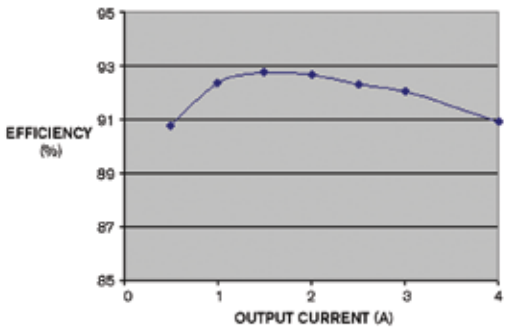

Figure 3 Conversion efficiency for the circuit in Figure 1 varies with output current.

which is also the node from which current is delivered to the load.

The circuit converts a −5.2V supply voltage to −3.6V. The boost converter, IC_1, regulates its output voltage to maintain its feedback voltage at −3.95V—1.25V above −5.2V. Resistor R_8 and capacitor C_8 form a low-pass filter that stabilizes the voltage at FB. You must then select the R_4/R_6 and R_5/R_7 pairs to produce the desired output voltage. Making R_4 and R_5 equal and making R_6 and R_7 equal improves the common-mode performance. The ratio of R_4 to R_5 determines the voltage level at the positive input of op amp IC_2, whose closed-loop configuration ensures that the same voltage appears at its negative input. Knowing IC_2's output voltage, −3.95V, and its negative input voltage lets you determine the output voltage using the values of R_6 and R_7: $V_{OUT}=-V_{REF}(R_6/R_7)$, where V_{REF} is the 1.25V nominal reference voltage of IC_1, $R_4=R_6$, and $R_5=R_7$.

The component values in **Figure 1**—for example, 1.96 kΩ for R_5 and R_7 and 5.76 kΩ for R_4 and R_6—produce an output voltage of −3.76V. Graphs of output voltage versus output current (**Figure 2**) and efficiency versus output current (**Figure 3**) illustrate this circuit's performance. EDN

ADC for programmable logic uses one capacitor

Jef Thoné and Robert Puers,
Katholieke Universiteit Leuven, Leuven, Belgium

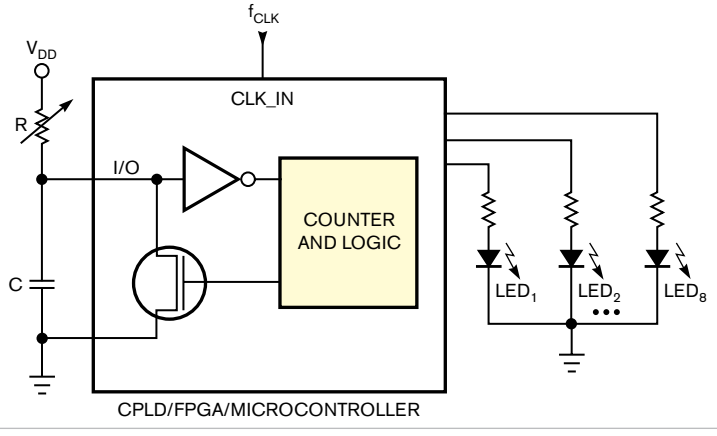

Figure 1 This circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Many electronic devices require user input for setting the application properties. Typical input devices include pushbuttons, potentiometers, and touchscreens. To minimize overall project cost, you may have to select low-range microcontrollers, FPGAs (field-programmable gate arrays), or PLDs (programmable-logic devices). These devices don't provide a wide range of peripherals and often lack analog-to-digital-conversion capability, which can prove annoying when trying to acquire user input. This Design Idea describes a method for adding a low-end ADC to a single programmable-logic I/O pin. The circuit charges a capacitor through a resistor while measuring the time to charge the capacitor to a certain voltage.

Before each measurement, the capacitor discharges to 0V. A single I/O pin can perform both the dis-

charging and the timing. For an FPGA or a PLD, you can perform a discharge by setting the I/O as an output pin and forcing a zero at that pin. You can charge the capacitor by setting the I/O as an input pin, which gives it a high impedance. The capacitor charges through the potentiometer (**Figure 1**). Meanwhile, a counter starts, and the CPLD monitors the input voltage. As soon as the capacitor voltage reaches the threshold, the counter stops at a value that is a measure of the charging time. The charging time or counter value relates to the clock frequency, the value of the resistor, the value of the capacitor, and the input threshold voltage:

$$V_{TH} = V_{DD} \times \left(1 - e^{\frac{-t}{R \times C}}\right)$$

$$T = \frac{COUNTERVALUE}{f_{CLK}}$$

$$COUNTERVALUE = -f_{CLK} \times R \times C \times \ln\left(1 - \frac{V_{TH}}{V_{DD}}\right).$$

If you assume that the capacitor value, the input threshold voltage, and the clock frequency remain fairly constant over the operating range, the charging time is linearly dependent on the value of the resistor. If you replace the resistor with a potentiometer, a counter value depends on the potentiometer position. The application uses a Xilinx (www.xilinx.com) XC9500 XL CPLD (**Figure 2**). The I/O, which VHDL (very-high-speed-IC hardware-description language) declares as a tristate buffer, first shorts the capacitor. Hardware limits the output short-circuit current of the I/O pins to ±10 mA, so the capacitor's shorting should last long enough to guarantee a full discharge. You can calculate the minimum shorting time using the capacitor value, short-circuit current, and discharge voltage, assuming that the threshold voltage must discharge from the capacitor:

Figure 2 The application uses a Xilinx XC9500 XL CPLD.

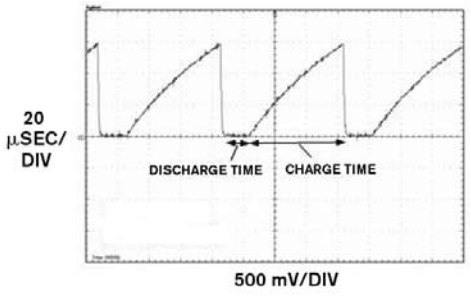

Figure 3 In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor.

$$t_{DISCMIN} = V_{THRESHOLD} \times \frac{C}{I_{SHORT}}.$$

The discharge delay can be realized with a small counter. After the discharge time, the I/O pin acts as an input, which causes the capacitor to charge through a pullup potentiometer. Meanwhile, the internal counter starts. When the capacitor voltage reaches the input threshold voltage, the counter stops. Eight LEDs show the 8-bit value. In this application, a 10-kΩ potentiometer in series with a 1-kΩ resistor charges a 22-nF capacitor. The input clock of the PLD is 1.8432 MHz. The input threshold is 1.5V at a supply of 3.3V. This arrangement allows a measurement range between a counter value of 25 and 270, equivalent to a resolution of almost 8 bits. **Figure 3** shows the capacitor charging/discharging waveform.

Every IC's I/O pin has a certain bias sink or source current, causing a voltage drop over the charging resistor. This situation limits the charge voltage to $V_{DD} - R_{CHARGE} \times I_{BIAS}$. In other words, if the charging resistance is too large, the capacitor doesn't charge above the input-pin threshold voltage, stopping the circuit's operation. Similar applications for microcontrollers or PLDs (**references 1** through **5**) include adding multiple inputs to a single I/O pin and using a different pullup-resistor value for each input. By discriminating the charging times for each resistor, the PLD can decide which resistor or combination of resistors the user has actuated.

Another application for microcontrollers is temperature measurement. By replacing the pullup resistor with a PTC (positive-temperature-coefficient) or an NTC (negative-temperature-coefficient) resistor, you can derive the temperature from the charging time after calibration. You can also use these devices to make true analog-to-digital measurements. By replacing the pullup resistor with a voltage-controlled current source, an input-voltage change causes a linear change in the charging time, providing a real analog-to-digital conversion. EDN

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Use two phases to cut current and improve EMI

Goran Perica, Linear Technology, Milpitas, CA

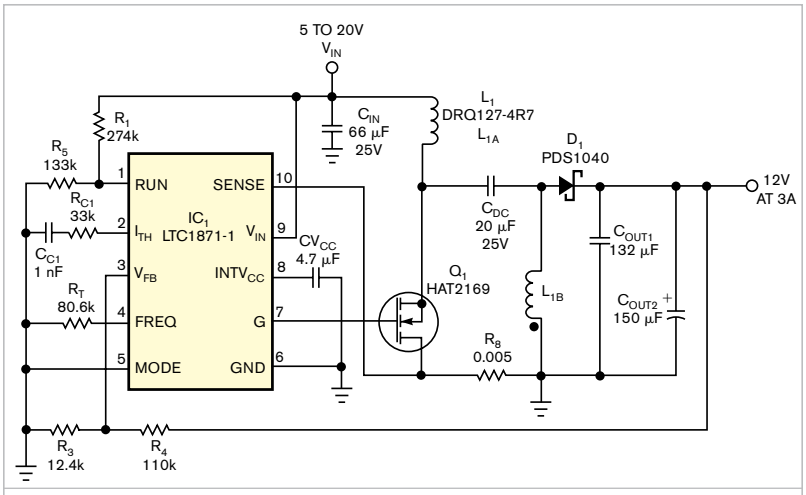

Figure 1 A single-phase SEPIC has low input ripple currents and is suitable for power levels of 5 to 50W.

In dc/dc-converter applications in which the input voltage may be lower or higher than the output voltage, you can use either a flyback converter or a SEPIC (single-ended-primary-inductor converter). SEPICs offer lower input-current ripple and higher efficiency than do flyback designs. Both converters suffer from relatively high output-current ripple, especially at high load currents and low input voltages. As output-current ripple increases, so does the circuit's output-filter-capacitance requirement, which increases size and cost. You can reduce output-current and -voltage ripple without increasing the application size and cost by using a multiphase SEPIC or flyback converter. Using a multiphase flyback circuit also greatly reduces the input-current ripple.

To evaluate the benefits of a dual-phase versus a single-phase SEPIC, this Design Idea compares two designs running at 300-kHz switching frequency. For consistency, both examples use the same power components, resulting in twice the output power in the two-phase design.

The single-phase SEPIC circuit can generate 3A of output current (**Figure 1**). SEPICs are typically 1 to 2% more efficient than flyback converters. **Figure 2** shows the output diode's current (bottom trace) at minimum input voltage and maximum load and the output-voltage ripple (top trace). The circuit's output capacitors must handle the peak output-diode current of 14A. Even though the circuit uses four low ESR (equivalent-series-resistance) output capacitors, output-voltage ripple is still 110 mV p-p. The aluminum output capacitor, C_{OUT2}, doesn't help much in reducing the output ripple due to its much higher ESR. C_{OUT2} mainly helps reduce load transients by adding bulk capacitance to the output rail.

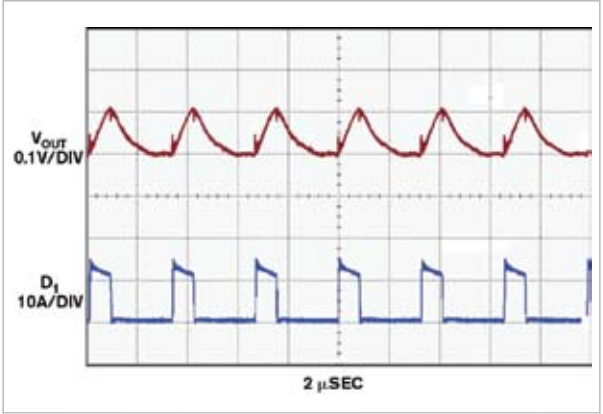

Figure 2 The single-phase circuit in Figure 1 has a peak capacitor output current of about 14A (bottom trace).

Figure 3 (pg 52) shows a two-phase converter, which is similar to the single-phase converter in **Figure 1** except for the addition of an identical second-phase power stage. The second phase halves the peak inductor, MOSFET, and output-diode currents. The 50% lower peak output-diode currents produce 50% lower output ripple (**Figure 4**, pg 52). Also, the output-ripple-current frequency doubles, thus making it easier to filter out with an additional LC filter if necessary.

The benefits of using a dual-phase converter become clear when you consider output-capacitor ripple current (**Figure 5**, pg 52). The two-phase converter's output-capacitor ripple current is always lower than that of an equivalent single-phase converter. Depending on the duty cycle, the two-phase converter's output-capacitor ripple current can approach 0A at a 50% duty cycle. Inductor ripple current is still present, and you can reduce it by using larger inductors.

Using a two-phase converter means that you can use smaller inductors, MOSFETs, output diodes, and output capacitors than you can use in an equivalent single-phase converter. Because high-power designs may need to use more than one MOSFET anyway, a dual-phase design may need only one additional smaller inductor and one smaller diode. Output LC filters can also be smaller because of the doubling of the output ripple frequency. Finally, the EMI performance of a dual-phase SEPIC should be better than that of a single-phase converter because of lower current slew rates and smaller current loops. EDN

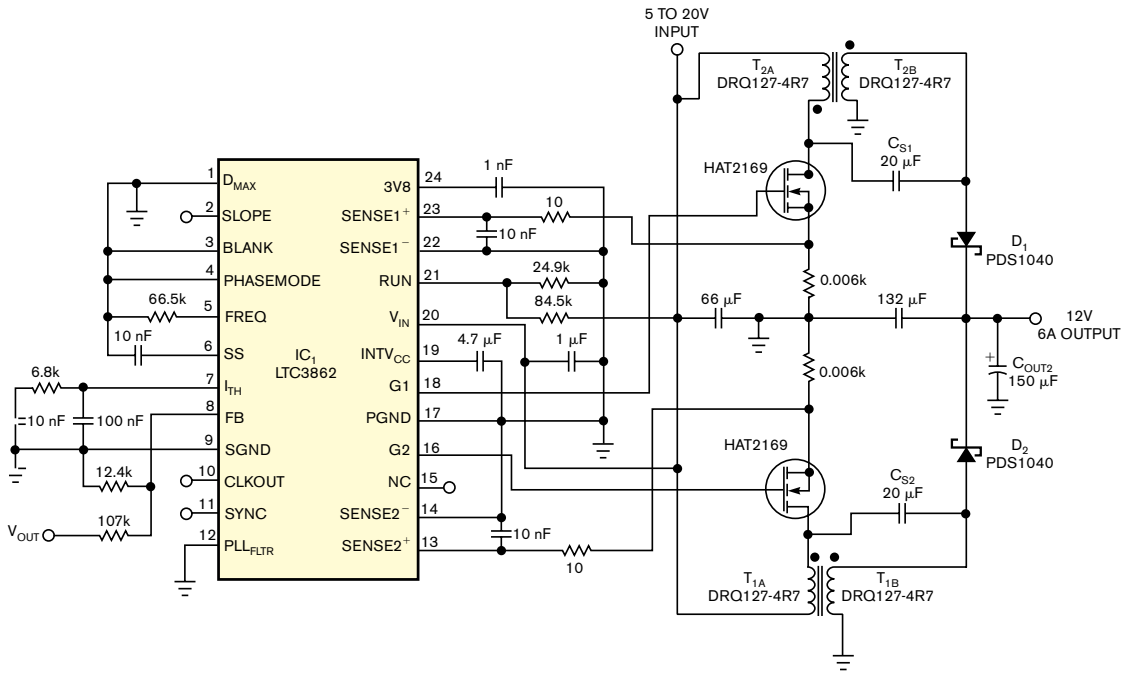

Figure 3 By adding second power stage and shifting the phase by 180°, you can reduce the output ripple currents by more than 50%.

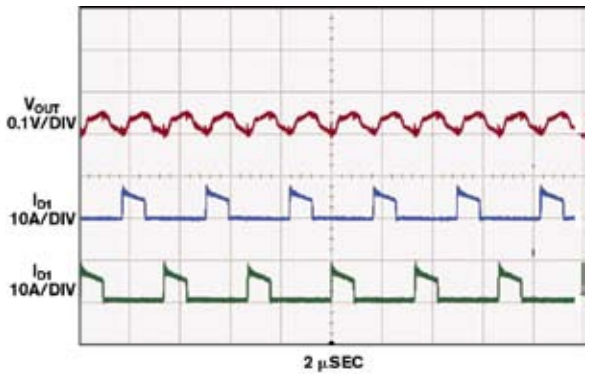

Figure 4 The output ripple current is 50% lower for a two-phase SEPIC. The output ripple voltage is 50% lower than that of a single-phase design with the same output capacitors.

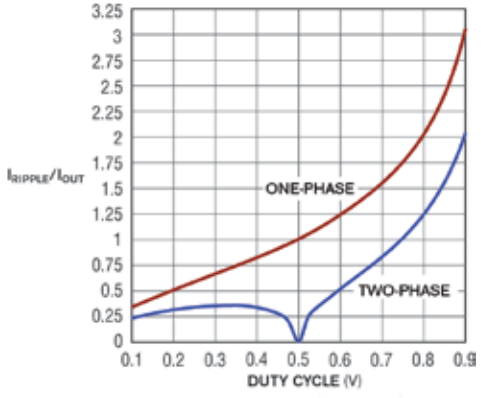

Figure 5 The normalized output-capacitor ripple current for single- and dual-phase SEPICs shows lower output ripple with a two-phase design.

Fader switch uses inexpensive controller

William Grill, Lenexa, KS

Customizing a model or a simulator with a bit of illumination is a nice touch. Rather than a simple on or off, you can add a touch of both refinement and control to your display with fading light. Employing a Microchip (www.microchip.com) 10F20x microcontroller, the circuit in **Figure 1** provides dual-rate fader control for a push-on/push-off switch, a momentary pushbutton switch, or a simple on/off SPST (single-pole/single-throw) switch. The circuit monitors and debounces the switch and generates a multiple-cycle, 470-Hz, PWM (pulse-width-modulated) output to drive LEDs or incandescent lamps. The circuit includes a MAX16823 (www.maxim-ic.com) IC that drives multiple LEDs.

The microcontroller produces 64 linear steps of a PWM signal between 0 and 100% duty cycle. The controller maintains each pulse width for a variable number of cycles employing a table in the assembly code (**Listing 1**,

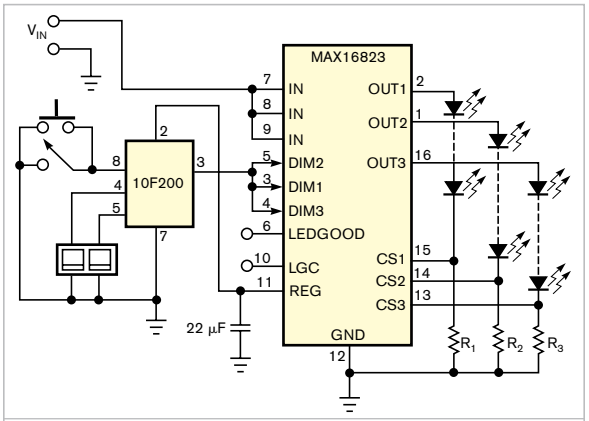

Figure 1 A microcontroller provides pulses with adjustable widths to create fading in LEDs.

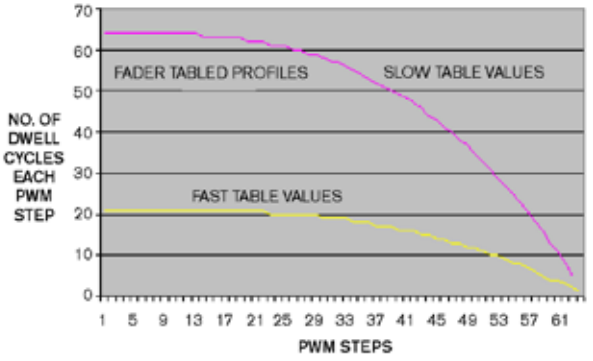

Figure 2 A table in the microcontroller code lets you run fast- or slow-fading profiles.

which you can download at the online version of this Design Idea at www.edn.com/091112dia). You can modify the code to build profiles of LEDs or incandescent lamps by applying a settable dwell time to each PWM step. The code contains two tables to set fast- and slow-fade characteristics. The fade values provide a cubed index that produces a 3-to-1 fade ratio (**Figure 2**). Using the final state of the output at Pin 3 of the 10F200, you access the tabled number of dwell cycles from the first table entry to the last for a high final state or from the last entry to the first to arrive at the final low state.

Fade-transition timing is user-selectable for either a 3- or a 9-second period. The circuit periodically samples both the fade rate and button or switch mode, allowing you to multiplex the design or use it in multiple configurations. The mode control is on Pin 5 of the controller, and the rate control is on Pin 4. The application exploits the controller's internal 4-MHz clock and the configurable pullup resistors on the monitored inputs. A prototype of the circuit uses a 10F20x in an eight-pin DIP, but the controller is also available in a smaller SOT-23 package. EDN

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READERS SOLVE DESIGN PROBLEMS

Inspect solar cells without a microscope

Chun-Fu Lin and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

Solar cells convert light energy into electricity, making them a renewable energy source. Solar-cell manufacturers often use SEMs (scanning electron microscopes) to detect defects in solar cells while they're still in wafer form. Although SEMs can see down to a solar cell's grain structure, they can be slow because their scan area is small. A SEM must scan a wafer many times to cover it.

Instead of using a SEM, you can use an SWIR (shortwave-infrared) camera system to detect defective cells. You can take advantage of a solar cell's electroluminescence signature to find defects on a solar cell. A cell's light has a wavelength of about 1.1 micron, which results when you apply a forward bias voltage and forward operating current of at least 7A to the cell. An SWIR sensor can provide an image of an entire wafer, eliminating the need to scan the wafer. The sensor identifies defects by detecting a wafer's electroluminescence.

Figure 1 shows the system, which uses an SWIR sensor that converts an image into an analog voltage. A preamplifer boosts the signal to a level sufficient for an ADC in a digital-processing module to digitize the analog signal at 10M samples/sec.

The ADC's digital output travels through an LVDS (low-voltage-differential-signaling) data interface to a Dalsa (www.dalsa.com) frame-grabber card in a computer. Custom image-processing software, written in C++, processes the data, producing an image of the entire wafer on the computer's screen.

The board containing the sensor, preamplifier, and ADC also has a microcontroller, which generates a clock signal for the timing of the sensor and the ADC. An RS-232 communica-

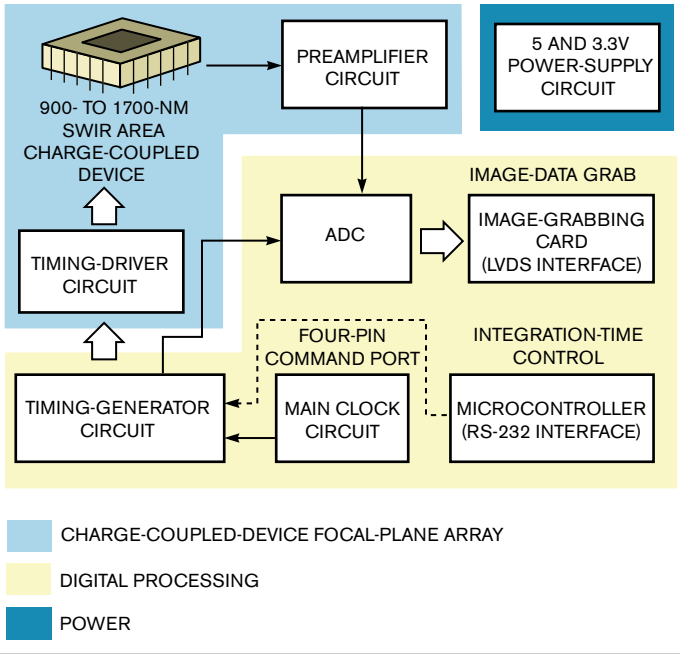

Figure 1 An ADC digitizes an analog signal from an SWIR sensor and sends the signal to a frame grabber for processing.

DIs Inside

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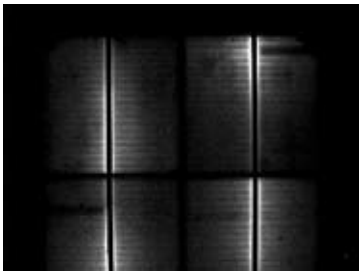


Figure 2 An electroluminescence image of solar cells shows dark areas that indicate failed cells.

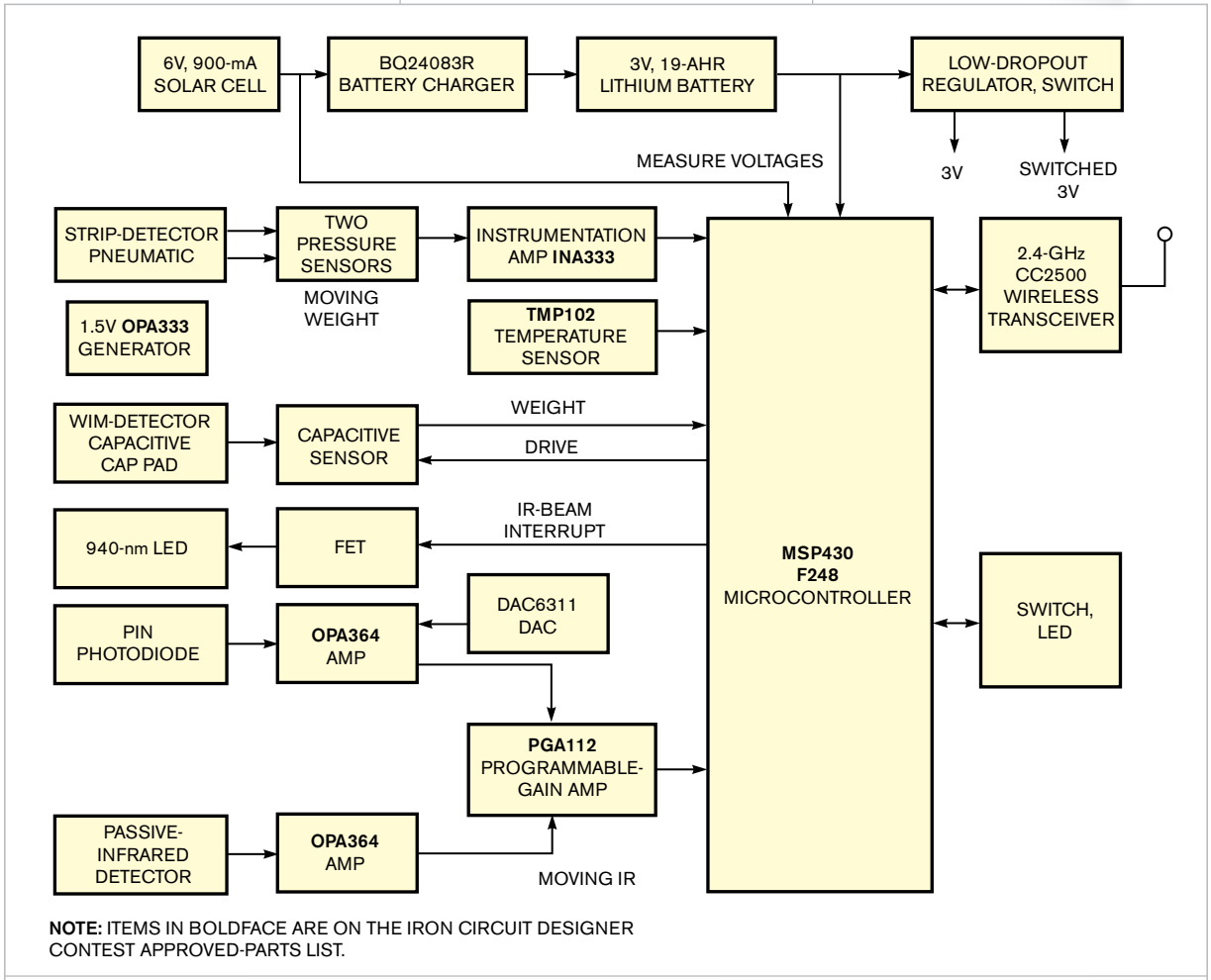
tions port on the Atmel (www.atmel.com) microcontroller allows it to communicate with a PC to get commands from the user who set parameters such as the SWIR sensor's operating mode. A timing-driver circuit sends the clock signal to the SWIR sensor.

Figure 2 shows the image from the SWIR camera circuit. This image shows the intensity distribution of the cell's light output. A homogenous intensity-distribution image is essential for a high-quality solar cell, but solar cells always show some inconsistencies. All defects resulting in a local reduction of the carrier concentration are visible on the electroluminescence image as dark bars. EDN

Solar-powered sensor controls traffic

Larry K Baxter, Capsense, Lexington, MA

Have you ever sat in your car waiting for the light to turn green when nobody's using the cross street? This wait is due to the fact that the sensors controlling these traffic signals—in one large-suitcase-sized box per intersection—are classically dumb, with relays, cams, and switches, although they now may include software that accepts data from local sensors, automobile-sized inductive loops buried in the asphalt. Modern controllers have gained some intelligence. For example, they may share



NOTE: ITEMS IN BOLDFACE ARE ON THE IRON CIRCUIT DESIGNER CONTEST APPROVED-PARTS LIST.

Figure 1 Most of the circuit amplifies outputs from four sensors, digitizes them with the MSP430's 12-bit ADC, does some preprocessing, and messages the controller.

data with nearby intersections, respond to radio requests from emergency vehicles, and sometimes take commands from a traffic-control center. This Design Idea describes the TSP (traffic-sensor post), a more accurate, effective, inexpensive, and easy-to-install approach to monitoring traffic flow. These sensors measure vehicle location and speed in four or more streets at an intersection or at a distance from the intersection for early warning. A second application of this technology, the WIM (weight-in-motion) sensor, weighs moving trucks.

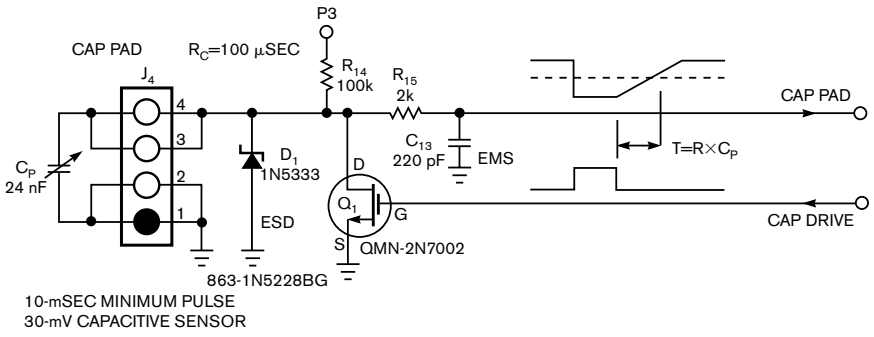


Figure 2 The Cap Pad sensor has a nominal capacitance of about 24 nF at rest, with a change of about 7% full-scale when a truck passes.

The circuit comprises a wireless, solar-powered sensor array that handles all the data collection at an intersection (**Figure 1**). Cities can install these sensors at each of the four corners of an intersection for full coverage. The sensors send data to the single controller box over IEEE 802.15.4 in a star network. The approach combines four sensors in an inexpensive, low-maintenance, 6-in.-diameter, 6-foot-tall post. You can build the circuit into the post that holds the traffic lights, or you can use it stand-alone. Not all TSPs require all four sensors; you can select those that your application needs based on usage. The TSP is the first wireless approach to this problem, and one of the sensors, the Cap Pad, provides a huge advantage over current expensive and inaccurate WIM sensors (**Figure 2**).

The TSP uses a PIR (passive-infrared) sensor that looks 10 microns into the deep-IR band for moving IR sources. This technology finds use in inexpensive motion-detecting lamp controls and senses vehicles from 30 feet away. The detection range is good, the parts are cheap, and the beam can see through a layer of dirt. It can't measure speed, distance, or direction.

The TSP also uses conventional pneumatic tubes. Rubber tubes are stapled to the asphalt and feed two pressure sensors. This approach accurately measures speed, but permanent installations cannot use it because it gets damaged easily. Municipalities often deploy pneumatic tubes to measure traffic volume in road construction.

The Cap Pad comprises a 10-in.×12-foot sandwich of three 0.05-in.-thick stainless-steel sheets separated by two 0.05-in.-diameter closed-cell urethane-foam layers (**Figure 3**). You capacitively measure the 0.025-in. deflection of the pad under a truck's tire to weigh the axle. One Cap Pad can handle the WIM requirements, and using two can add speed and direction information. You use multiple pads to handle multilane roads. The Cap Pad can be fastened to the asphalt with adhesive or pavement tape or buried under as much as an inch of asphalt for protection. Its materials cost is only a couple hundred dollars, a huge saving over the piezoelectric WIM sensors currently in use.

The TSP also uses a near-IR transmitter/receiver using a pulsed LED for transmission and a PIN (positive-intrinsic-negative) photodiode for reception. Both need cylindrical lenses to focus the beam to a 2°-wide, 5°-high ellipse that covers a remote retroreflective screen, as in highway signs, or to the IR sensors on another TSP. A multilayer optical bandpass filter that removes visible light further improves the range.

Precision capacitive sensors can measure an air gap between adjacent metal plates to subnanometer accuracy. Unfortunately, accuracy in the WIM application requires flat and parallel surfaces, and the Cap Pad has neither. Capacitive sensors can also accurately measure a force on adjacent flat plates with a restoring spring, but flatness and parallelism are still requirements. Maintaining parallelism over a 10-in. pad would be difficult, and roads are seldom flat.

If compression of the air pockets in closed-cell foam provides the restoring force, however, the resulting spring constant changes from the conventional F=K×x of springs or cantilevered beams to F=P0×H/(H−x), where F is force, P0 is atmospheric pressure, H is the starting gap, and x is the dis-

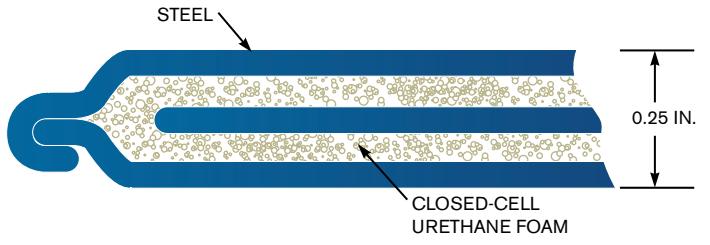


Figure 3 The Cap Pad sensor is a 10-in.×12-foot sandwich of three 0.05-in.-thick stainless-steel sheets separated by two 0.05-in.-diameter closed-cell urethane-foam layers.

placement. The result of this **equation** is that the capacitance of the pad varies linearly with applied force, and the surfaces of the Cap Pad no longer need to be parallel or flat. It accurately measures a force regardless of its size.

Most of the circuit amplifies outputs from the four sensors, digitizes them with the MSP430's 12 bit-ADC, does some preprocessing, and messages the controller. The 6V solar panel, 40 IXYS (www.ixys.com) solar cells in series, charges a 19-Ahr, 3V, lithium-polymer battery through IC_1. Low-dropout regulator/switch IC_2 regulates battery output at 3V. The battery generates more than 4V at full charge and 3.2V at the end of charge, and the low-dropout regulator at 42 mA generates only 50 mV. IC_2 also switches active-mode 3V power.

The road-strip sensor senses the 0.1- to 1-psi pulse when a car drives over the pneumatic tubes. A 400Ω silicon bridge sensor differentially outputs approximately 50 mV. Instrumentation amplifiers IC_3 and IC_4 boost the output to a few volts. The pressure sensor, as well as the Cap Pad and the PIN sensor, has a quiescent level with no traffic. A timer detects the no-traffic state and stores this level in RAM, updating every second to follow slow offset drifts from environmental factors, so sensor offset accuracy is not critical. The pressure sensor's scale accuracy—at approximately 30%—is relatively uncritical, but the Cap Pad's scale accuracy should be a few percentage points or less. All sensors must have good resolution.

IC_5 handles accurate temperature measurements, which are necessary for the Cap Pad, whose temperature dependence results from the elastic modulus change of polyurethane. The Cap Pad has a nominal capacitance of about 24 nF at rest, with a change of approximately 7% full-scale when a truck passes. The Cap Drive pulse discharges this capacitance at a 700-Hz rate, and a 100-kΩ resistor charges it to 3V with a 240-µsec time constant. A timer times the number of pulses it takes to cross the internal $V_{DD}/2$ reference using the internal comparator, and, because you can clock the timer at 12 MHz, the resolution is 1%. You can get increased resolution by timing out the nominal quiescent pulse width and capturing the pulse's level at that point with the 12-bit ADC.

The Cap Pad's sandwich construction shields the active element from electromagnetic interference, but a 3W zener diode cleans up any remnant lightning strokes. The IR LED drive is a 20-to-1 current mirror to handle LED voltage variation. A DAC handles the PIN photodetector's offset because the extreme night-to-day dynamic range would overrange the 12-bit DAC. The PIR sensor turns moving deep-IR targets into bipolar millivolt voltage pulses with its special segmented lens and dual-element pyroelectric detector. A PGA (programmable-gain amplifier) selects and variably amplifies the PIR sensor's signal and the PIN signal. The timer uses standard connections.

For a power budget, more schematics, and more details of this circuit, see the Web version of this article at www.edn.com/091126dia. EDN

Self-oscillating H bridge lights white LED from one cell

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

You can build a self-oscillating H bridge by replacing the pull-up collector resistors of a classical BJT (bipolar-junction-transistor) astable multivibrator with PNP BJTs (**Figure 1**). Because this circuit oscillates at supply voltages as low as 0.6V, you can use it in general low-voltage, low-power push-pull applications. You can, for example, drive a diode-capacitor charge pump to generate negative supply voltage in battery-powered systems. This Design Idea shows how to use it to light a white LED from one cell without an inductor.

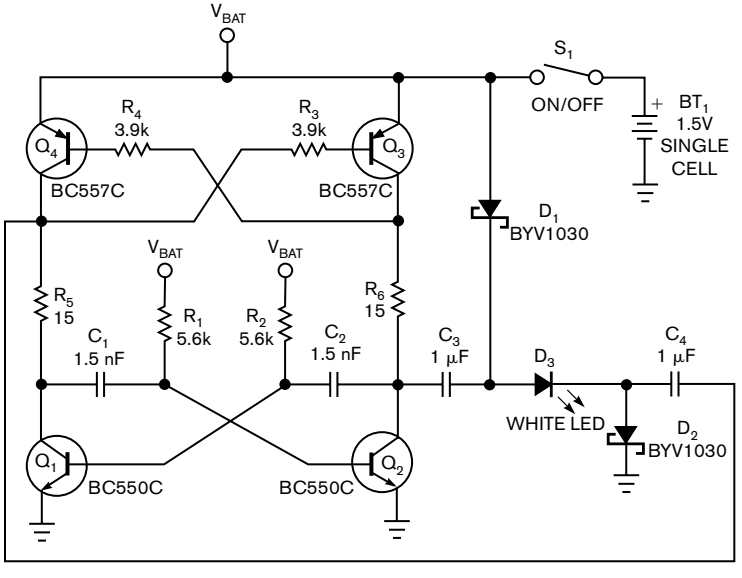


Figure 1 Resistors R_1 and R_2 and capacitors C_1 and C_2 set the oscillation frequency.

Transistors Q_1, Q_2, Q_3, and Q_4 form the H bridge, which acts as a simple charge-pump converter and requires only two small, inexpensive ceramic capacitors, C_3 and C_4, to perform its function. When Q_2 and Q_4 are on, capacitors C_3 and C_4 charge to the battery voltage through forward-biased Schottky diodes D_1 and D_2. When Q_1 and Q_3 are on, they discharge the capacitors through resistors R_5 and R_6 and the LED. Because this process repeats at a high rate of speed, the LED appears always on.

The circuit oscillates with a frequency based on time constants R_1C_1 and R_2C_2. During discharge, the voltage that develops across resistors R_5 and R_6 and the LED remains approximately constant because of the high switching frequency. The measured value, for a nominal 1.5V battery voltage, is 3.8V—enough to drive a white LED with a forward voltage of 3 to 3.5V. Resistors R_5 and R_6 set the LED's peak current and limit the possible current spikes that a push-pull output stage can produce.

Choosing the astable oscillator's frequency involves a trade-off between the time necessary to charge capacitors C_3 and C_4 and the need to reduce their discharge. For a given capacitance value of C_3 and C_4, you must experiment to find the optimum frequency. With the component values in **Figure 1**, the frequency and the duty cycle are about 66 kHz and 50%, respectively, and the LED's drive current is a square-wave signal with 20-mA peak value and 10-mA average value. The LED dims gradually as the battery voltage decreases, and the LED is off when the battery voltage falls below 0.9V. For high efficiency, use small-signal transistors with high dc current gain and low collector-to-emitter saturation voltage. Note that the circuit can drive any type of LED; in this case, you should increase current-limiting resistors R_6 and R_5 to achieve the LED-drive current your application requires. EDN

Low-cost LCD-bias generator uses main microcontroller as control IC

Tom Hughes, Dannemora, Auckland, New Zealand

LCD circuits often require a −10V voltage at 2 to 15 mA to bias a graphics-LCD-driver IC. You can usually accomplish this task with an external charge-pump IC, such as Maxim's (www.maxim-ic.com) ICL7660, but that approach adds cost to the design. Instead, you can control a buck-boost switch-mode regulator using the same microcontroller that sends data to the LCD. In addition, you can sequence the power rails under software control, as some types of LCD controllers require.

The circuit includes IC_1, an Atmel (www.atmel.com) Attiny15 microcontroller (**Figure 1**), which provides regulation with 200-mV-p-p ripple at a 30-mA load current when supplying −10V. **Listing 1**, which is available in the online version of this Design Idea at www.edn.com/091126dib, lets you download the source code, which uses only 4.8% of the total CPU time to achieve the stated regulation, even with a relatively low-speed clock frequency of 1.6 MHz.

To minimize CPU time, the software uses the 8-bit on-chip PWM (pulse-width modulator) to drive Q_1. With the on-chip ADC in free-running mode, the microcontroller generates a hardware interrupt with a period of 7.69 kHz. The interrupts have one drawback: If they stop, the circuit can go out of regulation. Thus, you must take care when using interrupts with long processing times. The Attiny15 uses an on-chip, 16× PLL (phase-locked loop) to drive the PWM timer. You can achieve a PWM carrier frequency of 100 kHz, which allows the use of a relatively low-capacitance filter capacitor, C_1.

Two constants in the source code let you alter the bias voltage of the circuit's output voltage. These constants employ basic buck-boost-converter theory (**Reference 1**). The following **equation** defines the maximum 8-bit constant, or threshold, that the ADC reads on the chip: $51.2\times\{V_{CC}-[(V_{CC}-V_{MAX})/(R_4+R_5)]R_5\}$, where V_{MAX} is the maximum desired output voltage and V_{CC} is the supply voltage. To achieve optimum operation, increase the PWM signal's duty cycle when you need higher voltages. Use the following **equation** to determine the 8-bit PWM's value: $255-V_{OUT}/(V_{OUT}-V_{IN})\times 255$, where V_{OUT} and V_{IN} are the output and input voltages, respectively. In practice, however, if you keep the current at less than 2 mA, this requirement is less important.

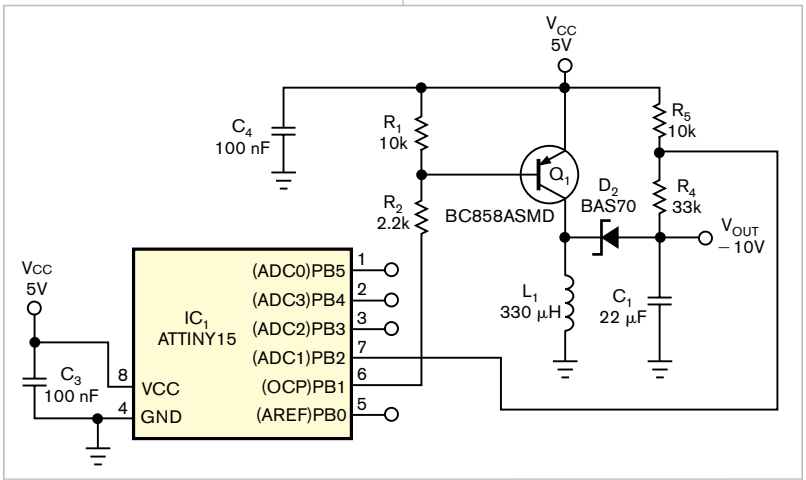


Figure 1 An Attiny15 microcontroller provides regulation with 200-mV-p-p ripple at a 30-mA load current when supplying −10V.

The circuit can deliver currents that Q_1's collector current predominantly delivers. This current is the peak output current that the circuit can safely deliver. The following **equation** calculates the current: $I_{OUTMAX}=(V_{IN}\times 0.08)/V_{OUT}$, where I_{OUTMAX} is the maximum output current. If your design needs higher current, then substitute a BC327 for Q_1. Additionally, the inductor should have a maximum rms (root-mean-square) current value of at least twice the peak output current and preferably be a low-ESR (equivalent-series-resistance) type to maximize circuit efficiency. EDN

REFERENCE

1 Hart, Daniel W, *Introduction to Power Electronics*, First Edition, pg 202, Prentice Hall, Oct 25, 1996, ISBN-10: 0023511826, ISBN-13: 978-0023511820.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Precision tilt/fall detector consumes less than 1.5 mW

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When you need to detect angular position related to Earth's gravity, you can use an Analog Devices (www.analog.com) three-axis MEMS (microelectromechanical-system) accelerometer. The ADXL335 has three analog outputs that correspond to the X, Y, and Z axes of an orthogonal coordinate system (**Reference 1**). Because the Z axis is perpendicular to the footprint, or base, of the MEMS IC's package surface, you can use the accelerometer to detect tilt if you mount it on a PCB (printed-circuit board) that's parallel to your product's base. The circuit in **Figure 1** lets you detect whether the tilt exceeds a preset limit. A digital output, in this example, drives an LED, but you can connect the signal to a microcontroller or another device.

When you orient the accelerometer IC horizontally relative to Earth, the LED is on. Whenever the Z axis of the device declines by a specific value, α_T, of the angle, α, from the vertical direction, the LED turns off. The voltage difference at the Z-axis output, Z_{OUT}, of the accelerometer, referenced to the power supply's midvoltage, $V_S/2$, is $V_{GZ}=V_G\cos\alpha$, where V_S is the power-supply voltage, V_{GZ} is the voltage at the Z_{OUT} pin, and V_G is the terrestrial full-scale voltage. When the power-supply voltage is 3V, the terrestrial full-scale voltage is either 300 or −300 mV, depending on whether you ori-

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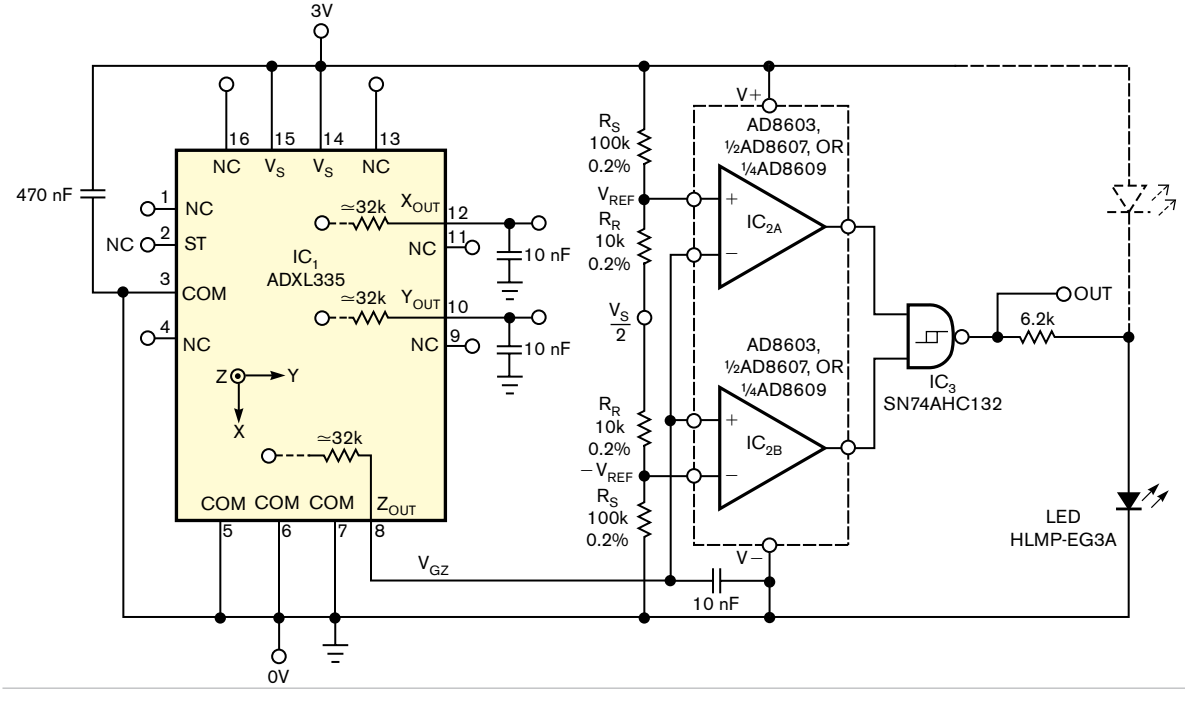

Figure 1 The tilt on MEMS accelerometer IC_1 produces a voltage, V_{GZ}. When compared with V_{REF} and $-V_{REF}$, V_{GZ} produces a digital output at the NAND gate.

ent the detector from the top down or from the bottom up. Op amp IC_2 compares the voltage at the Z_{OUT} pin to the reference voltage, V_{REF}. If the positive voltage at the Z_{OUT} pin is equal to or lower than the reference voltage, the output of IC_{2A} goes high, and the output of IC_{2B} remains high (**Reference 2**). Thus, the output of NAND gate IC_3 becomes low, and the LED turns off. You can calculate the threshold tilt angle, α_T, at which this action occurs from the **equation** $\cos\alpha_T=(V_{REF}/V_G)$.

Resistors R_S and R_R set the voltage reference to 136.36 mV. Thus, the threshold tilt angle is 62.96°. Similarly, when the negative voltage at the Z_{OUT} pin becomes lower in magnitude than the negative reference voltage, it indicates a tilt of 62.96° or more, the output of IC_{2B} goes high, and the LED (**Reference 3**) also turns off. Theoretically, you can choose any other threshold angle within the interval of 0 to 90°. The practical limits with the 10-nF filtering capacitor, however, are 21.23 and 86.10°. The probability of a short-term false detection is 8×10^{-5}. From the properties of the cosine function, the sensitivity of the tilt detector rises with rising tilt angle. To select another value of tilt within this interval, you calculate the appropriate reference voltage from the **equation** $\cos\alpha_T=(V_{REF}/V_G)$ and then change the value of the R_R resistors as necessary.

Gravity causes a voltage difference at the Z_{OUT} pin of IC_1. The circuit detects

THE DETECTOR'S OPERATION IS VIRTUALLY INSENSITIVE TO POWER-SUPPLY VARIATIONS.

fall on the loss of this gravity-induced voltage difference within "free fall"—moving bodies with no acceleration other than that provided by gravity. If the circuit is fixed to such a body while the Z axis of IC_1 is pointing roughly vertically, the free fall manifests itself as almost fully disappearing within the 300- or −300-mV voltage excursion at Z_{OUT}. When the voltage remains close to the power supply's midvoltage, the voltage at Z_{OUT} is 1.5V. The threshold of detecting the free fall in this case is an apparent decrease in gravity to 0.4545g.

The probability that the noise's peak value will achieve this threshold value is practically zero for "heavy" bodies. The probability that the noise's peak value will achieve 0.0679g is fairly low, and it decreases vastly when you elevate the decision level. An apparent decrease in gravity within the free fall causes a low-to-high transition at the output of either IC_{2A} or IC_{2B}, depending on whether the Z axis is close to parallel or antiparallel to vertical. The outputs of both IC_{2A} and IC_{2B} remain at a high state. Thus, in both orientations, the output of the NAND gate goes low, and the LED turns off.

The sensitivity of IC_1 is essentially ratiometric. The resistive voltage divider R_S/R_R derives the positive and the negative reference voltages, which are inherently ratiometric. Thus, the detector's operation is virtually insensitive to power-supply variations. Note that the NAND gate has an internal Schmitt trigger at its inputs, and its logic output therefore fulfills industrial-grade requirements, including duration of the logic-state transitions of no more than 10 nsec regardless of the slope of the detected signal when crossing the threshold. If you need a complementary on/off indication, you can reconfigure the circuit by another position of the LED (dashed lines in **Figure 1**). EDN

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Reset an SOC only when power is ready

Goh Ban Hok, Lantiq Asia Pacific Pte Ltd, Singapore

An SOC (system on chip) normally requires two power supplies—one for the core supply and the other for the I/O. To properly power up the chip, you need to get one of the power supplies ready before the other, according to the SOC's power-sequence requirement. Normally, the core voltage must power up first, and the I/O voltage powers up second. Instead of direct control of the power supplies, you can control the system reset to achieve a similar goal. **Figure 1** shows the reset-conditioning circuit that can accomplish this task. In this circuit, the core voltage is 1.8V, and the I/O voltage is 3.3V. The reset-SOC signal produces a logic high when the core voltage gets ready before the I/O voltage. When the I/O voltage powers up first, the reset signal resets the SOC chip only after the core voltage powers up.

Comparator IC_1 monitors both voltages. It operates on the 3.3V I/O-supply voltage. Resistor R_2 and variable resistor R_1 form a voltage divider that lets you set the required voltage based on the core voltage. In this case, the reference voltage is 1.65V at Pin 3. Pushbutton switch S_1 provides a hard reset of the SOC.

In **Figure 2**, the core voltage (Trace A) powers up first, and the I/O voltage (Trace B) follows. Com-

parator IC_1 remains inactive until the I/O voltage activates. When the I/O voltage turns on, comparator IC_1 and AND gate IC_{2A} operate. As the voltage at IC_1's Pin 2 is higher than that of Pin 3, the comparator produces a high at Pin 7, which pulls up through R_5.

The reset signal at IC_{2A}'s Pin 1 (Trace C) initially remains at zero and starts to charge capacitor C_1 to the I/O voltage through R_6. Depending on your application, you can adjust the RC time constant to suit your needs. The reset-in signal goes high after C_1 charges to the logic-high level, which produces a logic-high signal at Pin 3 (Trace D), resetting the SOC.

In **Figure 3**, the I/O voltage (Trace B) powers up first, and the core voltage (Trace A) follows. The core voltage powers up after the R_6/C_1 time constant. When the core voltage is 0V, the comparator voltage at Pin 3 is higher than it is at Pin 2. Thus, the comparator produces a logic low at Pin 7. Pin 1 of AND gate IC_{2A} remains high after the I/O voltage charges capacitor C_1. The reset-out signal remains at zero state because the core voltage is not yet present. When the core voltage comes up, the voltage at comparator IC_1's Pin 2 is higher than that of the threshold voltage at Pin 3. Thus, the comparator output's Pin 7 goes high. As reset remains high, the reset SOC of AND gate IC_2 goes high after a propagation delay. This action resets the SOC.

THE RESET-OUT SIGNAL REMAINS AT ZERO STATE BECAUSE THE CORE VOLTAGE IS NOT YET PRESENT.

In **Figure 4**, the I/O voltage (Trace B) powers on first, and the core voltage (Trace A) follows. This case is similar to that in **Figure 3** except that the core voltage powers up faster than the R_6/C_1 time constant. The comparator's IC_1 output, Pin 7, goes high when the core voltage turns on, and the voltage at Pin 2 crosses the threshold of 1.65V that resistor divider R_1/R_2 sets. However, the output reset's SOC signal goes high only when capacitor C_1 charges to the logic-high level. AND gate IC_{2A} then produces a high signal to reset the SOC. EDN

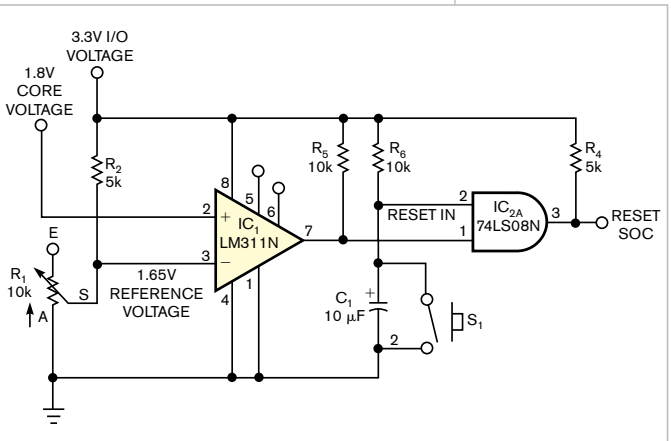

Figure 1 This circuit for reset conditioning uses a comparator and an AND gate.

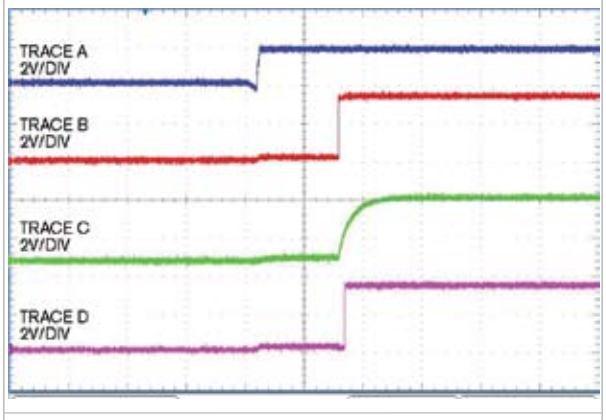

Figure 2 When the core voltage (Trace A) powers up before the I/O voltage (Trace B), the reset signal (Trace D) waits for the capacitor to charge.

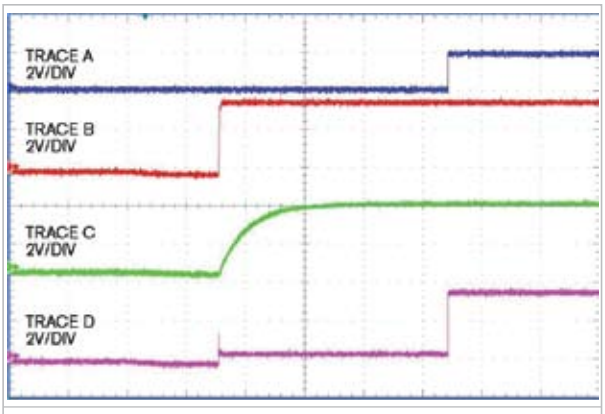

Figure 3 When the core voltage (Trace A) is late, the reset-SOC signal (Trace D) remains low.

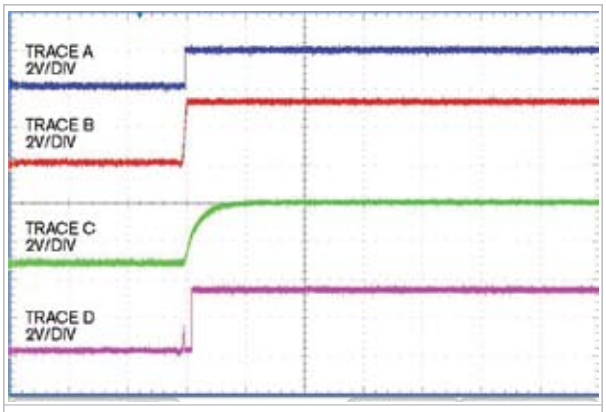

Figure 4 The reset signal (Trace D) goes high after both voltages come up and the capacitor charges.

Circuit provides simpler power-supply-sequence testing

Dan Karmann, DLK Engineering, Thornton, CO

A previous Design Idea (**Reference 1**) describes a three-IC control circuit for testing the power sequencing of an SOC (system on chip). Although that circuit lets you control the power-on sequence of two linear power supplies, it uses one eight-pin IC, two 14-pin ICs, several discrete components, and a DPDT (double-pole/double-throw) switch for the control. Replacing most of those components with an inexpensive, eight-pin microcontroller simplifies power-supply-sequencing control because the approach requires less wiring for component interconnections. The approach is also more versatile because it involves only simple changes to the controlling firmware. The simplicity and versatility come at approximately the same component cost.

A disadvantage of this circuit compared with the original is that it requires the appropriate firmware for the microcontroller, an Atmel (www.atmel.com) ATtiny13. However, free tools are available that let you develop and program the microcontroller. This Design Idea includes the source code for the operation of the sequencer in both Basic and C. You can download **Listing 1**, the code, from the online version of this Design Idea at www.edn.com/091203dia.

The demo version of the Bascom-AVR Basic compiler is fully functional and code-limited to 4 kbytes—four times the code space in the ATtiny13—and is freely downloadable for noncommercial development from MCS Electronics (www.mcselec.com). The WinAVR (winavr.sourceforge.net) tools used in this Design Idea use the GNU GCC C/C++, a fully functional, free open-source GNU GCC compiler. You can easily integrate the WinAVR compiler into the free IDE (integrated development) AVR Studio from Atmel. To program the Atmel microcontrollers, you can use free software tools through the microcontroller's six-pin SPI (serial-programming interface). You can download the easy-to-use, free PonyProg software from Lancos (www.lancos.com/prog.html) and also obtain the schematics for the programming circuits.

The circuit in **Figure 1**, like the circuit in **Reference 1**, includes two TPS75501 regulators, IC_2 and IC_3. This new circuit needs only IC_1, an eight-pin microcontroller; S_1, an SPST (single-pole/single throw) pushbutton switch to start the sequence; S_2, an SPST toggle switch, or a two-pin header with a jumper, to control the sequence order; and potentiometer R_3 to control the sequence delay. According to the firmware in **Listing 1**, pressing S_1 when S_2 is open causes the microcontroller to first turn on the 1.5V power supply and then turn on the 3.3V power supply following a delay that potentiometer R_3 controls. Pressing S_1 when switch S_2 is closed causes the microcontroller to first turn on the 3.3V power supply and then turn on the 1.5V power supply following a delay that potentiometer R_3 controls. As with the original Design Idea, a second press of S_1 causes the power supplies' turn-off to take place in the same sequence and with the same delay as their turn-on. This scenario provides an opportunity

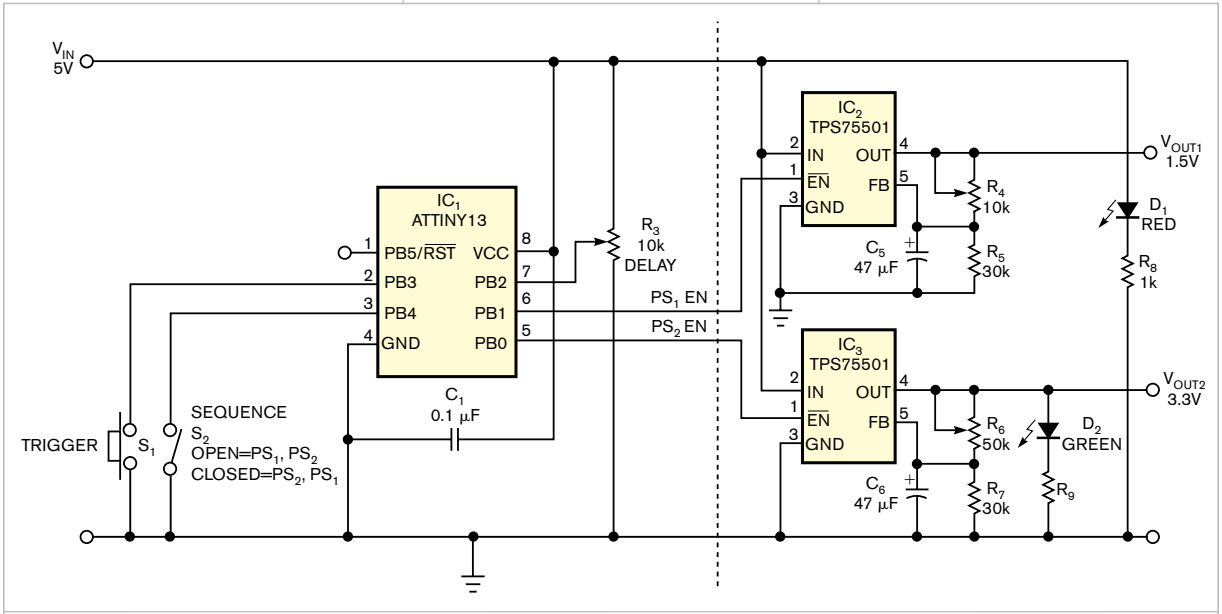

Figure 1 This circuit needs only an eight-pin microcontroller, an SPST pushbutton switch, an SPST toggle switch, and a potentiometer to control the sequence delay.

for an easy enhancement or change in operation.

The voltage level on Pin 7 of IC_1 determines the delay, under firmware control, between turning on or off the first and the second power supply. The microcontroller reads this delay voltage with its 10-bit ADC and uses the value to determine the delay according to the following **equation**: Delay=$(V_{DELAY}/V_{CC})\times1024\times1$ msec, where V_{DELAY} is the delay voltage. This **equation** yields a delay range from a few microseconds to a bit more than 1 second. As an example, if the delay-voltage value from R_3 is the midwiper value of 2.5V, the sequencing delay is approximately 512 msec: $(2.5/5V)\times1024\times1$ msec. The delay value is approximate because the microcontroller uses its internal 9.6-MHz RC oscillator to generate the timing with a simple firmware delay loop.

The code in **Listing 1** follows the original Design Idea in that a second press of trigger switch S_1 causes the power supplies to turn off in the same sequence and with the same delay with which they turn on. The **listing** includes a constant OFF_SEQUENCE that you can change to change the turn-off sequence with the second press of S_1 (**Figure 2**). This constant OFF_SEQUENCE is currently SEQUENCE_SAME to operate as the original Design Idea did, but if you set the OFF_SEQUENCE to SEQUENCE_REVERSE, the turn-off sequence will be in the opposite order of the turn-on sequence. Alternatively, if you set the constant OFF_SEQUENCE to SEQUENCE_NONE, both power supplies will turn off at once. This feature exemplifies the versatility of this follow-on Design Idea with a simple firmware change. Because the circuit uses only about half the code space in the ATtiny13, you could easily add other desired changes. Although this circuit uses an Atmel microcontroller, you can use almost any low-pin-count microcontroller with a built-in ADC. However, other brands may not have the readily available free development tools that exist for Atmel devices. EDN

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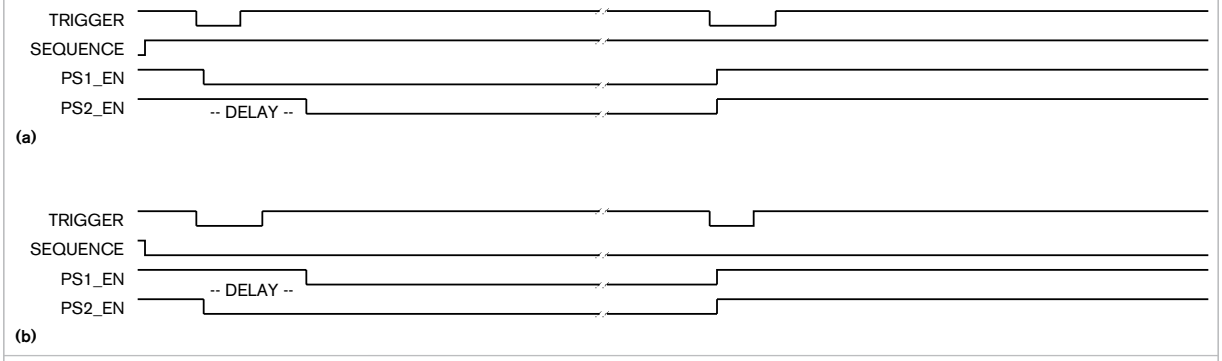

Figure 2 The timing sequence shows the power sequence for S_1 (a) and S_2 (b).

Inexpensive power switch includes submicrosecond circuit breaker

Anthony H Smith, Scitech, Bedfordshire, England

The circuit in **Figure 1** lets you switch high-voltage power to a grounded load with a low-voltage control signal. The circuit also functions as a submicrosecond circuit breaker that protects the power source against load faults. Power switches to the load when you apply a logic-level signal to the output control terminal. When the signal is lower than 0.7V, transistor Q_3 is off and the gate of P-channel MOSFET Q_4 pulls up to the positive supply through R_6, thus holding Q_4 off. During this off condition, the circuit's quiescent-current drain is 0A.

A 3 to 5V signal at the control terminal turns on Q_3, which pulls R_7 to 0V, providing gate drive for Q_4. The MOSFET now turns on and sources the load current, I_L, through sense resistor R_3 to the load. If R_3's and Q_4's on-resistances are smaller than the load resistance, the magnitude of the supply voltage, V_S, and the load resistance mainly determine the load current.

Under normal load conditions, the sense voltage developed across R_3 is too small to bias Q_1 on; thus, Q_1 and Q_2 are both off. If, however, the load current increases, the voltage across R_3 may become large enough to turn on Q_1. At that point, base current flows through R_4 to Q_1, and Q_1's collector current in turn provides base current for Q_2. As Q_2 turns on, it provides extra base drive for Q_1, and the two transistors rapidly latch in the on-state.

With Q_1 saturated, its collector pulls D_2's anode to the positive supply, which clamps Q_4's gate voltage to a diode drop below V_S. Without gate

drive, the MOSFET turns off, and I_L falls to 0A. With Q_1 and Q_2 both latched on, Q_4 remains off, which protects the power source from excessive load currents. You can reset the circuit breaker simply by taking the control signal low or by cycling the power. The resistance values in **Figure 1** are suitable for operation at supply voltages of 20 to 30V. Assuming that the transistors are suitably rated, the circuit can operate at much higher voltages, but you must scale the resistor values accordingly. Operation at a voltage as low as approximately 5V is also possible, but you may need to reduce the values of R_1 and R_5 to ensure proper drive for Q_1 and Q_2. Resistors R_6 and R_7 form a potential divider, which sets Q_4's gate-to-source voltage, V_{GS}, to a value large enough to enhance the MOSFET fully when Q_3 is turned on.

At low supply voltages, you may need to change the ratio of R_6 to R_7 to ensure that the gate-to-source voltage is large enough to provide adequate gate drive for Q_4. When the circuit is operating at high voltages, you may need small-signal diode D_1 to prevent reverse avalanche breakdown of Q_2's base-to-emitter junction when Q_3 is off. However, you can omit D_1 at low supply voltages, which are too small to cause avalanche breakdown.

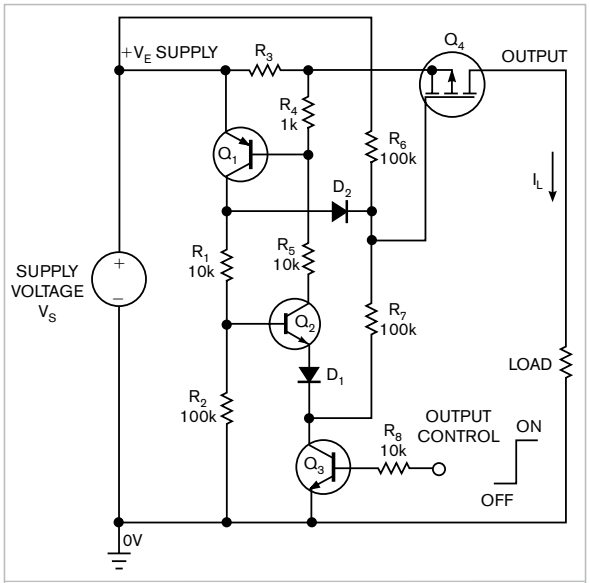

Figure 1 This inexpensive power switch incorporates a submicrosecond circuit breaker.

When selecting components, choose high-gain devices for the bipolar transistors and ensure that D_2 has low reverse-leakage current; avoid using a Schottky diode. In the off-state, each transistor has the full supply voltage across its collector-to-emitter or drain-to-source terminals, so ensure the maximum voltage ratings across these terminals are greater than the maximum supply voltage.

The circuit breaker trips at a load-current threshold: $I_{L(TRIP)} \simeq 0.5V/R_3$. For example, with a supply voltage of 24V and with R_3 having a value of 6.8Ω, a test circuit using the values in **Figure 1** trips at a load current of 70 mA. The actual trip point varies slightly with temperature and depends on the device you use for Q_1, so be prepared to adjust the value of R_3 to achieve the desired trip current.

In addition to providing a latching function, the positive feedback loop around Q_1 and Q_2 ensures that the circuit breaker responds quickly to an overload current. The actual trip time depends somewhat on the magnitude of the fault current. With a supply voltage of 24V and with R_3 having a value of 6.8Ω, the test circuit takes 6 μsec to trip at a fault current of 80 mA. However, increasing the fault current to 200 mA results in a trip time of just 500 nsec.

Capacitive loads, filament bulbs, and motors exhibit a large inrush current and could cause the circuit breaker to trip when the control signal goes high even though the normal, steady-state load current is below the trip threshold. If this scenario is likely to be a problem, consider connecting R_7 to a separate transistor so that you can independently control the circuit breaker and the power switch. This approach lets inrush current subside before enabling the circuit breaker. EDN

Create a DAC from a microcontroller's ADC

Vardan Antonyan, Glendale, CA

Few microcontrollers include a DAC. Although you can easily find an inexpensive DAC to control from your microcontroller, you can use unused peripherals instead of adding parts. Fortunately, you can convert a microcontroller's ADC channel along with a GPIO (general-purpose input/output) pin into a DAC. You can make a DAC by charging a capacitor to an analog level by driving it high. You can also discharge the capacitor by driving it low, or you can hold its voltage by tristating it (**Figure 1**). At first glance, this approach seems like a crude way to make a DAC. The technique becomes more plausible, however, when you use a PID (proportional-integral-derivative) algorithm and monitor the voltage with the microcontroller's ADC.

You can use the PID algorithm to compare the output voltage with the desired value and calculate the error. If the error value is zero, then the I/O control block tristates the GPIO pin. If the error signal is positive or negative, then the I/O control block turns the I/O pin to a high state to charge the capacitor or to a low state to discharge it. Your microcontroller code should load the error value into a timer to generate a timed pulse. The error-value sign determines the charge/discharge cycle, and its magnitude determines the duration of the pulse. Once the cycle is complete, you can set the I/O pin to a tristate mode, which holds the value.

The algorithm can run as a software loop. You can call it based on another timer interrupt. To minimize the response time, make sure that this algorithm runs at the desired output value slightly longer than 2.2RC. You need the extra time to completely charge or discharge the capacitor through resistor R_1.

The DAC's resolution depends on several factors, the foremost of which is ADC resolution. The DAC's resolution never exceeds that of the ADC. Variable selection and timer resolution also affect DAC resolution. To implement a 10-bit DAC, you need a 16-bit timer and 16-bit variables for the PID algorithm. You can use a lower-resolution timer, but you must more frequently call the algorithm. That action results in longer settling times and higher CPU usage.

By adjusting the algorithm's PID variables, you can achieve surprisingly good output settling times with little change to the DAC's output after settling. The stability of the ADC's voltage reference limits temperature stability. Neither the temperature stability of R_1 and C_1 nor the leakage of C_1 has an adverse effect on the DAC's stability. The selection of R_1 and C_1 depends on the application, and you should select them based on settling time. For relatively slow-acting DACs, you can increase the update rate by running the algorithm faster than the 2.2RC period and using an 8-bit timer. To buffer the DAC output, use an op amp as a voltage follower or use a common emitter follower. You can use a noninverting amplifier to amplify the output and feed just a portion of it to the ADC through a voltage divider. EDN

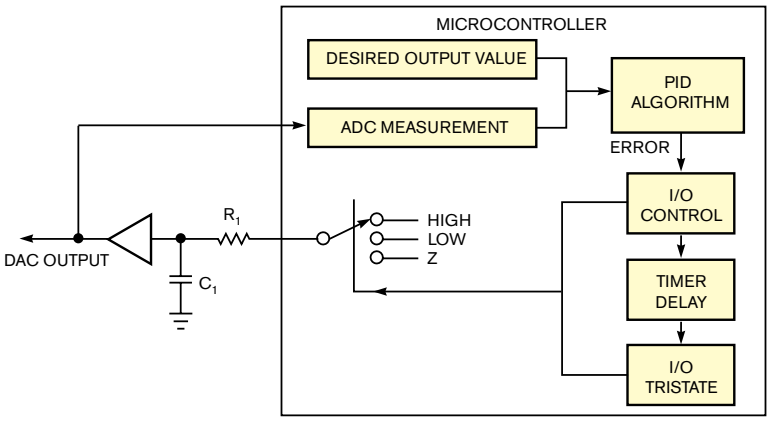

Figure 1 You can develop a PID algorithm to control pulse width and time, thus creating a DAC from a general-purpose I/O pin. Use the ADC as part of the feedback loop.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Compact, four-quadrant lock-in amplifier generates two analog outputs

Stefano Salvatori and Marco Girolami,
Universitã Degli Studi Roma Tre, Rome, Italy

The circuit in this Design Idea realizes a simple, low-cost lock-in amplifier employing an Analog Devices (www.analog.com) AD630 balanced modulator-demodulator IC (**Reference 1**). The device uses laser-trimmed thin-film resistors, yielding accuracy and stability and, thus, a flexible commutation architecture. It finds use in sophisticated signal-processing applications, including synchronous detection. The amplifier can detect a weak ac signal even in the presence of noise sources of much greater amplitude when you know the signal's frequency and phase.

As an analog multiplier, the AD630 reveals the component of the input-voltage signal in a narrow band around the frequency of the reference signal. The lowpass filter at the AD630's output allows you to gain information on the weak signal amplitude, which the uncorrelated noise originally masked. When the input voltage and the reference voltage are in phase, the lowpass filter's output, V_{OUT}, assumes the maximum amplitude. Conversely, if the input voltage and the reference voltage are in quadrature, the output voltage would ideally be 0V. In this way, if both in-phase and quadrature reference signals are available, two balanced demodulators reveal the in-phase output voltage to be 0° and the in-quadrature output voltage to be 90°. You can calculate the module and phase shift as follows:

$$|V_{OUT}| = \sqrt{V^2_{OUT0°} + V^2_{OUT90°}};$$

$$\angle V_{OUT} = \tan^{-1}\left(\frac{V_{OUT90°}}{V_{OUT0°}}\right).$$

The two AD630s have a gain of ±2 and receive the amplified signal, V_{IN}, through two identical amplifiers, A_1 and A_2. At Pin 7 of IC_1, a bipolar ±5V squared signal appears in phase with

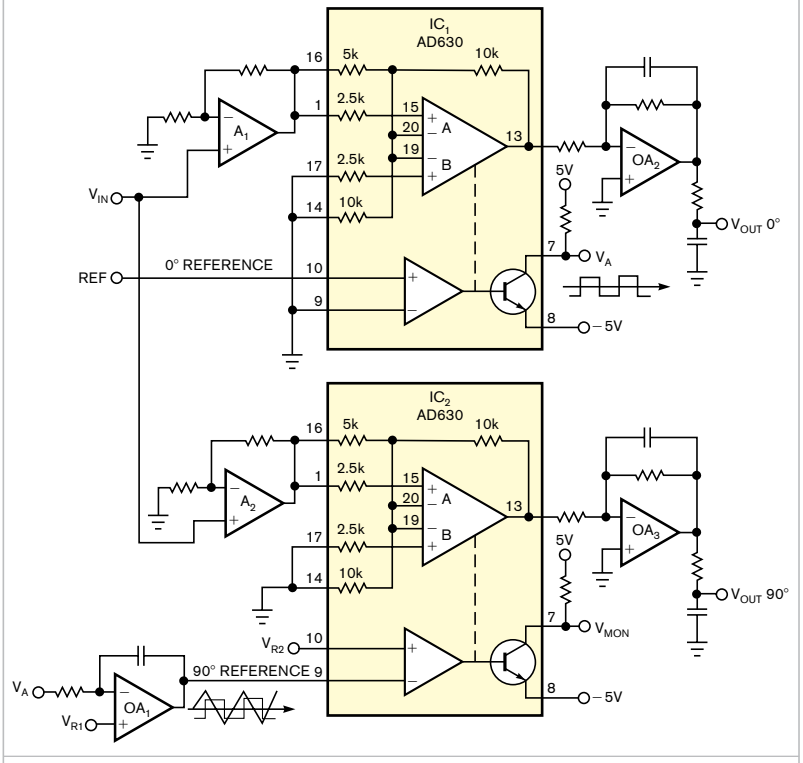

Figure 1 OA_1 integrates the bipolar V_A signal and creates a triangular wave. V_{R1} and V_{R2} obtain a 90°-shifted reference voltage with respect to V_A.

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the reference signal. OA_1 integrates the amplifier voltage, which generates a triangular wave that IC_2's comparator compares with the V_{R2} voltage. You must regulate V_{R1} and V_{R2} to obtain a perfect 90°-shifted command for IC_2. You can monitor the voltage at IC_2's Pin 7. Measurement accuracy and repeatability depend strongly on the RC time constant of the integrator and the values of V_{R1} and V_{R2}.

You can use a different approach to generate in-phase and in-quadrature reference signals. **Figure 2** shows an all-digital circuit, which you can implement in a small CPLD (complex programmable-logic device) to generate the 0 and 90° reference signals in **Figure 1**. Counter 1 measures the reference-signal time in terms of the N number of digital clock pulses, where the reference time can be different from 50%. It receives a preset command at the $N_1=1$ value at each positive front edge of the reference signal. D-type flip-flop IC_1 generates such pulses. At each positive edge of the reference signal, IC_2 acquires the N/4 value. Meanwhile, Counter 2 counts the clock periods and receives a restart command at the $N_2=1$ value when its value reaches the comparator-measured N/4 quantity.

AN INCREASE IN THE NUMBER OF BITS DECREASES THE MAXIMUM REFERENCE FREQUENCY.

To overcome the lack of the last EQ signal when the reference time is greater than approximately four times the N/4 integer value, the OR combination of the two RST and EQ pulses yields four almost-equidistant positive-edge commands in each reference-time period. The N/4 integer division, a logical right shift by 2 bits of N_1, gives a maximum error of three on the last pulse position. These pulses generate the in-phase and in-quadrature signals, 0 and 90°, respectively, resulting from simple commutations on the positive or negative edges of the signal. T-type flip-flop IC_3 generates a signal with twice the frequency of the reference signal. In this way, the accuracy is equal to $3/N_1$.

To maintain accuracy at least comparable with that of the AD630, the N_1 output of Counter 1 would be the highest. However, an increase in the number of bits decreases the maximum reference frequency for a given digital-clock frequency if you want N_1 to reach high values. For example, if N is 15 bits, the N_1 output assumes the 32,767 maximum value with an accuracy of approximately 0.01%. If the reference-time period decreases, you can assume a minimum value of 3277—that is, one-tenth of the maximum value—for N_1, with a correspondingly lower accuracy of 0.1%, which is comparable to the gain accuracy of the AD630. To increase the reference frequency, divide the digital clock's frequency to select low values when the reference time becomes too long. EDN

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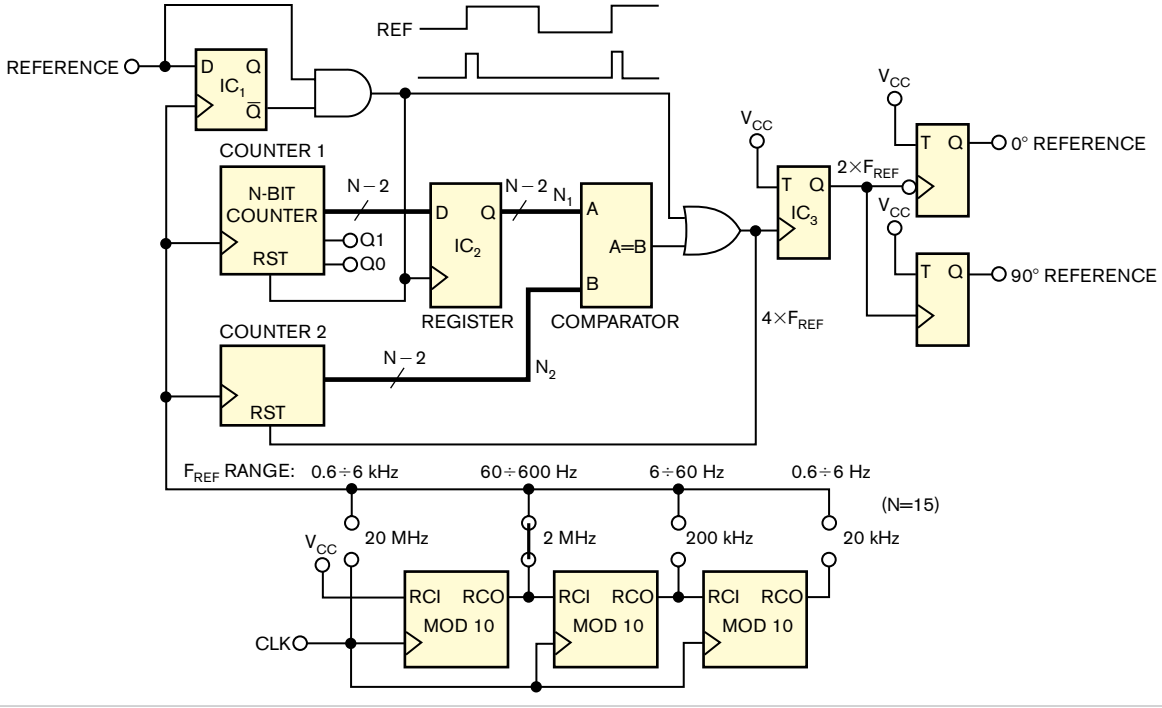

Figure 2 You can implement this all-digital circuit in a small CPLD.

Eight-function remote uses one button, no microcode

Jay Davis, Boeing Integrated Defense Systems, Wichita, KS

Many people with significant physical disabilities can't operate everyday mechanisms, such as TV remote controls. To make matters worse, adaptive technologies are often unaffordable unless insurance covers them. This Design Idea describes an interface circuit that lets a disabled person control eight remote-control functions. The design uses older, small-scale-integration ICs because of their simplicity, low power requirements, affordability, and availability at stores such as Radio Shack (www.radioshack.com). Because the circuit uses no microcontroller, you need not do any programming.

Power for the circuit in **Figure 1** comes from four 1.5V AA batteries in series. Diodes D_1 through D_4 reduce the battery power from 6V to approximately 3.4V, and they protect against accidental reverse polarity of the batteries. IC_1, a 555 timer, and associated discrete components form a repetitive-pulse generator. Potentiometer R_1 adjusts the pulse speed. This pulse feeds directly into decade counter, IC_2, which causes indicator LEDs LED_1 through LED_4 to sequence on and off. Each output of the decade counter feeds one input of CMOS gate IC_3 and AND gate IC_4.

Normally, the output of the NAND gate is low because both inputs must be logic one to produce a logic-one output to close one of the CMOS switches, IC_5 and IC_6.

If the user presses the control switch while the desired LED is lit, both inputs to one of IC_3's AND gates are at logic one, causing the output to be logic one and closing a 4066 switch, which is effectively the same as pressing one of the buttons on the remote control. As long as the control switch remains closed, the 555 pulses remain disabled and LED_1 through LED_4 remain in their current state. This characteristic is important because a person can continue to hold the control switch closed to continuously increment the changing of a channel or increase or decrease the volume. EDN

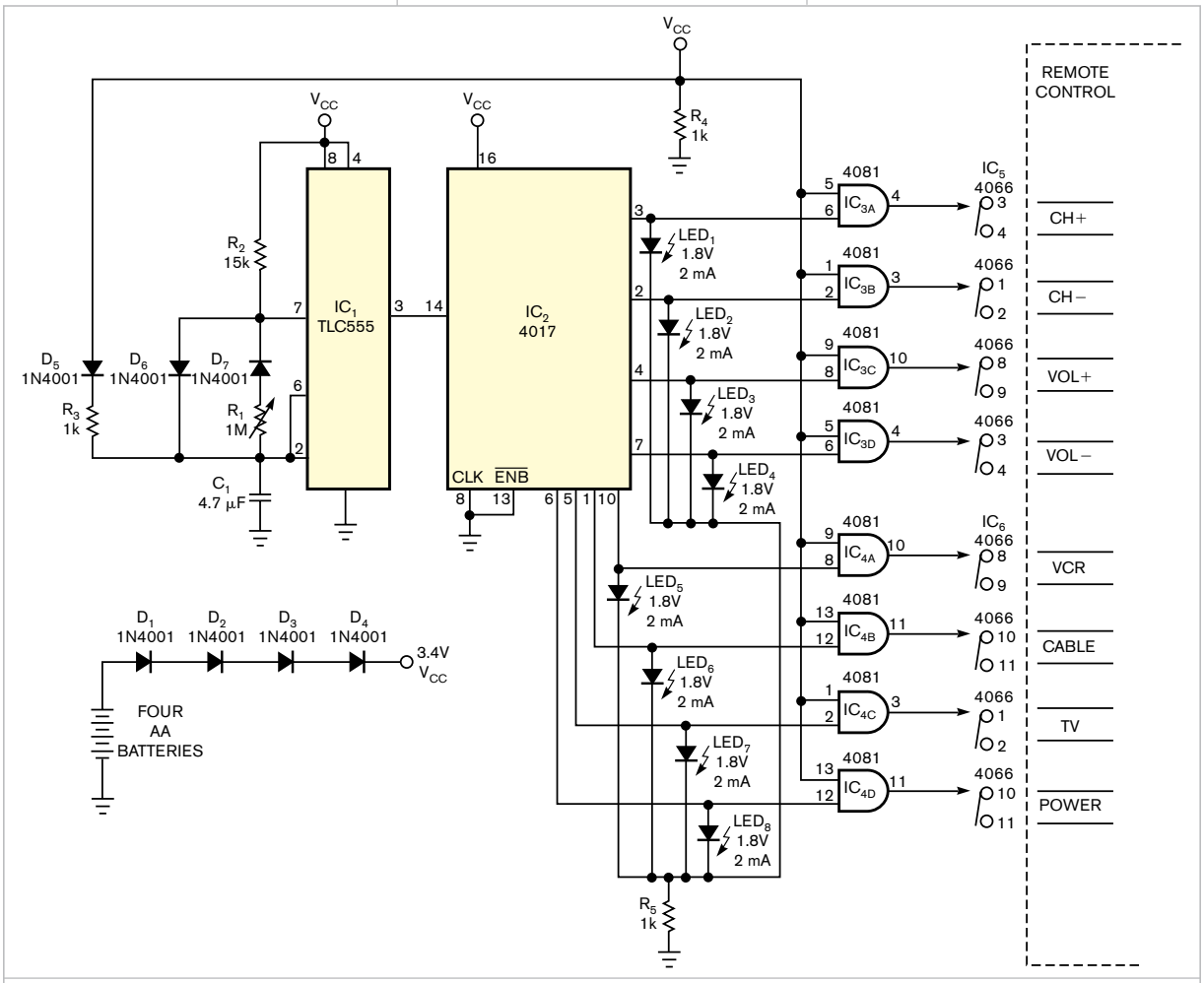

Figure 1 This interface circuit allows a disabled person to control eight remote-control functions.

Doorbell transformer acts as simple water-leak detector

Jeff Tregre, www.BuildingUltimateModels.com, Dallas, TX

Shortly after installation, the simple water-leak-detector circuit in this Design Idea saved the day and hundreds of dollars. The average life expectancy of a hot-water heater is about 10 years. It's not a question of whether it will leak; it is simply a matter of when it will leak. The builders of new homes in the Midsouth region of the United States have been installing hot-water heaters in attics. This approach saves valuable space; however, if you only infrequently visit the attic, you may not discover that your hot-water heater is leaking until it is too late. By that time, it may cost you hundreds of dollars to repair the water damage to ceilings and walls.

The circuit in **Figure 1** detects hot-water-heater leakage, and you can also use it for detecting leaks in dishwashers, garbage disposals, ice makers, swimming pools, hot tubs, and waterbeds. **Figure 2** shows the completed circuit.

Most doorbell transformers produce

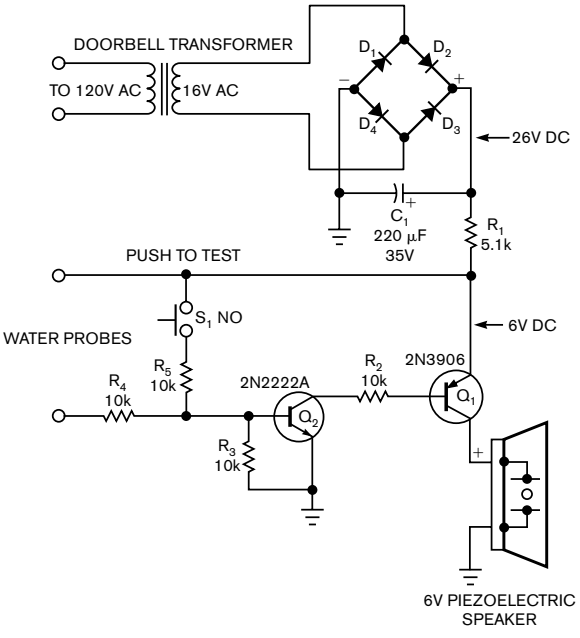

Figure 1 A transformer and a bridge provide power for the speaker.

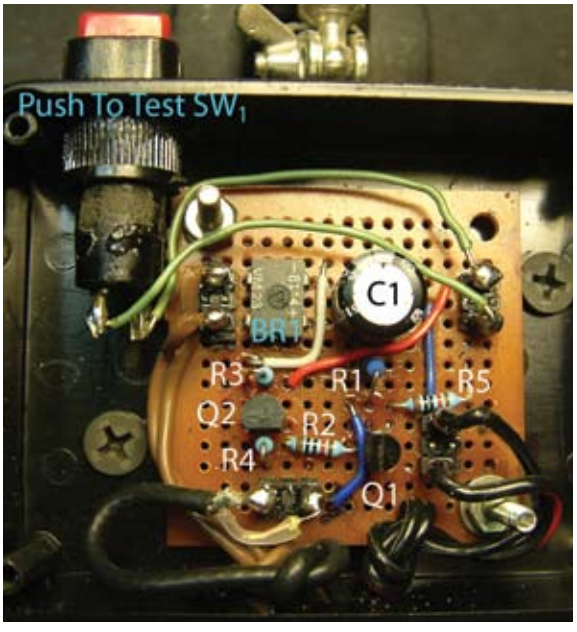

Figure 2 The circuit includes a push-to-test button.

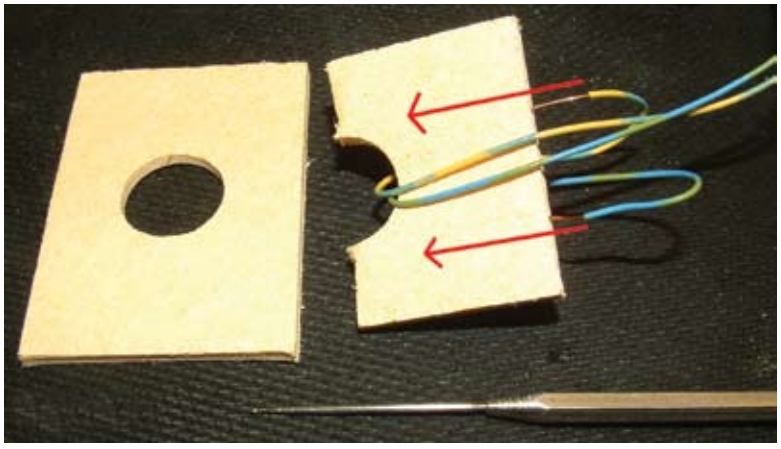

Figure 3 Use a sponge and copper wire to form a water probe.

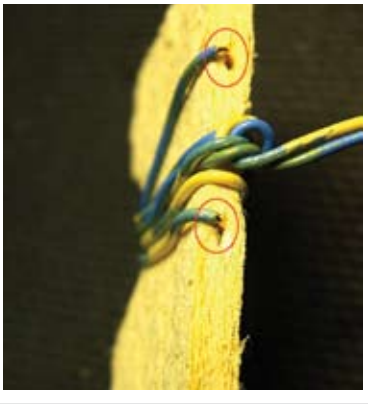

Figure 4 The completed probe with bare wire inside senses water through a change in resistance.

16 to 20V ac. To drive the buzzer, you must convert the ac voltage to dc: Multiply the ac voltage by 1.414 to yield the dc-rms voltage. Connect the wires to the secondary side of the transformer to a bridge rectifier and then into a filtering electrolytic capacitor. Your power supply should now be providing about 26V dc. The 5.1-kΩ resistor, R_1, limits the current to the buzzer. When the system detects water or when you press the push-to-test switch, you have about 6V dc to operate the circuit and sound the piezoelectric speaker. Mount the speaker so that you'll hear it when it sounds.

Transistors Q_1 and Q_2 can be any general-purpose NPN and PNP types, respectively. The water probes use copper wires about 1 in. apart from each other. You then pierce two holes, about 1 in. apart, into a sponge from a soldering station. Insert bare copper wire into these holes (**Figure 3**). Take some of the remaining wire but leave the insulation on it and wrap it around the sponge so that the bare copper wire does not come out (**Figure 4**).

You can now place this sponge in the metal overflow tray underneath the hot-water heater. When the hot water leaks, the sponge absorbs it. The resistance between the two bare copper wires then drops to about 1 MΩ or less, which forward-biases the two transistors and enables the piezoelectric speaker. The cost for this circuit shouldn't exceed $25. If you have more than one hot-water heater in the same area, you can make another water probe and tie the two probes together in parallel. EDN

Inverted regulator increases choice and reduces complexity

David McCracken, Aptos, CA

Most circuits are referenced to ground, where relatively low-voltage components can monitor and control the low side of a load but not the high side. For example, nearly any low-voltage rail-to-rail-input op amp can detect a voltage increase indicating overcurrent through a resistor that connects between the load and ground. To do the same thing on the high side, you typically select a differential amplifier that tolerates high common-mode voltage. This approach limits the component choices for the

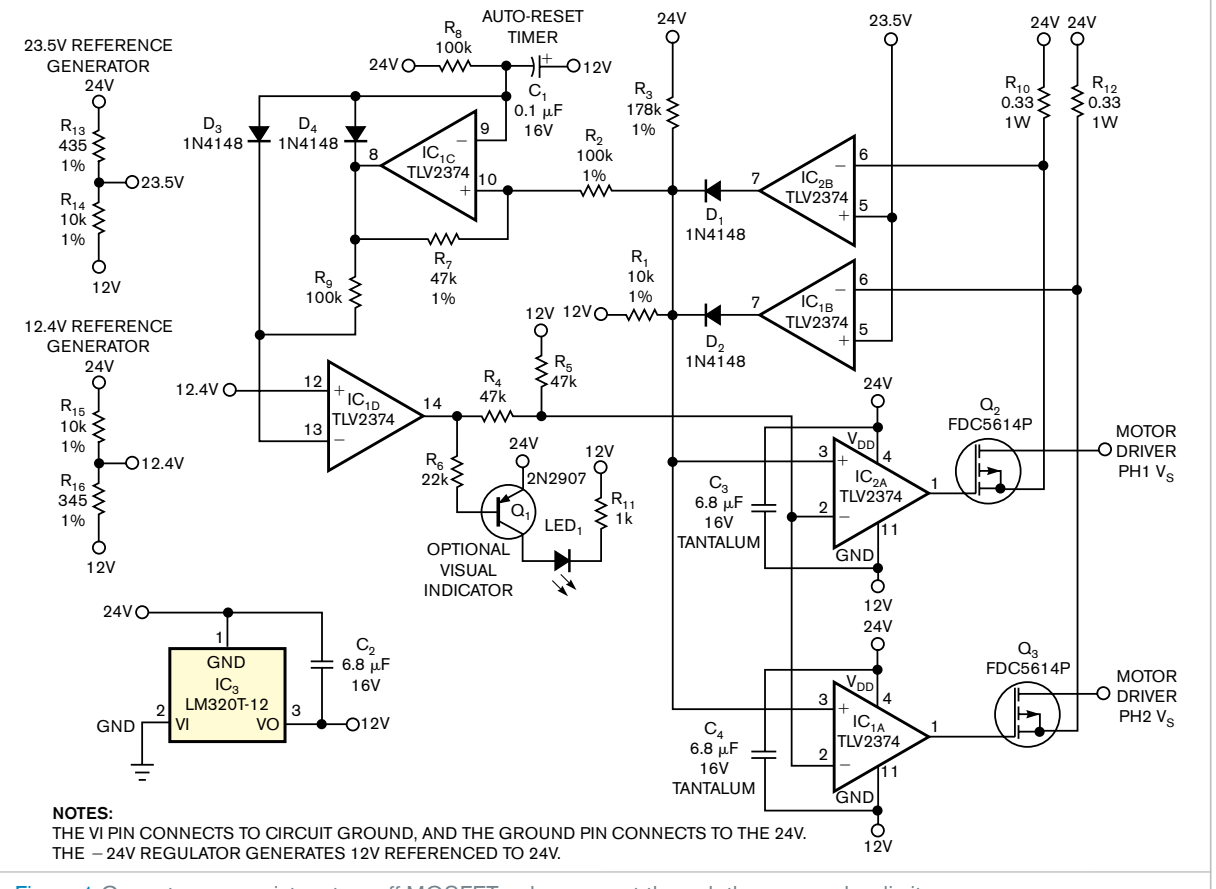

Figure 1 Current-sense resistors turn off MOSFETs when current through them exceeds a limit.

input amplifier and brings up the question of how to respond to an overcurrent. The differential amp produces a low ground-referenced signal from a high-side event, but you can prevent a high-side overcurrent resulting from a short to ground only by turning off the high-side power. In effect, the differential amp translates the high-side signal into the low-side domain in which you must then translate the response back into the high-side domain.

A simpler approach for any high-side overcurrent-protection circuit references the entire circuit to the high-side rail. Such circuits typically consume little power, which a small, three-terminal linear regulator can easily supply. However, this approach requires an unusual configuration employing a negative regulator whose ground pin connects to the high-side rail and whose input connects to system ground. There are no other connections to system ground. All "ground" points of the overcurrent-protection circuit connect to the regulator's out pin.

Figure 1 shows a two-phase-stepper-motor, fast-acting, self-resetting high-side circuit breaker with a 24V power supply to the motor and a 12V power supply to the circuit breaker that is referenced to 24V. The circuit breaker sees the 24V motor's power rail as 12V referenced to its local ground, which the regulator's output provides. Like all negative linear regulators, the circuit requires a 6.8-µF tantalum capacitor.

R_{10} and R_{12}, both 0.33Ω, 1W resistors, provide current sensing for the two phases. High-side power flows through a sense resistor and a P-channel MOSFET to the high-side input of an H bridge (not shown), which drives one motor winding. Current in either phase can cause the sense voltage to increase to 0.5V, triggering the breaker. The circuit responds by turning off both MOSFETs. It then waits 20 msec and turns them back on, automatically clearing momentary shorts. EDN

Debug a microcontroller-to-FPGA interface from the FPGA side

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Microcontrollers and FPGAs often work together in embedded systems. As more functions move into the FPGA, however, debugging the interface between the two devices becomes more difficult. The traditional debugging approach comes from the microcontroller side, which relies on a serial-port printout. This approach adds overhead and may cause timing problems. Furthermore, this approach cannot guarantee uninterrupted and exclusive access to certain addresses because of operating-system multitasking. Thus, a serial-port printout doesn't accurately describe the actions on the microcontroller/FPGA interface.

Instead, you can approach the problem from the FPGA side using a JTAG (Joint Test Action Group) interface as a communication port. This approach uses the internal logic of the FPGA to capture the read/write transactions on the microcontroller/FPGA interface. This method is nonintrusive because the circuit that captures transactions sits between the microcontroller and the FPGA's functioning logic and monitors the data without interfering with it. It stores the captured transaction in the FPGA's RAM resources in real time. You can transfer the data to a PC through the JTAG port's download cable.

The debugging tool comprises the data-capture circuit, the JTAG communication circuit, and the GUI (graphical user interface). The data-capture circuit uses standard HDL (hardware-description language) and instantiates a FIFO (first-in/first-out) buffer in the FPGA. Whenever you read or write to a register, the debugging tool records the corresponding value of the address and data on the bus and stores it in the FIFO buffer. You can retrieve the data through the JTAG's download cable to the PC (**Listing 1**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

Because the FPGA has limited on-chip RAM resources, you must keep the FIFO buffer shallow. To efficiently use the FIFO buffer, the design includes filter and trigger circuits. With inclusive address filtering, the circuit monitors only several discontinuous spans of addresses instead of the whole address space. Exclusive-address filters can filter out several smaller address spans from the inclusive-address spans, enabling finer control of the filter settings (**Listing 2**, which is also available in the online version of this Design Idea at www.edn.com/091215dia).

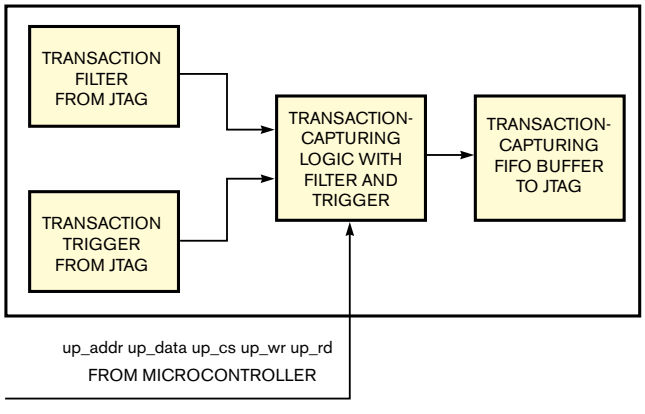

Figure 1 The JTAG's vendor-supplied, customizable communication circuit has two interfaces.

With transaction triggering, the circuit starts when you read from or write to a certain address. You can add certain data values to the triggering condition (**Listing 3**, which is available in the online version of this Design Idea at www.edn.com/091215dia). You can dynamically reconfigure the settings of address filters and transaction triggers through the JTAG's vendor-supplied, customizable communication circuit without recompilation of the FPGA design (**Figure 1**). The circuit has two interfaces, one of which is written in HDL to form a customized JTAG chain. It communicates with the user logic (**listings 1**, **2**, and **3**). The circuit is accessible through specific programming interfaces on the PC and communicates with the user program or GUI (**Listing 4**, which is available in the online version of this Design Idea at www.edn.com/091215dia).

The FPGA-based circuit facilitates writing and reading functions from PC to FPGA logic, and it promotes the JTAG interface to a general communication port attached to the FPGA. FPGA manufacturers, including Actel (www.actel.com), Altera (www.altera.com), Lattice Semiconductor (www.latticesemi.com), and Xilinx (www.xilinx.com), respectively, call this circuit UJTAG (user JTAG), Virtual JTAG, ORCAstra, and BScan (**references 1** through **4**).

The GUI for this circuit uses Tcl/Tk (tool-command-language tool kit). FPGA manufacturers provide vendor-specific APIs (application-programming interfaces) in Tcl for the PC side of the JTAG-communication circuit. The APIs include basic functions, such as JTAG-chain initialization, selection, and data reading and writing. With the data-read function, you can check the capturing status and get the transaction data from the FIFO buffer. With the data-writing function, you can send the filter and trigger configuration data to the capturing circuit in the FPGA (**Listing 4**). The JTAG-based debugging method provides dynamic visibility and controllability into the microcontroller-to-FPGA interface and the FPGA's internal logic without the need to recompile and download FPGA code. EDN

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