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electronic design

Circuit Enables Precision Control In Radiant Heating Systems

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Successful design of precision temperature-control loops, like all high-performance servo systems, depends on careful management of the usual feedback gain and bandwidth tradeoffs. While always tricky, these interactions can become unmanageable if the relevant thermal "constants" are unknown, or worse, not constant at all. Discussed in this article is a thermal design that arose from just such a challenging scenario. The design involves a system complicated by the nonlinear temperature-dependent parameters of radiant heat transfer.

The application requires accurate thermostasis of a silicon (Si) wafer over a 100°C to 1000°C setpoint range in an evacuated chemical-vapor-deposition (CVD) rig. Temperature control is accomplished via radiant heating from a large (250 W or larger) low-voltage dc incandescent lamp.

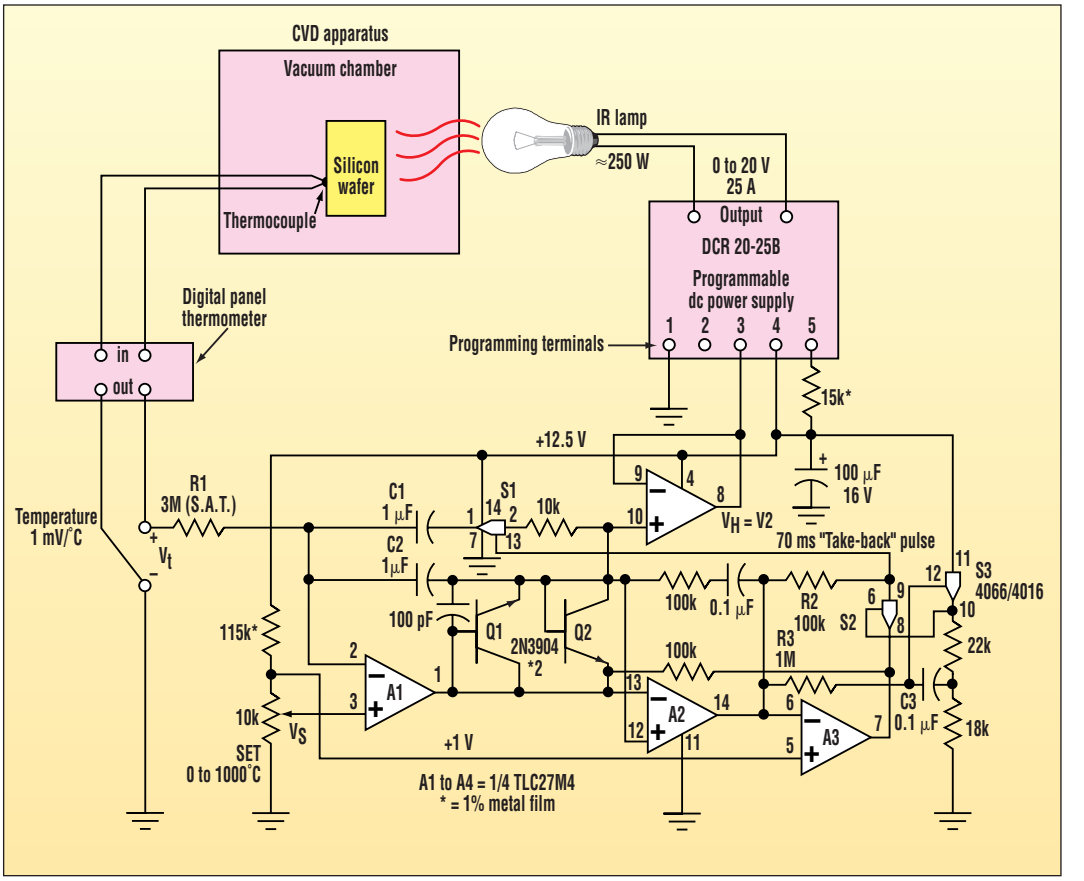
It was the radiant heating feature that made this control problem extra "interesting." So-called "Newtonian" heat exchange which occurs via conduction or convection tends to be nicely linear with temperature. But radiation, alas, is proportional to the fourth power of absolute temperature.

Consequently, the thermal time "constants" (degree-sec/degree) of radiation-coupled systems aren't linearly independent of temperature as they are in Newtonian systems. Instead, they're inversely proportional to T^3. This causes the thermal time-constant of the vacuum chamber's Si wafer to vary by a factor of 40 over the 100°C (373K) to 1000°C (1273K) setpoint range!

Such variation adds substantially to the difficulty of designing an accurate yet non-oscilla-

1. $V_E \equiv V_S - V_t \equiv$ temperature error
2. If $V_E = 0$, then $V1 \leftarrow V2 \leftarrow \frac{V1 + V2}{2}$
3. If $V_E \neq 0$, then $V2 \leftarrow V1 + \int_{t_0}^{t} t_0\, V_E dt$, where t_0 = last zero-crossing time
4. $V_H = V_2 \equiv$ heater input

1. An overview of the "Take-Back-Half" (TBH) integrating convergence-by-bisection temperature-control algorithm.



2. This circuit achieves accurate temperature control over a 100°C to 1000°C range by using a "Take-Back-Half" temperature-control algorithm, described in detail in an earlier Idea For Design.

tory control loop. Coping with this complication required use of a robust integrating convergence-by-bisection feedback control algorithm *(Fig. 1)*. This algorithm is used as the basis for the thermostat circuit shown in Figure 2. It's described in detail in *"Take-Back-Half: A Novel Integrating Temperature-Control Algorithm,"* ELECTRONIC DESIGN, *Dec. 4, 2000, p. 132.*

The Si wafer's temperature is sensed by a thermocouple. Next, it's cold-junction compensated, amplified, linearized, and repeated as a 1-mV/deg. analog output, V_T, by the digital panel thermometer. V_T is compared to the setpoint voltage, V_S. The $V_S - V_T$ difference is then integrated by A1, buffered by A4, and applied the control input of the programmable lamp supply.

Therefore, whenever $V_T < V_S$, the lamp voltage (and, therefore, the heat radiated onto the wafer) will ramp up, warming the wafer. Conversely, if $V_T > V_S$, the wafer will be cooled. Of course, if this simplistic error integration comprised the entire control algorithm, stable convergence to the setpoint wouldn't be likely. Instead, persistent oscillation above and below the setpoint would be virtually inevitable.

The "Take-Back-Half" (TBH) algorithm damps oscillations and stabilizes the servo loop. It does so by revising the estimate of the optimum steady-state lamp voltage at each setpoint ($V_T = V_S$) crossing. To make TBH action possible, some means for detecting setpoint crossings must exist. Crossed-diode-connected transistors Q1 and Q2 and comparator A2 accomplish this task by continuously tracking the polarity of the $(V_S - V_T)/R1$ error current. A2 goes high when $V_T < V_S$ and low when $V_T > V_S$, while inverter A3 generates the complementary logic term. Positive feedback around A2 keeps the logic transitions snappy. Meanwhile, the roles of TBH variables H_O and H are served by sample-and-hold capacitor C1 and integrator cap C2, respectively.

CMOS switches S1, S2, and S3 are arranged so that whenever $V_T < V_S$, S2 turns on and connects S1's control input to A3's logic-zero. This shuts off S1, which in turn isolates C1 and holds H_O. Alternatively, when $V_T > V_S$, S2 turns off, allowing R2 to pull S1's input to A2's logic-zero. Again, S1 turns off and C1 is isolated.

The fun begins whenever $V_T = V_S$. When $V_T < V_S$ flips to $V_T = V_S$, A3 switches from zero to one, which turns on S1. As a result, C1 (H_O) and C2 (H) are connected in parallel and set to $(H + H_O)/2$. This state persists for the time-out set by R3C3 (approximately 70 ms). After this period, S3, S2, and S1 all turn off and isolate C1 to await the next setpoint crossing. A similar cascade follows any toggle from $V_T > V_S$ to $V_T = V_S$. A2 turns S1 on via R2 until R3C3 times out and turns S3 and S2 on and S1 back off.

Optimization of overall servo-loop dynamics is easy since selected-at-test R1 is the only variable involved in the tuning process.

Circuit Detects When A Shared Telephone Line Is In Use

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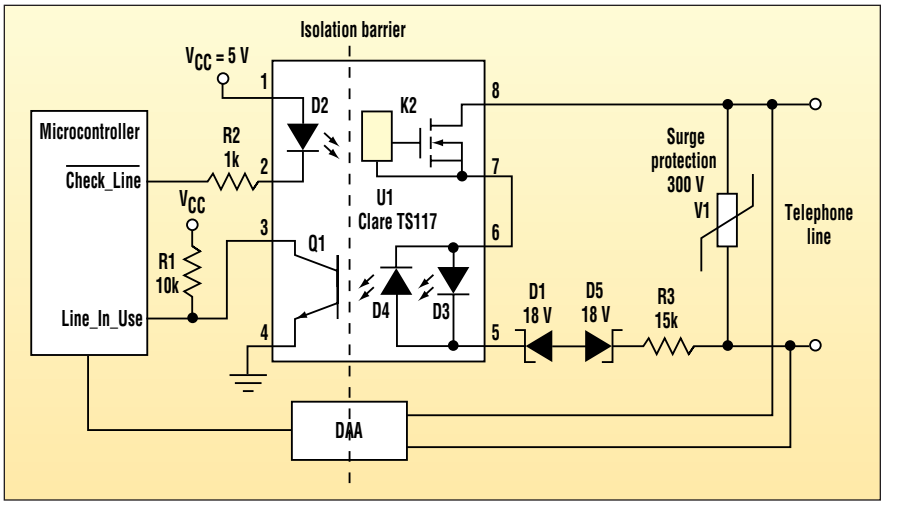
CIRCLE 501

The circuit shown can detect when a shared telephone line is in use *(see the figure)*. This is particularly useful when an automated device wishes to place an outgoing call without disturbing an established telephone line connection.

As the circuit demonstrates, when a telephone line isn't in use, the dc voltage across the line is between 42 and 52 V, with 48 V being the nominal. When any shared devices on the phone line go "off-hook," the voltage across the telephone line typically drops to somewhere between 4 and 18 V.

Clare's TS117 integrated relay and an optocoupler provide the circuit with 3750-V_{RMS} galvanic isolation between the microcontroller side of the circuit and the telephone line. In this circuit, the device wishing to make an outgoing call asserts the $\overline{\text{Check\_Line}}$ signal (i.e., low), which turns on LED D2. Next, the light from D2 activates the high-voltage solid-state relay K2 that provides a current path to LEDs D3 and D4. D3 and D4 are anti-parallel to allow the circuit to operate regardless of the telephone line polarity.

If the line isn't in use, the voltage across TIP and RING will be greater than 42 V, and Zener diodes D1 and D5 will conduct. Note that one of the Zener diodes will be conducting in the Zener region, and the other will be forward-biased, depending on the telephone line polarity. Such conduction causes a current to flow through the forward-biased LED D3 or D4. The light from this LED is coupled to phototransistor Q1, which is driven into saturation. This pulls the Line_In_Use signal low, indicating that the line is available.



Using a solid-state optoisolated relay to apply a voltage detector to the phone line helps this detector circuit meet the FCC requirements for on-hook impedance limits.

If the device wishing to make the call asserts the $\overline{\text{Check\_Line}}$ signal and the telephone line voltage is less than approximately 20 V, then Zener diodes D1 and D5 will not conduct. When this is the case, no current will flow through LEDs D3 or D4. Also, the Line_In_Use signal will be high, indicating that the line is in use. The device wishing to place the call should wait and retry at a later time.

R3 is selected so that the current drawn by the detector circuit does not assert an off-hook condition when $\overline{\text{Check\_Line}}$ is asserted. V1 is a 300-V surge suppressor that can be a MOV or thyristor-type device. Relay K2 is used to comply with the FCC's on-hook impedance requirements.

Random Number Generator Has A Predefined Distribution

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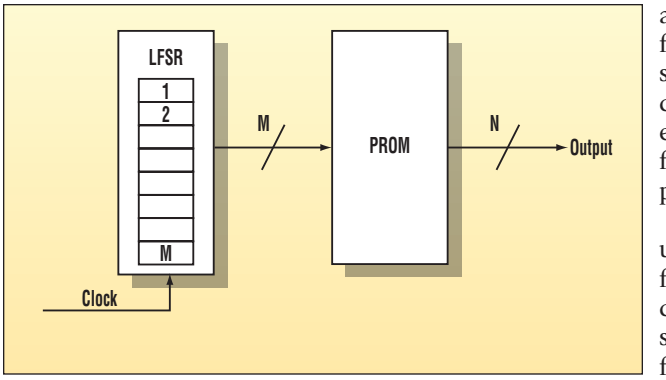
Many digital designs incorporate high-speed generation of pseudorandom numbers. Typically, pseudorandom number generation is implemented using linear-feedback shift register (LFSR). An LFSR produces a sequence of numbers that appears to be uniformly distributed over the range 1 to 2^{n-1}, where n is the LFSR size. For this type of generator, each output value has an equal probability of appearing.

Some applications, however, require the generation of random numbers that aren't uniformly distributed. Instead, they obey a predefined, arbitrary distribution. This example of an arbitrary probability distribution function (PDF) expresses the occurrence probability of 10 values *(Fig. 1)*. The cumulative distribution function (CDF) is an incremental aggregation of the PDF.

Since by definition the CDF is a positive monotonic function with values from 0 to 1, it's apparent that an inverse CDF always exists.

The inverse CDF may be interpreted as a function mapping uniformly distributed values to some arbitrary distribution described by the PDF. Such an explanation leads to a straightforward digital hardware implementation *(Fig. 2)*.

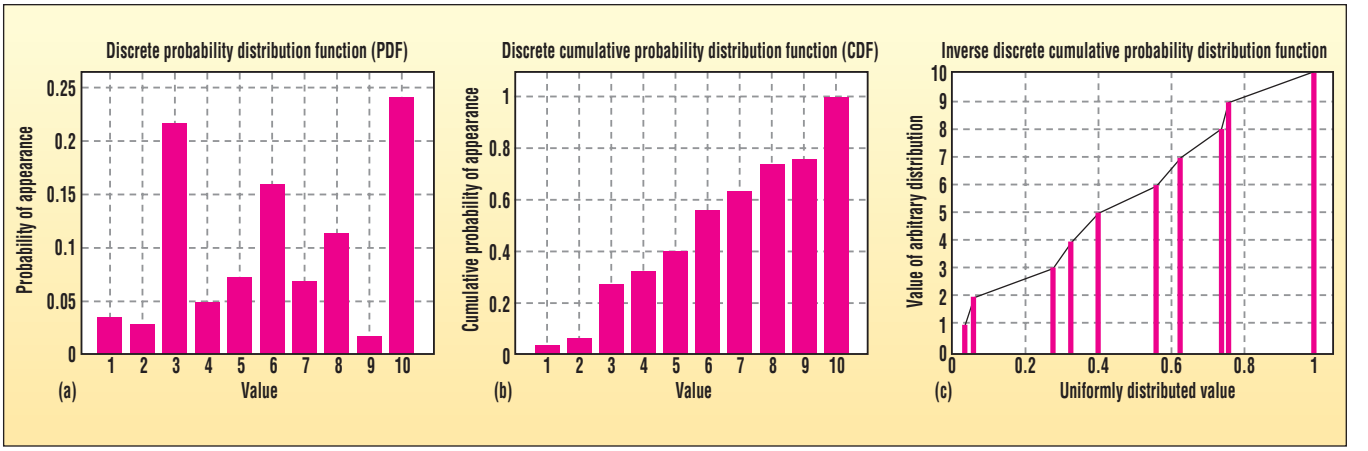


2. The high-speed hardware implementation of this random number generator allows the arbitrary output distribution to be controlled by the inverse cumulative distribution function.

Two basic components make up the design. One is an LFSR functioning as a pseudorandom number generator. As such, it generates values uniformly distributed over a specific range in accordance with the LFSR size (M). The other is a programmable ROM (PROM) containing the inverse CDF function. This PROM acts as a lookup table with the LFSR outputs used as input lines. The PROM is a sequence of random numbers, distributed with respect to the PDF, used as output lines (N). Depending on the requirements of the specific application, the PROM may be replaced with a RAM device.

Precision may be flexibly determined by choosing the LFSR and ROM sizes that meet with design needs. Longer LFSR widths and wider ROM addresses result in finer granularity.

This technique also is attractive in terms of speed. The critical path is composed of merely an LFSR (on the order of a single-gate level) and a memory component, yielding very high clock rates.



1. An arbitrary distribution is generated by analyzing the probability distribution function (a) and the cumulative distribution function (b) to create the inverse cumulative distribution function (c). The resulting CDF function is then embedded in the PROM contents.

Circuit Detects Phone-Line Breaks

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Alarm system designs often require circuitry that can detect whether a phone line is active or broken. With this type of design, the primary difficulty is drawing less than 5 µA from the phone line over a line-voltage range of 24 to 58 V as the standard dictates.

When the phone is in its "on-hook" state, the central office exchange (CO) acts as a current source. The circuitry on the line is restricted to impedances that create less than a 5-µA current from this source. When the phone goes off-hook, the phone's impedance lowers significantly. Consequently, a CO-detected voltage drop is produced. The CO creates the ringing signal by adding a low-frequency signal to this dc bias signal.

Shown here is a circuit based on a micropower oscillator biased by the telephone line *(see the figure)*. This oscillator generates a differential signal, which is coupled to a detector circuit via high-voltage capacitors. These capacitors supply the required isolation. The detection circuit merely recognizes the presence of the oscillation while presenting negligible output loading to the oscillator itself.

The oscillator uses an astable multivibrator. Instead of relying on the traditional collector resistors, which would otherwise become very large, it employs 1-µA current sources (Q4 and Q6). These determine the supply current. Also, capacitor-charging resistors (which establish the oscillation frequency) are based upon current sources of 0.1 µA nominal (Q3 and Q5).

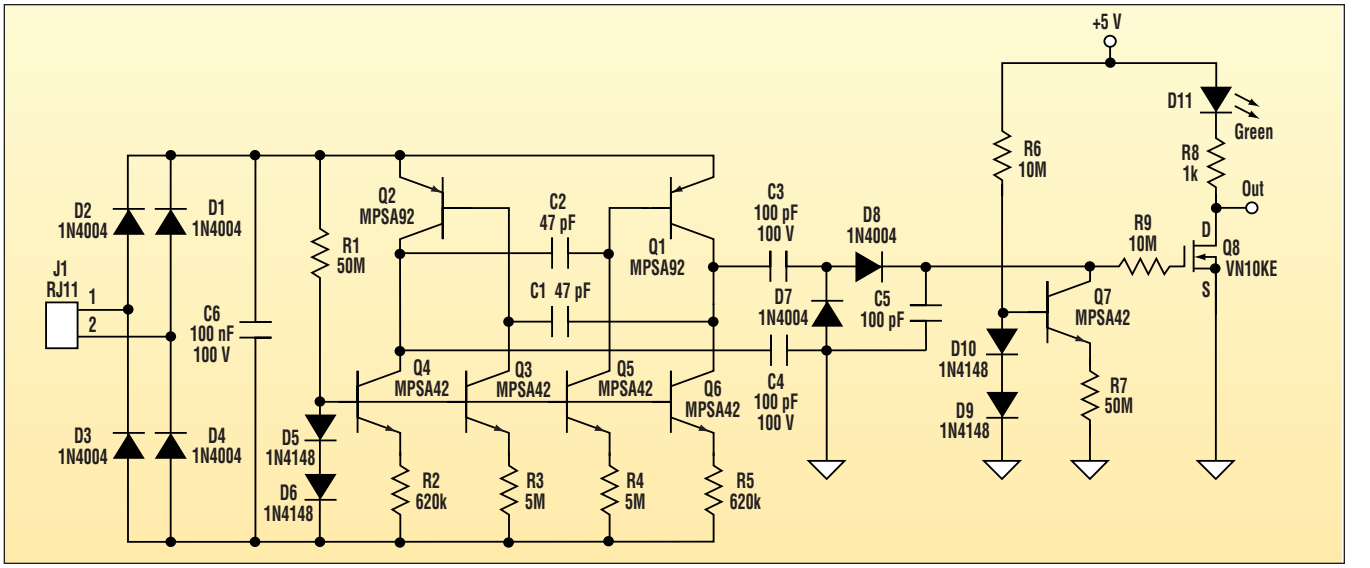
A full-wave rectifier (D1, D2, D3, and D4) and a smoothing capacitor (C6) bias the oscillator from the phone line. C6 has strong impact on the time needed to detect a line break due to the high impedances involved in this circuit.

To meet the galvanic isolation requirements for telephones, the oscillator section must be isolated from the detection circuitry. Traditionally, this has been achieved by means of a transformer. In addition to its cost and size penalties, the transformer is unable to couple dc current, which is needed for detection when the phone remains "on-hook."

At this point, capacitor coupling comes to the rescue. Low-capacitance, high-voltage devices couple the oscillator to the externally supplied detector circuitry. Normally, a capacitor such as C5 would be discharged by the Q7 current source (0.1 µA nominal). But the detector in this application contains a half-wave rectifier that charges C5. This is a better solution than using a simple resistor, which would require a very high value (i.e., greater than 100 MΩ).

Finally, a low-impedance output is provided by means of a MOSFET device. Since the MOSFET includes a gate-source zener diode, it's necessary to employ a large gate resistor. Doing so will prevent excessive loading when it enters the conduction region.

The possibility of high voltage levels in the phone lines determines the ratings of the devices to use. Otherwise, the component values are noncritical. To reduce leakage effects, very high valued resistors (over 10 MΩ) should be implemented by means of multiple 10-MΩ resistors in series. Solder flux must be carefully cleaned. This will prevent leakage around the resistors between the component pads on the printed-circuit (pc) board. Also, pc-board layout must be well planned to minimize the effect of external noise sources caused by the high impedances involved.



A micropower oscillator biased by the telephone line is coupled to an isolated detection circuit to detect possible breaks in the phone line.

Inexpensive "Reflectometer" Locates An Open Circuit Along A Cable

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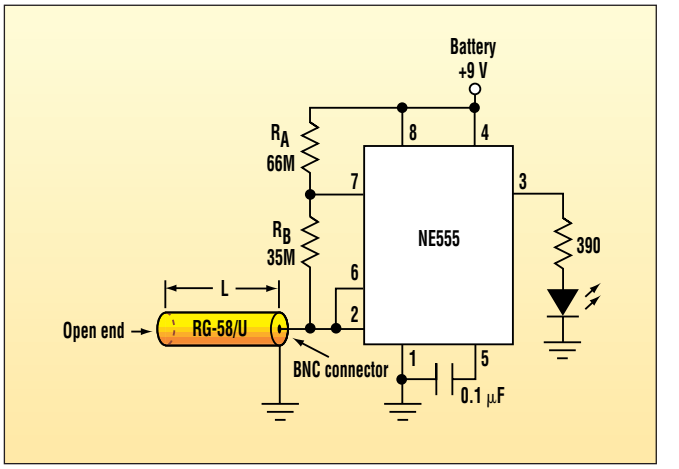
Faults such as opens, shorts, or mismatches can be precisely located along the length of a cable by using a time-domain reflectometer. This device launches a rectangular pulse toward the cable's end and waits for an echo signal. The time between the start of the pulse and the arrival of the echo is then converted in terms of distance, allowing the fault to be accurately located. An oscilloscope is typically used to obtain the elapsed time reading.

To detect ordinary open circuits along the cable, however, a simple, low-cost 555 timer IC operating in astable mode can be employed. Coaxial cables have distributed capacitances per unit length, which may be used to replace an actual capacitor *(see the figure)*.

The LED will blink at a rate inversely related to the length of the cable, or at a frequency = $1.443/[(R_A + 2R_B)C]$. For a 45-meter RG-58/U cable, the LED will flash at f1 = 1.67 Hz. When an open circuit is introduced at L2 = 25 meters from the IC, the LED will blink at about f2 = 3 Hz. By observing the increase in the LED's flash rate, the location (L2) of the open-circuit can be determined using the formula L2/L1 = f1/f2, where L1 = 45 meters.



A simple and inexpensive "reflectometer" locates cable breaks using the distributed cable capacitance and ratiometric calculations.

For other lengths of cable, the value of R_A and R_B may need to be modified to find the values that make visual checking possible. Alternatively, the output of the 555 can be sent to a frequency counter for a more precise reading.

12-Bit Data Recorder Downloads Results To A PC

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CIRCLE 521

This data recorder *(see the figure)* is a simple, low-cost, 12-bit data-acquisition system that can capture data from almost any external transducer and transfer the data to a computer. Temperature, humidity, pressure, air velocity, or light density can be collected. The system can be left unattended for hours or days and can record data with time logging. The recorder's 12-bit accuracy allows users to make high-quality measurements.

Another feature of this device is that it hooks up to the serial port of the computer or laptop. Also, the recorder's PC firmware is made to run under either GWBasic or QBasic.

The data recorder is designed around the ICL7109 (IC3), a dual-slope analog-to-digital converter (ADC). It can make 7.5 conversions per second when using a 3.58-MHz crystal, which gives it 60-Hz rejection, and has an input impedance of 1 MΩ. Although the ADC can make 7.5 conversions per second, the program only captures three to four readings per second. This may seem slow, but it's fast enough for most applications, since data is typically captured over hours or days. In one hour, at three readings per second, 10,800 readings will be taken. For most applications, the program will need to be slowed down to take fewer readings.

Offering a true differential input, the ADC will accept up to a ±2-V input. Yet it can be easily designed to accept a

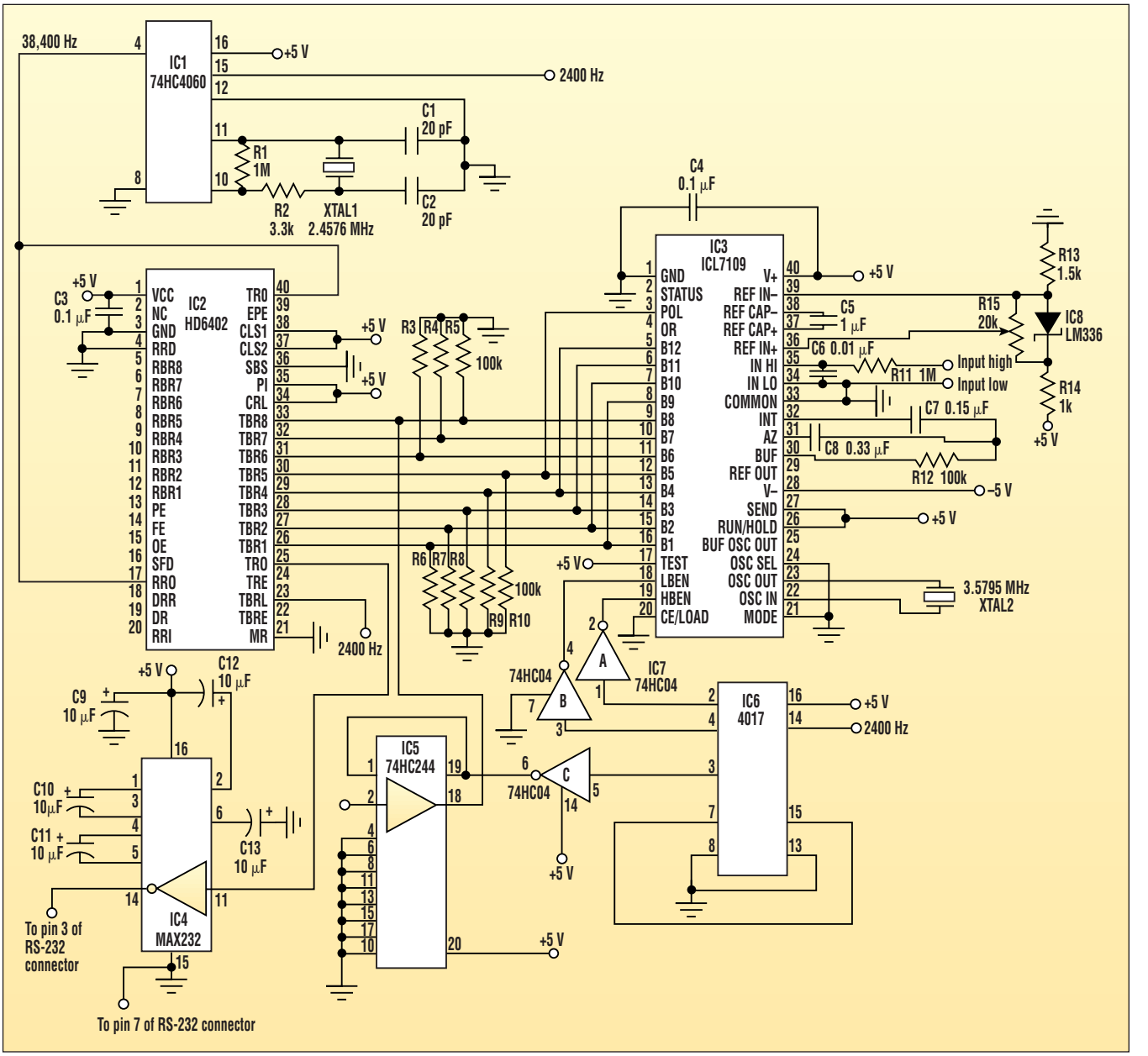
±200-mV input with only minor modifications to the circuit.

To convert the 12-bit ADC's parallel output to a usable RS-232 serial signal, an HD6402 UART (IC2) is used. This UART is set up for 2400 baud, one start bit, eight data bits, one stop bit, and no parity. Most UARTs require a clock signal 16 times the operating baud rate. In this circuit, a 38.4-kHz clock signal is supplied by the 74HC4060 (IC1), a 14-stage binary ripple counter.

Clocked at 2400 Hz, the 4017 divide-by-ten counter (IC6) synchronizes the ADC's LBEN and HBEN outputs as well as a signal sent by the 74HC244 octal buffer (IC5). On the first clock pulse, an output signal is sent to pin 3 of the counter and is inverted by the 74HC04 inverter (IC7). This drives the 74HC244, sending a high signal to pin 33 of the UART. Then the UART sends out the number 128, which the 5-V-powered MAX232 driver/receiver converts to a ±10-V RS-232 signal. At this point, the signal can be processed by the computer.

The program waits for this number before continuing. Pin 2 is set high and inverted on the next clock pulse. Next, this signal triggers the HBEN line on the ADC, activating high-order byte outputs B9 through B12 and the polarity byte. These signals are sent to the UART, translated to an RS-232 signal, and transmitted to the computer. On the third clock pulse, pin 4 goes high and is inverted. This signal enables the LBEN line on the ADC, which drives low-order byte outputs B1 through B8. As described above, the signal is sent to the UART, converted to an RS-232 signal, and sent to the computer. During the fourth clock pulse, the counter is reset and the cycle repeats.

The data-acquisition program prompts the user for the sampling interval, the number of readings, and the destination filename for the data *(see the listing)*. While running, the program dis-



This low-cost 12-bit data acquisition system can be used to capture data from almost any external transducer and transfer it to a computer. The recorder, which connects to the computer's serial port, uses firmware that runs under either GWBasic or QBasic.

```
10 REM ----------------------------------------
11 REM 12-BIT DATA RECORDER DOWNLOADS RESULTS TO PC
15 REM BILL DONOFRIO
16 REM ----------------------------------------
20 INPUT" INPUT NUMBER OF SECONDS BETWEEN READINGS";B
30 INPUT" INPUT NUMBER OF READINGS";Q
40 INPUT" INPUT FILENAME",P$
50 TIME$="00:00:00"
60 CLS
70 OPEN "COM1:2400,N,8,1,CS,DS" AS #1
80 TRIES =10:ON ERROR GOTO 410
90 A$=INPUTS(1,1#)
100 IF ASC(A$)=128 THEN 120 ELSE 90
110 REM WHEN THE NUMBER 128 IS RECEIVED, PROCEED.
111 REM THE NUMBER 128 IS USED TO SYNCHRONIZE THE
112 REM DATA RECORDER WITH THE COMPUTER.
120 B$=INPUT$(1,1#)
130 REM CHECK TO MAKE SURE THE ASCII VALVE OF B$ > 31
140 IF ASC(B$)>31 THEN 120 ELSE 160
150 REM CHECK IF THE NUMBER IS POSITIVE OR NEGATIVE.
151 REM NEGATIVE NUMBERS RANGE FROM 0 TO 15
152 REM POSITIVE NUMBERS RANGE FROM 16 TO 31.
160 IF ASC(B$)<16 THEN 170 ELSE 210
170 C$=INPUT$(1,1#)
180 REM CALCULATION FOR A NEGATIVE NUMBER.
190 X=(CINT(((ASC(B$)*256)+ASC(C$))*-2000/4096))/1000
200 GOTO 240
210 C$-INPUT$(1,1#)
220 REM CALCULATION   FOR A POSITIVE NUMBER.
230 X=(CINT((((ASC(B$)-16)*256)+ASC(C$))*2000/4096))/1000
240 E=E+1
250 T=TIMER
260 REM TIMER CONTROLS THE SPEED OF THE PROGRAM.
270 WHILE TIMER < (T+B)
280 WEND
290 LOCATE 8, 15
300 PRINT" NUMBER OF      VOLTS          TIME"
310 LOCATE 9,15
320 PRINT" READINGS"
330 LOCATE 11,18
340 PRINT E,X,T
350 CLOSE
360 REM OPEN THE DESTINATION FILE
370 OPEN "A",#2,P$
380 WRITE #2, E,X,T
390 IF E=Q THEN 420 ELSE 400
400 GOTO 70
410 RESUME
420 END
```

plays the number of readings, the voltage, and the time that the voltage was recorded. At the same time, it stores the data to the hard drive, where it can be accessed by a spreadsheet.

A relatively compact instruction sequence, this listing contains only 34 lines of programming, without including the REM statements. While the program is relatively simple, it does a number of things to prevent erroneous readings from being taken. Before proceeding, the program must receive the number 128, which synchronizes the data recorder with the computer.

After the computer correctly receives the number 128, it looks for a number between 0 and 31, which contains the HBEN and the polarity byte. If the number is negative, it will range from 0 to 15; if it's positive, it will range from 16 to 31. When this number is obtained, the low-order byte numbers (LBEN) can be processed.

Once the high- and low-order bytes are received, an equation is selected to calculate voltage recorded by the data recorder. Line 190 calculates negative voltages, while line 230 calculates positive voltages. After the voltage is calculated, it's displayed on the monitor with the number of readings and the time. These readings are then saved to the hard disk for future use.

To calibrate the unit, place the positive lead of the voltmeter on pin 36 and the negative on pin 39 of IC3, (ICL7109). Adjust R15, the 20-k trimpot, until the voltage reads 2 V.

Low-Power Solid-State Airflow Detector

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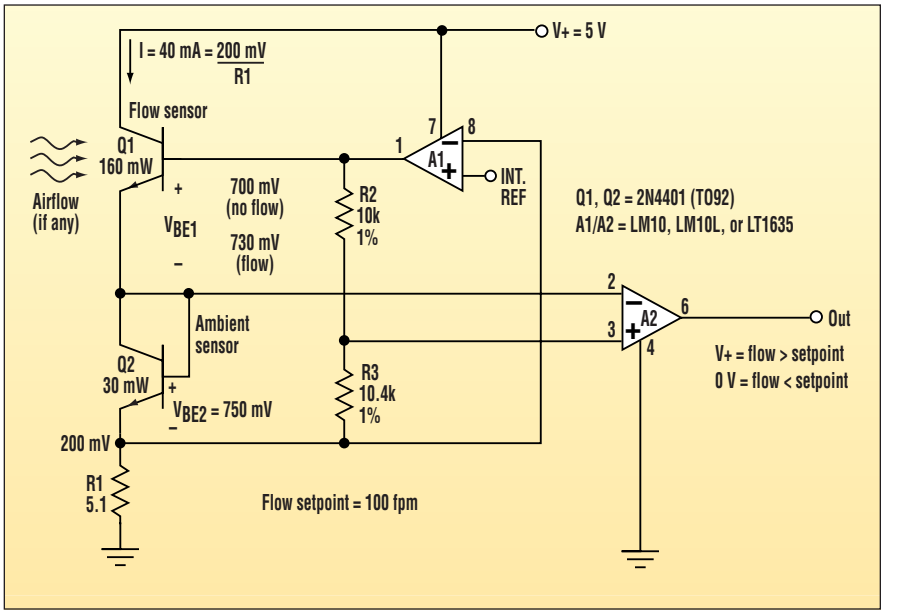
CIRCLE 522

Explicit airflow detection is essential in many applications. High power-density electronics are liable to overheat and self-destruct when cooling-fan failures go unnoticed. Heating and air-conditioning systems often incorporate multipoint monitoring of ventilation-duct flow. Clean-room air-handling systems with undetected dirty, blocked air filters can ruin process yield. Laboratory fume hoods can contain volatile solvents or toxic reagents, making adequate air turn-over critical to safety.

In these and similar scenarios, the consequences of undetected airflow interruption can range from the merely expensive to the frankly dangerous. Therefore, it becomes necessary to use some reliable means for airflow detection. Usually, either a mechanical pressure-actuated vane switch or one of the various types of heat-transfer-based airflow sensors is employed.

An advantage of thermal sensors is that they contain no moving parts. But they often require several watts of heating input to run hot enough to overcome ambient temperature variations. The detector described here is a power-thrifty member of the thermal genre. It employs an ambient-compensated airflow-detection scheme based on differential heating of a series-connected transistor pair *(Fig. 1)*.

In operation, 200-mV reference regulator A1 maintains a constant Q1/Q2 current drive equal to 40 mA (i.e., 200 mV/R1). Since the two transistors pass the same current, their relative power dissipations are determined solely by their respective V_{CE} voltages. For the circuit constants shown, these power levels work out to 4 V × 40 mA = 160 mW for Q1 and 0.75 V × 40 mA = 30 mW



1. This airflow detector uses an ambient-compensated detection scheme based on differential heating of a series-connected transistor pair.

for Q2. The 130-mW heat-flow difference leads to a temperature difference determined by the heat-dissipation-versus-airspeed characteristics of the 2N4401's plastic TO-92 package. The TO-92's thermal-impedance-versus-airspeed characteristic is well approximated by the simple equation shown in Figure 2:

$$Z_T = Z_J + 1/(S_C + K_T\sqrt{A_F})$$

where:

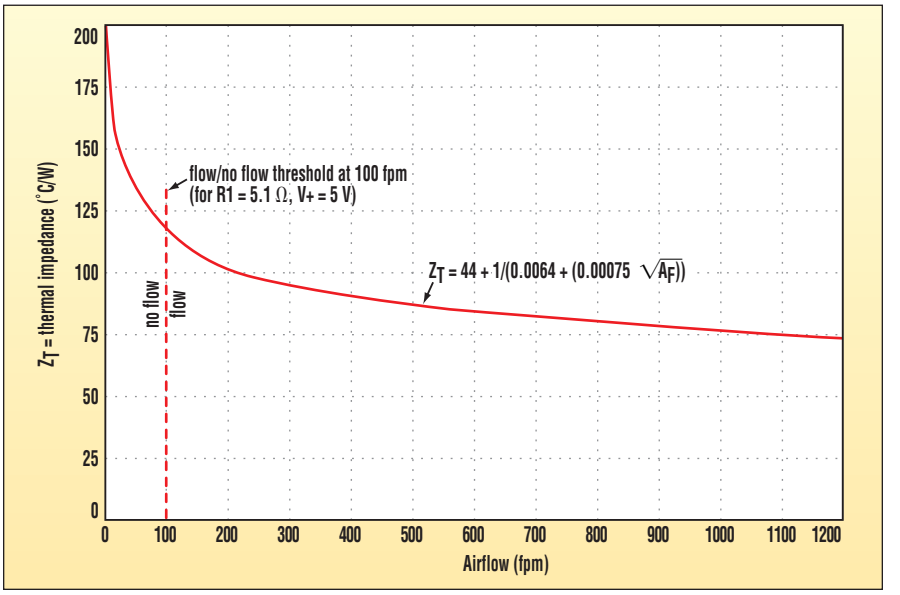
Z_T = "total immersion" junction-to-case thermal impedance = 44 °C/W

S_C = still-air case-to-ambient conductivity = 6.4 mW/°C

K_T = "King's Law" thermal diffusion constant = 750 µW/°C–$\sqrt{\text{fpm}}$

A_F = airspeed in ft./min.

Therefore, the Q1/Q2 temperature differential ranges from 130 mW × 200 °C/W = 26 °C at 0 fpm (zero flow), to 130 mW × 75 °C/W = 10 °C at 1200 fpm (the 14-mph breeze found at the output face of a typical 100-cfm cooling fan). This flow-dependent temperature differential gives rise to a flow-dependent V_{BE} differential via the 2N4401's typical-transistor V_{BE} temperature coefficient of –2 mV/°C. Comparator A2



2. The TO-92 packaging of the sensor selected has a thermal-impedance-versus-airspeed characteristic that is well approximated by a simple equation.

matches this $Q1_{VBE}/Q2_{VBE}$ ratio to R2/R3. Under high airflow, Q1 is cool and $Q1_{VBE}/Q2_{VBE} > R2/R3$, which makes A2's output high (i.e., "flow OK"). With a stagnant airflow (as might connote fan failure, flue fouling, or filter fill-up) Q1 is allowed to heat up, driving $Q1_{VBE}/Q2_{VBE} < R2/R3$. This causes A2's output to slew low, asserting the low-flow fault-alarm condition.

For these circuit constants, the no-flow alarm threshold is 100 fpm *(Fig. 1, again)*. But this "line in the sand" can be easily adjusted. Raising Q1's power dissipation by boosting collector current increases the threshold. Setting R1 = 4 Ω, for instance, would bump Q1's power input to 200 mW and quadruple the low-airspeed setpoint to 400 fpm. Increasing R1 allows the setpoint to be moved the other way (toward a lower flow level). For example, R1 = 6.4 Ω would cool Q1 to a tepid 125 mW and thereby quarter the no-go flow criteria to 25 fpm.

Besides being adaptable to different flow rates, the circuit also can accept different supply voltages. In these cases, R1 must be multiplied by $(V^+ - 1)/4$ to hold Q1's $I_C \times V_C$ heating level constant. Note that a different supply rail also will change the minimum voltage rating needed for A1/A2. LM10Ls are rated for 7 V maximum, while LT1635s are rated for as high as 14 V. The LM10 can tolerate up to 45 V.

One Single-Section Potentiometer Sets The Gain On Two Channels

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What signal conditioning circuit could possibly be easier or more straightforward to design than a dual-channel dc amplifier with a common tracking-gain control? Of course, the obvious way to realize this trivial function is by simply wiring up two identical amplifier channels and controlling the gain of each with matching sections of a dual-element, ganged potentiometer.

Unfortunately, a definite rub lurks in this apparent solution. Ganged pots, particularly the precision multiturn variety, are pricey and often hard-to-find, long-lead-time specialty components. This circuit offers an alternative. It avoids the liabilities of dual pots by controlling the gain of both channels with just one ordinary single-section pot, P *(see the figure)*.

The scheme hinges on the arrangement of P with its wiper terminal grounded. This setup creates two mechanically linked but electrically independent variable resistances: KR and (1 – K)R. K's value represents P's wiper's position. Therefore, it goes from 0 to 1 as P is rotated from full counterclockwise (zero gain) to full clockwise (maximum gain). R is P's total element resistance. The net result for both op amps A1 and A3 is a transfer function linear in K:

$$V_{OUT}/V_{IN} = K(1 + R_G/R) = KG$$

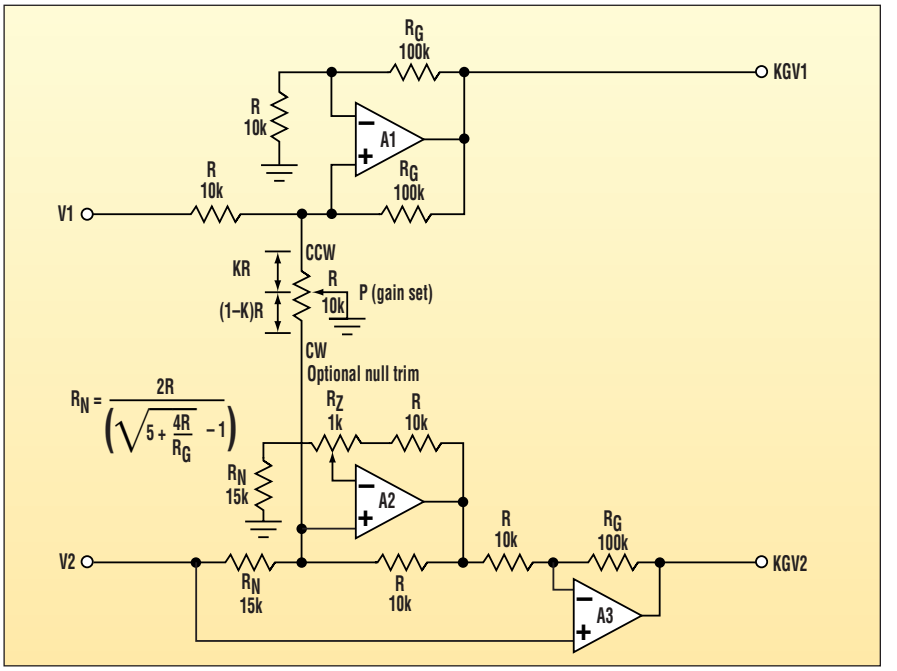
With the example component values shown, G = 11. Yet virtually any gain factor greater than unity can be accommodated by a suitable selection of resistors and op amps.

Why this formula applies to A1 is easy enough to see. Positive feedback from A1's output to P's CCW terminal results in constant current drive to the pot, given by I = V1/R. Therefore, the signal at A1's noninverting input is equal to $I \times K \times R = (V1/R) \times K \times R = K \times V1$. This voltage is boosted by A1's noninverting gain of $G = 1 + R_G/R$ to produce overall gain as a function of K given by $V_{OUT}/V_{IN} = KG$.

The story behind A3's operation is a bit more tangled. Surrounding A2 and P's CW terminal is a topology that produces a signal of $V2(1 - K)(1 + R/R_G)$ at A2's output. After attenuation by A3's feedback network to V2(1 – K), this voltage appears at A3's inverting input. So the differential voltage seen by A3 is $V2 - V2(1 - K) = V2 \times K$. When amplified by A3's gain of $(1 + R_G/R) = G$, this voltage becomes $V2 \times K \times G$. A3's gain, accordingly, is equal to KG, just like A1's.

For applications that are particularly sensitive to a non-zero gain error at K = 0, an optional null-trimmer (R_Z) may be used to accommodate tolerances in the various resistance ratios. This ensures that A1's and A3's gains will simultaneously vanish when P hits its full CCW rotation.

Component selection criteria for potentiometer P include a low resistance-element temperature coefficient (for good gain stability) and a low wiper resistance (for low interchannel crosstalk). Fortunately, potentiometers possessing the quality (and price points) sufficient that make all of this trouble worthwhile generally have



Instead of using a ganged pot, grounding the wiper terminal of a single pot creates two mechanically linked but electrically independent variable resistances: KR and (1–K)R.

excellent characteristics for these two design parameters.

Application of this circuit to manual gain control in stereo/audio and similar contexts where P is a mechanical pot is obvious. But the idea also has utility when P is an electronic digitally controlled potentiometer like the Xicor X9xxx series. For example, P might form the basis of an automatic gain-control loop in applications like an ALC for stereo/audio recording. To provide ALC loop feedback, one channel's signal magnitude, or the sum or the greater of both channels' average signal magnitudes would be compared to a setpoint. The signal would drive both channels to the same tracking/balanced gain.

Use Modified Video As An Analyzer Tool

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CIRCLE 521

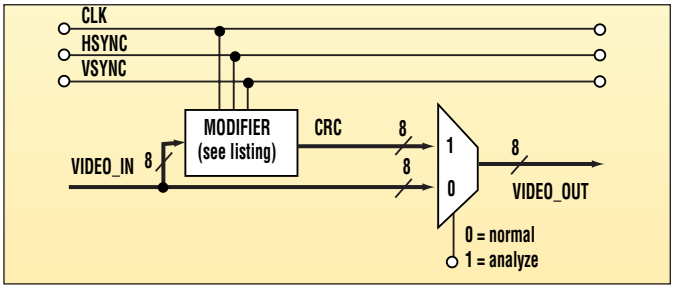
When designing digital video systems, a significant amount of time is spent searching the display for any instabilities arising from noise, cross-talk, or timing violations. These problems become even more difficult if the system contains compression, graphics processors, coders, decoders, or links working close to their maximum performance.

The suggested circuitry replaces the video signal with the checksum of itself, counting from the start of the frame down to the last pixel of the last line *(see the figure)*. A steady video signal will then show a stable and deterministic noise pattern.

Any single-bit error or minute variation in the video signal will change the noise pattern (actually the CRC values) from that point through the rest of the frame. Considering that the eye is very sensitive to change, it's impossible to miss the error or its position.

This design relies on the fact that linear feedback shift registers (LFSR) are used for generating checksums (CRC) as well as producing pseudo-random sequences. For a good paper on the background of CRCs and their implementation in FPGAs, go to *www.cypress.com/pub/appnotes/crc.pdf*.

A CRC of any length with an 8-bit input can be employed. This arrangement uses a 10-bit LFSR with taps on bit 2 and bit 9, since fewer taps makes the logic simpler. Depending on the internal architecture of the FPGA used, the design fits into one or two layers of lookup tables, making it compact and fast *(see the listing)*.



The video modifier replaces the normal video signal with a CRC-based signal to visually exaggerate errors on the video display itself. One of the three video channels (red, blue, and green) is shown.

```
module MODIFIER (VIDEO_IN, VSYNC, HSYNC, CLK,
CRC);

  input         [7:0]   VIDEO_IN;
  input                 VSYNC;
  input                 HSYNC;
  input                 CLK;
  output        [7:0]   CRC;
  reg           [9:0]   C;

  always @(posedge CLK)
    begin
      if (VSYNC==1 && HSYNC==1)
        C <= 8'h00;
      else
        C <= { VIDEO_IN,                    2'b00}^
             { C[7:0],                    C[9:8]}^
             { C[0], 2'b00, (C[7]^C[0]), C[6:1]};
    end
  assign CRC = C[7:0];
```

Stable I_Q Reduces DC-DC Losses

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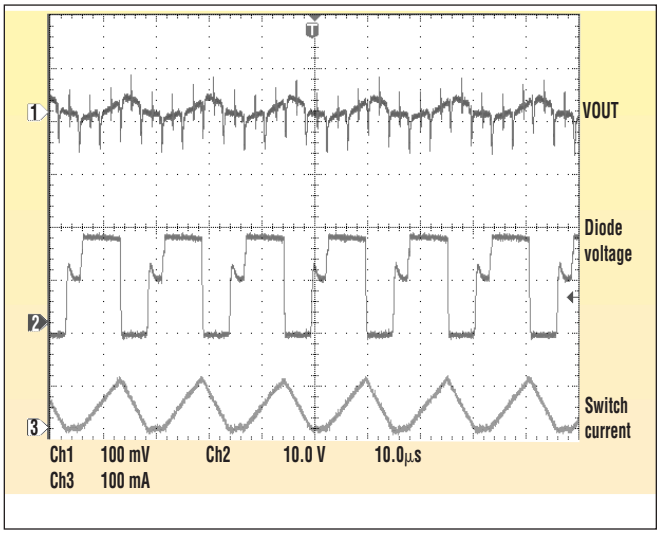
CIRCLE 522

Inexpensive, low-power dc-dc converters can suffer power inefficiencies if the system isn't designed properly. In a low-power converter, the system efficiency is greatly affected by the controller's quiescent current.

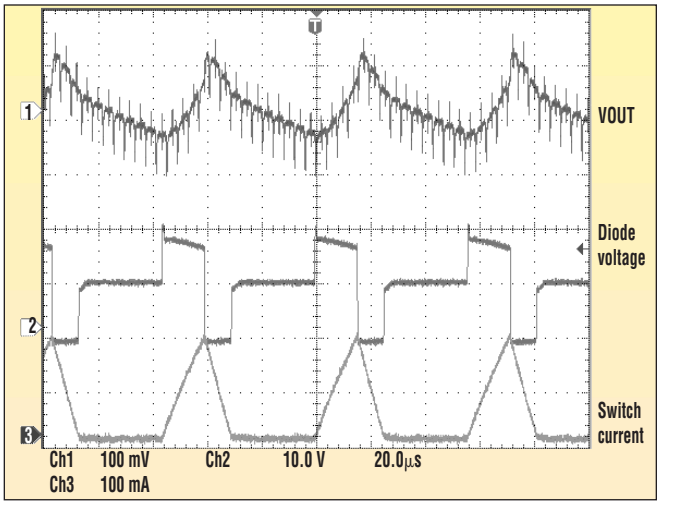
The MC34063A is constructed as either a buck-type or boost-type flexible dc-dc converter, or one that's able to output a negative voltage. Many companies offer the MC34063A in their portfolios. There are differences between designs and IC fabs within and between companies, however. Normal process shifts can make a stable system unstable from lot to lot. To ensure a good design, a system designer must account for all of these factors.

When manufacturing a dc-dc step-down converter, it's best to design the system to operate in discontinuous mode. A step-down converter in continuous mode has zeros in the system loop that must be compensated. In low-power systems, a shift in quiescent current of 1 mA makes a 5% difference in efficiency for a 20-mA input current.

Unstable systems, those whose duty cycle varies more than 10% from cycle to cycle, have higher quiescent currents. The instability in duty cycle causes the controller's internal circuitry to change rapidly, resulting in a higher current draw. Efficiency also is lost in the external circuit components due to higher peak currents. These higher peak currents produce a larger ripple voltage on the input and output. Figures 1 and 2 illustrate the difference in stable and unstable waveforms. Table 1 shows the differences in the critical parameters of a system with an 18-V input, a 9.5-V output, and a 30-mA output.



1. A dc-dc converter designed to maintain a constant 45% duty cycle produces a lower quiescent current and lower output ripple..



2. Unstable duty cycles cause a higher quiescent current, larger current peaks, and a bigger output ripple. The duty cycle alternates from one cycle at 75% to two cycles at 0%.

	Stable Duty Cycle	Unstable Duty Cycle
Switch peak current	95 mA	190mA
Output voltage ripple	40mV	150mV
Efficiency	80%	72%
Quiescent current	1.2 mA	2.5 mA
Duty cycle	Constant 45%	Cycles alternate from one at 75% to two at 0%

To correct the instability, it's necessary to slow the system loop. The first design approach would be to slow the feedback via RC compensation across the feedback op amp. But the MC34063A doesn't provide access to the output of the feedback op amp. Another choice is to maximize the inductance, the current sense resistor, or the output capacitor. Increasing either the resistor or inductor will limit the amount of variation in duty cycle, thereby decreasing the quiescent current.

Precise Trigger Aids In Recording Scope Signals On Plotter

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CIRCLE 523

Analog oscilloscopes remain the lowest-cost means for viewing waveforms. Capturing single-shot or repetitive signals using a film camera, digital camera, or camcorder[1] can be costly, however. Another drawback is that the resulting 2D format renders subsequent signal processing and storage difficult. Recording with a digital storage oscilloscope (DSO) or a DSO board with a dedicated PC, on the other hand, offers many advantages. Unfortunately, these aren't always readily available.

Repetitive signals displayed on an analog oscilloscope may be recorded using the circuit in Figure 1 with the previously described 1-GHz sampling circuit[2]. This technique is useful for all oscilloscope settings up to 50 ns/div. While monitoring several signals in sequence on a single-trace oscilloscope, multiple records may be made on an X-Y plotter in their proper temporal positions. Also, the circuit provides a highlighted panoramic view and a low-jitter output pulse for triggering a sampling oscilloscope[2] or DSO, for displays and plots with much faster sweep speeds.

The buffered CRO time-base ramp T triggers the MAX997 comparator at the plotter-voltage X, which is chosen manually on the 250-Ω, 10-turn potentiometer. Advancing this delay-control advances the plotter pen to plot the waveform. Concurrently, the intensified portion of the CRO beam advances along the displayed signal V_{IN} *(Fig. 2, trace A)*. This highlighted edge acts as a cursor to monitor the progress. The beam is modulated by the MAX997 output, which is connected to the CRO's *Z*-input *(Fig. 2, trace B)*.

Other similar channels may be added as needed to trigger on the

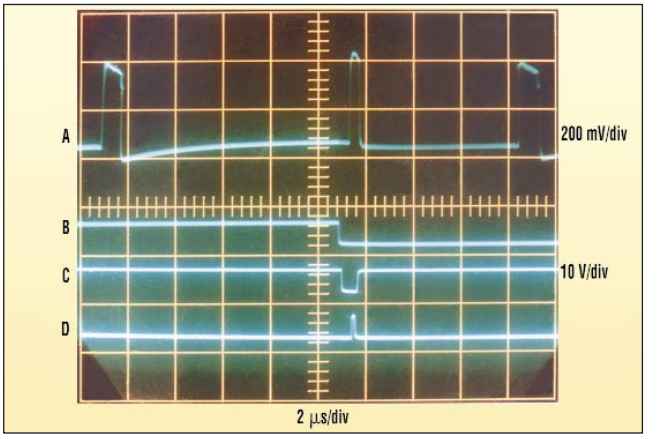
same ramp T at other phases on the waveform. This comparator's negative transition also triggers the MAX961 strobe comparator. If this circuit is installed in place of the fast ramp section, its outputs drive the T/H sampler in reference 2.

Feedback via the 1-nF, 1.5-k network to its latch enable (LE) terminal locks this comparator's state for 650 ns *(Fig. 2, trace C)*. An active probe[1] with a 50-Ω output is used to eliminate the effects of sampler kick-out. This probe connects the input signal to the 50-Ω sampler input V_{IN}, to acquire samples Y for the plotter. Even the graticule can be downloaded along with the plotted traces, if pen marks are made as the cursor crosses the extreme horizontal or vertical lines. Additional lines may be added with a ruler.

Times and voltages at the cursor point may be read at X and Y using a digital voltmeter. These uncalibrated, filtered outputs may also be read by any DSO board, or even by a PC's stereo sound card. Alternatively, incrementing a digital word representing X can drive the MAX997 via a DAC. As a result, the corresponding values of Y may be read by an ADC.

Level triggering on the trace A signal will often produce an unstable display since, like many signals, it contains several possible trigger points. The display may be reliably stabilized by using external triggering on a programmable counter output, set to countdown to the signal pattern's fundamental or subharmonic frequency.

Another option relies on the oscilloscope's variable trigger hold-off to adjust the sweep repetition rate. It does this until it triggers on a single feature of the signal at its pattern fundamental or subharmonic frequency. A different method is used for oscilloscopes lacking this control. In addition to indirectly providing variable trigger hold-off, this technique involves adjusting the variable time/div control. Although this places the time/div setting in an uncalibrated state, the horizontal-magnifier can still restore the desired time per division with the aid of a calibration signal.



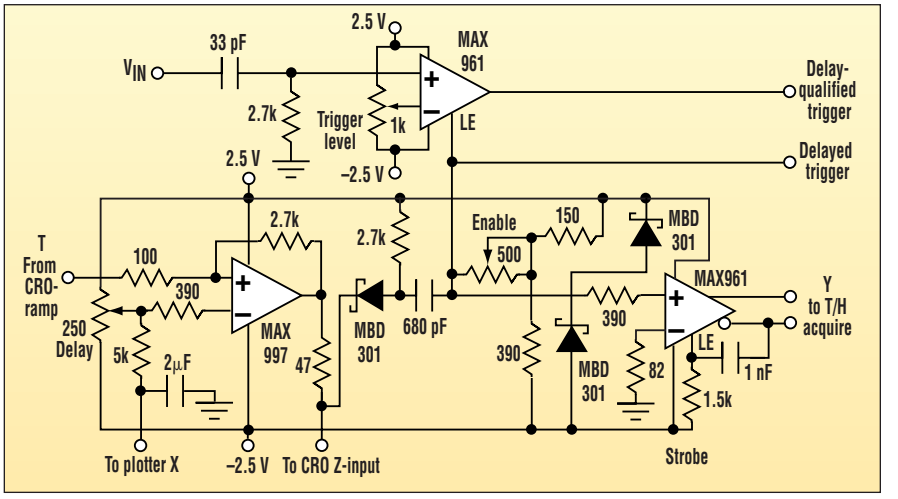
2. The input signal V_{IN}, trace A, is intensity-modulated by the MAX997 output, trace B. Trace C shows one of the MAX961 T/H driver outputs. The delay-qualified trigger, trace D, is exclusively synchronized to the central, narrow pulse at V_{IN}.

It's often necessary to display fine features in a signal concurrently using a faster sweep. Again, level triggering could occur at several points, leading to an unstable display. The highlighted signal illustrates how this circuit can provide a single delayed trigger for triggering a sampling oscilloscope *(Fig. 2, trace B, again)*. This unrefined method will exhibit considerable jitter due to slight ramp and signal fluctuations, however (particularly when the two sweep speeds are widely disparate).

The proper solution is to retrigger on the signal after the delay, which is accomplished using a second MAX961. Most dual-trace oscilloscopes can trigger their delayed sweep in this manner[3]. But since the bandwidth of a sampling oscilloscope is higher, this circuit provides better resolution. Rather than triggering the second oscilloscope itself, the delayed trigger briefly operates the latch enable terminal of the second MAX961.

For the reintroduced V_{IN} signal to produce a trigger pulse as shown here, the comparator must be enabled by the delayed trigger *(Figure 2, trace D)*. The 500-Ω control sets the enable window between 100 ns and 600 ns. Using the sign of the voltage level set on the 1-k potentiometer, it can be determined whether the triggering occurs on a positive or negative edge.

This resynchronized, delay-qualified trigger will reliably trigger any other oscilloscope with only a 4.5-ns propagation delay through the MAX961. The trigger system routinely displays fine features, like this short central pulse on a 1-GHz oscilloscope with less than 20-ps jitter *(Figure 2, trace A, again)*. It consistently rejects all other possible trigger edges outside the enable window. Together with its display oscilloscope, this circuit furnishes a precise delay-qualified trigger peripheral for a sampling oscilloscope[2] or any other instrument lacking this feature.



1. A 250-Ω control sets the delay of the MAX997's step pulse to modulate the CRO beam, trigger the strobe and the T/H for the X-Y plotter, and enable the delay-qualified trigger.

References:

1. Hickman, "Towards A 500-MHz Scope Add-On," *Electronics World*, March, 2000, p. 202.

2. H. Houtman, "1-GHZ Sampling Oscilloscope Front End Is Easily Modified," *Electronic Design*, September 18, 2000, p. 175.

3. J. Ganssle, "Delayed Sweep: A Critical Tool," *EDN*, April 27, 1995, p. 50.

Tunable Diode Laser Photocurrent Amplifier Has 80-dB Logarithmic Gain

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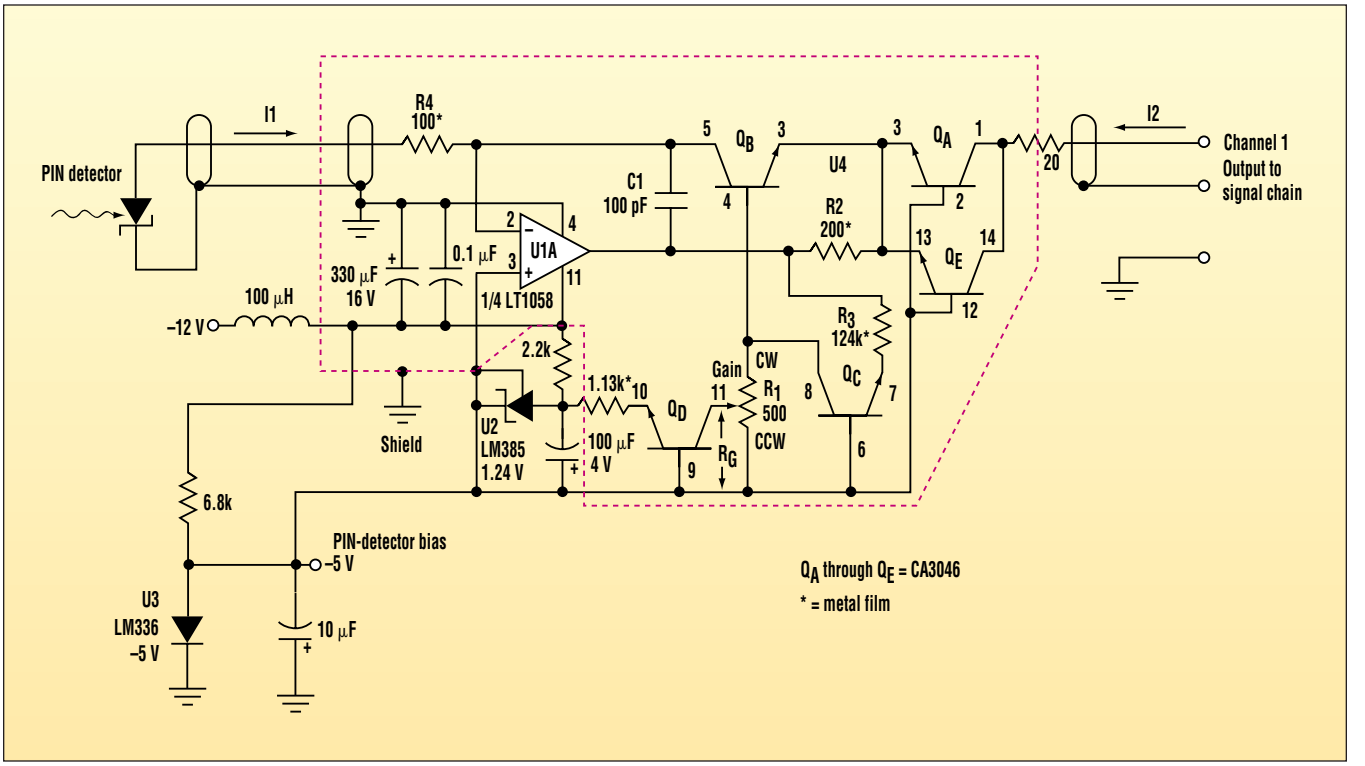
CIRCLE 451

Tunable diode lasers (TDLs) are of increasing importance in many optoelectronic applications, including wavelength division multiplex communications and chemical analytical spectroscopy. TDLs are unexcelled as coherent, high-intensity, wavelength-agile, tunable monochromatic light sources. They provide high throughput and sensitivity in a wide variety of precision optical instrumentation.

For example, two dual-channel TDL spectrometers, designed for water vapor and carbon dioxide abundance and isotopic ratio measurements, were part of the science payload of the (ill-fated) Mars Polar Lander *(see "Flash-ROM-Based Multichannel Arbitrary Waveform Generator," W. Stephen Woodward and Randy D. May,* ELECTRONIC DESIGN, *April 19, 1999, p. 86)*.

Optical measurements incorporating high-performance sources like TDLs need similarly high-performance optoelectronic detectors and signal-processing circuitry. This photocurrent amplifier incorporates a number of design characteristics to accommodate the peculiarities of analytical spectrometer alignment *(see the figure)*. At the same time, these features aim at preserving the signal quality (SNR) in the inherently noisy environment of aerospace applications.

The performance of any chemical analytical spectrometer directly depends upon two factors. Such devices rely on both the availability and the use of an intense source that matches the absorption spectrum of the analyte molecule of interest (e.g., CO_2 or H_2O). Fabricating TDLs with output wavelengths that accurately fit the predetermined spectra of the chosen analyte molecules is a specialized and still-evolving art. Consequently, some laser performance parameters (e.g., power output) must be relaxed in the interest



This TDL spectrometer detector-amplifier has a stable, wide-range gain adjustment to accommodate up to several orders of magnitude of variation in detector-incident light levels. This is achieved by exploiting the exponential characteristic of the V_{BE} junctions in the CA3046 array.

of achieving reasonable device yields.

A useful TDL spectrometer detector-amplifier needs a stable, wide-range gain adjustment to accommodate up to several orders of magnitude of variation in detector-incident light levels. To achieve this functionality, the amplifier shown exploits the exponential transconductance versus V_{BE} behavior of the CA3046 bipolar transistor array:

$Q_A - Q_E$: $A_Q = 2 \times EXP(11{,}000 \times V_{BB}/T_{KELVIN})$.

The 1.24-V voltage reference U2 cooperates with Q_D to sink an approximately −500-μA temperature-compensated bias current from the wiper of R1. An additional +1.5 μA/K must be factored in to accommodate the 0.3%/K T_{KELVIN} dependence of the transistor's exponential gain behavior. Therefore, as R1's wiper is adjusted from CCW to CW, Q_B's V_B (V_{BB}) varies linearly from 0 to −250 mV (at 25°C + 0.3%/K). This causes the overall amplifier current gain (I2/I1) to shoot from 2 to 20,000 (6 to 86 dB).

Positive feedback components Q_C and R3 improve the amplifier linearity by compensating for the emitter-resistance-related log-nonconformity of Q_A and Q_E. This nonlinearity-canceling "tweak" comes from adding a bias term to V_{BB} equal to I2 × 0.8 Ω = 800 μV/mA. That's enough to cancel Q_A's and Q_B's paralleled emitter resistances of 1.6 Ω each, which is typical of the transistors in a CA3046 array.

Regrettably, ground-loop related noise is common in avionics applications where digital and analog components are often forced to operate in close proximity. Immunity to ground-loop-induced noise is provided by the current-mode amplifier output signal. The voltage compliance of the I2 output is ±5 volts.

Hot-Swap Controller Creates A Flexible Current Limiter

Luca Vassalli

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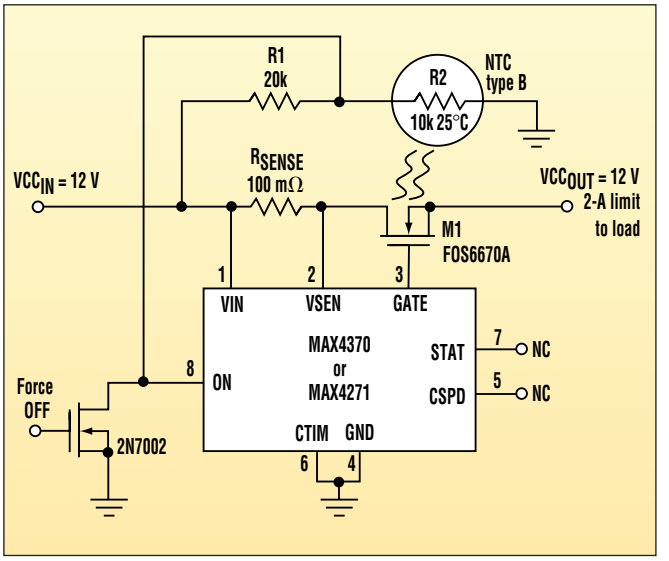
Current limiting is often necessary to protect a power supply from short circuits and load surges, which can pull the supply voltage low. ICs containing p-channel MOSFETs and adjustable current limits are available for this purpose. Yet most are limited to 5-V systems with a typical maximum current limit of 2 A and low accuracy (20% to 50%, according to the manufacturers).

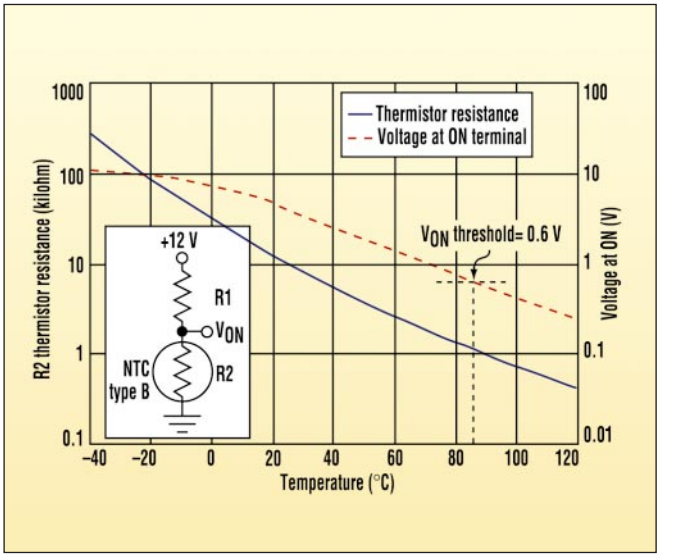
With the current-regulation capability of these "hot-swap controllers," it's possible to create a more accurate and versatile current limiter *(Fig. 1)*. The external MOSFET and sense resistor let this device protect a system operating from 3 to 12 V. Connecting the CTIM terminal to ground disables the IC's dual-speed/bi-level feature. This forces the device into startup mode, which regulates the current at the limit preset by the sense resistor [$I_{LIM} = (200\ mV)/R_{SENSE}$].

Achievable accuracy is 10% plus the sense-resistor error—a great improvement over the approach mentioned above. This circuit does more than protect against short circuits and current surges. It also limits the inrush current and ramps the supply voltage by limiting the MOSFET's gate-charging current to 100 mA. Driving the ON terminal (pin 8) to ground disconnects the load.

The external MOSFET easily handles normal operation. But a short circuit elevates its power dissipation and die temperature by imposing the full supply voltage across the MOSFET and sense resistor. If this condition exists



1. Combining a few components with a hot-swap controller IC yields a precision current-limited supply for 3- to 12-V loads.



2. The NTC thermistor resistance variation with temperature is shown. A thermal cutoff threshold of 85°C results.

for an extended period, thermal protection becomes necessary.

Thermal protection can be added by placing an NTC temperature monitor close to the MOSFET (on the back side of the board). IC1's internal precision comparator (accessible at the ON terminal) can then be used to disconnect the load when this monitor detects an excessive temperature. For example, the components needed toprovide a temperature threshold of 85°C when VCC_{IN} = 12 V are R1 (20 kΩ), and the type-B thermistor R2 (10 kΩ at 25°C)*(Fig. 2)*.

Precision Current Source Design Employs Bootstrapped Integrator

Clayton B. Grantham

CIRCLE 453

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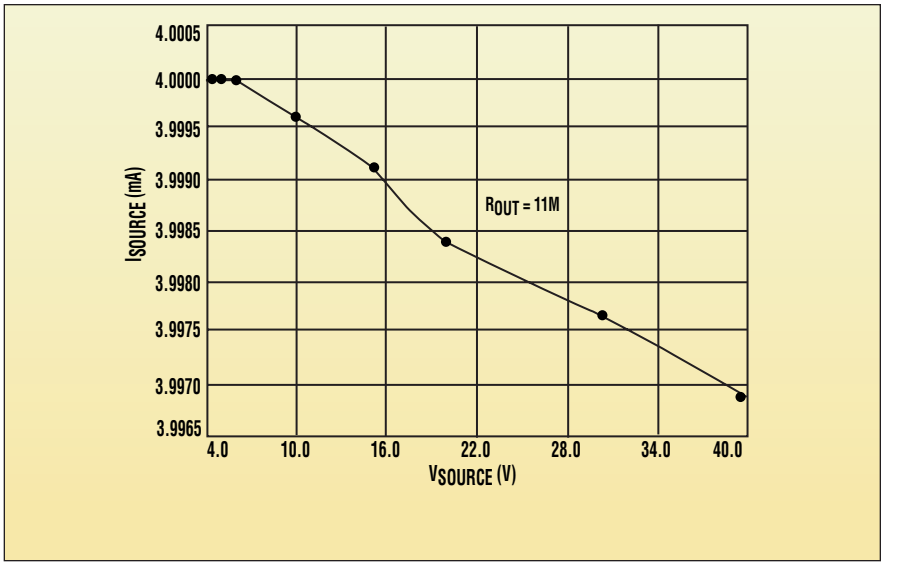
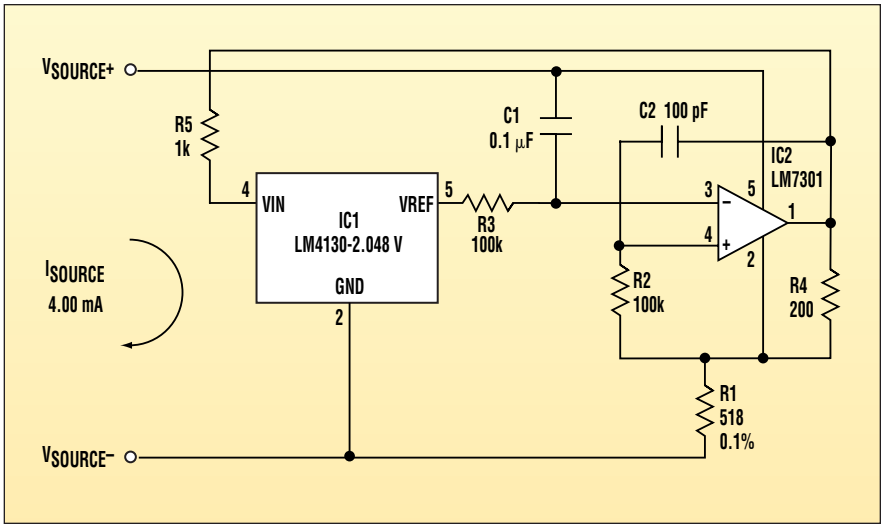
The general-purpose current source in Figure 1 is accurate within 1% and insensitive to temperature (less than 50 ppm/°C). It also has a high output resistance and a wide compliance range (4.3 to 34 V). This composite configuration uses an IC voltage reference (IC1) and resistor (R1) to create a current source that follows the expression $I_{SOURCE} = V_{REF}/R1$ + IC1's ground current.

IC1's accuracy is extended beyond its 5.5-V supply-voltage limitation (CMOS). This is achieved using a bootstrap integrator made by IC2, R2, and C2, which keeps IC1's input within compliance. Consequently, a precise current source that matches the wide supply range of IC2 is produced.

IC2 is the pass device that keeps IC1's input within compliance (below 5.5 V). With the bootstrapping of IC2, this configuration doesn't have an additional IC2 ground-current error. IC2, R2, and C2 form an integrator that forces IC1's input to keep the voltage across R1 equal to V_{REF}. At the same time, IC2's output sources current through R4. This current sums with IC2's negative supply current. I_{SOURCE} is generated by this current through R1 plus a small IC1 ground-current offset error (50 µA).



2. This plot of I_{SOURCE} versus V_{SOURCE} demonstrates that the composite op amp and voltage-reference current source has an output resistance of approximately 11 MΩ.



1. This composite CMOS voltage reference and op-amp integrator forms a general-purpose current source. The bootstrap configuration eliminates IC2's ground-current error.

The error in accurately setting I_{SOURCE} with this composite configuration is derived from three sources. V_{REF} and R1 are both available in 0.1% tolerance. IC1's ground-current variation of ±7 µA on 50 µA translates to an additional 0.2% tolerance. When these tolerances are combined, the total I_{SOURCE} tolerance is under 1%.

Similarly, I_{SOURCE}'s insensitivity to temperatures from –40°C to 85°C is a function of the temperature coefficients of V_{REF}, R1, and IC1's ground current. The LM4130 is available in a 0.1% tolerance with 20 ppm/°C TC grade. Inexpensive resistors are commonly available in 0.1% tolerance with 25 ppm/°C TC grade. The LM4130's ground-current variation of

±5 µA on 50 µA over temperature provides an additional TC of 20 ppm/ C. Therefore, the total I_{SOURCE} TC is lower than 50 ppm/°C.

C1 enables startup of the configuration from a V_{SOURCE} power-on step. With this choice of C1, the startup delay-time is 100 ms from a 5-V step. For a fast-edged V_{SOURCE}, a 1-ms startup can be obtained by using a 0.001 µF cap for C1. R3 is used to isolate V_{REF} from the integrator during startup. R4 level-shifts IC2's output (which is IC1's input) up above V_{REF}, while R5 current limits IC1's input during startup.

IC2 was selected because of its wide supply range and input common-mode range, which includes its negative supply. The typical ground current of IC2 (0.6 mA) restricts the lowest setpoint for I_{SOURCE}. IC2's maximum output current (10 mA) limits the highest setpoint for I_{SOURCE}.

Figure 2 shows I_{SOURCE} versus voltage with an output resistance greater than 10 MΩ. The compliance voltage is from 4.3 V to 34 V. This upper margin is the maximum IC2 compliance plus V_{REF}. The lower limit is the minimum IC2 compliance plus V_{REF}.

12-V Amplifier Is Designed Using Low-Voltage Digital Potentiometer

Chuck Wojslaw and Paul Standish

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Analog circuits today are typically biased from ±5 V to ±18 V. But the trend is toward lower voltages. For this reason, many components are designed to operate primarily in ±5-V systems. One example is the digitally controlled potentiometer (DCP). Can a low-voltage DCP be employed in a high-voltage circuit such as an amplifier? The answer is yes, if caution is paid to how and where the DCP is used.

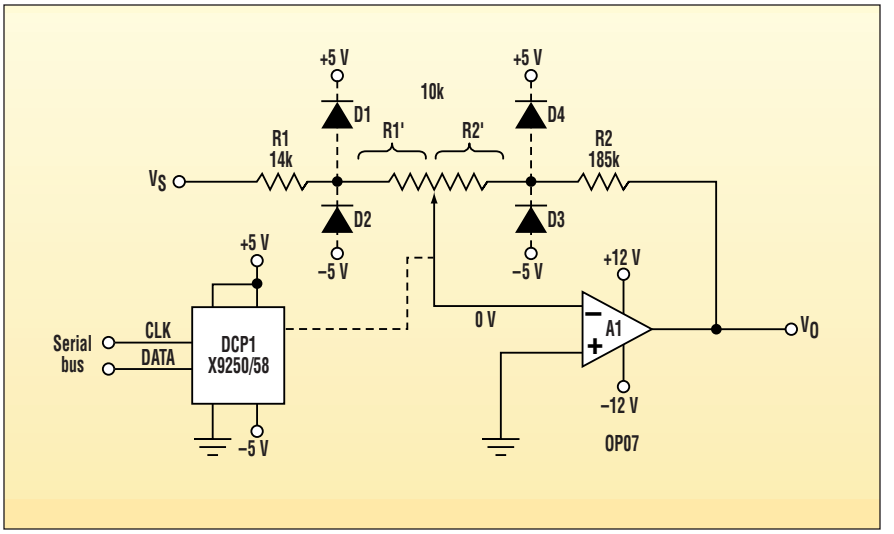
This ±12-V inverting amplifier circuit is designed for a nominal gain of ten *(Fig. 1)*. Use of a low-voltage, programmable DCP extends the programmable gain limits from 7.7 to 13.9. Xicor's 256-tap X9250/58 provides a gain resolution of 0.024 over this range. Therefore, it allows accurate gain setting without using expensive, precision resistors.

One feature of the inverting configuration is that the wiper is connected to 0 V or virtual ground. Consequently, any high common-mode voltages on the potentiometer terminals are removed. Another benefit is that the wiper resistance of the DCP is in series with the high input-resistance of the operational amplifier. So any error due to the wiper resistance is eliminated as well.

For the inverting amplifier, the gain is given by:

$$G = -(R2' + R2)/(R1' + R1)$$

A noninverting amplifier circuit can't be used since it lacks a virtual ground. The relative values of the potentiometer resistances R1′ and R2′ compared to R1 and R2 are established by the relative values of the maximum DCP and circuit voltages. For a 12-V circuit and a 5-V DCP, R1′ and R2′ must be less than five-sevenths of R1 and R2. Clamping-diodes D1 through D4 offer overvoltage protection to the DCP during power-up, power-down, and fault conditions.



This amplifier's virtual ground allows the ±12-V circuit shown to use a ±5-V digital pot for gain control. Due to the need for a virtual ground, noninverting configurations can't be used.

Linear-RMS Phase Control Improves Thyristor-Based Thermostat

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CIRCLE 520

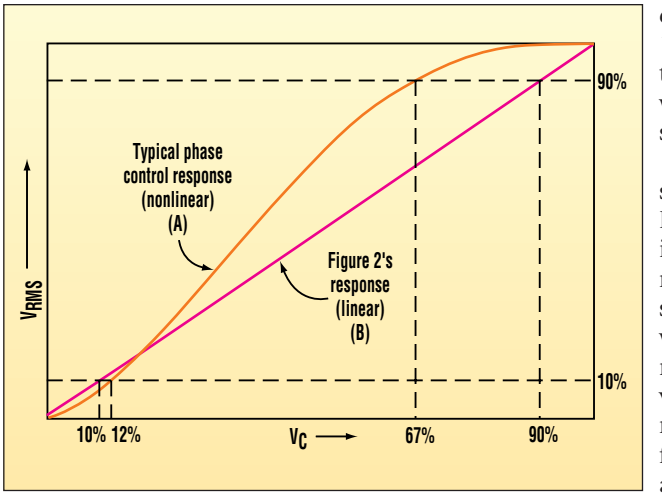
Precision temperature control circuits for small thermal loads like oscillator crystals and voltage references tend to be fairly easy to design. This is because simple, well-behaved, linear-output drivers running from regulated dc supplies are often used for straightforward heater control. While handy for low-wattage heaters, linear drive is an unappealing solution for satisfying the demands of bigger loads and their bigger heaters. Those thirsty power consumers call for more efficient switch-mode power-handling circuits.

This pursuit of efficiency frequently leads to the use of power-control circuits based on thyristors with 60-Hz phase-angle triggering. Cheap and robust, thyristor phase-angle circuits can easily drive multikilowatt heaters while achieving greater than 90% efficiency. Unfortunately, a serious obstacle hinders the use of these devices in precision control applications.

The problem can be seen in this typical thyristor phase-control response plot *(Fig. 1, curve A)*. Here, 80% of the thyristor rms output range (0.1 to 0.9 of full scale) is spanned by only 55% of the control-input range (0.12 to 0.67). This severe nonlinearity complicates the simultaneous achievement of adequate system feedback gain and nonoscillatory stability over the full range of heater control inputs.

Figure 2's thermostat dodges this bullet by incorporating a control-voltage-to-trigger-angle converter circuit (A4, D1, C3, Q5, and R2). The circuit achieves an essentially linear relationship between the control voltage and the rms heater drive *(Fig. 1, curve B)*. On each positive half-cycle of the silicon controlled rectifier (SCR) anode voltage, V_{AC}, timing capacitor C3 begins charging through D1 and R2. A4 compares the accumulating voltage (V_{C3}) to the heater control voltage on C2. A trigger pulse is issued to the SCR gate when $V_{C3} = V_{C2}$. This, in turn, generates the V_{C2}/SCR phase-conversion function and also resets C3 via Q5.

It's the sigmoidal (rather than triangular) shape of the V_{C3} waveform that produces the excellent linearity of the V_{C2}/rms-heater voltage conversion. This wave shape results in an inverse-sigmoidal relationship between V_{C2} and the SCR trigger timing. Consequently, the sigmoidal functionality of firing-angle-to-thyristor/heater current is accurately compensated and linearized. Although as illustrated the converter implements a 0° to 180° half-wave ac-control function, modification for full-wave 360° operation would be straightforward.



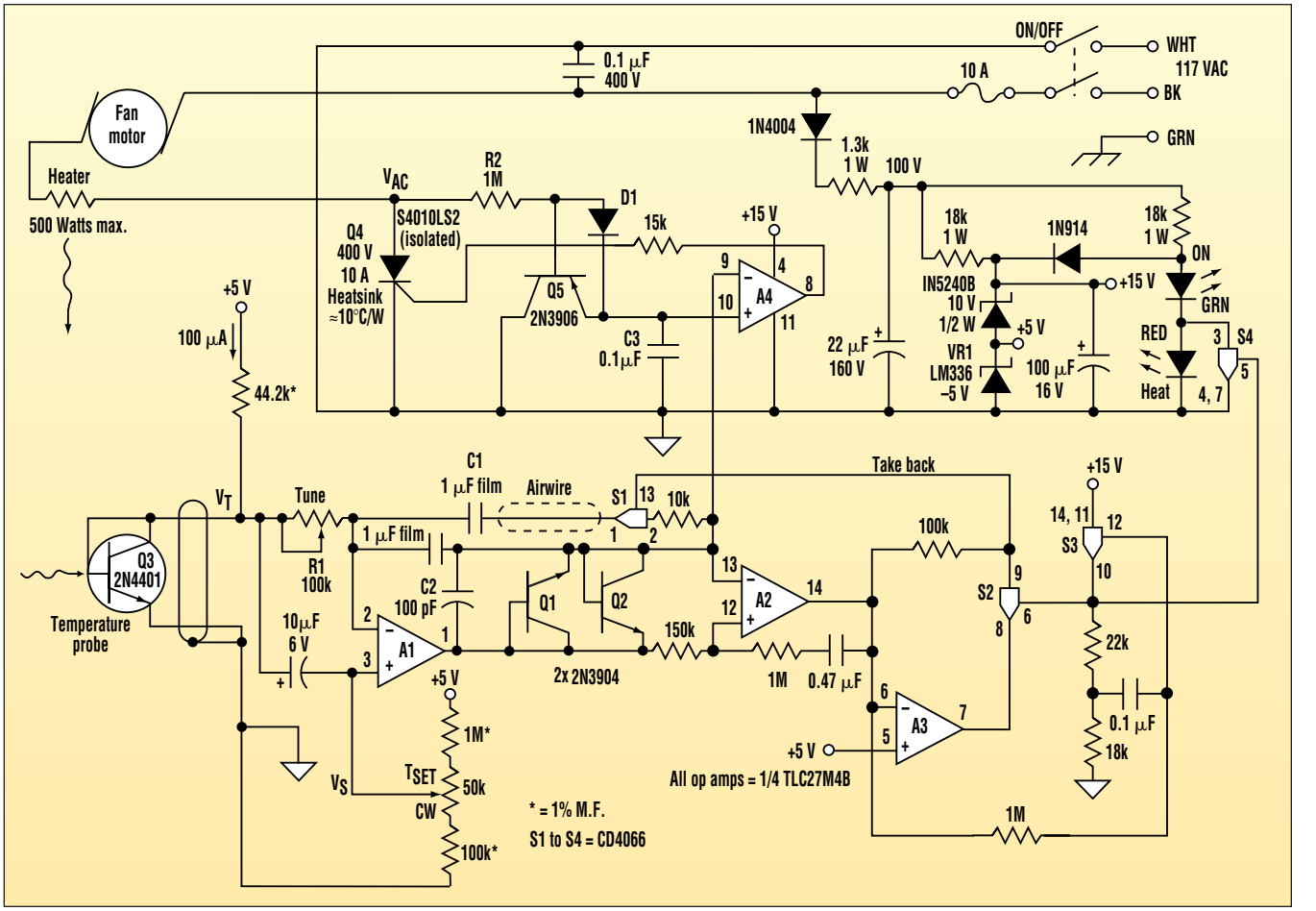
1. A typical thyristor phase-control response (plot A) compresses 80% of the thyristor rms output range in 55% of the control-input range. A circuit using a control-voltage-to-trigger angle converter produces both adequate gain and non-oscillatory stability (polt B).

Figure 2's circuit was designed to serve an Air Curtain Incubator application that satisfies a requirement for accurate thermostasis of biological samples and culture dishes when transferred from a cabinet incubator to a microscope viewing stage. This application requires the generation of a flow of temperature-controlled air. In this case, the airflow is conveniently and cheaply produced by an ordinary, unmodified household hair dryer.

The airstream temperature is sensed using Q3's V_{BE} temperature coefficient (–2 mV/°C). Q3's V_{BE} (V_T) is compared to the 0.43- to 0.65-V setpoint voltage (V_S). After being integrated, the $V_S - V_T$ error signal is applied to A4's voltage-to-trigger-angle converter circuit.

Due to the finite velocity of the heat-transporting airstream, there's a thermal time lag between heater H and sensor Q3. This interval complicates servo stability issues and requires the use of a robust, integrating, convergence-by-bisection feedback control algorithm *(see "Take Back Half: A Novel Integrating Temperature-Control Algorithm," ELECTRONIC DESIGN, Dec. 4, 2000, p. 132)*.

Take Back Half (TBH) damps oscillations and stabilizes the servo loop by revising the estimate of the optimum heater input at each setpoint ($V_T = V_S$) crossing. Comparator A2 detects these setpoint crossings by going high when V_T is less than V_S and low when



2. The thermostat circuit uses a control-voltage-to-trigger-angle converter circuit to achieve a linear relationship between control voltage and the rms heater drive. The thermal lag between heater H and sensor Q3 is addressed by using a convergence-by-bisection control algorithm.

V_T is greater than V_S. The positive feedback network around A2 keeps these logic transitions snappy.

Meanwhile, the role of TBH variables H_O and H are served by the sample-and-hold capacitor C1 and integrator cap C2, respectively. Further details of the workings of the analog TBH controller circuitry can be found in, *"Circuit Enables Precision Control In Radiant Heating Systems,"* ELECTRONIC DESIGN, *Jan. 8, 2001, p. 131.*

Compact, Inductorless Boost Circuit Regulates White LED Bias

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CIRCLE 521

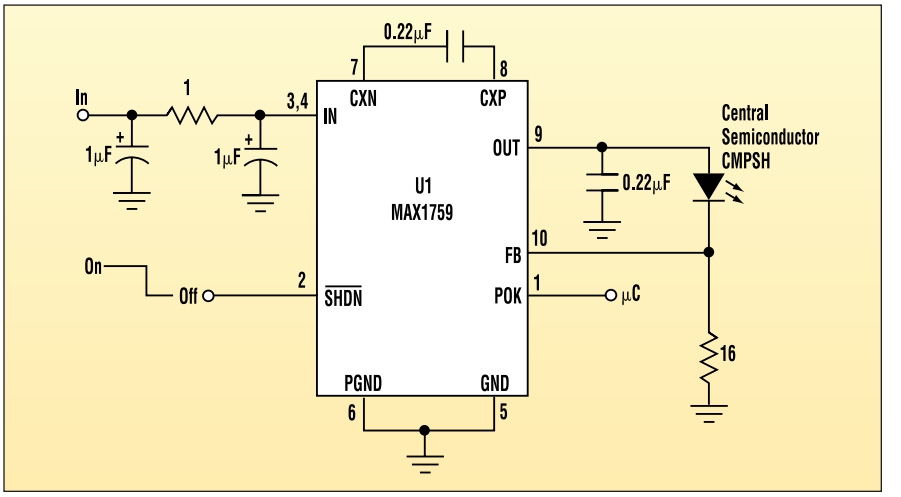
The increasing use of color LCDs in handheld equipment has created a need for smaller and cheaper sources of white backlight. In the past, cold-cathode fluorescent lamps (CCFLs) and electroluminescent (EL) panels have been employed. But such circuits are excessively large, expensive, and complex for today's handheld consumer electronics devices. Fortunately, recent advances in LED technology have produced LEDs that emit white light. White LEDs have several advantages over conventional backlight types, including small size, low cost, minimal complexity, and high reliability.

To obtain white light, an LED is simply forward-biased (the typical forward-bias voltage for white LEDs is about 3.5 V ±10%). A boost circuit is generally required since the white LED's forward voltage is often close to or greater than the battery voltage.

The conventional approach to this problem relies on a boost regulator that biases the LEDs via a ballast resistor. This arrangement has its drawbacks, however. For instance, the wide variation of forward voltage in white LEDs causes a large variation in bias current and the resulting light output. Also, the conventional boost converter has a dc path between the input and the output (even in shutdown) that allows an inactive LED to drain the battery.

This compact circuit overcomes these problems *(see the figure)*. U1 is a regulated buck/boost charge pump in a small µMAX package, with 100-mA output-current capability. Configured as shown, the circuit directly regulates bias current flowing through the white LED. By biasing multiple white LEDs in parallel, good light distribution can be achieved. U1's design eliminates the troublesome input-output path in shutdown. Its $\overline{\text{SHDN}}$ input (pin 2) lets users turn the backlight on and off. The circuit also includes a power-OK output (POK), which signals a microprocessor when the backlight is available.

Though not necessary in this case, the input RC π - filter limits the voltage ripple reflected back to the input to just 40 mV p-p (for V_{IN} = 3.6 V). Since the output voltage ripple is not visible to the human eye, it's of secondary concern in this application. This allows for the use of a small (0.22 µF) output capacitor. Even with this small output capacitor, the output ripple is only 40 mV p-p.



Unorthodox connections enable this charge-pump IC to directly regulate the current through a white LED backlight. The IC's shutdown feature prevents battery drain when the LED is off.

Design Method Allows Tradeoffs In Anti-Aliasing Filter Design

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This idea details a design method for making anti-aliasing prefilter parameter tradeoffs between several factors. These factors include the filter pass-band magnitude accuracy, the filter order (the number of poles), the ratio of sample frequency to the filter bandwidth of interest, and the filter attenuation at integer multiples of the sample frequency.

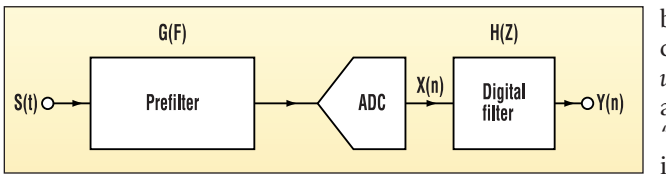
The gain magnitude and corner frequency expressions for a unity-gain low-pass Butterworth are given by:

$$G^2(kF_S) = \frac{1}{1+\left(\frac{1-ratio^2}{ratio^2}\right)\left(\frac{kF_S}{F_b}\right)^{2n}} \quad \text{for } k = 1,\ 2\ ,3,... \tag{1}$$

$$F_{3dB} = F_b = \left(\frac{ratio^2}{1-ratio^2}\right)^{\frac{1}{2n}} \tag{2}$$

where:

ratio = filter accuracy (e.g., 0.98 = 2%) at F_b



1. A typical DSP digital-filter channel incorporates an anti-aliasing prefilter prior to the analog-to-digital converter.

n = filter order

F_S = sample frequency in Hertz

F_b = bandwidth of interest in Hertz

Figure 1 shows the anti-aliasing prefilter ahead of the analog-to-digital converter (ADC) in a DSP's digital-filter channel. The low-pass digital filter's gain characteristic, H(Z), is detailed in Figure 2a. Spectra in the bands (bandwidth = $2F_b$) centered at multiples of F_S show up in the baseband of interest (0, F_b) as aliased signals. Figure 2b demonstrates the prefilter characteristic where the sampled spectra escaping the bands shown are aliased as unwanted energy. Via the prefilter, these spectra are attenuated to within practical limits.

The prefilter design program calculates the gain (in dB) for each of 10 bands (to view the code listing, go to *www.PlanetEE.com* and click on the "Ideas for Design" icon). Also displayed is the gain-sum-squared (in dB).

Another function of the program is to output the filter's −3-dB corner frequency and the RC time constant for a single-pole filter. Some prefilter characteristics for Band #1 are shown in the table. Observe that a large amount of oversampling is required (F_S/F_b = 130) for an RC single-pole −25-dB filter.

Noise samples escaping the prefilter are combined in a root-sum-of-the-squares manner, which represents the rms noise voltage in the baseband (0, F_b). The noise voltage is expressed as shown in Equation 3:

$$\frac{Erms}{\sqrt{2F_b}} = \sqrt{G^2(F_s)e_1^2 + G^2(2F_s)e_2^2 + \ldots G^2(kF_s)e_k^2} \tag{3}$$

PREFILTER ATTENUATION VERSUS SAMPLE RATE/BASE FREQUENCY RATIO FOR VARIOUS FILTER ORDERS

F_S/F_b Ratio	Prefilter order (n) 1	2	3	4	5	6
	Prefilter attenuation in decibels					
2	0.34	1.22	3.62	7.92	13.38	19.25
3	0.73	4.22	11.99	21.28	30.79	40.33
4	1.22	7.92	19.25	31.24	43.28	55.32
5	1.78	11.36	25.03	38.99	52.97	66.95
6	2.38	14.36	29.77	45.33	60.89	76.45
7	3.00	16.97	33.78	50.68	67.59	84.49
8	3.62	19.25	37.26	55.32	73.38	91.45
9	4.22	21.28	40.33	59.42	78.50	97.58
10	4.82	23.10	43.08	63.08	83.07	103.08
20	9.60	35.12	61.14	87.16	113.18	139.20
50	17.14	51.03	85.01	118.99	152.97	186.95

*Accuracy ratio = 0.99 (1% accuracy)

Here, e_n = noise spectral density input in Vrms/$\sqrt{\text{Hz}}$.

If $e_1 = e_2 \ldots = e_k$, then Equation 3 simplifies to the root-sum-of-squares of G2 × e. This calculation is performed by the program. Generally, the first term is the dominant term and the remaining terms can be ignored.

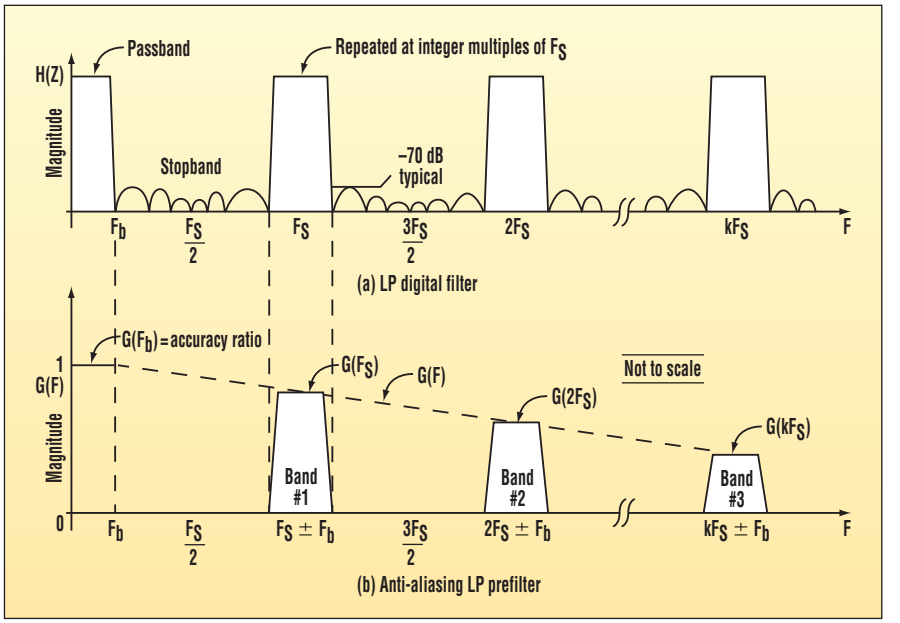
As an example, the maximum peak-to-peak noise of the ADC output, in terms of LSBs and N_B, can be calculated as follows:

$$N_B = 6 \times \frac{2^B}{V_{SPAN}} \times E_{TOT} \qquad (4)$$

where:

B = the word size of the ADC in bits

V_{SPAN} = the full-scale voltage span of the ADC



2. A low-pass digital filter (a) attenuates the spectra in the stopbands and passes the spectra in the passbands ($kF_S \pm F_b$) which are aliased to the band of interest ($0 - F_b$). Use of the prefilter (b) constrains the aliasing within the required limits.

E_{TOT} = the sum of the direct and aliased rms noise

Suppose a 12-bit ADC is used with a ±5-V, full-scale output, F_S = 5000 Hz, F_b = 500 Hz, along with a two-pole prefilter, and an input noise of 44.7 μV/$\sqrt{\text{Hz}}$. From the table, the filter gain $G(F_S)$ = −23.1 dB. The noise components can be calculated as:

direct noise = $\sqrt{500\ \text{Hz}} \times 44.7\ \mu\text{V}/\sqrt{\text{Hz}} = 0.001$ V

aliased noise = $\sqrt{1000\ \text{Hz}} \times 10^{-1.155} \times 44.7\ \mu\text{V}/\sqrt{\text{Hz}} = 0.0001$ V

then

$$E_{TOT} = \sqrt{(0.001)^2 + (0.0001)^2} \approx 0.001\ \text{V}$$

Substituting these values into Equation 4 yields:

$N_B = 6 \times 2^{12}/10 \times 0.001$
$= 2.46$ bits

Negative-Resistance Load Canceller Helps Drive Heavy Loads

Elliott Simons

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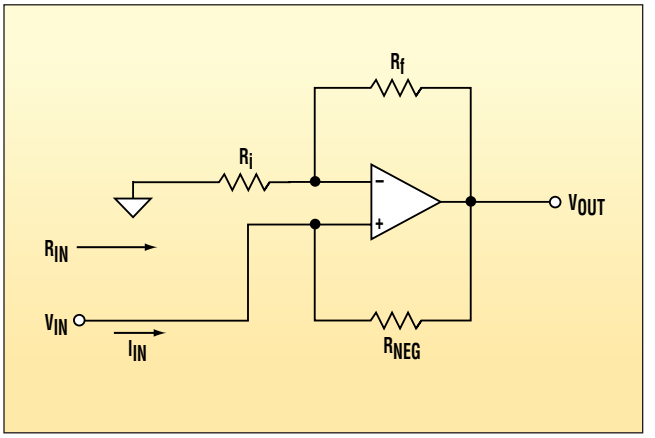
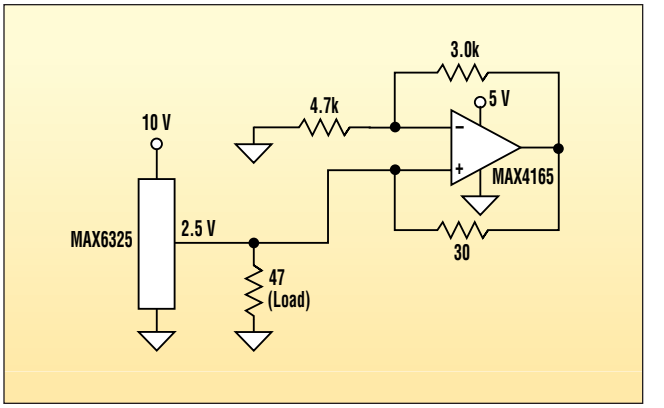


1. By matching this circuit's negative resistance (between the V_{IN} terminal and ground) with the load, the load will appear infinite.



2. Placing the circuit from Figure 1 in parallel with the load of a voltage reference (47 Ω in this case) cancels most of the reference's resistive load. Effectively, only the capacitive load will

Though not difficult, driving a load from a voltage reference IC requires some attention. After determining the supply voltage and output voltage, various other design parameters need to be considered. These include the output-voltage temperature coefficient, initial accuracy, drift, noise, line and load regulation, package size and type, power consumption, stability with various capacitive loads, and the required source and sink capabilities.

The need to source or sink more current than the voltage reference can provide is a common problem. A precision unity-gain buffer amplifier offers an adequate solution in applications that can tolerate its additional drift, noise, and gain inaccuracy. One serious drawback, however, is the buffer's potential instability when driving capacitive loads (such as the well-bypassed reference inputs of an analog-to-digital or digital-to-analog converter). Attempting to guarantee the buffer's stability by introducing an isolation resistor (between op-amp output and capacitive load) further degrades the reference circuit's accuracy.

Another alternative approach is to cancel the load, that is, to make it seem like a sizable resistance. If load resistance is made to appear large, the remaining load is then composed of any capacitance that may be in parallel with the load resistance. The load may be cancelled by placing a negative resistance in parallel with the load's positive resistance. If the magnitudes of these positive and negative resistances can be made equal, the effective load resistance becomes infinite. Unlike a buffer amplifier, this negative-resistance circuit adds negligible output error *(Fig. 1)*.

The input resistance from V_{IN} to ground is negative, and can be calculated as follows:

$$I_{IN} = \frac{V_{IN} - V_{OUT}}{R_{NEG}} = \frac{V_{IN} - V_{IN}\left(1 + \frac{R_f}{R_i}\right)}{R_{NEG}}$$

$$= \frac{-\frac{R_f}{R_i} V_{IN}}{R_{NEG}}$$

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = -R_{NEG}\frac{R_i}{R_f}$$

Adding this circuit to the output of an ultra-stable reference able to drive ±15 mA *(Fig. 2)* lets the reference drive ±50 mA or more. With perfectly matched components, the reference would source negligible dc current. When 1% resistors are used in the negative-resistance circuit, the required worst-case output current is ±2 mA. Load cancellation improves the output accuracy by lowering the error created by the reference output resistance. It also minimizes any drift due to self-heating, particularly when the output current is large and the difference between the output voltage and reference-supply voltage also is substantial. In addition, the circuit is unconditionally stable with any capacitive load.

Precision Thermostat Uses TBH And AC Feed-Forward Compensation

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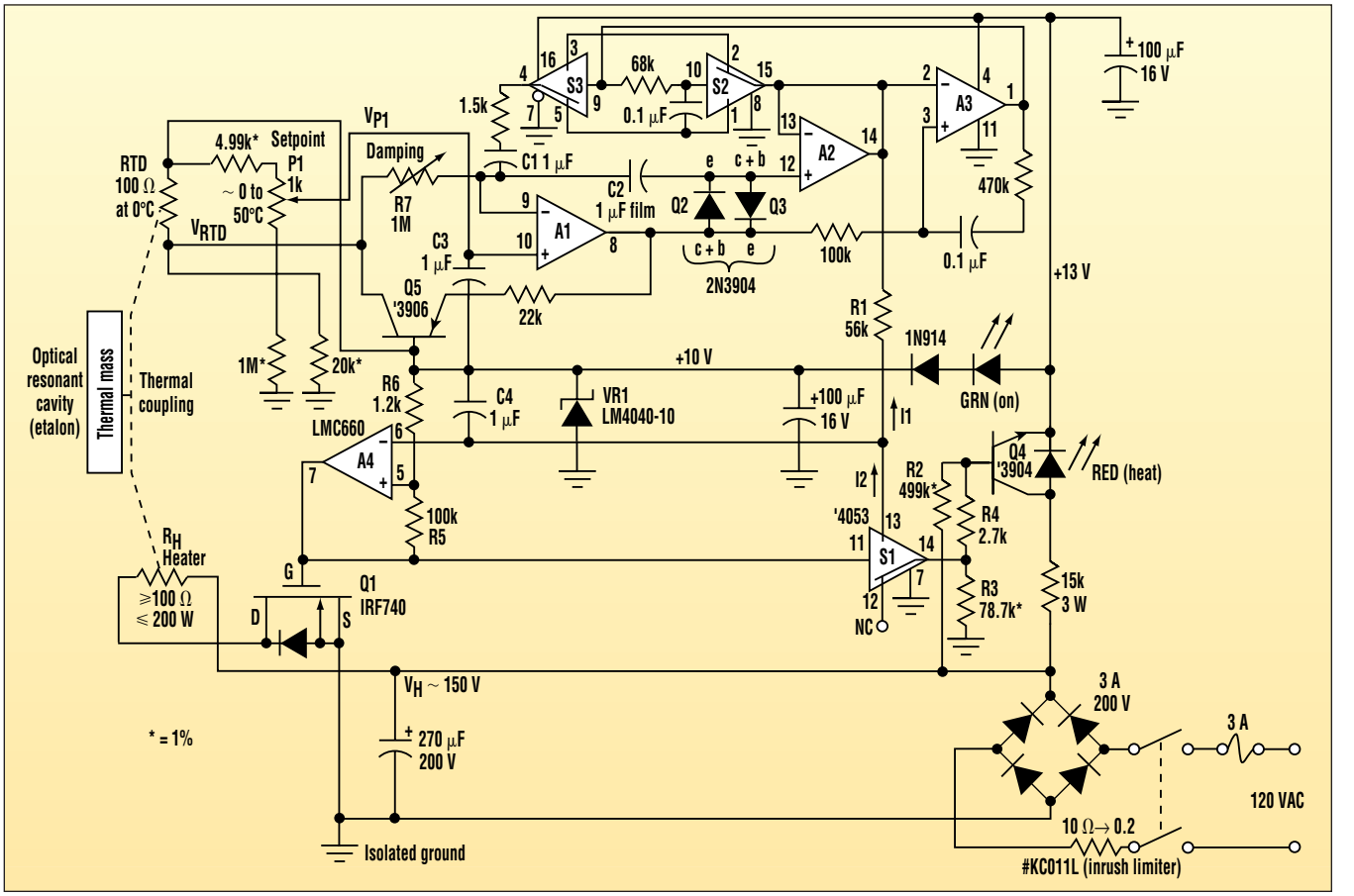
Precision temperature control with relatively high-power heaters driven directly from unregulated "120-V" ac lines is an efficient, inexpensive way to manage large thermal loads. A number of annoying complications can render this straightforward method problematic, however.

Among the worst of these troubles are the ubiquitous, random, and large variations in the ac mains. Variations in the RMS line voltage of ±5% (and worse) are ever present, which can make accurate temperature control very difficult. Every 1% twitch in RMS heater voltage will translate to a 2% lurch in square-law (V_H^2/R_H) heating. Temperature regulation may go entirely to pot before thermal excursions resulting from these random power changes can be caught and corrected by an unaided thermal control loop. Two possible solutions for this problem are pre-regulating the heater supply (expensive for big loads) and compensating for the variations.

This thermostat serves in a thermal control application that offers a perfect example of intolerance for temperature-variation, high-resolution, and optical resonant cavities (etalons) used in tunable-laser development *(see the figure)*. Etalons employ the principle of optical interference to precisely measure the wavelength of light in a laser beam. To do this accurately, the internal dimensions of the etalon must remain constant to within a tolerance of tens of nanometers. Despite the use of low thermal expansion materials in etalon fabrication, such extreme dimensional stability can only happen if the temperature of the etalon is rigidly controlled. For this reason, the design stability for this thermostat circuit is ±0.01 °C.

The principles underlying this circuit's thermal control loop are described in *"Take Back Half: A Novel Integrating Temperature-Control Algorithm,"* ELECTRONIC DESIGN, *Dec. 4, 2000, p. 132*. Here, a Kelvin-connected platinum resistance temperature detector (PRTD), operates in conjunction with the bridge network and voltage reference VR1. Together they produce a temperature-sensitive voltage, V_{RTD}, and a setpoint voltage, V_{P1}.



In addition to the "Take-Back-Half" control algorithm (TBH), this precision heating controller uses feed-forward compensation to virtually eliminate the effects of sudden ac-line variations. The sampling of the heater supply voltage (V_H) is performed by S1 and the R2/R4 network.

The temperature-setpoint error voltage ($V_{RTD} - V_{P1}$) is input to the TBH integrator A1. After this, the integrator output is scaled by the adjustable R7 × C1 time-constant, buffered by A2, and output as I1 to pulse-width-modulator A4. Therefore, if $V_{RTD} < V_{P1}$ (i.e., temperature > setpoint), V_{C2} will ramp up. This causes the heater duty factor (H_{PWM}) to ramp down and the heater, R_H, to cool off. If $V_{RTD} > V_{P1}$ (i.e., temperature < setpoint), H_{PWM} will ramp (and R_H will heat) up.

Meanwhile, crossed-diodes Q2/Q3 and comparator A3 track the sign of the $V_{P1} - V_{RTD}$ difference. A3's output goes high when $V_{P1} > V_{RTD}$ and low when $V_{P1} < V_{RTD}$. Temperature-setpoint crossings will cause the S2/S3 cross-connected CMOS switches to merge the charges on capacitors C2 and C1. This allows the TBH convergence-forcing bisection (described in the TBH article mentioned above) to go into effect.

Feed-forward compensation for potentially pesky 120-V variations occurs via sampling of the heater supply voltage (V_H) by S1 and the R2/R4 network. Compensation is achieved by the A4 PWM oscillator. It closes a feedback loop through S1, which strives to adjust H_{PWM} to maintain the charge balance on C4. For this to happen, I1, the heater power-control signal from the A1/A2 error-integrator, must be balanced by I2, the average current sourced to C4 by S1. Because $I2 = H_{PWM}(V_H - 75)/R2$, at balance $H_{PWM} = I1 \times R2/(V_H - 75)$. So for any given value of I1, H_{PWM} is inversely proportional to $(V_H - 75)$.

H_{PWM} then changes by –2% for each +1% deviation of V_H from its nominal value of 150 V. For example, let R_H = 100 Ω, V_H = 150 V, and H_{PWM} = 50%. Then $P_H = H_{PWM} \times V_H^2/R_H = 0.5 \times 150^2/100 = 112.5$ W. Now suppose V_H were to suddenly increase by 10 V (V_H = 160 V). Without the feed-forward compensation feature, P_H would jump by more than 15 W to $0.5 \times 160^2/100 = 128$ W. But instead, the feed-forward compensation kicks in to drop H_{PWM} to 44%, limiting P_H to $0.44 \times 160^2/100 = 112.6$ W. Consequently, the unwanted P_H excursion is reduced to an insignificant 0.1 W.

Flyback Power Supply Powers Subscriber Line Interface Circuit

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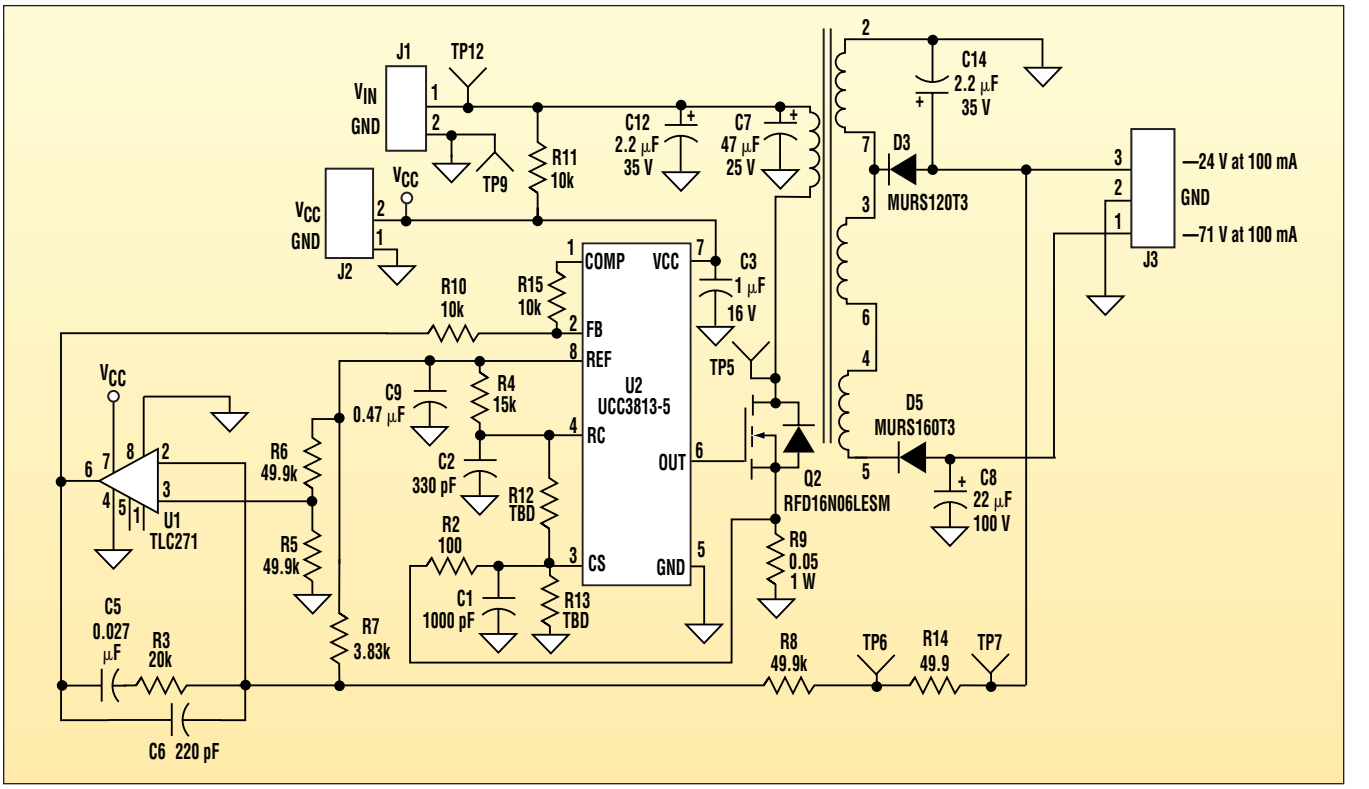
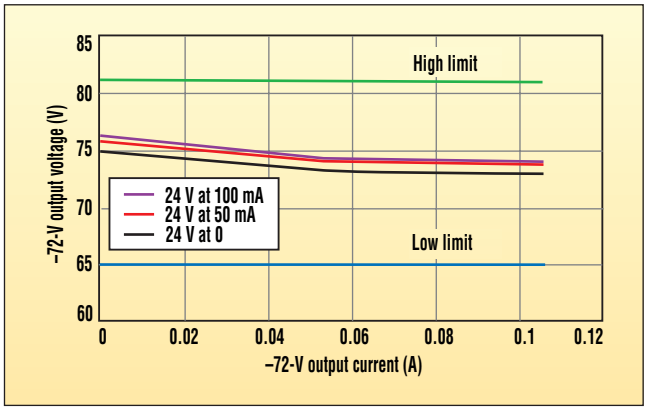
CIRCLE 522

Cable and xDSL modems are experiencing increasing popularity. For this reason, many designs are now required to interface with existing telephones at the subscriber's location. The subscriber line interface circuit (SLIC) within the modem has the additional burden of ringing the phone as well as providing loop current



1. This multi-winding flyback power supply allows a single control circuit to regulate both voltage outputs.

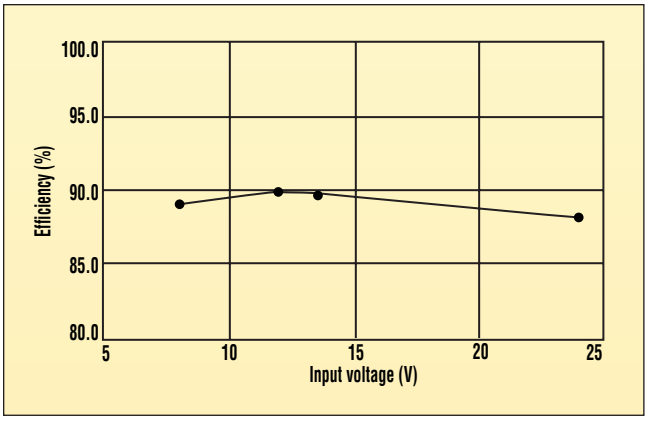


2. The load regulation of the –72-V output is well within the ±14-V telephony requirements. The worst-case variation is less than 4 V.

while a conversation is taking place.

While the phone is ringing and "on-hook," it appears as an 8k resistance in series with another 1k of capacitive reactance. Typically, the SLIC must be capable of driving this impedance with a 45-V_{RMS}, 20-Hz sinewave with a negative dc-offset in order to ring the phone. Therefore, a high voltage of between –50 and –105 V is usually mandated by the SLIC. Once the handset is lifted, the phone places a much lower impedance across the phone terminals, and the SLIC goes into a 20-mA constant-current mode. As a result, the SLIC only needs a power supply of –24 V.

Figure 1 shows the schematic of the power supply for the SLIC portion of the modem. This circuit provides multiple outputs from a single power switch and control IC. It also uses an efficient n-channel MOSFET with low voltage stress. A low input voltage powers a flyback topology. The input source could be either a widely differentiating (generally 2.5 to 1) output from an ac adapter, or a regulated supply used by some other portion of the system.



3. The low conduction and switching losses of the n-channel MOSFET help to provide excellent efficiency performance.

U2 is the brain of the power supply, as it modulates Q2's duty factor to control the output voltage. Also, it produces a reference voltage inverting amplifier U1 uses to generate an error signal. The control IC can perform either in current-mode or voltage-mode control.

A key advantage of the multi-winding approach is that a single control circuit and single MOSFET can supply two telephony voltages. Good cross-regulation can be achieved even though the SLIC places large current swings on both outputs *(Fig. 2)*. With the –24-V output, variations range from 3 mA of load current (when all phones are idle) to 80 to 100 mA of current (when all phones are off-hook). The –72-V output current can vary from 1 mA to a peak of 100 mA. Changes in the –24-V output voltage occur due to the operational amplifier's offset voltages, which are typically 3%, as well as divider and reference tolerances. Capable of such tolerances, the –72-V output also offers cross regulation of the transformer and the fluctuating diode voltage drops. Even with all of these variables, however, the –72-V output's worst-case variation is less than 4 V, way below the 14-V requirement.

Because of its low conduction and switching losses, the n-MOSFET, multi-output flyback configuration provides excellent efficiency. The efficiency measurements with the –72-V output loaded to full current are given over a wide input voltage range *(Fig. 3)*. This design has been optimized with approximately 90% efficiency for a 12-V input. For the low input voltages, the efficiency is somewhat lower due to the increased conduction losses in the MOSFET. But at high voltages, the higher switching losses cause the lower efficiency.

Manually Operated Digital Pot Doesn't Need A Microprocessor

Ken Yang

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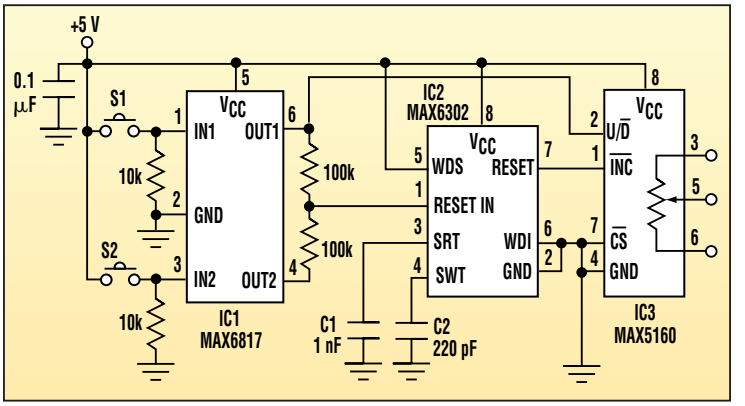
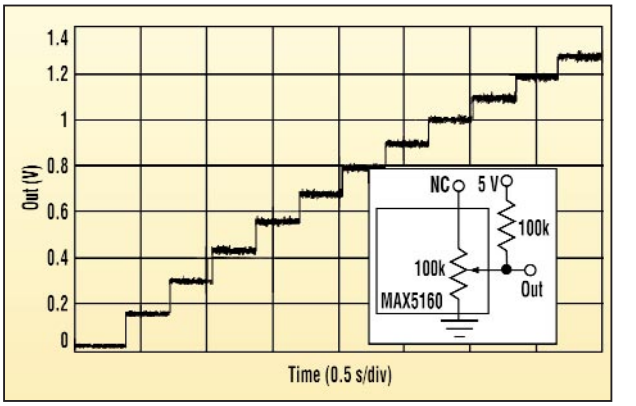


1. This circuit provides manual up/down control of a digital potentiometer using two pushbutton switches without using a microcontroller.



2. The resistance-ramp operation is observed by adding an external resistor to the wiper to form a voltage divider.

Digital potentiometer ICs such as the MAX5160 and MAX5161 are good replacements for mechanical types. But these ICs are designed to work with microcontrollers. In this manually operated digital potentiometer, two pushbuttons control the wiper resistance without a microcontroller *(Fig. 1)*.

To mask the effect of contact bounce in mechanical switches S1 and S2, a dual switch-debouncer (IC1) is used. A microprocessor-supervisor device configured as an oscillator (IC2) provides a clock signal to the digital potentiometer. Initially, OUT1, OUT2, and RESET are high. If S2 is momentarily depressed and released, OUT2 causes the RESET input of IC2 to go low. When S2 is released, OUT2 and RESET return high. The wiper position is controlled by a 5-bit resistive ladder internal to IC3 (similar to that of a 5-bit digital-to-analog converter). Therefore, this single cycle of oscillation lowers the wiper resistance by 1/32 of the total resistance range of the potentiometer.

IC2 continues to oscillate if S2 is depressed and held. As a result, the resistance is lowered in a series of steps *(Fig. 2)*. Similarly, depressing S1 increases the potentiometer's resistance. Capacitors C1 and C2 set the frequency of oscillation at approximately 3 Hz.

The "Starved-Circuit" Amplifier Is Revived In A Transistor Version

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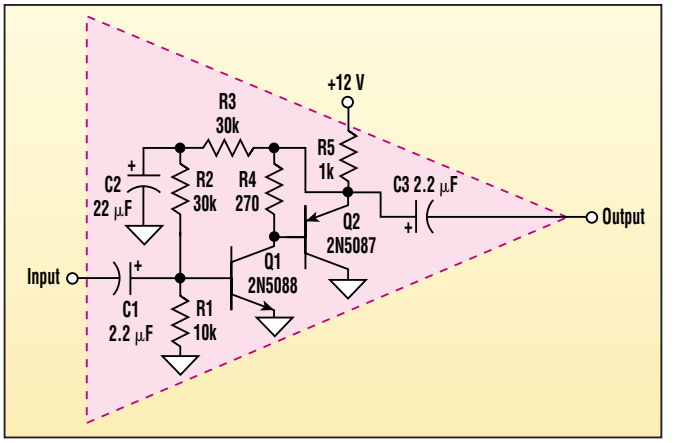
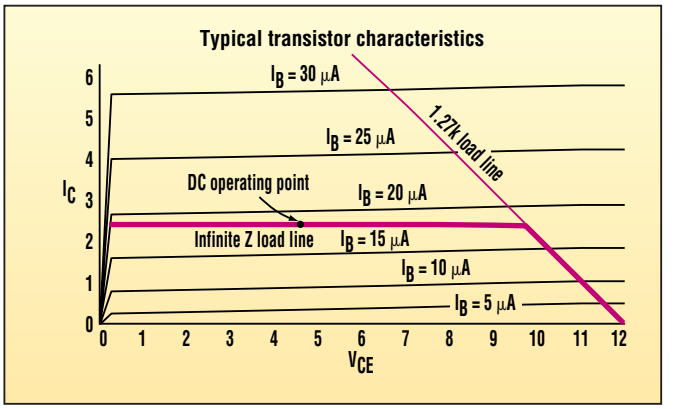
Back in the '60s, there was an intriguing circuit article titled "Starved-Circuit Amplifier" published in *Popular Electronics* magazine. It used a sharp cut-off pentode with a 3-MΩ load resistor and had a voltage gain of over 1000. Of course, it had little application since any load added to the output tended to reduce the load resistance and the gain.

Like tube-type amplifiers, transistor amplifiers have a maximum voltage gain of about 100 (40 dB). Additional stages are required to increase the voltage gain. A cursory examination of this circuit might indicate that this amplifier uses a conventional composite npn-pnp transistor arrangement, which is nothing new *(Fig. 1)*. What is new is the value of R4. In the typical composite connection, R4 is 50k, which is sufficient to drain off leakage to increase the dc stability. In this case, however, R4 = 270 (more than two orders of magnitude lower).



1. An updated version of the "starved-circuit" amplifier.

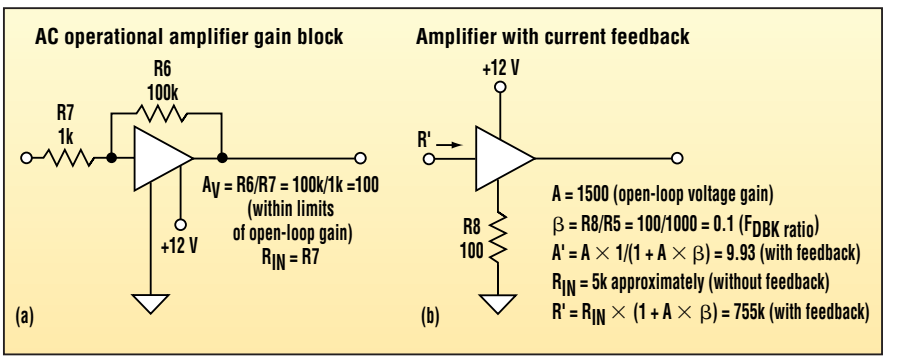


3. Use of current feedback via an external resistor reduces gain, noise, and distortion while increasing input resistance.

Q2's V_{BE} regulates the current through R4. This current source is Q1's collector current. A good current source has the property of an infinite ac resistance, which increases the voltage gain of Q1 by a factor of 10. The typical voltage gain is about 1500 (63 dB).

Q2, operating as an emitter-follower, has a unity voltage gain. To prevent the dc bias circuit from providing ac feedback, C2 bypasses the ac to common. For best results, Q1 should have a beta that exceeds 250. Q2 should have a relatively high beta as well.

High voltage gain is just one of the beneficial properties. Low distortion is another. Since the ac load line is horizontal, I_C doesn't vary over the large-signal voltage range. As a result, large-signal distortion is low even without feedback. Noise performance is good because Q1 runs at about 2.5 mA, which is close to the minima of the noise curve. The equivalent noise input voltage runs below 1 μV. Another feature of this circuit is that the frequency response of its amplifier is suitable for audio applications. The input resistance runs at about 5k, while the output resistance, driven by an emitter-follower, is low.



2. The circuit may be redrawn as an op-amp gain block with external components controlling the gain (a). An alternative hookup uses a resistor in the ground-return circuit (b).

This circuit may be redrawn as an operational-amplifier gain block with external components controlling the gain. An alternative hookup uses a resistor in the ground-return circuit. In this "current feedback" version, the voltage developed across R8 is a voltage feedback signal *(Fig. 2)*. It has the advantage of reducing gain, noise, and distortion while increasing input resistance *(Fig. 3)*.

Digital-To-Analog-Resistance Converter Is Optically Isolated

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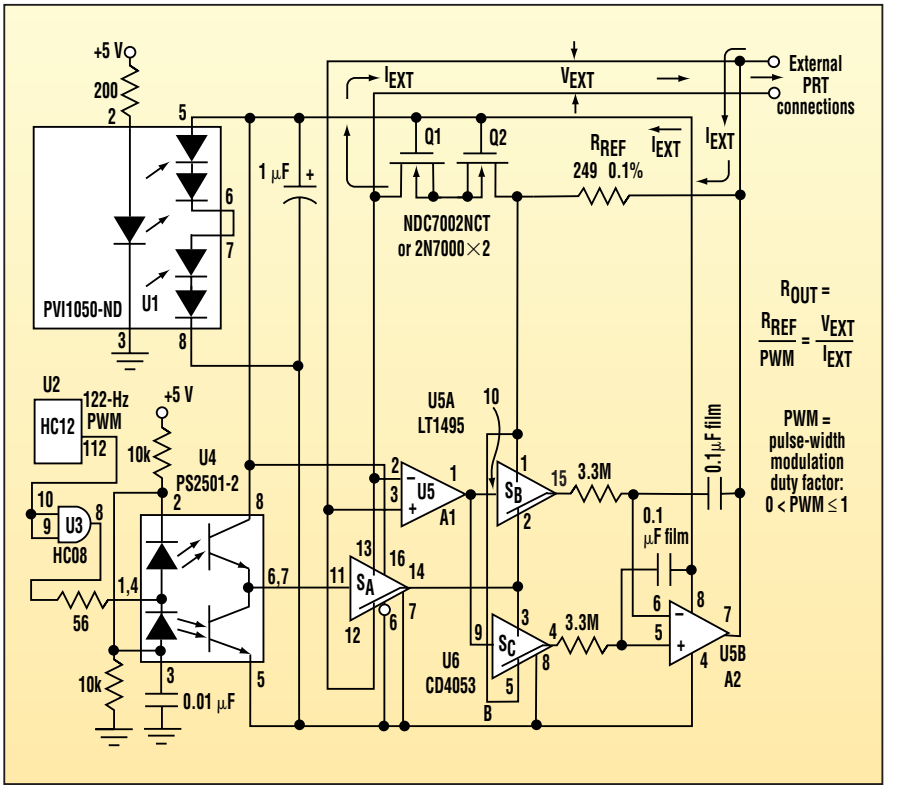
CIRCLE 522

The subject of digital-to-analog converter (DAC) applications is generally rather tame. It's usually confined to a boring discussion of settling time, the number of bits of resolution needed, the virtues of serial or parallel interfaces, and whether current or voltage output is best. Occasionally the conversation may become slightly enlivened by a requirement for such nonstandard features as optical isolation or a pulse-width-modulated (PWM) digital input. But mostly that's about as exciting as the topic ever gets.

Sometimes, however, an application comes along with a satisfyingly weird wrinkle. This DAC circuit affords a fine example because it produces neither an analog voltage nor an analog current output *(see the figure)*. Instead, it outputs an optically isolated pure ohmic resistance in response to a PWM control input with 16-bit resolution ($R_O = R_{REF}/PWM$). Here, PWM is the 0 to 1.0 duty cycle of the control signal produced by the HC12 microcontroller. It can be used to digitally simulate a 1000-Ω (at 0°C) platinum-resistance temperature detector (PRTD).



This DAC circuit simulates a 1000-Ω PRTD by outputting an optically isolated pure ohmic resistance in response to a PWM control input ($R_O = R_{REF}/PWM$).

The circuit can therefore be used in automated digital calibration of precision PRTD signal conditioning. This feature makes it possible to thoroughly optimize PRTD linearization *(see "Precision Thermometer Linearizes, Digitally Calibrates Platinum RTDs," ELECTRONIC DESIGN, May 29, 2000, p. 112)* and algorithms *(see "Efficient Algorithms Improve The Linearization Of Platinum RTDs," ELECTRONIC DESIGN, Oct. 2, 2000, p. 138)* over the full range of the DIN 43 760 standard of −200°C to 850°C. Either polarity of dc excitation is accommodated, and all necessary operating power (less than 10 µA at 10 V) for the isolated part of the DAC circuitry is derived from photovoltaic optoisolator U1. Optical isolation of the PWM signal is performed by the dual-channel optoisolator U4.

In operation, comparator A1 controls the state of switches S_B and S_C, causing the polarity of A2's feedback loop to match the polarity of the external "PRTD" excitation. This action correctly arranges A2's input configuration. This assures that the feedback from A2 to the gate bias of FETs Q1 and Q2 forces the voltage across $R_{REF} = V_{REF} = I_{EXT} \times R_{REF}$ to equal V1 (the average voltage output by S_A). Since V1 = PWM × V_{EXT}, A2's feedback loop forces $I_{EXT} \times R_{REF}$ = PWM × V_{EXT}. So $V_{EXT}/I_{EXT} = R_{REF}/PWM$. Yet by definition, V_{EXT}/I_{EXT} = the DAC output resistance (R_O). Consequently, $R_O = R_{REF}/PWM$.

The A2 low-pass RC time constants as shown (3.3 MΩ and 0.1 µF = 0.33 sec = 0.5 Hz) produce an acceptable ripple level with a 122-Hz PWM signal. This signal is generated by an on-chip counter/timer of a 16-MHz HC12 microcontroller (U2). Varying PWM source frequencies or ripple attenuation requirements may dictate different RC values. Likewise, simulation of diverse PRT nominal resistances (e.g., 100 Ω at 0°C) may require a different R_{REF}.

Subject to these provisos, this isolated PRT DAC circuit is quite versatile. Both excitation currents of up to 10 mA and excitation voltages of several volts can be accommodated. Accuracy and resolution are limited almost entirely by R_{REF}'s tolerance. Therefore, they can be made to rival those of even the best "real" PRTDs.

Active Feedback Amplifier Enables High-Performance A-To-D Conversion

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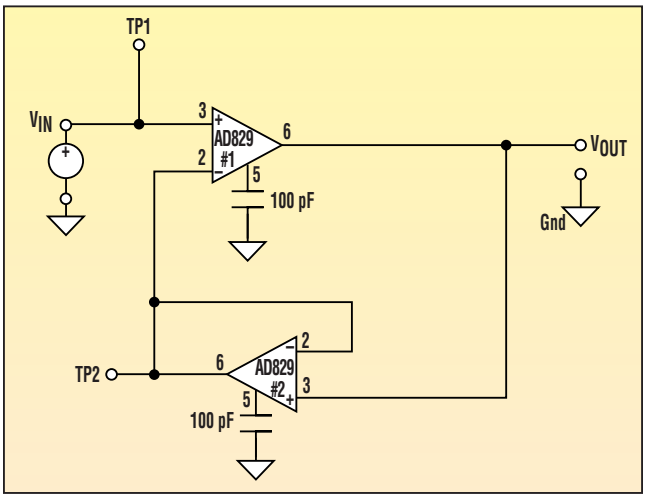
CIRCLE 523

Designers employing high-performance analog-to-digital converters (ADCs) have a common problem: there are few, if any, amplifiers on the market that can provide the accuracy needed to buffer an input signal and drive a 16-bit ADC without a loss of performance. A 10-V full-scale ADC must be able to resolve 150 µV. This is a tall order, even when the input frequencies are as low as 100 kHz.

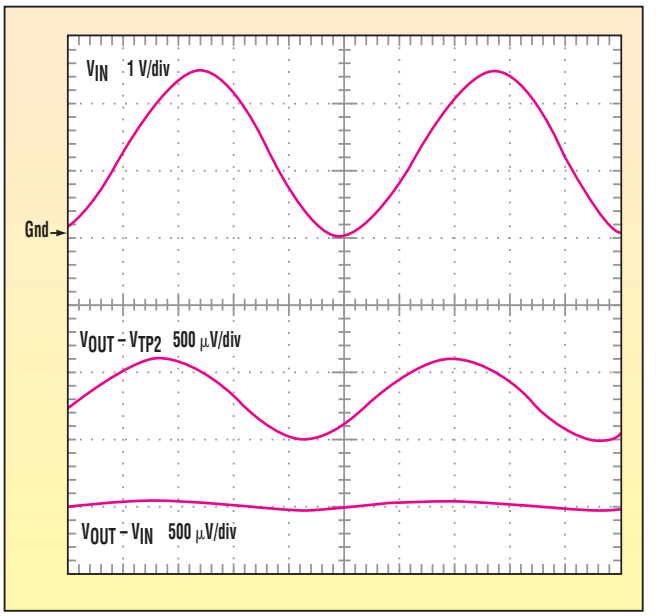
To compound the matter, many of today's ADCs have a full-scale range of 5 V. Any buffer used to drive such a device must contribute no more than 75 µV of error or the system performance will be compromised. This low-noise and low-distortion requirement ensures that a finite-bandwidth amplifier (e.g., f_T = 30 MHz) is simply incapable of such performance.

Total error = root-sum-squared (noise, distortion, CMRR, gain error) < 75 µV

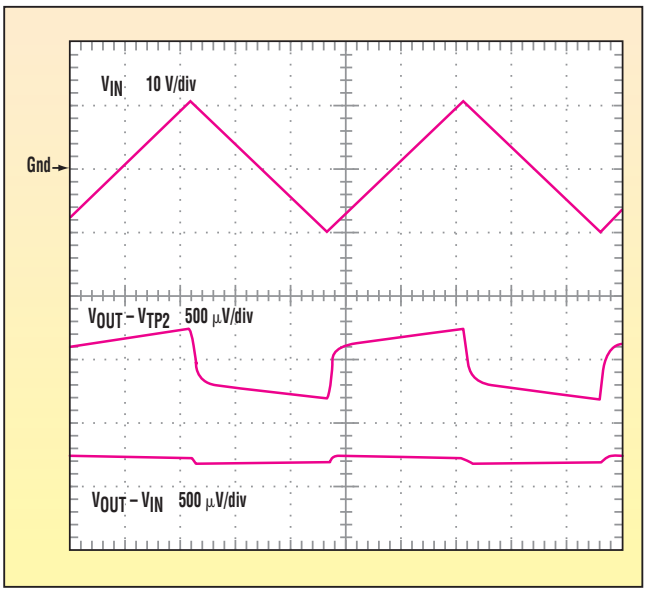
This device improves state-of-the-art circuitry by about 20 dB over currently available buffers *(Fig. 1)*. Two ampli-



1. Adding an active feedback amplifier provides error cancellation, improving system error performance by as much as 20 dB.



2. With this amplifier, using a 0- to 2.5-V 10-kHz sinewave input, a significant error reduction is seen when the buffer amp error (middle trace) is compared with the output error (bottom trace).



3. The performance of this circuit using a ±10-V triangle waveform input at 1 kHz indicates error reductions similar to those in Fig. 2.

fiers make up the system. The second amplifier is contained in the feedback loop of the first amplifier and configured for a gain of one.

Note that V_{OUT} is approximately equal to V_{IN}. The voltage at TP2 is similar to V_{IN} as well. Consequently, the error between the noninverting terminals and inverting terminals of the first amplifier is the same as the error between the noninverting and the inverting terminals of the second amplifier. Therefore:

$$V_{OUT} = V_{IN} + V_{ERROR1} - V_{ERROR2}$$

or

$$V_{OUT} = V_{IN}$$

Figure 2 shows the performance of this circuit for a 0- to 2.5-V sinewave input at 10 kHz. When comparing the error ($V_{OUT} - V_{IN}$) in the bottom trace to that of the buffer alone ($V_{OUT} - V_{TP2}$) in the middle trace, a significant error reduction can be observed. Figure 3 shows a similar improvement for a ±10-V triangle waveform input at 1 kHz. The amplifier bandwidth was programmed to be 30 MHz.

Programmable-Gain Amp Uses Arbitrary-Attenuation Step Ladder

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The R-2R ladder, a well known resistor topology, is often used to implement a current or voltage 6-dB step attenuator. By appropriately scaling the resistor values, this network also can be modified to provide any desired attenuation.

The modified resistor ladder uses three different resistor values *(see the figure)*. A short algebraic manipulation can show that:

Step attenuation (dB) = 20 log [R3/(R1 + R3)]

$R_{IN} = R1 + R3$

$R2 = R3\ (1 + R3/R1)$

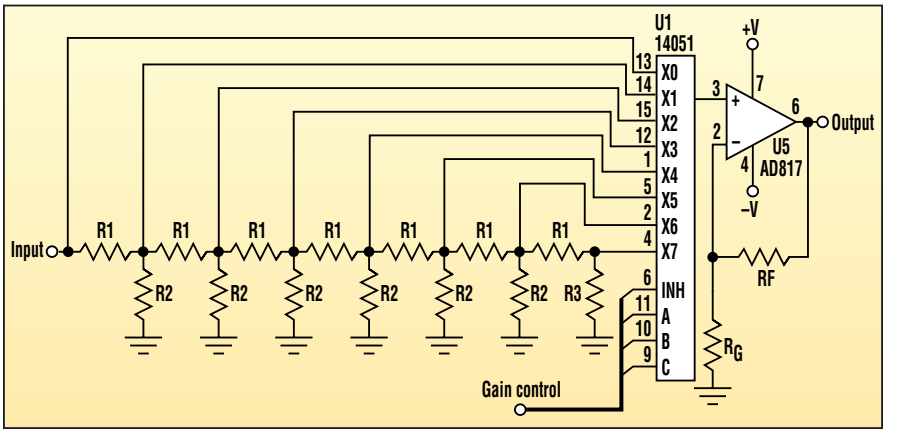
If R1 = R3, then R2 = 2 × R1. In this case, the R-2R network provides a 6-dB step attenuation.

To determine the resistor values for a specific step attenuation and input resistance, use the formulas:

$K = 10^{[\text{step attenuation (dB)}/20]}$

(Note that the step attenuation (dB) value should be negative!)

$R1 = R_{IN}\ (1 - K)$



This wide-bandwidth, low-distortion programmable gain amplifier (PGA) is built using low-cost standard devices, eliminating the need for an expensive programmable-gain amp IC.

$R2 = R_{IN} \times K/(1 - K)$

$R3 = K \times R_{IN}$

For example, to implement a resistor ladder with a −1.5-dB step attenuation and 500-Ω input impedance:

K = 0.8414

R1 = 500 (1 − 0.8414) = 79.3 Ω

R2 = 500 × 0.8414/(1 − 0.8414) = 2653 Ω

R3 = 0.8414 × 500 = 420.7 Ω

There are a couple of interesting points to observe about the PGA circuit. A standard CMOS analog switch is used to connect the attenuated signal to the noninverting input of the op amp, which has a high input impedance. Since the current through the switch is negligible, low attenuation and distortion is achieved. A wide-bandwidth (video-bandwidth), low-distortion PGA is created through the use of very low-cost standard devices.

Resistive Dummy Load Draws Constant Current From 1.2 To 50 V

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This dummy-load circuit has been in use at Maxim for more than 10 years *(see the figure)*. It's useful for testing power supplies and power amplifiers as well as drivers for LEDs, relays, and solenoids. Plus, it overcomes the limitations of power rheostats, which are bulky and have coarse setting accuracy. The device also has an advantage over large, expensive power decade boxes, which provide limited resolution.

Unlike conventional resistive loads, the "dummy load" maintains a constant but adjustable load current for voltages in the range of 1.2 to 50 V. Both the power MOSFET and the sense resistor are used to dissipate the load power. Battery operation provides isolation while eliminating grounding problems.

The 10-turn potentiometer R6 affects accuracy and resolution. Consequently, it should be rated for at least 3% absolute accuracy and 0.2% or better linearity. (If desired, R6 can be replaced with a three-digit pushbutton potentiometer such as Bourns model 3680.) R6's wiper provides a reference to the op amp, whose input common-mode range includes ground. Feedback ensures that the wiper voltage appears across the sense resistor (R9), thereby forcing a desired load current through the MOSFET.

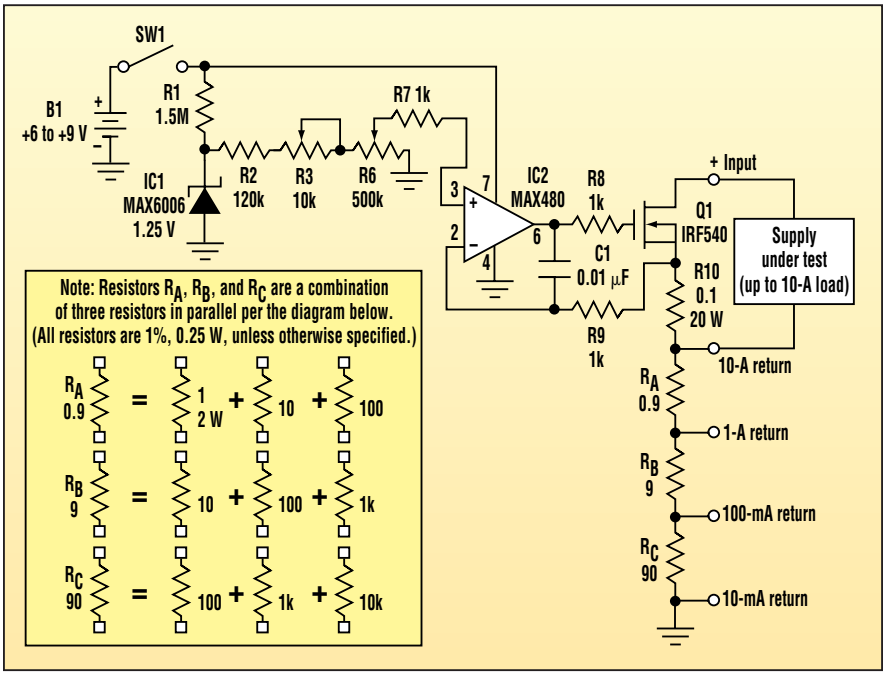
Bias current for the op amp (3 nA maximum) flows through the series combination of R_A, R_B, R_C, and R10. Multiplying this current by the sum of the four series resistors (100 Ω) yields a 300-nV error. This error voltage is small compared to the voltage presented by R6 at the op amp's noninverting terminal. Therefore, the resulting output-current error is insignificant. Capacitor C1 enhances stability by reducing bandwidth (already low by this point).

The series-connected, decade-weighted load resistors R_A, R_B, and R_C yield four ranges of output-current capability. To set the range for a power-supply load, connect the positive lead of the supply to the "+" input of the load circuit and the negative load to one of the four return terminals.

For calibration, insert a battery and turn on the circuit. Then, connect the positive terminal of a 5-V/10-A power supply (in series with an ammeter that has a 4.5-digit display or better) to the "+" input of the dummy load. Next, connect the ground terminal of the power supply to the 10-A return of the load box. With R6 at full scale, adjust R3 so the ammeter reads precisely 10.00 A. To check the circuit's linearity, set R6 to exactly five turns and verify that the ammeter reads 5.00 A.

Calibrate the remaining ranges by regulating the values of R_A, R_B, and R_C. Since each of these consists of three resistors in parallel, the value is best adjusted by changing the largest of the three parallel-connected resistors. For example, to regulate R_A, set R6 at full scale and adjust the largest of the three resistors in R6 (100 Ω) until the ammeter reads 1.00 A. Then adjust the largest of the R_B resistors for a 100-mA reading, and the largest of the R_C resistors for a 10-mA reading.

The minimum operating current for the MAX6006 reference is 1 µA, yielding an overall supply current of only 18 µA. Given the 580-mA-hr rating of a 9-V battery, this circuit can operate continuously for several years. With its 15-µA maximum supply current and 25-µV typical offset voltage, the MAX480 is an excellent choice for this application.



A low-power control circuit in this adjustable dummy load enables the high-resolution potentiometer R6 to precisely control load currents as large as 10 A.

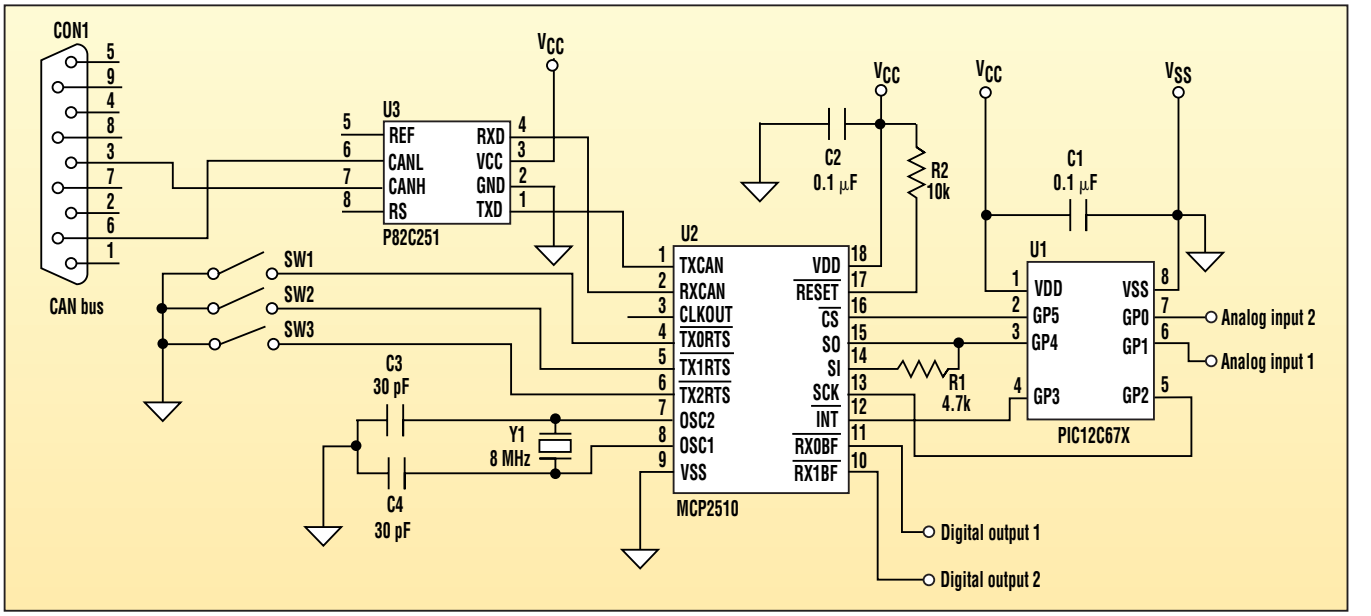
Build A Simple And Inexpensive Controller Area Network Node

Pat Richards and *Rick Stoneking*

Microchip Technology Inc. ***Anadigics Inc.***

Shown here is the schematic for a simple, inexpensive controller area network (CAN) node *(Fig. 1)*. The PIC12C672 was chosen because of its low pin count (8 pins) and powerful feature set. This set includes an internal oscillator, on-board multichannel 8-bit analog-to-digital converter (ADC), multiple interrupt sources, and a low-power sleep mode.

A full CAN 2.0 implementation with message filtering is supplied by the MCP2510 14-pin standalone CAN controller. Therefore, the host microcontroller is relieved from performing any CAN-bus-related overhead. This is a key feature given the limited available code space of the PIC12C672. The PCA-82C251 transceiver was selected arbitrarily because this article focuses on implementing the CAN



1. Using a diminutive 8-pin microcontroller, this CAN node provides two analog input channels and six digital I/O channels.

protocol, and the physical layer is undefined by CAN.

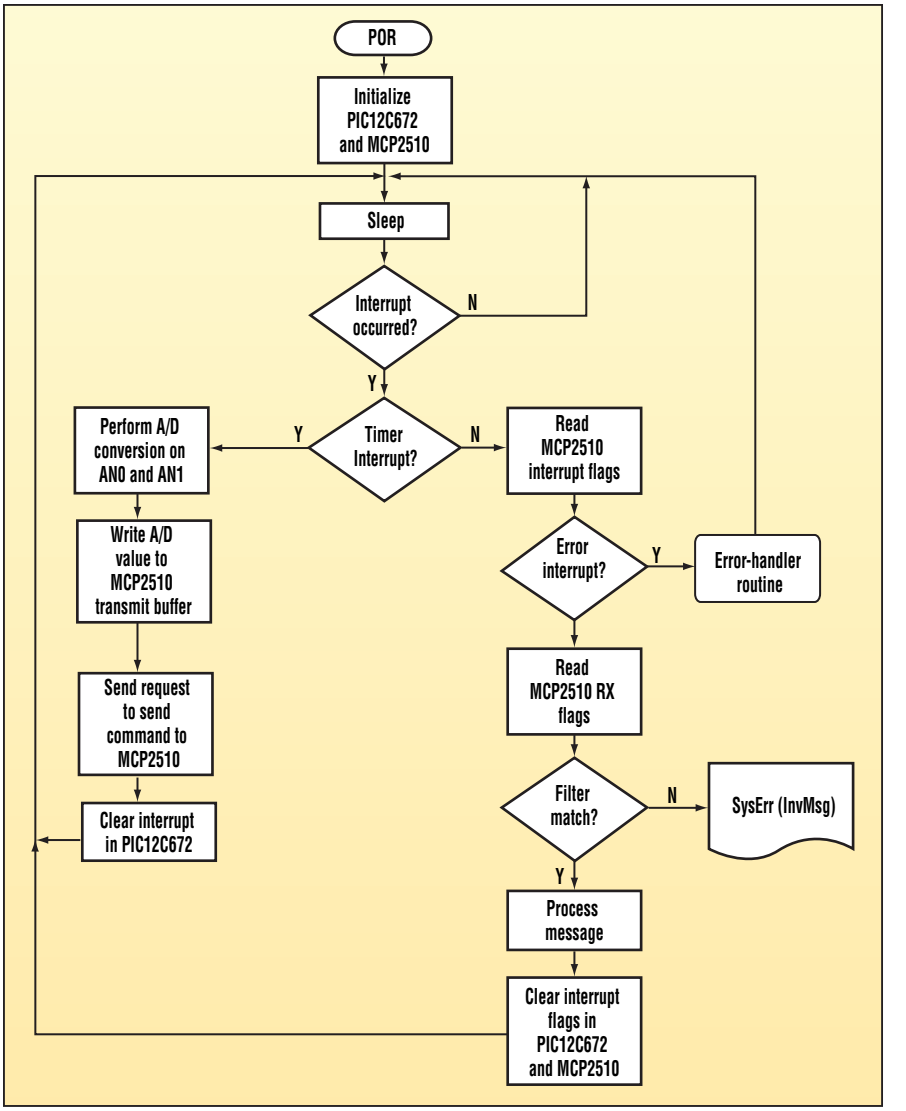
The PIC12C672 uses all six available I/O pins. It also takes advantage of the internal RC oscillator, which provides a 4-MHz system clock that translates into a 1-µs instruction cycle. Two I/O ports are used for analog input, while four I/Os are used to interface to the MCP2510 (three SPI and one interrupt).

An 8-MHz crystal is used to operate the MCP2510. While the three TXnRTS pins are configured as general-purpose inputs, the RXnBF pins are configured as general-purpose outputs. As a result, all of the pins the MCU lost for the SPI interface are regained. The TXnRTS inputs are connected to switches. These pins have internal pull-up resistors that cause the input to read as a logic "1" when the switch is open. The RXnBF outputs are connected to LEDs.

(To view the firmware, written in assembly, visit *www.PlanetEE.com* and click on the "Ideas for Design" icon).

Figure 2 shows the top-level flowchart for the overall system operation. After going through self-initialization and initializing the MCP2510, the microcontroller simply goes to sleep and waits for an interrupt to take place (timer 0 or $\overline{\text{INT}}$ pin).

Communication between the PIC12C672 and the MCP2510 is accomplished via the MCP2510's built-in SPI interface. Since the PIC12C672 doesn't have a hardware SPI interface, the necessary functions are implemented in firmware. The system achieves a total



2. This CAN bus node provides both CAN-initiated and self-timed analog-to-digital conversions.

IDENTIFIER DESCRIPTION		
ID (HEX)	**TX/RX**	**Command**
3F0	RX	Read analog channel 1; transmit result (ID = 3f8)
3F1	RX	Read digital inputs; transmit result (ID = 3f9)
3F2	RX	Change digital output 1
3F3	RX	Change digital output 2
3F8	TX	Analog channel 1 value
3F9	TX	Current values of digital inputs
3FA	TX	Command acknowledgement (for 3F2)
3FB	TX	Command acknowledgement (for 3F3)
3FE	TX	Analog channel 0 value (timed)
3FF	TX	System error

SPI bus rate of slightly more than 80 kbits/s. Its raw SPI clock rate averages 95 kbits/s. The clock's low time is a fixed 5 µs, while its high time is either 5 µs or 6 µs depending upon whether a "0" or a "1" is being sent/received. These timing values yield a worst case raw clock rate (i.e., sending the value 0xff) of 90.9-kbit/s . The overall effective speed realized includes the additional software overhead of "bit-banging" the SPI protocol.

Note that the SPI rate is slow enough that, in some scenarios, message overruns may result. These are caused by multiple back-to-back messages arriving at the MCP2510 before previous messages can be serviced. As a safeguard to ensure message delivery, each received message is acknowledged with a return message (either with the requested data or with a command-acknowledge-type message). If a predetermined timeout expires without a response from the node, the node requesting the information or change in outputs can assume the message wasn't received.

In this example, the MCP2510 is configured to operate on the CAN bus at 125 kbits/s. This is done by setting the bit time at 8TQ and the baud-rate prescaler equivalent to divide by four.

There are two interrupt sources in the system. One is the PIC12C672's timer0 interrupt. Occurring every 10.16 ms, this interrupt is used as a trigger to transmit the results from analog channel 0. The other interrupt source is the $\overline{\text{INT}}$ pin of the PIC-12C672, which is connected to the $\overline{\text{INT}}$ output of the MCP2510. This interrupt happens any time a valid message is received, or if the MCP2510 detects a CAN-bus-related error.

To respond to the four defined receive identifiers, the node uses the MCP2510's multiple filters *(see the table)*. The masks and filters are set to accept messages into receive buffer 1 (RX1) only. Each received message matches only one filter. This simplifies the interrogation required by the MCU as the FILHIT bits in RXB0CTRL are used to determine the message type instead of reading the 11-bit identifier.

Since only receive buffer 1 is used, the masks and filters for receive buffer 0 are set to reject all messages. This is achieved by setting the mask and filters associated with buffer 0 to all ones.

In addition to the four receive messages, there are six transmit message IDs. Four of the transmit messages are in response to the four received messages. The other two transmit messages are for sending the timed AN0 results and for system errors.

All transmitted messages use data byte 1 of the CAN message to hold the data to be sent. Messages intended for the node require a standard identifier that has a value of 0x3f0 to 0x3f3, with each of the four filters configured to accept one of these messages. For the messages transmitted back, the node uses the same identifier as the received message, except the ID3 bit is set to "1." So for instance, when the "read analog channel 1" message is received (ID = 0x3f0), the node transmits the data back using a message ID of 0x3f8 (ID bit three = 1).

As the proliferation of CAN continues, the need for simple, low-cost CAN nodes will increase. The PIC12C672 combined with the MCP2510 CAN controller demonstrates an inexpensive yet versatile CAN node.

Second-Order Audio Filter Performs Multiple Functions

Ilkka Marttila

CIRCLE 520

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The second-order multipurpose filter described here can perform as a low-pass, bandpass, high-pass, or notch filter at audio frequencies. What makes this filter unique is that all of its characteristics can be varied independently with potentiometers.

To calculate the transfer function of the second-order filter, the following equation is used:

$$H(s) = \frac{k_{HP}s^2 + k_{BP}\frac{\omega_o}{Q}s + k_{LP}{\omega_o}^2}{s^2 + \frac{\omega_o}{Q}s + {\omega_o}^2}$$

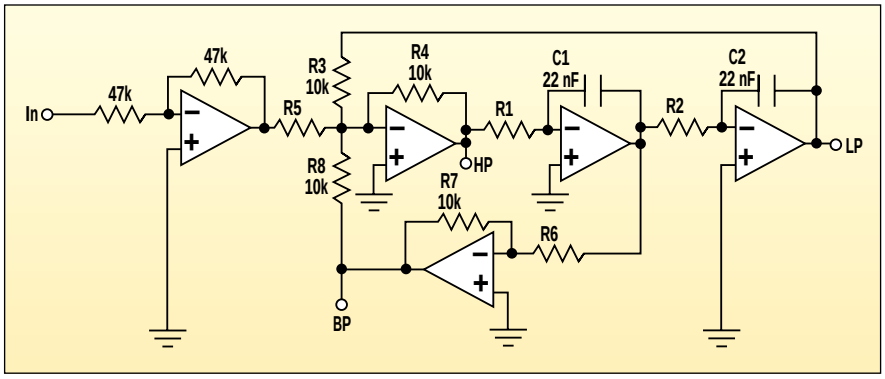
where s = jω

In basic filters, only one k value is non-zero. Figure 1's circuit includes the three basic types of filters. The characteristic frequency, Q value, and transfer gains are:

$$\omega_o = \sqrt{\frac{R_4}{R_3}\frac{1}{R_1C_1R_2C_2}} = \sqrt{\frac{1}{R_1C_1R_2C_2}}$$

$$Q = \frac{R_6}{R_7}\frac{R_8}{R_4}\sqrt{\frac{R_4}{R_3}\frac{R_1C_1}{R_2C_2}} = \frac{R_6}{R_7}\sqrt{\frac{R_1C_1}{R_2C_2}}$$

$$k_{HP} = \frac{R_4}{R_5} \qquad k_{BP} = \frac{R_8}{R_5} \qquad k_{LP} = \frac{R_3}{R_5}$$



1. The building block of the basic filter provides low-pass, bandpass, and high-pass outputs.

When resistors R3, R4, and R8 have the same value, the parenthetical expressions are valid. R1 and R2 cause the characteristic frequency to change independently. To independently vary the Q value, R6 is adjusted. All of the gains change when R5 is modified.

There are three useful outputs in the circuits. They are low-pass, high-pass, and bandpass outputs. In the circuit

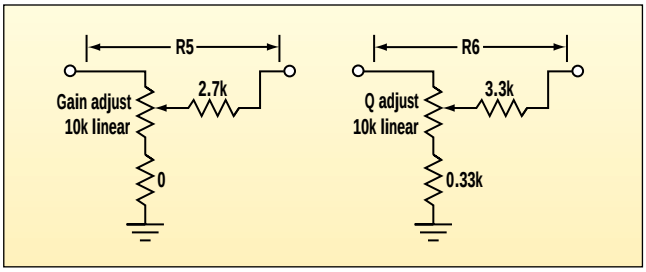
TABLE 1: FILTER CHARACTERISTICS

	Unit	Min.	Mid.	Max.
F0	kHz	0.2	1	5
Q		0.3	1	11
Gain	V/V	0	1	4

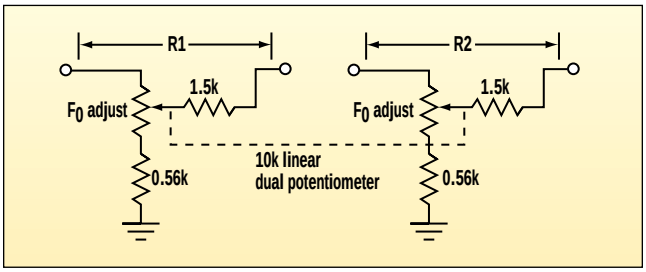
TABLE 2: FILTER SUMMARY

Filter Type	k_{LP}	k_{BP}	k_{HP}
Low-pass	1	0	0
Bandpass	0	1	0
High-pass	0	0	1
Notch	1	0	1
Low-pass*	1	0	<1
High-pass*	<1	0	1
All-pass	1	–1	1
Pass-through	1	1	1

* = with a notch in the stop-band



2. These networks can be substituted for R5 and R6 to provide variable gain and an adjustable Q value.

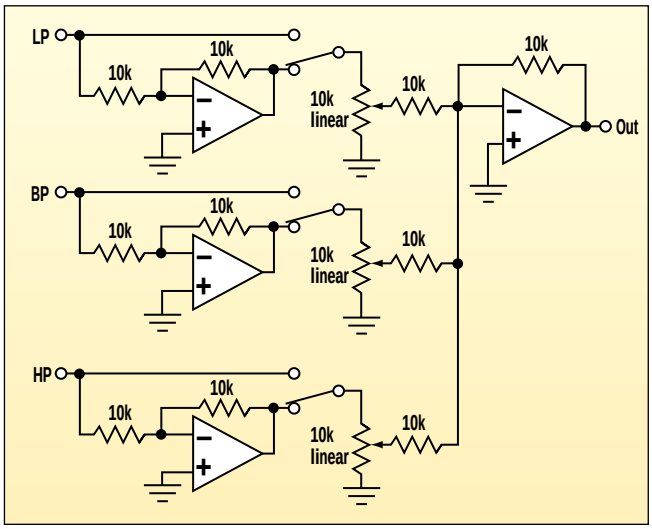


3. If variable adjustment of characteristic frequency, f_0, is required, these networks can be substituted for R1 and R2.

diagram, these are marked with abbreviations LP, HP, and BP. Replacing resistor R5 with the circuit in Figure 2 makes the gain adjustable. This method can also be used with the Q value. It's possible to achieve adjustability by replacing resistor R6 with Figure 2's circuit.

The characteristic frequency adjustment is more complicated. To keep the adjustments independent, resistors R1 and R2 should be adjusted at the same time. This can be accomplished using the dual potentiometer as demonstrated in Figure 3. Although the pots are linear, the adjustment is logarithmic due to the virtual ground at the op amp's negative input. The component values are selected so that the characteristics dependent on the potentiometer rotation follow Table 1. It must be emphasized that all the adjustments are independent. Gain adjustment has no effect on Q value or frequency. This is true for the Q value and characteristic frequency adjustments as well.

There are several other types of filters that can be derived using this basic configuration. All can be made using linear combinations of the three basic filters, as summarized in Table 2. Figure 4 illustrates a circuit that can be used to implement the linear combination filter. It allows both polarities, and each of its inputs has a variable voltage gain from 0 to 1.



4. This linear-combination arrangement can be used to provide several different types of useful filter characteristics.

The second-order filter also is a building block for higher-order filters. By cascading these filters, even-order filters can be built.

Micropower Circuit Offers Automatic Shutdown And Low-Battery Lockout

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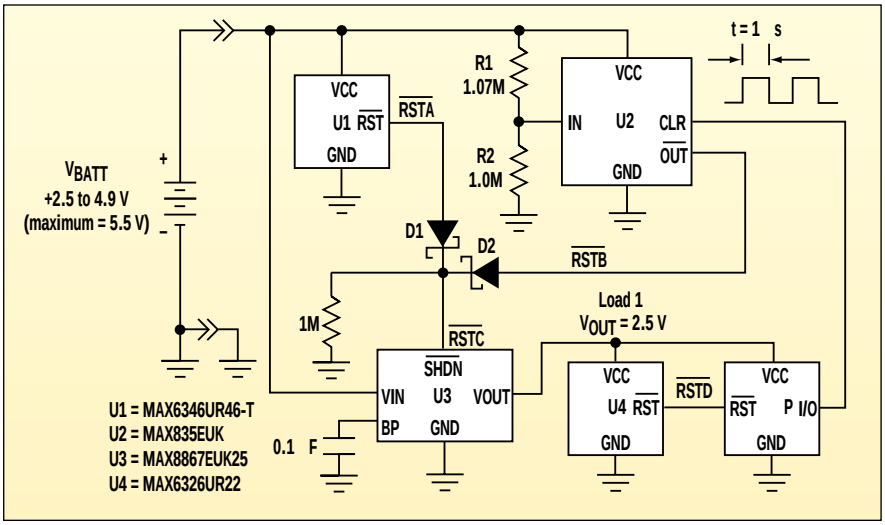
CIRCLE 521



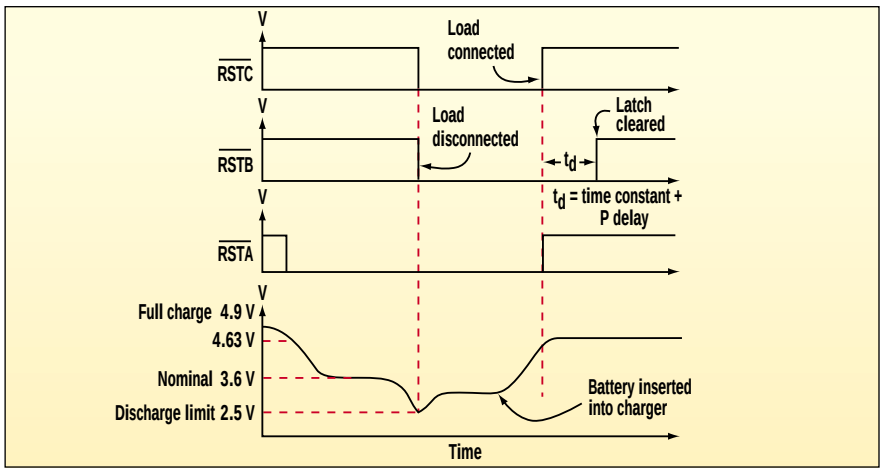
1. This micropower circuit provides shutdown, power-up, and low-battery lockout functions for this three-cell NiCd-based circuit without the need for software or operator control.

This micropower circuit provides shutdown, power-up, and low-battery lockout functions automatically, without the need for software or operator control *(Fig. 1)*. Featuring 2.3-V hysteresis, the circuit eliminates the use of microprocessor I/O pins for charger detection, battery-threshold monitoring, and shutdown control. Under full load, the complete power-management circuit draws less than 200 µA of supply current.

After the cutoff point for battery discharge is reached, the circuit locks out (disconnects) the battery from the load (Load1). This action prevents circuit "chatter" and deep discharge until the battery is in its charger cradle. A common and annoying problem with battery-voltage monitors, chatter is the circuit's response to fluctuations in battery-terminal voltage. These fluctuations take place when the recurring load connections toggle the battery between its discharge and relaxed-open-circuit conditions.

For a three-cell NiCd battery, the typical terminal voltage is 4.9 V fully charged, 3.6 V under load, and 2.5 V at discharge. The load should be disconnected at 2.5 V, but not reconnected as the resulting terminal voltage (V_{BATT}) floats to the open-circuit condition. Figure 1's circuit disconnects the load at 2.5 V and reconnects it while the battery is in its charger cradle (4.68 V).

An ultra-low-power microprocessor(µP)-reset device (U1) generates an active-low output ($\overline{RSTA}$) whenever V_{BATT} equals 4.63 V. The output of a micropower latching comparator (U2) causes $\overline{RSTB}$ to transition low if V_{BATT} is



2. The response of the three reset signals in Figure 1 is shown over a typical discharge-charge cycle. The battery voltage profile is shown in the bottom waveform.

less than 2.5 V. These outputs from U1 and U2 are ORed by diodes D1 and D2, generating a system-shutdown control (RSTC). Figure 2 demonstrates the relationship between the various reset states and the battery-discharge profile.

When V_{BATT} is less than 2.5 V, RSTC disconnects Load1 from the battery by shutting down U3. U3 is a low-noise, low-dropout, linear regulator in an SOT-23 package. It has a preset output of 2.5 V, a maximum ground-pin current of 180 µA (when supplying 150 mA), and a supply current of only 10 nA during shutdown.

If V_{BATT} is greater than 4.63 V, the circuit releases RSTC. As a result, U3 comes out of shutdown and delivers power to the µP. Another µP-supervisor (U4) holds the RSTD signal low until the microprocessor's V_{CC} exceeds 2.2 V. Once RSTD is released, the µP begins operating and clears U2 by pulsing its CLR input high for 1 µs.

Differential Feedback Produces Two Regulated Outputs From One

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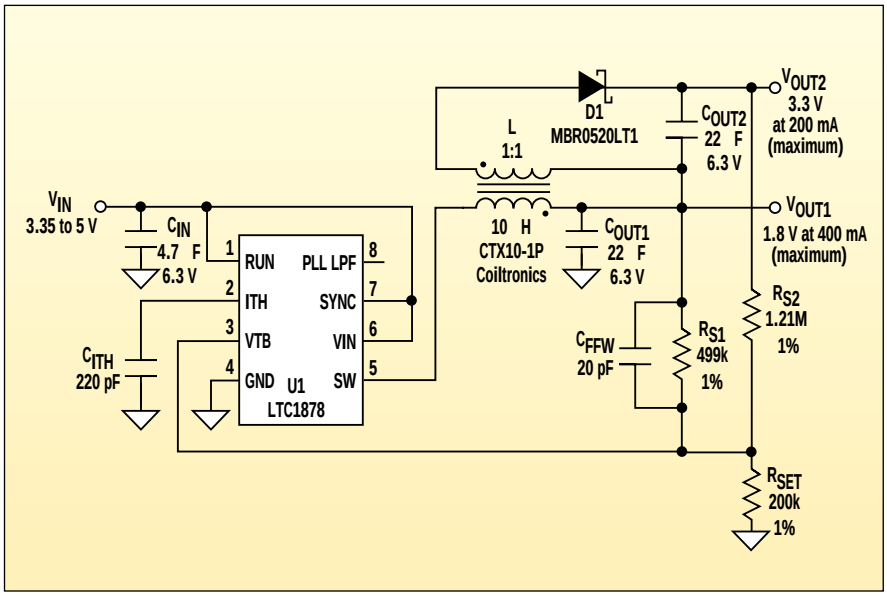
CIRCLE 522

The need often arises for a circuit with two regulated outputs from a single supply (controller). In some cases, the output won't require particularly tight regulation. Instead, only adequate regulation will be necessary for the parts to be powered. This circuit does just that *(Fig. 1)*. It provides two quasi-regulated voltages controlled by one controller IC.

Implemented using a buck regulator with an overwinding, the device's main or "primary" output is 1.8 V (±2.5%) at 300 mA (maximum). Its auxiliary or "secondary" output is 3.3 V (±2.5%) at 150 mA (maximum). The overwinding is 180° out of phase with the primary winding so that the voltage developed across C_{OUT2} is the main output voltage, 1.8 V, minus a diode drop. Adding this to the 1.8-V primary output generates the 3.3-V secondary output voltage.

Both outputs are fed back to the error amplifier via a couple of resistors. Since the error amplifier is configured as a summing-junction amplifier, both outputs are sensed by the error amplifier and driven accordingly. The feedback voltage is developed by the sum of the two feedback currents through the bottom resistor of the voltage divider. Therefore, the error amplifier controls both outputs and maintains 5% regulation on each output over all line and load variations.

All components, including the inductor/transformer, are easy-to-obtain, off-the-shelf items. For instance, the inductor/transformer is a Coiltronics CTX10-1P Econo-Pac. Since the LTC1878 controller used in this circuit operates on very low quiescent current, the circuit is very efficient. At a V_{IN} of 5 V, the efficiency at full load is approximately 80%. Another feature is that the IC will run at 100% duty cycle. Therefore, when the input voltage drops to 3.3 V, the auxiliary output will still regulate at 3.3 V.



Implemented using an "overwinding" on the buck regulator's inductor, this circuit produces two quasi-regulated outputs by incorporating a dual-feedback arrangement.

Series-Connected Transistors Use Differential Heating To Sense Airflow

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Among the methods available for airflow measurement, thermal flow meters enjoy the virtues of simplicity. They also offer simple construction, low cost, and superior sensitivity to low flow rates (less than 1000 fpm). All thermal anemometers make use of the relationship between airspeed (A_F) and the thermal impedance (Z_T) of a heated sensor. One practical example of such a relationship is this model of the TO-92's thermal impedance:

$$Z_T = Z_J + 1/(S_C + K_T\sqrt{A_F})$$

where: Z_J = "total immersion" junction-to-case thermal impedance = 44°C/W

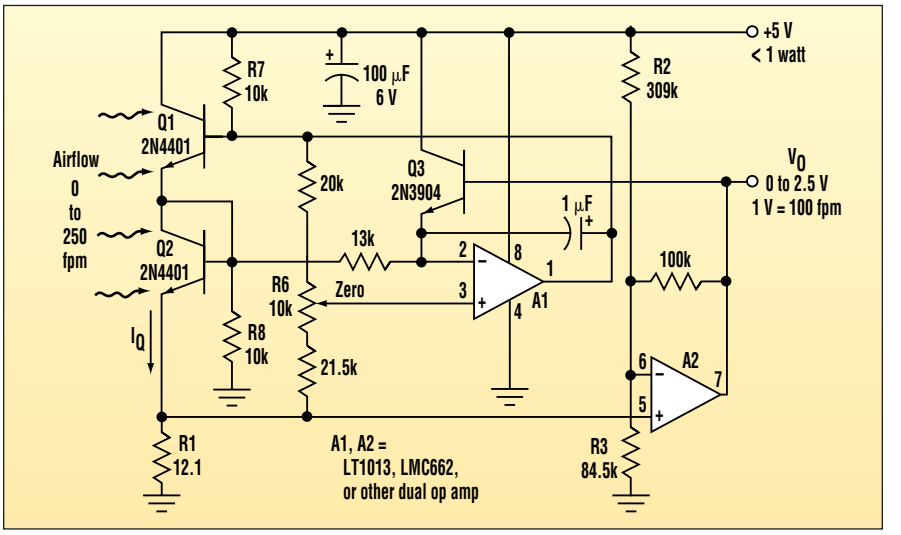
S_C = still-air case-to-ambient conductivity = 6.4 mW/°C

K_T = King's Law thermal diffusion constant = 75 µW/°C–$\sqrt{\text{fpm}}$

A_F = airspeed in ft/min

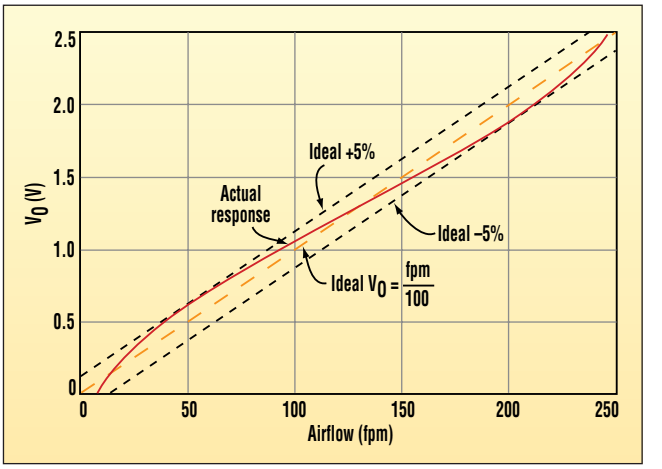
In this model, the raw sensor output is inherently nonlinear with airspeed, a problem common to all thermal airspeed sensors. To compensate, thermal anemometer designs must include some provision for measurement linearization. The circuit in Figure 1 combines ideas from two earlier IFDs (*"Low-Power Thermal Airspeed Sensor,"* ELECTRONIC DESIGN, *May 25, 1998, p. 116; and "Low-Power Solid-State Airflow Detector,"* ELECTRONIC DESIGN, *Jan. 22, 2001, p. 118*). In doing so, it implements a simple, linearized (±5%), ambient-temperature-compensated thermal anemometer. A robust, power-efficient device, it draws less than 1 W of total operating power from a single regulated 5-V rail.

In operation, A1 maintains a constant temperature differential (about 25°C) between Q1 and Q2, independent of changes in thermal impedance and ambient temperature. A1 achieves this by maintaining a constant ratio between the two transistors' V_{BE} voltages. It can do so by controlling the collector currents of the series-connected devices, and thereby their power dissipation.



1. The circuit combines ideas from two earlier IFDs to implement a simple, linearized thermal anemometer. An ambient-temperature-compensated device, it is robust and power-efficient.

Since both transistors pass the same current (I_Q), their relative power dissipations are determined solely by their respective V_{CE} voltages. $V_{Q1} > V_{Q2}$ for all valid operating modes (Q3 sees to this). So for any given I_Q, Q1 will always dissipate more power and more heat, meaning it will run hotter than diode-connected Q2. Consequently, as airflow increases and thermal impedance decreases, A1 can hold any chosen Q1/Q2 temperature differential by increasing I_Q. The resulting air-



2. The quadratic relationship between I_Q and Q1/Q2's power dissipation does a fair job of canceling nonlinearity, erasing all but ±5% FSR linearity error over the range of on-scale airspeeds.

flow-dependent I_Q is sensed by R1, then offset and boosted by A2. In turn, it becomes the 0- to 2.5-V anemometer output signal V_O, scaled for 10 mV = 1 fpm = 0 to 250 fpm (~2.5 kts).

Meanwhile, Q3 acts with A2 to limit the maximum voltage across R1 to about 2 V. This is done to avoid the risk of latch-up, which would occur if A1's output were allowed to rise too near the 5-V rail. In that event, V_{Q1} would approach V_{Q2}. As a result, it would be impossible to achieve the programmed temperature differential and Q1/Q2 V_{BE} ratio, no matter how high I_Q might rise. Similarly, R7 and R8 prevent latch-up when the circuit is first powered up.

But what about measurement linearization? As illustrated in Figure 2, the inherent quadratic relationship that exists between I_Q and Q1/Q2's power dissipation does a fair job of canceling nonlinearity. It erases all but ±5% FSR linearity error over the entire range of on-scale airspeeds. Also, anemometer calibration is quick and straightforward. The transistor sensor pair is simply placed in slowly moving air (almost, but not quite stagnant; A_F = 5 to 7 fpm is ideal). R6 is then adjusted for V_O = 0.

The "tranemometer" is illustrated with circuit constants that scale its output for V_O = 0.01 V/fpm = 1 V/kt. Yet virtually any range of airflow rates can be accommodated with appropriate choices for R1, R2, and R3.

Quad Video Amp Splits And Buffers An S-Video Signal

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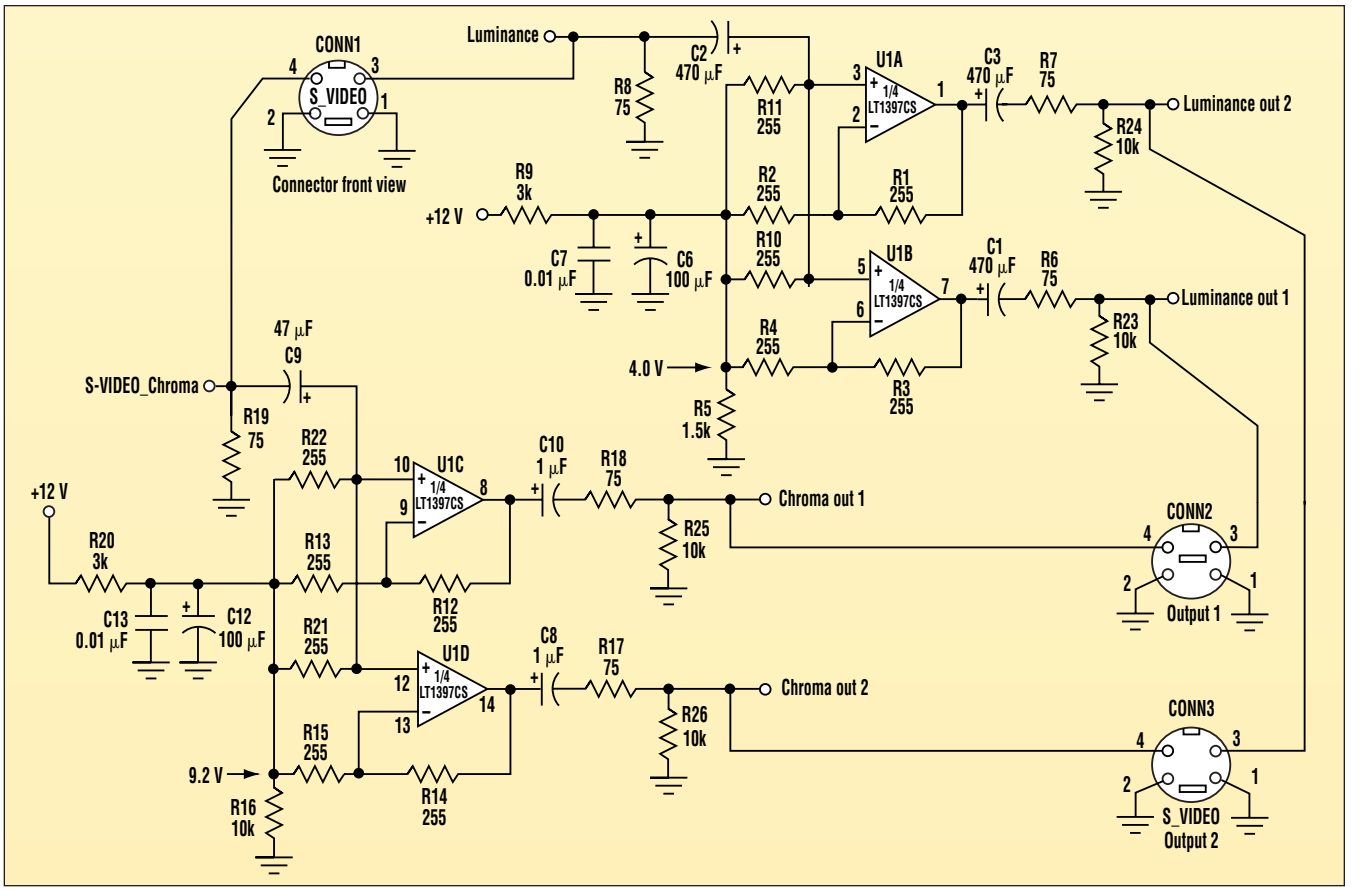
CIRCLE 481

This circuit employs a quad 400-MHz gain-bandwidth, 800-V/µs, low-power, current-feedback amplifier *(Fig. 1)*. It's used to split a single S-video signal input (luminance and chroma) into two buffered S-video signal channels. Each channel can drive 80 mA into standard 75-Ω video cables.

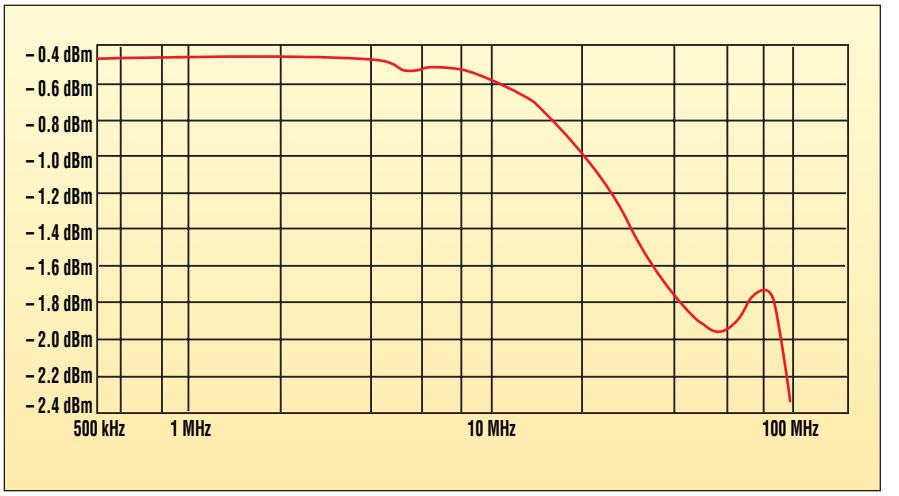
High-valued coupling capacitors are used at the input and outputs of the current feedback amplifiers to prevent loss of low-frequency information. The 10-kΩ resistors on the outputs allow the 470-µF output-coupling capacitors to charge. This reduces spikes when the cables are connected to the amplifier. The amplifiers are biased to prohibit the signal from clipping. R9 and R5 bias U1A and U1B to 4.0 V, while R20 and R16 bias U1C



1. A quad 400-MHz current-feedback amplifier is used to split an S-video signal into two buffered S-video signals.

and U1D to 9.2 V. Consequently, the amplified luminance and chroma signals are restricted from running into the supply rails.

The gain for this circuit (and layout) is flat to within ±0.2 dB from 500 kHz to 13 MHz for a unity gain *(Fig. 2)*. The 3-dB point for this circuit (and layout) is 112 MHz. A comparison between the input and output signals of a burst of chroma information revealed virtually no loss of signal fidelity. An input/output comparison of a stepped luminance signal also indicated no fidelity loss. The amplifiers in this circuit draw only 4.6 mA each, making the device an excellent low-power video-distribution amplifier solution.



2. The unity-gain amplifier's gain is flat to within ±0.2 dB from 500 kHz to 13 MHz.

4-To-20-mA Loop Powers Temperature Sensor

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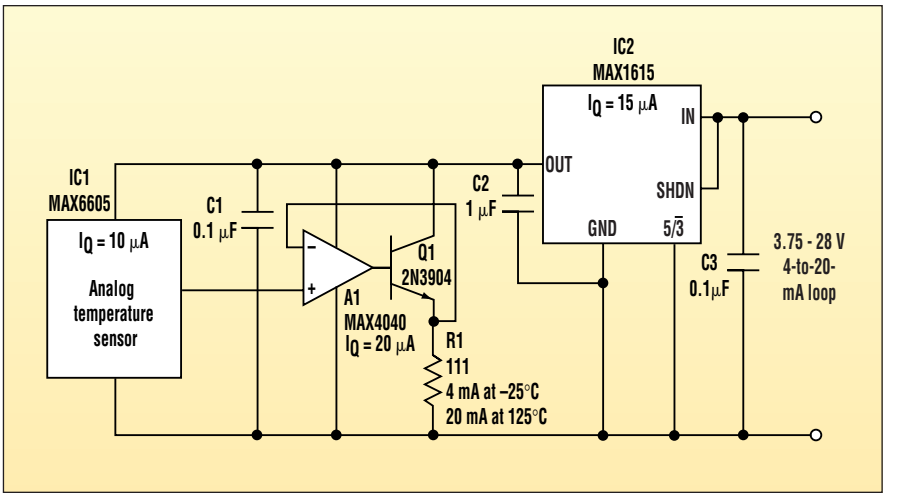
CIRCLE 482

Using an analog temperature sensor, an op amp, a transistor, and a low-dropout linear regulator, this circuit provides a 4-to-20-mA output over a 3.75- to 28-V compliance range *(see the figure)*. Because the devices used maintain a low quiescent current, they can be powered by the loop with a slight offset error being the only consequence.

The temperature sensor IC1 feeds the op-amp/transistor combination, A1 and Q1, with R1 acting as the load on the amplifier. The temperature sensor's output characteristic is described by an offset of 744 mV at 0°C and a scale factor of 11.9 mV/°C.

R1 is selected to achieve the best possible fit between IC1's temperature range and the 4-to-20-mA output. In this example, IC1's output at –25°C is 0.4465 V. Also, a 111-Ω resistor for R1 will supply a 4-mA output at –25°C. At 125°C, IC1's output is 2.213 V, yielding a 19.937-mA output with the 111-Ω resistor previously selected for R1. This current is reflected at the input of the low-dropout linear regulator IC2.

IC2 regulates the voltage to the sensor and op-amp circuit. Also, at the input voltage, it supplies the compliance necessary for connection to the 4-to-20-mA loop. Another feature of IC2 is that it's pin-programmable to generate either a 3- or 5-V output. In this circuit, IC1 and A1 operate at 3 V. This maximizes the input compliance by permitting input voltages as low as 3.75 V. This also results in a slight reduction of quiescent current of IC1 and A1, decreasing the error related to their quiescent currents.



Using low-quiescent-current devices, this temperature sensor derives its power directly from the 4-to-20-mA current loop. This results in a slight offset error that can be compensated out.

The quiescent currents of all components combine and add to the 4-mA output that corresponds to negative full-scale. Consider this 45-µA current in light of the output-current scale factor, which is proportional to:

$$\frac{119\ \text{mV/°C}}{\text{R1}}$$

This yields a current of 106.66 µA/°C. The 45-µA quiescent current represents an offset of approximately 0.43°C. Since the current is an offset, it's possible to compensate for it elsewhere (such as in software, when the temperature data is digitized).

PLD Code Implements Arbitrary CRC Functions

Clive Bolton and Ken Sinclair

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CIRCLE 520

This idea presents PLD code that can be used to generate arbitrary polynomial cyclic-redundancy-check (CRC) functions.

Communication systems often use CRCs to detect transmission errors. CRC functions are typically implemented as shift registers with a series of taps into which the last bit in the shift register is XOR'd.

Written in Altera's high-level design language (AHDL), the PLD code can be directly compiled into any of Altera's programmable logic devices (*shown below*). Both CRC and residue-matching outputs are implemented.

The module automatically generates the required hardware from six compile-time parameters, including WIDTH, POLYNOMIAL, SEED, INVERT, RESIDUE, and MATCH_PIPELINE. These

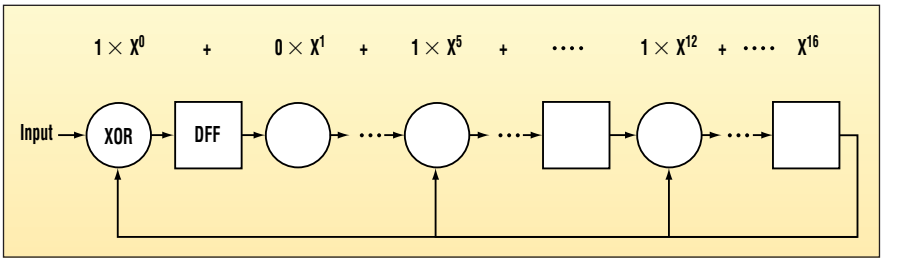
```
%————————————————————————————————————-
% PLD Code Implements Arbitrary CRC Functions
% Author: Clive Bolton and Ken Sinclair
%       Bolton Engineering, Inc.,
%       72 Stone Place, Melrose, MA 02176
%       E-mail: cbolton@world.std.com
% Filename: crc.tdf
%————————————————————————————————————-
% Implements a general-purpose serial-input CRC generator/checker.
% By setting several parameters, the design can  implement a
% variety of CRC polynomials.
%————————————————————————————————————-
% Please note that the only CRC implementation we have actually
% used is the CRC-CCITT implementation; we believe the others are
% correct, but we have not had a chance to verify them.
%
% Check out this url for a good tutorial on how CRCs work:
%   http://bbs-koi.uniinc.msk.ru/tech1/1994/er_cont/crc_how.htm
%————————————————————————————————————-
% Update: by Ken Sinclair
% Added SEED and INVERT parameters needed for correct
% implementation of the CRC-CCITT specification.  Also changed
% the implementation to the simpler current-remainder bit-serial
% one recommended in the following reference, excerpted below:
%
%   Ritter, T. 1986. The Great CRC Mystery. Dr. Dobb's Journal
%               of Software Tools. February. 11(2): 26-34, 76-83.
%
% "The CRC result can be obtained without shifting in the two zero
% bytes by rearranging the CRC register and feeding the data in at
% the top end of the system (see Figure 2, below).  By shifting the
% CRC register we can shift zeros in from the right.  The data bit
% will be compared to the MSB in the CRC register, and only if they
% differ will the polynomial be subtracted.  As before, this acts
% to keep the full remainder in the register; however, the
% remainder is now correct after each bit, and requires no trailing
% zeros.
%
%                 Example Poly = x^5 + x^4 + x^2 + 1 = 110101
%     INPUT
%       |     x^4         x^3     x^2          x^1     x^0
%       V    +—-+        +—-+   +—-+        +—-+   +—-+
%    +<-XOR<-|Q D|<-XOR<-|Q D|<—|Q D|<-XOR<-‖Q D|<—|Q D|<-+
%    |       |   |   ^   |   |   |   |   ^   ‖   |   |   |  |
%    |       +—-+   |   +—-+   +—-+   |   |   +—-+   +—-+  |
%    |              |                 |   |                |
%    +———————-———————+—-———————————————+———————————————-+
% (endquote)
%
% ——— Defines for CRC-16 polynomial X^16+X^15+X^2+1 ———
% With MATCH_PIPELINE == 1, CRC-16 runs at 125 MHz in 10K10-3
%                           and takes 21 LCs
%       WIDTH               = 16;
%       POLYNOMIAL          = B"1000000000000101";
%       SEED                = H"FFFF";
%       INVERT              = "YES";
%       RESIDUE             = "800D";
%
% ————————- Defines for CRC-32 polynomial ————————-
% X^32+X^26+X^23+X^22+X^16+X^12+X^11+X^10+X^8+X^7+X^5+X^4+X^2+X+1
% With MATCH_PIPELINE == 2, CRC-32 runs at 125 MHz in 10K10-3
% With MATCH_PIPELINE == 1, CRC-32 runs at 99 MHz  in 10K10-3
%                           and takes 45 LCs
%       WIDTH               = 32;
%       POLYNOMIAL          = B"00000100110000010001110110110111";
%       SEED                = H"FFFFFFFF";
%       RESIDUE             = H"DEBB20E3";
%       INVERT              = "YES";
%
% ——— Defines for CRC-CCITT polynomial X^16+X^12+X^5+1 ———-
% This is the only polynomial actually tested in hardware
%       WIDTH               = 16;
%       POLYNOMIAL          = B"0001000000100001";
%       SEED                = H"FFFF";
%       INVERT              = "YES";
%       RESIDUE             = H"1D0F";
%————————————————————————————————————-

PARAMETERS
(       WIDTH               = 16,                   — Defaults to CRC-CCITT
        POLYNOMIAL          = B"0001000000100001",  — Polynomial, MSB left out
        MATCH_PIPELINE      = 1,                    — # clks after which out=active
        SEED                = H"FFFF",              — Initial value (for sinit)
        INVERT              = "YES",                — 1's complement result
        RESIDUE             = H"1D0F"               — Constant remainder
);

SUBDESIGN CRC
( ———————————- INPUT PINS ———————————
        clock               : INPUT;
        enable              : INPUT = VCC;          — Shift enable
        shiftin             : INPUT;                — Input data
        aclr                : INPUT = GND;          — Async Clear
        sinit               : INPUT = GND;          — Loads SEED at start of xfer
        calculate           : INPUT = VCC;          — 1 to calc, 0 to shift
  ———————————- OUTPUT PINS ———————————-
        q[WIDTH-1..0]       : OUTPUT;               — CRC result
        match               : OUTPUT;               — CRC == RESIDUE
                                                    — (not gated by enable)
        shiftout            : OUTPUT;
)
VARIABLE
  ———————————— NODES ————————————
        s[WIDTH-1..0]     : NODE;
        poly[WIDTH-1..0]: NODE;
        feedback : NODE;

BEGIN
        poly[]   = POLYNOMIAL;

        FOR i IN 0 to (WIDTH-1) GENERATE
                q[i]   = DFFE(s[i], clock, !aclr, VCC, enable);
        END GENERATE;

        — Pipeline this value on system clock just to relax timing requirements
        feedback = DFF((shiftin XOR q[WIDTH-1]) AND calculate, clock, !aclr, VCC);

        IF sinit THEN
                s[] = SEED;
        ELSE
                s[0] = feedback;
                FOR i IN 0 to (WIDTH-2) GENERATE
                        s[i+1] = q[i] XOR (feedback AND poly[i+1]);
                END GENERATE;
        END IF;

        IF INVERT == "YES" GENERATE
                shiftout = NOT q[WIDTH-1];
        ELSE GENERATE
                shiftout = q[WIDTH-1];
        END GENERATE;

        IF USED(match) GENERATE
          match =LPM_COMPARE(.dataa[]=q[],.datab[]=RESIDUE,.clock=clock,.aclr=aclr)
                        WITH (LPM_WIDTH=WIDTH,LPM_PIPELINE=MATCH_PIPELINE,
                        ONE_INPUT_IS_CONSTANT="YES") returns (.aeb);
        END GENERATE;
END;
%————————————————————————————————————-
```

parameters are used to define the CRC function as follows:

WIDTH sets the CRC length.
POLYNOMIAL sets the taps at which XOR gates are added.
SEED sets the value loaded into the shift register at the start.
INVERT determines whether the CRC output of the chain is inverted.
RESIDUE sets the value to which the result is compared at the end of the calculation.
MATCH_PIPELINE sets the number of clocks after which the residue-match output becomes valid.

As shown in the figure, a CRC-CCITT function of $X^{16} + X^{12} + X^5 + 1$ can be generated by setting:

WIDTH = 16
POLYNOMIAL = H"1021"
SEED = H"FFFF"
INVERT = "YES"
RESIDUE = "1D0F"
MATCH_PIPELINE = 1



The sample CRC-CCITT polynomial function of $X^{16} + X^{12} + X^5 + 1$ can easily be generated for an Altera PLD by simply setting a few parameters in the AHDL code.

When the polynomial is being set, its most significant bit is omitted because no XOR gate is implemented at the end of the shift chain. Polynomials for CRC-16, CRC-32, and CRC-CCITT functions are included in the source code. The CRC-CCITT polynomial is the only one that has been tested in actual hardware. All of the others have been included for reference only.

Although the code is written specifically for Altera's devices, the program structure and flow are readily translatable into VHDL or Verilog. When implemented as part of a low-end EPF10K10-3 device, a CRC-CCITT function with EQZERO_PIPELINE = 1 takes 23 LCs and runs at 125 MHz.

While the math behind CRCs is fairly straightforward, bridging the gap between the math and hardware requires an understanding of modulo-two arithmetic, polynomials, and logic. A good detailed reference on the subject can be found in *Data and Computer Communications*, William Stallings, Prentice Hall, N.J., 1997.

Dual-Regulated Voltages Control STN-LCD Contrast

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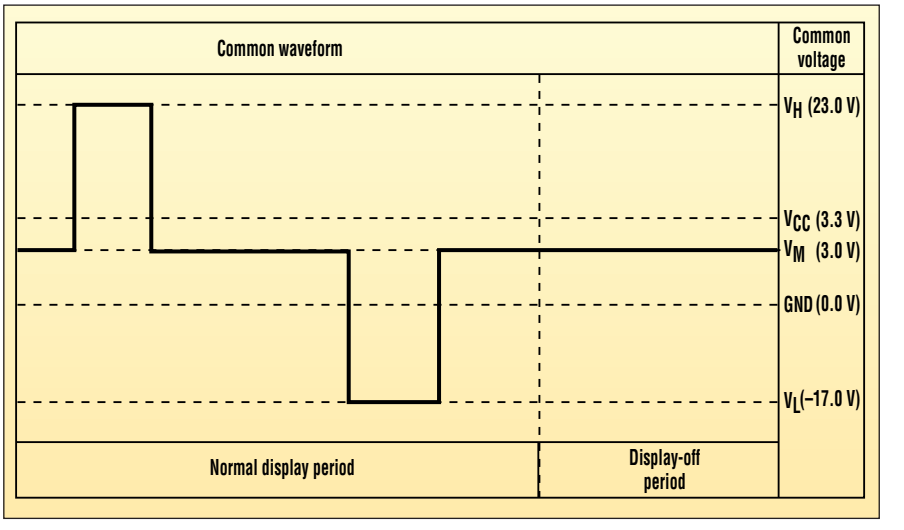
Generating a stable, dual-voltage, LCD-contrast supply can be difficult, particularly if the two voltage amplitudes must track each other with respect to a given reference level. In Figure 1, the ±20 V outputs are centered on a 3-V reference level (V_M). The contrast voltages must be symmetric about V_M to avoid creating a dc component across the liquid crystal. If this were to occur, it would damage the LCD or shorten its life.

Figure 2's arrangement provides a triple-output, regulated LCD supply, which produces a main supply voltage and two LCD voltages symmetric around the LCD offset voltage (V_M). To achieve this, four Schottky diodes (D1 to D4) and two flying capacitors (C2 and C3) were added to a dual-V_{OUT} circuit. U1 normally supplies a digital V_{MAIN} (typically 3.3 V) and an LCD supply (up to 28 V). Here, the ±LCD output equals $V_M \pm LCD_{REF}$.



1. In order to avoid creating a damaging dc component across the LCD, the contrast waveforms generated by the supply must be symmetric about the LCD reference level V_M.

U1 is a high-efficiency, dual-output boost converter for portable devices needing two regulated outputs. Operation with inputs as low as 0.7 V allows it to accept one-, two-, or three-cell alkaline, NiCd, or NiMH batteries, as

well as one-cell Li-ion batteries. It requires no external switching FETs and draws only 20 µA of supply current, making it ideal for handheld PDAs and pen-input devices.

A switching FET internal to U1 repeatedly connects LCDLX (pin 12) to ground and then releases it. As a result, the LCDLX voltage toggles between ground and LCDR plus one diode drop (LCDR is the LCD_{REF} output). This action, similar to that which produces the V_{MAIN} output at pin 16, generates the ±LCD voltages as follows:

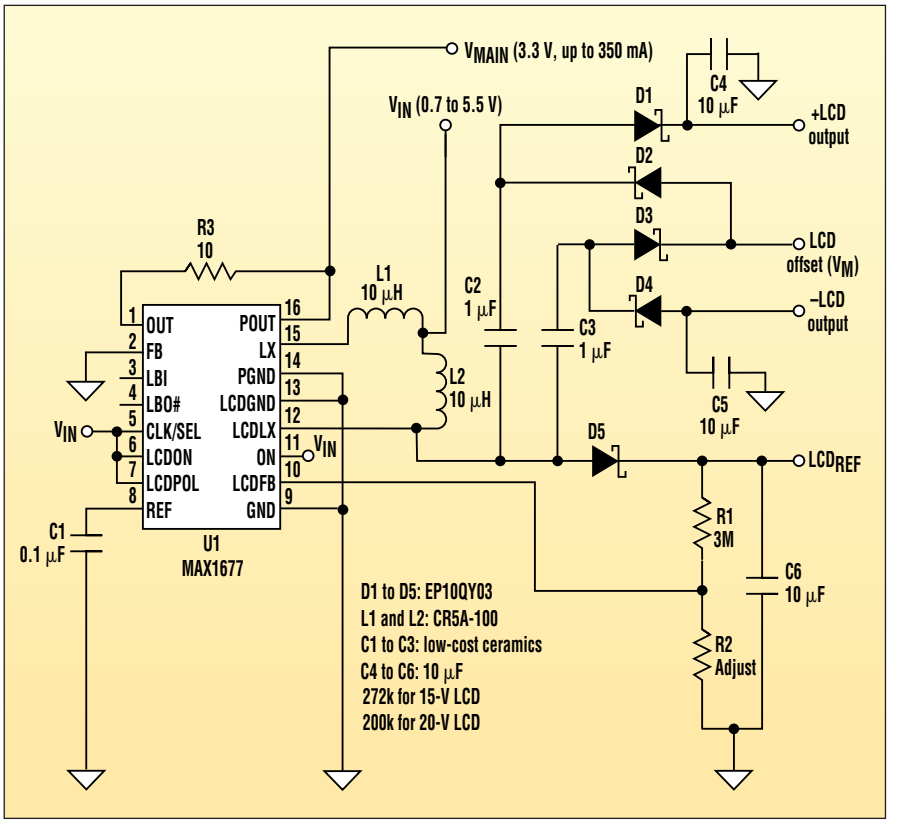
In phase 1 (–LCD output), the rise of LCDLX voltage to $LCD_{REF} + V_{DIODE}$ forces voltage on the other side of C3 to $V_M + V_{DIODE}$. Doing so creates a differential voltage of $LCD_{REF} - V_M$ across C3. The LCDLX voltage is the reference point. During phase 2, as LCDLX goes to ground, the load side (–LCD OUT) sees a voltage equal to $-LCD_{REF} + V_M$. This drives current from the –LCD load through D4. When this current flow discharges C3 slightly, the cycle starts again. Note that the +LCD and –LCD outputs develop on alternate phases. The resulting –LCD voltage is:

$$-\text{LCD OUT} = -LCD_{REF} + V_M + V_{DIODE}$$

In phase 2 (+LCD side), when LCDLX goes to ground, the load side of C2 sees a voltage equal to $V_M - V_{DIODE}$. Then, phase 1 takes place. The rise of LCDLX to $LCD_{REF} + V_{DIODE}$ forces a voltage of $LCD_{REF} + V_M$ on the other side of C2. The +LCD load also sees an additional diode drop across D5:

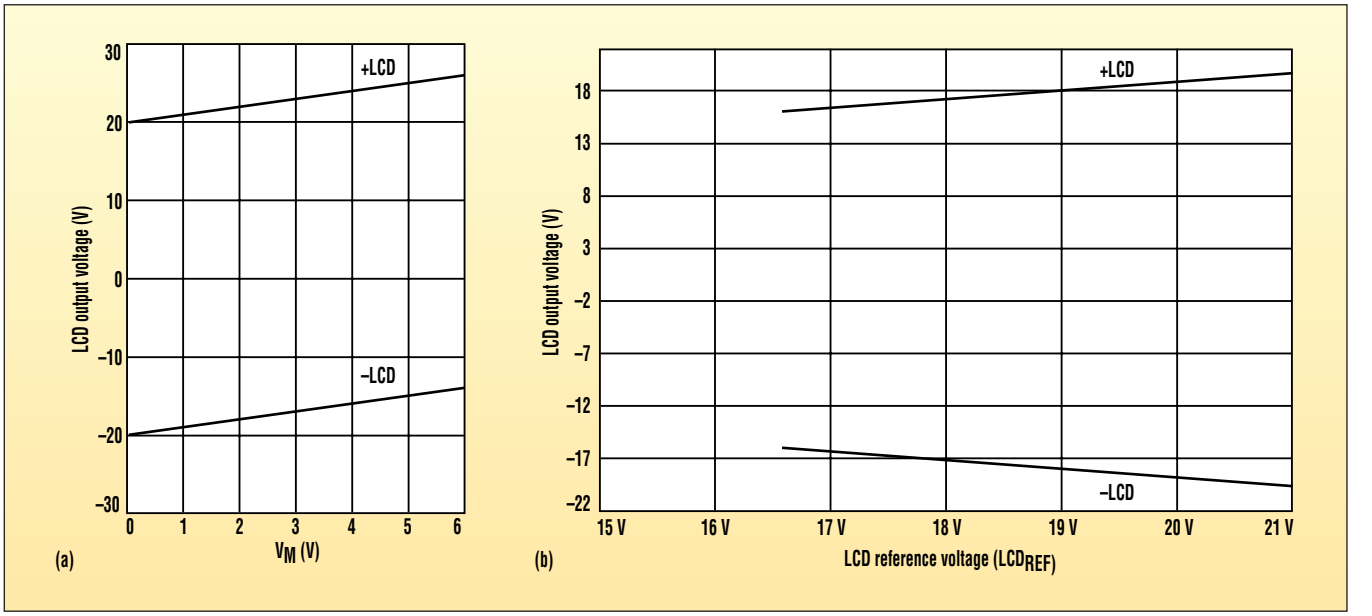
$$+\text{LCD OUT} = LCD_{REF} + V_M - V_{DIODE}$$

These load equations show that –LCD OUT and +LCD OUT track each other with respect to LCD_{REF} *(Fig. 3)*. They're offset from V_M by less than one diode drop.



2. Implemented using a high-efficiency, dual-output boost converter, this single-IC circuit generates the dual voltages that are required to control the contrast in an STN LCD.

Schottky iodes D1 to D5 can be EP10QY03 or MBR0530 types. C2 and C3 can be 1 µF, preferably with voltage ratings of at least $2 \times LCD_{REF}$. Typical L1 and L2 values are 10 µH each. The output capacitors (C4 to C6, shown as 10 µF) may be sized according to the allowable output ripple.



3. The ±LCD outputs track each other and the LCD reference voltage (a), as well as the sum of V_M ±LCD_{REF} (b).

Decompensated Op-Amp Gain Is Adjustable From Zero To Open-Loop

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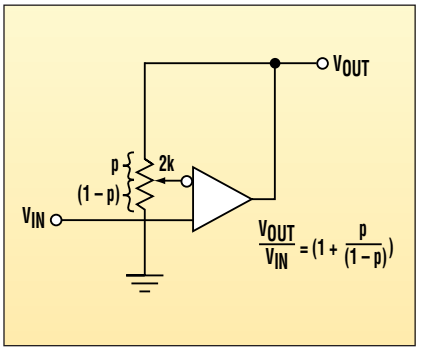
CIRCLE 520

Over three decades ago, the internally frequency-compensated, monolithic op amp was introduced. Since then, many of these devices have been made available in two variations. While both versions are designed to maintain the same dc parameters, they demonstrate very different ac characteristics.

In op-amp duos such as these, one member is heavily frequency-compensated to provide stability at unity gain (exemplified by the LF156, OP27, and LT1007). Meanwhile, its partner plays the role of the much faster, albeit sometimes "twitchy," decompensated sibling (the LF157, OP37, and LT1037, respectively). In each case, the decompensated member enjoys about a four to five times advantage in slew rate and gain-bandwidth product over its more stable partner. "Decomps" are therefore the obvious choice for high-speed high-gain amplifier applications.

But sometimes there's a penalty for making this selection. This is true when an application requires a variable gain that can be set over a range extending below the op amp's minimum stable closed-loop gain (G_{MIN} = typically 5). The problem exists in simple and versatile gain-set topologies



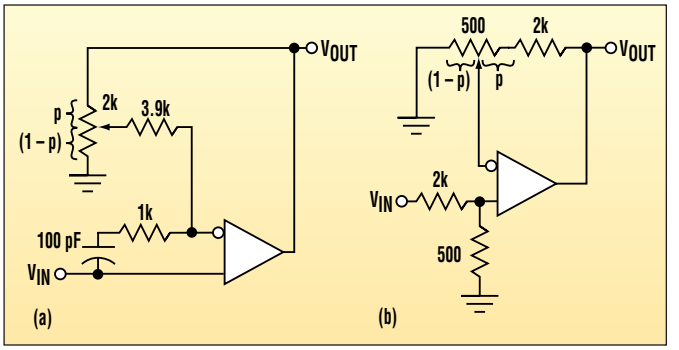
1. A decompensated op amp with the typical gain-set arrangement can exhibit instability when low gain settings are used.

whose gain is given by G = 1 + p/[1 – p], where 0 < p < 1 *(Fig. 1)*. While perfectly usable with unity-gain-stable op amps, these configurations won't work with their high-pressure decompensated alter egos when $G < G_{MIN}$. Trying to use this type of circuit to set a decomp's gain to unity or less will result in instability or outright oscillation.

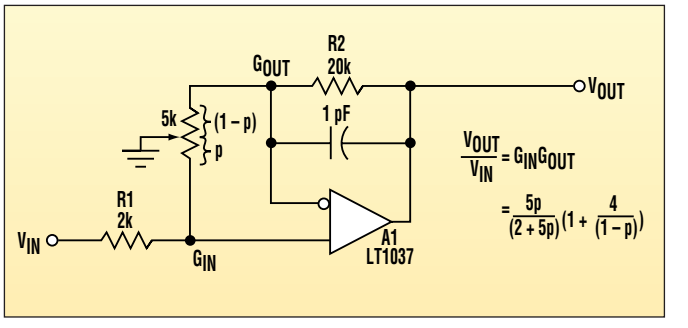
In principle, the G_{MIN} gremlin could be exorcised with an ac-gain-limiting, or it may be driven out with a brute-force $1/G_{MIN}$ input attenuator *(Fig. 2)*. While they definitely work, these circuits are far from ideal. The rub is that they unnecessarily erode the noise and gain performance at high gain settings (by a whopping 14 dB for the circuit in Figure 2b). As a result, such circuits waste most of the benefits of using a decompensated op amp in the first place. A better solution would be to make Figure 2's input-attenuator variable instead of fixed. Then it could get out of the way when $G >> G_{MIN}$.

Figure 3 shows how to do this without incurring the cost of a dual potentiometer. The circuit here relies upon an idea suggested in a previous IFD *(see "One Single-Section Potentiometer Sets The Gain On Two Channels," W. Stephen Woodward,* ELECTRONIC DESIGN, *Feb. 5, 2001, p. 115)*. As described in this earlier article, grounding the pot wiper creates two mechanically linked but electrically independent variable resistors. The bottom half (pR) cooperates with R1 to form a variable input attenuator with a gain of: $G_I = 5p/(2 + 5p)$. So G_I, the attenuator's gain, goes from zero to near unity, more or less, as p goes from 0 to 1.

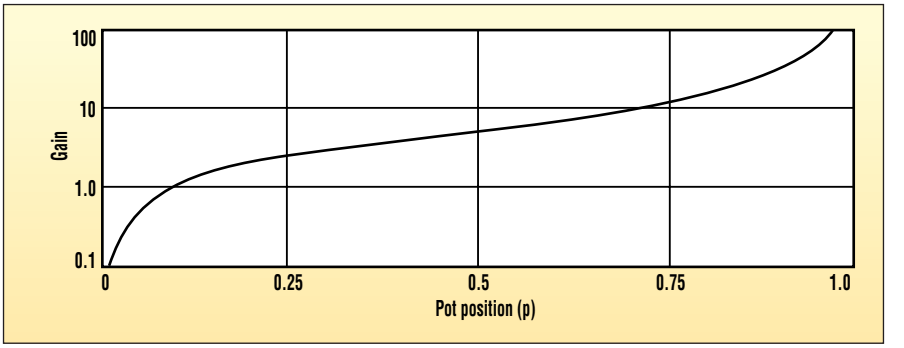
Meanwhile, the top half of the pot, (1 – p)R, forms a variable feedback network with R2. This network sets A1's closed-loop gain as a function of p: $G_O = [1 + 4/(1 – p)]$. Note that $G_O > 5$ (A1's G_{MIN}) for all values of p. Also, noise



2. Overcoming the G_{MIN} problem can be accomplished using an ac-gain-limiting network (a) or a brute-force $1/G_{MIN}$ input attenuator (b).



3. By modifying Figure 2b's topology, the input attenuator can be made variable by grounding the pot wiper to create two mechanically linked but electrically independent variable resistors.



4. The resulting composite gain-versus-p curve ($G = G_I \times G_O$) is shown. The possible gain settings extend from zero (at p = 0) to the open-loop gain of the op amp (at p = 1).

performance at high gain ($G >> 1$) is only 3 dB worse than it would be if there were no pR input attenuator at all.

The resulting composite gain-versus-p curve ($G = G_I \times G_O$) is graphed in Figure 4. It runs from zero (at p = 0) to open loop (at p = 1). Since it's dependent on the circuit layout, feedback-capacitor C is best optimized empirically. A good place to start, however, is $C = 1/(2\pi \times GBW \times R2)$. In this equation, GBW represents A1's gain-bandwidth product (60 MHz for the LT1037).

Latching Overvoltage Indicator Handles Large Overloads

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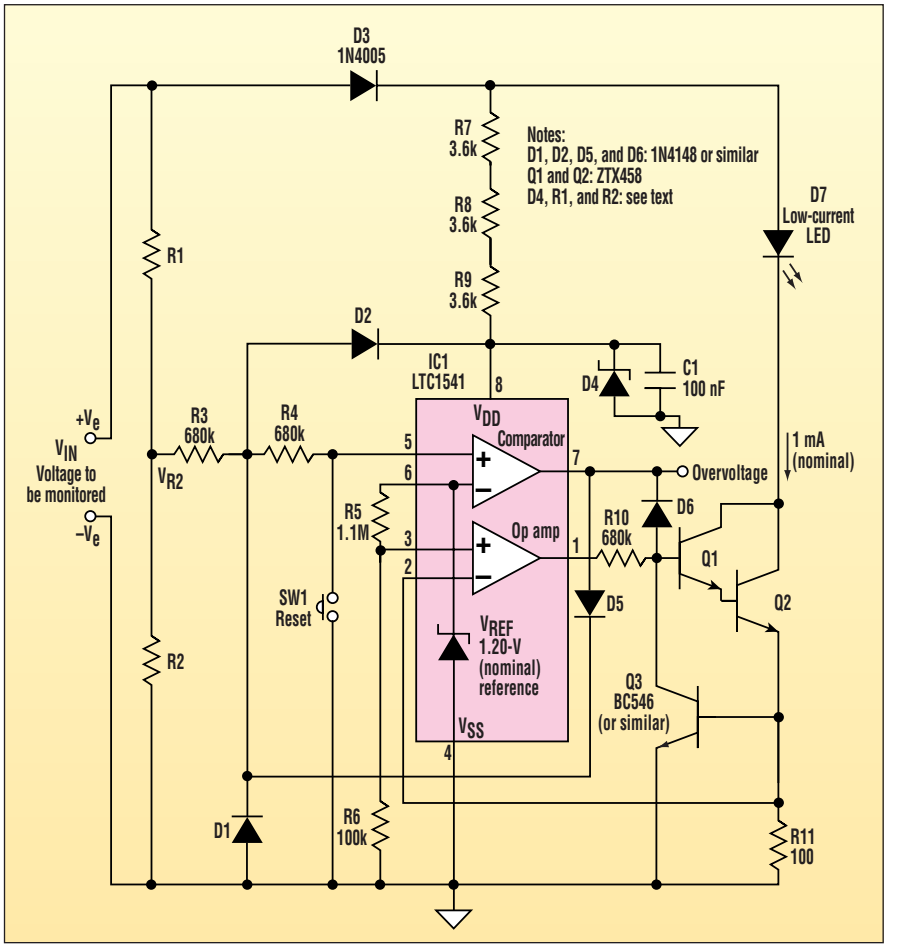
This overvoltage detector can be connected to any dc power source *(Fig. 1)*. Its purpose is to provide a visual indication of when the voltage exceeds a preset value, which may range from around 3 V to several hundred volts. The circuit also implements latching overvoltage detection, allowing it to capture transient overvoltage spikes as narrow as 30 µs.



This latching overvoltage detector draws less than 25 mA under normal operating conditions.

Under "normal" voltage conditions, the whole circuit draws less than 25 µA, making it ideal for monitoring battery-powered systems. But despite its frugal diet, the detector is a fairly tough character, able to withstand continuous mains overloads without damage.

IC1, an LTC1541, is a micropower comparator, op amp, and voltage reference (1.20 V nominal) with a maximum quiescent current of just 13 µA. The op amp and the Q1/Q2 Darlington pair form a precision current sink. With R5 = 1.1 MΩ and R6 = 100k, the op amp puts a nominal 100 mV across R11. By doing so, it sinks 1 mA through the LED (D7). If the LED is a low-current type, such as the HLMP-D155, 1 mA is sufficient to achieve adequate brightness.

With no overvoltage condition present, IC1's comparator output is low. It clamps Q1's base to around 0.6 V via D6, which holds the current sink off. R1 and R2 determine the trip voltage, V_T (the value of V_{IN} at which the circuit indicates an overvoltage).

When the voltage (V_{R2}) across R2 exceeds the 1.20-V reference, the comparator trips and its output goes high. D6 becomes reverse-biased, enabling the current sink to illuminate the LED. This provides immediate visual indica-

tion of the overvoltage event. At the same time, D5 becomes forward-biased, pulling the comparator's noninverting input toward V_{DD}. The circuit is now latched, and the comparator output remains high even if V_{R2} subsequently falls below 1.20 V. By either disconnecting V_{IN} or momentarily closing switch SW1, the circuit can be reset.

Under normal conditions, when D6 clamps Q1's base, the op-amp output rises toward V_{DD}, desperately trying to bias Q1 on. Consequently, a substantial value is needed for R10 to minimize the op amp's output current (which adds to IC1's quiescent current). This means that only a few microamperes are available at Q1's base, dictating the use of the Darlington pair. The ZTX458 devices specified for Q1 and Q2 have an h_{fe} high enough to furnish the LED with 1 mA when Q1's base current is as low as 1.5 µA. Since they're high-voltage types, rated to 400 V, they can withstand the 350-V peak voltage of the 240-V_{RMS} mains supply.

If a MOSFET were substituted in place of the Darlington pair, its voltage and power ratings would have to cope with the worst-case anticipated overload. In addition, the MOSFET's gate-threshold voltage would need to be low enough to allow operation at lesser values of V_{IN}.

D1 to D4 and R7 to R9 supply IC1 with overload protection. Diode D3 blocks any excessive negative inputs. The 1N4005 has a 600-V reverse voltage rating, which is more than adequate for a 240-V_{RMS} overload. Diode D2 protects the comparator input against high positive voltages.

For precision voltage monitoring, R1 must be connected "upstream" of D3 as shown. Therefore, D1 is required to protect the comparator input against excessive negative voltages. Selecting a large value for R3 provides ample current limiting for D1 and D2. It also makes it necessary for the comparator to source negligible current through D5, permitting a relatively small value to be selected for R2 if required. Resistor R4 offers additional current limiting for the comparator input. Plus, it prevents the comparator output from being dragged low via D5 when SW1 is closed to reset the circuit.

Because the comparator's input bias current is very low (1 nA maximum), the voltage dropped across R3 and R4 is negligible. Zener diode D4 clamps IC1's positive supply to a safe value. Since the LTC1541's maximum working voltage is 12.6 V, using an 11-V zener is an appropriate selection.

A single resistor with suitable power and voltage ratings could be used instead of R7 to R9. But connecting three resistors from the MRS25 series (0.6-W, 250-V) in series guarantees that the parts will easily withstand a mains overload. The resistance values should be great enough to satisfy the 0.6-W power rating and ensure the zener's power dissipation is kept low. Using large values also minimizes the circuit's current draw when V_{IN} exceeds the zener voltage. Yet the values shouldn't be too big, otherwise, IC1's V_{DD} current will cause a relatively significant voltage drop. This would degrade (increase) the circuit's minimum working voltage.

When determining which values for R7 to R9 will be able to withstand mains overload, remember that D3 effectively half-wave rectifies the mains waveform. Therefore, even though the peak voltage at R7 will equal $1.414 \times V_{RMS}$, the RMS voltage at this point will only be $V_{RMS}/2$. For example, if V_{RMS} is 240 V, each resistor will see just 40 V_{RMS}. So selecting values of 3.6k will dissipate 0.44 W in each resistor. The resulting power dissipation in the 11-V zener would be 0.12 W.

With the circuit subjected to mains overload, the op amp's output briefly rises toward V_{DD} on each positive cycle. It then settles down to the proper, lower value required to regulate the current sink. Ordinarily, this phenomenon would result in a large RMS voltage across R11, leading to an excessive LED current and excessive power dissipation in Q2. Fortunately, this problem is easily remedied by connecting Q3 across R11 as shown. Q3 normally has no effect on the current sink. But under mains overload conditions, Q3 keeps Q2's rms collector current below 2 mA. In doing so it ensures that the power dissipation is well within the ZTX458's 1-W limit.

The trip voltage, V_T, is given by:

$$V_T = V_{REF}(R1+R2)/R2 \text{ (volts)}$$

so:

$$R1 = R2(V_T - V_{REF})/V_{REF} \text{ (ohms)}.$$

R1 and R2 should be as large as possible to minimize the current drawn from V_{IN} and the power dissipation under overloads. The voltage ratings of R1, R2, and R3 must be able to withstand the maximum overvoltage at V_{IN}.

A prototype circuit was built with R1 = 300k and R2 = 100k, equivalent to a nominal V_T of 4.80 V. With V_{IN} = 4.70 V (circuit untripped), the total current draw was just 20.6 µA. The circuit tripped when V_{IN} exceeded 4.78 V. In the tripped state, the circuit's minimum working voltage (below which the LED current began to fall under 1 mA) was found to be V_{IN} = 2.94 V.

The LTC1541 could be replaced by the pin-compatible MAX951, if required. Note, however, that the MAX951's maximum working voltage is only 7 V (9 V absolute maximum), requiring a lower zener voltage for D4.

If narrow transients on V_{IN} cause nuisance tripping, a capacitor across SW1 will provide some immunity, but at the expense of response time.

Create A D/A Output Using Two Pins On A PIC Micro

Jim Walker

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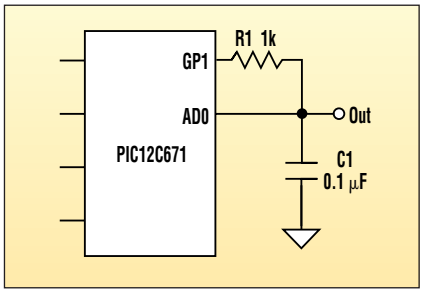
CIRCLE 520

With the addition of only a resistor and a capacitor, the low-cost eight-pin PIC12C671 can be used to provide an 8-bit digital-to-analog output *(Fig. 1)*. Of course, this topology will work with almost any microprocessor that has an internal analog-to-digital (A/D) peripheral.

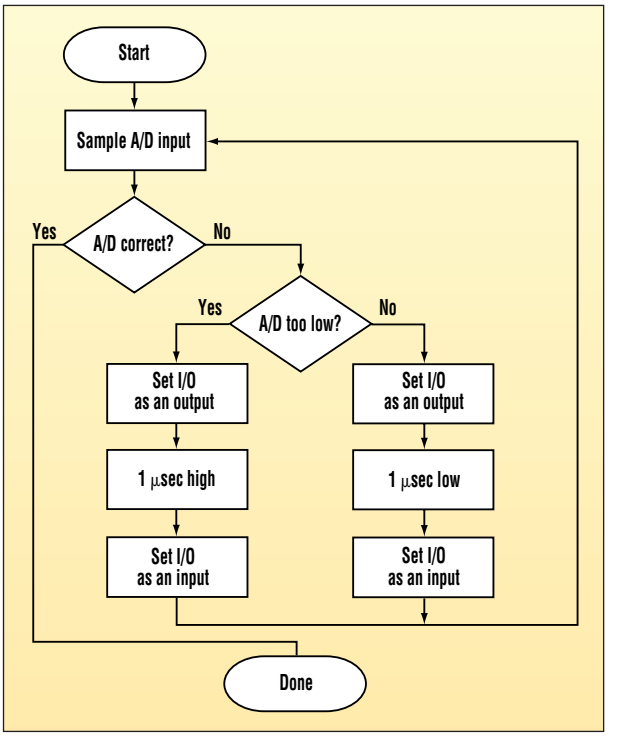
Following a simple concept, one of the microcontroller's A/D inputs monitors the voltage across an external capacitor (C1). Next, one of the digital I/O port pins pulls the voltage up or down (through R1) until it reaches the required value. When the digital I/O isn't being used to set the voltage on C1, it serves as a high-impedance input.



1. By taking advantage of the microcontroller's internal analog-to-digital (A/D) peripheral, an 8-bit digital-to-analog (D/A) output can be implemented with the addition of only a resistor and a capacitor.

The flow diagram regulates the voltage across C1 at a rate of about 1 LSB per microsecond *(Fig. 2)*. Therefore, C1 can be shifted (up or down) quickly enough to settle even a near-rail-to-rail output adjustment in about 20 ms. More clever algorithms, which match the pulse-adjustment time with the error, will obviously allow much faster convergence.

To view a sample code listing for the PIC12-C671, go to *www.PlanetEE.com* and click on "Ideas for Design."



2. This simple algorithm can adjust the voltage across C1 at a rate of about 1 LSB per microsecond, allowing completion of a near-rail-to-rail output swing in about 20 ms.

Ultra-Small Inductorless Regulator Drives White LED Backlights

David Kim

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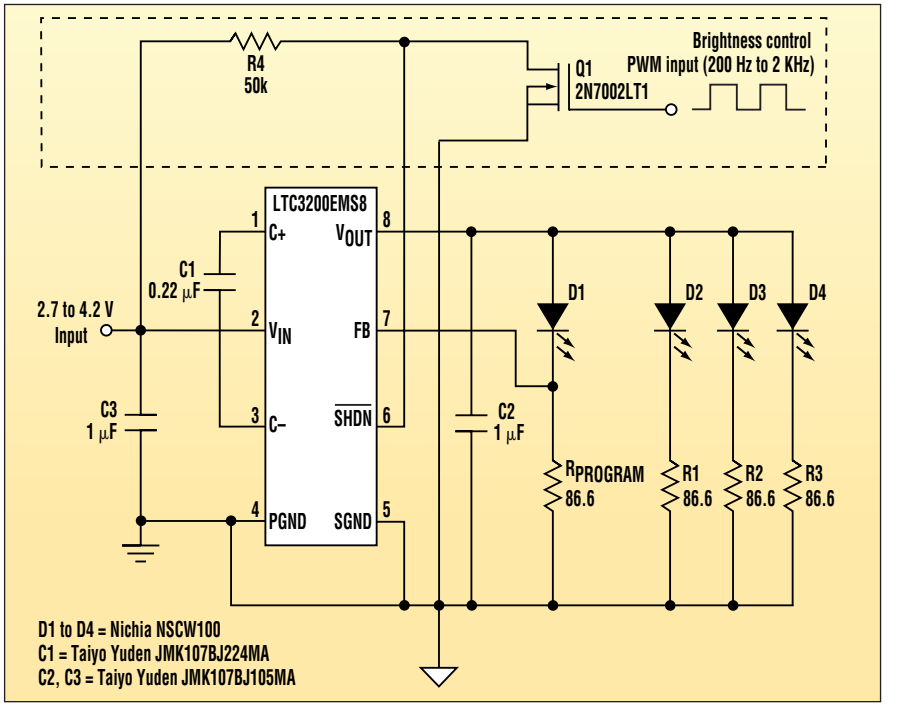
CIRCLE 521

High-intensity white LEDs are ideal for backlighting of small, color LCD displays used in handheld devices such as cellular phones and PDAs. When compared to other backlight solutions, white LEDs provide higher reliability and lower power consumption.

But portable devices powered by a single Li-ion cell require a step-up voltage conversion to drive white LEDs over the entire voltage range of the Li-ion cell (2.7 to 4.2 V). This is because the forward voltage drop of a typical white LED is 3.6 to 4 V. Shown here is a constant-current backlight supply using the LTC3200 inductorless regulator to drive four white LEDs.

The LTC3200's inductorless architecture and 2-MHz switching frequency result in a small circuit size—less than 1.1 mm in height and 28 mm^2 in area. The constant-current source illustrated in the figure accurately controls the LED current regardless of variations in the forward voltage drop of the LEDs. This results in constant light output from different white LEDs.



With this inductorless step-up circuit, constant-current output control drives white LEDs regardless of the magnitude or variations in their forward-voltage characteristics.

The LED current is programmed via the $R_{PROGRAM}$ resistor. Using the feedback voltage of the LTC3200 ($V_{FEEDBACK}$ = 1.4 V), the LED current is regulated according to the formula:

$$I_{LED} = V_{FEEDBACK}/R_{PROGRAM}$$

In this circuit, an 86.6-Ω resistor is used to set the LED current at 16 mA. To maintain the same current in each LED, the paralleled LEDs also are ballasted with 86.6-Ω resistors.

The brightness of the LEDs can be adjusted by changing the duty cycle of the PWM signal at the external MOSFET connected to the shutdown pin. A lower duty cycle will result in lower brightness, whereas a higher duty cycle will result in higher brightness. For the best results, a PWM signal in the range of 200 Hz to 1 kHz should be used.

Single-Cell Flashlight Uses Any Type Of LED

Al Dutcher

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CIRCLE 522

With this circuit, any type of LED can be driven from a single-cell supply in the range of 1.0 to 1.5 V *(see the figure)*. As a result, it can be used with alkaline, carbon-zinc, NiCd, or NiMH cells. The device was designed for use in LED flashlights. But here it serves as an astronomer's flashlight, operating in its red mode to prevent interference with night vision. Substituting white LEDs would create a good general-purpose flashlight.

This circuit may be used with LEDs from infrared (1.2 V) to blue/white (3.5 V). It tolerates LED voltage turn-on requirements and delivers relatively constant power. Some compensation for battery voltage also is included.

The best way to describe this circuit is as an open-loop, discontinuous, flyback, switch-mode boost converter. Q2 is the main switch. When conducting, it charges L2 with the energy to be delivered to the LED. When Q2 is turned off, the energy stored in L2 is dumped into the LED during the flyback cycle.

Q1, an inverting amplifier, drives Q2, an inverting switch. Feedback around the circuit is provided by R4, R5, and R2. Two inversions around the loop create a noninverting regenerative arrangement. If L2 were replaced with a resistance, the circuit would be bistable as in the classic flip-flop. As it prevents dc feedback, L2 allows ac feedback only. Therefore, the circuit is astable and will oscillate. Q2's on-time is determined by the time it takes L2's current to ramp up to the point where Q2 can no longer stay in saturation. When Q2 turns off, the circuit flips to the off state for the duration of the energy dump into the LED. Then, the process is repeated.

Since the inductor stores current flow, it essentially acts as a current source for the duration of the stored energy dump. Inductors will attain any voltage necessary to maintain their stored current flow. This property allows the circuit to be very compliant with the LED voltage requirement. Constant voltage devices (LEDs) are happiest when driven by current sources. The LED is actually being pulsed at a rapid rate.

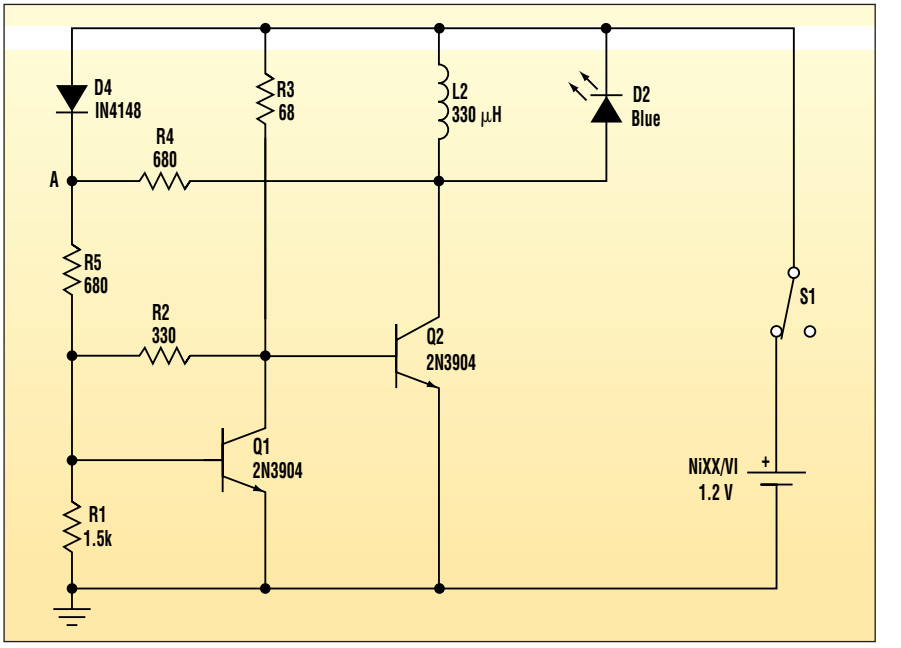
In this example, the inductor size is relatively unimportant as it only determines the oscillation frequency. If the inductor is too large (unlikely), the LED will flash too slowly and appear to flicker. If it's too small, switching losses will predominate and efficiency will suffer. Using the value shown causes the circuit to oscillate at about 50 kHz—not a bad compromise.

Diode D4 supplies compensation for varying cell voltage. Because of the voltage division at node A, D4 includes a variable-clipping operation. As the supply increases, the clipping level is raised and the feedback is decreased. Q1 inverts this clipping level so it can reduce the turn-on bias to Q2 at higher cell voltages.

Although the devices chosen here are 2N3904s, any small npns will do. Q2 runs at rather high currents at the end of the charging ramp. L2 also needs to handle this peak current without saturating. Internal resistance causes Q2's base-voltage requirement to rise. The R2/R1 divider at Q1's base raises its collector voltage to match that requirement, thereby controlling Q2's final current.

The LED drive current is a triangular pulse with about a 120-mA peak, averaging about 30 mA for a red LED and 15 mA for a white one. This gives a flashlight a nice brightness without unduly beating up the LED. The supply current is approximately 40 mA. A 1600-mA-hr NiMH AA cell will last approximately 40 hours.

In total, this circuit costs less than a white LED. It's possible to use higher-current devices and larger cells to run multiple LEDs. Such LEDs would be placed in series. If the LEDs are in parallel, sharing resistors should be used. Though uncontrolled, the circuit's output also can be rectified and filtered to offer a convenient dc supply for any number of uses. The amplified, noninverting feedback to Q1's base could provide regulation.



This LED flashlight circuit can drive any type of LED from a single-cell battery. In this application, the circuit operates over a battery voltage range of 1.0 to 1.5 V.

Low-Cost VHF Inductors Use Nylon Toroids

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Toroidal inductors can be used in passive-filter and equalizer circuits in the VHF range. Although SAW filters have taken over many bandpass filter applications, LC low-pass and high-pass filters are still viable.

When inductance values are smaller than 1 µH, air cores with unity relative permeability can be used instead of powdered-iron or ferrite cores. For magnet-wire sizes thinner than number 20 AWG, a coil form is often needed for mechanical support. Nylon 6/6 standard flat washers are usable as low-cost coil forms. The nominal electrical parameters of this material are a dielectric constant of 3.6, a dissipation factor of 0.04, and a dielectric strength of 385 V/mil.

TABLE 1: NYLON WASHER DIMENSIONS

Screw clearance	Outer diameter	Inner diameter	Thickness
Number 4	0.250 in.	0.115 in.	0.125 in.
Number 10	0.375 in.	0.194 in.	0.125 in.

Two different-sized nylon washers were used in fabricating these toroidal inductors *(see Table 1)*. Some typical toroidal inductors were then wound and tested as illustrated in Table 2. The maximum inductances shown were obtained with the windings squeezed, and minimum inductances were obtained with the windings spread. Inductance values were calculated from measured resonant frequencies using a known capacitor. As the winding area is filled, the adjustability of toroidal inductors decreases. The nylon toroids have limitations on the number of turns that can be applied as a single-layer winding *(see Table 3)*.

TABLE 2: INDUCTANCE WINDINGS AND MEASURED VALUES

Toroid diameter	Inductor winding	Maximum inductance	Minimum inductance
0.250 in.	7 turns-No. 26	116 nH	86 nH
0.375 in.	7 turns-No. 22	113 nH	86 nH

Despite its dielectric constant and dissipation factor, the quality of nylon toroidal inductors is quite good. Typical inductor unloaded Q's are in the 75 to 125 range. Inductor unloaded Q's of 50 are very adequate for most low-pass and high-pass filters. Surface-mount inductors with unloaded Q's of only 10 to 20 can still be used in many of these filters. Nylon toroidal inductors are primarily suitable for small-signal applications.

TABLE 3: TOROIDAL INDUCTOR MAXIMUM WINDINGS

Toroid diameter	Maximum turns (22 AWG)	Minimum turns (26 AWG)
0.250 in.	6	15
0.375 in.	15	30

Low-cost VHF inductors can be realized using readily available standard nylon washers as coil forms. These inductors can provide small size, some adjustability, and efficient unloaded Q's. When operating between 30 and 100 MHz, they are very useful for prototypes and small-quantity runs. For large-volume production, surface-mount inductors or integrated circuits, at the subsystem and system levels, would typically be preferred.

Program Converts Real Sequences To Cosine Series

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CIRCLE 524

This program converts a sampled real sequence stored in a disk file to a harmonically related set of cosine waveforms *(see the listing on www.PlanetEE.com by following the Ideas For Design link)*. The cosine series can be used for waveform approximation, circuit design and analysis, simulation, and waveform synthesis.

First, the program downloads N samples of the waveform from disk and copies the data to the signal[n] array. Then, the discrete Fourier transform (DFT) is applied to the real sequence in signal[n]. The resulting N complex-amplitude spectral components X(k) are stored in the spectrum[k] array. Real and image frequencies (k), which have conjugate-symmetry for real sequences, make up the spectrum X(k). If N is even, the program eliminates the last sample, forcing an odd value of N. This ensures complete conjugate pairs of real/image frequencies.

As shown in the following, the inverse DFT applied to the spectrum X(k) has the form of a cosine series.

$$signal(n) = \frac{X(0)}{N} + \frac{2}{N}\sum_{k=1}^{\frac{N-1}{2}} |X(k)|\cos\left(2\pi\frac{kn}{N} + \theta(k)\right)$$

for n: 0 to N – 1
N: odd - valued

(1)

where $\theta(k) = \tan^{-1}(\text{imX}(k)/\text{reX}(k))$ radians.

From the Nyquist sampling criterion,

$$\frac{k}{N} = \frac{F}{Fs} < \frac{1}{2} \quad (2)$$

where F = actual frequency (Hz) and F_S = sampling frequency (Hz).

The coefficients of the series are stored in an array of coefficient structures [k] as demonstrated below:

$$\text{term(k).ampl} = \frac{2}{N}|X(k)| \text{ volts} \quad (3)$$

$$\text{term(k).omega} = 2\pi\frac{k}{N} \text{ radians / sample} \quad (4)$$

$$\text{term(k).phase} = \theta(k) \text{ radians} \quad (5)$$

COSINE COEFFICIENTS VERSUS INDEX K

Frequency index (kΩ)	Amplitude (volts)	Omega (rad/sample)	Phase (radians)
0	2.512	0.000	0.000
1	4.519	0.031	–0.773
2	3.183	0.063	–1.547
3	1.483	0.094	–2.320
4	0.025	0.126	0.047

These coefficients are listed in tabular form. To test the program, a single pulse is used. Next, the function get_real-data( ) in function main( ) is disabled and these statements are added:

```
int i;
for (i=0; i < 50; i++) signal(i) = 10.0;
for (i=50; i < 250; i++) signal(i) = 0.0;
```

After this, the program is recompiled and run, generating a 10-V input pulse that's 50 samples wide. At the prompt, the number of real data points is entered as 200. The program then displays the calculated cosine coefficients versus index k *(see the table)*.

Low-Cost, 24-V Industrial Controller Is ESD-Protected

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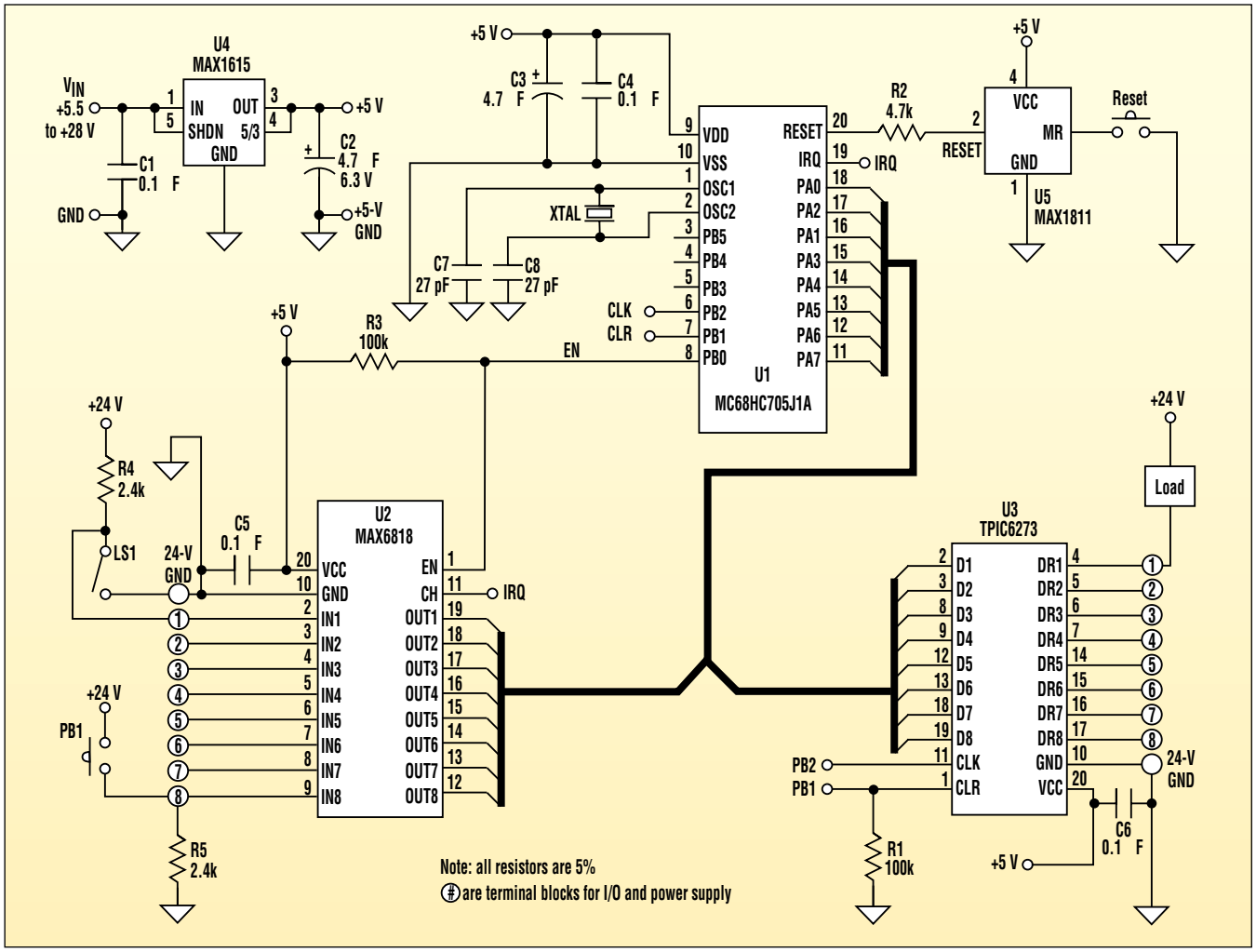
CIRCLE 520

To validate a new process before its full-scale deployment, developers first test it in a small-scale pilot plant. Although controlling this plant with programmable logic controllers (PLCs) would allow maximum flexibility, PLCs are too large and expensive for such temporary use. In most cases, the alternative is hard-wired relay logic. But such an approach makes modifications difficult and time consuming. (For safety reasons, modern pilot and process plants employ 24-V and 12-V dc control logic rather than 120-V ac logic.)

This circuit incorporates PLC programmability with the low cost of relay control *(see the figure)*. These features are combined with a software program to form a robust 24-V industrial controller that offers low cost, full surface-mount construction, low power, and ESD protection (to view the listing, visit *www.PlanetEE.com*, and click on the "Ideas For Design" icon).

With an 8-bit microcontroller used to provide the program control, the circuit's eight debounced and ESD-protected inputs can accept voltages up to 24 V dc. The eight open-drain outputs can handle up to 45 V dc and



This low-cost, programmable industrial controller is an attractive alternative to larger, more expensive PLC controls.

sink up to 250 mA (or 1.5 A of pulsed current). A 24-V, low-power linear regulator drives the circuit, while a voltage monitor with a manual reset guards against power brownouts.

CMOS switch debouncer U2 ensures robust industrial-rated inputs and a wide input-voltage range. It offers eight fully debounced and ESD-protected inputs, eight tristate outputs, and a change-of-state output ($\overline{CH}$) for simplifying connections to the microcontroller. Pull-up resistor R3 provides a logic high that disables U1 and U2 during power-up until the microcontroller I/O has been configured.

An octal D-type latch (U3) supplies eight open-drain outputs, rated to 45 V dc. These outputs can easily drive process indicator lamps, isolation relays, and other logic controls in a 24-V control system. A built-in voltage clamp on each output enables direct connection of relays, solenoids, buzzers, and other inductive loads. Resistor R1 ensures that all outputs are off during power-up until the microcontroller I/O has been configured.

Microcontroller U1 includes 32 bytes of RAM for variables and 1232 bytes of EPROM for storing the process control program. (A low-cost, one-time-programmable version is also available.) The bidirectional pins of port A (PA0 to PA7) furnish an 8-bit data bus for I/O data to U2 and U3. Using software, the first three pins of bidirectional port B (PB0 through PB2) are configured as outputs. As a result, they can provide the control signals $\overline{EN}$, $\overline{CLR}$, and CLK for U2 and U3.

By issuing a logic-low reset during power-up, the U5 voltage monitor ensures automatic recovery during power brownouts. U5 also offers a debounced manual reset to U1 when the reset pushbutton is pressed. R2 prevents contention with the microcontroller's bidirectional $\overline{RESET}$ pin.

Power to the controllers is provided by U4, a high-voltage, low-power linear regulator configured to deliver up to 30 mA from a 5-V output. U4 accepts input voltages to 28 V dc. Therefore, it lets the controller function with 12/24-V control systems and mixed-voltage control systems (i.e., 24-V field devices and 12-V control logic).

Since every U2 input pin (IN1 to IN8) has an internal, 63k pull-up resistor, each one requires an applied logic low to indicate a change of state. Input "8" shows a pushbutton-switch interface where R5 limits the 24-V-to-ground current to 10 mA. This enables the use of low-cost switch contacts and a logic-high level (24 V) as the change-of-state signal. Input "1" demonstrates a limit-switch interface in which R4 limits the current to 10 mA and a logic low (0 V) is the change-of-state signal. U3's output "1" illustrates a lamp, solenoid, or other load connected to a 24-V source.

The timer function internal to the microcontroller can replace expensive relay timers in the control system. Additional inputs are easily gained by adding another switch-debouncer IC, installing a pull-down resistor on the microcontroller's $\overline{IRQ}$ pin, and adding steering diodes between each $\overline{CH}$ pin and U1's $\overline{IRQ}$ pin. One of U1's unused port-B pins can be configured as the $\overline{EN}$ signal to the new IC. For analog functions, a serial digital-to-analog converter (DAC) or analog-to-digital converter (ADC) and the microcontroller's unused port-B pins (PB3 to PB5) can be used to implement 0- to 10-V or 4-to-20-mA process controls.

"Take-Back-Half" HVAC Thermostat Is Precise And Energy-Efficient

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CIRCLE 521

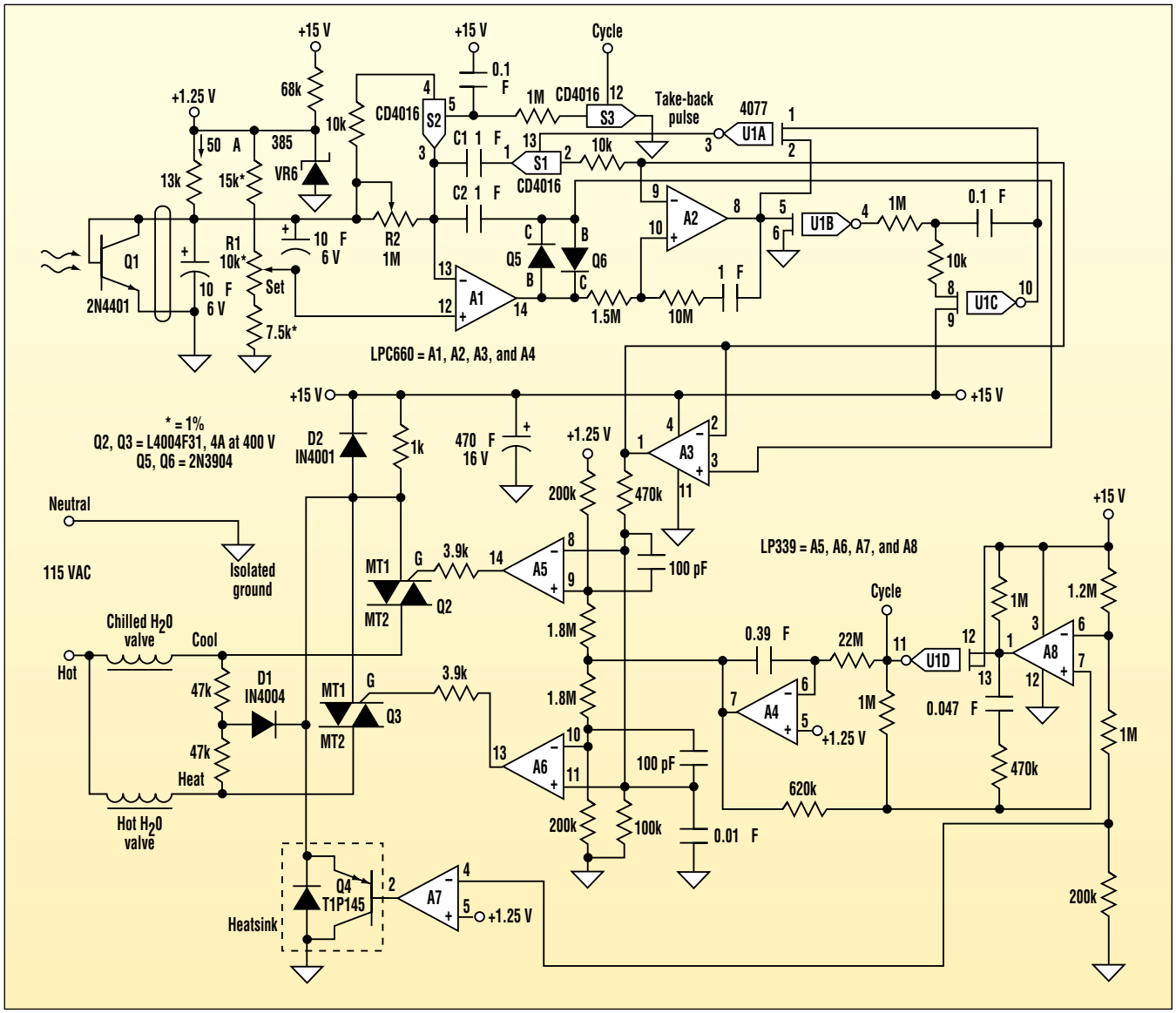
Implementing tight control of environmental temperature is essential in many critical areas. For instance, it's necessary when research laboratories house sensitive instrumentation and for manufacturing facilities involved in high-precision microphotolithography. However, the conventional ways to achieve such control can run directly afoul of responsible energy conservation practices.

In one commonly used technique, for example, the refrigeration side of the air-handling system is allowed to run continuously at full throttle. Meanwhile, the addition of opposing heat is used to close the temperature feedback loop. This energy-intensive arrangement is a popular ploy considering how difficult it is to achieve accurate temperature control in systems that are capable of switching freely between heating and cooling modes.

In such systems, errors arise from the unavoidable time delays and shifts in feedback parameters that occur whenever the direction of heat flow is reversed. Undesirably complex and hard-to-tune feedback algorithms would typically be required to cope with these parametric shifts. Consequently, the energy cost of the simpler heat-only feedback method, although regrettable, is often perceived as the lesser of the two evils.

Fortunately, there's an unconventional control algorithm that offers a suitably robust yet simple-to-tune alternative that largely avoids both difficulties *(see "Take Back Half: A Novel Integrating Temperature-Control Algorithm,"* ELECTRONIC DESIGN, *Dec. 4, 2000; "Circuit Enables Precision Control In Radiant Heating Systems,"* ELECTRONIC DESIGN, *Jan. 8, 2001; and "Linear-RMS Phase Control Improves Thyristor-Based Thermostat,"* ELECTRONIC DESIGN, *March 5, 2001)*. As illustrated in the figure, TBH makes accurate environmental temperature control (<< ±1°C) possible. Plus, it's optimized with a single tuning variable and avoids the undesirable energy consumption of a traditional variable-heat-only approach.

Circuit operation centers around the diode-connected temperature sensor Q1. Temperature-dependent V_{Q1} (about –2 mV/°C) is compared to the setpoint voltage developed by R1. The difference is then integrated by A1. Next, the integrated error is scaled by the adjustable R2-C2 time constant, buffered by A3, and applied to the A4-



This TBH-based thermostat provides accurate and efficient environmental temperature control (<<±1°C), optimized with a single tuning variable.

A6 dual-PWM circuit. Circuit topology is such that when $V_{R2} > V_{Q1}$ (ambient temperature is greater than the setpoint), A1 ramps positive. As a result, comparator A5 triggers TRIAC Q2 for proportionally greater duty cycles. This action progressively opens the chilled-water solenoid valve, thereby cooling the ambient temperature and forcing it toward the setpoint.

Conversely, when $V_{R2} < V_{Q1}$ (ambient temperature is less than the setpoint), the error voltage ramps negative. As a result, A6 and Q3 cause the hot-water valve to admit increasing amounts of hot water into the air-handling system, thereby warming the ambient. Bias voltages developed by the passive summing network surrounding A5 and A6 prevent the overlap of hot/cold valve operation, promoting efficient energy use.

The 70-second period of the timing ramp generated by the A4-U1D-A8 oscillator was chosen to be appropriate for both ripple-free ambient temperature control and acceptable mechanical valve life (typical valve-life expectancies of 2×10^6 actuation cycles imply a valve MTBF greater than four years). By tuning the feedback-loop time constant (TBH "F" factor), the A2, S1, U1A, U1B, U1C logic chain implements the crucial convergence-by-bisection principle of the TBH algorithm. By adjusting R2, this time constant can be set to accommodate a particular HVAC heat exchanger and air handling system. S2 and S3 act to accelerate initial settling of the circuit on power turn-on.

The prototype of the TBH thermostat has been in service for over eight years. During this time, it has maintained a stable and accuracy-enhancing environment in a nuclear magnetic resonance (NMR) facility of several thousand square feet.

ideas wanted

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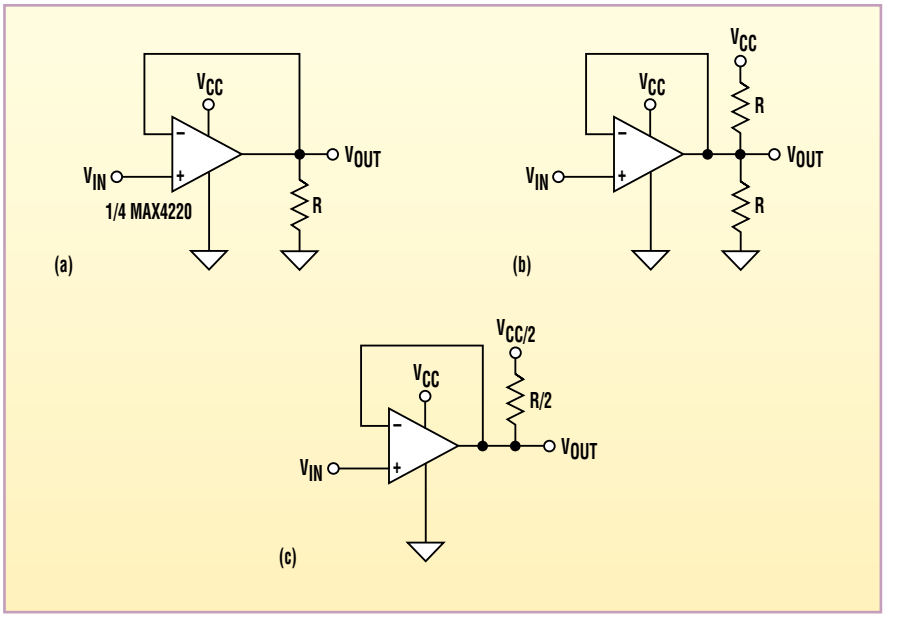
One Resistor Takes The Heat From Single-Supply Op Amps

Elliott Simons
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086

CIRCLE 520

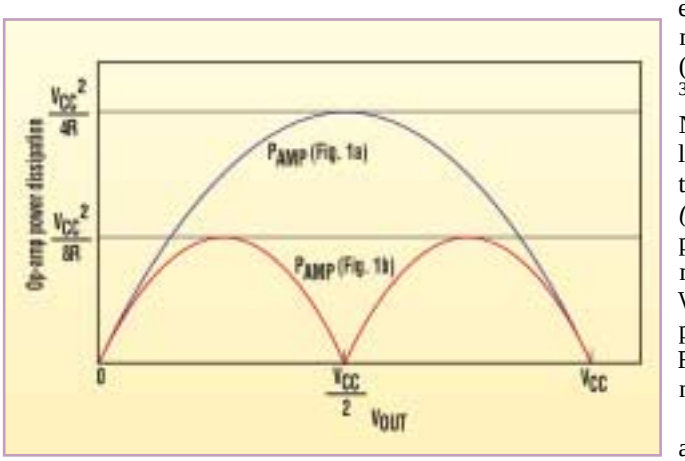


1. The power dissipated in a single-supply op amp biased at mid-V_{CC} (a) is reduced by adding a load-value pull-up to V_{CC} (b). A Thevenin-equivalent circuit aids analysis (c).

To maximize signal swing, the output of a single-supply op amp is usually biased at half the supply voltage *(Fig. 1a)*. For ground-referenced loads, however, this configuration can result in maximum power dissipation in the IC.

A simple and effective solution is realized by connecting a pull-up resistor, with a value equal to the load resistor, between the output and the positive supply voltage *(Fig. 1b)*. Use of this type of resistor enables the op amp to operate at higher ambient temperatures and drive lower-resistance loads. As a result, the op amp is limited only by its maximum ratings for output voltage and current, rather than by package power dissipation.

For example, consider the MAX4220 quad op amp, in which each output drives a 30-Ω resistor to ground. If V_{CC} = 5 V, the device would exceed its package power rating. But remember that since the pull-ups are connected, each op amp's output current is zero. So connecting 30-Ω pull-ups at each output minimizes the IC's power dissipation. Power is now dissipated in the pull-up resistors and not in the op amps.



2. The maximum power dissipation, occurring at the quiescent point, of the op amp in Figure 1a is twice that of the op amp in Figure 1b.

Calculating power dissipation for the op amp in Figure 1a is straightforward:

$$P_{DC} = \frac{(V_{CC} - V_{OUT})V_{OUT}}{R}$$

Solving the differential equation $dP_{DC}/dV_{OUT} = 0$ for V_{OUT} shows that the op amp's maximum power dissipation ($V_{CC}^2/4R$) is reached when $V_{OUT} = V_{CC}/2$. The corresponding power calculation for the circuit in Figure 1b, which uses a pull-up resistor, is simpler when the load circuit is converted to its Thevenin equivalent *(Fig. 1c)*:

$$P_{DC} = \frac{(V_{CC} - V_{OUT})\left(V_{OUT} - \frac{1}{2}V_{CC}\right)}{\frac{1}{2}R}$$

$$\left(\text{for } V_{OUT} \geq \tfrac{1}{2}V_{CC}\right), \text{ and}$$

$$P_{DC} = \frac{V_{OUT}\left(\frac{1}{2}V_{CC} - V_{OUT}\right)}{\frac{1}{2}R}$$

$$\left(\text{for } V_{OUT} \leq \tfrac{1}{2}V_{CC}\right)$$

Solving $dP_{DC}/dV_{OUT} = 0$ for these two equations shows that the maximum power dissipation ($V_{CC}^2/8R$) occurs for $V_{OUT} = {}^3/_4V_{CC}$ and for $V_{OUT} = {}^1/_4V_{CC}$. Note that this maximum power level would be twice as much if there were no pull-up resistor *(Fig. 2)*. The amplifier with no pull-up resistor delivers maximum output current at the $V_{CC}/2$-quiescent point. With a pull-up resistor like the one in Figure 1b, the op amp delivers no output current at all!

Similar power advantages accrue for ac applications. Consider a sinusoidal signal superimposed on a dc level of $V_{CC}/2$:

$$V_{OUT} - \tfrac{1}{2}V_{CC} + V_P \sin \omega t$$

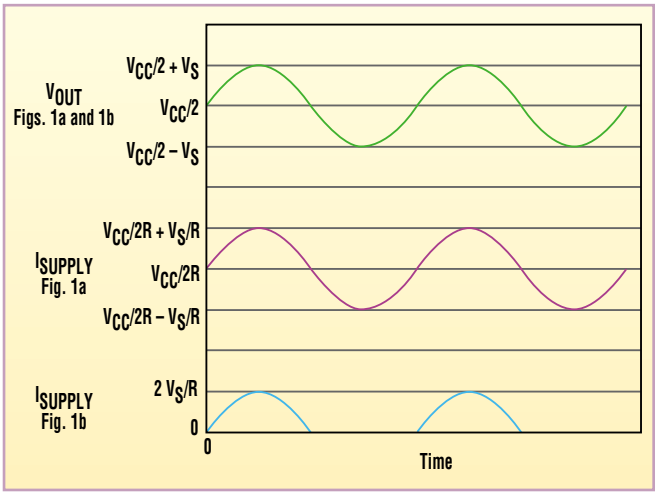
where V_p is the peak value of the sinusoidal signal.

Figure 3 illustrates the resulting waveforms. To calculate power dissipation in the op amp, a power-balance equation is employed in which the supply power equals the sum of the power dissipated in the load and in the op amp. In turn, the op-amp dissipation equals the supply power minus the load power.

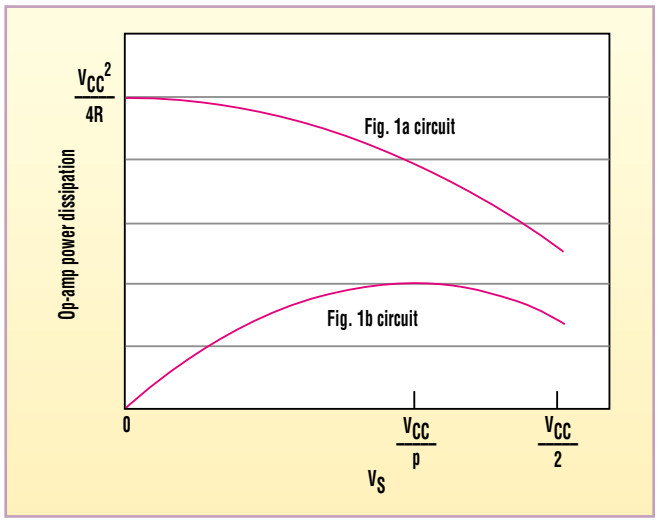
In the case of Figure 1a, supply power equals the average supply current ($V_{CC}/2R$) times V_{CC} (i.e., $V_{CC}^2/2R$). The power in the load is $(1/R)(^1/_2V_{CC})^2 + (1/R)(V_p/2^{1/2})^2$, which is the sum of the dc and ac components. Therefore, the supply power minus the load power for the Figure 1a circuit is $P_{AC} = (V_{CC}^2/4R) - (V_p^2/2R)$, as shown in Figure 4.

For the circuit in Figure 1b, the supply power equals the average supply current $2V_p/\pi R$ multiplied by V_{CC}. This is demonstrated in Figure 3 (i.e., $2V_pV_{CC}/\pi R$). Power in the load is $2(V_p/2^{1/2})^2/R$. The supply power minus the load power is $P_{AC} = (2V_{CC}V_p/\pi R) - (V_p^2/R)$ *(Fig. 4, again)*. By solving the equation $dP_{AC}/dV_p = 0$ for V_p, it's clear that the op amp in Figure 1b achieves its maximum power dissipation when $V_p = V_{CC}/\pi$.

Although overall circuit power isn't reduced, this technique is useful for decreasing the power dissipation within an op amp. Doing so keeps the device within its power limitations.



3. These waveforms illustrate the op-amp voltage and current relationships for the circuits shown in Figures 1a and 1b.



4. The power dissipation in the op amp of Figure 1a is always significantly greater than the dissipation in the op amp of Figure 1b.

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READER SERVICE 130

Surge Devices Protect Subscriber-Line Interface Circuits

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CIRCLE 521

A subscriber-line interface circuit card (SLIC) supplies the interface between the analog loop of the telecommunication network and a digital central office (CO). It does so by providing what's commonly referred to as the BORSCHT functions:

B—battery feed
O—overvoltage protection
R—ringing
S—signaling
C—coding (analog-to-digital conversion and digital-to-analog conversion)
H—hybrid (two- to four-wire conversion)
T—test

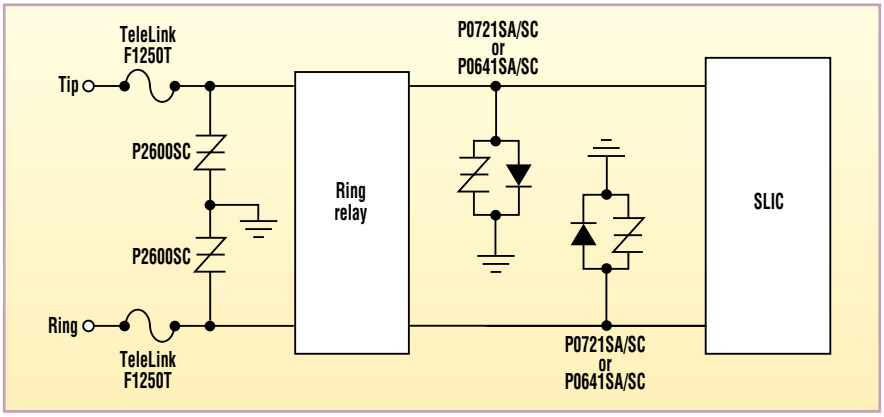
Network hazards such as lightning and power-line-cross conditions can pose a serious threat to line cards deployed at central offices, remote switching locations, and customer premises. To minimize the danger, both overvoltage and overcurrent protection are required. These features guarantee reliable line-card operation and provide regulatory compliance.

SLIC line cards should be protected against overvoltages that can exceed:

- 2500 V and overcurrents up to 500 A for central office and remote switching locations
- 1500 V and 200 A for customer premises applications, and
- 800 V/100 A for intrabuilding requirements.

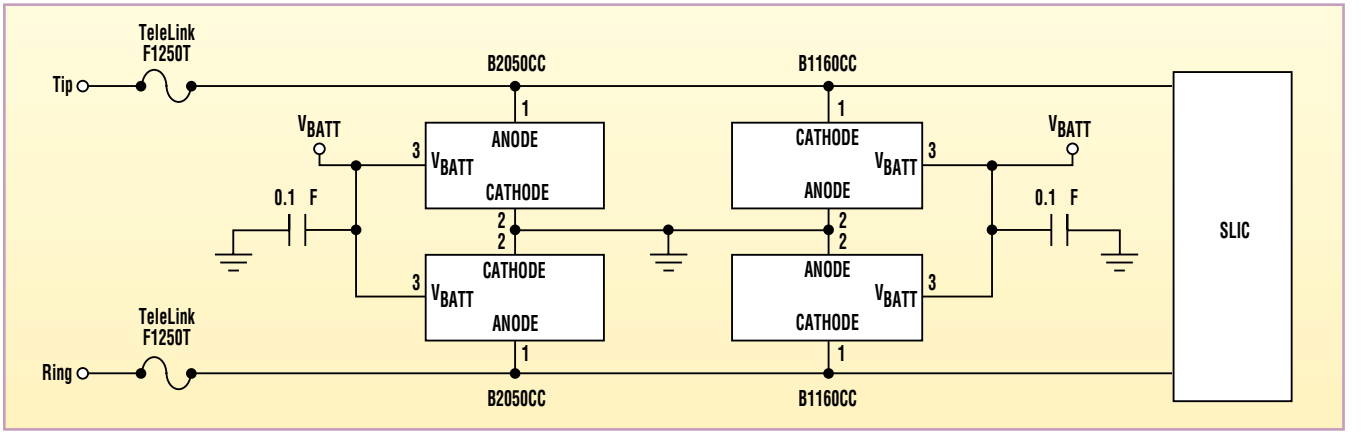
Many different environments benefit from SLIC cards. Among them are typical CO-to-customer-premises connections, private branch exchange (PBX), remote terminal (RT), and digital loop carrier (DLC) systems. As seen here, each of these applications has very unique requirements:

- Some SLIC applications may use a fixed voltage supply such as –24, –48, –72, or –90 V.
- Other SLIC applications may need to be flexible enough to use any of these supply voltages.
- Some applications will require two different power supplies, one negative and one positive. In this case, the ring signal can be driven to a positive and negative threshold, which extends the SLIC's transmission capability.
- Some SLICs use a ring relay to add ringing signals to the line, while other SLICs have the ringing function inte-



1. The SLIC application shown requires overvoltage protection for both the on-hook condition and the off-hook condition to provide reliable operation and meet FCC compliance criteria.

READER SERVICE 131



2. A SLIC chip with integrated ringing requires both positive (B2050CC) and negative (B1160CC) surge protection. If no positive battery supply is used, the B2050 devices are replaced by two diodes, which will short all positive events to ground.

grated within the SLIC chip.

Each configuration's surge protection device has a peak-pulse current (I_{pp}) rating able to withstand the lightning immunity regulatory requirements without the use of an additional series resistance. Likewise, the fuse is chosen with an amps^{2}time (I^2t) rating large enough to withstand the appropriate lightning immunity tests. Yet it's small enough to open safely during severe power-cross conditions.

This SLIC application requires overvoltage protection for both the on-hook condition and the off-hook condition *(Fig. 1)*. The two P2600SC SIDACtor devices furnish the ring-relay protection for the on-hook condition. Their standoff voltage parameter is high enough to pass the FCC Part 68.306 leakage-current requirements. Either the P0721SA/SC or the P0641SA/SC SIDACtor devices supply the off-hook condition protection. If the battery supply is higher than 75 V, then the P0901 and/or the P1101 may be used here instead. The integrated diode in these off-hook-mode protection devices eliminates the need for external discrete diodes (which offer protection from voltage levels exceeding ground potential).

Overcurrent protection also is needed for this application. The two TeleLink fuses provide overcurrent protection that doesn't operate during surge conditions. Although this prevents nuisance openings during lightning-induced surge events, it also furnishes the required power-cross protection.

Shown here are a negative Battrax (B1160CC) and a positive Battrax (B2050CC) surge protector *(Fig. 2)*. Once the positive Battrax is referenced to the positive power supply, it shunts all surge events exceeding the positive supply voltage. The B1160 Battrax device shunts all surge events exceeding the negative supply voltage. If no positive battery supply is used, then the two B2050 devices are replaced with two diodes. These diodes provide the positive surge protection by shorting all positive events to ground.

The two TeleLink fuses provide overcurrent protection for the circuit.

Counter Demodulates Narrowband FSK Without Synchronization

A. Navarro and M. Rostami

CIRCLE 520

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Frequency shift keying (FSK) is a popular digital modulation technique for data transmission. Some common applications of FSK modulation include both wired and wireless data transmission as well as infrared remote controls for consumer electronic equipment.

FSK demodulation can be either coherent or noncoherent. Coherent detection always demands carrier and bit synchronization, typically achieved using phase-locked loops (PLLs). PLLs are very noise-sensitive and normally call for a trimming adjustment inside the loop filter.

FSK noncoherent demodulation can be implemented with two bandpass filters and two envelope detectors. Bit synchronization may be required as well. In narrowband FSK transmission systems, bandpass filters must have a very high quality factor, making implementation more complex.

This idea presents a noncoherent, narrowband FSK receiver that eliminates the drawbacks mentioned above. Figure 1 shows the FSK demodulation circuitry in which neither PLLs nor high-quality-factor bandpass filters are used. With this high-frequency (HF) demodulation circuit, no trimming adjustments are necessary.

L1, L2, C4, and C7 form two resonant circuits, implementing an input filter whose passband is centered at 10 MHz. A differential high-frequency amplifier amplifies the 10-MHz signal. IC1 and IC2 combine to make an automatic gain-control (AGC) circuit. The amplified signal is then converted into a digital waveform by a wideband comparator, IC3. The resulting digital signal clocks a 4-bit counter (IC4). Oscillator IC5 clears the counter. IC6A, the D-type flip-flop, latches the counter's most significant bit at the rising edge of the oscillator signal OSC_OUT. Since the oscillator circuit generates a 50% digital waveform duty cycle and the two FSK frequencies are:

$f1 = 9.83 \times 10^6$ Hz (bit "0")
$f2 = 10 \times 10^6$ Hz (bit "1")

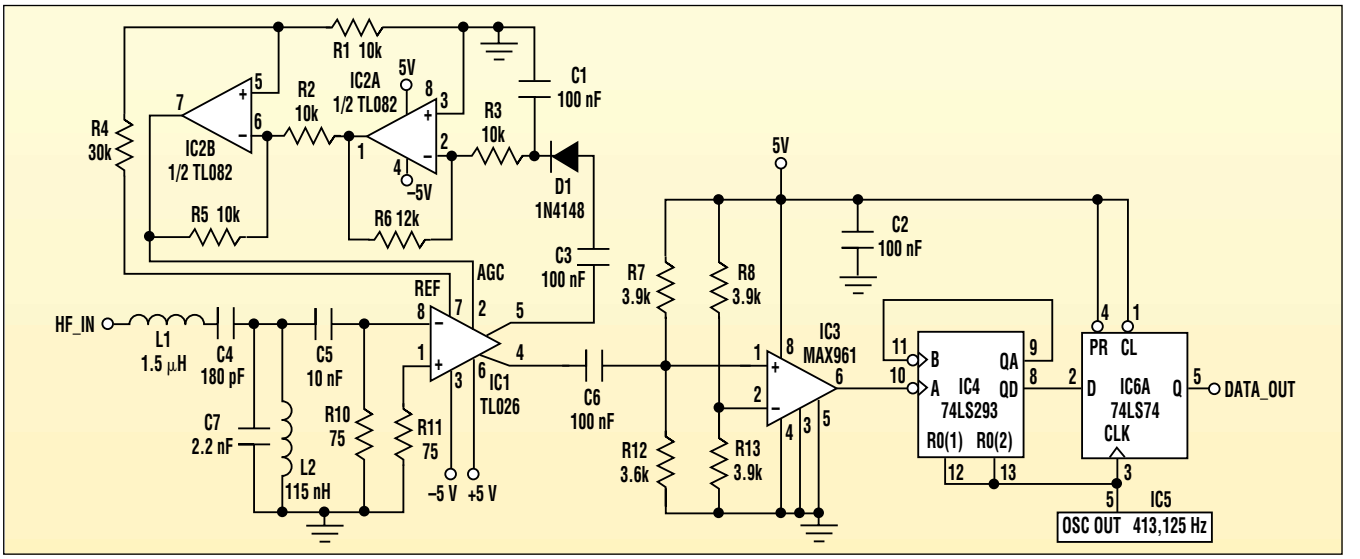
the desired oscillator frequency for IC5 is calculated as:

$$OSC\_OUT = \frac{\frac{f2 + f1}{2}}{\frac{2(2^n + 2^{n-1})}{2}}$$

$$= 413{,}125\ Hz$$

The calculated OSC_OUT frequency also can be divided or multiplied by a power of two. Counter IC4 counts only during the low period of the oscillation cycle. To clear the counter, the OSC_OUT signal's remaining high period is used. IC5 can be implemented using a crystal oscillator module, a TLC555 in an astable configuration, or an oscillator circuit powered by a quartz crystal and a 74HCT02 IC.

Resistors R10 and R11 should have values equal to the HF_IN source impedance. For instance, if this FSK receiver is connected to a 50-Ω cable, then R10 and R11 should be 50-Ω resistors. This selection will provide maximum power transfer. Once diode



This noncoherent, narrowband FSK receiver doesn't employ any PLLs, high-quality-factor bandpass filters, or trimming adjustments.

D1 rectifies amplifier IC1's output voltage, the resulting dc voltage is amplified and inverted by IC2A.

Differential amplifier IC2B inverts IC2A's output voltage, producing a positive AGC voltage signal. IC2B also adds the REF voltage, which is scaled by resistors R1 and R4. The differential voltage amplification is then equal to $40 + 25(V_{REF} - V_{AGC})$, with $V_{REF} = 1.4$ V. IC3 receives the AGC-system output signal and converts it into a TTL-compatible signal to drive the IC4 clock.

To provide the negative supply voltage required by the AGC system, a MAX660 is used to generate a –5-V supply voltage from the 5-V single-supply voltage.

1-kV Piezo Amplifier Keeps Cost, Noise Low

Marco Pisani

Institute of Metrology, Torino, Italy

Piezoceramic (PZT), or "piezo," actuators are known to be excellent position transducers in the nanometer or micrometer range. These actuators are widely used in many precision applications. PZTs, which come in different shapes (tubes, disks, and plates), are cost effective and easy to use. Just glue them to the parts you want to move (mirrors, fibers), connect the wires to the amplifier, and go.

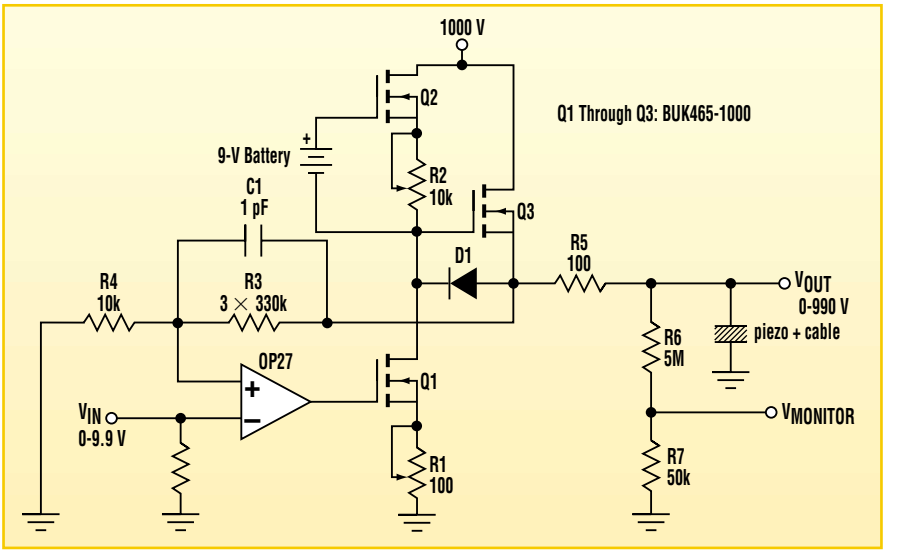
The "big" problem with PZT ceramics is that the maximum elongation (typically 0.1% of their size) is obtained with electrical fields on the order of 20 kV/cm. For common-size transducers, this can lead to full-scale operating voltages close to 1 kV, requiring expensive high-voltage amplifiers. Manufacturers partially solve this problem by building piezo "stacks," a pile of small piezoceramic pieces mechanically connected "in series" and electrically connected in parallel. These stacks have operating voltages one order of magnitude lower. The stacks are expensive, however, and are not as stiff as a single piece of ceramic. In practical applications, additional mechanics like steel parallelograms must be added.

The low-cost amplifier presented in Figure 1 permits the use of "high-voltage" piezos with excellent results. It is based on three high-voltage MOSFETs and a low-noise op amp. To understand how the amplifier works, consider that the piezo behaves more or less like a capacitor, having typical values of tens of nanofarads. Therefore, when driving the piezo with large voltage steps, the piezo needs high currents to charge and discharge itself.

Assume for a moment that Q3 is not present and D1 is a short. Q1, driven directly by the op-amp output, acts with R1 as a voltage-controlled current-sink. Together, Q2 with R2 and the 9-V battery act as a fixed current-source that pulls up the drain of Q1. Note that Q2's gate drains no current from the battery which can, therefore, last for years. (Caution: this battery is at the same high voltage as the output!)

When the amplifier needs to discharge the piezo, the output of the op amp goes up and Q1 sinks a current limited only by the set value of R1. When the amplifier needs to charge the piezo, the charge rate is fixed at the value of the current source Q2-R2.

Since this value is also the quiescent current of the amplifier, this quiescent current must be low (1 mA = 1 W) to "cool" the device at 1 kV. This limits the positive slope slew rate. For a 10-nF piezo, the slew rate is 0.1 V/μs for a 1-mA quiescent current.



1. Rather than using piezo "stacks," this low-cost 1-kV amplifier produces excellent results using less expensive "high-voltage" piezos, which are physically superior and easier to use.

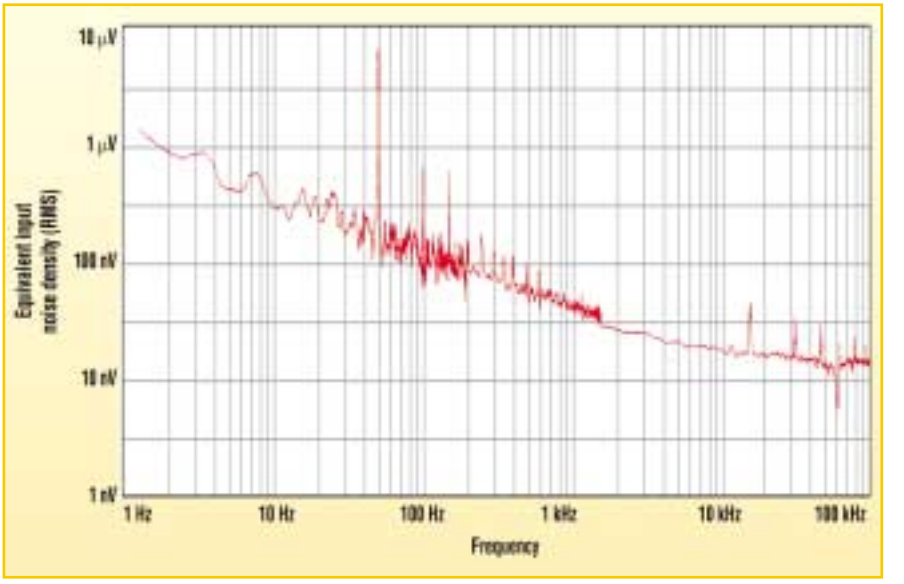
Q3 serves as a current buffer that isolates the capacitance of the load when charging it, enabling higher slew rates at low quiescent currents. Diode D1 provides a path for the discharge current through Q1.

R3 and R4 set a positive gain of 100. Note that R3 and C1 must support a 1-kV voltage drop. A series of three 0.5-W, 330-kΩ resistors is effective. R5 isolates the capacitive load, improving the stability. The voltage divider R6-R7 provides a monitor signal that is 1/100th of the output (always advisable when high voltage is present).

The measured slew rate with a 26-nF piezo-tube load is 10 V/µs for a 1.5-mA quiescent current and 20 V/µs for a 3.5-mA quiescent current. The up/down slew rates can be set independently by trimming R2 and R1, respectively.

The output-noise spectral density of the amplifier is shown in Figure 2. At high frequencies, it is limited by the Johnson noise of the feedback network (chosen to be as low as 10 kΩ). The 50-Hz ripple is within 5 mV p-p (5 ppm) and can be reduced by further filtering the power supply.

The HV power supply is also quite simple. While a transformer with a 710-V secondary is used, the diode bridge is made with eight 1N4007s. The filter capacitor is made with a series of four 470-µF 250-V capacitors, each one paralleled with a 330-kΩ resistor to provide a discharge path when the HV supply is switched off.



2. The equivalent input noise density of the amplifier versus frequency is shown.

READER SERVICE 142

Tiny Programmable Oscillator Operates From 5 kHz To 20 MHz

Jerry Wasinger

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CIRCLE 522

By merging a digital potentiometer with an oscillator chip, a very small programmable oscillator (1 µMAX and one SOT-23 package) can be realized. In addition to consuming very little board space, the circuit requires only three signals from a microprocessor for control *(see Fig. 1)*.

The MAX5160 from Maxim is a 200-kΩ digital potentiometer with 32 taps. To move up to the next tap, set the UP/DOWN input high and pulse the increment input low. To move down, set the UP/DOWN low before pulsing the increment input.

The LTC1799 is a programmable oscillator from Linear Technology. The frequency of oscillation is inversely proportional to the value of the resistor between V+ and the SET pin. The chip contains an internal divider, which is controlled by the DIV pin. The relationship between the divide ratio and the input on DIV is given in the table.

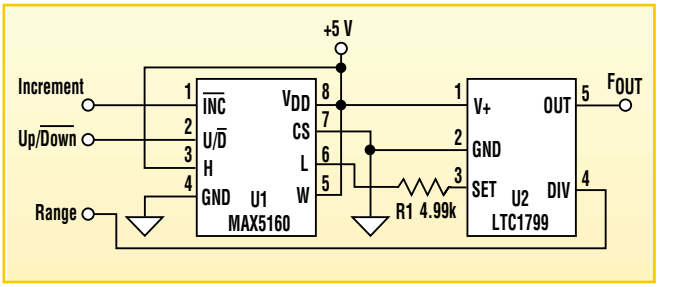
The equation for the oscillator frequency is:

$$F_{OSC} = 10\text{MHz}\left(\frac{10000}{NR_{SET}}\right)$$

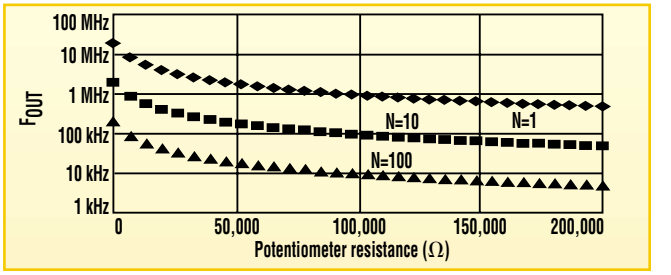
Where N is the divider value shown in the table.

A plot of this equation for each value of N versus each of the tap locations on the digital potentiometer can be seen in Figure 2. Note that there is some overlap between the curves for each value of N.

To satisfy the minimum R_{SET} requirements for the LTC1799, resistor R1 was added in series with the digital potentiometer. The circuit can be further simplified by setting the DIV input to a fixed value, which restricts operation to a narrower output range.



1. This tiny programmable oscillator (one µMAX and one SOT-23 package) needs only three signals from a microprocessor for control.



2. The output frequency for each divider value versus each tap location on the digital potentiometer is shown.

DIVIDER VALUES

DIV input	Internal divider value (N)
Ground	1
High impedance	10
V+	100

ideas wanted

Address your Ideas for Design submissions to: Ideas for Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604 or e-mail to: mjames@penton.com.

16-Bit PWM Optoisolated DAC Is PC-Controlled

W. Stephen Woodward

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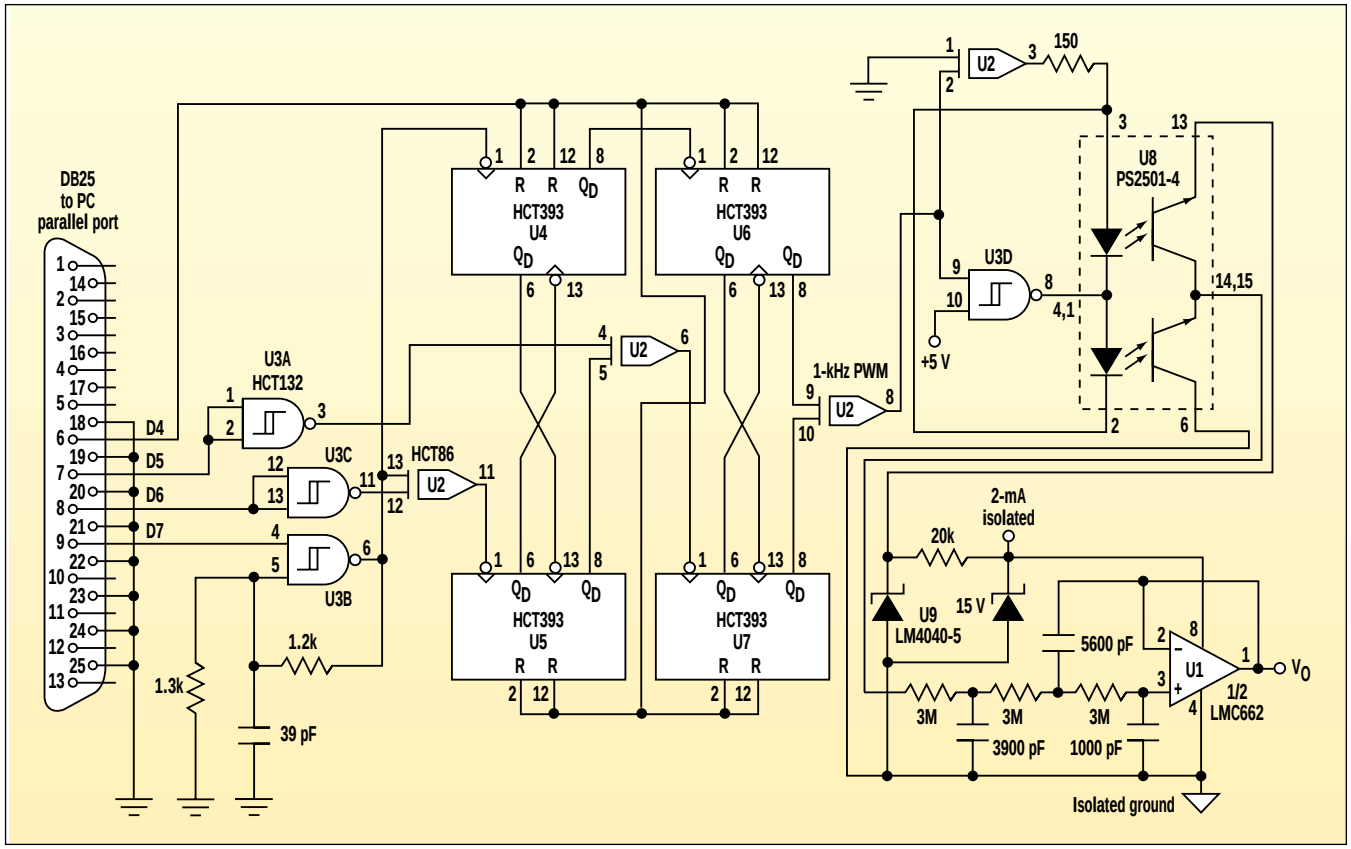
There was a time when an "honest" (e.g., DNL < 1/2 LSB) 16-bit digital-to-analog converter (DAC) was an expensive, premium component. Nowadays they're almost jellybeans—almost. Some applications, however, can still benefit from multichip 16-bit DAC solutions. The circuit presented here *(see the figure)* was designed to serve one of these applications. It features a virtually perfect DNL, which is an inherent characteristic of PWM conversion. It also includes an optoisolated output and an interface to the ubiquitous PC's parallel (printer) port.

A general description of DAC circuit operation is as follows: control of the 16-bit PWM conversion waveform comes from the relative phase of the 500-Hz square-wave outputs of two 16-bit ripple-carry counters (comprising U4, 5, 6, and 7) free-running from a common 30-MHz RC clock (U3B). The phase is determined by the initial values loaded into the counters before the clock is enabled and the states of PC port bits D5 and D6. Depending on this phase, the duty cycle of the output of exclusive-OR U2C can be varied linearly from 0% to 100% in increments of 0.0015% ($1/2^{16}$). The PWM waveform is then split into two complementary drive signals and applied to the anti-parallel LEDs and inverted (i.e., $V_{CE} < 0$) phototransistors of optoisolator U8.

The operation of the U8 phototransistors in inverted mode reduces their on-state saturation voltage to the sub-mV range. Thus, the dc component of the isolated square wave is accurately (to 13-bit precision) equal to the product of the PWM duty cycle and the U9 voltage reference. The dc component is extracted by the three-pole, 14-Hz, uni-



Criss-crossed ripple counters equalize the carry propagation delays of the four 'HCT393s to eliminate unacceptable zero-offset in the PWM waveform.

ty-gain, low-pass filter (U1). The sub-pA bias current of U1 limits the error term arising from the net 9-MΩ filter resistance to negligible levels. Also, the good CMR of U1 preserves better than 14-bit integral nonlinearity (INL). While the output ripple of the filter is at the sub-16-bit level, its 16-bit settling time is approximately 0.1 s.

A closer look at the circuit reveals such details as the criss-crossed connection of ripple counters U4-U7. The purpose of this curious topology is to equalize the carry propagation delays of the four 'HCT393s. Together these delays, of the order of 20 ns/bit, represent more than 10 DAC LSB-bits. If left uncompensated, the manufacturing tolerances in the counter chips could result in an unacceptable (up to several LSB-bits) zero-offset in the PWM waveform. Adding the cross-connects allows each '393 to contribute equally to both counters. It distributes the propagation delay of the four chips equally over the two 16-bit counting chains, thus cancelling this error source.

Downloading a DAC setting from the PC to the PWM DAC involves a three-step process. First, the D7 bit is cleared to disable the clock. D4 is set to clear all the counter bits. Then, D4 is cleared and D5 and D6 are toggled the requisite number of times to enter the desired output value into the MSB byte (D5) and LSB byte (D6) of the conversion value. The somewhat large number (up to 256) of interface operations required to enter the conversion value using this "unary" serial means is outweighed by the simplification it affords in the conversion logic. The ability to use non-presettable counter chips was quite convenient. The actual time required for download of a new conversion is, in any case, much faster than the settling time of the U1 filter.

Following the download of the conversion value, bit D7 is set to enable the clock. Then, the continuous generation of the PWM waveform commences. An example of suitable code for keyboard input and downloading of DAC settings is presented in the MSBasic listing. This code listing is located at *www.PlanetEE.com* (click on the Ideas for Design icon).

Window Comparator Enhances Integrator Circuit's Flexibility

Jim Mahoney

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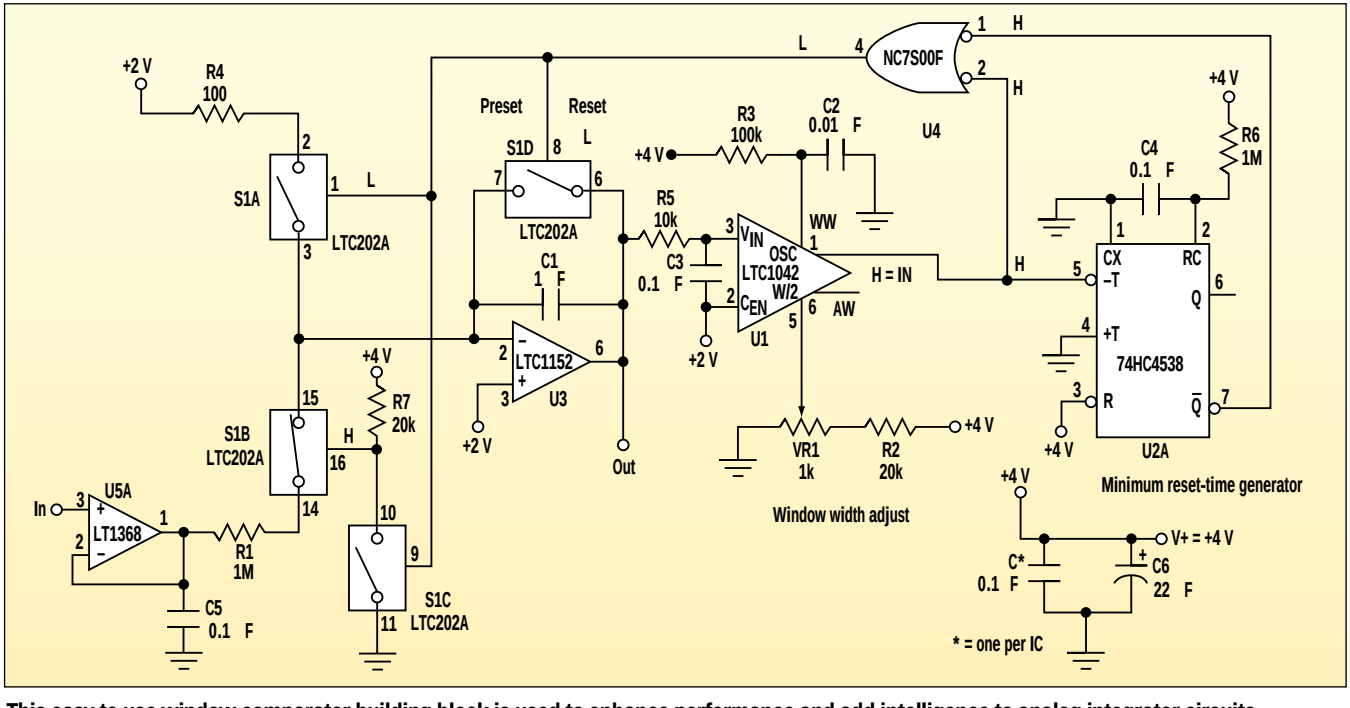
A simple to use window comparator can make short work of integrator, antiwindup, and reset circuits. Control systems that incorporate an integrator stage need some form of integrator reset or antiwindup function. An integrator drifts with time and is subject to saturation when driven by large error signals. This saturation effect causes the device's output information to become invalid and out of phase with the commanded system response. In this circuit, an LT1042 window comparator is used to detect and initiate integrator reset as required *(see the figure)*.

Integrator design starts with determining the accuracy necessary for the



This easy to use window comparator building block is used to enhance performance and add intelligence to analog integrator circuits.

selected integration time interval. Once the required accuracy is known, the components needed to meet it can be selected. The op amp and integrating capacitor are critical. For example, the µA741's 80-nA input bias current is enough to reach 1% error in 0.25 seconds. But an LTC1152, with its 100-pA input bias current, will reach the 1% error level in 200 seconds.

In order of preference, the integrating capacitor should be polystyrene, Teflon, or polypropylene. Even the best op amp and integrating capacitor won't do much good if proper attention isn't paid to pc-board layout and cleanliness. For longer integration times and/or lower error rates, temperature-compensated input-bias-current compensation should be used.

Once the integrator core is created, the need for integrator reset or integrator antiwindup is evaluated. Then the circuit is designed and tested.

As shown in the figure, window comparator U1 monitors the low-pass-filtered (via R5 and C3) integrator output signal from U3, pin 6. The low-pass filter reduces comparator trips due to noise. R3 and C2 determine U1's sample rate. (R3 must be between 100 kΩ and 10 MΩ.) The voltage at pin 5 of U1 sets the window width symmetrically around the center voltage set at pin 2. U1 compares the integrator's output to the center and window-width parameters. Its output ("within window"), at pin 1, goes low when the input value exceeds these parameters.

When U1's pin 1 goes low, it drives U4's pin 2 low. As a result, the integrator is reset for as long as its output is outside of the set window limits. Pin 5 of U2A also is driven low, triggering one-shot U2A. The one-shot output (pin 7) drives U4's pin 1 low for a set period of time [equal to $0.7 \times (R3 \times C2)$]. Doing so ensures a minimum reset time. To reset the integrator, the output of U4's pin 4 controls sections S1A, S1C, and S1B of the LTC202A. While section S1C is used as an inverter, section S1B disconnects the input as the integrator is being reset.

This easy to use window-comparator building block enhances performance and adds intelligence to analog integrator circuits by way of its decision-based action. A flexible, decision-based analog-computer element, the comparator is used to achieve integrator reset. It does this by executing one important but simple task—comparing its input to a reference value and outputting a decision based on the input information.

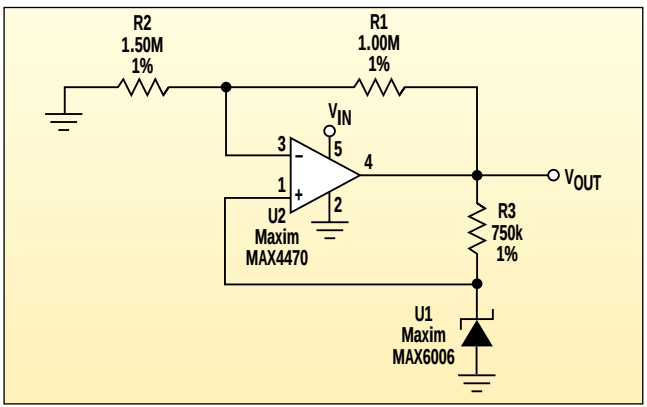
Low-Voltage Series Reference Draws Only 2.4 μA

Steve Lee and John Guy

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086

For systems with miniscule power budgets, implementing a low-power voltage reference involves many compromises. One design option is the low-voltage shunt reference. Available since the birth of the bandgap cell, this device traditionally operates with less current than a series reference. The shunt reference offers flexibility in its bias and application. Yet it can sink or source only modest currents. Using a series reference can provide improved sink/source capability, but this choice would incur the penalty of a tenfold increase in supply current.

This circuit combines the low power consumption of a shunt reference with series-reference performance *(see the figure)*. As a result, it yields an ultra-low-power series reference with excellent line and load regulation. At the heart of this circuit is a 1-μA, 1.25-V shunt reference (U1). Bias current for this shunt reference comes directly from the amplified reference voltage, virtually eliminating line-regulation error. Because the op amp (U2) supplies the load current, load regulation is greatly improved compared to designs using resistively biased bandgap references.



A shunt reference (U1) in this series-reference circuit yields a composite circuit that provides the low power consumption of a shunt reference with the line-load regulation of a series reference.

A low supply current is the most important attribute of this op-amp/shunt-reference configuration. The total supply current for U1 and U2 is 2.4 μA, including the current in the feedback network. While this network sets the output to 2.0 V, it can easily be adjusted for other voltages.

The circuit sinks and sources current quite well. Line regulation is 90 dB from V_{IN} = 2.2 V to 5.5 V. Load regulation (with V_{IN} = 2.5 V) is 1 μV per 10 μA of output current. The total supply current is 2.4 μA, independent of the supply voltage. This performance greatly exceeds that of existing series references, whose minimum supply currents are 10 μA and above.

ideas wanted

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Transformer Improves High-Pass Filter Performance

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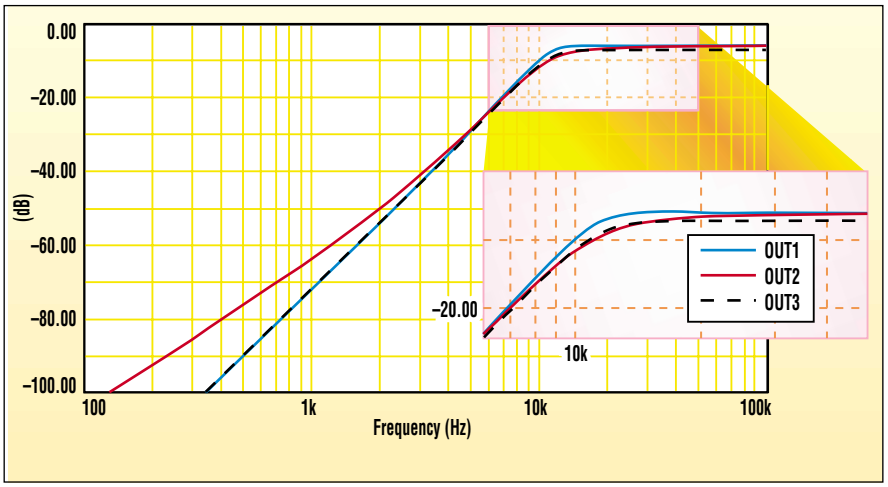
The low-frequency LC performance of a high-pass filter is strongly affected by the quality of the filter components. Typically, the inductor is the component that deviates most significantly from the ideal.

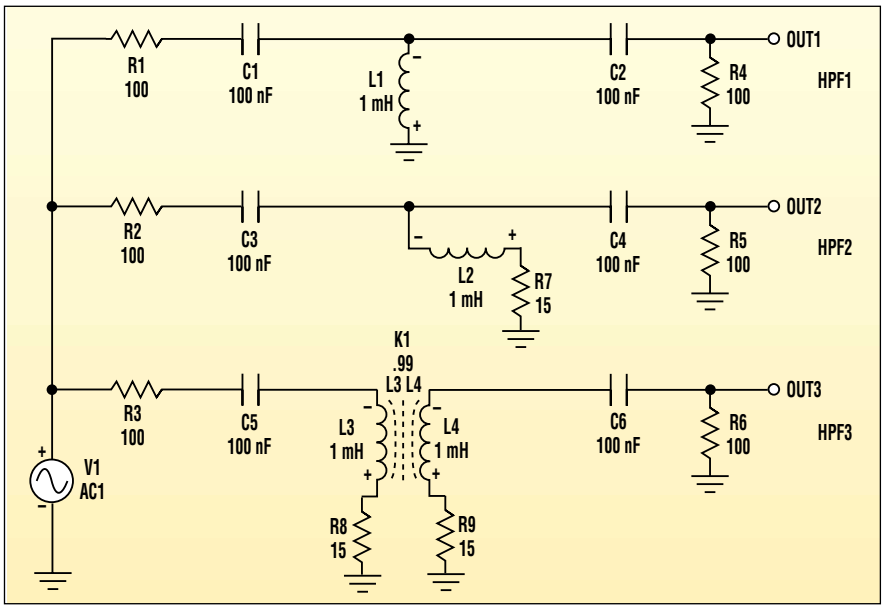
The first-order inductor paradigm consists of an inductor in series with a resistor that models the ohmic resistance of the inductor's wire. Low-frequency inductors can have a high value of loss resistance.

HPF1 in the circuit diagram shows an ideal third-order high-pass filter with an ideal inductor *(Fig. 1)*. HPF2 depicts the same filter with a non-ideal inductor. The 15-Ω inductor loss-resistance is the equivalent of Q = 4 at the HPF cutoff frequency of 10 kHz.

Examining the frequency response in Fig. 2, the HPF2 output OUT2 deviates from the HPF1 ideal-filter curve (OUT1) as the frequency gets lower.



2. The frequency response of the HPF3 filter is observed to be closest to the ideal filter.



1. HPF1 is an ideal third-order high-pass filter with an ideal inductor. While HPF2 is the same filter with a non-ideal inductor, HPF3 replaces the inductor with a transformer.

The attenuation slope changes from 18 dB/octave (third-order) to 12 dB/octave (second-order).

This situation seems to be unavoidable due to the inductor's loss component. However, the use of a transformer instead of an inductor alters the situation dramatically. As in HPF3, the loss resistance is not in a branch that is common to the input and output. Therefore, it does not affect the ultimate attenuation at low frequencies.

Examination of the frequency response of the HPF3 filter's OUT3 shows that this value is identical to the ideal filter's output at low frequencies. The deviation from ideal of HPF3's frequency response is a small added loss at the passband for frequencies above the cutoff frequency. This loss is due to the resistor's voltage dividers at the input and output of the filter. In many cases, the source and load resistance values can be adjusted to compensate for this loss. In any case, the curve shape remains close to the ideal shape.

Eight-Wire Resistive-Touchscreen Controller Has I²C Interface

Antonio Cebrián and José Millet

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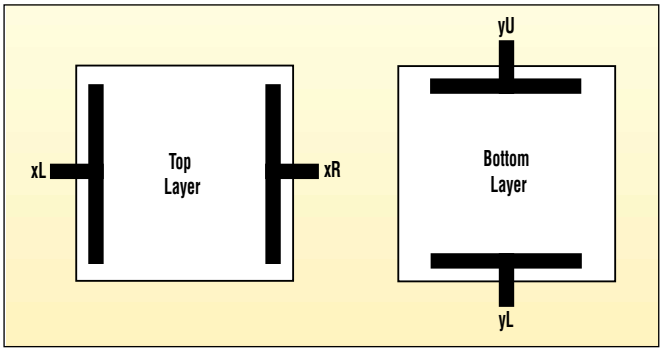
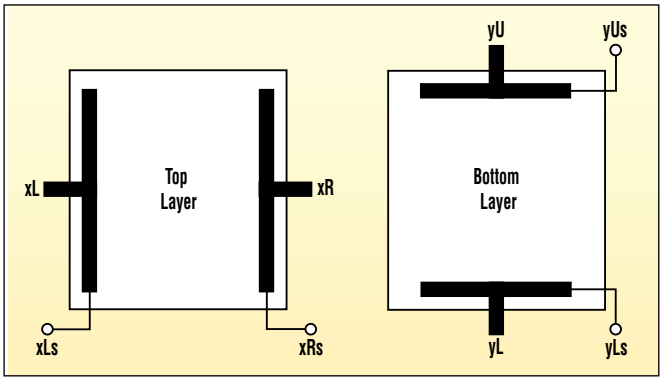


1. The four-wire touchscreen is decoded by placing a voltage across the top layer and reading the horizontal touch location on the bottom layer. The process is then reversed and a vertical touch location voltage is read from the top layer.



2. An eight-wire resistive touchscreen is similar to the four-wire version. It has four additional sense lines to improve accuracy and counter environmental effects.

An analog, resistive touchscreen is a sensor consisting of two opposing layers, each coated with a transparent resistive material. The layers are separated by small spacer dots of nonconductive polyester that prevent the two layers from making contact. Touching the top surface compresses the flexible top layer towards the supported bottom layer. This causes electrical contact of the two layers between the span of insulating dots.

Determining a touch location requires two measurements: one to determine the X coordinate and one to determine the Y coordinate. For a single axis measurement, a drive voltage is applied across one layer. Once applied, the voltage linearly changes from the minimum drive voltage at one end to the maximum drive voltage at the other end. The opposing layer is used to measure the voltage at the point of contact. This process is repeated, alternating the functions of the two layers to obtain a measurement on the opposing axis.

The four-wire touchscreen *(Fig. 1)* is decoded by developing a voltage across the vertical layer's resistive material (top layer) and reading the horizontal touch location voltage on the opposing layer (bottom layer). A voltage is then placed across the horizontal layer's resistive material (bottom layer), and a vertical touch location voltage is read from the opposing layer (top layer).

For four-wire decoding:

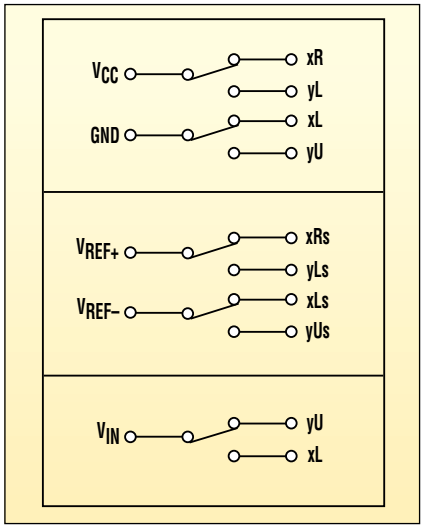
1) Apply V_{CC} to xR, GND to xL, leave yL and yU unconnected.

2) Read yU voltage.

3) Apply V_{CC} to yL, GND to yU, leave xR and xL unconnected.

4) Read xL voltage.

The four-wire touchscreen analog-to-digital converter (ADC) output is:



3. When multiplexing sense lines for an eight-wire touchscreen, the sense lines are individually multiplexed to the inputs of the microcontroller's five-channel ADC.

$$n = \frac{N(V_{IN} - V_{REF-})}{(V_{REF+} - V_{REF-})}$$

where:

n = ADC output count

$N = 2^{BITS}$

V_{REF+} = positive voltage reference

V_{REF-} = negative voltage reference

V_{IN} = ADC input voltage

In general, $V_{REF+} = V_{CC}$. The simplified four-wire touchscreen ADC output is then:

$$n = NV_{IN} / V_{CC}$$

An eight-wire resistive touchscreen is similar to the four-wire version. It has four additional sense lines to improve accuracy and counter environmental effects *(Fig. 2)*. These lines are individually multiplexed to the references of the ADC *(Fig. 3)*.

The decoding steps for the eight-wire touchscreen are:

1) Apply V_{CC} to xR; GND to xL; leave yL, yLs, yU, and yUs unconnected; connect xRs to V_{REF+} and xLs to V_{REF-}.

2) Read yU voltage.

3) Apply V_{CC} to yL; GND to yU; leave xR, xRs, xL, and xLs unconnected; connect yLs to V_{REF+} and yUs to V_{REF-}.

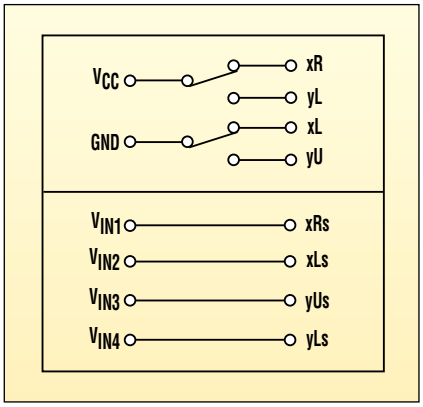
4) Read xL voltage.

The eight-wire touch screen ADC output is:

$$n = \frac{N(V_{IN} - V_{REF-})}{(V_{REF+} - V_{REF-})}$$

where:
n = ADC output count
$N = 2^{BITS}$
V_{REF+} = positive voltage reference
V_{REF-} = negative voltage reference
V_{IN} = ADC input voltage

It is possible to avoid multiplexing the sense lines if a four-channel ADC is available *(Fig. 4)*.



4. Designers can eliminate the need for multiplexing of the sense lines if a four-channel ADC is available in the system.

The eight-wire touchscreen nonmultiplexing decoding steps are:
1) Apply V_{CC} to xR; GND to xL; leave xRs, xLs, yLs, yU, and yUs unconnected.
2) Read yU, xRs, and xLs voltages.
3) Apply V_{CC} to yL; GND to yU; leave yLs, yUs, xR, xRs, xL, and xLs unconnected.
4) Read xL, yLs, and yUs voltages.

The eight-wire touchscreen nonmultiplexing-sense-lines ADC output is:

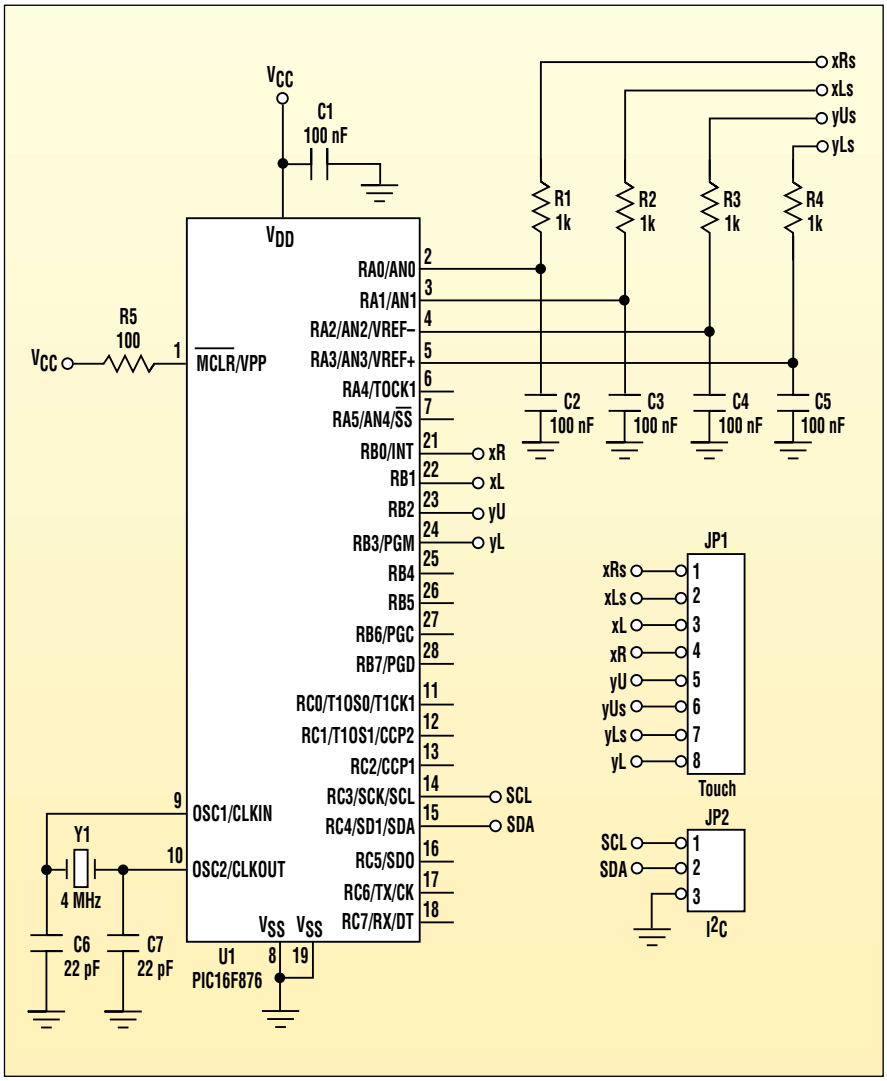
$$n_{IN} = \frac{NV_{IN}}{V_{CC}} \quad n_+ = \frac{NV_{REF+}}{V_{CC}} \quad n_- = \frac{NV_{REF-}}{V_{CC}}$$

Combining these values will return the same result as for the multiplexing-sense-lines conversion:

$$n_{IN} = \frac{N(n_{IN} - n_-)}{(n_+ - n_-)} = \frac{N(V_{IN} - V_{REF-})}{(V_{REF+} - V_{REF-})}$$

Both techniques (multiplexing and nonmultiplexing the sense lines) are equivalent. However, the last technique is particularly useful in microcontroller-based touchscreen controllers. This technique has been used to build a touchscreen controller with an I²C interface for a 12.1-in. eight-wire resistive touchscreen. While there are some commercial touchscreen controllers available, all of these utilize an RS-232 interface. In this application, there were no free RS-232 ports.

The touchscreen controller is based in the PIC16F876 microcontroller from Microchip *(Fig. 5)*. This microcontroller includes a five-channel 10-bit ADC and supports the I²C interface. The above mentioned nonmultiplexing-sense-lines technique was employed. With this technique, a minimal amount of external components are needed (only an optional low-pass filter has been added to eliminate noise). Low cost and compact size distinguish the resulting I²C-compatible eight-wire touchscreen controller.



5. The PIC16F876-based eight-wire touchscreen controller includes a five-channel 10-bit ADC and supports the I²C interface. An optional low-pass filter has been added to eliminate noise.

ideas wanted

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Digitally Controlled Pots Program PWM's Features

William F. Slack

CIRCLE 522

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Chuck Wojslaw

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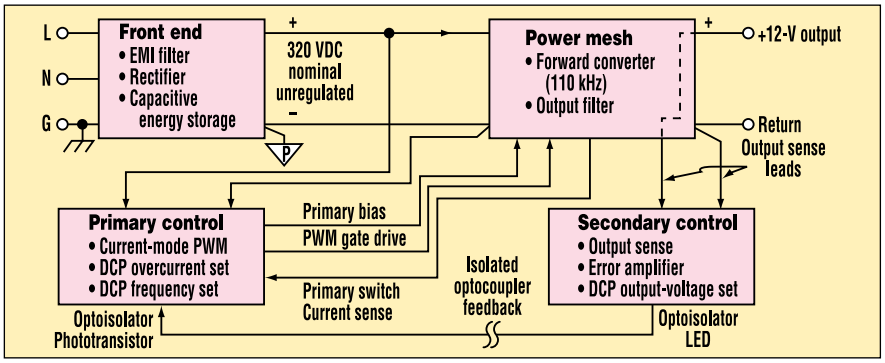
The circuit described here is a switching 12-V, 10-A power supply whose topology is that of a conventional single-switch forward converter *(Fig. 1)*. To derive the pulse-width modulation for its switch, the converter uses peak-current control. The front end processes the ac-line power and delivers an unregulated 320 V dc to the downstream dc-dc converter in the power mesh.

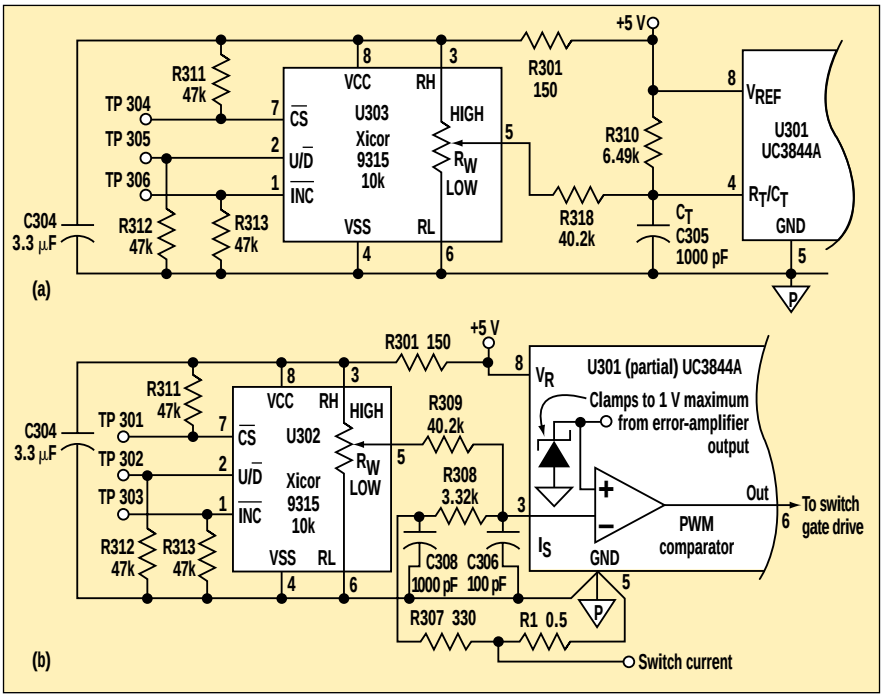
After processing the power delivered by the front end, the power mesh drives a regulated 12 V dc at 10 A at the front end's output. Included in the secondary control is an error amplifier that compares the 12-V dc output voltage with a reference voltage. It also provides optocoupled feedback to the primary control. The primary-control section of the power supply is designed around the low-cost UC3844A pulse-width-modulator (PWM) current-mode controller *(Figs. 2a and 2b)*. In addition to controlling the transformer switches in the power mesh, the pulse-width-modulated output of the PWM regulates the power supply's output voltage.

Two key features of the PWM, the operating frequency and the overcurrent limit, are programmed by Xicor's digitally controlled potentiometers (U303 and U302). Using electronic potentiometers rather than their traditional mechanical counterparts offers lower cost, higher reliability, and automatic calibration during production testing. The PWM clock frequency is set by C305 (C_T) and the Thevenin resistance (R_T) formed by R310, R318, and potentiometer U303 *(Fig. 2a, again)*. For high values of R_T, $f \approx 1.72/R_TC_T$. Setting the converter frequency precisely to its design target value of 110 kHz reduces the design margin needed when designing the supply's expensive magnetic components.



1. In addition to the 12-V output level, both the switching frequency and overcurrent limit are programmed by digitally controlled potentiometers in this 10-A switching supply.

The PWM's overcurrent limit is established by the 1-V zener diode connected to the PWM comparator's noninverting input *(Fig. 2b, again)*. This voltage's



2. The clock frequency is set by C305 (C_T) and the Thevenin resistance (R_T) at U301, pin 4 (a). The overcurrent limit is controlled by the 1-V zener diode internal to U301 (b).

limit controls the maximum value of the transformer's primary peak current. The voltage at the inverting input is proportional to the sum of the switch/output current through R1 and the current through R309 (which is generated by the programmed voltage of digitally controlled potentiometer U302). The nominal onset of overcurrent protection is 10.67 A.

From the measured data, the programmable converter frequency can be varied from 101.7 kHz to 122.9 kHz. The overcurrent protection onset can range from 8.09 A to 13.85 A. A "bed-of-nails" interface, similar to those used for parametric testing, supplies low-cost access to the DCP pins through test points 301 to 306. R301 and C304 provide the proper turn-on slope for the 5-V output or V_{REF}. As a result, the proper initial wiper setting of the DCP can be recovered from nonvolatile memory during power-up.

Embedded Processor Directly Drives An On-Screen Display

Daniel Malik

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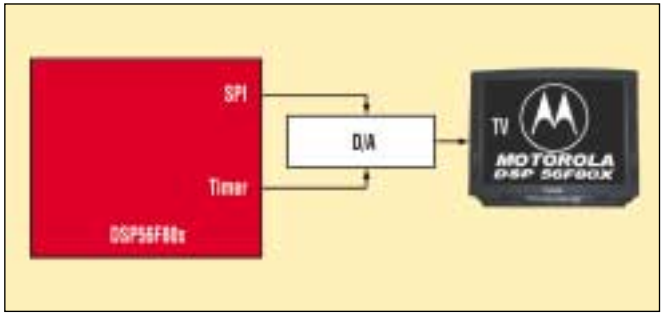
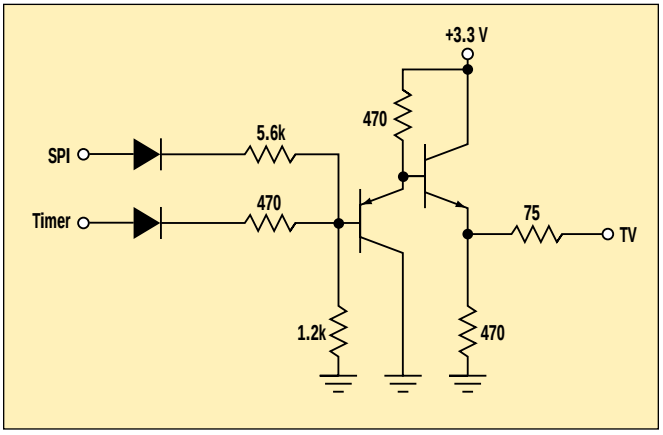


1. The on-screen display (OSD) combines a synchronization signal generated by an on-chip timer peripheral with the pixel-data signal output, also generated on-chip using an SPI peripheral.



2. This simple circuitry converts the two digital signals into an analog-video signal and matches the 75-Ω input impedance of the TV set.

Visualization of measurement results or application status is an increasingly requested feature. However, the generation of images on a TV screen does not always require expensive cards or chips. In some cases, a black-and-white picture will suffice.

The black-and-white video signal accepted by standard TV equipment requires only three discrete voltage levels. This signal can be further separated into two binary components: the synchronization signal and the picture signal. This property can be utilized advantageously during video-signal synthesis. The synchronization signal is always the same. Only the picture component differs from image to image.

The synchronization signal can easily be generated by an intelligent timer peripheral, according to a static lookup table. A suitable timer peripheral is often present on-chip in modern microcontrollers or DSPs.

The on-screen display (OSD) is formed by a picture data stream consisting of pixel values (black = 0, white = 1). The simplest way to generate such a data stream is to make use of almost any serial on-chip interface, such as a synchronous serial port or an SPI peripheral. This interface simply transmits data from a pixel map stored in memory. This operation must be aligned with the synchronization signal generated by the timer. This requirement can easily be met by taking advantage of the timer-interrupt feature.

The above idea was tested using the DSP56F805 from Motorola. The implementation of the OSD circuit is shown in Figure 1. The circuitry needed to convert the two digital signals into an analog-video signal and the output amplifier needed to match the 75-Ω input impedance of the TV set can be arranged in a configuration as simple as that shown in Figure 2.

3. This sample video image features a display resolution of 256 by 287 pixels.

When considering image quality, a compromise must be made between resolution and the memory space needed for the picture pixel map. The required computing power increases with picture resolution. More performance is required than the raw power needed to actually display the picture—the creation of the picture in memory can be even more demanding than displaying the image itself.

In this application, the compromise between resolution and memory space resulted in a resolution of 256 by 287 pixels with about 20% of the computing power consumed by the display process. The maximum reasonable res-

olution achievable with this particular DSP would be about 1024 by 574 pixels. Note that while the horizontal resolution can be freely modified, the vertical resolution is defined by the appropriate video standard (a PAL-compatible TV set was used in this case). An example of the displayed picture is shown in Figure 3.

SOT-223 High-Voltage Transistor Creates LCD Heater

Martin O'Hara

Telematica Systems Limited, University Way, Cranfield, Bedfordshire, MK43 0TR, England

Occasionally, components cannot be obtained that function over the full temperature range of a product. For example, LCDs have a very limited operating-temperature range of typically 10°C to 50°C. One way to eliminate complications at the low-temperature end of this range is to provide a heat source for the component within the circuit design. A simple technique is presented in Fig. 1 that effectively requires only a single surface-mount transistor as a logic-controlled heating element.

This design takes advantage of the fact that FETs designed for high-voltage signal-switching applications often feature what might otherwise be described as high on-resistance values (R_{DSON} > 10 Ω). Yet, some of these FETs are designed to interface with low-voltage control systems. Hence, a 5-V TTL/CMOS signal can control these transistors, intended for over 200-V drain-source switching. Since these devices are expected to carry low currents, they are available in small surface-mount packages, such as SOT-223. Small package size allows easy integration without occupying a large amount of board space. Space is often a problem in designs where resistor heaters or TO220-packaged FETs are used.

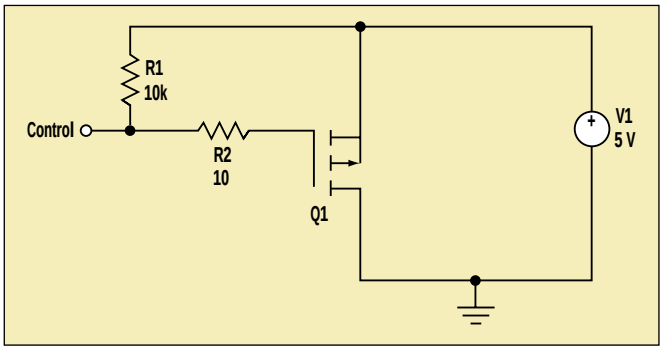
P-CHANNEL FET THERMAL CHARACTERISTICS WITH 5-V SUPPLY

FET	Max R_{DSON} (Ω)	Min R_{DSON} (Ω)	Min P_D (mW)	Max P_D (mW)	Min I_{DS} (mA)	Max I_{DS} (mA)	Min temp rise (°C)	Max temp rise (°C)
ZVP0545G	150	50	167	500	33	100	10	31
ZVP2120G	25	20	1000	1250	200	250	63	78

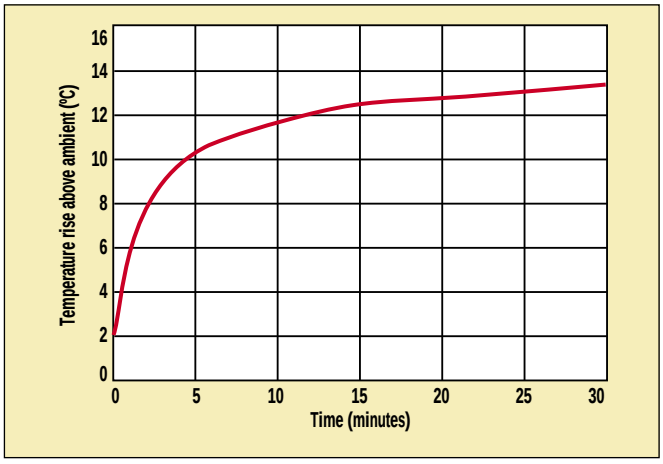
A p-channel FET simplifies the design, with control maintained via a 0-V (ground) signal applied to the gate. Otherwise, the heater is off and the gate is pulled high via a pull-up resistor (R1). R1 can be a low-power surface-mount resistor. The heat generated is transferred from the silicon through the metal tab of the 2-W SOT-223 package. Since the drain is also the tab connection on the SOT-223 package, the heater metalization also provides a ground shield even when the heater is off. Another benefit of this design is that the heater power can be easily increased by paralleling FETs. These FETs can have either a single control (i.e., on/off) or multiple digital controls, where different heating settings can be applied (e.g., rapid heat-up and maintenance heating).

Table 1 shows the calculated thermal performance at the tab of two Zetex FETs when operated at 5 V. The temperature rise is measured at the drain tab. Since some loss of heat will occur in the thermal transfer from the tab to the heating pad, the temperature at the drain tab is not the same as the temperature under the heated component.

The graph *(Fig. 2)* shows the temperature rise obtained using the ZVP0545G under a small LCD display. While the heat is not enough to cause significant overheating in either the FET or the LCD, it is sufficient to extend the low-end operating temperature of the product from 10°C to 0°C.



1. This heater circuit utilizes the fact that FETs designed for high-voltage switching applications often feature high R_{DSON} values.



2. The temperature rise obtained is sufficient to extend the low-end operating temperature of the product from 10°C to 0°C.

Switch-Debouncer IC Creates A Long-Period Timer

Phill Leyva

Maxim Integrated Products, Sunnyvale, CA

One major application for long-period timers is in remote weather-data stations. These stations measure environmental conditions at regular time intervals and transmit the results to a central collecting facility. Since these small weather stations are often located in remote areas that depend on solar-cell power during cloudy weather, power efficiency is an important factor in their design. Size and cost are also prominent considerations.

A minimum-component configuration is possible for an all-surface-mount, low-power, long-period timer. This design can be implemented with two low-cost components and firmware that reduces power consumption by allowing the microcontroller (µC) to enter a "sleep mode." Later, the µC is awakened to perform regularly scheduled measurements. The circuit shown in Fig. 1 accomplishes this task by taking advantage of the extra section in a dual CMOS switch-debouncer (U1).

THRESHOLD VERSUS V_{CC} VOLTAGE FOR MAX6817 SWITCH DEBOUNCER

System voltage, V_{CC}	Threshold voltage, V_T
2.7 V	1.30 V
3.0 V	1.45 V
3.3 V	1.50 V
5.0 V	2.00 V

The µC (U2) provides 32 bytes of RAM and 1232 bytes of EPROM. (A low-cost, one-time-programmable version is also available.) The IN1/OUT1 pins of the dual debouncer U1 are configured to debounce the µC's system-reset pulse. The IN2/OUT2 pair is configured as the long-period timer. Capacitor C1 and a 63-kΩ (typical) pull-up resistor internal to U1 form the time constant for this purpose.

U1 initiates a 50-ms delay when the C1 voltage reaches U1's input-voltage threshold. Following this delay, OUT2 turns on the n-channel digital FET N1, which must remain on long enough to completely discharge C1 in preparation for the next timing cycle. The second transition (high-to-low) at IN2 initiates another 50-ms delay. Following this delay, the cycle repeats. Thus, the timer period can be calculated using the following equation:

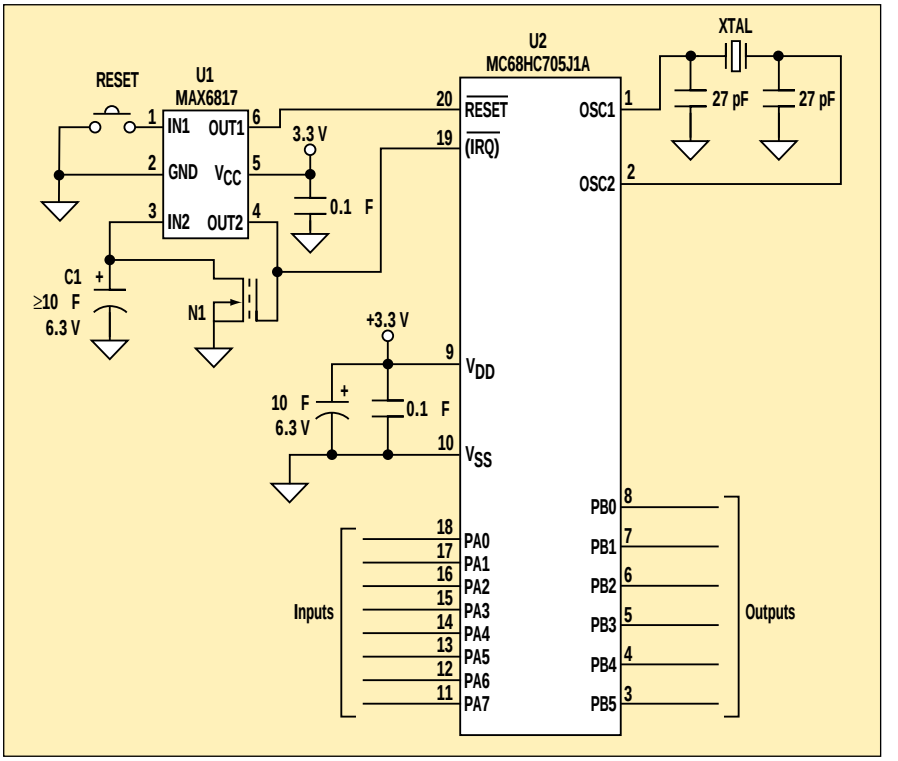
$$\text{Period (s)} = (63\text{k} \times \text{C1} \times (-\ln(1 - V_T/V_{CC})) + 0.1\text{s})$$

Table 1 shows the input threshold voltage (V_T) for U1 at various operating voltages (V_{CC}). The following equation can be used to determine the C1 value for a desired timer period:

$$\text{C1} = (\text{Period} - 0.1\text{s})/(63\text{k} \times (-\ln(1 - V_T/V_{CC})))$$

where Period equals the desired time delay in seconds.

Remote weather stations report at certain intervals, and the time of these



In addition to debouncing the microcontroller's RESET input, the unused half of this dual switch-debouncer IC (U1) is used to implement a long-period timer function.

reports is recorded by the collection station. Since timing is not critical, the C1 capacitor can be a tantalum type with ±20% tolerance. If tighter timing is desired, a surface-mount ceramic capacitor can be substituted for C1.

The digital FET N1 was chosen for its low-level gate drive, which enables it to operate properly in 3- to 5-V circuits. If a different FET is substituted, it must be capable of discharging C1 completely before U1 changes the output state to low. Specifically, it should provide a discharge time ($5R_{DSON}C1$) less than 50 ms. If the shortest possible period is desired, U1 can be configured as a 10-Hz stable multivibrator by removing C1 (leaving the drain of N1 connected to pin 3 of U1).

The program code, written in 68HC705 assembler, for the long-period timer is available for download at *www.PlanetEE.com* by following the Ideas for Design link.

Single-Wire Sensors Interface Directly To A PC

D.S. Oberoi — *CEDTI, Jammu, India*

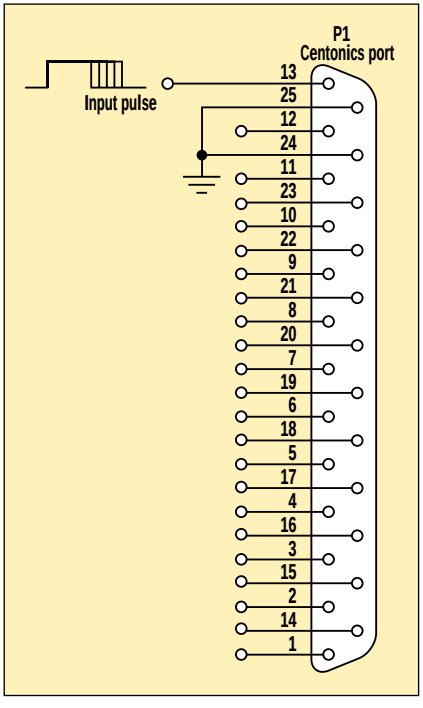
Harinder Dhingra — *GCET, Jammu, India*

Over the years, various vendors have developed a number of interfacing techniques to help address design requirements for simplified signal conditioning, reduced component count, and lowered development and system costs. One such low-cost interfacing technique is the use of pulse-width-modulated (PWM) digital outputs to eliminate the need for costly analog-to-digital converters (ADCs). This approach also decreases the number of signal wires required.

Using this PWM approach, the measured data's value is passed on as a variable-length pulse to the measurement and control system through a single-wire interface. The on-period (t_{ON}) of the pulse indicates the value of the measured quantity. Any change in the measured value will cause t_{ON} to vary. The measured data can be captured to a specified degree of resolution by measuring t_{ON}. Modern microcontrollers have an onboard timer/counter peripheral that can easily be used to measure the pulse width.

PWM-output devices (single-wire interface) can be interfaced directly to a PC as shown in the figure. In a PC, there are no unused timer/counters available for measuring pulse widths. However, the PC's counter2 (a 16-bit, 8254 timer/counter), normally utilized for the PC's speaker operation, can be used for measuring the pulse width of a PWM signal. This counter operates using a clock frequency of 1.1931817 MHz (TIMER_FREQUENCY) and can be enabled or disabled by setting bit-0 of port 61h to one or zero, respectively.

For this application, counter2 is operated in mode 2 (i.e., as rate generator) and is configured by loading its control register at port 043h with a control word value of 0b4h. Initially, counter2 is loaded with an ffffh count at port 042h (i.e., counter2's read/write I/O port) in two cycles. During operation, the input signal is sampled continuously and, at the first rising edge, counter2 is enabled by setting bit-0 of port 61h to one. When counter2 is enabled, its count follows an auto-decrement pattern of one count every 0.838095 µs (1/TIMER_FREQUENCY). As long as the input pulse is high, counter2's count (elapsed_count) is read back in two cycles from port 042h. At this juncture of operation, the elapsed count is checked to see if the time period of the pulse is greater than ~54.9 ms (this is the maximum time period that counter2 can measure). If the input pulse width is greater than this limit, the overflow counter is incremented and the counter2 count is automatically set to an ffffh count. With the trailing edge of the input pulse, counter2 is disabled by setting bit-0 of port 61h to zero.



Single-wire sensors can be acquired directly by a PC if the counter/timer associated with the PC speaker function is reallocated for use by this application's pulse-width measurement function.

The counter data is stored in a data array (count[i]) whose length depends on the pulse width. If the pulse width is less then 1 ms, the length of the data array is 20; otherwise, it is 1. This is necessary to minimize the error when measuring small-pulse-width signals. The 20 array elements are arranged in ascending order (averagedata( )) and the average of the 10 middle values is used in the calculation of pulse width. Pulse width (pulse_width) is calculated using the overflow counter and the counter's count data. It is then displayed. Before starting the next read cycle, counter2 is reset with a count of ffffh. This process continues until the user presses the 'Q' key, which terminates the program and restores the screen attributes.

The software listing, written in C (Turbo C++, version 3.0) and assembly, can be found at *www.PlanetEE.com* by following the Ideas for Design link. It was tested in the MS-DOS mode of Win95 on a 450-MHz Pentium II. The minimum pulse width that could be measured was ~23 µs. The software can be easily modified to determine t_{OFF} or to calculate the frequency of the input pulse stream.

Taking The Stops Out Of Digital Potentiometers

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CIRCLE 522

A three-wire bus is commonly used to control digitally controlled potentiometers (DCPs). One example of this type of bus is Xicor's 32-tap X9315 (U3), shown in the figure. This asynchronous bus has no protocol and is popular in real-time and control applications.

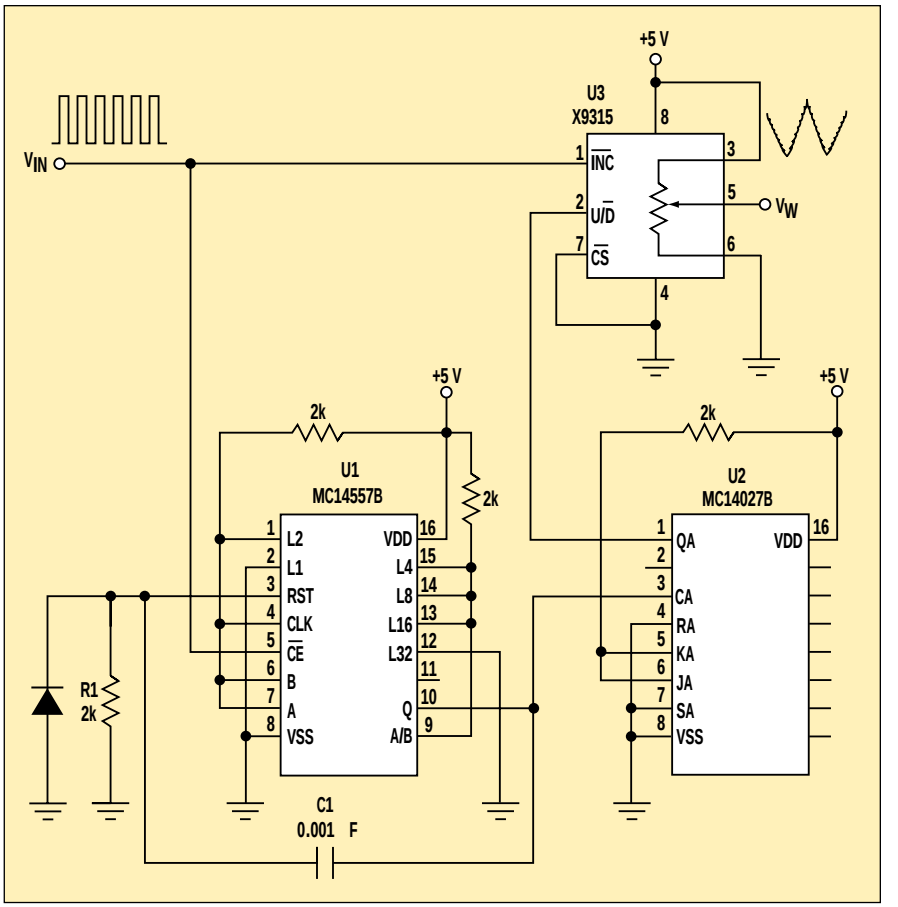
The bus consists of a chip-select pin ($\overline{CS}$) required for addressing, and an up/down pin (U/$\overline{D}$) to establish the direction of the potentiometer's wiper. It also includes an increment pin ($\overline{INC}$), which advances the wiper. A gated clock often is used to drive the $\overline{INC}$ pin. When the wiper reaches the end of the potentiometer in the up or down direction, it remains at that limit (it "stops").

Many continuous real-time applications require that the wiper's direction be automatically reversed when its limits are reached. Fade-in/fade-out controllers in neon light systems are a good example of this type of application.

By changing the high/low state of the signal on the potentiometer's up/$\overline{down}$ input, the U1 and U2 portions of the circuit automatically reverse the wiper's direction. U1 is a variable-length serial shift register, while U2 functions as a J-K flip-flop connected in the toggle mode. A variable-length shift register can accommodate 16-, 32-, and 64-tap potentiometers if the register's L1 to L32 lines are programmed appropriately.

For every clock pulse at V_{IN}, the DCP's wiper is moved forward one position and a logic 1 is moved one position in the shift register. The Q output of the shift register will go high after 31 pulses. As a result, the output of the J-K flip-flop complements Q's output state. Differentiated by the R1/C1 circuit, this signal also resets the shift register to start the cycle over again. If V_{IN} is a continuous stream of clock pulses and the potentiometer pins are connected across a 5-V supply, the wiper output voltage (V_W) will be a staircased triangular signal.

The circuit's operation was confirmed over a 10-Hz to 100-kHz range. For continuous, closed-loop feedback applications, adding the U/$\overline{D}$ signal to the stop-less circuit reduces the pin count of the serial bus.



The potentiometer's up/$\overline{down}$ input is used to automatically reverse the wiper's direction. A variable-length serial shift register (U1) allows operation with 16-, 32-, and 64-tap devices.

ifd winners

Ken Yang, Maxim Integrated Products, Sunnyvale, CA.

The idea: *"Single-Chip Transmitter Extends Home-Entertainment Systems."* November 6, 2000 Issue.

W. Stephen Woodward, University of North Carolina, Marine Sciences; e-mail: woodward@unc.edu.

The idea: *"Simple Current-Loop Transmitter Converts PWM To 4-to-20-mA Output."* November 20, 2000 Issue.

W. Stephen Woodward, University of North Carolina, Marine Sciences; e-mail: woodward@unc.edu.

The idea: *"Take-Back-Half: A Novel Integrating Temperature-Control Algorithm."* December 4, 2000 Issue.

Huw Jones, ESD Consultants, Llantrisant, Mid Glamorgan, U.K.

The idea: *"RS-485-To-RS-232 Transceiver Takes Its Power From The COM Port."* December 18, 2000 Issue.

ECL Pulse Generator Produces Balanced Outputs At 1 MHz

Hubert Houtman
4298 Masterson Rd., Blaine, WA 98230

CIRCLE 520

Sub-nanosecond risetime pulse generators with high repetition rates are necessary for gauging an oscilloscope's step response, time-domain reflectometry (TDR), and differential TDR. They're also effective for measuring the reverse recovery of diodes as well as the response and propagation delay of cables, transistors, amplifiers, and comparators. Time-domain studies like these generally require bipolar pulses, with a separate low-jitter pulse capable of triggering an oscilloscope or other test equipment.

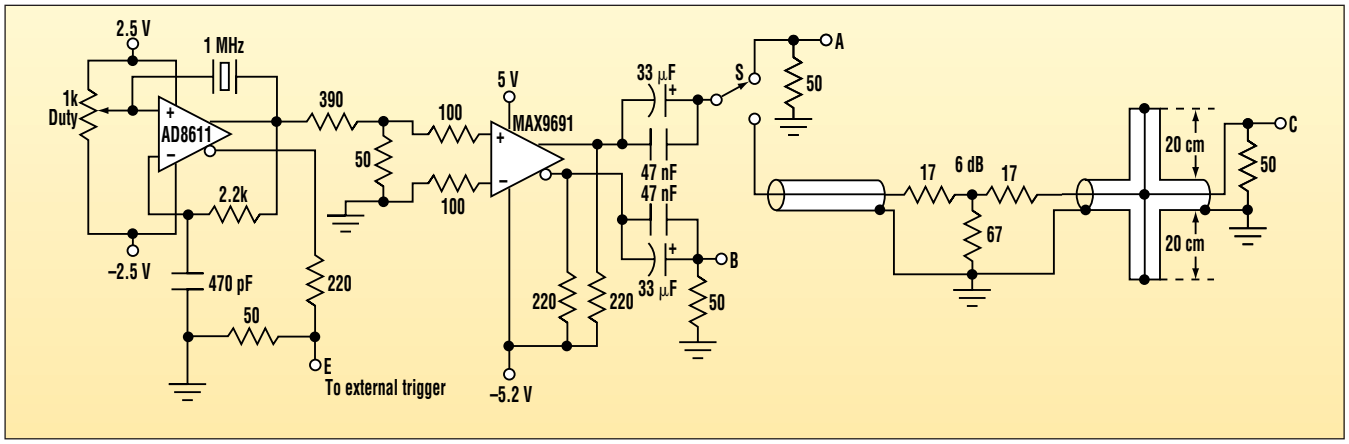
This circuit produces such a trigger, along with balanced ECL outputs, at a pulse-repetition frequency of 1 MHz *(Fig. 1)*. The AD8611 high-speed comparator is wired as a square-wave oscillator. Using the 1-kΩ potentiometer, positive feedback via a 1-MHz crystal is adjusted to yield a 50% duty cycle. While the complementary output provides a fast step-pulse to trigger an oscilloscope, the other output triggers a MAX9691 high-speed comparator. This comparator delivers balanced, ECL-level transitions that are specified at a 500-ps risetime. All components, including three BNC-connectors at A, B, and E, were mounted on a small PC board (Radio Shack #276-150) employing surfboards for the SO-8 comparators.

If the RG-58A/U cable network is connected using the switch S, the double shorting stub produces a short pulse at C. A single, inverted, delayed step-pulse is created, which follows the incident step-pulse toward C. The 6-dB attenuated step is divided at the cross-joint. It first splits into three equal transmitted pulses and one equal-and-opposite pulse that's reflected back toward the attenuator. Each pulse carries one quarter of the power, or half the voltage of the step.

At each shorted end, the pulse reflects with a sign reversal and returns to the cross-joint. Here, it splits again into three transmitted pulses and one equal-and-opposite reflected pulse. This reflected pulse, however, is canceled exactly by the equal-and-opposite pulse transmitted across the cross-joint from the other stub. So the result at C is that the primary step-pulse, which is one-quarter of the comparator's voltage, is followed by an equal-and-opposite step. The relative delay caused by the stub's round-trip time defines the length of the short pulse observed at C.

Two BNC T-adapters (i.e., Radio Shack #278-112) make up the coaxial cross-joint. Using a bandsaw, a 90° "V" is cut into the back of one of the T-adapters at a 45° orientation. Doing so makes it possible to fit a fourth BNC port, cut similarly from the other adapter. This fourth port is soldered to the adapter's V-cut using a low-heat iron. Finally, the brass center-conductor is threaded into the cross-joint center-conductor. A short length of 1-72 UNF threaded rod, cut from a small machine screw, is used for the threading process. The completed cross-joint is then plugged into the four RG-58A/U cables *(Fig. 1, again)*.

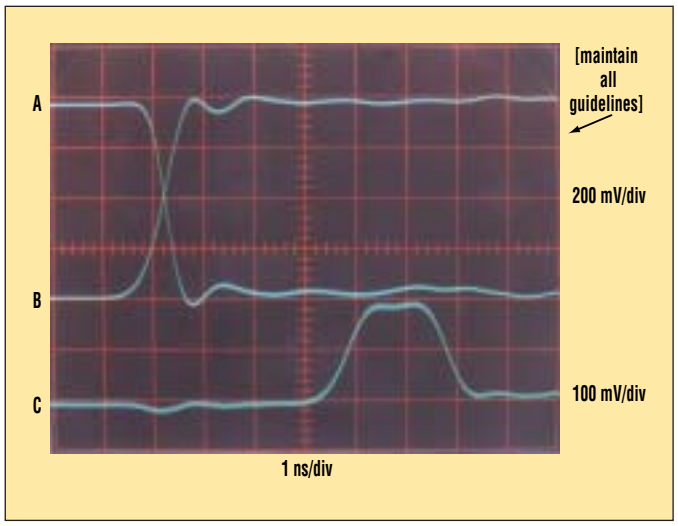
These outputs were measured on a 1-GHz-bandwidth, homebrew sampling oscilloscope with a Tek 503 X-Y oscilloscope for the display *(Fig. 2)*. The high pulse-repetition frequency of 1 MHz allows a high scan rate of 50 Hz. As a result, a live, flicker-free display is produced. Each nanosecond of equivalent time displays 200 samples,



1. The square-wave oscillator triggers the oscilloscope and the MAX9691 comparator to produce the ECL-level output step-pulses, or nanosecond pulses via the shorting-stub network. A pulse-repetition frequency of 1 MHz yields a flicker-free display at a 50-Hz scan rate.

corresponding to an interval of 5 ps/sample. The sampler was triggered by a terminated RG-58A/U cable using the attenuated AD8611 complementary output at E.

While Trace A depicts the MAX9691's ECL-level output driven by coupling capacitors, Trace B shows the complementary output. Transition durations are about 500 ps, in agreement with the component specification sheet. Trace C illustrates the pulse after the shorting-stub network, connected by switch S.



2. Shown is the sampling-oscilloscope display of the MAX9691's output (Trace A) and its complementary output (Trace B). Trace C shows the output of the shorting-stub network.

For this 2-ns pulse, 20-cm long stubs were employed. But different stub lengths will yield other pulse durations, including sub-nanosecond pulses. Transition trace widths on this photograph are less than 0.10 of the 200-ps smallest divisions. This indicates that the system jitter is less than ±10 ps.

Due to frequency-dependent attenuation of the line, the 40-ns delay line commonly used in a sampling oscilloscope input limits the device's bandwidth. As an alternative, a 40-ns delay line may be installed between the two comparators, becoming part of the 390-Ω:50-Ω attenuator. The AD8611 will then provide a low-jitter trigger at E, which precedes the MAX9691's pulses by 40 ns. In turn, the delay line may be eliminated from the sequential-sampling oscilloscope, thereby improving its bandwidth.

For a general-purpose pulse generator, it may be beneficial to have pulses shorter than those shown. With TDR tests, however, it's better to have steps whose transition durations are commensurate with the risetime of the pulses implemented in the final system. Super-fine structure details are then automatically filtered out by the transition duration. Therefore, they will not obscure the TDR traces. A faster component, such as the Motorola MC100EL32D flip-flop, can be substituted for the MAX9691 in order to produce shorter pulses.

Four-Digit Panel Meter Costs Less Than Six Dollars

Jim Walker

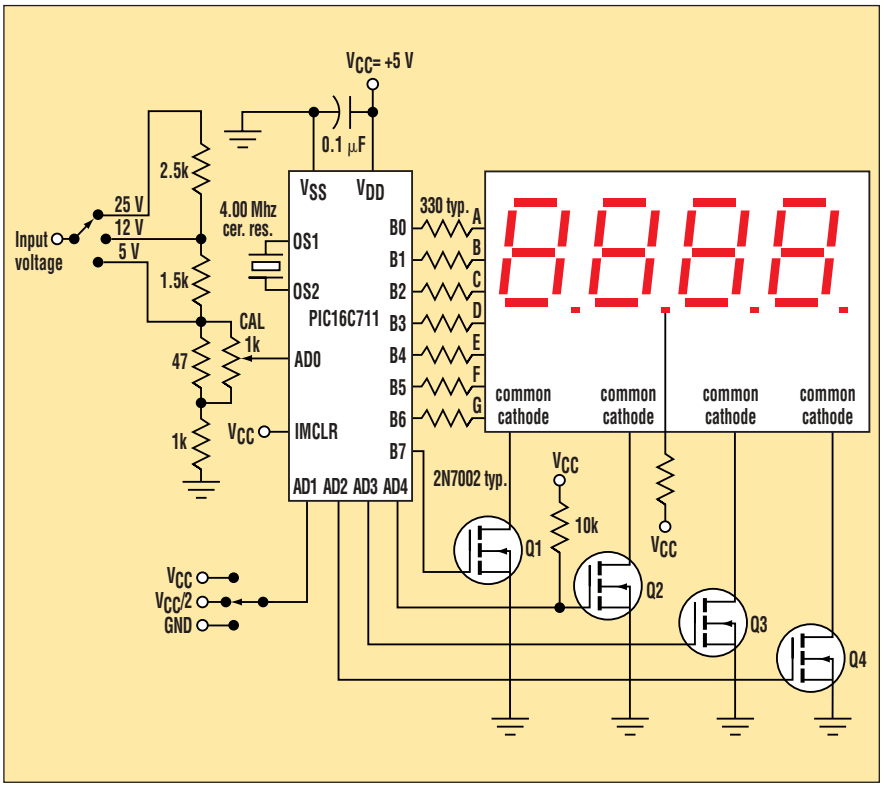
812 North Rd., San Bernardino, CA 92404; (909) 987-4673

CIRCLE 521

While many products can be improved by the incorporation of a digital panel meter, the price of the device often precludes its inclusion. The circuit shown offers a low-cost solution *(see the figure)*. As an added bonus, the circuit is pin-selectable for three different display ranges. The total parts cost is less than $6.00 in quantities of 100.

The low-cost PIC16C711 forms the heart of the panel meter. It is config-

READER SERVICE 138



This four-digit panel meter is an inexpensive but attractive add-on for a variety of products.

ured with two of its inputs as 8-bit analog-to-digital converters (ADC). While AD0 is the voltage input, AD1 is the range-select input. If AD1 is wired to ground, the unit will display a range of 0.00 to 5.10 V with a 20-mV resolution (the left digit is blank).

With AD1 wired at mid-voltage, the display reads 00.00 to 12.75 V with a 50-mV resolution. With AD1 wired to V_{CC}, the display reads 00.0 to 25.5 V with a 100-mV resolution (the right digit is blank). A total of 256 voltage increments are displayed.

Since the voltage reference is the V_{CC} supply, the accuracy after calibration is as stable as V_{CC}. The 16C711 is rated for ±1/2-LSB over temperature. The micro has an open drain output on RB4, requiring an external pull-up resistor. Also note that external voltage attenuators are required for the upper voltage ranges.

The PIC chip functions as a seven-segment decoder/driver, driving all four seven-segment LEDs at once. Only one of the four seven-segment LEDs is illuminated at a time. It is pulled to ground on the common cathode terminal by Q1 through Q4, respectively. The decimal point is selected through an independent resistor.

The LED pack is MSQC6940C, available from Mouser for $2.06 per 100 units. The PIC16C711-04P is available from Digikey for $2.23 per 100 units. The 4-MHz resonator is ZTT-4.00MG, also available from Digikey at $0.45 per 100 units. The PIC code listing for the PIC16C711 can be viewed or downloaded at *www.PlanetEE.com* (click on the Ideas for Design icon).

ifd winner

W. Stephen Woodward, Marine Sciences, Univ. of North Carolina, Venable Hall, CB3300, Chapel Hill, NC 27589-3300; woodward@unc.edu.

The idea: *"Circuit Enables Precision Control In Radiant Heating Systems."* January 8, 2001 Issue.

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Measure Projectile Velocity Optically With An Ohmmeter

W. Stephen Woodward
University of North Carolina, Marine Sciences, Venable Hall, CB3300, Chapel Hill, NC 27599-3300; e-mail: woodward@unc.edu

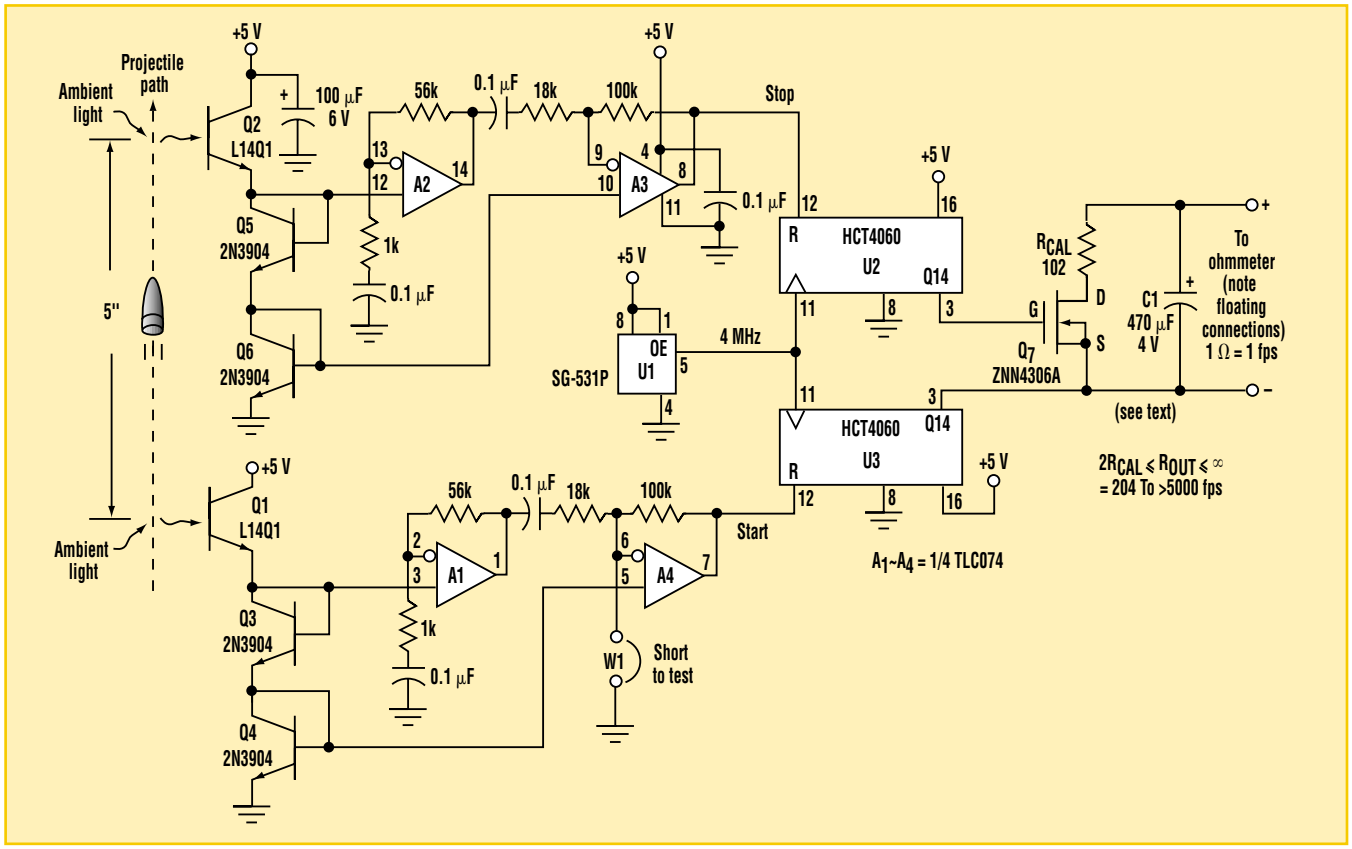
CIRCLE 520

Archery and target shooting with firearms and air guns are just a few of the many sports and pastimes that involve high-speed projectiles. A handy accessory for any of these activities is some means of accurately measuring the speed of the projectile (e.g., air gun pellet muzzle velocity). This enables the condition of the gun, bow, etc., to be monitored, allowing optimum performance and accuracy to be maintained.

Commonly called chronographs, such devices are commercially offered at reasonable prices (less than $100). For some folks, though, the do-it-yourself approach maintains its perennial appeal. For this group, the circuit shown is offered as a cheap, simple, and functional alternative.

Like most electronic chronographs, this one works via optical detection of the passage of the projectile over two points separated by a known distance, D (in this case, the five inches separating phototransistors Q1 and Q2). The time-of-flight, T, between the detectors is, of course, inversely proportional to the average speed, S, of the projectile: S = D/T.

Optical detection of a projectile whizzing past a given point is not always trivial—especially for BBs and other small-caliber air gun pellets that may fill only a small fraction (about 1%) of the detector's field of view. The logarithmic optical-detection method employed here is borrowed from an earlier IFD *("Available-Light Photota-*



A handy accessory for archery and target-shooting buffs with a do-it-yourself tendency, this circuit allows the speed of a projectile to be accurately measured with a standard ohmmeter.

chometer Simplifies Outdoor Remote Sensing," ELECTRONIC DESIGN, *January 25, 1999)* and has a wide dynamic range compatible with low-contrast signals in both outdoor and indoor lighting.

Velocity measurement begins with the passage of the projectile over Q1. The resulting partial occlusion of Q1's view generates a negative pulse at A1's noninverting input of about 500 µV for every 1% of light blocked. A1 and A4 boost and invert by 70 dB to produce a reset (start) pulse to the free-running 14-bit ripple counter U3. Following the projectile's passage, U3 resumes counting from zero, tallying the time of flight (T) with 250-ns resolution.

The same process occurs when the projectile reaches Q2, generating a reset (stop) pulse to U2, marking the end of the flight between detectors. This action results in the capture of a phase difference between the 244-Hz (4 MHz/16,384) square-wave outputs of free-running U3 and U2 equal to T. This phase difference will persist until detection of a subsequent TOF event. Therefore, until then, the TOF measurement remains available for readout.

The problems then remaining are: (1) conversion of this time measurement into the desired reciprocal velocity measurement, a process usually accomplished with software division via a microcontroller, and (2) provision for display of the calculated velocity. This is where that ohmmeter comes into play.

Enhancement-mode MOSFET Q7 ($R_{ON} < 0.25\ \Omega$) is arranged so that it only turns on when U3's output is at logic zero and U2's output is simultaneously at logic one. This state occurs once every 4096-µs U2/U3 cycle and has a duration exactly equal to the phase difference, T. So, the duty factor of Q7's conduction is equal to T/(4096 µs). As a result, the average conductance of the $Q7/R_{CAL}$ combination is equal to $T/(4096\ \mu s \times R_{CAL})$.

This makes the average resistance seen by an ohmmeter connected to the output terminals equal to $R_{OUT} = (4096\ \mu s)R_{CAL}/T$. Because T = D/S, D = 5 in. = 0.417 ft., and $R_{CAL} = 102\ \Omega$, we have: $R_{OUT} = 4096\ \mu s \times 102 \times S/0.417 = 1\ \Omega/ft/s$. Thus, the R_{OUT} resistance readout is a direct linear representation of projectile velocity expressed in ft/s. Depending on the 244-Hz ripple-rejection characteristics of the ohmmeter, ripple-filter capacitor C1 may not be necessary.

Although the circuit constants and flight-path dimensions shown are optimized for the measurement of gun-muzzle velocities in the range of 204 to 3500 ft/s, other component choices can easily adapt the ohmmeter/chronometer to other scenarios and preferences. For example, changing R_{CAL} to 310 Ω will change the scale factor to 10 Ω = 1 m/s; R_{CAL} = 69.8 Ω yields 1 Ω = 1 mph.

High-Speed Noninverting Summing Amplifier Operates To 220 MHz

Chau Tran and Brian Rousseau

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CIRCLE 521

The schematic in Figure 1 is a common summing amplifier with multiple inputs and one single-ended output. It is a variation of a standard inverting amplifier. Point X is a virtual ground and is referred to as the summing junction.

The transfer function for this circuit is:

$$V_O = -[V1(R_F/R1) + V2(R_F/R2) + V3(R_F/R3)]$$

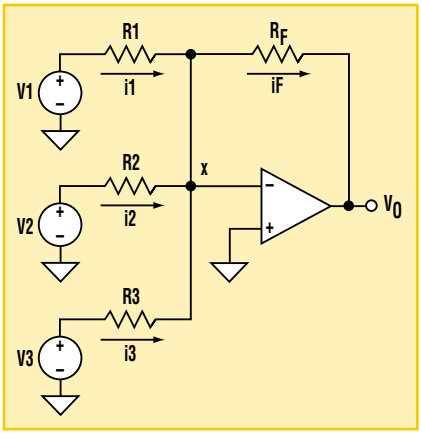
This indicates that the output is a weighted sum of the inputs, with the weights being determined by the resistance ratios. If all resistances are equal, the circuit yields the inverted sum of its inputs:

$$V_O = -(V1 + V2 + V3)$$

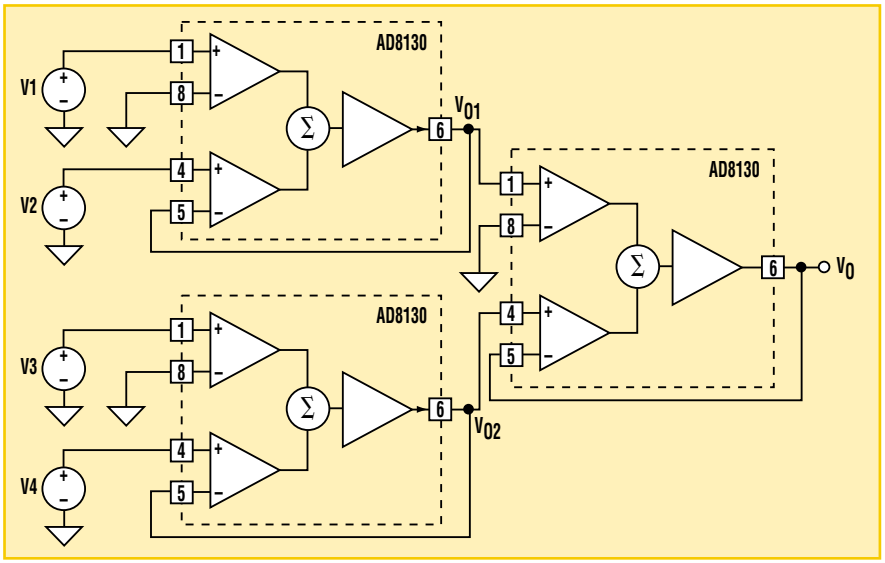
Note that if the noninverted result, $V_O = (V1 + V2 + V3)$, is needed, another inverting amplifier must be added with a gain of –1. The circuit in Figure

1 has many other disadvantages, including low input impedance, different input impedances for positive and negative inputs, narrow bandwidth, and the need for tightly matched resistors.

Figure 2 is the schematic of a high-speed summing amplifier, which can sum as many as four input voltages without the need for an inverter to change the sign of the output. This feature can prove useful in audio and video applications. The circuit contains three low-cost, high-speed instrumentation amplifiers. The first two interface with input signals, and their total sum is taken at the third amplifier's output with respect to ground. The inputs are very high-impedance, and the signal that appears at the network output is noninverting.

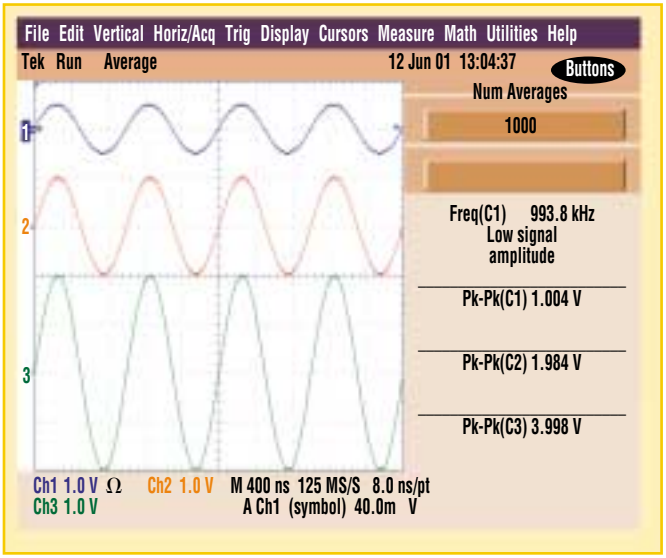


1. The traditional summing amplifier shown above has multiple inputs and one single-ended output.



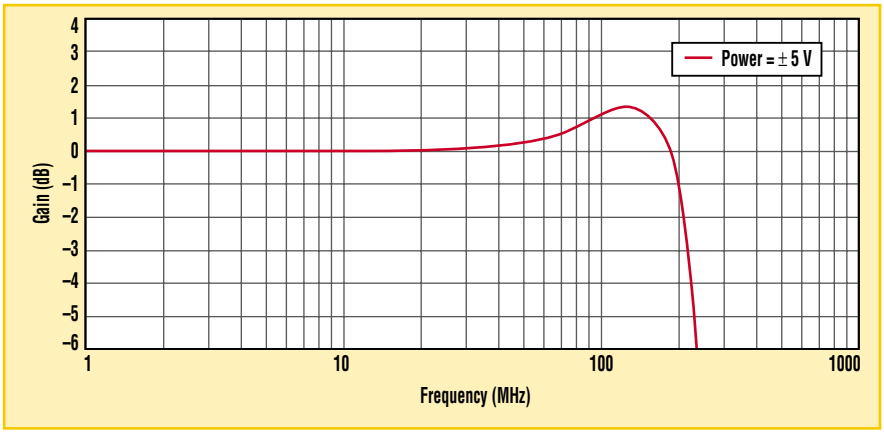
2. This high-speed summing amplifier can sum as many as four input voltages without the need for an inverter to change the sign of the output.

Figure 3 is the performance photo at 1 MHz. The top trace is the input signal for all four inputs. The middle trace is the sum of inputs V1 and V2. The bottom trace is the output of the system, which is the total sum of all four inputs.



3. The performance of the high-speed summing amp at 1 MHz is shown. The top trace is the input signal for all four inputs. The middle trace is the sum of inputs V1 and V2. The bottom trace is the summing output.

Figure 4 demon-



4. The bandwidth of the improved summing amplifier is about 220 MHz.

strates the high bandwidth of the system in Fig. 2. As can be seen from this figure, the –3-dB point is about 220 MHz.

Sub-μA Oscillator Extends Battery Life

Yongping Xia

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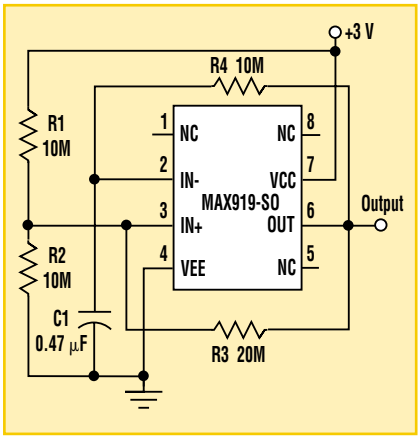
CIRCLE 522

For battery-powered devices, one of the major design challenges is the reduction of power consumption in all functional blocks. An oscillator, a common functional block in many designs, can easily consume anywhere from a few microamps to a milliamp or more. The circuit shown uses a MAX919 to create an ultra-low-power oscillator for designs where the accuracy of the oscillation frequency is not critical *(see the figure)*. The MAX919 is a single comparator with 0.4-μA power consumption.



The use of an oscillator based on an ultra-low-power comparator can provide significant battery-life improvements.

C1	Frequency	Power consumption
22 pF	2.5 kHz	1.7μA
100 pF	1.1 kHz	1.1 μA
470 pF	350 Hz	0.8 μA
1000 pF	170 Hz	0.7 μA
3300 pF	52 Hz	0.6 μA
0.01 μF	20 Hz	0.6 μA
0.033 μF	6.3 Hz	0.6 μA
0.1 μF	2.2 Hz	0.6 μA
0.47 μF	0.5 Hz	0.6 μA

R1 and R2 provide a reference voltage to the comparator. R3 is used to increase the threshold of the comparator. R4 and C1 are the main components that determine the frequency of the output signal. The table gives the output frequency for particular values of C1 as well as the resulting power consumption. The useful power-supply voltage ranges from 1.8 to 5.5 V. Since the MAX919 is a CMOS device, the logic-high and logic-low output voltages are nearly rail-to-rail.

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READER SERVICE 121

Resettable High-Speed Fuse Uses FET As A Sense Resistor

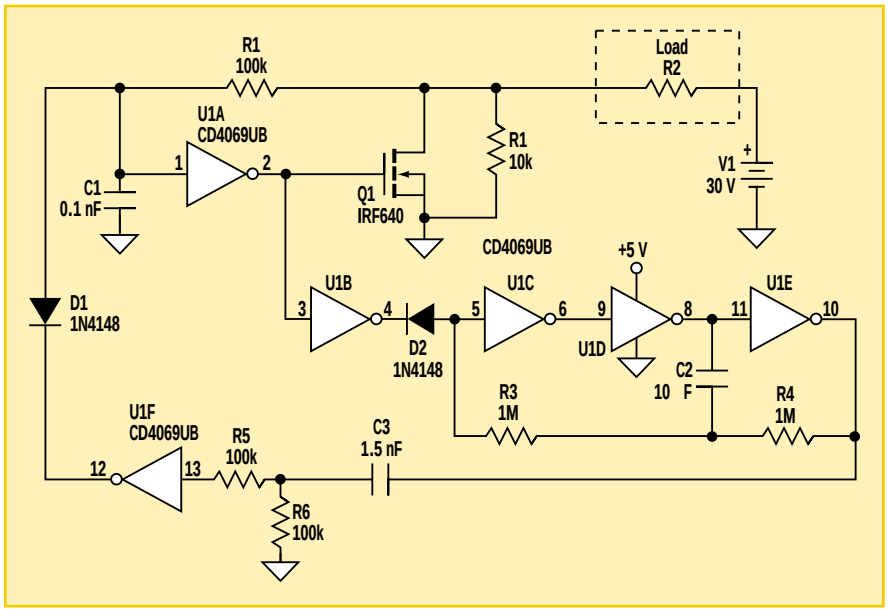
Giovanni Romeo
Instituto Nazionale di Geofisica e Vulcanologia, Rome, Italy

This design idea describes a resettable high-speed fuse that uses only a few off-the-shelf parts, resets itself after blowing, and doesn't require a special current-sense resistor. While the circuit has been designed to switch on a negative current from ground, it can easily be modified for use in a floating arrangement.

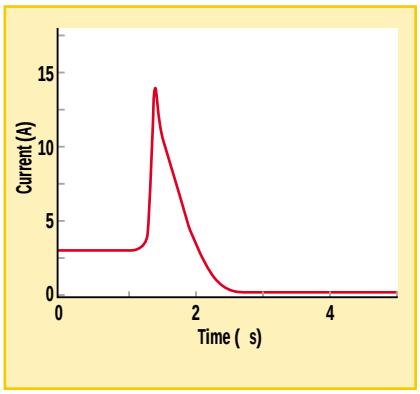
The circuit shown in Fig. 1 uses a power FET as a switch and, when saturated, as a sense resistor. When an excessive current flows through the FET, the source-drain voltage increases and is sensed by inverter U1A. This decreases the gate potential, causing the drain voltage to go even higher and the circuit to drop out in a stable state. In this state, almost no current flows through the load.

The speed of the fuse can be tuned by modifying capacitor C1, which low-pass filters the signal from Q1's drain. The fuse's firing current can be made adjustable by inserting a resistive voltage divider between the inverter output and the transistor gate. Since the fuse speed will decrease due to the FET's gate capacitance, it should be compensated with a capacitor. With the values shown in the schematic, the fuse blows in roughly 1 µs when changing load resistor R2 from 10 to 1 Ω *(Fig. 2)*.

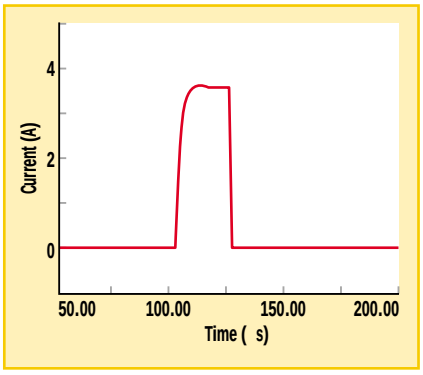
Prior to the activation of the fuse, the three-gate oscillator (U1C-E) is disabled



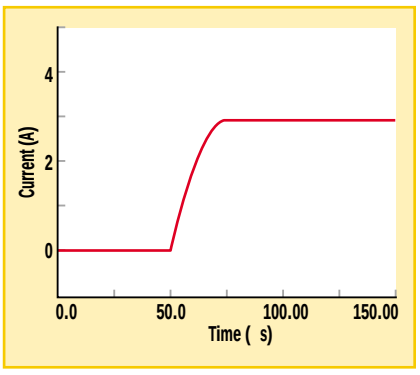
1. This resettable fuse uses the on-resistance of FET Q1 as the current-sense element.



2. When the load is stepped from 10 to 1 Ω, the electronic fuse trips in roughly 1 µs.



3. If the overload condition is still present when the fuse attempts to reset itself, the load current rises to the trip point in 25 µs.



4. During a successful fuse reset, the current rises to its normal operating level in 25 µs.

by gate U1B and diode D1. When the fuse "blows," the oscillator begins oscillating. This periodically (every few tenths of a second) sends a pulse to the inverter U1A input, attempting to reset the fuse. If the short persists, the fuse blows again; this process takes 25 µs *(Fig. 3)*. If the short does not persist, the current rises in 25 µs *(Fig. 4)*.

Spread-Spectrum DC-DC Converter Combats EMI

Ken Yang

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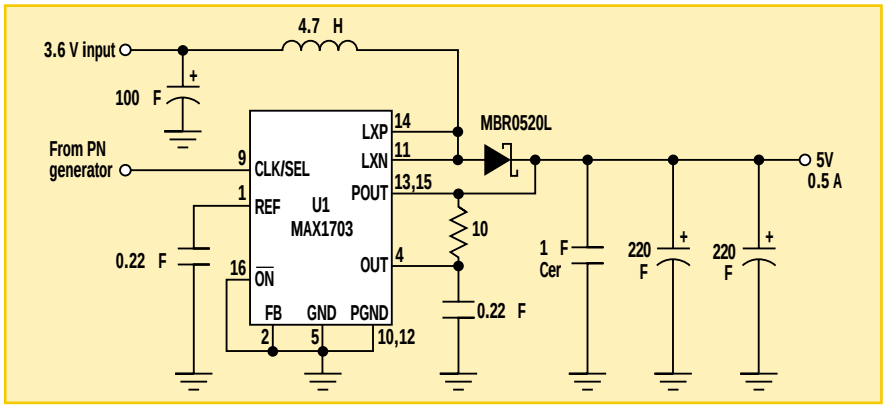
CIRCLE 521

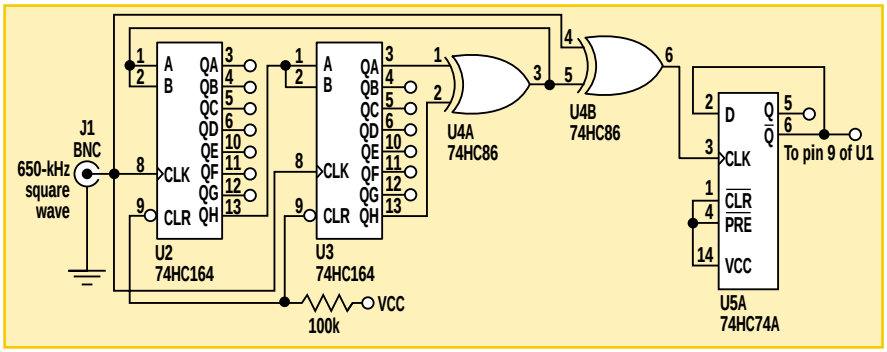
Electromagnetic radiation (called electromagnetic interference or EMI when unwanted) is emitted by almost all electronic systems, including switching regulators. The conventional approach to suppressing EMI is to block the radiation at its source with a metallic or magnetic shield, or both. For switching regulators, you can further enhance suppression by adopting a spread-spectrum pulse-width-modulation (SSPWM) control scheme.

In Fig. 1, the switching regulator IC (U1) has an external clock input. Driving this input with a digital signal of pseudorandom noise (PN) provides the regulator with a spread-spectrum clock that reduces EMI. By spreading interference frequencies over a wide range, this technique lowers the EMI power density that is otherwise concentrated at a single clock frequency.

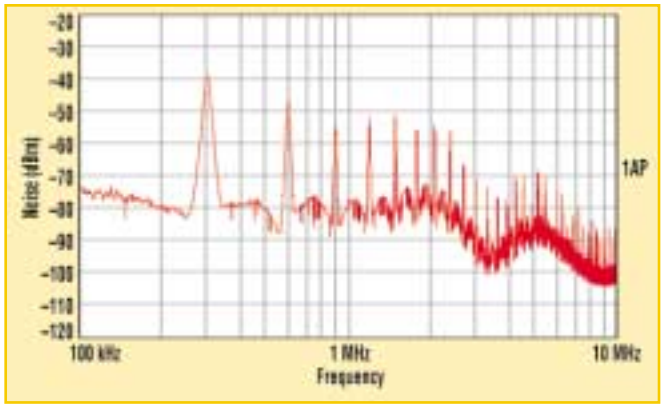
The PN generator spreads interference over a wide spectrum. Its key element is a 16-bit shift register formed by the series connection of two 8-bit shift registers (U2 and U3), with feedback from the XOR gate U4A *(Fig. 2)*. The result is an almost random (pseudorandom) output, consisting of a repeat-



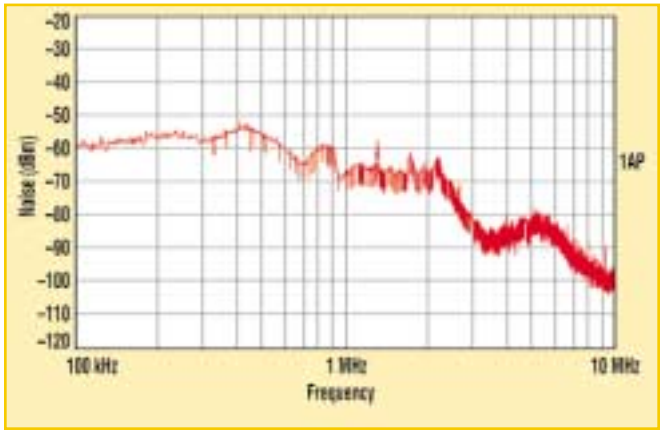
1. To reduce EMI, this conventional step-up dc-dc converter employs spread-spectrum pulse-width modulation (SSPWM) produced by the pseudorandom noise at the clock input.



2. This generator of pseudorandom noise (PN) produces a nominal 325-kHz clock signal for the step-up dc-dc converter circuit in Figure 1.



3. The output-noise spectrum produced by the Fig. 1 circuit operating with a fixed-frequency control scheme contains strong peaks at the clock harmonics.



4. An SSPWM control scheme produces less output noise in the Fig. 1 circuit than the conventional fixed-frequency approach.

ing sequence of ones and zeroes at a nominal frequency of 650 kHz. The D-type flip-flop (U5) divides this frequency by two, producing a nominal 325-kHz spread-spectrum clock signal to the switching regulator.

Bench measurements show a 15-dB reduction in peak power density at about 300 kHz. Except for 9 mA of extra current drawn by the PN generator, the regulator's efficiency remains unchanged. (The efficiency is 94% while delivering 0.5 A with a 3.6-V input and a 5-V output.) Ripple amplitude in the time domain also remains unchanged. Output spectra demonstrate that a conventional fixed-frequency clock *(Fig. 3)* produces considerably more noise than does the spread-spectrum technique *(Fig. 4)*.

Low-Cost Programmable Key Lock Uses A PC-Hardware Monitor IC

Sean Gilmour

Analog Devices, One Technology Way, Norwood, MA 02062

Simplicity is the key to a good security system design. The following is a simple yet powerful security system employing an ADM-1024 PC-hardware monitor as the key's decoder.

The ADM1024 was designed to monitor the local temperature, the die temperature of up to two Pentium processors, and the speed of up to two fans. This device monitors up to seven supply voltages and a 5-bit VID code. It also includes a 10-bit digital-to-analog converter (DAC). In this application, the ADM1024 is used to monitor seven voltages provided by a digital key as well as to open a lock if the correct key is inserted.

The basic principle of this lock decoder is the division of a voltage into seven specific levels that can be measured by the ADM1024. The voltage dividers are embedded in a key that can be inserted into the lock, as shown in the figure. For simplicity, only details relating to the ADM1024 and the key are given in this diagram.

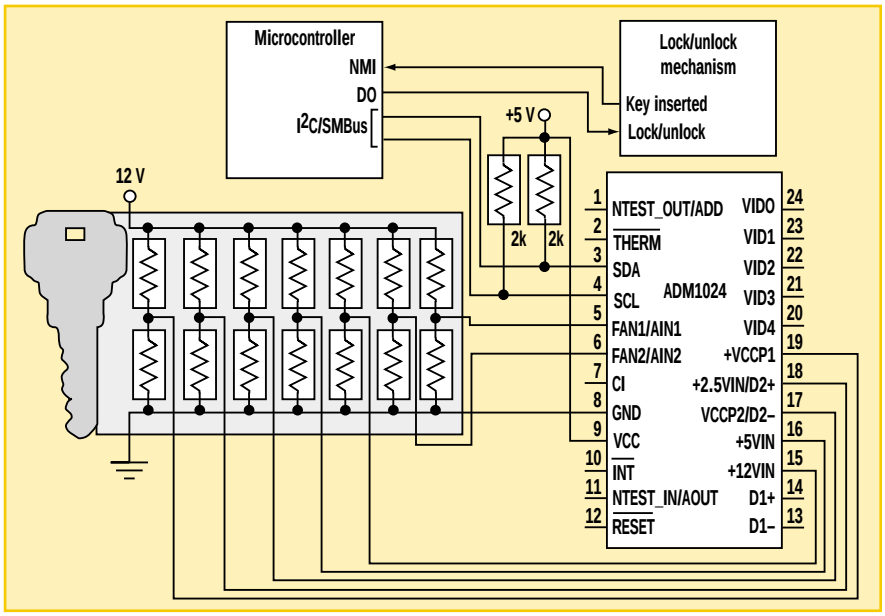
The seven voltage-input channels are each capable of measuring a voltage with 10-bit resolution. However, only eight bits of data are available on the serial bus. Hence, the theoretical maximum number of key combinations is

7.2×10^{16}! The number of different keys is limited to 4.4×10^{12} by practical concerns, the given standard 1% resistor values, and the allowance of a 16-LSB measurement span for each key combination. This is still a very secure system.

In production, keys could be created by vapor deposition of resistive material directly onto a circuit board. Absolute accuracy is not critical since the resistors are used in a voltage divider. Resistors created in a batch will match well, so their ratios can be precisely defined.

The on-board temperature sensor can be used to measure the ambient temperature. This enables the calculation of voltage changes caused by resistor-temperature drift if desired.

This system has several advantages. Only two signal wires are required to communicate with the lock. The first enables the lock to tell the microcontroller that a key has been inserted. The second allows the microcontroller to tell the lock to lock or unlock. The microcontroller can easily process all of the combinations to determine that the correct key was inserted. Keys can be manufactured at a relatively low cost and can be authenticated in milliseconds. The enormous number of possible combinations makes this key decoder very secure.



The ADM1024 finds an unusual use for its power-supply-monitor inputs in the detection of the seven analog voltages produced by the low-cost key.

ifd winners

W. Stephen Woodward, University of North Carolina, Marine Sciences. The idea: "*Circuit Enables Precision Control In Radiant Heating Systems*." January 8, 2001.

William Donofrio, Nu-Products, 1393 Hawkerest Cove S., Cordova, TN 38018. The idea: "*12-Bit Data Recorder Downloads Results To A PC*," January 22, 2001.

W. Stephen Woodward, University of North Carolina, Marine Sciences. The idea: "*One Single-Section Potentiometer Sets The Gain On Two Channels*," February 5, 2001.

W. Stephen Woodward, University of North Carolina, Marine Sciences. The idea: "*Tunable Diode Laser Photocurrent Amplifier Has 80-dB Logarithmic Gain*," February 19, 2001.

Len Sherman, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. The idea: "*Compact, Inductorless Boost Circuit Regulates White LED Bias*," March 5, 2001.

READER SERVICE 112

Noncascaded Arrangement Optimizes Bridged Amplifiers

John Guy and Joe Neubauer

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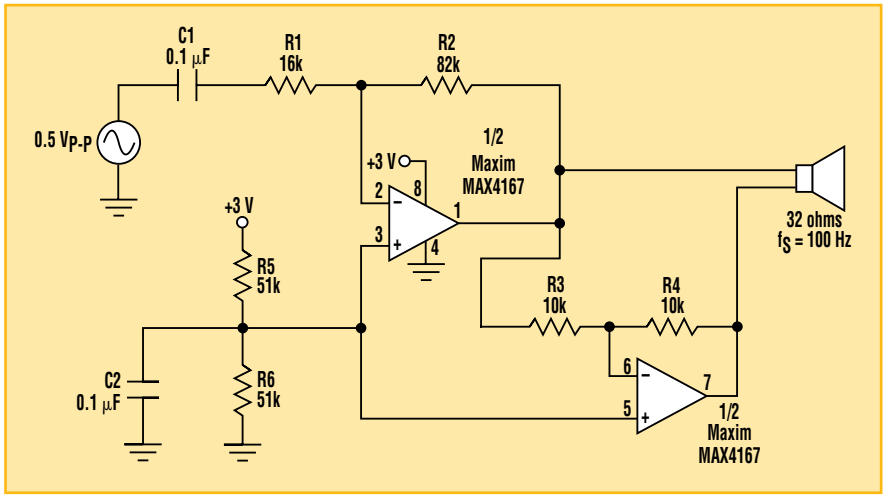
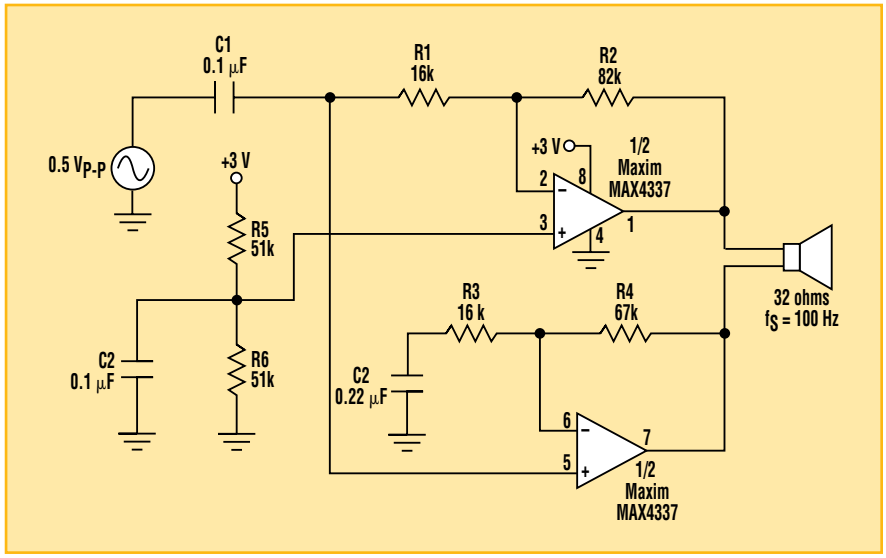
Low-voltage systems that drive loudspeakers often employ a bridged-amplifier configuration that effectively doubles the voltage swing at the transducer (speaker).

In a typical bridge-amplifier circuit, an ac-coupled inverting stage with gain is used to drive one side of the speaker *(Fig. 1)*. This stage also drives a second unity-gain inverting amplifier. This amplifier, in turn, is used to drive the other side of the speaker.



1. This conventional bridged amplifier features two matched amplifiers in tandem.



2. This circuit optimizes the configuration in Fig. 1 by distributing gain between the two amplifiers. The elimination of dc gain in the noninverting amplifier also improves the design.

Usually, bridged amplifiers incorporate a matched pair of amplifiers. Yet in this configuration, the first amplifier dominates the overall performance since its output noise and distortion are replicated in the second amplifier.

This drawback can be eliminated by placing the two amplifiers in a noncascaded configuration. While one is inverting, the other is noninverting *(Fig. 2)*. Since both amplify the same input signal, neither amplifier reproduces the noise, distortion, or clipping introduced by the other amplifier.

An additional improvement to the design in Figure 1 is the bias arrangement in the Figure 2 circuit. In this circuit, the dc bias for the noninverting circuit is derived from the inverting amplifier's source resistor (bias is required because the input is ac-coupled). Using the inverting amplifier's source resistor as a bias source lowers the component count and eliminates signal injection into the high-impedance bias source ($V_{CC}/2$ applied to the top amplifier's noninverting input).

Another advantage of the circuit in Figure 2 is the elimination of dc gain in the noninverting amplifier. For the circuit shown, C2 sets the –3dB point at half the input cutoff frequency. R1/C1 sets the input high-pass cutoff frequency at 100 Hz.

Thermostat For High-Altitude Atmospheric Sampler Is Fault-Tolerant

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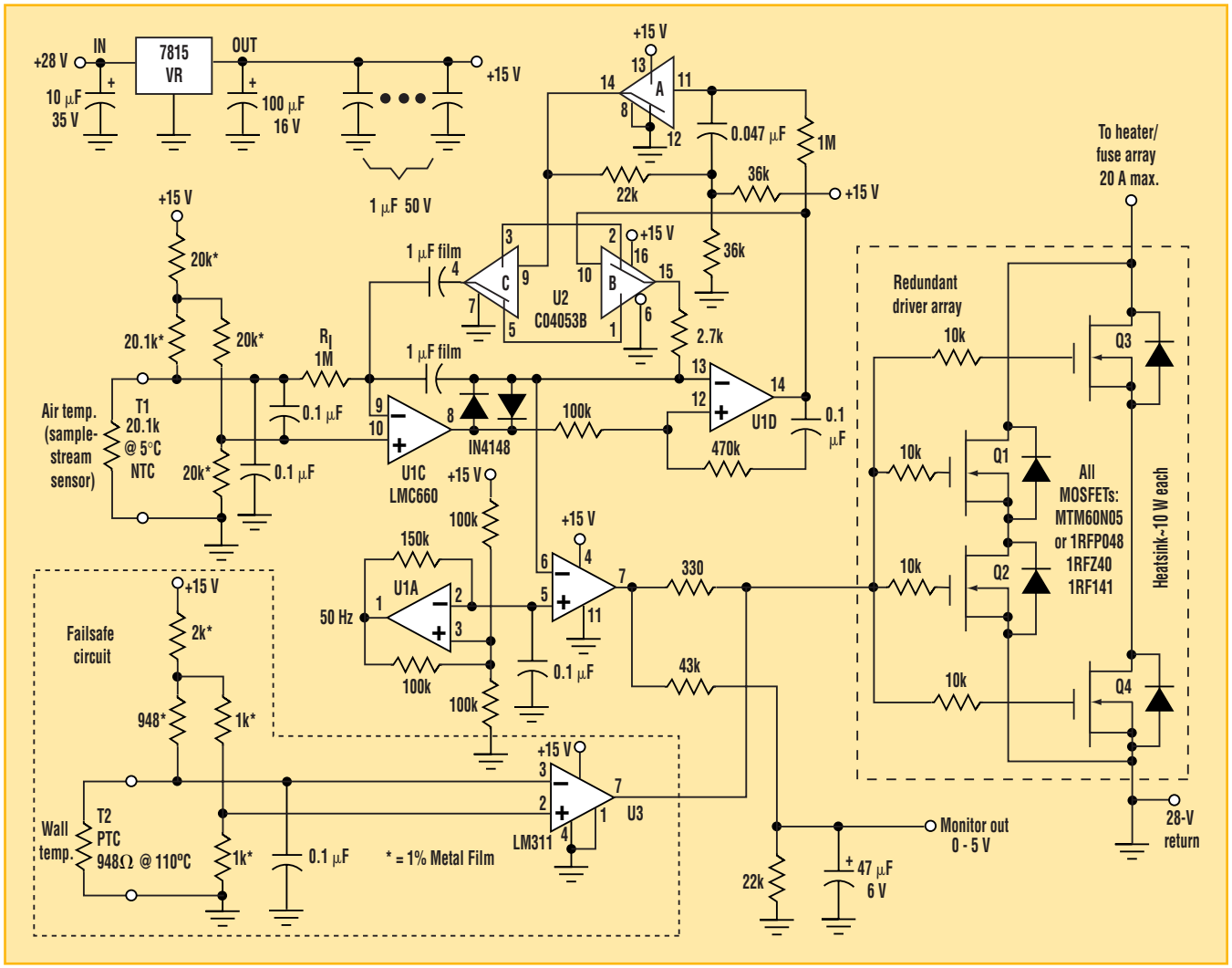
Among the many measures of good circuit design (e.g., cost, performance, and efficiency), none is more important than reliability. Usually, adequate expected reliability can be achieved by simply sticking to conservative design rules and good engineering practices. Yet in some critical applications, "any" unnecessary risk of failure may be unacceptable. At the same time, the trouble and cost of exhaustive environmental and life-cycle testing may be difficult to justify for one-of-a-kind research instruments. In these cases (like the one shown here), special design-in-depth tactics may be the most cost-effective route to adequately bulletproof system designs.

In this example, an atmospheric analysis apparatus carried aboard a NASA ER-2 high-altitude aircraft is used in ozone-layer depletion research. This device incorporates an electrically heated, constant-temperature air-sampling probe. The probe warms the incoming air stream from the stratosphere (ambient temperatures from −70 °C to 5 °C, ±1 °C) for input to a laser spectrometer. The large delta-T (about 75 °C) and high flow rate (tens of liters per second) involved in this application dictate large heater power inputs—around 400 W. Consequently, any failure of the heater control circuits would risk severe thermal probe damage. Even if permanent probe damage doesn't occur, in-flight thermostat failure would cause the loss of valuable scientific data and waste very expensive aircraft flight time.

To prevent these calamities, this design incorporates several backup provisions in the heater-control circuit-



This heater-control design incorporates several backup provisions for improved reliability, including parallel MOSFET outputs and a probe-wall overtemperature monitor.

ry. The central principle of operation of the thermostat is an analog implementation of the "Take-Back-Half" (TBH) algorithm *(see "Take-Back-Half: A Novel Integrating Temperature-Control Algorithm," ELECTRONIC DESIGN, December 4, 2000; "Circuit Enables Precision Control In Radiant Heating Systems," January 8, 2001; and "Linear-RMS Phase Control Improves Thyristor-Based Thermostat," March 5, 2001)*.

The temperature of the sampled air stream is sensed by T1, an NTC thermistor. The resistance of T1 will equal 20.1 kΩ when the sample-stream temperature equals the 5°C setpoint, resulting in bridge balance. At any other sample-stream temperature, the voltage at the common node of T1 and the 20.1-kΩ reference resistor will not equal the voltage at pin 10 of U1C. This imbalance will cause an error current to flow through R_T to the TBH integrator formed by U1C and the 1-μF feedback capacitor. The resulting charge accumulation will cause pin 6 of U1B to ramp down for stream temperatures below the setpoint, and up for temperatures above the setpoint.

U1B compares the integrated error voltage to the 5-V p-p, 50-Hz triangle waveform produced by U1A. This comparison produces a square wave at U1B-pin 7, with a duty cycle that increases as the integrated error signal decreases. U1B's output is applied to the MOSFET array, resulting in an average heater power that can proportionate from 0 to 400 W in response to the integrator. Thus, the average heater power will gradually increase when the stream temperature is below the setpoint, and decrease when the temperature is too high. The net result is to drive temperature deviations toward the setpoint, as any good thermostat should. Meanwhile, the TBH principle forces steady-state convergence.

To enhance reliability, four MOSFETs are used for heater power switching where one would theoretically suffice. This lets the MOSFETs be arranged in a redundant series-parallel topology that permits uninterrupted operation even with any single MOSFET open and/or any single MOSFET shorted. As further safety backup to prevent overheating damage to the probe in the event of thermostat runaway, thermal override comparator U3 monitors the probe's wall temperature. The U3 override function will take over the degraded (but still useful) control of the heater drive if a primary U1 control-loop failure should ever allow the probe wall to heat beyond 110°C.

"Manually Operated Digital Pot" Is Revisited

Yongping Xia

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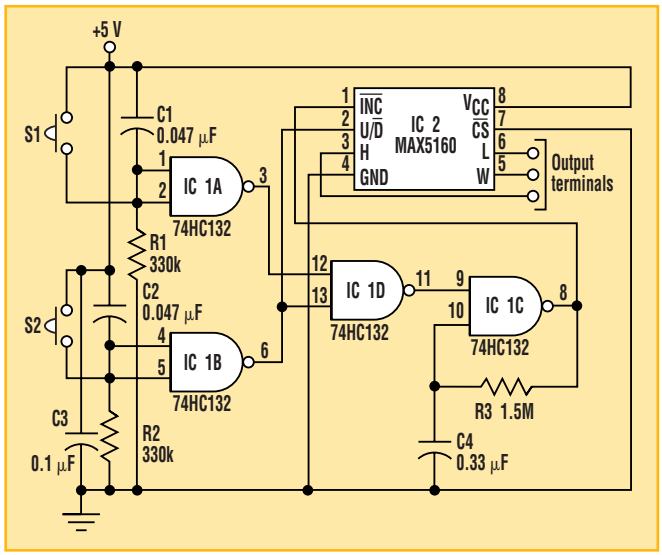
CIRCLE 522

An idea for design published in the April 2, 2001 issue, "Manually Operated Digital Pot Doesn't Need A Microprocessor," uses two proprietary ICs to manually control a digital potentiometer. After reviewing this design, a simpler solution came to mind. This solution employs a commonly used IC with fewer components, resulting in a much lower cost *(see the figure)*.

IC1 is a quad, two-input NAND Schmitt trigger. IC1A, R1, and C1 form a debouncer for S1. Switch S2 is debounced by IC1B, R2, and C2. IC1C, R3, and C4 form an oscillator that's used as the clock signal for the digital pot. The oscillator is controlled by the status of S1 and S2 through IC1D. If no switches are pressed, both inputs of IC1D remain at logic high. This causes IC1D to output a logic low, which inhibits oscillation. The output of IC1C remains at logic high. When S1 or S2 is pressed, IC1D's output becomes high. This change generates a high-to-low transition on IC1C's output. This transition forces IC2 to increase or decrease the wiper position of the pot by one step.

Holding down either S1 or S2 will allow the oscillator to continue running, stepping the pot's wiper position continuously. The oscillation frequency is around 3 Hz. Since the increase or decrease of the wiper position is controlled by the output of IC1B, pressing or releasing S2 determines the pot's direction.



This simpler manual-control design for a digital pot uses less expensive, second-sourced components.

ifd winners

Elliott Simons, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. The idea: *"Negative-Resistance Load Canceller Helps Drive Heavy Loads,"* March 19, 2001.

Ken Yang, Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086. The idea: *"Manually Operated Digital Pot Doesn't Need A Microprocessor,"* April 2, 2001.

Victor Koren, Tioga Technologies, 32 Nachalat Yitzhak St., Tel Aviv 67448 Israel. The idea: *"Programmable-Gain Amp Uses Arbitrary-Attenuation Step Ladder,"* April 16, 2001.

Iikka Marttila, VTT Information Technology, Otakaari 78, P.O. Box 1201, FIN-02044 Espoo, Finland. The idea: *"Second-Order Audio Filter Performs Multiple Functions,"* April 30, 2001.

Simple LED Flasher Yields 99% Power Reduction

Clayton B. Grantham

CIRCLE 520

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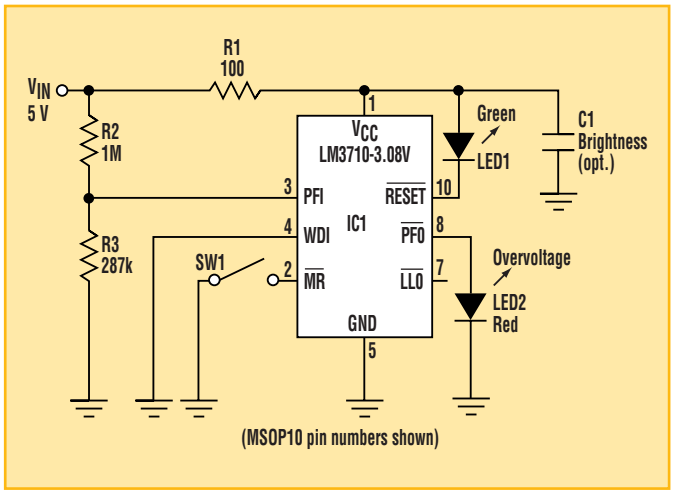
e-mail: clayton.grantham@nsc.com

An LED is commonly used as a "power on" indicator for many electronic devices. For the LED to produce discernible visible light in daylight, the forward-bias current needs to be in the moderate range (10 to 20 mA). This amount of current may be too large for many low-power designs. Also, it results in wasted power. All that is needed in most cases is a once-in-a-while or on-demand indication that there is power to an electronic device. In Figure 1, National Semiconductor's LM3710, a supervisory circuit, is configured to reduce the power consumption of a traditional LED indicator by 99%.



1. This controller blinks the green "Power-Good" LED1, resulting in less than a 0.2-mA average current drain.

When V_{IN} is above 4.4 V, green LED1 blinks on for 200 ms and off for 25.6 s, repeatedly. IC1's reset timeout pulses the LED1 on for 200 ms. This 200-ms on period is customizable from 1.4 to 1600 ms at the factory. The LED1 off period is controlled by IC1's watchdog timeout period, which is also customizable from 6.2 ms to 25.6 s.

The watchdog input monitors transitions at WDI. If there are no changes at WDI, then the reset engages. The WDI in Figure 1 is grounded to prevent a change. Thus, the reset timeout and watchdog timeout form two one-shots that produce a repetitive pulse train. The 25.6-s pause between the LED1 flashes can be short-cycled by pressing the momentary switch, SW1.

LED1's current is limited by IC1's RESET pin, which is approximately 13 mA. The 28-µA quiescent current of IC1 can be ignored. The approximate V_{IN} set-point equation to initiate blinking is:

$$V_{IN(BLINK)} = 3.08\ V + R1\ (I_{RESET})$$

where

$$I_{RESET} = 13\ mA$$

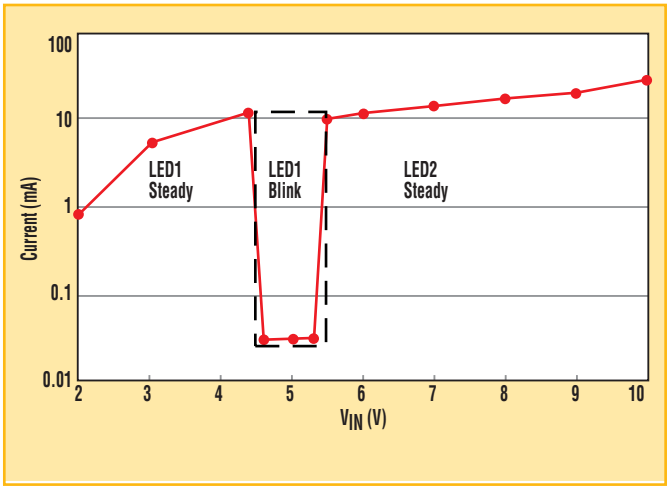
(for R1 < 200 Ω)

The average current in LED1 is reduced by the ratio of the two time intervals. A 13-mA continuous bias current would be reduced to 0.1 mA in average LED1 current—a 130× power savings.

If V_{IN} goes above 5.5 V, red LED2 illuminates as an overvoltage indicator. The resistor divider of R2 and R3 and the PFI input of IC1 set this power-fault level. IC1's PFI threshold voltage is 1.225 V. This overvoltage condition causes the PFO output to drive LED2 continuously. The V_{IN} set-point equation to initiate an overvoltage condition is:

$$V_{IN\ (OVERVOLTAGE)} = (1.225\ V)(R2 + R3)/R3.$$

In the brief time before V_{IN} reaches 4.4 V, the LED1 is on continuously. Figure 2 shows the current-voltage waveform of the circuit.



2. The average input current becomes very low for input voltages between 4.5 and 5.5 V.

Here are a couple of other

examples. For a 5-V, ±5% monitor, set R1 = 121 Ω and R3 = 301 kΩ. For a 3.3-V, ±10% monitor, set R1 = 0 Ω and R3 = 511 kΩ. Keep the absolute maximum ratings of IC1 in mind during the design.

An optional capacitor, C1, can be added to provide an energy reservoir that will increase the brightness of LED1's flash and its average current. Values in the microfarad range are needed to create a noticeable change.

Universal Impedance Generator Handles Biomedical Applications

Saurav Gupta

Linear Integrated Circuit Lab, NSIT, New Delhi, India

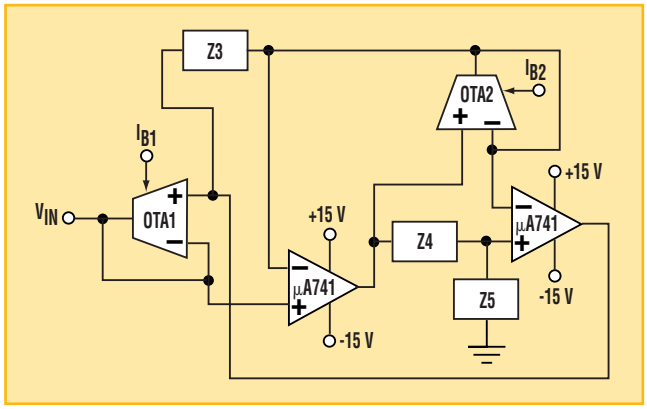
Components like inductors and capacitors constitute an integral part of filters and oscillators used for communication and biomedical applications. A common problem intrinsic to passive inductors is their enormous size as their value increases. Efforts have been made to actively simulate such passive devices.

In biomedical applications, various filter and oscillator structures need to operate at very low frequencies (less than 50 Hz). Brain-wave frequencies are typically in the low-Hertz range (e.g., Delta: 0-4 Hz, Theta: 4-8 Hz, Alpha: 8-12 Hz, Beta1: 14-16 Hz, Beta2: 16-20 Hz, etc.). Hence, very high-value inductors and capacitors are often required when designing devices such as EEG instruments.

To achieve such high values (e.g., greater than 1000 H) using conventional impedance simulating circuits, very high-value resistors would be needed. This is not feasible for integrated circuit technology.

An economical and versatile circuit is presented here that can simulate high-value, grounded inductors. It can also function like an impedance multiplier/scalar. In addition, this arrangement provides the added advantage of tunability, since a wide range of values can be achieved without disturbing the design. The design, as shown in Figure 1, is robust and economical. It uses a commonly available dual transconductance op amp (OTA) chip from National Semiconductor (LM13600) and off-the-shelf μA741 op amps. With G_M as the OTA transconductance, the input impedance of the circuit is:

$$V_{IN}/I_{IN} = Z_5/(G_{M1}G_{M2}Z_3Z_4)$$



1. This arrangement is used to realize an input impedance given by $Z_5/(G_{M1}G_{M2}Z_3Z_4)$. I_{B1} and I_{B2} are the OTA bias currents.

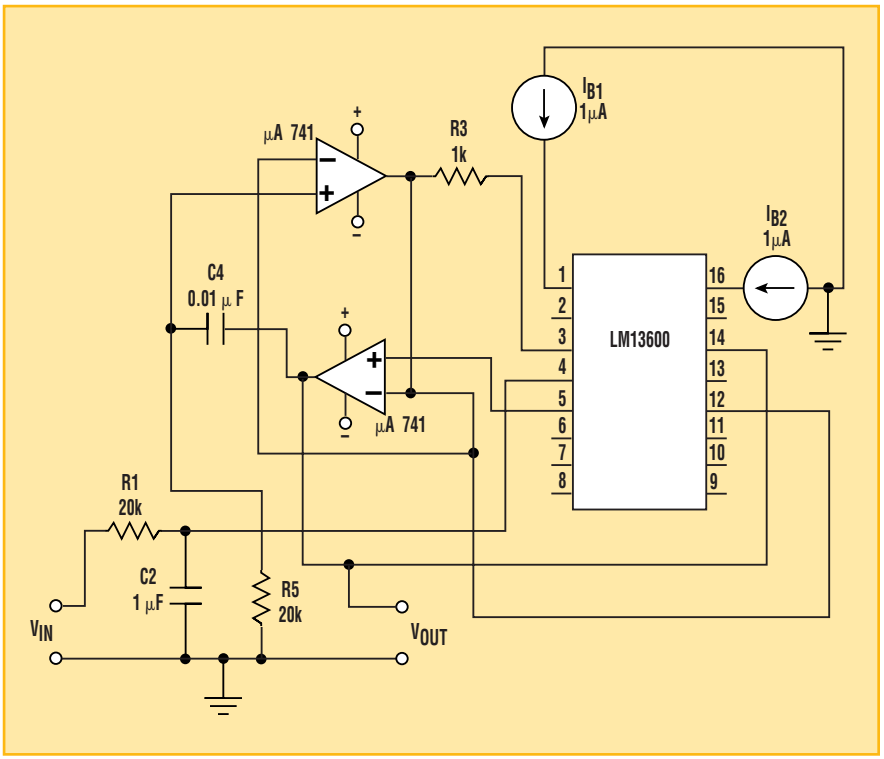
where Z_I can be resistors or capacitors and

$$G_M = I_B/2V_T$$

where I_B is the OTA bias current.

Since G_M can be varied theoretically up to six decades (per datasheet), the overall impedance function can be varied up to 12 decades. This yields a possible multiplication factor of nearly 2.5×10^{11}.

Figure 2 shows a bandpass filter (BPF), using this scheme, which is very useful when designing EEG instruments. Though the BPF has been configured to pass Theta-type waves (associated with lifelike imagination, particularly dominant in children), the



2. This prototype bandpass filter was designed to pass Theta waves in EEG applications. The filter's f_C is approximately 7 Hz, and its Q factor is about one.

intuitive use of OTA for design makes it possible to program the filter for any wave frequency by simply tuning the bias current.

With the component values shown, the filter yields a center frequency of approximately 7 Hz and a Q factor of about one.

The OTA amps are biased with 1-µA currents. (Widlar-type current mirrors are capable of supplying such low currents while using nominal resistor values). It should be mentioned that, although the scheme synthesizes grounded impedances, the circuit can easily be converted into a floating structure using only an additional OTA and an on-chip buffer (This grounded-to-floating conversion method is attributed to Prof. Raj Senani).

Single-Gate VHF Temperature Transmitter Runs On 3.6 V

Shyam Sunder Tiwari, DE

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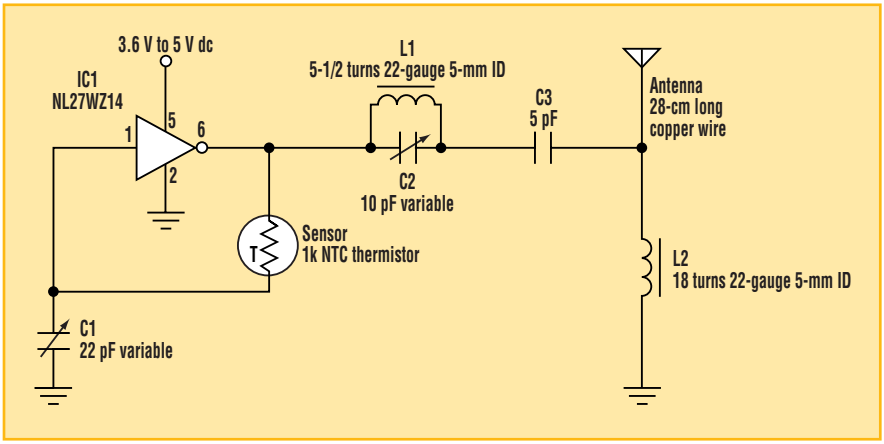
CIRCLE 522

This design idea illustrates what may be the simplest and smallest temperature transmitter in the VHF 50- to 100-MHz range. As seen in the figure, the design employs an ON SEMI single-gate IC (NL27WZ14). The sensor is a negative-temperature-coefficient 1-kΩ SMD thermistor. It causes an increase in the oscillator frequency as temperature increases. Since the design of the circuit is not critical, the value of C1 can be selected high enough to lower the transmission-frequency band down to 1 MHz if necessary. The thermistor-resistance value, however, is critical and should not exceed 3 kΩ. If the resistance value exceeds this limit, the circuit may not oscillate properly.

The data is transmitted as a slowly modulated FM signal (i.e., the frequency shifts as temperature changes). Therefore, rapid signal modulations, typical in audio FM receiver systems, are not involved in this design. At the receive end, the receiver locks on to the transmission frequency and monitors the frequency variation directly as the temperature signal. C1 must not have a positive temperature coefficient or frequency compensation will be required to cancel the temperature dependency in the R1C1 time constant.

To limit the size of the transmitter, a small wire hanging from the tiny pc board is used as the antenna. Other types of antennas may also be used.

Since this circuit draws less than 10 mA from a NiCd cell, its operating time with a small cell is reasonably high (i.e., a few days). Power can also be supplied from other types of cells in the 3- to 5-V dc range.



The values of L1 and C1 are tuned to the center frequency of the desired transmission band.

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Clive Bolton and Ken Sinclair, Bolton Engineering Inc., Melrose, MA 02176. The idea: *"PLD Code Implements Arbitrary CRC Function,"* May 21, 2001.

W. Stephen Woodward, University of North Carolina, Marine Sciences. The idea: *"Decompensated Op-Amp Gain Is Adjustable From Zero To Open-Loop,"* June 4, 2001.

W. Stephen Woodward, University of North Carolina, Marine Sciences. The idea: *"'Take-Back-Half' HVAC Thermostat Is Precise And Energy Efficient,"* July 9, 2001.

Elliott Simons, Maxim Integrated Products. The idea: *"One Resistor Takes The Heat From Single-Supply Op Amps,"* July 23, 2001.

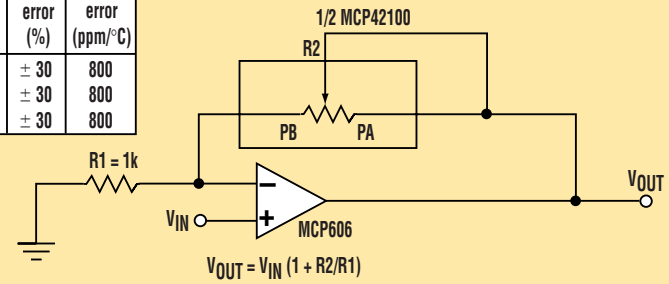
Dual Digital Pot Creates Accurate, Temperature-Stable Amp

Bonnie C. Baker

Microchip Technology Inc., 2355 West Chandler Blvd., Chandler, AZ 85224; (480) 792-7200; fax (480) 792-9210

Programmable Gain Range				
Digital Code	R2* value (kΩ)	Gain* (V/V)	Initial* error (%)	Temp. error (ppm/°C)
3	1.17	2.17	± 30	800
127	49.6	50.6	± 30	800
255	99.6	100.6	± 30	800

* assuming $R_W = 0$



1. The thermal performance of a simple gain circuit using a digital potentiometer in this configuration is typically 800 ppm/°C.

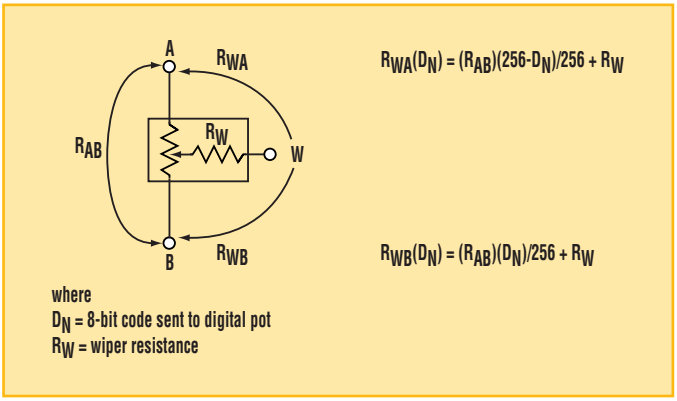
Digital potentiometers enable systems designers to program resistive values in the circuit during initial calibration or even later on, during normal operation of the circuit. This ability permits the dynamic alteration of the circuit conditions, creating a "smart" analog system that can respond to the surrounding environment. In fact, the programmability feature seems all too promising; as usual, suspicious analog engineers will expect that this advantage is not for free. And, they are right.

Initial examination of the temperature performance of today's array of digital potentiometers shows that the devices perform with much less accuracy than the standard mechanical potentiometer or discrete resistor combinations. Certainly, the temperature performance of these digital potentiometers is much less than ideal.

But, the clever designer can take advantage of secondary temperature behavior by using the matching characteristics of these devices. The resistive material of current digital potentiometers is predominantly fabricated with the poly-diffusions (soon to be nichrome) of CMOS processes. Because these resistors are manufactured using poly-diffusions, the resistive elements are not trimmed precisely. Consequently, the initial accuracy of the digital potentiometer from part to part at room temperature is ±30% maximum. The thermal-drift specifications for these types of diffusions are either 800 or 500 ppm/°C, depending on the poly level used for the resistive element. With these specifications, it is easy to see that the simple gain circuit shown will have poor performance over temperature *(Fig. 1)*.

In the circuit in Figure 1, the noninverting gain is established using a standard resistor for R1 and a 256-tap, 100-kΩ digital potentiometer (an MCP42100 from Microchip Technology) positioned as R2. The gain of this circuit is determined by the ratio of R1 and R2 as stated in the formula in Figure 1. The amplifier (an MCP606) is a single-supply CMOS amplifier with a low offset voltage (± 250 µV, max.) and high input impedance (1 pA, typical at 25°C). The lower offset of this amplifier allows for gain changes with a minimal increase in offset errors translating to the output of the amplifier.

The key specifications of the digital potentiometer in Figure 1 in regard to this application are the nominal initial resistance (100 kΩ ±30%, max.) and the change in resistance over temperature (800 ppm/°C, typical). Both of these specifications can cause a significant error in the system, limiting the applications for this circuit. The nominal resistor values of this digital potentiometer are easily calculated using the formulas shown in Figure 2.

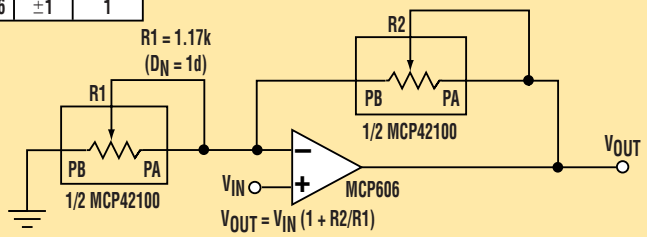


2. The resistance values of the digital pot can be defined as shown.

An alternative circuit that addresses both the accuracy and temperature-performance issues of the Figure 1 circuit is shown in Figure 3. In this circuit, a dual digital potentiometer is used to fill

Programmable Gain Range				
Digital Code	R_2^* value (kΩ)	Gain* (V/V)	Initial* error (%)	Temp. error (ppm/°C)
3	1.17	2.17	±1	1
127	49.6	50.6	±1	1
255	99.6	100.6	±1	1

* assuming $R_W = 0$



3. The intrinsic matching of a dual digital pot is used to achieve an initial gain accuracy of ±1% (max.) and a typical temperature coefficient of 1 ppm/ °C.

both resistor positions in the circuit. Since both resistor elements are on the same IC, their nominal matching and temperature-drift characteristics are closely matched.

Now, instead of an initial gain accuracy of ±30%, the initial gain accuracy of the circuit becomes ±1% maximum. The gain accuracy over temperature is also tightened with this topology from the previous typical performance of 800 ppm/°C to 1 ppm/°C.

With a little attention to circuit design detail, the temperature behavior of digital potentiometers can be optimized using these simple design techniques.

Multiple Serial Devices Interface To The I²C Bus

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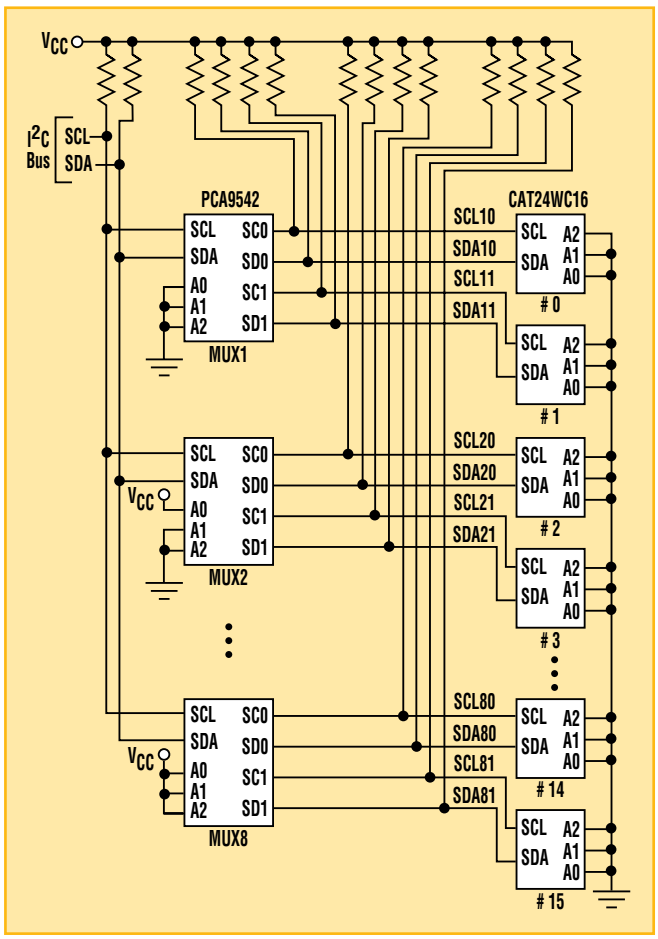
CIRCLE 521

The circuit shown can be used to interface multiple serial devices to the I²C bus, even if they lack the extended-addressing capability required.

Information transfer between I²C devices connected to the I²C bus requires two signals: serial data (SDA) and serial clock (SCL). A device connected to the bus can operate as a transmitter or a receiver. A master device initiates a data transfer on the bus, generates clock signals, and terminates the transfer. A device addressed by the master is considered to be a slave. To connect devices on an I²C multimaster bus, the SDA and SCL lines must be bidirectional and connected to a positive supply voltage through pull-up resistors.

In I²C-bus addressing, the first byte after a START condition determines the slave selected by the master. The slave address (upper 7 bits) is usually made up of a fixed and a programmable part. The eighth bit (the least significant bit) determines the direction of the transfer: read or write. The programmable part of the slave address determines the maximum number of identical devices that can be connected to the I²C bus.



Multiple non-I²C-addressable serial devices, like these CAT24W16 serial EEPROMs, can be interfaced to the I²C bus using Philips PCA9542 I²C multiplexers.

This circuit suits applications in which several devices that lack extended addressing capability (in this case, serial EEPROMs) must be connected over an I²C bus. The circuit also proves useful when there is a need to connect more devices than the maximum number allowed by the devices' address pins.

By multiplexing the SDA and SCL bus lines of connected devices, multiple I²C devices with the same address can be accessed. The figure shows 16 noncascadable CAT24WC16 EEPROMs accessed by using eight, two-channel I²C multiplexers. The Philips PCA9542 is a bidirectional, 1-of-2 multiplexer that is controlled over the I²C bus. It has three address pins.

The circuit MUXi connects the I²C bus lines, SDA/SCL, to either the SDAi0/SCLi0 or SDAi1/SCLi1 channel (where i = 1 to 8). No false conditions

are generated at the time of connection because the channel becomes active when the I^2C bus lines are in a high state.

The I^2C bus commands used to control the hardware are:

1. Send the multiplexer slave address, 1110 xxx (where xxx = 000 to 111) with R/W = 0.
2. Send multiplexer command code to select the channel: xxxx x100 for channel 0; xxxx x101 for channel 1.
3. Send or read data to/from the EEPROM connected to the selected channel.

C++ Program Offers Versatile Waveform Spectral Analysis Tool

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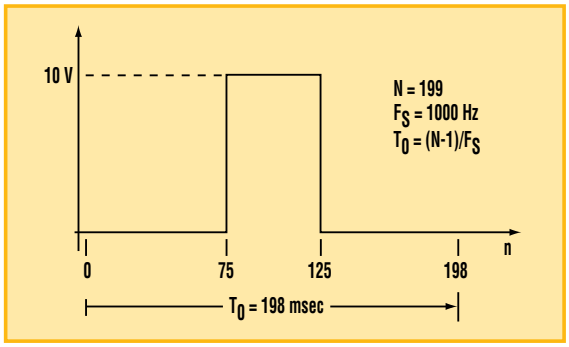
CIRCLE 522

This idea presents a C++ program that uses the complex class, which enables complex arithmetic. The Discrete Fourier Transform (DFT) is applied to the waveform stored in a disk file—a real sequence of double-precision floating-point binary values. (The program listing is available at *www.PlanetEE.com*. Follow the Ideas for Design link.)



1. To demonstrate the program, an input 50-ms pulse was created and fed into the program.

The function dft( ) performs a DFT on the real sequence of N samples in Datain(n) and outputs the resulting spectra in the complex array Dataout(k). The program is set up for a 1024-point DFT; however, this can be altered by revising MAXPTS.

The transform is given by:

$$\text{Dataout}(k) = \frac{1}{F_S}\sum_{n=0}^{N-1}\text{Datain}(n)e^{-j2\pi\frac{kn}{N}}$$

for k = 0 to N – 1 and F_S = sample frequency in Hertz.

The real frequency, F, is related to the index k by $F = kF_S/N$, where the frequency spacing is F_S/N. The DFT generates both real and image frequencies. From the Nyquist sampling criterion, $kF_S/N < F_S/2$, where the real frequencies are $k < N/2$ and the image frequencies are $k \geq N/2$. The real and image frequencies have conjugate symmetry—i.e., Dataout(k) = conjugate[Datain(N – k)] for real sequences.

An example 10-V, 50-ms pulse waveform is shown in the figure. Three *for( )* loops will generate this waveform:

```
for(n = 0; n < 75; n++) a(n) = 0.0;
for(n = 75; n < 125; n++) a(n) = 10.0;
for(n = 125; n < 199; n++) a(n) = 0.0;
```

To test your program, in the main( ) function, block out the disk operations and add the for( ) statements. The representative waveform characteristics of power, energy, and voltage are shown in Figure 2. In addition to amplitude, the spectra, power, energy, and voltage spectral densities of the example pulse waveform are shown. The frequency band (k_low, k_high) is user-selectable, allowing calculation of in-band characteristics.

Note that the program is set up to handle odd values of N, which generates the same number of real and image frequencies. However, the program will accept even values of N and will make the required adjustment in the value of N.

A 1024-point DFT was run on the 120-MHz Pentium I and a 350-MHz Pentium II. The respective run times were approximately eight and two seconds. For slower platforms, a run indicator is included.

```
POWER, ENERGY, AND VOLTAGE
k_low = 0 to k_high = 99 (497.48 Hz)
P_DC = 6.313 watts;     E_DC = 1.256 joules;     V_DC = 2.513 volts
P_TOT = 25.126 watts;   E_TOT = 5 joules;        V_RMS = 5.013 volts

AMPLITUDE SPECTRA AND DENSITIES
k = 1 (5.025 Hz)
complex-amplitude spectra = (-0.450, 0.0)
magnitude = 0.450 volt-secs;   angle = -3.142 radians
PSD = 1.016 watts/Hz
ESD = 0.202 joules/Hz
VSD = 1.008 volts/√Hz
```

2. The DFT results of the sample pulse waveform in Figure 1 are shown.

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```
// A Versatile Waveform Spectral Analysis Tool Author:  Frank N. Vitaljic, Bellingham, WA
// C++ Source Code Listing.
// Calculate and display average power, energy, rms voltage; complex-amplitude,
magnitude/angle
// spectra; and power, energy, voltage spectral densities of real data sequences.

#include        <iostream.h>                            // header files
#include        <stdio.h>
#include        <complex.h>                             // Borland C++ compiler
#include        <conio.h>
#define   MAXPTS     1024              // maximum number of data points,
                                                                  // can be
increased or decreased
void power ( complex [], int, double );         // function prototypes called
void spectrum (complex [], int, double);        // by dft( ) function

// discrete Fourier transform (DFT)
void dft (double Datain[ ], complex Dataout[ ] )
{
double Fs; int k, n, N;                 // Fs=sample freq, k=freq index,
complex j (0, 1) ;                      // n=data array index, N=size of DFT
                                        // real data points
                                        // square root of -1 (constructor)
cout <<  " \nMust be less than or equal to " << MAXPTS;
cout <<  " \nEnter number of real data points: ";
cin  >>  N; if ( N%2 == 0 ) --N;        // make N odd
cout <<  " \nEnter sample rate in Hertz: ";
cin  >>  Fs;
cout <<  " \nCalculating Discrete Fourier Transform..... ";
cout <<  " \nFor frequency indices k = 0 to k = " << (N-1)/2;
cout <<  " (" << (N-1)*Fs/(2.0*N) << " Hertz)\n" << "Run Indicator: "

for (k = 0; k <= (N-1)/2; k++)
{
        Dataout [k] = complex (0);
        for (n = 0; n < N; n++)
        {
                Dataout(k] += Datain[n] * exp (-j*2.0*M_PI*k*n/N);
        }
        Dataout[k] /= Fs;                       // true time-base scaling
        if (k % 8 == 1) cout << '#'; // DFT Run Indicator
}
power(Dataout, N, Fs);                  // calculates power, energy, voltage
spectrum (Dataout, N, Fs);      // complex-amplitude spectra,
                                                        // spectral densities
} // end of  dft()

void power (complex X[ ], int N, double Fs)
{
double          Pdc,   // DC power in watts
Edc,   // DC energy in joules
Vdc,   // DC voltage in volts
Ptot,  // total avg power from k_low to k_high
Etot,  // total energy from k_low to k_high
Vrms;  // volts rms in band k_low to k_high
int     k, k_low, k_high; // frequency bands

Pdc = (Fs/N)*(Fs/N)*norm (X[0]);
Edc = Pdc*(N/Fs);
Vdc = sqrt (Pdc);
cout << "\n\nPOWER, ENERGY, AND VOLTAGE"
```

```
cout << "\nEnter frequency indices k_low to k_high: "
cin >> k_low >> k_high;
Ptot = 0.0; // initialize Ptot accumulator
for (k = k_low; k <= k_high; k++)
{
if (k == 0) Ptot += Pdc;
else Ptot += 2. 0* (Fs/N) * (Fs/N) *norm (X [k]);
}
Etot = (N/Fs) *Ptot; Vrms = sqrt (Ptot) ;
cout << "\npdc = "  << Pdc << " watts;"  << " Edc = "
< < Edc << " joules;" << " Vdc = " << Vdc   << " volts";
cout << "\nPtot = " << Ptot << " watts;"  << " Etot = "
<< Etot << " joules;" << " Vrms = " << Vrms << " volts";
// end of power( )

void spectrum (complex X [ ] , int N, double Fs)
{
int k, k-low, k-high; double mag, angle, PSD, ESD, VSD;
cout << "\n\nAMPLITUDE SPECTRA AND SPECTRAL DENSITIES";
cout << "\nEnter frequency indices k_low to k_high; ";
cin >> k_low >> k_high;

for (k = k_low; k <= k_high; k++)
{
mag = sqrt (norm (X [k] ) ); angle = arg (X [k] );
PSD = (Fs/N) * norm (X [k] ); ESD = (N/Fs) * PSD;
VSD = sqrt (Fs/N) * sqrt (norm (X[k] ));
cout <<  "\n\nk = << k << "    " << Fs*k/N << " Hertz";
cout <<  "\ncomplex-amplitude spectra = " << X[k);
cout <<  "\nmagnitude = " << mag << " volt-secs";
cout <<  " angle = " << angle <<    radians";
cout <<  "\NPSD =  << PSD  <<  watts per Hertz";
cout <<  n\nESD =  << ESD  <<  joules per Hertz";
cout <<  "\NVSD =  << VSD  <<  volts per root Hertz";
char key; key = getch( ); // pause, any key to continue
if (key == 'q' || key == 'Q') return; // 'q' or 'Q' to quit
}
} // end of spectrums

void main (void)
{
double  a[MAXPTS];      // real data sequence from disk
char                    filename[80];   // disk filename
complex         b[MAXPTS];      // complex-amplitude spectrum
FILE                    *fp;                    // disk file pointer

cout << "\nEnter disk file name: ";
cin >> filename;                                // [drive:][path]filename
fp = fopen (filename, "rb");    // open disk file
if (!fp)
{
cout << "cannot open file";
return;
}
fread (a, sizeof(double)*MAXPTS, 1, fp); // load a[ ] array
fclose (fp);
dft (a, b); // parameter prompts, calculate DFT, display results
} // end of main( )
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```