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Simple phototimer controls load
Delay line upgrades vintage scope
Circuit reduces negative-voltage stresses on control IC
Track multisite temperatures on your PC

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Printer port activates CMOS switches
Circuit improves on temperature measurement
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Sampling peak detector has shutdown feature
Circuit provides bidirectional, variable-speed motor control
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Supply uses ac to generate 5V, power-on reset
More on two-transistor circuit
Routine automates pattern/sequence detection
Digital potentiometer programs and stabilizes voltage reference
Add voice command to virtual instrumentation
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Power meter is ±1% accurate
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Make a truly linear RF-power detector
Simple circuit provides 5V gate bias from –48V
Circuit provides laser-diode control
One amplifier has two gain figures
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Passive circuit limits inrush current
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Precision circuit closely monitors –48V bus
PLD code reveals pc-board revisions
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Positive regulator makes negative dc/dc converter
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Circuit provides watchdog for microcontrollers
Circuit translates I2C voltages

design ideas

Edited by Bill Travis

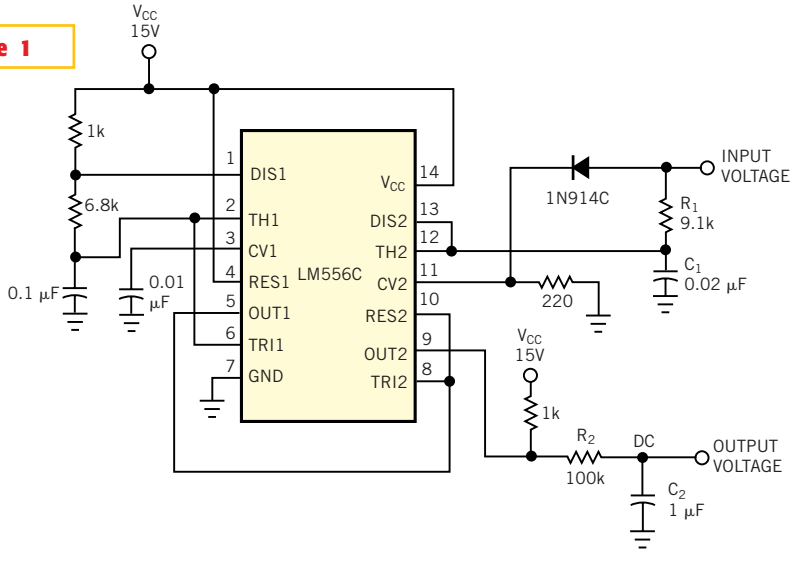
Log amp uses capacitor-charging law

Jayashree Raghuraman and Ajoy Raman, Aeronautical Development Establishment, Bangalore, India

THE NOVEL LOGARITHMIC amplifier in **Figure 1** relies on the exponential charging characteristics of a simple RC circuit. The expression for the time, T, required for a capacitor, C, to reach a voltage ($V_{IN}-V_K$) from 0V, when charged through a resistor, R, with an applied voltage of V_{IN}, is $V_{IN}-V_K=V_{IN}(1-e^{-T/RC})$, where V_K is a fixed voltage. The expression for T reduces to $T=RC\ln(V_{IN}/V_K)$, clearly showing an inherent logarithmic characteristic. The circuit in **Figure 1** demonstrates this characteristic, using a 556 timer. With the values shown, the first stage of the 556 timer is a standard astable circuit operating at a frequency of approximately 1 kHz. The output of this stage acts as the trigger for the second stage. The second stage operates as a modified monostable circuit. In this modified configuration, the RC combination, R_1 and C_1, charges from an external voltage, V_{IN}, instead of V_{CC}. The control-voltage pin, CV2, has the value V_{IN} minus one diode drop, V_K.

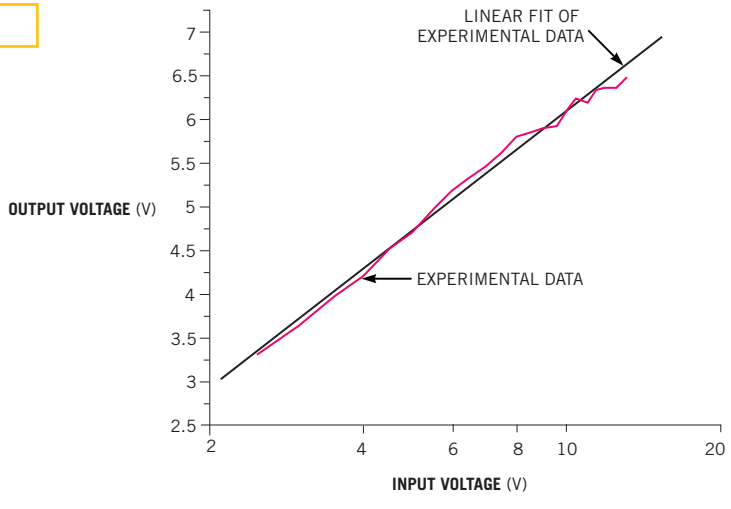
The monostable pulse width, T, then depends on the time required for capacitor C_1 to charge to $V_{IN}-V_K$ through R_1

Figure 1



A simple 556 timer depends on RC charging to form a logarithmic amplifier.

Figure 2



The circuit of Figure 1 produces a distinct logarithmic output.

with the applied voltage V_{IN}. The output of the second stage, filtered through R_2 and C_2, depends on the first stage's astable frequency; the supply voltage, V_{CC}; and the monostable pulse width, T. Because V_{CC} and the astable frequency are constant, V_{OUT} is proportional to T. **Table 1** tabulates the experimental results, and **Figure 2** shows graphical results. The circuit operation is limited to an input range of 2.5 to 13V to satisfy the internal biasing requirements of the second stage of the 556. The diode drop, V_K, is not strictly constant, because it varies with current. In spite of these limitations, **Table 1** and **Figure 2** clearly show a distinct logarithmic characteristic.

TABLE 1–OUTPUT VERSUS INPUT VOLTAGE

Input voltage	Output voltage	Input voltage	Output voltage
2.5	3.324	8	5.782
3	3.667	8.5	5.861
3.5	3.954	9	5.886
4	4.227	9.5	5.945
4.5	4.506	10	6.098
5	4.705	10.5	6.187
5.5	4.956	11	6.204
6	5.151	11.5	6.312
6.5	5.315	12	6.371
7	5.444	12.5	6.378
7.5	5.615	13	6.476

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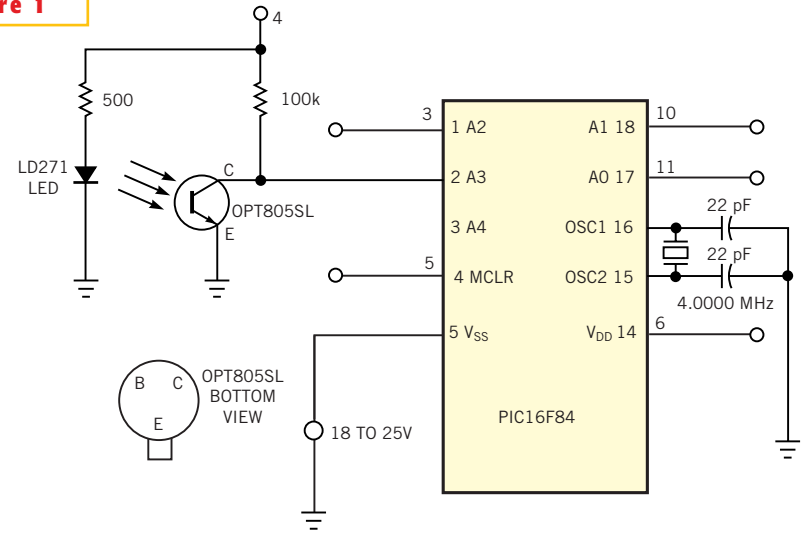
Extend the timing capabilities of a PC

Martin Connors, Athabasca University, Athabasca, AB, Canada

Even when you use the internal timing registers and under DOS, a PC cannot easily measure time intervals with better time resolution than a millisecond. Measuring long intervals with even this precision is a waste of many CPU cycles. A microcontroller is well-suited for this task; you can easily integrate a PIC with a PC to extend the timing precision into the microsecond range for periods from tens of microseconds to more than 24 hours. The flash-programmable PIC16F84 microcontroller from Microchip Technology (www.microchip.com) is an inexpensive and widely used device. The precision timer in **Figure 1** requires only the IC, two capacitors, and a crystal and accepts direct input of timing data to a PC via the parallel port. The PIC16F84 draws only 2 mA and can operate from an output pin in the parallel port without a battery. You can assemble the circuit on a small pc board with a male DB-25 connector glued or soldered to one end for connection to the parallel port, LPT1. In this example, the timing signal occurs when you block a photogate comprising a paired LED and a phototransistor.

Figure 1



This zero-power photogate allows you to use a PC to generate precise timing intervals.

Listing 1 represents the timing application implemented, which comprises two basic parts. The first part waits for a signal and starts a loop that checks the continuing presence of the signal and increments 32 timing bits while the signal is present. The second part transmits 32 bits of timing information to an external device, using one data-output line and two handshaking lines. With a 4-MHz crystal, most instructions take 1 µsec, so the timing loop is 5 µsec long. You can run newer PIC16F84s with a 20-MHz clock, so, in principle, the timing loop can be 1 µsec long. Port A of the PIC serves for the timing signal on bit 3 and for communication. A minor coding change allows you to use positive or negative log-

ic levels. If the timing signal is present at the start of the program, an error flag arises, with an output of 4 bytes of 0xFF. A similar error occurs if the signal is present long enough (roughly a day) to cause overflow of the counter. DATO (data output) occurs through bit 0. The routine uses two handshake lines: VALID on bit 1 from the PIC to signal the presence of valid data on the DATO line and SEND from the PC to bit 2, signifying that the PC is ready to receive data. This robust transmission method does not depend on timing characteristics in a critical way.

Listing 2 (pg 76) shows sample C code for Borland Turbo C for DOS with a simple timing conversion that doesn't take account of the overhead of byte overflow. After the PIC times an event, it waits for the PC to signal that it wants to download data. The transmission protocol for transmitting 1 bit of data is as follows: PC SEND is low, and the PIC polls it. PIC VALID is initially low; the PC raises SEND and polls VALID. In response, the PIC puts DATA on the line. The PIC than raises VALID and polls SEND; in response, the PC reads DATA. The PC then lowers SEND, and the PIC lowers VALID. This operation repeats for 32 bits, starting with the lowest bit of the lowest byte and proceeding to the highest bit of the highest (fourth) byte. Although this transmission method is inefficient, it is robust, and the polling timing is unimportant. The efficiency matters little, because the method involves little data transfer. By referring to the **listings**, you can "step through" the process to see how the transfer takes place. **Listing 2** includes a test routine that allows you to supply a signal from the PC to test the circuit's operation. You can download **listings 1** and **2** from the Web version of this article at *EDN*'s Web site, www.ednmag.com.

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LISTING 1—ZERO-POWER PHOTOGATE-ASSEMBLY PROGRAM

```
;
;
; hardware connections needed are as follows
; PC parallel port connections (see below for software aspect)
; DAT0 pin11, VALID pin 10, SEND pin 2, SIGNAL* is not used but reserve pin 3
; TRANS_ON/LED_ON pin 4 are power output from parallel port
; MCLR* is output from parallel port pin 5 causing reset if low
; Vdd is output from parallel port pin 6 for power
      include "D:\pic\mplab\P16f84.inc"

      __CONFIG    (_XT_OSC & _WDT_OFF & _PWRTE_ON & _CP_OFF)

; Equates
Bank0RAM    equ   20H
DATO        equ   0
VALID       equ   1
SEND        equ   2
SIGNAL      equ   3
; Variables
      cblock Bank0RAM
      BYTE1
      BYTE2
      BYTE3
      BYTE4
      BYTEO
      COUNT8
      endc
;
      org   0000H
      goto  MAINP
      org   0004H       ; should never get here
      goto  OVERFLO           ; error exit if INT
MAINP
      bsf   STATUS,RP0  ; select Bank 1
; PORT A detects signal on Bit 3, communicates with PC on 0-2
; Bit 0 is serial data out (DATA)
; Bit 1 is valid data indicator (VALID)
; Bit 2 is input from PC saying it is ready (SEND)
      bcf   TRISA, DATO ; PORT A Bit 0 output (DATO)
      bcf   TRISA, VALID      ; PORT A Bit 1 output (VALID)
      bsf   TRISA, SEND ; PORT A Bit 2 input  (SEND)
      bsf   TRISA, SIGNAL     ; PORT A Bit 3 input  (signal)
      bcf     STATUS,RP0      ; select Bank 0
        clrf    BYTE1
      clrf  BYTE2
      clrf  BYTE3
      clrf  BYTE4       ; all counter bytes to 0

      bcf   PORTA,VALID ; no valid data for PC

      btfsc PORTA,SIGNAL      ; signal must NOT be on now
      goto  OVERFLO           ; error exit if it is
WAITI btfss PORTA,SIGNAL      ; wait for signal on PORTA
      goto  WAITI
      goto  INC1
INC4  incfsz      BYTE4,F           ; incr BYTE4 if BYTE3 over
      goto  INC1
      goto  OVERFLO           ; if BYTE4 over, error exit
INC3  incfsz      BYTE3,F           ; incr BYTE3 if BYTE2 over
      goto  INC1
      goto  INC4
INC2  incfsz      BYTE2,F           ; incr BYTE2 if BYTE1 over
GTI1  goto  INC1
      goto  INC3
INC1  btfss PORTA,SIGNAL      ; signal still on PORTA?
      goto  SERIAL            ; if gone, transmit results
      incfsz      BYTE1,F           ; incr&test
      goto  INC1        ; if nonzero
      goto  INC2        ; if zero overflow to BYTE2

; three-wire handshake with PC
; byte data is shifted out on PORTA DATO lowest->highest
SERIAL
      movf  BYTE1,W
      movwf BYTEO
      call  BYTOUT
      movf  BYTE2,W
      movwf BYTEO
      call  BYTOUT
      movf  BYTE3,W
      movwf BYTEO
      call  BYTOUT
      movf  BYTE4,W
      movwf BYTEO
      call  BYTOUT
      goto  MAINP

BYTOUT      movlw 8
      movwf COUNT8
WAITS btfss PORTA,SEND  ; wait for PC to allow send
      goto  WAITS       ; if clear check again
SHIFC bcf   STATUS,C    ; clear carry flag
      rrf   BYTEO,F           ; BYTEO into carry
      btfss STATUS,C    ; check carry bit
      goto  OUT0        ; if 0 output 0
      goto  OUT1        ; if 1 output 1
OUT0  bcf   PORTA,DATO
      goto  DEC8
OUT1  bsf   PORTA,DATO
DEC8  bsf   PORTA,VALID ; valid data is now there
WAITL btfsc PORTA,SEND  ; wait for send to be lowered
      goto  WAITL
      bcf   PORTA,VALID ; lower valid
      decfsz      COUNT8
      goto  WAITS
      return

OVERFLO comf      BYTE1,F           ; all bytes must be zero
      comf  BYTE2,F           ; set to FF for all
      comf  BYTE3,F           ; which means error
      comf  BYTE4,F
      goto  SERIAL            ; and output error

        END
```

LISTING 2—PHOTOGATE-SUPPORT PROGRAM

```
#include <stdio.h>
#include <dos.h>
#include <conio.h>
#include <process.h>

/* SIGNAL* is not connected but reserve Pin 3 (D1) and A3 on PIC
   power to PIC through VDD_ON on pin 6 (D4)
   power to LED and transistor wiht TRANS_ON/LED_on pin 4 (D2)
   MCLR* on pin 5 (D3) normally high
   NORMAL OPERATION with Power and not reset (i.e. go) OR with POWGO (0x1C)
   The MSB of the printer Status port (S7*) or Pin 11 is used as input data
   Pin 10 (S6) is VALID signal from PIC that data is valid on Pin 11
   Pin 2 (D0) is SEND signal to PIC that PC is ready to receive
HAS BASIC CONVERSION ONLY 5 microsec per step
*/

#define DELAY     320           /* timing delay 320 for 166Pentium, 4Mhz */
#define TIMES     640000*16     /* length of time pulse if used */

#define SIGNAL    0x02
#define SEND      0x01
#define POWGO   0x1C

#define BYT 4         /*total number of bytes of data */
#define BIT 8        /*bits in 1 byte */

void main(void)
{
int dport_lpt1, sport_lpt1, bit, byt, columns, rows;
unsigned char shift_reg[BYT],temp;
char c;
long i,itemp;
float tempus;

/*Get LPT1 port addresses */

if(!(dport_lpt1 = peek(0x40,0x08)))
 { printf("\n\n\nLPT! not available... aborting\n\n\n"); exit(1); }
sport_lpt1 = dport_lpt1 + 1;  /* status port address */

/* Initialize the Printer DATA Port both for timing and SEND=0 */
outportb(dport_lpt1,0x00|POWGO);

/* Generate timing SIGNAL */
#undef USE_SIGNAL
#ifdef USE_SIGNAL
outportb(dport_lpt1,SIGNAL|POWGO);
for(i=0;i<TIMES;i++) ; outportb(dport_lpt1,0x00|POWGO);
#endif USE_SIGNAL

for(byt=0; byt<BYT; byt++)  /* number of bytes */
  {
    for(bit=0; bit<BIT; bit++) /* bits / Switch */
      {
        outportb(dport_lpt1,SEND|POWGO); /* raise SEND */
      for(i=0;i<DELAY;i++);
      /* poll VALID i.e. bit 6 of STATUS register */
      while(!(inportb(sport_lpt1)&&0x40)) ;

      /* Read the Status Port bit S7* which is input data */

       temp = inportb(sport_lpt1) ;
       outportb(dport_lpt1, 0x00|POWGO); /* have data, lower SEND */
       temp ^= 0x80;       /*invert bit no. 7 since port inverts */
       temp &= 0x80;     /*mask all bits except bit 7 */

      /* Concatenate it in the variable */
       shift_reg[byt] >>= 1;       /* shift bit one right */
         shift_reg[byt]  &= 0x7f;    /* make MSB 0 */
       shift_reg[byt]   |= temp;    /* new bit in MSB */
       for(i=0;i<DELAY;i++);
      } /* for(bit */
  } /* for(byt */

for(byt=0; byt<BYT; byt++) printf("Byte %d = %02X\n", byt, shift_reg[byt]);

itemp=0;
itemp|=shift_reg[3]; itemp<<=8;
itemp|=shift_reg[2]; itemp<<=8;
itemp|=shift_reg[1]; itemp<<=8;
itemp|=shift_reg[0];
tempus=5.0e-6*itemp;
printf("physical time %f seconds\n",tempus);

printf("hit key to end\n"); while(!kbhit()) ; exit(0);
}
```

Optocoupler simplifies power-line monitoring

Alfredo del Rio and Ana Cao y Paz, University of Vigo, Spain

The use of a linear optocoupler and a capacitor-based power supply yields a simple, yet precise power-line-monitoring system. The circuit in **Figure 1** converts the 110V-ac power-line voltage to an ac output voltage centered at 2.5V, covering 0 to 5V. The circuit isolates the output signal from the power line. You can connect the output directly to an A/D converter. For other power-line voltages, simply change the value of R_1. For a power-line voltage of 220V ac, use a value of 470 kΩ for R_1. The input stage is a nonisolated block that uses the neutral line as a ground reference. This block receives power from a capacitor-based power supply that provides a stabilized 5V-dc voltage and a 3.3V dc reference. The TLC2272 op amp, IC_1, and the TLC2272 linear optocoupler, IC_3, form a feedback amplifier in which the I_{P1} current is proportional to the input voltage, V_{IN}.

TABLE 1—OUTPUT OFFSET-VOLTAGE DRIFT

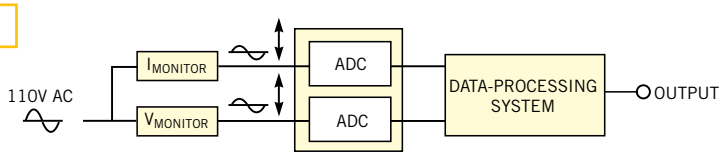
TIL300 (°C)	V_{OUT} (V)	TIL300 (°C)	V_{OUT} (V)
17.5	2.496	37.5	2.506
20	2.497	40	2.507
22.5	2.498	42.5	2.509
25	2.5	45	2.51
27.5	2.501	47.5	2.512
30	2.503	50	2.513
32.5	2.504	52.5	2.515
35	2.505		

Resistor R_2 adds a dc offset current to allow for both polarities in V_{IN}. The match between the two photodiodes in the IL300, IC_2, ensures that I_{P2} is closely proportional to I_{P1}. The output stage converts I_{P2} to a voltage level isolated from the power line. Variable resistor VR_2 trims the overall gain, and VR_1 adjusts the output-voltage offset, which is nominally 2.5V. You can test this circuit using simulation the model in **Listing 1** for IC_2. Typical values for K_1 and K_2 (optical transfer ratios) are approximately 0.007. The global optical transfer ratio is $K_3=K_2/K_1$. After performing the simulation, you can build and test a prototype. The power

supply for the isolated block provides 5V dc and a 3.3V reference from an available voltage of 7 to 10V. You do not need the regulated 5V if that voltage is already available in your system.

An important goal in this design is to obtain a stable dc voltage at the output. This property is crucial for dc measurements of V_{IN}. Even if you suppose the ac power line to be free of dc voltage, some types of loads drain dc currents, thereby introducing a small dc voltage because of voltage drops in the ac lines. Thermal drifts in the output voltage stem principally from drifts in K_3. In tests of the prototype, the K_3 temperature coefficient was 470 ppm/°C. **Table 1** shows V_{OUT} at different temperatures. The TLC2272 op amp has rail-to-rail output, yielding a wide output-voltage range, and low quiescent current, simplifying the capacitor-based power supply. Because the TLC2272 is a dual device, you can connect the unused half as a voltage follower. When you monitor a three-phase power line, you'd use one and one-half TLC2272s. Note that the op amps in the isolated block, IC_3, and the nonisolated block, IC_1, cannot be halves of the same chip; otherwise, you'd lose the isolation.

Figure 2



By adding two ADCs and a microcontroller, you can measure power-line voltage and current parameters.

LISTING 1—SIMULATION MODEL

```
.SUBCKT IL300 1 2 3 4 5 6
D1    2    10   DIN4002
D2    10   20   DIN4002
F1    3    4    VF_F1    0.007
VF_F1 20   30   0V
F2    6    5    VF_F2    0.007
VF_F2 30   1    0V
.ENDS
```

The main specifications of the circuit are 5300V-ac-rms galvanic isolation, 0.08% linearity, 470-ppm/°C thermal shifts in V_{OUT}, 2° phase shift at 50 Hz, and dc to 1-kHz bandwidth at −3 dB. If you connect the output to a 10-bit A/D converter, one LSB is equivalent to 0.5V in the 110V power line. You can add a Hall-effect sensor to the circuit for current measurements. The LTS series from LEM (www.lemusa.com) is suitable for this purpose, because these devices operate from a single 5V supply and provide a 2.5V-centered output. **Figure 2** shows a system that integrates voltage and current measurements. The processor computes true-rms voltages and currents, apparent and active power, and power factor.

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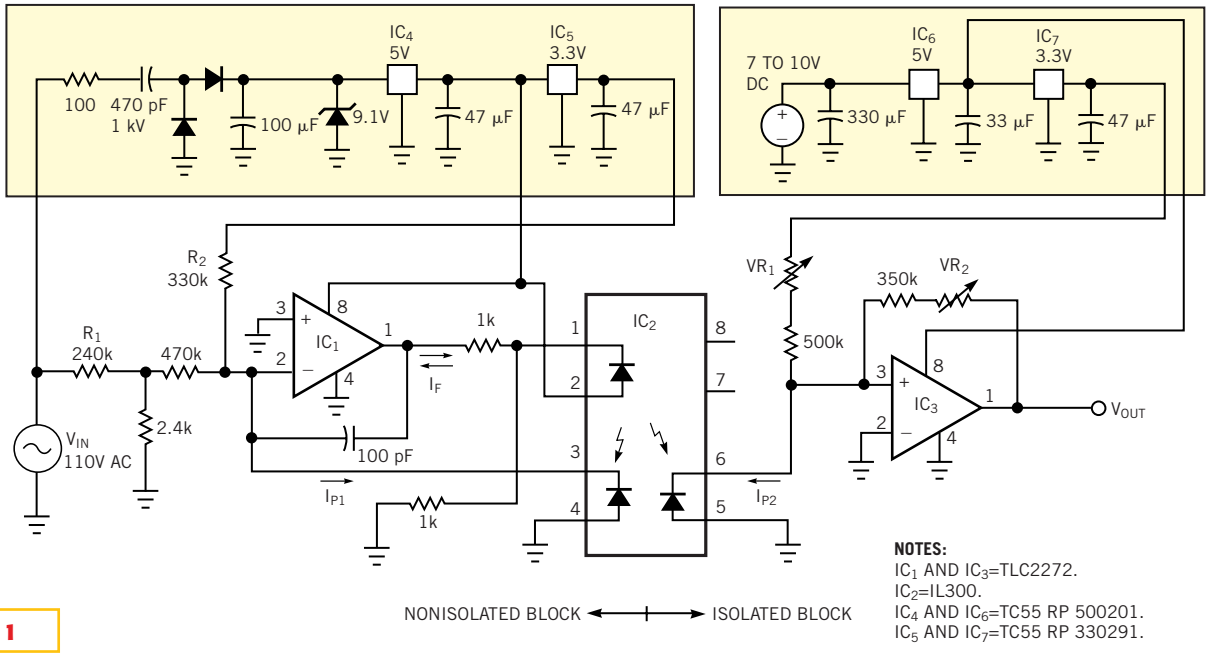


Figure 1

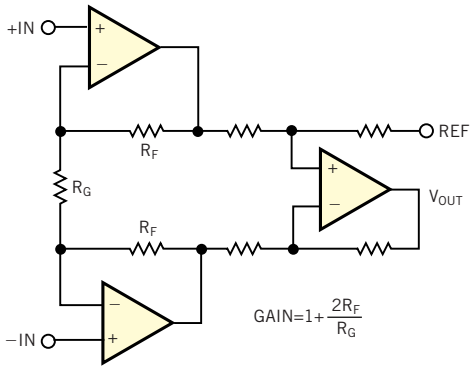
An isolated optocoupler circuit allows you to make dc measurements of the power-line voltage.

Improved amplifier drives differential-input ADCs

Stephan Goldstein, Analog Devices, Wilmington, MA

ADCs with differential inputs are becoming increasingly popular. This popularity isn't surprising, because differential inputs in the ADC offer several advantages: good common-mode noise rejection, a doubling of the available dynamic range without doubling the supply voltage, and cancellation of even-order harmonics that accrue with a single-ended input. But the differential input structure doesn't eliminate the frequent need for additional gain between the signal source and the ADC. A frequently used gain stage is the classic, three-op-amp instrumentation amplifier (**Figure 1**). This popular circuit offers excellent common-mode rejection and high input impedance. The circuit also has an output-reference (ground-sense) terminal, allowing you to reference the output voltage to a voltage other than ground. However, this circuit has a single-ended output (relative to the reference terminal), so it's a poor match for a differential-input ADC.

Figure 1



The classic three-op-amp instrumentation amplifier does not provide differential outputs.

Figure 2 shows two easy ways to create a differential-input instrumentation amplifier. In **Figure 2a**, IC_4 and its associated feedback resistors are connected in parallel with the original output amplifier but with inverted polarity relative to the original circuit. The two outputs together provide the desired function, but the circuit requires many matched resistors. Furthermore, the common-mode reference input could require several milliamperes of drive, depending on the resistor values and voltages involved. However, the circuit does the job, and you can build it by using a high-quality quad op amp and a handful of resistors. **Figure 2b** shows a more efficient and elegant approach, using only the four resistors required in the original output stage. In this circuit, a modern, fully differential op amp, such as the AD8138, replaces IC_3 and IC_4 in **Figure 2a**. The amplifier's two outputs swing symmetrically about its high-impedance, common-mode reference input. The differential outputs provide a clean, simple interface to a differential-input ADC.

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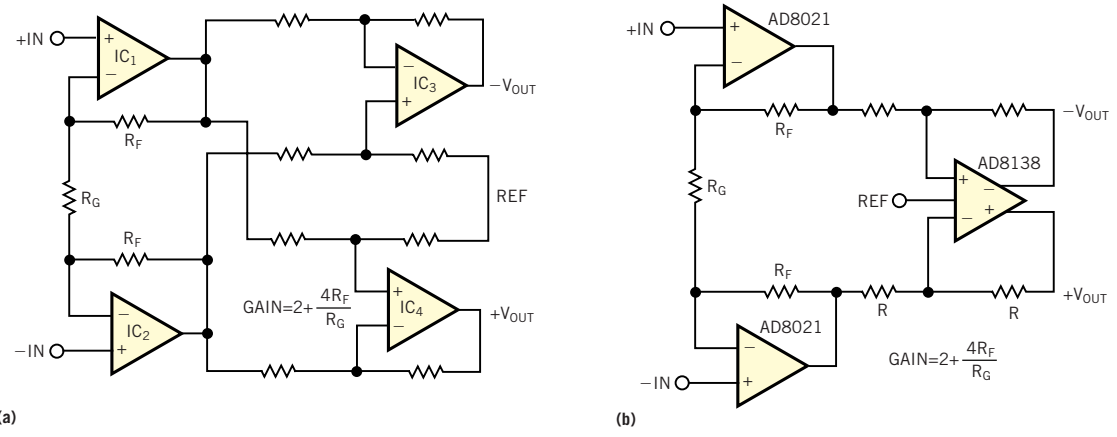
Figure 2



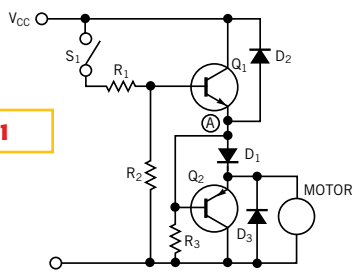
The four-op-amp instrumentation amplifier (a) provides differential outputs but requires many matched resistors. A differential-output op amp (b) reduces the IC count in Figure 2a to three.

Circuit forms dc-motor switch with brake

JB Guiot, DCS AG, Allschwil, Switzerland

Controlling a small dc motor without speed control sounds like a trivial task; a switch or a relay should suffice. However, several problems accompany this approach. For one, the switch, because of the inductive load and the low starting resistance of the motor, tends to wear out prematurely (with all the related sparks and EMI problems). Second, when you cut the power, the motor continues to rotate for a certain time, depending on its initial speed and inertia. The circuit in **Figure 1** can be useful for designs that don't need precise control of speed and stopping position but can benefit from enhanced deceleration. The circuit comprises two parts. Q_1 plays the role of the switch. D_2 protects Q_2 against inductive surges. Resistor R_2 keeps Q_1 off as long as switch S_1 is open. R_1 limits the base current of Q_1 when S_1 is closed. S_1 can be a manual switch, a relay contact, an optocoupler, or a transistor. If you close S_1, Q_1 turns on, and the motor runs.

Figure 1



This circuit provides both motor-drive and braking functions.

Q_2, D_1, and R_3 constitute the braking circuit. This circuit is similar to the output circuit of TTL gates. D_3 protects Q_2 from inductive surges. When S_1 closes, Q_1 turns on, and the voltage at Point A goes high (near V_{CC}). The voltage at the base of Q_2 is higher than the voltage at the emitter, because of the voltage drop in D_1. If you open S_1 while the motor is running, Q_1 turns off. The voltage at Point A is near zero. The self-induced, back-EMF voltage from the motor sees a short circuit in Q_2, whose emitter is more positive than its base and thus conducts. Short-circuiting the motor results in braking it. The higher the speed of the motor, the stronger the braking effect.

You should mount the circuit of Q_2 as near as possible to the motor to reduce the series resistance of the wiring. This parasitic resistance limits the braking current and, thus, the deceleration. The circuit of Q_1 can be remote. The dividing line between the two circuits is at Point A. This design mounts the circuit on the tool-changer motors of small machine tools, and it has worked perfectly for years. The values of the components are not critical. The transistors should preferably be Darlington pairs and, like the diodes, should be types commensurate with the power-supply voltage and the motor current. (Also, don't forget the high inductance of the motor.) The components in **Figure 1**, for example, are suitable for a 24V, 3.5A motor.

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Edited by Bill Travis

Autoreferencing circuit nulls out sensor errors

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

The autoreferencing circuit in **Figure 1** nulls out the error of a sensor, such as a pressure transducer, at its reference level—for example, at ambient pressure. The circuit is an analog-digital-feedback control system that uses a digitally programmable potentiometer to provide the variability. The circuit in **Figure 1** is designed to accommodate a pressure transducer with a nominal 1V±50-mV output at ambient pressure and provide a voltage of 1V±1 mV. Amplifier IC_{1A} is a summing/difference circuit whose inputs are the sensor's output voltage, V_{SENSE}; a voltage shift, V_{SHIFT}, of 100 mV; and a correction voltage, V_{CORR}. IC_{1B} functions as a comparator, comparing the output voltage of the summing amplifier with the ideal output voltage of the sensor, 1V. The logic output of the comparator sets the direction for incrementing or decrementing the potentiometer's wiper, whose buffered wiper voltage provides the correction voltage, V_{CORR}.

The potentiometer is a Catalyst 30-tap digitally programmable potentiometer with an increment/decrement interface. The correction voltage varies from 0 to 200 mV and subtracts from the shifted sensor voltage. Mathematically, $V_{OUT}=(V_{SENSE}+V_{SHIFT})-V_{CORR}$, where $0\le V_{CORR}\le 200$ mV, $V_{SHIFT}=100$ mV, and $0.95V\le V_{SENSE}\le 1.05V$. The 100-mV, 200-mV, and 1V references for the circuit come from a 2.5V reference, stepped down by a resistive divider and buffered by voltage followers. IC_{2A} implements a square-wave oscillator whose frequency is approximately equal to 1/RC—in this case, 10 kHz. You program the autoreferencing circuit using the logic-input signals OSC and $\overline{CS}$. The circuit becomes disabled when OSC is low and $\overline{CS}$ is high. When the circuit is disabled, V_{OUT} is at its last corrected value.

The circuit becomes enabled and corrects the output voltage for a new sensor or different set of conditions when OSC is high and $\overline{CS}$ is low. To store the current wiper setting of the digitally programmable potentiometer in nonvolatile memory, first make OSC low and then bring $\overline{CS}$ from low to high. If power disappears and is later restored, the potentiometer goes to the corrected value stored in nonvolatile memory. The measured error in the system is less than 1 mV, but better performing amplifiers, a higher resolution potentiometer, and more accurate resistors can reduce the error to the low-microvolt region. This circuit uses three ICs and a handful of discrete parts and is an alternative, low-cost approach to more complex autoreferencing circuits using DACs, ADCs, and microprocessors.

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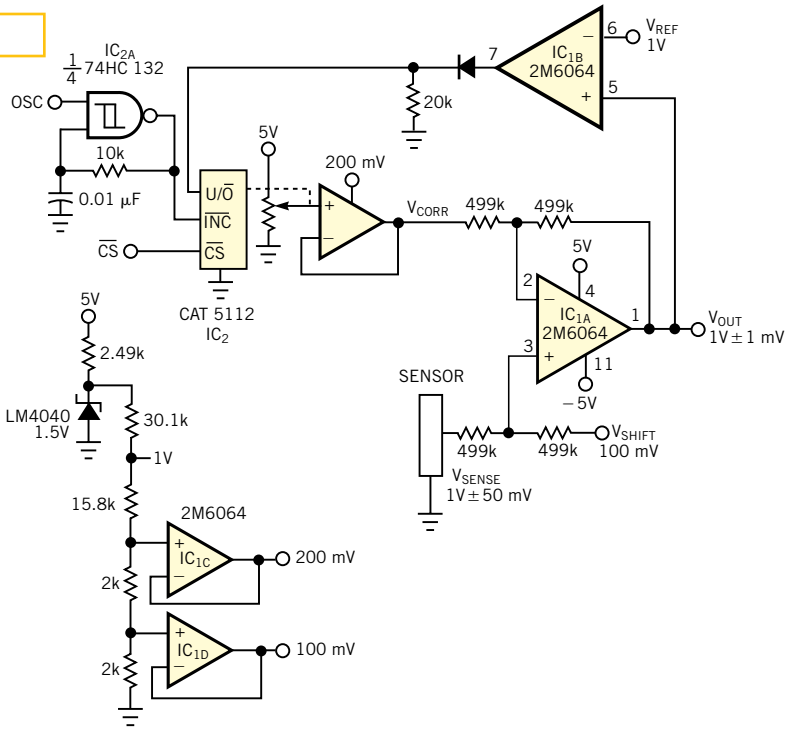
Figure 1



This autoreferencing circuit nulls out output errors at a sensor's reference (ambient) condition.

Low-power keypad consumes only 100 nA

Mike Mitchell, Texas Instruments, Dallas, TX

Often in the use of products with keypads, one or more keys become "stuck" or are being pressed. For example, a cell phone in the bottom of a purse or in a hip pocket could have one or more of its keys inadvertently pressed and held down for a considerable period. Depending on the circuit design and implementation of the keypad interface, this condition could cause excess current to flow, thereby draining the batteries in portable equipment. The circuit in **Figure 1** is a keypad interface that solves this problem by using an ultralow-power microcontroller. The circuit typically consumes 100 nA while awaiting a key press and consumes a maximum of only 2 µA if all keys are stuck or held down. An added bonus of the circuit is that it requires no crystal.

The circuit uses the MSP430, IC_1, because it offers low power consumption, individually configurable I/O pins with interrupt on rising or falling edges, and wake-up time of less than 6 µsec. In normal mode, port pins P3.0 to P3.3 drive the rows high. The columns connect to port pins P1.0 to P1.2, configured as inputs with interrupts enabled and set to interrupt on a rising edge. The pulldown resistors hold the inputs low in the inactive state. The MSP430 then goes into low-power Mode 4, in which the microcontroller draws 100 nA. This state continues indefinitely until you depress a key. The circuit is completely interrupt-driven with no need for polling. When you depress a key, the column associated with that key receives a rising edge, thereby waking the MSP430. The timer for the delay uses the internal digitally controlled oscillator of the MSP430, an RC-type oscillator. The digitally controlled oscillator is subject to tolerances, so you use a debounce delay to yield a worst-case minimum delay of 25 msec. That figure translates to a worst-case maximum delay of approximately 86 msec and a typical delay of approximately 40 msec. This range is eminently usable for keypad-debouncing purposes. After the debounce delay, the circuit scans the keypad to determine which key you depressed.

After you depress a key, the MSP430 goes into a "wait-for-release" mode, in which it drives only the necessary row for the key you depressed. (Other rows switch low.) The microcontroller reconfigures the P1.x I/O to interrupt on a falling edge, and it again goes into low-power Mode 4 and waits for the release of the key. Again, the circuit needs no polling at this point. The detection of the key release is completely interrupt-driven, allowing the MSP430 to stay asleep while the key is held, thereby reducing current consumption. Once you release the key, the circuit again executes the debounce-delay routine. After the debounce delay, the circuit again scans the keypad to determine whether any other keys are being held. If so, the wait-for-release mode continues. When all the keys are released, the MSP430 reverts to "wait-for-press" mode. During the wait-for release mode, only one row of the keypad goes high, thereby limiting the maximum current consumption to the condition in which all three keys on a single row are pressed. For a 3V system, this condition equates to approximately 2 µA. Any other key press does not result in increased current consumption, because the corresponding row is not in a high state. You can download the software for the microcontroller from the Web version of this article at www.ednmag.com.

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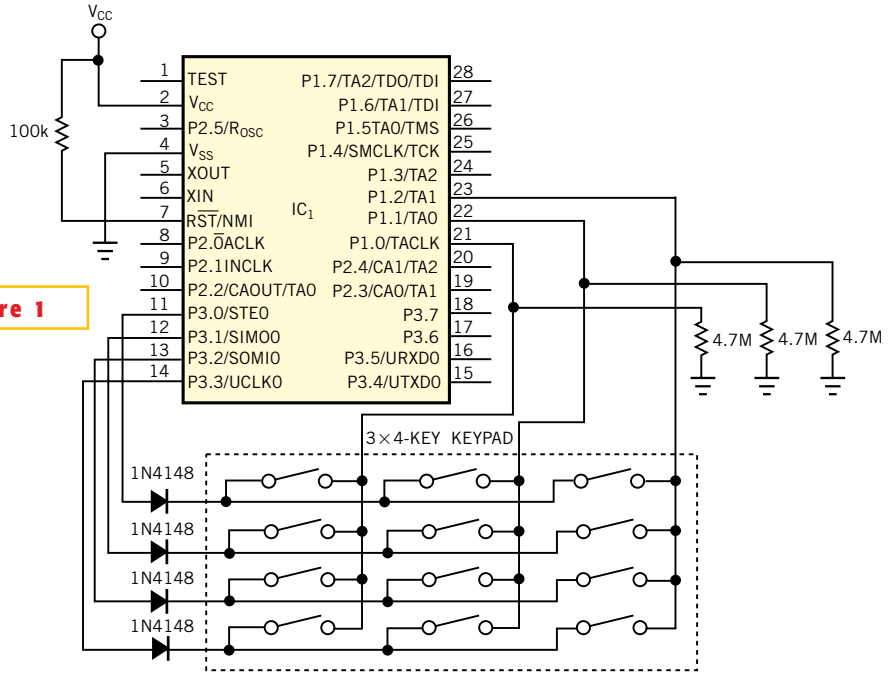


Figure 1

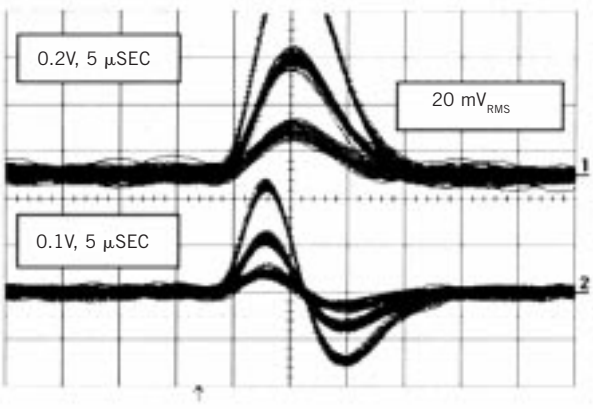
This keypad interface draws only 100 nA in standby mode and avoids "stuck-key" problems.

Time-tag impulses with zero-crossing circuit

Elio Rossi, Itesre-CNR, Bologna, Italy

A "constant-fraction discriminator" usually performs the time-tagging of impulsive events, which have a peaking time of the signal amplitude. The implementation of this technique requires a delay in the input signal of approximately the same amount as the signal's rise time. You can attain this delay by using a coaxial cable of an appropriate length. For many applications, in which the rise time for impulsive events is 1 to 10 µsec, you must consider alternative solutions, because of the length of the cable you'd require. **Figure 1** shows the typical output from a spectroscopic amplifier, where the presence of a large amount of detector noise with Gaussian distribution is a limiting factor for system performance in amplitude and timing resolution. The time-tagging of such pulses is subject to two well-known types of errors: the jitter related to the noise and the "walking time" arising from the amplitude variation of the signals. You can eliminate the walking time by differentiating the signal and detecting the zero crossings. The jitter is related to the noise around the zero-crossing line.

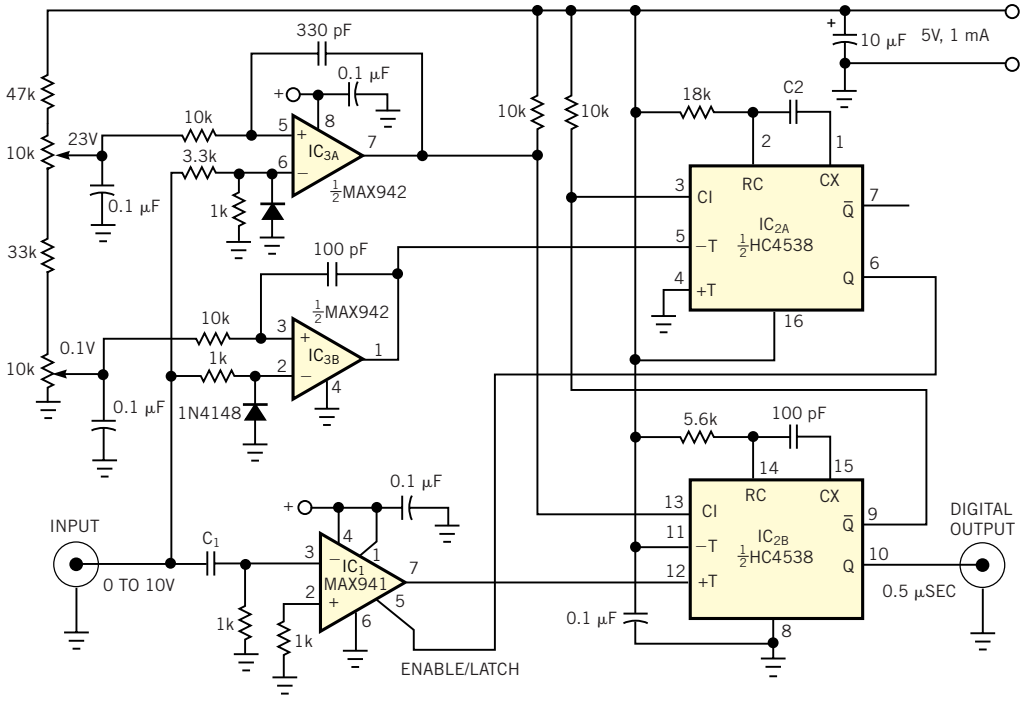
Figure 1



A spectroscopic amplifier produces differentiated signals (lower traces) in response to input impulses (upper traces).

In **Figure 2**, an arming discriminator with a fixed threshold of 100 mV ($5\times V_{RMS(NOISE)}$) enables the IC_1, a MAX-941 zero-crossing discriminator, via the

Figure 2

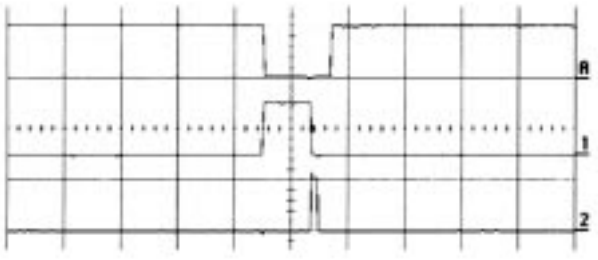


A discriminator and a zero-crossing detector eliminates "walking-time" error for impulsive events.

first half of IC_2, an HC4538 resettable monostable multivibrator. The propagation delay in these ICs allows enabling the zero-crossing discriminator when the differentiated signal is well over the baseline noise for the full range of the input signal. The positive-going output pulse from IC_3, a MAX941, corresponding to the zero-crossing time, reaches the output with a fixed length of 0.5 µsec, set by the second monostable multivibrator. This second multivibrator resets the first and latches the MAX941 at the high output level until a new trigger arrives from the arming discriminator. In this way, you avoid spurious triggers at the beginnings and ends of input pulses. The upper-threshold discriminator output, with a minimum output length of 5 µsec, serves to "veto" the 0.5-µsec output and works even for highly saturated input signals. Because of the input configuration of the MAX942, it is necessary to reduce the upper threshold level to less than 2.8V. **Figures 3** and **4** show the timing sequences for 0.2V and 10V input signals, respectively.

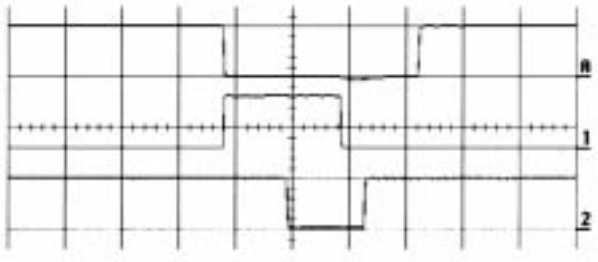
You can obtain the same results using many different implementations of the circuit, depending on the ICs available off the shelf. For example, you can substitute the MAX941 with a common discriminator and a CMOS analog switch to commutate the threshold from a positive voltage to ground. A single flip-flop then completes the circuit. This design uses an amplification stage with back-to-back limiting diodes in front of the zero-crossing discriminator. **Table 1** shows the results, with comparisons to the shaping-time value of 3 µsec. You measure the walking time and jitter using a pulse generator, preamplifier, shaping amplifier, time-to-amplitude converter, and multichannel analyzer. **Figure 5** shows just three of the many histograms used to calculate the walking time and jitter results.

Figure 3



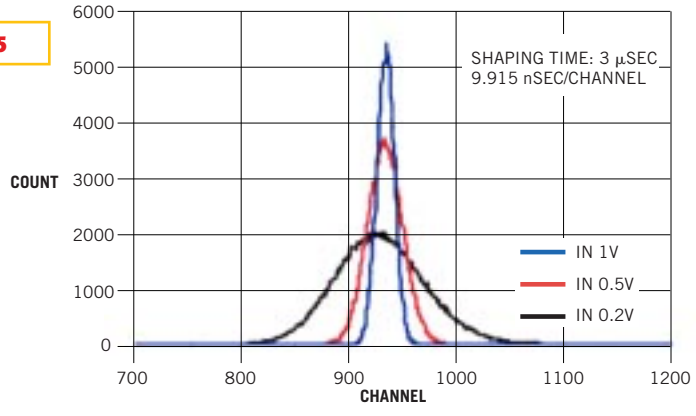
For 200-mV input, Trace A is the output from the arming discriminator, Trace 1 is the Enable signal for the MAX941, and Trace 2 is the signal output.

Figure 4



For a 10V input, Trace A is the output from the lower level discriminator, Trace 1 is the Enable signal for the MAX941, and Trace 2 is the output from the upper level discriminator.

Figure 5



These jitter histograms are for input signals of 0.2, 0.5, and 1V.

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TABLE 1–MEASUREMENT RESULTS AT 1 kHz AND WITH 20 mV RMS OF NOISE

Shaping time (µsec)	Peak time (µsec)	C_1 (nF)	C_2 (nF)	Jitter	$0.1V_{IN}$[1]	$0.2V_{IN}$	$0.5V_{IN}$	$1V_{IN}$	$2V_{IN}$	$5V_{IN}$	$10V_{IN}$	Walk
1	2	0.47	0.33	σ (µsec)	0.249	0.145	0.06	0.029	0.015	0.009	0.006	0.06 µsec
3	6	1	1	σ (µsec)	0.594	0.395	0.156	0.081	0.042	0.017	0.009	0.2 µsec[2]
6	12	2.2	2.2	σ (µsec)	1.608	0.939	0.372	0.195	0.096	0.04	0.021	1.1 µsec[2]
3	6	1	1	Amplifier	0.664	0.417	0.161	0.081	0.042	0.017	0.009	0.47 µsec[3]

Circuit provides reference for multiple ADCs

Ron Gatzke and Tanja Hofner, Maxim Integrated Products, Sunnyvale, CA

The achievable accuracy for systems with multiple ADCs depends directly on the reference voltages applied to the ADCs. Medical-ultrasound-imaging systems, for example, commonly include a large number of ADCs in the system's beam-former electronics, with the ADCs usually organized in groups of 16, 24, 32, and so on. To obtain maximum beam accuracy, you must minimize errors in the ADC path. Poor accuracy of the reference voltages of the individual ADCs degrades the overall system accuracy. Another source of degradation is the distributed load, which comprises many individual resistive and capacitive loads. Several approaches are available to provide the reference voltage for such ADC arrays:

- Individual on-chip references. Though this approach offers a convenient local connection to each ADC, it can result in relatively poor matching among the converters.
- A single external reference voltage applied to all ADC reference inputs. Such a configuration allows you to engineer an external reference voltage of arbitrary accuracy but incurs errors from the small variations among the internal ladders of the ADCs.
- An external reference directly driving the ADCs' reference-ladder taps. This option delivers maximum gain accuracy by directly controlling the reference voltage applied to each ADC ladder. However, it requires driving the relatively low resistance of the ladders. Moreover, some ADCs do not allow access to that internal bias point.

ADC ACCURACY

In many applications, gain and noise level have a major effect on ADC accuracy. The gain of an ADC is in effect the slope of its transfer function, which relates analog inputs to the allowable range of digital-output codes. One way to quantify gain is to measure the full-scale input range, which is a direct function of the reference-voltage level. For medical-ultrasound-imaging systems, variations in the full-scale ranges of the ADCs can cause errors in beam formation. The variations also affect the ADCs' clipping point—an effect that may be important is certain signal-demodulation schemes. An ADC's noise level determines its usable dynamic range. This dynamic range should be as great as possible. The reference-noise component of ADC noise can be additive or multiplicative. Local bypass capacitors on the individual ADCs can easily filter additive noise. Multiplicative noise, on the other hand, is more insidious. For ultrasound applications, reference noise in the audio-frequency

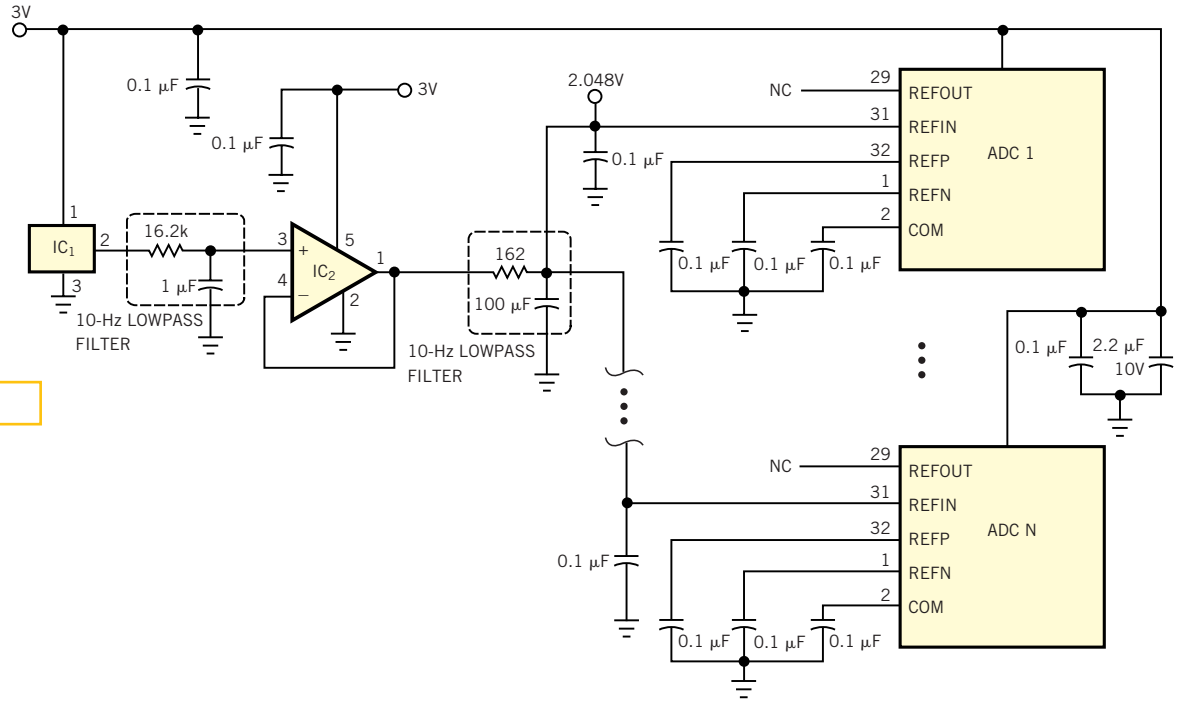


Figure 1

For ultrasound applications, a single, low-noise reference circuit can drive as many as 1000 ADCs.

spectrum can modulate large "stationary" signals in the RF spectrum. Such signals arise from stationary tissue in the ultrasound target.

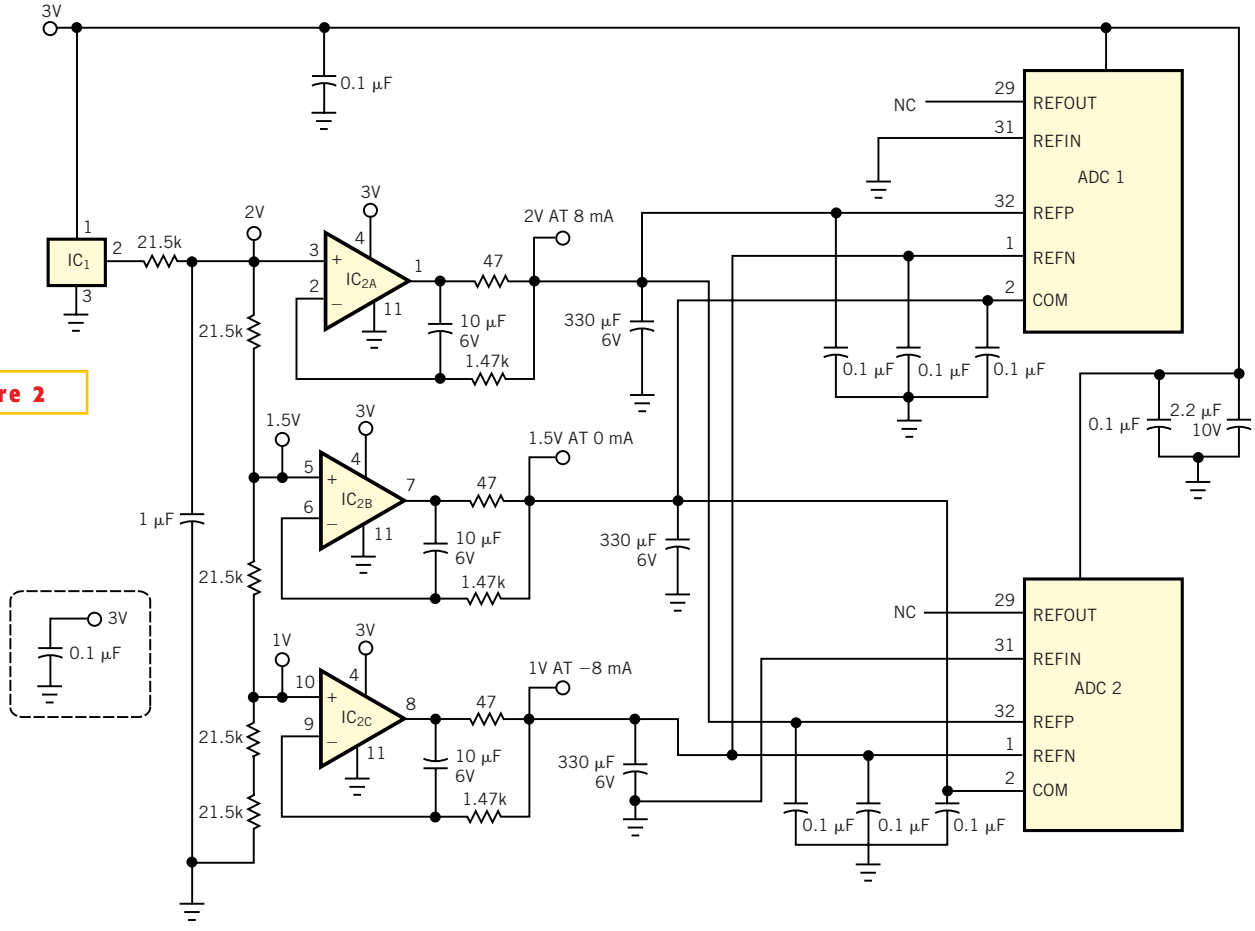
Audio modulation produces sidebands in the RF signal that a Doppler detector can demodulate, producing audio tones. To estimate the amount of audio noise tolerable in an ultrasound application, assume a nearly full-scale RF signal applied to a 10-bit ADC such as the MAX1448. The device's dynamic range of almost 60 dB equates to a noise floor of −60 dBFS (relative to full scale). You can normalize that noise level to a 1-Hz bandwidth. The Nyquist bandwidth for an 80-MHz sampling rate is 40 MHz. The correction factor is $\sqrt{40\ \text{MHz}}$=76 dB, which places the ADC's noise floor at −60 dBFS−76 dBFS=−136 dBFS. Because a conservative design requires the reference-voltage noise to be at least 20 dB lower (−156 dBFS), a 2V reference requires an extremely low noise level of 33 nV p-p (approximately 8 nV/$\sqrt{\text{Hz}}$).

A multiple-ADC array may require a more accurate reference voltage than the one internal to each converter. The reference voltage internal to MAX144x converters, for example, has an accuracy of ±1%. The following two circuits are reference designs for such arrays. They feature a single, common low-frequency noise filter, and they offer high-frequency noise suppression via local decoupling capacitors connected to individual ADCs.

SINGLE EXTERNAL REFERENCE

Multiple-converter systems based on the MAX144x family are well-suited for use with a common reference voltage. You can the REFIN pin of these converters to an external reference source and thus eliminate the need for any circuit modification. Moreover, the high input impedance of REFIN (even of multiple REFIN terminals connected in parallel) results in only a small load-current drain. **Figure 1** shows a precision source, such as the MAX6062, that generates an external dc level of 2.048V and exhibits a noise-voltage density of 150 nV/$\sqrt{\text{Hz}}$. The output of the IC passes through a one-pole lowpass filter with 10-Hz cutoff frequency to op amp IC_2, which buffers the reference. The buffered reference voltage then passes through a second 10-Hz lowpass filter. IC_2 exhibits a low offset voltage for high gain accuracy and a low noise level. The passive 10-Hz filter following the buffer attenuates noise produced in the voltage-reference IC and buffer stage. The filtered noise density, which decreases with frequency, meets the noise levels re-

Figure 2



For ultrasound applications, a precision, low-noise reference circuit can drive as many as 32 ADCs.

quired for precision-ADC operation.

Converters of the MAX144x family specify a typical gain error of ±4.4% (better than ±0.5 dB). This performance is better than the gain tolerance of all other building blocks in the signal path of an ultrasound receiver. Note that the circuit in **Figure 1** ensures proper power-up/power-down sequencing, because all active parts receive their power from the same supply-voltage rail. This approach yields excellent gain matching and an extremely low noise level with minimal circuitry. The circuit should prove adequate in many applications that require multiple gain-matched ADCs.

PRECISION EXTERNAL REFERENCE

For applications requiring more stringent gain matching, the MAX144x family fills the bill. In **Figure 2**, connecting each REFIN to analog ground disables the internal reference of each device. You can thus directly drive the internal reference ladders from a set of external reference sources. These voltages can have an arbitrarily tight tolerance; the ADCs typically track them within 0.1%. ADCs of this family have 4-kΩ resistance across the ladder's reference connection, so it's easy for the reference source to drive the load, even with many ADCs connected in parallel. IC_1 generates a dc level of 2.500V, followed by a 10-Hz lowpass filter and a precision voltage divider. The buffered outputs of this divider provide 2, 1.5, and 1V, with an accuracy that depends on the tolerances of the divider resistors. The quad op amp IC_2, selected for its low noise and dc offset, buffers the three voltages.

The individual voltage followers connect to 10-Hz lowpass filters, which filter both the reference-voltage and buffer-amplifier noise to a level of 3 $nV/\sqrt{Hz}$. The 2 and 1V reference voltages set the differential full-scale range of the associated ADCs at 2V p-p. The 2 and 1V buffers drive the ADCs' internal ladder resistances between them. The load is 4 kΩ divided by the number of ADCs in the circuit. As an example, 32 ADCs draw 8 mA from the supplies, a load current that is well within the capability of IC_2. The gain accuracy of the configuration in **Figure 2** can be almost arbitrarily tight, depending on the accuracy grade of IC_1 and the tolerances of the resistors in the voltage divider. The gain matching of the ADCs in such a configuration is typically 0.1%. With a noise level below 3 $nV/\sqrt{Hz}$ at 100 Hz, this circuit provides exemplary performance. As in **Figure 1**, the common power supply for all active components removes any concern about power-supply sequencing.

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Motor-control scheme yields four positions with two outputs

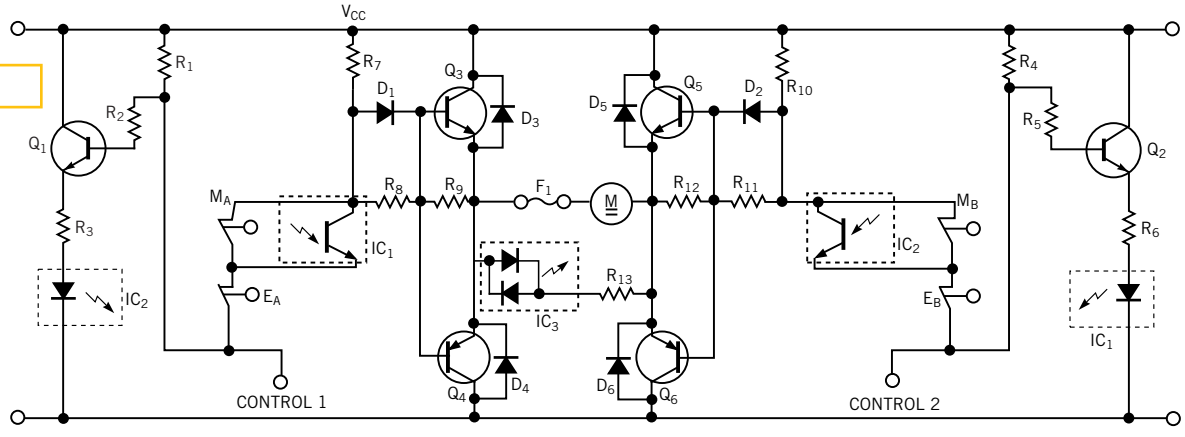
Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

FIGURE 1 shows how to position a mechanical device into four discrete positions but with only two free outputs and one free input from the control system. The position depends on a set of cams and four corresponding limit switches. The 24V-dc motor comes with a worm gear. Darlington transistors Q_3 to Q_6 and resistors R_7 to R_{12} form an H-bridge that drives the dc motor, M. Diodes D_3 to D_6 protect these transistors from inductive spikes. The outputs of the controller (not shown), connected to the Control 1 and Control 2 inputs, have open-collector structures that connect Control 1, Control 2, or both to ground upon activation. If you activate neither Control 1 nor Control 2, Q_3 and Q_5 conduct, receiving base current through R_7 and D_1 and R_{10} and D_2, respectively. This action short-circuits (brakes) the motor. In this case, Q_4 and Q_6 are turned off. Optocouplers IC_1 and IC_2 are on, thereby short-circuiting the limit switches, M_A and M_B.

Activating only one control input (for example, Control 1), if the cam does not push open the corresponding limit switch, E_A, causes Q_3 to switch off and Q_4 to switch on with R_8 limiting the base current. Thus, the motor rotates until the cam pushes open limit switch E_A (Position 1 in **Figure 2**). The limit switch, M_A, has no influence because optocoupler IC_1 short-circuits M_A when Control 2 is in a high state. A similar, symmetrical operation occurs if you activate (ground) Control 2. In this case, the motor rotates to push open limit switch E_B (Position 4). To bring the motor to one of the middle positions—say, Position 2—you use the following procedure:

1. With Control 2 high (not connected), activate (ground) Control 1. The motor rotates until it pushes open limit switch E_A. The bases of Q_3

Figure 1



NOTES:

D_1, D_2: 1N4148
D_3 TO D_6: 1N4937
R_1, R_2, R_4, R_5, R_9, R_{12}: 10 kΩ, 0.25W
R_7, R_8, R_{10}, R_{11}: 3.3 kΩ , 0.25W
R_3, R_6, R_{13}: 1.5 kΩ, 0.6W

Q_1, Q_2: 2N2222, 2N3904...
Q_3, Q_5: BDX33C
Q_4, Q_6: BDX34C
IC_1 TO IC_3: PC814, H11AA1, SFH6206-2...

This simple circuit provides four-position motor control with two inputs.

through Q_6 are all high.

2. Activate (ground) Control 2. The bases of Q_5 and Q_6 switch low. (M_B and E_B are closed.) The motor rotates in reverse until M_A closes. At this time, all bases are low. Q_4 and Q_6 short-circuit the motor to ground, thereby braking it to a stop.

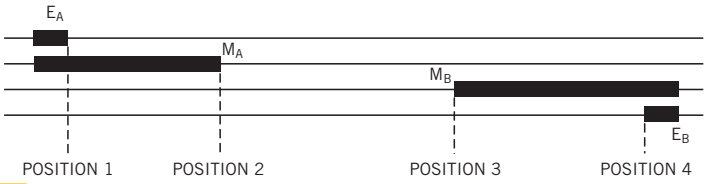


Figure 2

Cams operate the limit switches in Figure 1, producing four discrete positions.

First activating Control 2 and then Control 1 brings the motor to Position 3, the edge of cam M_B. Otocoupler IC_3 remains on as long as the motor receives voltage. The output of IC_3 connects to a feedback input of the controller. Thus, you can control whether the motor is rotating or stopped through this input. F_1, a polymer-based resettable fuse, protects the motor and the circuit against overcurrent conditions, such as a stalled motor. You can mount the circuit in **Figure 1** on small machine tools, such as a workpiece changer. The values of the components are not critical. The transistors are preferably Darlington types and, like the diodes, should have adequate ratings to accommodate the power-supply voltage and the motor current. (Don't forget the high inductance of the motor.) The components in **Figure 1** accommodate a 24V-dc, 2.5A motor.

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Single switch controls digital potentiometer

Chuck Wojslaw and Gary M Craig, Catalyst Semiconductor, Sunnyvale, CA

The control of electronic potentiometers in most today's applications comes from controller-generated signals. However, a significant number of applications exist that require adjustments using manual, front-panel controls. The circuit in **Figure 1** uses one IC, one switch, and 10 discrete components. It implements the interface of a single DPDT, momentary-contact rocker switch to a DPP (digitally programmable potentiometer). The Catalyst DPP has a three-wire increment/decrement interface. The traditional way to implement the front-panel controls for potentiometers with this type of interface is to use two single-pole, single-throw switches. Switch S_1 reduces the front-panel hardware by half. The action of the switch is natural for the control of increment-up/increment-down potentiometers.

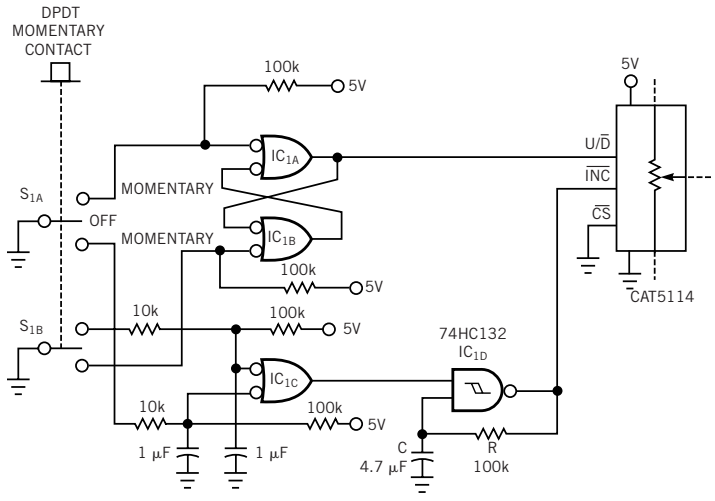

Figure 1

A single switch is all you need to control a digitally programmable potentiometer.

IC_{1A} and IC_{1B}, which implement an R-S flip-flop, control the potentiometer's wiper direction—up or down. The output of the flip-flop reflects the up/down position of S_1. The potentiometer's wiper advances on the falling edge of the signal driving the $\overline{INC}$ input of the DPP. The clock output of IC_{1D} drives $\overline{INC}$. The clock becomes enabled when you depress the rocker switch either up or down. The RC networks at the inputs of IC_{1C} debounce the switches. If you momentarily depress the rocker switch, the clock generates one pulse. If you continuously depress the rocker switch, the clock free-runs at a frequency of approximately $1/R_1C_1$.

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Versatile power-supply load uses light bulbs

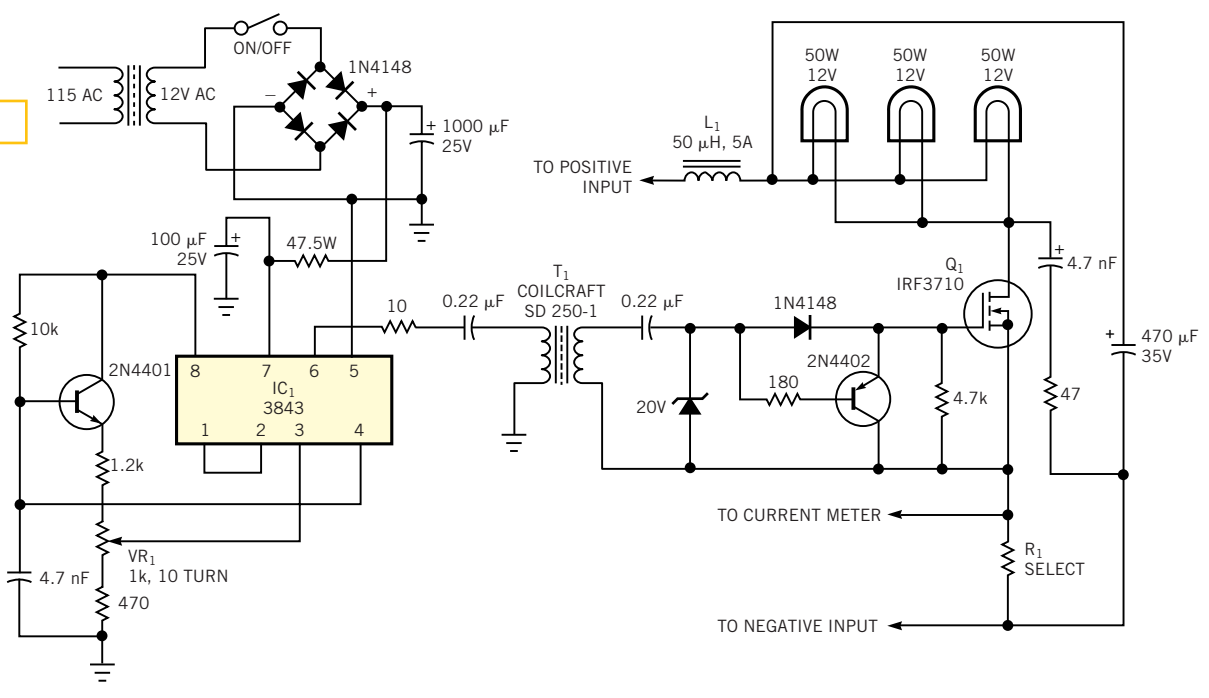
William Sloot, Computron Display Systems, Mount Prospect, IL

Improvising loads for bench-testing and designing power supplies is often a frustrating and sometimes hazardous experience. When you push large power resistors to their limit, they tend to burn benches and melt solder connections. Many electronic loads are on the market but are usually expensive and of laboratory-type precision and often represent overkill for the average designer. Incandescent light bulbs make excellent loads, able to handle large amounts of power. Moreover, they come in small packages and require no heat sinks. Furthermore, because they light up, you obtain instant feedback, rather like an analog versus a digital meter. The drawback is that the resistance of an incandescent lamp changes dramatically with the power input. The power into the load must therefore be controllable over a broad range, if the bulb is to be a useful current sink. A simple approach to this control problem is to pulse-width-modulate a power MOSFET in series with the load. This design uses a four-rail, 100W supply with outputs of 5, 12, and ±15V. For these voltage and power levels, 50W, 12V bulbs provide a suitable load. This application required three bulbs connected in parallel (**Figure 1**). Many automotive-supply dealers offer 50W, 12V bulbs.

Because these bulbs screw into an ordinary 115V light socket, you can create a virtually unlimited combination of loads. The use of old-fashioned porcelain-type sockets wired in parallel allows you connect any number of bulbs in the load circuit. The circuit in **Figure 1** addresses supplies of 1 to 24V output levels, of positive or negative polarity, with power levels as high as 150W. You can use the same basic approach to load higher voltage supplies by using 115V light bulbs and appropriately sizing the power MOSFET and other components. The circuit uses a standard PWM 3843 IC, IC_1, in open-loop mode. Potentiometer VR_1 controls the duty cycle over its full range. The frequency is not critical and is approximately 37 kHz with the values shown in **Figure 1**. A small, modular plug-in transformer provides power, but you can use any source of approximately 18V dc at 50 mA.

T_1 provides isolated drive to the power MOSFET, Q_1. The transformer allows you to load negative as well as positive sources. The various components in the gate circuit provide efficient drive to Q_1 over a broad range of duty cycles. The L_1 choke isolates the input from the switching pulses in Q_1. You could use either an analog or a digital current readout. This design uses an LED readout salvaged

Figure 1



Incandescent light bulbs provide convenient loads for testing power supplies.

from an old power supply. You must size the current resistor, R_1, for the power dissipation and the requirements of the current meter. In this application, three metal-oxide, 0.1Ω, 2W resistors connected in series met the requirements (maximum current of 4A). You must fasten Q_1 to a heat sink adequate for the application. The circuit in **Figure 1** uses an Aavid (www.aavid.com) 530101B00100. This heat sink is a U-shaped radiator measuring approximately 1.75×175 in. on each side. Applications requiring higher currents could use two MOSFETs in parallel. The gate-drive scheme shown has enough power to drive two MOSFETs.

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Two-transistor circuit replaces IC

Jim Hagerman, Hagerman Technology, Honolulu, HI

Linear Technology's recently introduced LTC4300 chip buffers I²C clock and data lines to and from a hot-swappable card. This task is difficult because the IC must work bidirectionally, meaning that you can simultaneously and actively drive both sides. However, as is sometimes the case, you can replace a complicated circuit by a simple one without much loss of performance. For example, transistors and resistors replace the entire IC (**Figure 1**). The circuit handles only the clock signal or only the data signal. Two npn transistors, connected head-to-head, form the heart of the circuit. I²C signals come from open-collector or open-drain outputs, so can only pull down (sink current). When Enable is high, a low-going SCL signal drives the emitter of one of the transistors as a common-base amplifier. The 10-kΩ resistor in the base circuit provides enough current to saturate the transistor and drop the V_{CE} voltage to approximately 0.1V, thereby pulling the other side low.

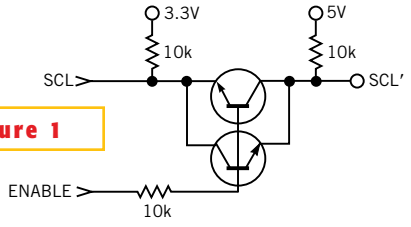

Figure 1

This circuit is an I²C-compatible, hot-swappable translator/buffer.

The circuit acts like an efficient diode. With Enable low, the hot-swappable side has no effect on the signal, with or without power applied. The two-transistor circuit offers the additional benefit of acting as a level translator between two logic levels. This example shows a buffer-translation between a 3.3V system and a 5V card. For proper operation, the Enable line must not go higher than the lower of the two supply voltages. **Figures 2a** and **b** show operation at 100 kHz. Some edge glitches and overshoot, stemming from transistor-junction capacitance, are evident in the 3.3V signal, but these slight defects should be tolerable in many low-cost applications. **References 1** and **2** treat similar level-translation circuits.

References

1. Hagerman, Jim, "Two transistors form bidirectional level translator," *EDN*, Nov 7, 1996, pg 114.
2. Poon, CC, and Edward Chui, "Low-voltage interface circuits translate 1.8V to 5V," *EDN*, Nov 5, 1998, pg 119.

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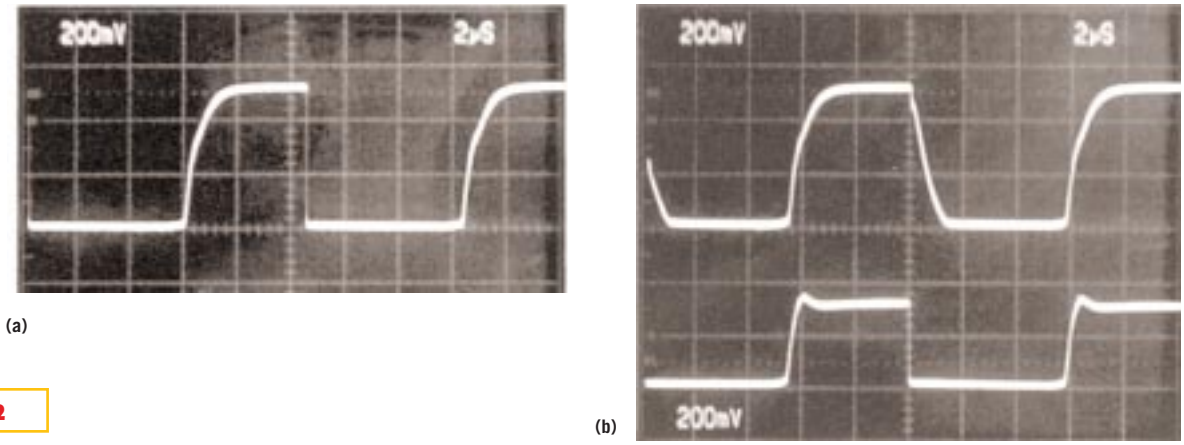


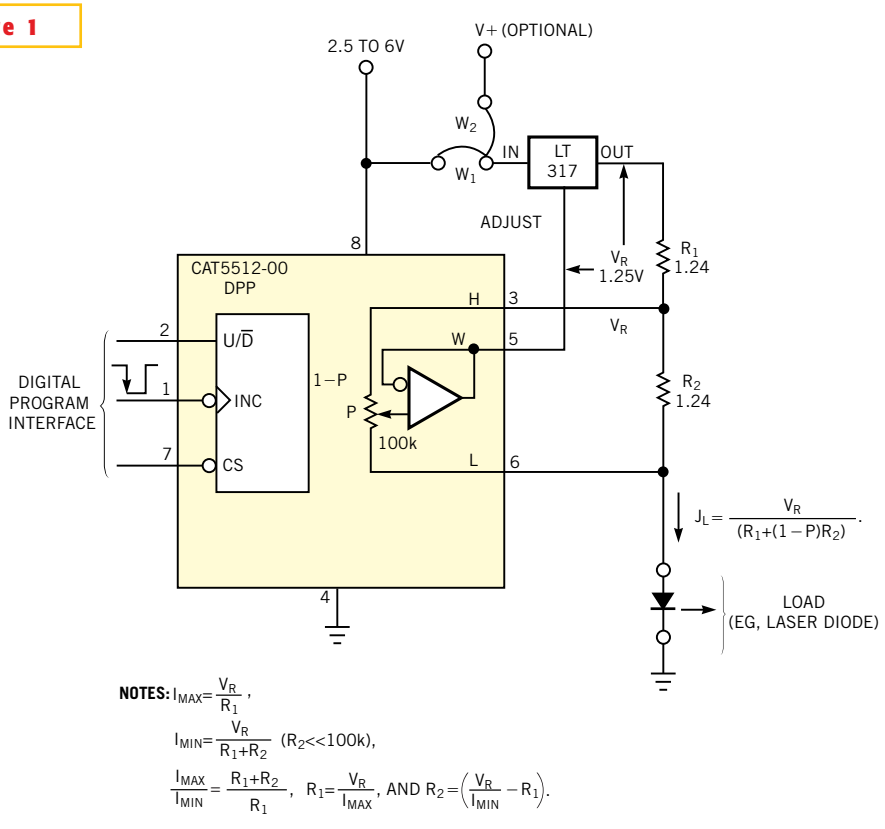
Figure 2

The 5V side (a) and the 3.3V side (b) drive operation with the circuit.

Digital current source is nonvolatile

Stephen Woodward, University of North Carolina, Chapel Hill

Figure 1



This digitally programmable current source is suitable for driving VCSELs in communications equipment.

Digitally programmable current sources that feature automatic trimming and retain the setting despite power-down cycles are useful in applications such as RF- and laser-communications drivers. The circuit in **Figure 1**, for example, is particularly suited for setting the drive current for the optical pump in widely tunable VCSELs (vertical-cavity surface-emitting lasers). These lasers are suitable in systems using wavelength-agile DWDM fiber-optic communication links. The circuit in **Figure 1** delivers a stable drive current that derives its control from DPP (digitally programmed potentiometer), a Catalyst Semiconductor (www.catsemi.com) CAT5512. For the circuit values shown, you can set the output current to 500 mA to 1A; however, you can alter this span over a wide range by the judicious selection of sense resistors R_1 and R_2.

The unique features of the CAT5512 make possible the low component count (two chips and two resistors). The device combines a 5-bit-resolution, 100-kΩ DPP, a nonvolatile EEPROM for long-term storage of the DPP setting, and a unity-gain analog-wiper-buffer amplifier. The DPP provides a complete digital interface of the LT317 precision regulator chip to the R_1, R_2 split current-sense-resistor network. The result is a robust, precision programmable current source with 5-bit resolution over a flexible I_{MIN} to I_{MAX} range. The basis of circuit operation is the fact that the LT317 regulator generates the current necessary to maintain a constant 1.25V across the effective sense resistance: $R_1+(1-p)R_2$, where p is the DPP setting: 0, 0.032, 0.064, 0.097, ..., 0.98, 1. In this way, $I_1=1.25V/(R_1+(1-p)R_2)$ over the range of $I_{MIN}=1.25V/(R_1+R_2)$ for p=0 to $I_{MAX}=1.25V/R_1$ for p=1. The pertinent design equations are $R_1=1.25V/I_{MAX}$, and $R_2=1.25V/I_{MIN}-R_1$.

Note that the R_2 equation is an approximation, based on the assumption that R_2 is much lower than 100 kΩ, the parallel DPP resistance. The full expression for R2 is:

$R_2=1/(1/((1.25V/I_{MIN})-R_1)-1/100\,k\Omega)$.

You exert control of the DPP setting "p"—and storage of the setting in nonvolatile EEPROM—via the three-wire digital interface, as described in the CAT5512 data sheet. The load-voltage-compliance limit is a function of the W_1 and W_2 V+ supply jumpers, connected to the LT317. The maximum output voltage is the difference between the LT317's input voltage and the sum of the LT317's dropout voltage (approximately 2V) and the voltage drop across the R_1+R_2 series resistance: $V_{MAX}=V+ - 2V-I_{MAX}(R_1+R_2)$. In the circuit in **Figure 1**, this voltage is V+ − 4.5V. This arithmetic leads to a V_{MAX} of only 500 mV if you use the W_1 option and V+ = 5V. This compliance figure may be insufficient for some applications. If, by contrast, you choose the W_2 option and V+ is greater than 7.5V (not necessarily regulated), V_{MAX} increases to a much more adequate 2.5V.

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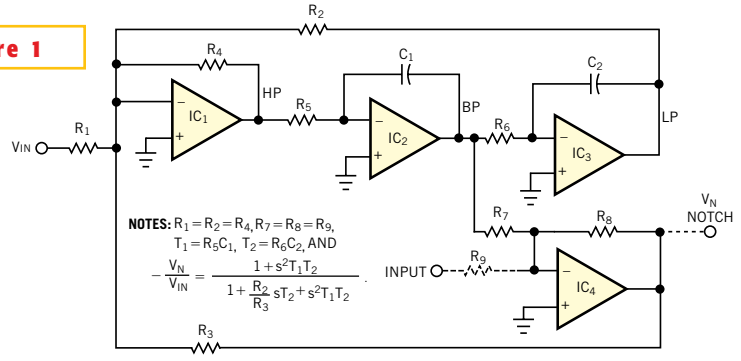
Closing the loop deepens notches

Tom Napier, North Wales, PA

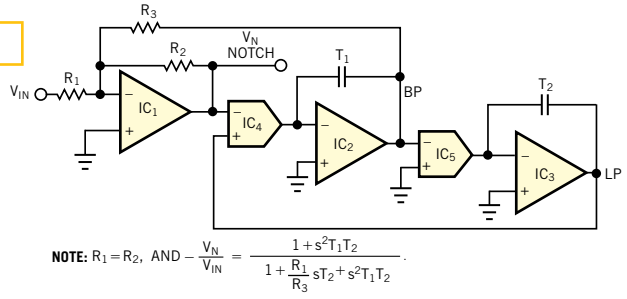
Notch filters remove a single unwanted frequency from an input signal. They are also a vital component of pulse-shaping networks, such as time-averaging filters. You can tune a state-variable filter over a wide range by changing the time constants of its integrating amplifiers (**references 1**, **2**, and **3**). Textbooks focus on its highpass, bandpass, and lowpass outputs, but they sometimes fail to note that subtracting the bandpass output from the input signal creates a notch filter. The attenuation of such an open-loop notch filter is limited by how well the components match; typically, it's approximately 40 dB. **Figure 1** shows a standard state-variable filter with an amplifier, IC_4, added to invert the bandpass output. You can implement a notch filter by adding a further amplifier to sum the input signal and the output of IC_4.

Figure 1



Changing connections makes the depth of the notch depend only on the gain of the integrating amplifiers.

Figure 2



Replacing two resistors by multiplier ICs results in a tunable notch filter.

An alternative is to move the input to R_9 and to take the notch output from the output of IC_4. Closing the loop around the notch filter makes the depth of the notch depend only on the gain of the integrating amplifiers. Replacing R_5 and R_6 by differential-input, current-output multipliers (for example, the Harris HA2547) creates the tunable notch filter in **Figure 2**. The time constants T_1 and T_2 are the products of the values of the integrating capacitors and the multipliers' transimpedances. In **Figures 1** and **2**, R_3 controls the width of the notch.

References

1. Napier, Tom, "Multipliers implement tunable filters," *EDN*, March 16, 1992, pg 131.
2. Siu, Chris, "Design innovations provide for voltage-tunable, state-variable active filters for megahertz ranges," *EDN*, Sept 28, 1995, pg 117.
3. Napier, Tom, "Take tunable lowpass filters to new heights," *EDN*, Jan 15, 1998, pg 145.

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Hints and kinks for USB decoding

Bert Erickson, Fayetteville, NY

The USB is a serial data-transmission system that uses cables to connect peripheral equipment to PCs. All new computers have two or more USB receptacles, and the predictions are that they will replace most of the legacy receptacles on older PCs. The 1.0 and 1.1 standards for USB were for 1.5 and 12 Mbps at low- and full-speed rates, respectively. These standards targeted low- and medium-speed peripherals. The latest 2.0 standard is for a 480-Mbps rate that will accommodate many high-speed devices along with the previous low- and full-speed rates. At the PC-accessible USB receptacle and at the peripheral, if it has a receptacle, the signal has the format of differen-

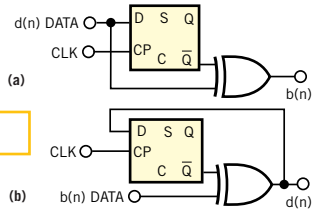
TABLE 1–BINARY VERSUS DIFFERENTIAL-NRZI CODE

Binary		Differential NRZI				
b(n − 1)	b(n)	d(n − 1)	d(n)	or	d(n − 1)	d(n)
0	0	1	0		0	1
0	1	0	0		1	1
1	0	0	1		1	0
1	1	1	1		0	0

tial-NRZI (nonreturn-to-zero-inverted) code. After conversion (with a simple circuit or test probes) of this differential to single-ended signal, the signal becomes a waveform that assumes the voltage levels used to recognize ones and zeros in computer code.

In this NRZI waveform, a transition between the d(n−1) and d(n) bits decodes to a binary b(n)=0 data bit. No transition decodes to a binary b(n)=1 bit. However, when you display the d(n) waveform on an oscilloscope of a logic analyzer, it is difficult for an observer to decode it back to the originating binary waveform, or vice versa. In this situation, you may doubt your judgment and turn to dedicated test equipment to make the conversion. Much of the human problem occurs because NRZI decoding depends on knowledge of the previous and current input bits to determine a value for the current output bit. In the encoding descriptions in most textbooks and technical articles, the transitions receive passing mention, and the material presents a pair of waveforms with little or no elaboration. The following suggestions involve some computer statements and logic circuits that provide a different way to effect the conversion.

Figure 1



Simple circuits perform NRZI-to-binary (a) and binary-to-NRZI (b) conversion.

Table 1 shows all the combinations that can exist in NRZI encoding. For the differential-NRZI-d(n)-to-binary-b(n) code conversion, the following observations apply:

- The conversion is independent of b(n−1).
- If d(n−1)≠d(n), then b(n)=0.
- If d(n−1)=d(n), then b(n)=1.
- Or, simply, b(n)=d(n) XOR NOT d(n−1).

You can perform the conversion by using an XOR gate and a 74LS74 D-type, positive-edge-triggered flip-flop (**Figure 1a**). The flip-flop's Set and Clear terminals connect to V_{CC}, and you do not need to reset either one. For the binary b(n) to differential NRZI d(n) conversion, we offer the following observations:

- The conversion is not independent of d(n−1).

d(n)=d(n−1) *unless*

- b(n−1)=0 AND b(n)=0, then d(n)=NOT d(n−1), or
- b(n−1)=1 AND b(n)=0, then d(n)=NOT d(n−1).

You can perform the conversion by using an XOR gate and a 74LS74 D-type positive-edge-triggered flip-flop (**Figure 1b**). The flip-flop's Set and Clear terminals connect to V_{CC} *after* you use them to set d(n) to its proper initial value. For all input-data sequences that keep repeating, you must select the last and first bits to produce the first output bit. You can download a computer program that confirms the decoding from the Web version of this article at www.ednmag.com.

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design ideas

Edited by Bill Travis

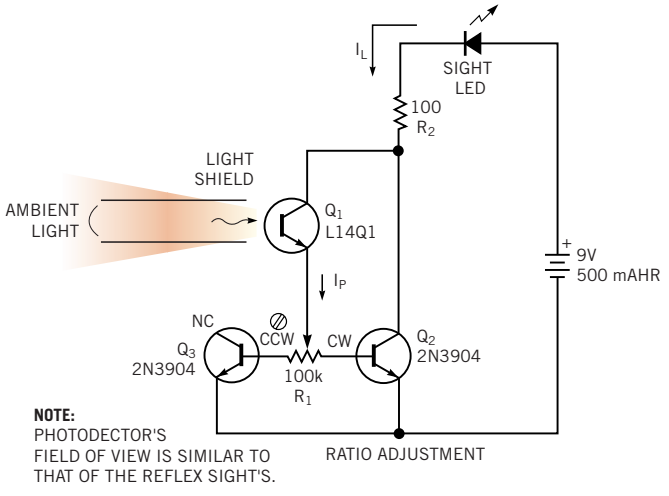
Circuit controls intensity of reflex optical sights

Stephen Woodward, University of North Carolina, Chapel Hill, NC

A POPULAR CATEGORY of aiming/pointing aids is the reflex, or "red-dot," sight. This system finds use in such diverse applications as astronomy, archery, and shooting. In the reflex sight, light from an internal source—typically a high-intensity red LED—reflects from a curved, transparent optical (reflex) element through which you view the target. The result of this geometry is that the image of the LED (the red dot) appears superimposed on the target image, thus indicating the point of aim. When you correctly adjust the aiming point of the telescope, bow, or gun, the target and LED images coincide. The reflex sight offers several advantages over competing pointing technologies, such as telescopic and open sights. These benefits include rapid and intuitive target acquisition, noncritical eye positioning, and a wide field of view.

For best sight performance, the intensity of the red-dot light source must at least roughly match the illumination level of the target. Otherwise, if the source is too dim, the aim-point dot loses itself in the brightness of the target. If too bright, the dot flares, and its apparent size increases, obscuring the point of aim and making precise pointing difficult or impossible. For this reason, most reflex sights require manual adjustment of the source intensity. Although this adjustment is effective enough, the time and attention needed to optimize intensity with a manual control detracts from the fast and intuitive target-acquisition capabilities of the red dot. The circuit in **Figure 1** uses phototransistor Q_1 to sense target brightness and automatically adjust the LED output. The circuit maintains near-constant dot size over a wide range of ambient-light levels.

Figure 1



This simple circuit automatically adjusts red-dot intensity in reflex optical sights.

Potentiometer R_1 divides Q_1's photocurrent, I_P, between the LED driver, Q_2, and the bias transistor, Q_3 (connected as a diode). The adjustment of R_1 therefore determines the ratio between drive current, I_L, and ambient (target) intensity over the range of 1 to B, where B is the beta of Q_2 (greater than 100). The prototype of the intensity-control circuit was packaged in a small plastic enclosure attached to the side of a Compasseco Inc (www.compasseco.com) Tech Force model 90 30-mm objective reflex sight. The light shield mimics the field of view of the sight, so the light that Q_1 samples represents the target intensity visible through the sight. Proper adjustment of R_1 results in good compensation of dot intensity for a wide range of both incandescent and natural light. The circuit effectively maintains a constant angular dot diameter of 4 minutes of arc under outdoor ambient lighting ranging from dark overcast to full sunlight. The circuit also delivers similar performance under indoor incandescent-lighting conditions. Compensation with fluorescent lamps, however, is less satisfactory because of the absence of an adequate near-infrared component in the spectrum of these light sources. You could probably fix this shortcoming by using a suitable visible-light filter in front of Q_1.

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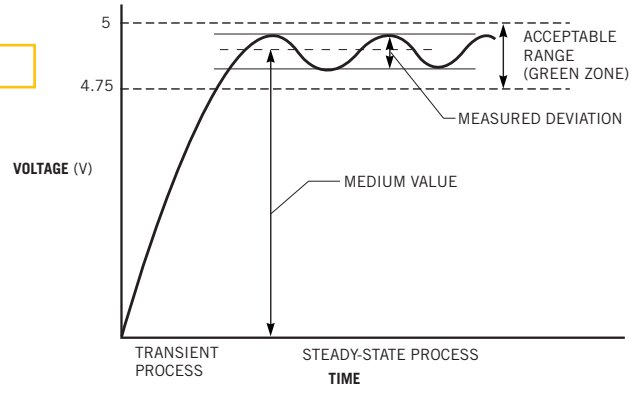
Indicator features expanded scale

Abel Raynus, Armatron International, Melrose, MA

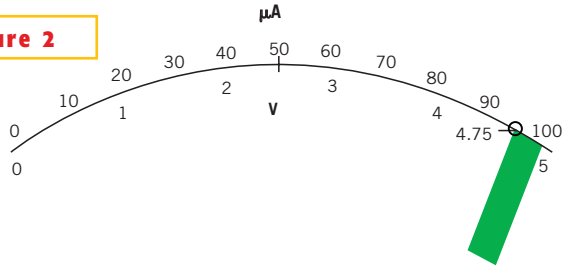
Test equipment for a production line should be user-friendly (read "idiot-proof") and should offer minimal test time. In many cases, the test fixture must give an operator only one answer: pass or fail. Usually, two indicators assume this role: green for pass and red for fail. In most applications, a sensor transforms the tested parameter to a voltage; the test fixture must measure this voltage and display the result. Sometimes, an operator needs to observe the dynamics of the tested parameter to verify that the results are inside the permitted "green zone." For example, when evaluating a regulated system's behavior, the operator is often interested in measuring the parameter's deviation and estimating its average value after the process reaches steady state (**Figure 1**). In this situation, using an analog meter with marked red and green zones is preferable to using a digital or bar-graph LED display.

Figure 1



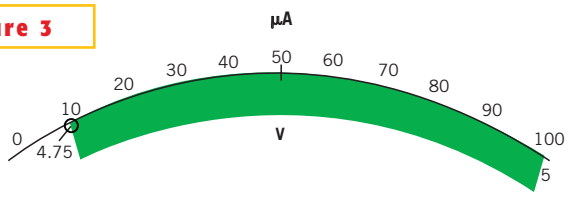
It's desirable to observe deviations in values inside the acceptable "green zone."

Figure 2



It's difficult to discern deviations from the norm when the green zone represents only 10% of full-scale.

Figure 3

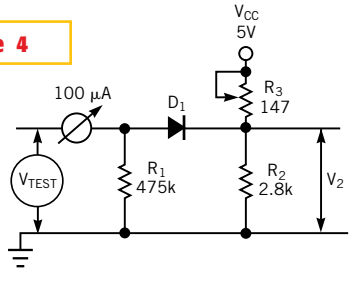


Expanding the green zone to 90% of full-scale makes readings much easier.

Assume that the range of the tested voltage is 4.75 to 5V. To make a voltmeter with maximum 5V reading by using a 100-µA dc meter, you would use a series resistor of 50 kΩ. The meter scale is linear, and the tested voltage zone represents only 5% of full-scale (**Figure 2**). It is difficult for an operator to observe the meter reading inside such a narrow zone. It would be desirable to expand the test zone to, say, 90% of full-scale (**Figure 3**). The circuit in **Figure 4** does just that. When the tested voltage, V_{TEST}, is lower than the threshold voltage, V_2, the diode, D_1 does not conduct, and the voltmeter comprises the microammeter and resistor, R_1. When the tested voltage surpasses the threshold V_2, the diode conducts, and resistor R_2 connects in parallel with R_1. The voltmeter's impedance decreases, thereby expanding the measurement scale. You can calculate the values of resistors R_1, R_2, and R_3 as follows:

- The voltage at the beginning of the tested zone, 4.75V, should consume 10% of the scale, with a corresponding current of 10 µA. Hence, neglecting the internal meter impedance, R_1 equates to 4.75V/10 µA, or 475 kΩ.
- After the measured voltage exceeds the threshold level, 4.75V, the voltmeter impedance equates to $R_{1,2}=(5-4.75)V/(100-10)$ µA, or 2.8 kΩ.
- Hence, $(R_1R_{1,2})/(R_1-R_{1,2})=(475\times 2.8)/(475-2.8)=2.8$ kΩ, and $R_3=R_2(V_{CC}/V_2-1)=2.8\ (5/4.75-1)=147\Omega$.

Figure 4



This simple circuit expands the acceptable test results to 90% of full-scale.

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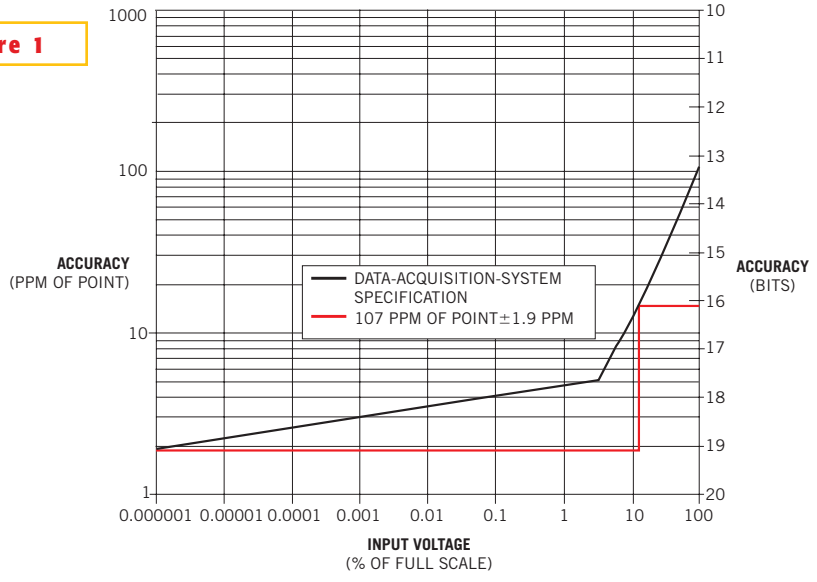
16-bit ADC provides 19-bit resolution

Alain Guery and Charles Kitchin, Analog Devices, Wilmington, MA

Many data-acquisition systems require both high accuracy and a fast acquisition rate. These attributes allow the system to detect small data signals and to group more sensor channels into the same system. With more channels, the system can be smaller, less expensive, and less power-consuming. Long-distance optical communications and medical equipment, such as CT scanners, can benefit from a fast and accurate data-acquisition system. Optical power systems, such as laser pumps, need to constantly monitor their power levels. In such systems, the incoming laser-power range and the laser control-loop response time are such that the system needs a dynamic range of 90 dB or more and a sampling rate of 1M sample/sec. In CT scanners, 16- to 22-bit resolution is necessary for the data-acquisition system to process the large dynamic range of the X-rays through various body tissues. A large number of photodetectors (more data-acquisition channels) and high data accuracy improve the image resolution.

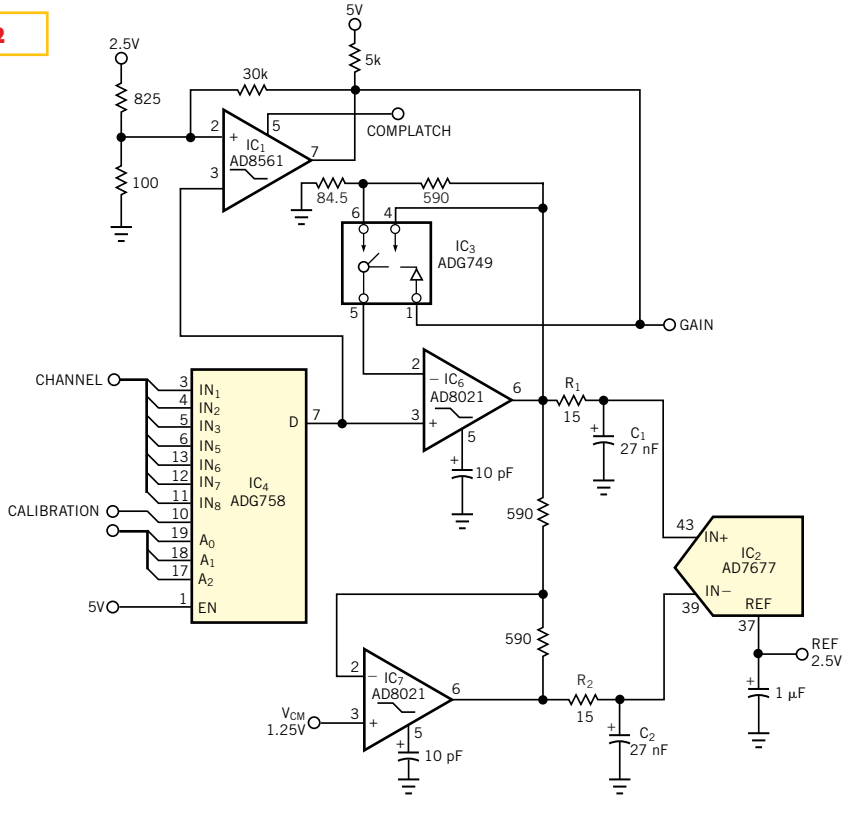
These two examples show the need for relative accuracy, as opposed to absolute accuracy. Although it's important to be able to detect a 10-nW change in an optical power of 1 µW, it is almost irrelevant to see the same 10-nW difference between 1 mW and 1.00001 mW. However the ADC's accuracy appears under the integral-nonlinearity specification as an absolute error. For the best relative accuracy, a classic solution is to use a programmable-gain amplifier in front of an accurate ADC. The AD7677 ADC specifies ±15-ppm of full-scale nonlinearity (±1 LSB at the 16-bit level). A programmable-gain amplifier ahead of this converter must be able to settle

Figure 1



Using a programmable-gain amplifier ahead of an ADC increases the accuracy of a 16-bit ADC to 19 bits.

Figure 2



This system provides 19-bit accuracy by combining a programmable-gain amplifier with a 16-bit ADC.

quickly enough with the same resolution and speed as the ADC. It also must have the lowest noise possible, because the amplifier sets the SNR of the data-acquisition system. To meet these challenges, the amplifier in this design uses an AD8021, an op amp combing speed, accuracy, and fast settling time. The noise density of the AD8021 is only 2 nV/$\sqrt{\text{Hz}}$. **Figure 1** shows how the gain settings of the programmable-gain amplifier divide the specified accuracy of the ADC. The system reaches 19-bit accuracy when the input level is low.

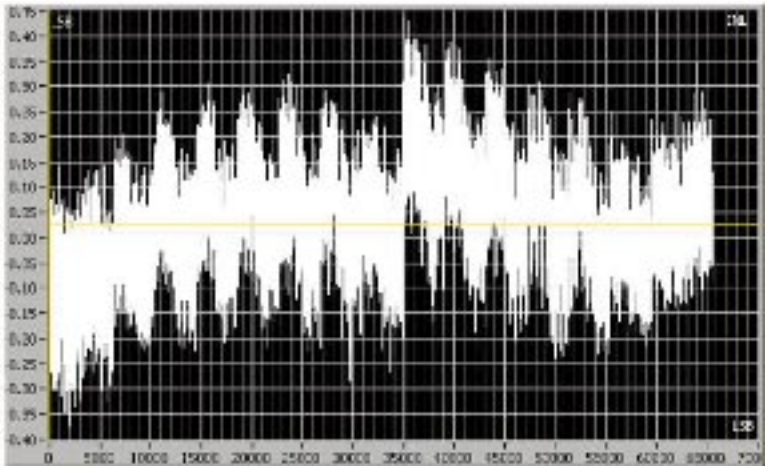
Relative accuracy is normally specified as parts per million of reading plus or minus the absolute minimum error. The circuit in **Figure 2** can achieve a relative accuracy of 107 ppm±1.9-ppm maximum error. Analog multiplexer IC_4 combines many lower bandwidth channels to take advantage of the 1M-sample/sec sampling rate of the ADC. Because the programmable-gain amplifier presents a high input impedance to the multiplexer, you can cascade the multiplexer, thus increasing the number of channels. The multiplexer also provides a simple way to calibrate the offset and gain errors at each gain setting by applying a calibration-reference voltage to one of the multiplexer's input ports. You need to calibrate only at power-up or when operating conditions, such as temperature, change. The amplification chain comprises the multiplexer, the comparator, and the amplifier on one side and the ADC on the other side. The successive-approximation structure of the AD7677 ADC allows the individual sections in the amplification chain to work simultaneously. While the ADC converts one sample, the comparator/amplifier can settle the following channel. Therefore, the data-acquisition system can operate at the ADC's maximum sampling rate.

Shortly after the analog multiplexer settles, the fast comparator, IC_1, applies the appropriate gain setting. The comparator's thresholds are such that the amplifier does not saturate or clip the signal after amplification by IC_6 and IC_7. The AD8561 comparator has a response time of 7 nsec. It integrates a latch signal that holds the gain constant during the time the amplifier settles and the ADC acquires the signal. The usual programmable-gain-amplifier configuration requires the user to predict the amplifier's gain setting before applying the signal at the input. The programmable-gain amplifier in **Figure 2** has an "autorange" feature that selects the most appropriate programmable-gain amplifier gain to maximize accuracy without incurring saturation or clipping. The comparator incorporates hysteresis to reduce gain-setting change when signals are close to the limits of an individual gain range. The circuit automatically boosts the ADC accuracy to 19 bits while maintaining a full-speed sampling rate of 1M sample/sec.

IC_6 amplifies the multiplexer signal using one of two possible gain settings: 1 or 8. You can modify the feedback network to provide different gains to a maximum of 25. The analog switch, IC_3, controls the gain setting. The high gain-bandwidth product of the AD8021 op amp provides more than enough bandwidth, so its compensation capacitor remains the same for all gains. Amplifier IC_7 generates the differential signal for the ADC. The settling times of the comparator and the amplifier and the acquisition time of the ADC are all significantly less than the ADC's full conversion period of 1 µsec. The RC noise filters at the two ADC inputs, R_1/C_1 and R_2/C_2, use this extra time. These filters limit the noise bandwidth of the programmable-gain amplifier, which is the main noise source of the data-acquisition system when IC_7 operates at a gain of −1.

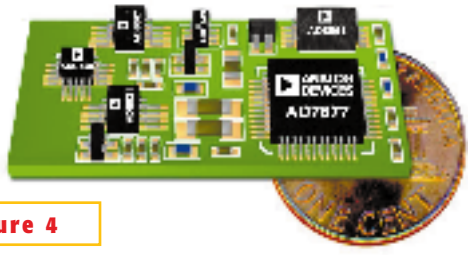
Figure 3 shows the circuit's nonlinearity. The photo shows a maximum nonlinearity of 0.44 LSB and a minimum of −0.37 LSB for the highest gain setting, which poses the most difficult challenge. This nonlinearity corresponds to a typical error of ±0.9 ppm. At a gain of 8, output noise is 85 µV rms. If desired, you can further reduce the noise by using software averaging. **Figure 4** shows the complete data-acquisition system assembled using the AD7677 evaluation board. The pc-board area measures 15×30 mm.

Figure 3



This plot shows the differential nonlinearity of a data-acquisition system for all possible ADC codes.

Figure 4



The dime shows the relative size of the complete data-acquisition system.

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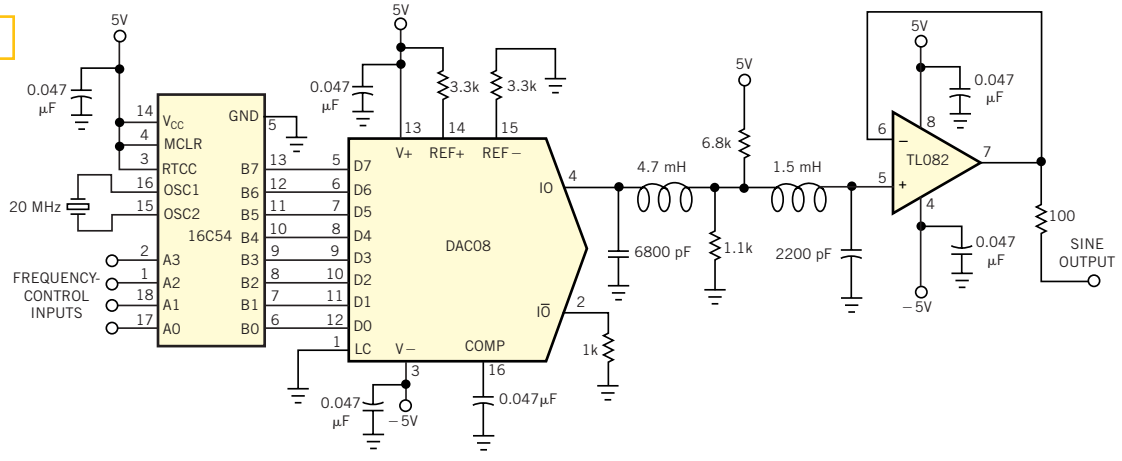
Microcontroller emulates numerically controlled oscillator

Tom Napier, North Wales, PA

Microcontrollers commonly add intelligence or digital functions to products, but they can also provide a variety of analog signals. An 18-pin PIC 16C54 microcontroller, combined with an inexpensive, 8-bit DAC and a simple lowpass filter, can generate sine waves from dc to approximately 50 kHz with a tuning resolution of 24 bits. The accuracy and stability of the output is as good as that of the crystal driving the microcontroller. You can connect a binary data signal to one or more PIC ports to apply FSK (frequency-shift-keying), BPSK (binary-phase-shift-keying), or QPSK

Figure 1



An inexpensive microcontroller and DAC emulate a numerically controlled oscillator.

LISTING 1—16C54 NUMERICALLY CONTROLLED OSCILLATOR-EMULATION ROUTINE

```
START   MOVLW   0
        TRIS    PORTB           ;Set port B to output
        MOVWF   PHASL           ;Initialize phase
        MOVWF   PHASM
        MOVWF   PHASH
        MOVWF   ZER             ;Constant = 256
        MOVLW   64
        MOVWF   MAX             ;Constant = 64

; Set up default frequency, here 1000 Hz

        MOVLW   64
        MOVWF   FREQL
        MOVLW   150
        MOVWF   FREQM
        MOVLW   1
        MOVWF   FREQH

        GOTO    DONE

; Set up fixed return address in stack

RETX    CALL    RETY
        GOTO    LOOP            ;Start generating output

RETY    RETLW   0               ;Dummy to fix return address

DONE    CALL    RETX            ;Set up fixed return address

; Look-up return reenters at this point with sine sample in W

LOOP    BTFSC   TEMP,INV        ;Test if inversion needed
; Replace previous instruction by BTFSC PHASH,INV
; if BPSK modulation not needed.
        SUBWF   ZER,0           ;Invert output
        MOVWF   PORTB           ;Output sample

; Check if user wants to load a new frequency
        BTFSC   PORTA,DAT       ;Test for change flag
        GOTO    NEW             ;Get new user frequency
```

```
; Three-byte addition of control to phase accumulator
        MOVF    FREQL,0         ;Get frequency low byte
        ADDWF   PHASL,1         ;Increment phase low byte
        MOVF    STATUS,0
        ANDLW   1               ;W = carry
        ADDWF   PHASM,1         ;Add carry
        BTFSC   STATUS,CY       ;Skip if no carry
        INCF    PHASH,1         ;Propagate carry
        MOVF    FREQM,0         ;Get frequency mid byte
        ADDWF   PHASM,1         ;Increment phase mid byte
        BTFSC   STATUS,CY       ;Skip if no carry
        INCF    PHASH,1         ;Propagate carry
        MOVF    FREQH,0         ;Get frequency high byte
        ADDWF   PHASH,1         ;Increment phase high byte

        SWAPF   PORTA,MOD       ;Modulation input to bit 7
        XORWF   PHASH,0         ;XOR inversion bit
        MOVWF   TEMP            ;Save inversion bit
; Remove above three instructions if modulation not needed.

        MOVF    PHASH,0
        ANDLW   63              ;Get table index
        BTFSC   PHASH,REV       ;Test if reversal needed
; Replace above instruction by BTFSC TEMP,REV for QPSK

        SUBWF   MAX,0           ;Reverse index direction
        ADDWF   PC,1            ;Jump to table

; Partial sine look-up table
; 65 entries - sines of first quadrant

        RETLW   128
        RETLW   131
        RETLW   134
        :
        :
        RETLW   255
```

(quadrature-phase-shift-keying) modulation to the output. **Figure 1** shows the emulation scheme, and **Listing 1** controls the operation of the microcontroller. The 16C54's firmware emulates a 24-bit numerically controlled oscillator. A fixed-length loop continuously adds the contents of one set of registers (the frequency control) to another set (the phase accumulator). The phase accumulator increments at a rate proportional to the desired output frequency and wraps around once per output cycle.

With a 24-bit accumulator, the output frequency is $f \times N/[67108864(L+2)]$, where f is the clock frequency, N is the tuning control number, and L is the number of instructions in the loop. (The loop period is two instruction times longer than the instruction count, L.) For example, if the PIC's clock crystal's frequency is 16.777 MHz, and the loop has 30 instructions, you can set any frequency to approximately 40 kHz in steps of 1/128 Hz. Once per loop, the highest byte of the phase accumulator selects an output sample from a 65-element look-up table, which contains one quadrant of a sine wave. To create the other three quadrants, bit 6 determines whether to read the table forward or backward, and bit 7 specifies the output sign. An exclusive-OR operation on bit 7 with a port bit generates BPSK operation. An exclusive-OR operation on both bits 6 and 7 with port bits generates QPSK modulation. The result goes to the DAC via the PIC's 8-bit output port. A 50-kHz lowpass filter then converts the DAC's output into a smooth sine wave.

You can preset the output frequency or load it serially via two pins of the PIC's 4-bit port. You obtain FSK by using an input bit to select which of two frequency-control registers to use. If the two frequencies have a large common multiple, as in minimum-shift keying, the accumulator can be shorter, leading to a higher output frequency for a given clock input. Without modulation, the firmware loop can be as short as 26 instruction times (**Listing 1**). You can insert nonoperation instructions to make the loop-repetition rate a convenient submultiple of the crystal frequency. For example, a 31-instruction loop and a 20-MHz crystal yield a scale factor close to 104 steps/Hz.

The code takes advantage of a quirk in the 16C54's operation: If two addresses exist on the return stack, the first copies endlessly into the second every time the routine pops the second. The initialization code puts two copies of the loop-start address into the return stack, causing all subsequent RETLW instructions to jump to the start of the loop. Indexing into the look-up table with a calculated GOTO instruction both supplies an output sample and executes a jump to restart the loop. This procedure is much faster than executing a CALL, a GOTO, a RETLW, and a further GOTO. You can download **Listing 1** from the Web version of this article at www.ednmag.com.

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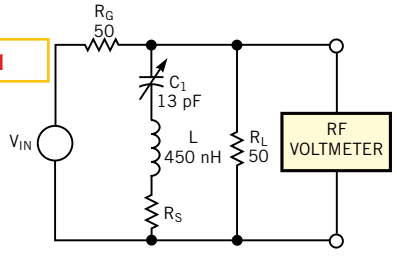
Method simplifies testing high-Q devices

Alan Victor, IBM Microelectronics, Research Triangle Park, NC

THE DESIGN of low-phase-noise oscillators requires careful attention to resonator unloaded Q. In the construction of a low-phase-noise, high-frequency oscillator, the goal is to achieve an unloaded-Q figure greater than 400 in a reasonable package. Also, you need to monitor the effect of the package and pc-board arrangement. Shielding, inappropriate grounding, and some construction techniques can degrade unloaded Q. Q meters; various bridges, such as Maxwell and Hayes; and both vector and scalar impedance analyzers are useful but inconvenient-to-use test instruments. You must carefully set up test fixturing and calibration that duplicates the final environment to obtain reasonable agreement with the final measured results. A simple test set uses nothing more than the voltage-divider relation with the device under test embedded as a series trap network (**Figure 1**). You can measure the inductor's value, or calculate it from known equations based on the inductor's form factor, such as solenoid, toroid, helical, or flat spiral. You use the inductor's value to select C_1, a variable, air-dielectric high-Q capacitor. At resonance, the impedance of the inductor-capacitor combination goes to zero, so the effective load is the series resistance R_S in parallel with the 50Ω termination resistance.

Figure 1



A simple test set allows you to determine the unloaded Q of an inductor.

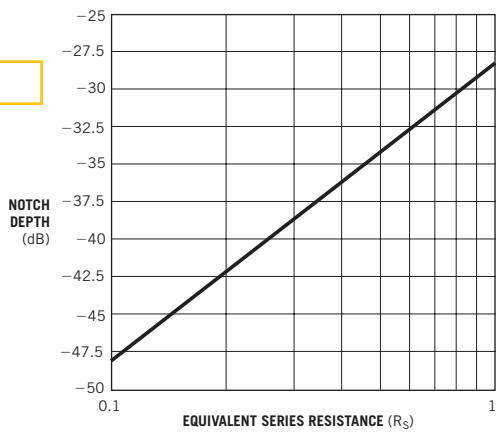
TABLE 1–NOTCH DEPTH VERSUS SERIES RESISTANCE

R_S (Ω)	Notch depth (dB)
0.1	−47.993
0.2	−42.007
0.3	−-38.52
0.4	−36.055
0.5	−34.151
0.6	−32.602
0.7	−31.297
0.8	−30.171
0.9	−29.181
1	−28.299

You use an RF generator and voltmeter to read the depth of the notch the trap creates. This attenuation depth is a function of the remaining finite-series resist-

ance of the resonator. **Table 1** shows the notch attenuation for R_S ranging from 0.1 to 1Ω. These values assume 50Ω source and termination impedance and the component values shown in **Figure 1**. Unloaded Q equates to X_L/R_S, where X_L is the reactance of the inductor, and R_S is the equivalent series resistance. **Figure 2** shows the notch attenuation as a function of the equivalent series resistance. In addition, a crosscheck is available: You can the 3-dB bandwidth of the notch and calculate unloaded Q from f_0 divided by the bandwidth. Finally, as a "sanity check," you can readily reduce the unloaded Q to a known value by inserting a series resistance in the trap circuit. The reduction in unloaded Q should correlate with added resistance value. Any variations you notice in these simple experiments are usually the result of subtle factors. One factor in particular is a component operating near its self-resonant frequency. In the test case of **Figure 1**, six-gauge wire on a 0.75-in. Delron rod with careful construction lets you achieve unloaded Q near 500 at 70 MHz. The measurement technique unveils issues with shielding, namely the reduction in Q from the effect of the shield on the solenoid coil. The details of the measurement are as follows:

Figure 2



The notch depth of the circuit in Figure 1 at resonance is inversely related to the equivalent series resistance of the inductor.

Assume an inductor with known L and X_L at a frequency of interest f_0. The inductor shall resonate in a series-tuned (trap) configuration, driven from a 50Ω generator and terminated in a 50Ω shunt. An RF voltmeter placed across the shunt reads notch depth in decibels. From **Figure 2**, you can determine the unloaded Q from the expression $Q=X_L/R_S$. For example, a solenoid inductor measuring 0.75 in. in diameter and wound with five turns of six-gauge wire has a measured inductance of 460 nH at 65 MHz. The inductor series-resonates at 65 MHz with a 13-pF capacitor. You set the signal generator at 65 MHz and use a variable, air-dielectric capacitor to fine-tune the notch at 65 MHz. The measured notch depth is 36 dB. R_S is 0.4Ω, and the unloaded Q is 469. You can readily notice changes in the depth of the notch with fine variations in coil position relative to conducting surfaces.

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design ideas

Edited by Bill Travis

Annual Design Ideas Grand Prize Winner

Frequent Design Ideas author takes home annual award

EDN is pleased to announce that Stephen Woodward's design entry is the grand-prize winner of *EDN*'s 2001 Design Ideas competition. Woodward will receive a $1500 check for his July 5 entry, "Quickly discharge power-supply capacitors," which we present again below in case you missed it the first time. Woodward is a frequent *EDN* contributor and previously won the annual award for his first submission to *EDN* in 1974.

The Design Ideas section is among the most popular features in *EDN*, because it embodies the traditional engineering challenge: An individual sees a well-defined and bounded problem; applies a mix of hardware, software, and algorithms; and produces an innovative solution to that problem. In many cases, the problem is unique or requires a solution that is complex and costly.

According to Woodward, "There's nothing quite like the satisfaction that comes from seeing your name in print attached to something that others find a useful idea. I've done over a hundred of these bite-sized articles, and the pleasure has never faded. The ideas that form the basis for my Design Ideas come from two basic sources. Some I develop specifically for publication. Others come from real-life applications. The circuit that won this year is one of these. The rapid and safe discharge of large power-supply filters is a problem I've been bothered by for years. The topology in this year's winning Design Idea is a solution I came up with only after long consideration. It has served me well in dozens of designs."

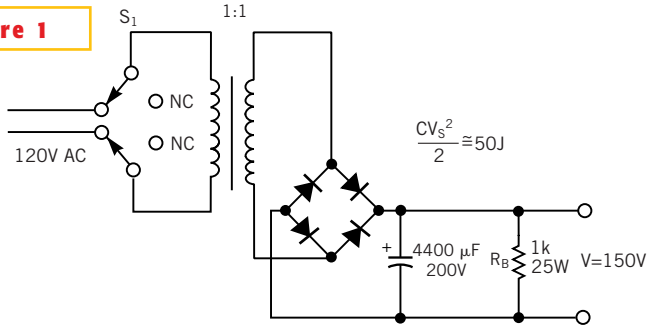
We congratulate Woodward on his achievement.

Quickly discharge power-supply capacitors

Stephen Woodward, University of North Carolina, Chapel Hill, NC

A perennial challenge in power-supply design is the safe and speedy discharge, or "dump," at turn-off of the large amount of energy stored in the postrectification filter capacitors. This energy, $CV^2/2$, can usually reach tens of joules. If you let the capacitors self-discharge, dangerous voltages can persist on unloaded electrolytic filter capacitors for hours or even days. These charged capacitors can pose a significant hazard to service personnel or even to the equipment itself. The standard and obvious solution to this problem is the traditional "bleeder" resistor, R_B (**Figure 1**). The trouble with the R_B fix is that power continuously and wastefully "bleeds" through R_B, not only when it's desirable during a capacitor dump, but also constantly when the power supply is on. The resulting energy hemorrhage is sometimes far from negligible.

Figure 1

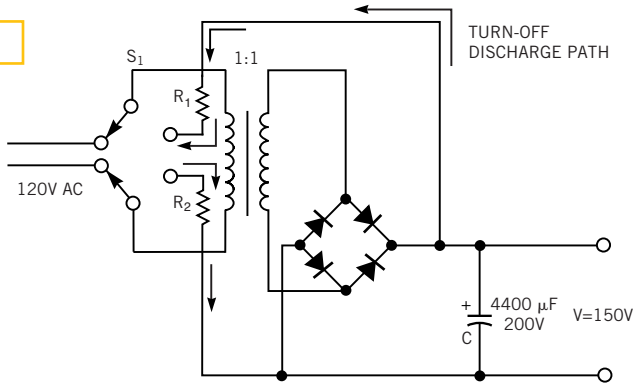


A bleeder resistor ensures safety but wastes much power.

Figure 1 offers an illustration of the problem, taken from the power supply of a pulse generator. The $CV^2/2$ energy stored at the nominal 150V operating voltage is $150^2 \times 4400\ \mu F/2$, or approximately 50J. Suppose that you choose the R_B fix for this supply and opt to achieve 90% discharge of the 4400-µF capacitor within 10 sec after turning off the supply. You then have to select R_B to provide a constant RC time no

longer than 10/ln(10), or 4.3 sec. R_B, therefore, equals 4.3 sec/4400 µF, or approximately 1 kΩ. The resulting continuous power dissipated in R_B is 150^2/1 kΩ, or approximately 23W. This figure represents an undesirable power-dissipation penalty in a low-duty-cycle pulse-generator application. This waste dominates all energy consumption and heat production in what is otherwise a low-average-power circuit. This scenario is an unavoidable drawback of bleeder resistors. Whenever you apply the 10%-in-10-sec safety criterion, the downside is the inevitable dissipation of almost half the $CV^2/2$ energy during each second the circuit is under power.

Figure 2



Otherwise unused switch contacts can dump energy while not wasting power.

Figure 2 shows a much more selective and thrifty fix for the energy-dump problem. The otherwise-unused off-throw contacts of the dpdt on/off power switch create a filter-capacitor-discharge path that exists only when you need it: when the supply is turned off. When the switch moves to the off position, it establishes a discharge path through resistors R_1 and R_2 and the power transformer's primary winding. The result is an almost arbitrarily rapid dump of the stored energy while the circuit suffers zero power-on energy waste. Use the following four criteria to optimally select R_1, R_2, and S_1:

- The peak discharge current, $V/(R_1+R_2)$, should not exceed S_1's contact rating.
- The pulse-handling capability of R_1 and R_2 should be adequate to handle the $CV^2/2$ thermal impulse. A 3W rating for R_1 and R_2 is adequate for this 50J example.
- The discharge time constant, $(R_1+R_2)C$, should be short enough to ensure quick disposal of the stored energy.
- S_1 must have a break-before-make architecture that ensures breaking both connections to the ac mains before making either discharge connection and vice versa. Otherwise, a hazardous ground-fault condition may occur at on/off transitions.

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High-side current sensor has period output

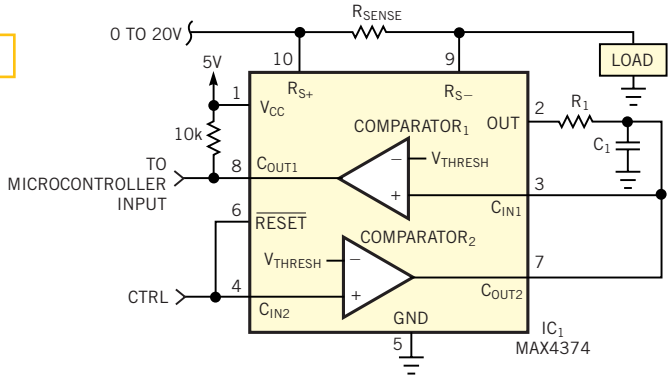
Greg Sutterlin, Maxim Integrated Products, Wexford, PA

Publish your Design Idea in *EDN*. See the What's Up section at www.ednmag.com.

You use high-side current monitoring in many battery-powered products that require accurate monitoring of load current, charger current, or both. In applications for nonportable designs, high-side-current monitoring serves as a power-supply watchdog that can flag a failure in downstream devices. The monitoring can also eliminate hazardous conditions by preventing power-supply overloads. Further, high-side-current monitoring of motor/servo circuits can produce useful feedback in control applications. These applications require a device that converts high-side current directly to a digital signal (**Figure 1**). IC_1 is a low-cost, high-side-current-sense amplifier that converts high-side current to a proportional, ground-referenced voltage. Its two internal comparators (latching and nonlatching) implement a voltage-to-pulse converter that produces an output pulse width proportional to the measured current.

IC_1's Out pin charges C_1 via R_1. When C_1's voltage reaches 0.6V, $Comparator_1$ latches in the high-impedance state. The time required to charge C_1 to 0.6V is proportional to the measured current. $Comparator_2$, in conjunction with the Reset pin, initiates the conversion and removes the previously existing charge on C_1. The Reset and C_{IN2} pins, tied together and connected to a TTL-compatible microcontroller output, CTRL, control the conversion process. Normally, CTRL is

Figure 1



The duration of a negative-going pulse at C_{OUT1} is proportional to the current flowing through R_{SENSE}.

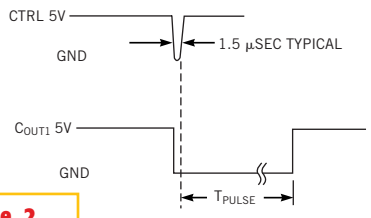


Figure 2

These waveforms illustrate the operation of the circuit in Figure 1.

high. The microcontroller starts a conversion by pulsing CTRL low, discharging C_1 and clearing the latch in comparator$_1$ (C_{OUT1} goes low.) The microcontroller now measures the time from the CTRL transition to the low-to-high transition at C_{OUT1} (**Figure 2**). The period begins at the low-to-high transition of CTRL and ends at the low-to-high transition of C_{OUT1}. As a function of the current levels of interest, you select R_1 and C_1 values to create pulse durations in the tens of milliseconds. As a result, the Out settling time of 20 µsec and the comparator propagation delays of 4 µsec have negligible effects on the measurement accuracy.

To derive an expression for the output pulse width, start with the relationship for an RC-charging circuit: $V_{THRESH} = Out(1-e^{-TPULSE/R_1C_1})$. For the Out-pin voltage, substitute the expression $I_{LOAD} \times R_{SENSE} \times A_V$ and solve for I_{LOAD}: $I_{LOAD} = V_{THRESH}/[R_{SENSE} \times A_V(1-e^{-TPULSE/R_1C_1})]$, where I_{LOAD}=measured current in amperes, V_{THRESH}=comparator threshold=0.6V, R_{SENSE}=current-sense resistor in ohms, A_V=gain of IC_1, and T_{PULSE}=time to charge C_1 to V_{THRESH} in seconds.

For example, selecting R_1=1 MΩ, C_1=0.1 µF, R_{SENSE}=0.075Ω, and A_V=20 produces a T_{PULSE} measurement of 0.022 sec in response to a 2A current. Thus, given a microcontroller timer port, an external interrupt, or simply an available microcontroller input, IC_1, and two external passive components implement high-side-current-to-digital conversion without the need for a discrete A/D converter.

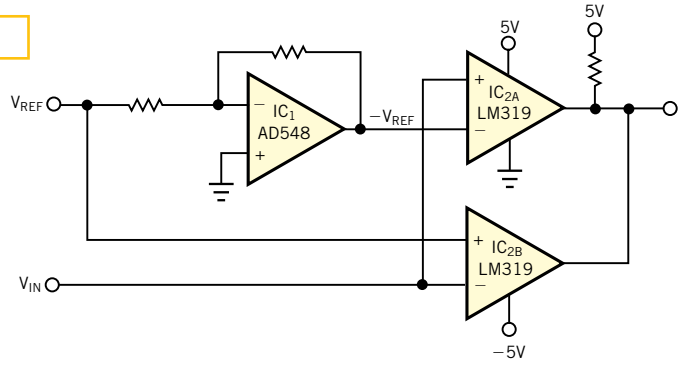
Is this the best Design Idea in this issue? Select at www.ednmag.com.

Absolute-value comparator touts accuracy, size

Teno Cipri, Engineering Expressions Consulting, Sunnyvale, CA

A TYPICAL WINDOW COMPARATOR uses two comparators and a single op amp to determine whether a voltage is inside or outside a boundary region. **Figure 1** shows a typical implementation. IC_1 is an inverting op amp with a gain of −1. V_{REF} and $-V_{REF}$ create the window limits. When V_{IN} becomes more positive than V_{REF}, the output of IC_{2A} goes low. When V_{IN} becomes more negative than $-V_{REF}$, the output of IC_{2B} goes low. If V_{IN} is lower than V_{REF} and greater than $-V_{REF}$, both outputs of IC_2 remain high. The LM319 and AD548 come in 14- and eight-pin DIPs, respec-

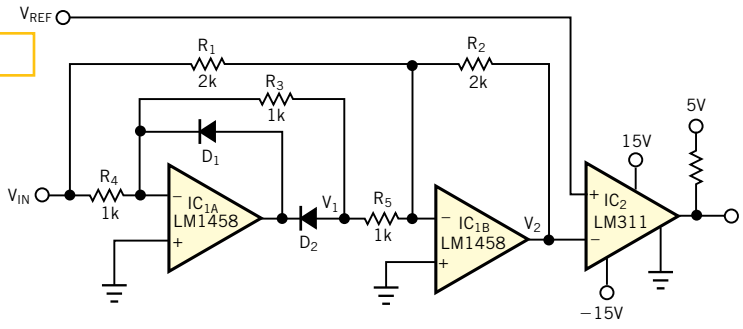
Figure 1



This traditional window-comparator circuit suffers from limited input range.

tively. The LM319 accommodates separate input and output power supplies. The input supply can be ±15V referenced to analog ground, and the output can use a logic supply referenced to logic ground. The circuit's input limit is ±2.5V because of the maximum differential-input limit of the LM319. If you think the input will exceed a ±5V differential voltage between V_{REF} and V_{IN} or $-V_{REF}$ and V_{IN}, then you must incorporate a clamping network with many additional discrete components. The circuit in **Figure 2** overcomes these limitations.

Figure 2



An absolute-value comparator circuit offers a wide input range and improved dc performance.

To increase the maximum differential-input voltage, you can use an LM311, but it is available only in eight-pin packages, so the circuit would require three eight-pin packages. To reduce the chip count, the circuit in **Figure 2** uses an absolute-value amplifier driving a single LM311 comparator, IC_2. Although at first glance the circuit in **Figure 1** may look simpler than the one in **Figure 2**, you can save pc-board area and improve performance by using a dual amplifier in a single eight-pin DIP and an LM311, also in an eight-pin DIP. In **Figure 2**, when the absolute value of V_{IN} exceeds V_{REF}, the output of comparator IC_2 goes low. When V_{IN} is positive, IC_{1A} inverts the signal, and the voltage at R_5 is equal to $-V_{IN}$. The current flowing through R_5 is −2 times that flowing through R_1, and the output of IC_{1B} is equal to V_{IN}. When V_{IN} is negative, D_2 blocks the output of IC_{1A}, which is clamped to the forward voltage of D_1. Because the inverting input of IC_{1A} and IC_{1B} are both at virtual ground, no current flows through R_3 and R_5. With IC_{1A} effectively out of the circuit, IC_{1B}'s gain is −1, and the output voltage is positive. The inverting-input voltage of IC_2 is always at a positive value. This circuit is symmetrical for positive and negative voltages. The following expressions define V_2: $V_2 = |V_{IN}| = -V_{IN} - (-2V_{IN})$ for positive inputs, and $V_2 = -V_{IN}$ for negative inputs.

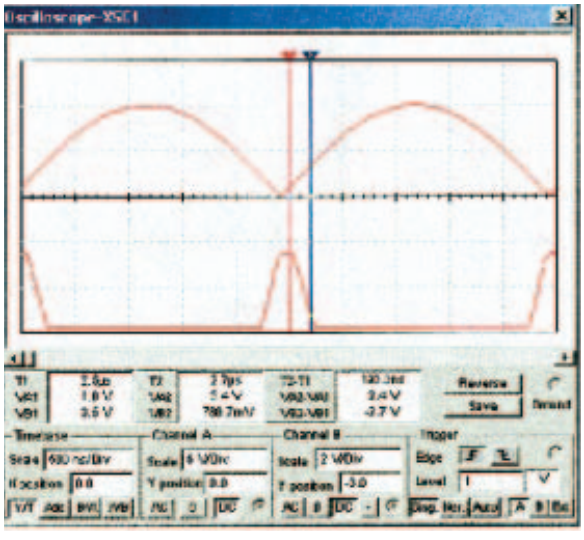
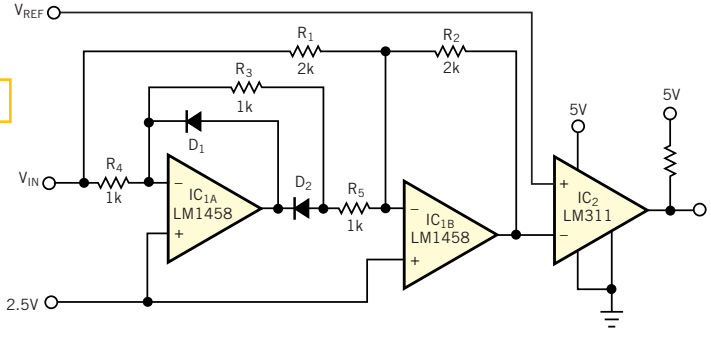


Figure 3

Channel A is the rectified (absolute-value) output of IC_{1B}; Channel B is the output of the comparator.

The dual comparators of **Figure 1** can have slightly different thresholds. You can select the dual op amps in **Figure 2** for input offsets below 1 mV; doing so allows the circuit in **Figure 2** to offer improved dc performance. Another advantage of the circuit in **Figure 2** is the fact that you need change only R_2 to set the gain of the circuit. Most comparators have offset voltages of several millivolts, so scaling up the input voltage improves accuracy by increasing the signal/offset ratio. The circuit in **Figure 1** would require the addition of another op amp to achieve this goal. The simulation in **Figure 3** shows the circuit response. Channel A is the output of IC_{1B}. Channel B is the output of the comparator with V_{REF} set at 1V. Marker 1 corresponds to the 1V threshold, and Marker 2 corresponds to logic low at the output of the comparator. The circuit in **Figure 4** is another variation of the circuit that uses a single 5V supply. It works for input signals of 0 to 5V and V_{REF} of 2.5 and 5V. The 0 and 5V inputs result in the maximum value of 5V at the output of IC_{1B}. With V_{IN} at 2.5V, the output of IC_{1B} assumes the minimum value of 2.5V.

Figure 4



You can modify the circuit in Figure 2 to work with a single supply.

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Programmable oscillator uses digital potentiometers

Alan Li, Analog Devices, San Jose, CA

DIGITAL POTENTIOMETERS are versatile devices; you can use them in many filtering and waveform-generation applications. This Design Idea describes an oscillator in which setting the resistance of two digital potentiometers independently programs the oscillation amplitude and frequency. **Figure 1** shows a typical diode-stabilized Wien-bridge oscillator that generates accurate sine waves from 10 to 200 kHz. In this classic oscillator circuit, the Wien network comprising R, R′, C, and C′, provides positive feedback, and R_1 and R_2 provide negative feedback. R_2 is the parallel combination of R_{2A} and R_{2B} in series with R_{DIODE}. To establish sustainable oscillation, the phase shift of the loop should be 0° when the loop gain is unity. In this circuit, you can determine the loop gain, $A(j\omega)\beta(j\omega)$ by multiplying the amplifier gain by the transfer function V_P/V_O. With R=R′ and C=C′, the loop gain is

$$A(s)\beta(s)=\frac{1+R_2/R_1}{3+sRC+1/sRC}. \quad (1)$$

Substituting s=jω and rearranging the real and imaginary terms yields

$$A(j\omega)\beta(j\omega)=\frac{1+R_2/R_1}{3+j(\omega RC-1/\omega RC)}. \quad (2)$$

You define the phase angle of the loop gain as

$$0=\tan^{-1}\left[\frac{\mathrm{Im}|A(j\omega)\beta(j\omega)|}{\mathrm{Re}|A(j\omega)\beta(j\omega)|}\right]. \quad (3)$$

You force the imaginary term to zero to set the phase shift to 0°. As a result, the oscillation frequency becomes

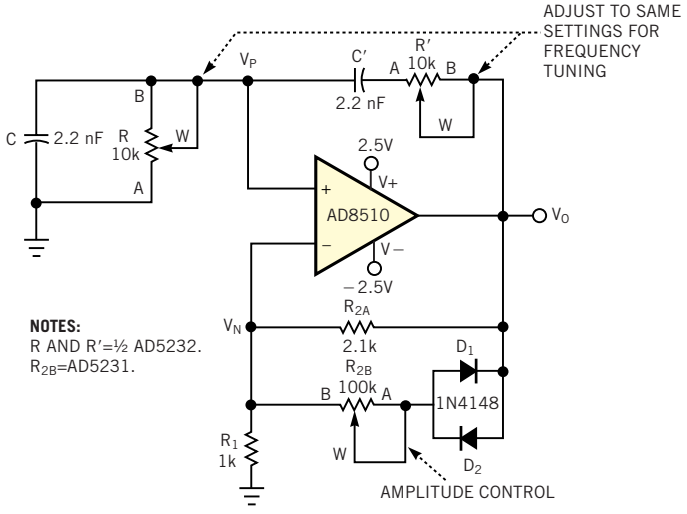
$$\omega_0=\frac{1}{RC} \text{ or } f_0=\frac{1}{2\pi RC}, \quad (4)$$

where R is the programmable resistance:

$$R=\frac{256-D}{256}R_{AB}. \quad (5)$$

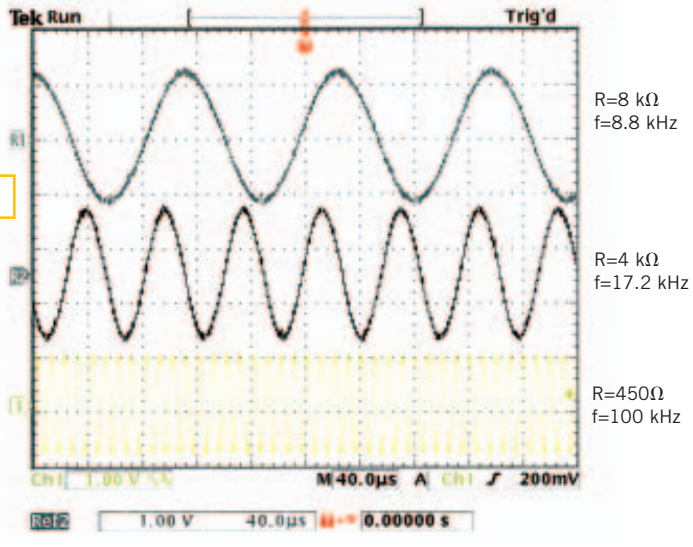
D is the decimal equivalent of the digital code programmed in the AD5232, and

Figure 1



This Wien-bridge oscillator uses digital potentiometers to provide independent settings of amplitude and frequency.

Figure 2



These three frequencies reflect three digital-potentiometer settings.

R_{AB} is its end-to-end resistance. To sustain oscillation, the bridge must be in balance. If the positive feedback is too great, the oscillation amplitude increases until the amplifier saturates. If the negative feedback is too great, the oscillation amplitude damps out. As **Equation 2** shows, the attenuation of the loop is 3 at resonance. Thus, setting $R_2/R_1=2$ balances the bridge. In practice, you should set R_2/R_1 slightly higher than 2 to ensure that the oscillation can start. The alternating turn-on of the diodes makes R_2/R_1 momentarily smaller than 2, thereby stabilizing the oscillation. In addition, R_{2B} can independently tune the amplitude, because $2/3(V_O)=I_DR_{2B}+V_D$.

You can short-circuit R_{2B}, which yields an oscillation amplitude of approximately ±0.6V. V_O, I_D, and V_D are inter-

dependent variables. With proper selection of R_{2B}, the circuit can reach equilibrium such that V_O converges. However, R_{2B} should not be large enough to saturate the output. In this circuit, R_{2B} is a separate 100-kΩ digital potentiometer. As the resistance varies from the minimum value to 35 kΩ, the oscillation amplitude varies from ±0.6 to ±2.3V. Using 2.2 nF for C and C′, and a 10-kΩ dual digital potentiometer with R and R′ set to 8, 4, and 0.7 kΩ, you can tune the oscillation frequency to 8.8, 17.6, and 100 kHz, respectively (**Figure 2**). The frequency error is ±3%. Higher frequencies are achievable with increased error; at 200 kHz, the error becomes ±6%. Two cautionary notes are in order: In frequency-dependent applications, you should be aware that the bandwidth of the digital potentiometer is a function of the programmed resistance. You must therefore take care not to violate the bandwidth limitations. In addition, the frequency tuning requires that you adjust R and R′ to the same setting. If you adjust the two channels one at a time, an unacceptable intermediate state may occur. If this problem is an issue, you can use separate devices in daisy-chain mode, enabling you to simultaneously program the parts to the same setting.

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Time-delay relay reduces inrush current

P Seshanna, Assumption University, Bangkok, Thailand

A transformer switching onto a line can sometimes cause a circuit breaker to trip or a fuse to blow. This phenomenon occurs even if the transformer presents no load, such as when the secondary is open. The problem arises because of the heavy magnetizing inrush current in the transformer. The amplitude of the current depends on the instant on the ac waveform at which the transformer becomes energized. The inrush current is at its maximum value if the transformer becomes energized when the ac waveform goes through its zero-crossing point. A similar situation exists when a capacitor in a power-factor-improvement bank switches onto the line. In this case, the inrush current is at its maximum when the ac waveform goes through its peak value. Normally, a mechanical contactor effects the switching without any control of the instant of switching. The inrush current dies down exponentially to the normal operating value of the load within a few cycles. If the breaker trips from the initial inrush current, you close the breaker to re-energize the circuit and hope for the best. You can limit inrush current by inserting a series resistor, R_1, during switching and then shorting this resistor after the transient period (**Figure 1**).

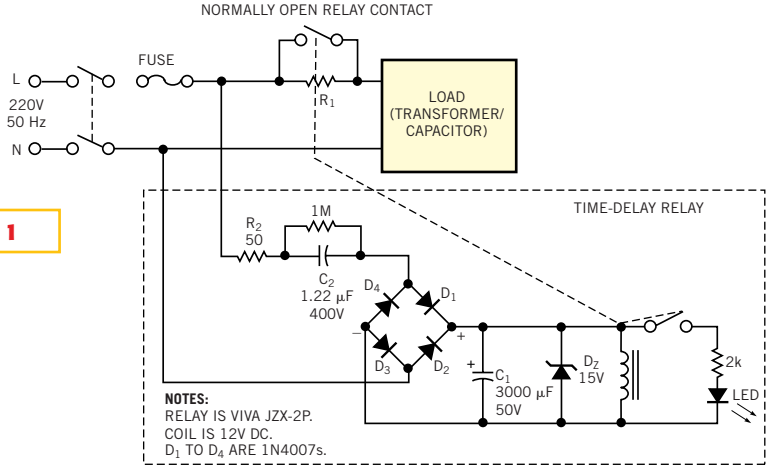

Figure 1

A time-delay-relay circuit can eliminate annoying circuit-breaker trips and blown fuses.

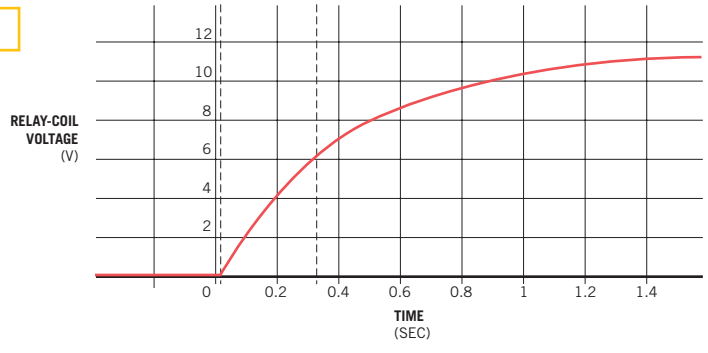

Figure 2

Only after 330 msec does the time-delay relay short-circuit the resistor in series with the load.

Lately, designers have been inserting negative-temperature-coefficient thermistors in series with some loads, such as switch-mode power supplies. This device presents a high resistance at the instant of switching, thus limiting the inrush current. After a few cycles, the resistance of the thermistor drops to a low value, allowing normal operation of the load. In contrast, the circuit in **Figure 1** physically inserts a resistor in series with the load to limit the inrush current and then short-circuits the resistor after a time delay. You can adapt the circuit to any size load by suitably selecting the series resistor and the relay-contact rating. A drawback of negative-temperature-coefficient thermistors is their limited joule heat-absorption capacity. The circuit in **Figure 1** works directly from the ac line to which the load drawing inrush current is connected.

The steady-state dc-current requirement of the relay coil determines the values of the other circuit components. You select capacitor C_2 such that the average value of the rectified current, I_{AVE}, is equal to the current the relay coil requires. The coil resistance should be smaller than the capacitive reactance of C_2 at line frequency. Under these conditions, the average rectified current is approximately $I_{AVE}=V(2\pi fC_2)/1.11$, where V is the rms value of the line voltage (220V), f is the line frequency (50 Hz), and C_2 is the required capacitor value. Once you know the relay current, you can select capacitor C_2 and the bridge diodes. The value of capacitor C_1 determines the delay time.

The voltage across C_1 rises exponentially with a time constant, $\tau=R_LC_1$ (**Figure 2**). If you know the relay's pickup voltage and its coil resistance, R_L, you can choose the required value for C_1. It is easy to see that when you close the main switch, the circuit simultaneously energizes the load drawing inrush current and the time-delay relay. A constant average-current source drives the capacitor/relay combination, and the dc voltage rises exponentially. When this voltage reaches the pickup voltage of the relay, the relay's normally open contact across the series resistor closes, thereby short-circuiting the resistor. When you open the main switch, the voltage across the relay coil drops, again exponentially. When this voltage reaches the dropout voltage of the relay, the contact opens. The resistor is again in series with the load and ready for the next switching operation. The pickup voltage of the 12V relay in the test is approximately 6V, and the contact-closure time is 330 msec, as the dashed line in **Figure 2** shows.

The important design considerations are as follows:

- The normal operating voltage of the relay must be less than 10% and must be lower than the ac-line voltage.
- C_2 determines the average operating current through the relay.
- The relay's contact rating must be adequate to meet the load-current requirement. The relay in **Figure 1** is small and has 12V-dc coil rating and 220V-ac, 5A contact rating. The measured coil resistance is approximately 160Ω.

The function of the 50Ω resistor, R_2, in **Figure 1** is to limit the switch-on surge current into the time-delay-relay circuit. The zener diode, D_Z, limits the voltage rise across C_1 to 15V in the event of a relay-coil open circuit. You can use the circuit in **Figure 1** in the laboratory for energizing a 220V, 1-kVA transformer for use in experiments.

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Optimize linear-sensor resolution

Steve Woodward, University of North Carolina, Chapel Hill, NC

A wide variety of sensors and transducers of physical phenomena work via the mechanism of variable resistance. These devices sense temperature, light, pressure, humidity, conductivity, and force, for example. Such sensors measure the physical parameter of interest by reading out the inherent parameter-sensitive resistance or conductance. All resistive sensors share the need for interface circuitry that provides a suitable source of excitation current and appropriate gain and offset of the resulting parameter-dependent voltage. The circuit in **Figure 1** and the design equations provide a universal solution for an application-specific, optimum-resolution, ratiometric interface of almost any resistive sensor. The technique works with any unipolar ADC with an externally accessible full-scale reference. When you configure it properly, the interface circuit selectively maps the range of interest of sensor output resistance (R_{MIN} to R_{MAX}) onto the full-scale span of the ADC. The circuit thus optimally uses available resolution that might otherwise be wasted on sensor resistances that lie outside the range of a given application.

The circuit works as follows: R_1 sources the sensor excitation/bias current, I_B. The op amp boosts and offsets the resulting sensor voltage, I_BR_T, as a function of the R_1-R_2-R_3 network. When $R_T=R_{MIN}$, $V_{OUT}=0V$, and, when $R_T=R_{MAX}$, $V_{OUT}=V_{REF}$. Thus, $R_T=(V_{OUT}/V_{REF})(R_{MAX}-R_{MIN})+R_{MIN}$. Positive feedback via R_4 cancels the effect of voltage variation across R_1 and thus maintains constant-current excitation of the sensor throughout the R_{MIN} to R_{MAX} range. You select R_1 through R_4 as follows: First, select a value for I_B. Sometimes, sensor limitations determine an appropriate value for I_B. Self-heating errors, for example, may limit the maximum excitation current you can apply to temperature sensors such as thermistors and RTDs. But if the given sensor is indifferent to the magnitude of I_B, then you'll obtain optimum tolerance of op-amp offset and gain errors with

$I_B=V_{REF}/(R_{MAX}+R_{MIN})$. With I_B known, you can compute the required gain: $G=V_{REF}/(R_{MAX}-R_{MIN})$. Then,

$R_1=(Z-R_{MAX})(1+1/G)$.

$R_2=Z-R_1$.

$R_3=(G-1)(R_1R_2/Z)$.

$R_4=GR_1$, where $Z=V_{REF}/I_B$.

For a practical example of how this circuit can be handy in a real application, consider a system in which you use a 100Ω platinum RTD to sense temperatures in the range of 25 to 50°C with 0.1° resolution. The corresponding resistance range is 109.73 to 119.4Ω. The 0.39Ω/°C temperature coefficient would require at least 12 bits of conversion resolution without scale expansion. But you can make an 8-bit ADC suffice using the circuit in **Figure 1** with the values shown. The calculations are as follows: $I_B=1$ mA limits self-heating power to an acceptable 120 µW. Assuming $V_{REF}=2.5$V, $Z=2.5\text{V}/1\text{ mA}=2500\Omega$. $G=2.5/9.67/1\text{ mA}=258.5$. It therefore follows that

$R_1=(2500-119.4)(1+1/258.5)=2390\Omega$.

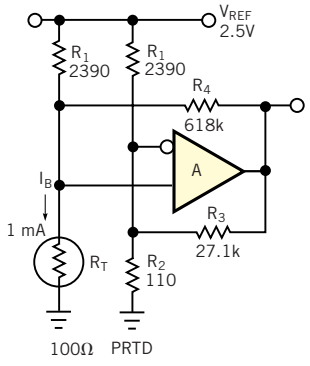
$R_2=2500-2390=110\Omega$.

$R_3=(257.5)(2390\times110/2500)=27{,}100\Omega$.

$R_4=258.5\times2390=618{,}000\Omega$.

$R_T=9.67(V_{OUT}/V_{REF})+109.73$.

Figure 1



NOTES:
$R_{MIN}=109.73\Omega$ (25°C).
$R_{MAX}=119.40\Omega$ (50°C).

$$V_{OUT}=V_{REF}\left(\frac{R_T-R_{MIN}}{R_{MAX}-R_{MIN}}\right).$$

$$R_{MIN}\le R_T\le R_{MAX}.$$

$$R_T=\frac{V_{OUT}(R_{MAX}-R_{MIN})}{V_{REF}}+R_{MIN}.$$

I_B=SENSOR REQUIREMENTS, OR

$$\frac{V_{REF}}{(R_{MIN}+R_{MAX})}.$$

$$\Delta V=I_B(R_{MAX}-R_{MIN});\ G=\frac{V_{REF}}{\Delta V};\ Z=\frac{V_{REF}}{I_B}.$$

$$R_1=(Z-R_{MAX})\left(1+\frac{1}{G}\right).$$

$$R_2=Z-R_1$$

$$R_3=(G-1)\left(\frac{R_1R_2}{Z}\right).$$

$$R_4=GR_1.$$

This circuit allows you to optimize resolution for sensors using resistive elements.

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design ideas

Edited by Bill Travis

Circuit adds programmability to sensor amplifier

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

THE PRESSURE-SENSOR AMPLIFIER circuit of **Figure 1** offers a number of advantages over the traditional approach using the classic three-op-amp instrumentation amplifier. The circuit can operate from a single supply and uses only two op amps and 1% resistors. If the reference voltage, V_{REF}, is 0V, the transducer gain for the circuit is

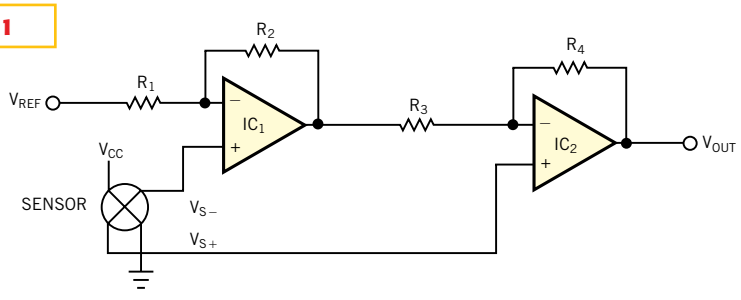
$$V_{OUT} = V_{S+}\left(\frac{R_3+R_4}{R_3}\right) - V_{S-}\left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_4}{R_3}\right).$$

To ensure equal gain for the two ground-referenced voltages making up the differential sensor voltage, you must impose the following condition:

$$\frac{R_1+R_2}{R_1} = \frac{R_3+R_4}{R_4}.$$

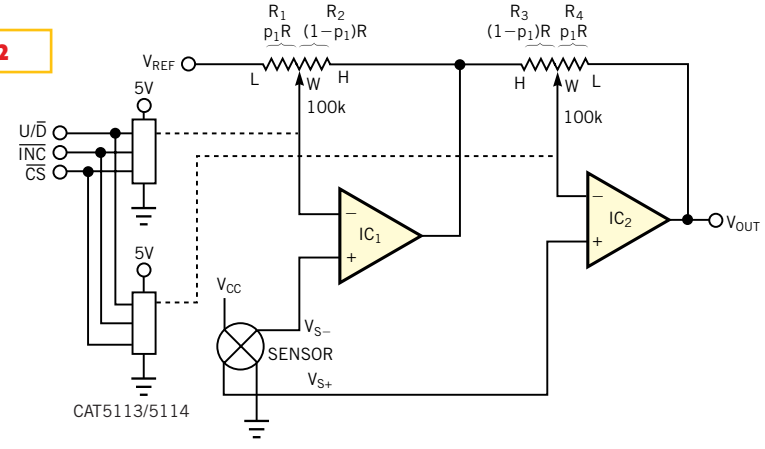
This restriction complicates the design and makes it difficult to add variability to the circuit. The circuit in **Figure 2** has the same advantageous topology as the original circuit, but it adds variability and programmability to the gain, simplifies the design expressions, and reduces the component count. Two ganged Catalyst digitally programmable potentiometers replace resistors R_1 through R_4. The potentiometers' wiper-to-low and wiper-to-high resistances establish the voltage gains of IC_1 and IC_2. Because the potentiometers are identical, the end-to-end resistances are the same, thus meeting the $(R_1+R_2)=(R_3+R_4)$ requirement. If you reverse the wiper-to-low and wiper-to-high resistances for IC_1 and IC_2, R_1 and R_4 are equal. If you mathematically model the wiper-to-low and wiper-to-high resistances as $(1-p_1)R_{POT}$ and $(p_1)R_{POT}$, the gain expression becomes

Figure 1



This circuit is a good sensor amplifier but suffers from a lack of variability.

Figure 2



An improved circuit features programmability and fewer components.

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$$V_{OUT} = \frac{V_{S+} - V_{S-}}{1 - p_1}, \text{ FOR } 0 \le p_1 \le 1.$$

The factor p_1 models the relative position of the wiper as it moves from one end ($p_1=0$) of the potentiometer to the other end ($p_1=1$). The number of values p_1 can assume is a function of the number of taps on the potentiometer. The sensor gain is inversely proportional to $(1-p_1)$, is pseudo-logarithmic, and varies from less than unity to 31 for a 32-tap potentiometer, such as the CAT5114, and to 99 for a 100-tap potentiometer, such as the CAT5113. The voltage, V_{REF}, represents a programmable offset voltage for the signal-conditioning circuit. You can easily implement the reference voltage by using a digitally programmable potentiometer configured as a programmable voltage divider.

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Add CAD functions to Microsoft Office

Alexander Bell, Infosoft International, Rego Park, NY

Microsoft Word has excellent drawing capabilities. You could use it effectively to perform some CAD tasks, such as schematic entry. Word is by far the most popular text processor on the market, and it would seem desirable for technical writers to be able to create a single integrated document file combining both text and graphics in an editable format. Of course, many third-party drawing or CAD packages are available, but most of them cost a significant sum. Also, the use of third-party software components could raise licensing issues. Moreover, in a shared development situation, you could face a document-interchangeability problem. Some of your coworkers may lose the ability to perform schematic editing if the third-party component is not installed on their computers. This Design Idea provides a great deal of flexibility, because anyone who has Word can create and modify drawings using standard Word features.

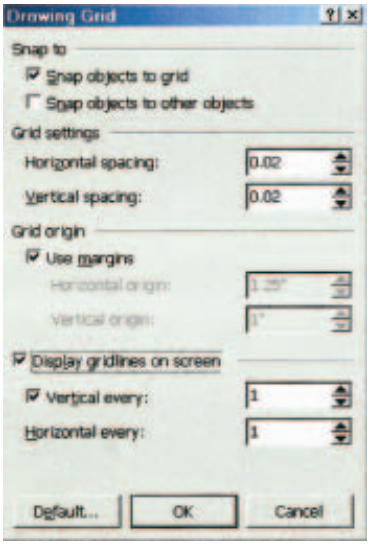

Figure 1 To display this dialogue box, click on the "Draw" button in the Drawing Toolbar, shown in Figure 2.

You can add some "convenience features" that can ease the schematic-entry process within Word. The first step is to create an Electronic Components Symbol Library and add it to the Clip Gallery. You can use those clips with Word or any other Microsoft Office application. These applications support drawing basically in the same way, with their built-in AutoShapes and Clip Art collection. In addition, you can use Clip Gallery with other graphics editors that support object linking and embedding. You can even use Clip Gallery as a stand-alone program. (For more information, refer to Microsoft Help for the Clip Gallery and related topics.) The task of creating the components library comprises several steps.

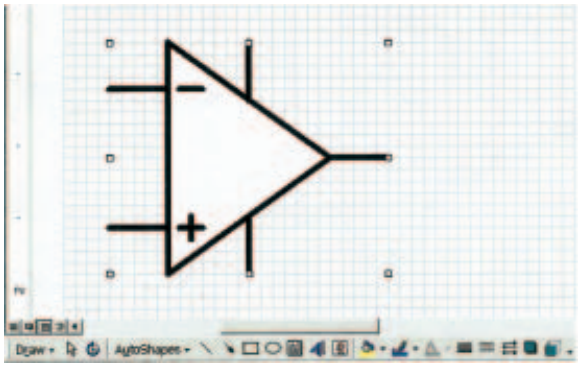

Figure 2 Create the component symbol by using Drawing Toolbar objects and then group them.

First, open a new file and then adjust the grid-line settings. You can reduce "Horizontal Spacing" and "Vertical Spacing" to 0.02 in. for good resolution. Make the gridlines visible by checking the box, "Display gridlines on screen" (**Figure 1**). To make the Drawing Grid dialogue box pop up, use the Drawing Toolbar button, labeled "Draw" in **Figure 2**. Set the scale to its maximum: 500%. Save the file as a Template by using the "Save As" option and choosing "Save as Type: Document Template" with extension .dot (for example, MyCad.dot) in the Word Templates default folder and then close the file. Now, when you open the new file for drawing, use this template as follows: Go to the "File" menu item, click the "New" subitem, and then choose the "MyCad" template. Note that the grid lines are not printable objects; they are visible only on the screen. You could type the text, draw the schematic, and then turn the grid lines off in the final document.

The next step is to create the symbol and add it to the Library. Use Drawing Toolbar objects via the corresponding buttons (**Figure 2**). After you have finished the drawing, select

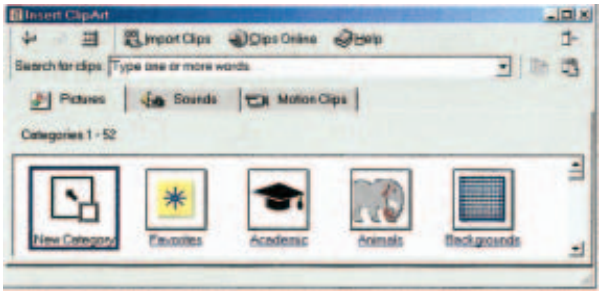

Figure 3 You can use the Clip Gallery with many Microsoft Office applications and even in stand-alone mode.

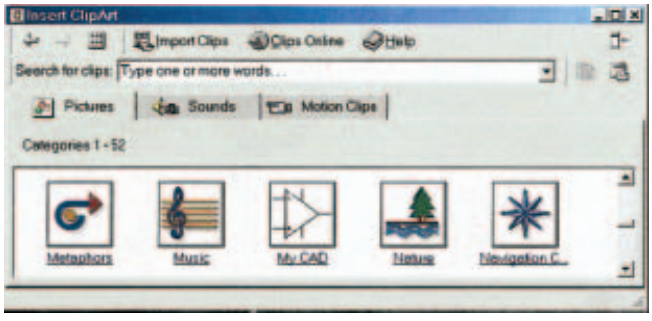

Figure 4 Add the new category, "MyCad," which serves as your Components Library.

all of its constituent parts by pressing the Shift key and holding it down while making the selection and then right-click the mouse on the pop-up menu, select the "Grouping" item, and click "Group." Now, Word treats the created component symbol as Clip or Auto Shape Object, which you can move, resize, and format as a whole image. To edit a part of the symbol image, you should first ungroup it, make the necessary changes, and then group it again. To add symbols to the Library, you should first create a new category in the Clip Gallery, which serves as a "container" for your graphic images and then copy and paste the symbols into the Gallery. The procedure is as follows:

1. Open the Clip Gallery by clicking on the icon "Insert Clip Art" located at the Drawing toolbar.
2. Click on the "New Category" icon (**Figure 3**) and type the name (for example, MyCad) for your Library when prompted, then click "OK."
3. Check to see whether the new "MyCad" category icon appears in the Clip Gallery window (**Figure 4**) and then click on the icon to open it.
4. Select the component you want to add to the Library and copy it to the clipboard (the shortcut for the "Copy" command is Ctrl-C).
5. Paste the component to the "MyCad" Category (the shortcut for the "Paste" command is Ctrl-V). Type the name for the symbol when prompted and then click "OK."
6. Repeat steps 2 to 5 for any components you want to add.

Figure 5 shows a variety of symbols in the MyCad Category. The usage of the Components Library is straightforward and similar to the usage of built-in Clips. To insert the symbol image into you document, you could use the Clip Gallery's standard "Import Clips" feature or the "Drag-and-Drop" option, depending on your personal preference. The Clip Gallery has a Help utility you can use to obtain more information. You could further improve ease of use by adding macros to automate the most common tasks, such as resizing, rotating, or flipping objects or adding labels, for example. You can assign the macros to shortcuts (certain key combinations). However, only qualified users, who have extensive experience dealing with VBA/macros, should attempt these operations. Also, you must be aware of the security issues associated with the use of macros in the applications:

- Some macros can perform potentially dangerous and harmful actions, and some of them may contain viruses. Use the macros at your sole risk without warranty of any kind.
- When using the Clip Gallery in a shared-development environment, and also with regard to network-installation or distribution issues, refer to the licensing/legal information, "Legal restrictions for using clips provided in the Clip Gallery" in the in the Help menu and the Microsoft Office End-User Legal Agreement, because certain restrictions could apply.

You can download several sample macros from the Web version of this article at www.ednmag.com. You can use them to Add Label to the selected graphic component, to resize the component or to rotate it 45° clockwise. You can store macros in the Macro Module that you add to the default Normal.dot template, thus affecting all opened documents. Alternatively, you can store the macros in the Template Macro Module within the MyCad.dot file. In this case, the macros are available only for opened documents based on the MyCad template file. For more information on creating and storing template files, refer to the Microsoft online Help features.

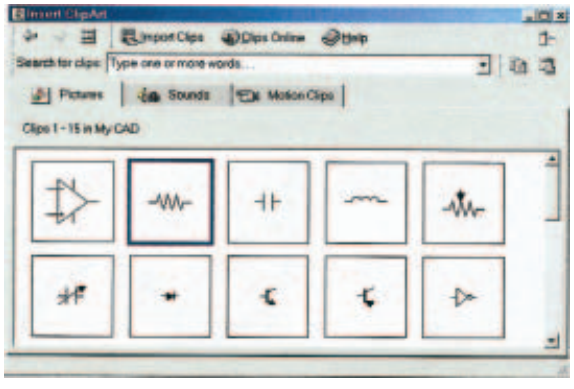

Figure 5 After adding the components to the Clip Gallery, you can use them in the same way you'd use built-in Clips.

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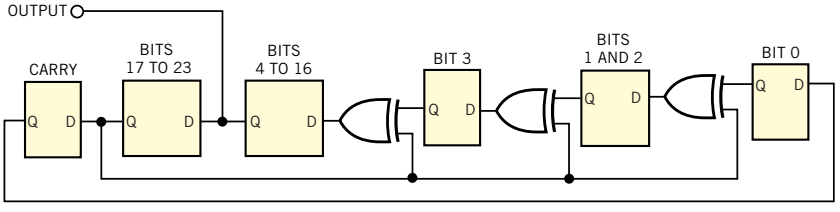
Single IC forms pseudorandom-noise source

Steve Ploss, Veridian, Dayton, OH

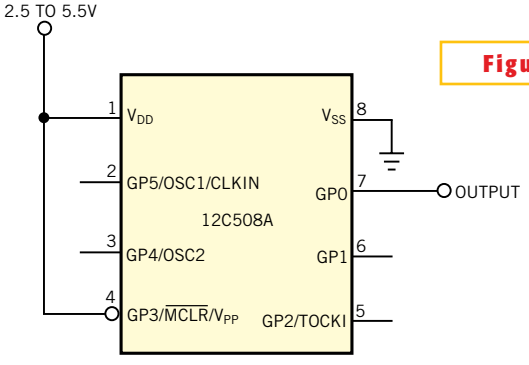
Trying to find a single IC noise source can be frustrating. National Semiconductor once made such a noise source for audio applications, but it's now hard to find. This situation leaves the designer with several choices, most of which involve using several ICs. You can take the analog approach of using a lot of gain to amplify diode-avalanche noise, or you can design a linear-feedback-shift-register pseudorandom-noise source using multiple CMOS ICs. Alternatively, you could use a single-chip microcontroller, such as Microchip's 12C508. The classic approach to generating a pseudorandom-noise sequence is to model the linear-feedback-shift register in software. The method involves testing and XORing together multiple bits to provide the single-bit feedback into the shift register. One problem with this approach is that it doesn't yield the highest possible bit rate. The approach in **Figure 1** is more optimum for using the lowest number of machine cycles per loop.

Figure 1



The shift register's length in this pseudorandom-noise generator is effectively 25 bits.

Figure 2



The connections for the 12C508 microcontroller are exceedingly simple.

The approach is similar to the one that CRC bit-shift algorithms take. These algorithms test only a single bit but XOR multiple bits in parallel. A microcontroller quickly accomplishes the task. The bit-test and XOR operations require only three instruction cycles to complete. **Listing 1** shows the assembly code for the complete noise source. The entire loop takes only 10 instruction cycles. You can download **Listing 1** from the Web version of this Design Idea at www.ednmag.com. The circuit in **Figure 2** produces an output rate of 100 kHz for the 12C508 with its internal 4-MHz oscillator. The shift register's length is effectively 25 bits, three bytes plus a carry bit. For a maximal-length sequence such as this, the pattern does not repeat itself for 5 minutes and 35 sec. If you desire higher bit rates, you can simply use a 20-MHz part with a crystal to obtain an output rate of 500 kHz. Another trick for increasing the rate is to use a part with an 8-bit output port and use that port in place of the Hibyte register. Then, the commands "movf Hibyte,W" and "movwf GPIO" are unnecessary. The result is a loop time of eight instruction cycles and a 25% increase in output rate. Be sure to configure the port pins as all outputs.

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LISTING 1—12C508 ASSEMBLY CODE FOR PSEUDORANDOM-NOISE GENERATOR

```
;
;*****************************************************************
;    Pseudorandom noise generator
;*****************************************************************
;     12/13/01 Stephen J. Ploss
;
;

        LIST    p=12C508A

#include "P12C508A.INC"

        __CONFIG _CP_OFF & _WDT_OFF & _IntRC_OSC & _MCLRE_OFF

        cblock  0x07            ;Start of GP Regs

        Lobyte                  ;Shift Registers
        Midbyte                 ;       "
        Hibyte                  ;       "

        endc

start   movlw   0xC0            ;No Wake on pin change,
                                ;No pull ups, ignore timer
        option
        movlw   0xFE            ;Only GP0 as output
        tris    GPIO

        ;Start the PN Generator
main    movlw   0xFF            ;Initialize shift reg's
        movwf   Lobyte
        movwf   Midbyte
        movwf   Hibyte

loop    rlf     Lobyte,F        ;Perform shift
        rlf     Midbyte,F
        rlf     Hibyte,F
        movlw   0x1A            ;Polynomial
        btfsc   STATUS,C        ;Test Carry
        xorwf   Lobyte,F        ;XOR if set

        movf    Hibyte,W        ;Get Hibyte
        movwf   GPIO            ;Send LSB to output
        goto    loop

        END
```

LED dimmer uses only two lines

Jerry Wasinger, WallyWare Inc, Norcross, GA

THE CIRCUIT IN **Figure 1** provides 32 steps of brightness control—from 0 to 100%—for a backlight or instrument panel, using just two general-purpose-microprocessor signals. In addition, the circuit requires little board space, because it uses only three SOT-23s and one µMax package. Although **Figure 1** shows the circuit driving white LEDs, the load could also be a dc motor or an incandescent lamp. The basis of the circuit is a modified Schmitt-trigger relaxation oscillator (**Figure 2**). The output of IC_1 is high when

$$\tau_H = CkR_P \ln\left[\frac{V_{CC}-V_D-V_N}{V_{CC}-V_D-V_P}\right],$$

where k is the wiper position, V_{CC} is the supply voltage, V_D is the diode voltage, and V_N and V_P are the threshold voltages of the Schmitt trigger. The output of IC_1 is low when

$$\tau_L = C(1-k)R_P \ln\left[\frac{V_D-V_P}{V_D-V_N}\right].$$

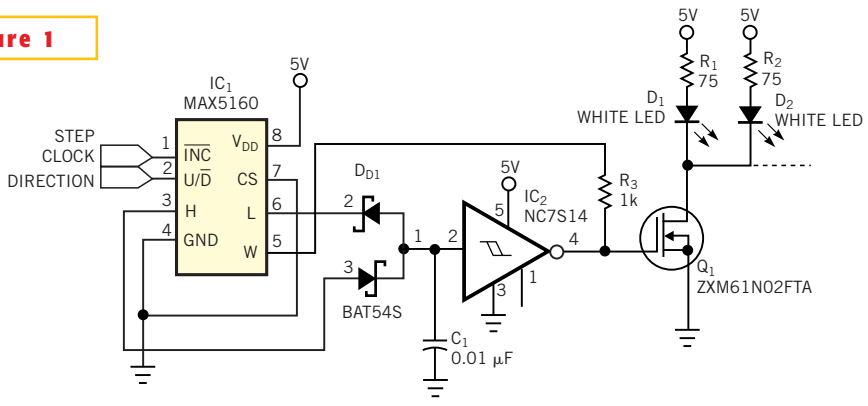
The period and duty cycle are $T=\tau_L+\tau_H$, and $DC=100\tau_H/T$, where DC is duty cycle. Initial inspection of the foregoing equations may make the substitutions to solve for the duty cycle appear to be a tedious, algebraic exercise. But, when you substitute V_{CC}, V_D, V_N, and V_P into the two logarithmic terms, their results are close in value. So, you can simplify the expanded solution to the duty-cycle equation to

$$DC = 100\left[\frac{kR_P}{(1-k)R_P + kR_P}\right] =$$

$$100\frac{kR_P}{R_P} = 100k.$$

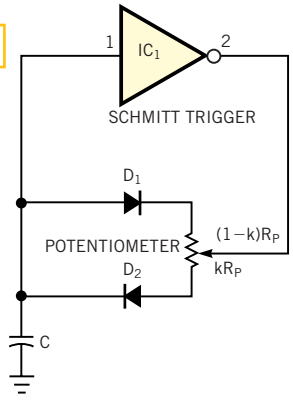
Based on the above considerations, you can see that the duty cycle of the circuit is not only linear, but also independent of the selected components. The component selection affects only the center frequency of oscillation. An approximate equation for the operating frequency is $f=1.75/(CR_P)$. This circuit uses a MAX5160 digital potentiometer that has a full-scale resistance of 200 kΩ in combination with a 10-nF capacitor. This combination results in an operating frequency of approximately 875 Hz. Note that slight mismatches of the two logarithmic terms cause the frequency to vary slightly as you adjust the duty cycle. **Figure 3** shows a plot of duty cycle versus the potentiometer's tap position; **Figure 4** shows the variation in the oscillation frequency with tap position.

Figure 1



By controlling the duty cycle of a Schmitt trigger, you obtain 32 steps of brightness in an LED display.

Figure 2



The MAX5160 digital potentiometer controls the duty cycle of the Schmitt trigger.

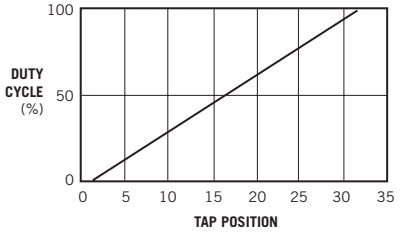


Figure 3 **The duty cycle of the Schmitt trigger is a linear function of the potentiometer's tap position.**

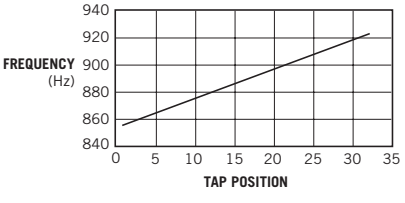


Figure 4 **Frequency also varies with the tap position, but with no effect on performance.**

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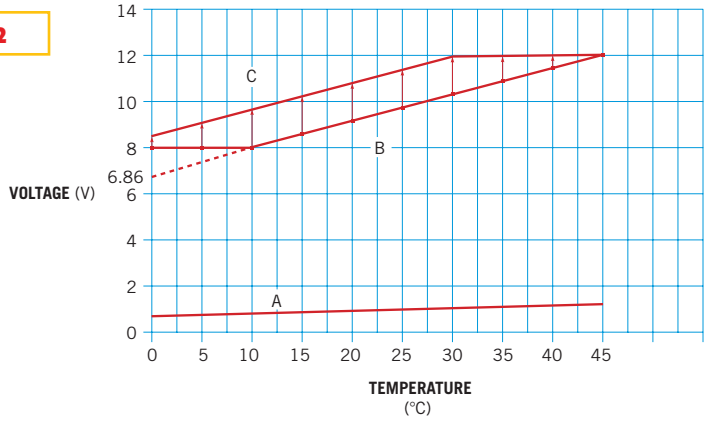
Circuit generates fan-speed control

Jim Christensen, Maxim Integrated Products, Sunnyvale, CA

Fan noise is becoming a significant issue as electronic equipment increasingly enters the office and the home. Noise is proportional to fan speed, and the airflow—hence, fan speed—necessary for cooling is less at low ambient temperatures. Because ambient temperature is lower than the upper design point most of the time, a fan can run slower, making it easier on the ears. Fan-control circuits range from simple switches that boost the speed from low to high, to digital, proportional speed-control designs. High/low-speed switches are inexpensive, but the sound of sudden speed changes can be annoying. Digitally controlled fans perform well, but the circuitry is costly, and the system must include a serial bus. As an alternative, consider a low-cost, self-contained analog circuit for fan-speed control (**Figure 1**). You can easily adjust the circuit for any desired linear relationship between the fan voltage and temperature (**Figure 2**, curves B and C). We plotted measured data points against the desired voltage in **Figure 2**.

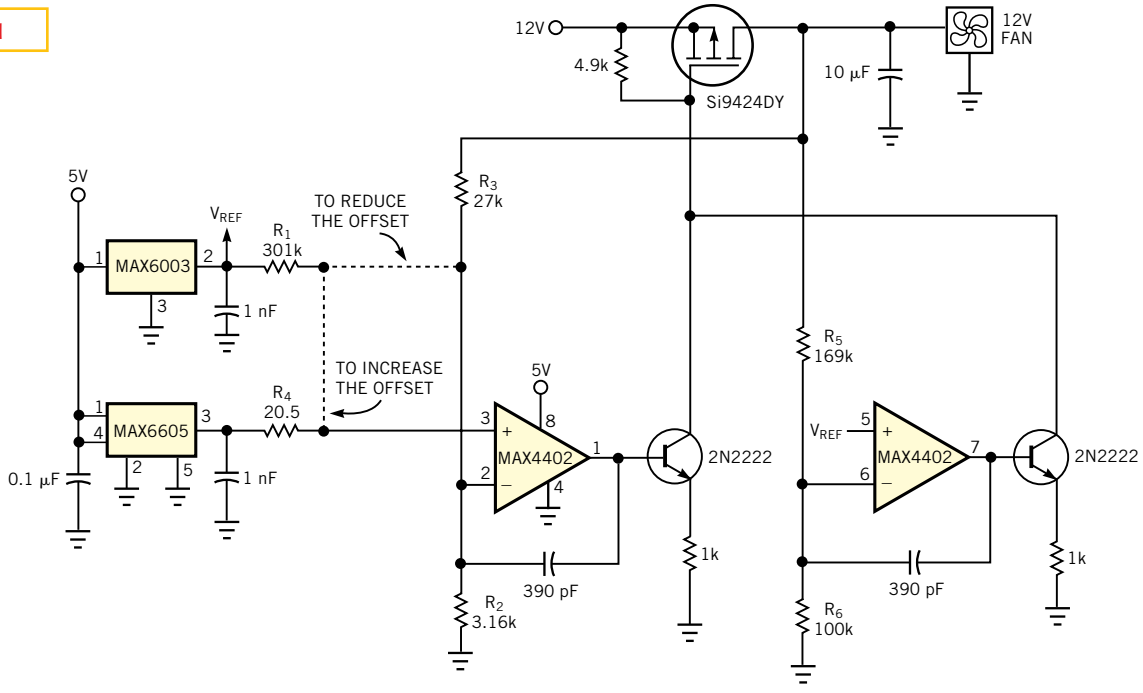
Figure 2



These curves illustrate voltage output versus temperature for the circuit in Figure 1.

Curve A in **Figure 2** represents the output of a MAX6605 analog temperature sensor versus temperature in degrees Celsius: V_{SENSOR}=0.0119 V/°C+0.744V. Curve B relates the fan voltage to tem-

Figure 1



This circuit delivers a continuous and linear fan-control voltage that is proportional to temperature.

perature and combines a minimum "floor" voltage of 8V with a sloping line: $V_{FAN}=0.114V/°C\times T+6.86V$, where T is the system temperature. The floor voltage ensures fan rotation at low temperatures. Above 10°C, the voltage increases with a slope of 0.114V/°C until it reaches full value at 45°C. Simply amplifying the MAX6605's output does not provide the 8V floor voltage. Moreover, the gain (9.58=0.114/0.0119) needed to obtain the fan-voltage slope is not the same gain (9.22=6.86/0.744) needed to obtain the y-intercept point.

To transform Curve A into Curve B, you must subtract a voltage offset from the temperature sensor's output and then multiply the result by a constant. The circuit in **Figure 1** performs this operation. You connect the dotted line labeled "To reduce the offset." One op amp creates the sloped line, and the second op amp creates the floor voltage. The op amps' outputs connect to transistors in such a way that the op amp demanding a higher output voltage dominates. The following equations allow you to determine resistor values:

For the condition in which $R_2<<R_1$, R_1=any reasonable value; $R_2=R_1(A_V V_{TEMP0}-V_{Y\text{-}INTB})/[(A_V-1)(V_{REF}-V_{TEMP0}+V_{Y\text{-}INTB}/A_V)]$; and $R_3=R_2(A_V-1)$, where $A_V=0.114/0.0119=9.58$=the ratio of the desired slope in volts per degrees Celsius to that of the sensor; $V_{TEMP0}=0.744V$=the temperature-sensor voltage at 0°C; $V_{Y\text{-}INTB}=6.86V$=the y-intercept indicated by the desired (extrapolated) temperature curve; and $V_{REF}=3V$=the reference voltage.

Thus, choosing $R_1=301\ k\Omega$ lets you calculate $R_2=3.158\ k\Omega$ and $R_3=27.09\ k\Omega$. The closest 1% values are 3.16 and 27 kΩ, respectively. The following equation lets you calculate the floor voltage: $R_5=R_6(V_{FLOOR}-V_{REF})/(V_{REF})$, where R_6 equals any reasonable value. $V_{FLOOR}=8V$, the desired minimum output voltage. Thus, choosing $R_6=100\ k\Omega$ lets you calculate $R_5=169\ k\Omega$. In some cases, the required offset gain is greater than the required slope gain, so you must increase the temperature sensor's natural offset. For a desired temperature, Curve C, expressed as $V_{FAN}=(0.114\ V/°C)(T)+8.5V$, the gain (slope) of $A_V=9.58$ is the same as for Curve B, but the required offset gain is (8.5/0.744)=11.42 is greater. You therefore use the "To increase the offset" version of the circuit in **Figure 1**. The following equation applies in such cases: $R_4=R_1(V_{Y\text{-}INTC}/A_V-V_{TEMP0})/(V_{REF}-V_{INTC}/A_V)=20.41\ k\Omega$, where $V_{Y\text{-}INTC}=8.5V$ is the intersection of the desired temperature curve with the y-axis. For $R_1=301\ k\Omega$, the closest 1% value for R_4 is 20.5 kΩ.

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design ideas

Edited by Bill Travis

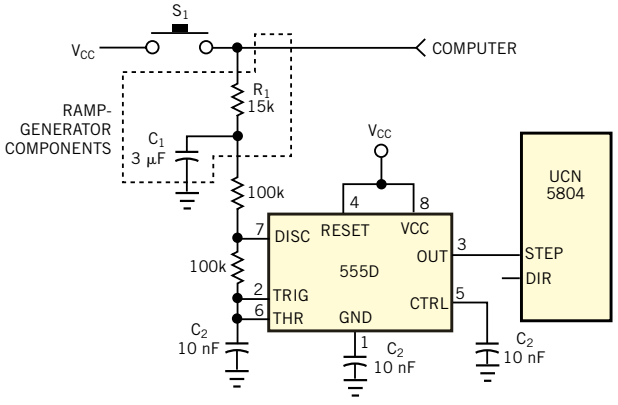
Make a simple ramp generator for stepper motors

Richard Brien, GSI Lumonics, Wilmington, MA

Stepper motors are synchronous motors that step at the pulse rate of the driving signal. For the motor to move quickly, the stepping rate must be fast. However, because of motor and load inertia, the motor often cannot go from 0 rpm to the desired number of revolutions per minute in one step. Therefore, most stepper motors receive their drive from a pulse chain that starts out slowly and then increases in rate until the motor reaches the desired rate. To stop the motor, the drive signal must not abruptly stop; it must gradually decrease or ramp down to zero. Microprocessors can easily generate the needed ramp-up and then ramp-down signals, often called a trapezoidal profile, but in any circuit without a microprocessor, this ramp is difficult to generate.

The 555-based bistable circuit in **Figure 1** can easily generate a pseudo-trapezoidal move profile. Note that the timing string of R_1 and associated components does not connect to V_{CC}, as it would in a normal circuit, but instead receives its power through a pushbutton switch.

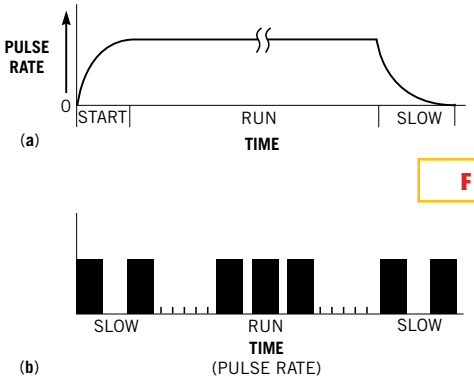
Figure 1



This circuit generates a pseudo-trapezoidal motion-control profile for controlling stepper motors.

When you push the button, capacitor C_1 starts charging up to a point at which C_2 can start charging. As C_1 charges, the output frequency of the 555 starts off slowly and gradually increases to a frequency or pulse rate that's a function of all the components in the timing string. This final frequency is lower than the frequency the circuit would adopt, if C_1 and R_1 were not in the string. When you release the pushbutton, the 555 does not immediately stop running but ramps down in frequency until it finally stops (**Figures 2a** and **2b**). The ramp frequencies generated do not follow a linear profile, but neither do those in most microprocessor-driven circuits. The ramp-frequency profile of the circuit should resemble that of **Figure 2a**, depending on the component values.

Figure 2



The move profile from the circuit in Figure 1 is roughly trapezoidal (a); the step-rate profile exhibits low frequencies at ramp-up and -down (b).

You can operate this circuit with a simple pushbutton. This concept opens a world of manual control to stepper motors. Usually, stepper motors do not use manual control, because of the difficulty of generating a trapezoidal frequency profile in hardware. With this circuit, you can use low-torque, low-revolu-

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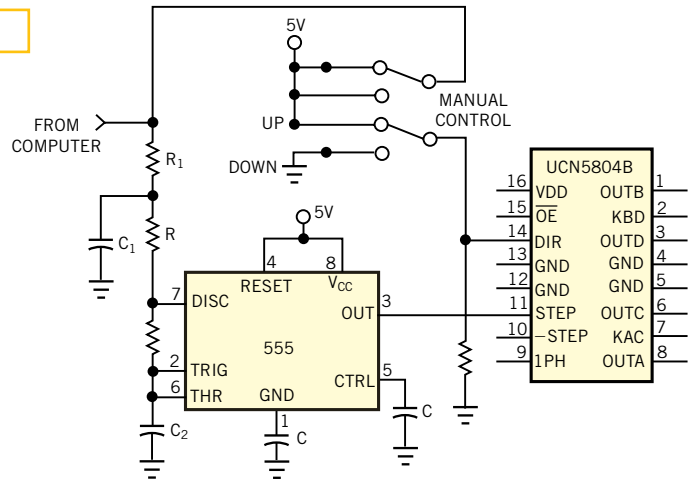
tions-per-minute stepper motors in systems in which you formerly needed dc gearbox motors. By changing the pushbutton to a dpdt switch, you can make a stepper motor run clockwise and then counterclockwise without microprocessor control (**Figure 3**). These concepts also apply to stepper-motor-based linear actuators. You could also replace the pushbutton with a control signal from a computer or a controller, thus allowing stepper motors to take their drive from controllers that do not have a built-in ramp-generating function.

Figure 3



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By changing the pushbutton in Figure 1 to a dpdt switch, you can make a stepper motor run clockwise and then counterclockwise without microprocessor control.

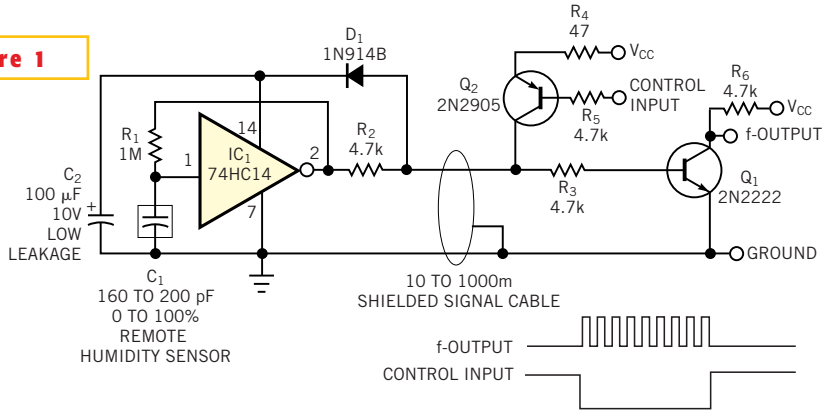
Remote humidity sensor needs no battery

Shyam Tiwari, Sensors Technology Private Ltd, Gwalior, India

Using AC-line power sources and batteries for remote humidity sensors is undesirable because these sources can be troublesome if you mount them in inaccessible points, such as smokestacks, cold-storage chambers, or darkrooms, where maintenance is difficult and inconvenient. **Figure 1** shows a simple way to remove the power source from the humidity-sensor circuit. The circuit uses a 160- to 200-pF, capacitor-type HS1101 humidity sensor from Humirel for the circuit. IC_1 forms a classic oscillator of time constant R_1C_1. The center frequency is 5 to 10 kHz, depending on the value of R_1. The circuit charges the 100-µF, low-leakage capacitor, C_2, through the diode, D_1, directly from the output line of the sensor oscillator, IC_1. C_2 becomes the power source for IC_1.

When you make measurements, you stop charging C_2 for a short time by removing the Control Input signal (0V for charging and V_{CC} or floating for measurement). You then measure the frequency of the signal at the output of transistor Q_1. Transistor Q_2 supplies enough current to charge C_2 through R_4. The HS1101 sensor measures approximately 160 pF at 0% relative humidity and 200 pF at 100% relative humidity. Therefore, frequency decreases with increasing relative humidity. Although the sensor has a linear response within ±5% of full-scale range over 1 to 25°C, you should calibrate the circuit at several humidity points. You can find more details about the HS1101 sensor at www.humirel.com or www.sensorstechnology.tripod.com/humidity.html.

Figure 1



Eschew troublesome power sources for remote humidity sensors by using this simple scheme.

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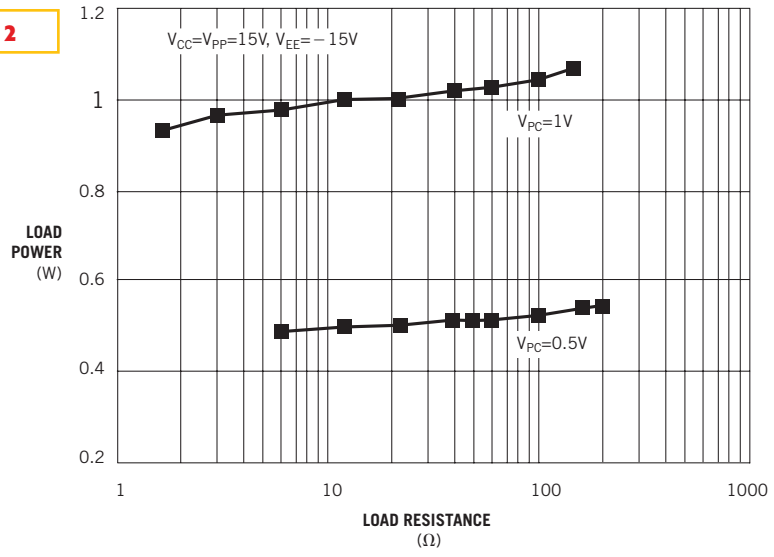
Power source is insensitive to load changes

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

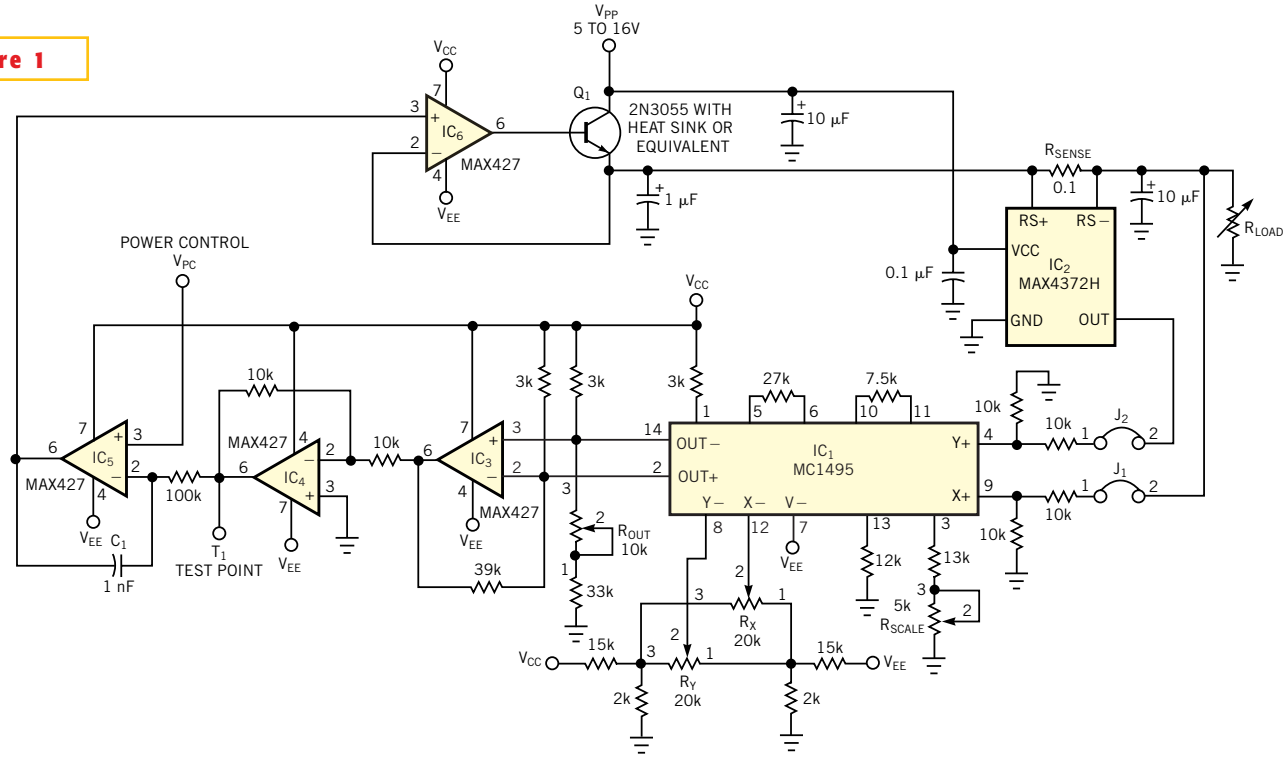
For the heating and cooling elements common in industrial systems, resistance is not a fixed quantity. These elements include such devices as positive-temperature-coefficient heaters and thermoelectric coolers. Their resistance can change more than 100% during operation, and the result is a change in power dissipation for elements receiving drive from a fixed voltage or current source. Worse, excessive power can damage the heating or the cooling element. Driving the element with a fixed and regulated power driver overcomes these problems (**Figure 1**). The circuit is analogous to a voltage or a current source but delivers fixed power levels that are independent of the load resistance. A feedback loop senses load power and automatically adjusts the output voltage to maintain the desired pow-

Figure 2



Power delivery to the load is nearly independent of load resistance.

Figure 1



This regulated power source delivers fixed power to a varying load.

er level. The circuit measures the output current with a current sensor, IC_2 and then determines the output power by multiplying the current by the voltage with the use of a four-quadrant analog-voltage multiplier, IC_1 and IC_3.

Because the multiplier's output is inverted, you add a unity-gain-inverting stage, IC_4, to reinvert the output-power signal. Op amp IC_5 then compares output power to the reference power, V_{PC} input, and integrates any difference between them. The integrator provides an automatic power adjustment by increasing or reducing the output voltage until output power equals reference power. IC_6 and Q_1 form a voltage follower that drives the load. The following formula sets output power: $V_{PC}=10PR_{SENSE}$, where P is the desired output power in watts, R_{SENSE} is the sensing resistor in ohms, and V_{PC} is the reference-power input in volts. If, for example, the desired load power is 1W, and $R_{SENSE}=0.1\Omega$, then set V_{PC} to 1V.

Curves for load power versus load resistance for 0.5 and 1W loads show that power delivered to the load changes less than ±7% for a change of 10,000% (two decades) in load resistance (**Figure 2**). If you define load regulation as the change in output power divided by the output power, then for a load change of 6 to 40Ω at 1W, the load regulation is ±2%. For the circuit to work properly, you must calibrate the analog multiplier as Motorola's MC1495 data sheet delineates. You repeat that calibration procedure below for convenience. Remove jumpers J_1 and J_2 for the calibration.

1. X-input offset adjustment: Connect a 1-kHz, 5V p-p sine wave to the Y input. Connect the X input to ground. Using an oscilloscope to monitor test point T_1, adjust R_X for an ac null (zero amplitude) in the sine wave.
2. Y-input offset adjustment: Connect a 1-kHz, 5V p-p sine wave to the X input. Connect the Y input to ground. Using an oscilloscope to monitor test point T_1, adjust R_Y for an ac null (zero amplitude) in the sine wave.
3. Output-offset adjustment: Connect the X and Y inputs to ground. Adjust R_{OUT} until the dc voltage at T_1 is 0V dc.
4. Scale-factor (gain) adjustment: Connect the X and Y inputs to 10V dc. Adjust R_{SCALE} until the dc voltage at T_1 is 10V dc. Repeat steps 1 through 4 as necessary.

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Encrypted routines impede hackers, protect licenses

Lawrence Arendt, Oak Bluff, MB, Canada

The use of public-key-encrypted algorithms within licensed applications can prevent hackers from cracking the licensed algorithms. Moreover, you can use them to disable licensed features that a user doesn't purchase. Licensing schemes eventually arrive at some critical decision point at which an algorithm decides whether the user is entitled to run that application. If not, the algorithm usually generates a console message or a message box to notify the user of his or her ineligibility. Then, the application terminates or continues in a feature-limited mode. The decision code generally resolves to one of the following (or similar) commands in assembly code:

Jump/Branch if not equal (for example, JNE, BNE)

Jump/Branch if equal (for example, JE, BEQ).

Typically, a hacker searches a disassembled listing for the termination message, finds the routine that displays the message, and then traces backward through the calling sequence until he locates the decision code. Often, changing a single hex byte in a binary image of the executable code completely bypasses the decision logic. Or changing the byte can reverse the decision logic. (The new copy runs only if it *does not* have a license.) The edited file can then generate a new .exe file. For example, you could replace the hex code for a JNE with a JMP (jump always) or a JE. To thwart hackers,

1. Select the code, C_{PT}, consisting of a single routine or a block of contiguous routines, that implements the licensing scheme.
2. Compile the application, linking in temporary code C_{EN} that generates a CRC of the associated object bytes and then compress and encrypt the associated object bytes. Then, dump the output C_{CT} to a file formatted for direct pasting into a C/C++ file. This file serves to initialize a *const char* array called *EncryptedRoutines*.
3. Now, insert runtime code, C_{DE}, that copies the contents of *EncryptedRoutines* to a buffer and then decrypts and decompresses the contents. Also, remove the original unencrypted code, C_{PT}, and the temporary code, C_{EN}.
4. Finally, recompile the application to link in C_{DE} and C_{CT} and to exclude C_{EN} and C_{PT}.

When the application starts up, it executes code C_{DE}, which copies the encrypted bytes from the *EncryptedRoutines* array into a dynamically created buffer. It then decrypts the buffer's contents using a public key, K_2, which the vendor provides, followed by decompression. The

routine computes a CRC of the decrypted block. If this CRC matches the original CRC, the application then constructs a pointer to a decrypted entry-point function and uses the pointer to execute that function. CRCs that differ from each other indicate the use of the wrong public key, and the application terminates, because executing the still-encrypted code could be catastrophic. As a result, any system calls made from within the encrypted code do not show up in any disassembled listing. A hacker can detect them only if he or she is willing to acquire and use an emulator and trace through the execution.

Compression of the code to be encrypted—before encryption—prevents the hacker from simply replacing the encrypted bytes with the decrypted bytes. Now, even if the hacker recovers the decrypted bytes, he cannot subvert or change the licensing logic and then encrypt and replace the existing encrypted bytes, because he does know the private key, K_1. You should also encrypt all messages that the encrypted routines use. Most compilers for Windows/DOS generate position-independent code that results in relative calls: Jumps and Branches. When the system compiles and links the original application, the compiler assumes that all code executes from code space. Subroutine calls compile into PC-relative call instructions with the correct displacements. However, the decrypted routines run out of dynamically allocated data memory, so the displacements are all wrong.

The solution is to force all subroutine calls from the decrypted routines to be made to absolute addresses. However, the absolute addresses of all linked functions depend on the compiler and the options used, the order of the linked libraries, and *the size of the user code*, which will change because of Steps 2 to 4. Three solutions to these problems are:

1. If necessary, pad the code with dummy instructions, such that the size of $C_{PT}+C_{EN}$ equals the size of $C_{DE}+C_{CT}$.
2. Link all subroutines called from within the decrypted code to fixed, user-specified addresses that will not change because of Steps 2 to 4.
3. Use an encrypted table of absolute-runtime-function addresses.

You can use the same concepts to protect code that implements a licensed feature. If you enter the correct public key, the decrypted code is usable. If you enter the wrong public key, the "decrypted" code remains encrypted, rendering that function unusable. You should use a unique private/public key pair for each licensed feature. **Listing 1** shows Borland 5.02 code fragments that illustrate the concept of running decrypted code from dynamically allocated memory. You can download **Listing 1** from the Web version of this article at www.ednmag.com. The programmer can decide the implementation details of the CRC generation, compression, and private/public key algorithms.

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LISTING 1—ROUTINE FOR GENERATING ENCRYPTED CODE

```
#ifdef GENERATE_ENCRYPTED_CODE
// This is the licensing function we want to protect
void CheckForLicense (void *pRuntimePrintf, void *pRuntimeExit)
{
    // unscramble absolute addresses and create pointers to functions we will call
    void (*pExit)(int)                  = (void (*)(int))((char *)          pRuntimeExit   - 0xD91E639A);
    int (*pPrintf)(const char *,...) = (int  (*)(const char *,...))((char *)pRuntimePrintf - 0x76532984);

    pPrintf ("Verifying license...\n");          // use a function call

    bool HaveLicense = false;
    // insert code here to determine if we have a license
    if (HaveLicense == false) pExit(0);
}
void End () { ; }       // just used to get size of the original code to be encrypted

// This code just scrambles for illustration. Use a true private/public key algorithm in your application.
void Encrypt (UCHAR *Buf, int szBuf)
{
    for (int i=0; i<szBuf; i++)
        Buf[i] = (UCHAR)((Buf[i] + i) ^ (~i));
}
void SaveBuf (UCHAR *Buf, int szBuf)
{
    FILE *fp = fopen ("code.cpp", "w");
    for (int i=0; i<szBuf; i++)
        fprintf (fp, "0x%02X, ", Buf[i]);
    fclose (fp);
}
void Generate (void)
{
    UCHAR Buffer[100];
    int szCode, nCBytes;
    szCode = (char *)End-(char *)CheckForLicense;  // get the size of the function
    memcpy  (Buffer, CheckForLicense, szCode);     // copy the original routine
    int CRC = GetCRC(Buffer, szCode);
    nCBytes = Compress(Buffer, szCode);            // user-supplied code. nCBytes = size after compression
    Encrypt (Buffer, nCBytes);                     // encrypt it
    SaveBuf (Buffer, nCBytes);                     // save output to disk
    printf ("code size: %d, CRC=%d\n", (char *)End-(char *)Encrypt, CRC);
}

#else if GENERATE_RUNTIME_CODE
// a table of encrypted absolute subroutine addresses linked for the runtime executable
void *AbsAddrTable[3] = { (void *)(char *)printf + 0x76532984),
                          (void *)(char *)exit   + 0xD91E639A),
                          (void *)0x81663874};    // can add random #'s to confuse hackers

const UCHAR EncryptedRoutine1[] = {
0xAA, 0x72, 0x13, 0xAA, 0x74, 0x98, 0xEB, 0x70, 0x3C, 0x99, 0x53, 0x18, 0xC1, 0x6A, 0xA2, 0xE7,
0xFA, 0x6J, 0x05, 0x53, 0x76, 0x97, 0x63, 0x6F, 0x8F, 0xFF, 0xFC, 0x0F, 0x96, 0x82, 0x3F, 0x43,
0x3F, 0x48, 0xFA, 0x51, 0xFF, 0xFE, 0x20, 0x58, 0x54, 0x50, 0x38};

#define CRC1  0x7682   // CRC of original code
#define SIZE1  43      // size of original code before compression
// This code just unscrambles for illustration. Use a true private/public key algorithm in your application.
void Decrypt (UCHAR *Buf, int szBuf)
{
    for (int i=0; i<szBuf; i++)
        Buf[i] = (UCHAR)((Buf[i] ^ (~i)) - i);
}
#endif

void main (void)
{
#ifdef GENERATE_ENCRYPTED_CODE
    Generate();                                    // generate the encrypted bytes, then quit
    exit(0);
#else if GENERATE_RUNTIME_CODE
    int nCBytes = sizeof(EncryptedRoutine1);       // get size of compressed code
    UCHAR  *Ram = new UCHAR[SIZE1];                // get a buffer from memory
    memcpy   (Ram, EncryptedRoutine1, nCBytes);    // copy the encrypted bytes
    Decrypt  (Ram, nCBytes);                       // decrypt the encrypted bytes
    Uncompress(Ram, nCBytes);                      // user-supplied decompression code

    if (GetCRC(Ram, SIZE1) != CRC1)                // check if have decrypted correctly
        exit(0);                                   // no, code is still encrypted, so quit

    // create a pointer to the code
    void (*pCheckForLicense)(void *, void *) = (void(*)(void *, void *))Ram;
    // execute the decrypted code
    pCheckForLicense(AbsAddrTable[0], AbsAddrTable[1]);

        :       :                                  // other user code
#endif
}
```

Capacitor improves efficiency in CPU supply

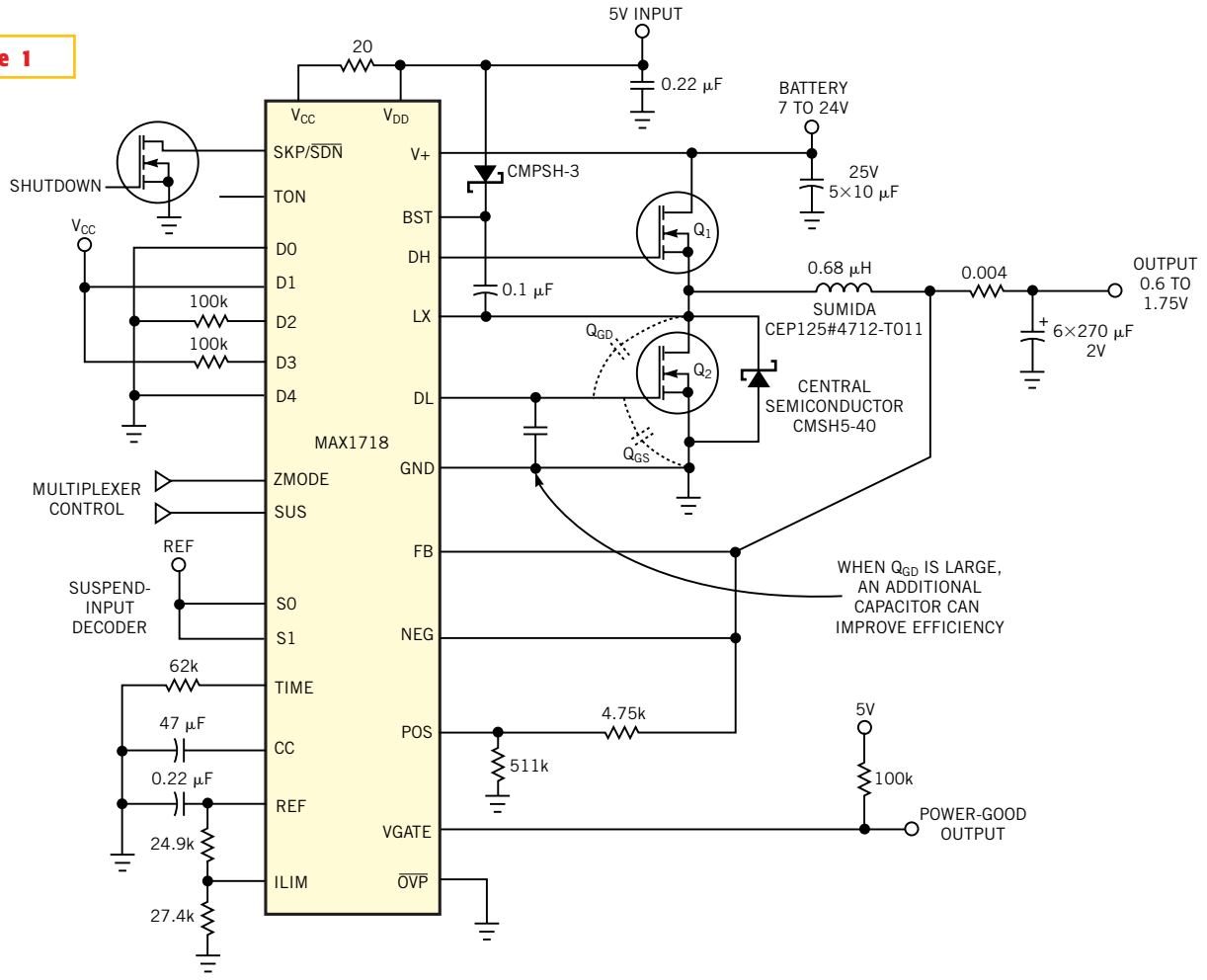
Masami Muranaka, Maxim Integrated Products, Tokyo, Japan

High efficiency is important for the dc/dc buck converters that supply high currents in notebook PCs. This efficiency extends battery life and minimizes temperature rise. A low-dissipation synchronous rectifier using an external MOSET provides this high efficiency. Synchronous rectifiers require special attention, however. Poor designs allow shoot-through current when the high- and low-side MOSFETs conduct simultaneously. Some designers believe that providing enough dead time between the turn-off of one MOSFET and the turn-on of the other can eliminate this problem, but using dead time is inadequate in some applications. **Figure 1** illustrates a step-down power supply in which a step-down controller, the MAX1718, provides the CPU's core supply. Recent CPU cores require a 1 to 2V supply rail at more than 20A of input current. The input-voltage range, on the other hand, is 7 to 20V. This scenario dictates a low duty cycle for the high-side MOSFET.

Obtaining high efficiency with a low duty cycle requires different types of MOSFETs for the high- and low-side devices, Q_1 and Q_2, respectively. Q_1 requires high switching speed even if its on-resistance is relatively high, but Q_2 requires low on-resistance even if its switch speed is relatively low. This combination of parameters allows no possibility of shoot-through current when Q_2 turns on, because Q_1's fast turn-off occurs first. Because Q_2's turn-off is slow, however, you must allow enough dead time before Q_1 turns on. The MAX1718 solves this problem by monitoring Q_2's gate voltage, thereby ensuring that Q_1 turns on only after Q_2 shuts completely off.

Now, consider a third condition leading to the possibility of shoot-through

Figure 1



A buck-regulator IC drives external power MOSFETs to form a CPU-core power supply.

current: a rise in Q_2's gate voltage when Q_1 turns on because of high dV/dt at Terminal LX. That condition can appear even with sufficient dead time, because it involves high current flow into Terminal DL through Q_2's gate-drain capacitance, Q_{GD}. The MAX1718's ample current-sinking ability at DL solves this problem. Sometimes, however, if Q_2's gate-drain capacitance is large, the trace from DL is long, or both, you can eliminate the shoot-through current by adding a capacitor of several thousand picofarads between the gate and the source of Q_2. **Figure 2** shows that the addition of a 4700-pF capacitor improves the high-current efficiency of the circuit in **Figure 1** by a considerable margin. However, note that using a too-large gate-source capacitor, Q_{GS}, can increase the driver's losses.

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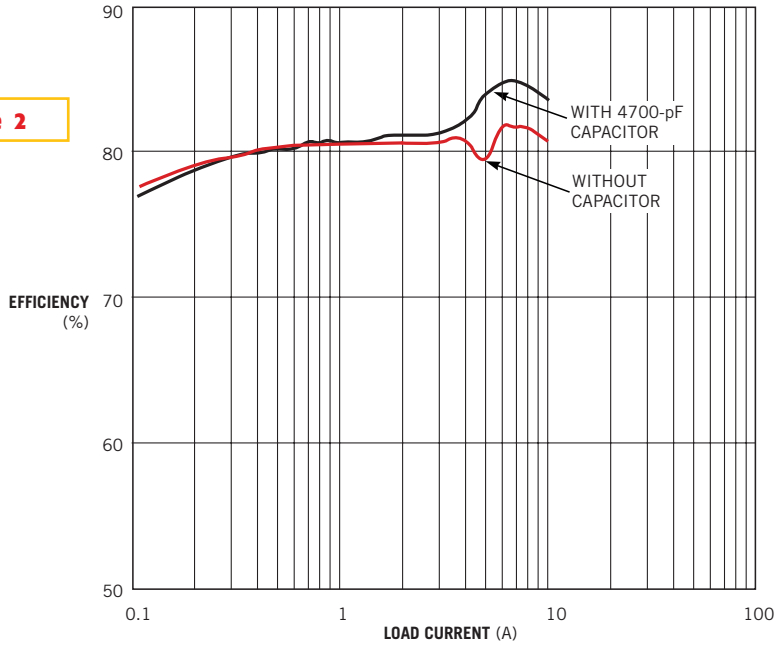
Figure 2



NOTES:
BLACK LINE REPRESENTS TWO µPA2701s.
RED LINE REPRESENTS TWO µPA2700s.
V_{IN}=20V; V_{OUT}=1.3V.

The addition of a capacitor increases high-current efficiency by approximately 3%.

design ideas

Edited by Bill Travis

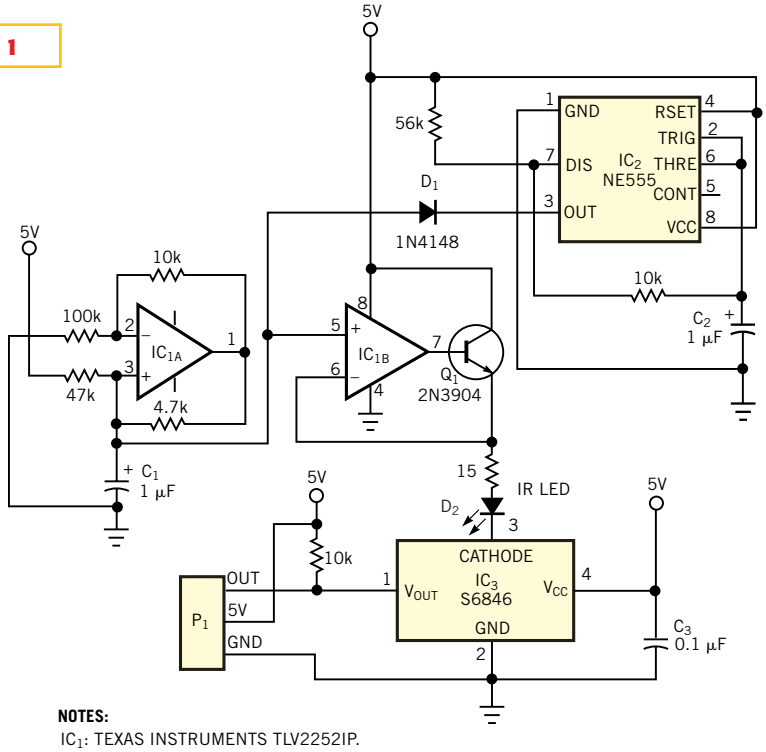
IR distance ranger covers 1 to 20 cm

Paul Florian, McKinney, TX

COMMERCIALLY AVAILABLE IR distance rangers typically handle a 3- to 30-in. detection distance. Many times, it is necessary to determine smaller distances. The circuit in **Figure 1** is useful for measuring small distances to reflective surfaces. Its measurement range is from less than 1 cm to approximately 20 cm for a flat, white surface. The output of the circuit is an active-high pulse at connector P_1. A 12-msec pulse corresponds to the minimum measurable distance; the output frequency is approximately 25 Hz. If the circuit detects no reflection, then the output at connector P_1 remains high. IC_{1A} is a 0.1-mA current source. The source charges C_1 and produces a linear voltage ramp. Every 40 msec, the output of IC_2 switches low and discharges C_1 through D_1. IC_{1B} and Q_1 buffer the voltage on C_1. Q_1 ramps the current through the IR LED from 0 to 60 mA. IC_3 is a synchronous-detection photo IC. IC_3's output switches low when the IC detects a reflection from D_2.

When the reflection distance is small, not much current through the IR LED is necessary to trigger the photo IC, and the pulse-width output is short. When the reflection distance is greater, it takes more current through D_2 to trigger IC_3, and the pulse-width output is greater. The maximum pulse width is always less than 40 msec. The duration of the output pulse also depends on the color of the reflecting surface and the alignment of D_2 and IC_3. D_2 and IC_3 are spaced 0.5 in. apart. A piece of heat-shrink tubing shields the sides of D_2. To align the circuit, leave some extra lead length when you mount D_2 and IC_3. Next, make small bends in the positions of these components while monitoring the output pulse width to achieve the minimum pulse width for a given distance to a reflective surface. With careful adjustment, a detection range of 20 cm is possible to a flat, white surface. The detection distances for nonwhite surfaces are lower.

Figure 1



NOTES:
IC_1: TEXAS INSTRUMENTS TLV2252IP.
IC_2: NATIONAL SEMICONDUCTOR LM555CN.
IC_3: HAMMAMATSU S6846.
D_2: LUMEX OED-EL-1L2.

This circuit detects distances considerably lower than commercial IR rangers.

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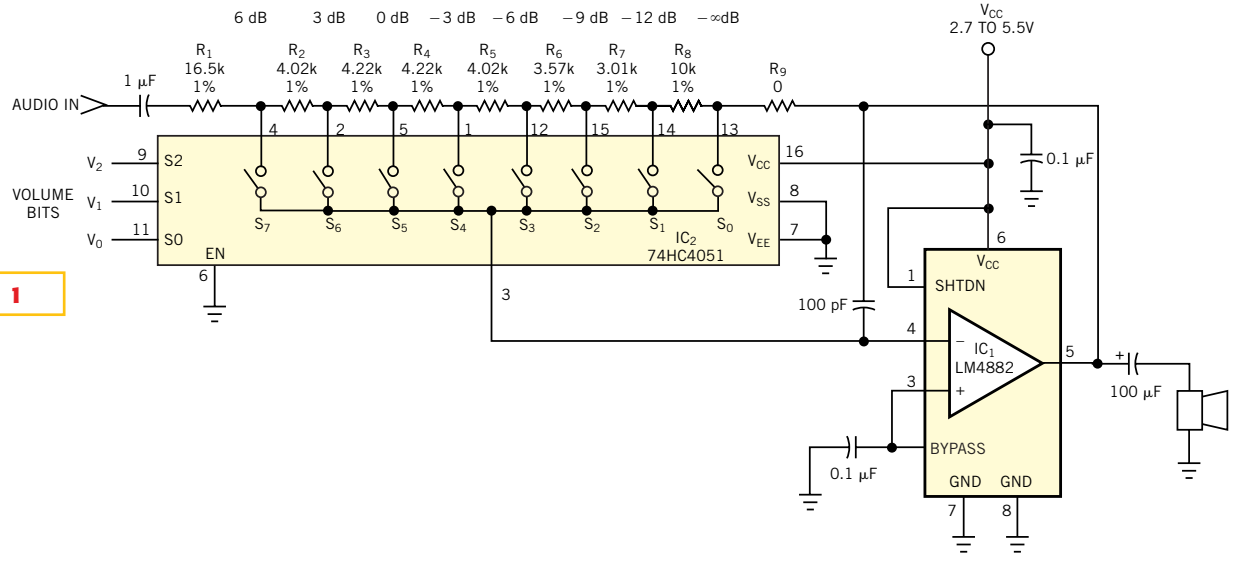
Digital volume control has log taper

Doug Farrar, Los Altos, CA

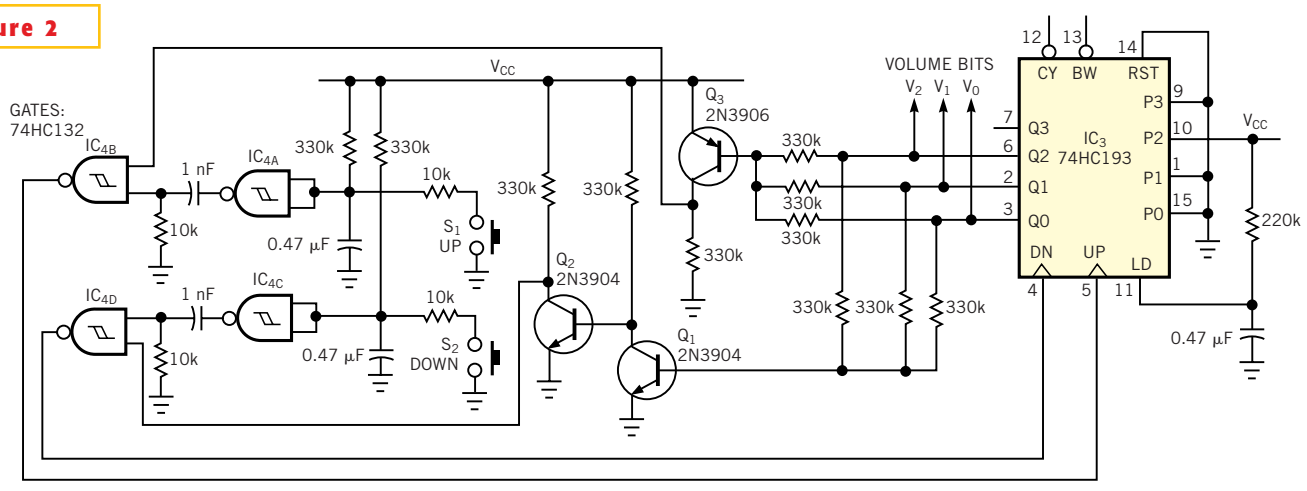
DIGITAL POTENTIOMETERS provide a compact and convenient way to attenuate audio-amplifier signals. However, most such potentiometers suffer from at least one flaw: a nonlogarithmic step increment. To avoid this problem, a user must usually step the potentiometer in a nonlinear sequence to simulate a logarithmic taper. For this reason, the potentiometer needs many taps, and you need software help to complete the design. The circuit in **Figure 1** is a low-cost, digitally attenuated audio amplifier that does not use a digital potentiometer. The circuit attenuates the signal in logarithmic steps, by using an inexpensive 8-to-1 analog switch as its "potentiometer." The resistor string, R_1 through

Figure 1



This circuit sets audio gain logarithmically in 3-dB steps.

Figure 2



Up/down pushbutton switches step the gain in the circuit of Figure 1.

R_8, sets the gain of power amplifier IC_1. Analog multiplexer IC_2 selects one of the eight tap voltages and applies it to IC_1's inverting feedback node. Because only one bias current flows through the nonlinear switches, the topology introduces no measurable distortion.

The amplifier changes gain in 3-dB steps, starting from a high of 6 dB, then decreasing to 3 dB, 0 dB,...−12 dB, and finally −∞ dB (in other words, "mute" or "off") as you step the volume bits V_2 to V_0 from 7 to 0. If you don't want to turn off the amplifier at the minimum-volume setting, you could change resistor R_9 to a finite value for whatever end-attenuation level you desire. The assumption in **Figure 1** is that your system has a way to generate the 3-bit volume codes. For those applications that do not have these bits available, you can use the circuit in **Figure 2** to generate them. Pushing switches S_1 and S_2 clocks up/down counter IC_3 up and down, respectively. Transistors Q_1 and Q_2 decode the counter's zero state and disable the down clock when the count reaches zero. In this fashion, the circuit limits the counter to a value of 0 to 7. Once you attain a maximum or minimum volume, further pushes on the up and down switches, respectively, have no effect on the volume setting until you go in the opposite volume direction. Standby-current consumption of the logic is almost entirely a function of the resistors you use for Q_1 to Q_3, because the logic chips use almost no power. You can set a nonzero power-up volume by using IC_3's load (LD) pin when you first apply power. In **Figure 2**, the counter powers up at a "4" volume, rather than "0" (muted). 74HCXX logic operates over 2 to 7V, but the power amplifier, IC_1, uses 2.7 to 5.5V. Therefore, IC_1 sets the operating-voltage range.

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Tricks improve on Excel LCD initialization

Aubrey Kagan, Weidmüller Ltd, Markham, ON, Canada

A previous Design Idea on using Excel for LCD initialization relies on the user for cutting and pasting from Excel into an editor (**Reference 1**). It appears that it would take a minimum of six keystrokes or mouse strokes from one character to a new character to perform this operation. This procedure does not allow for the addition of comments, which would be advantageous in the maintenance of the character set. Over a set of 64 characters, a user would take nearly 400 actions. The use of macros would allow for the reduction of these keystrokes or mouse strokes and would probably improve the previous idea.

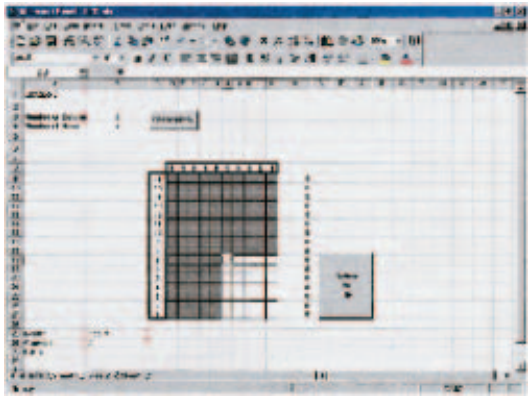

Figure 1 This Excel configuration simplifies LCD-matrix initialization.

In using such macros, rather than copy the numbers associated with characters into the text editor, as the previous Design Idea suggests, you append each sequence of numbers to a text file. When the character set is complete, you can open the text file, massage it with find-and-replace techniques, and then paste it as a whole into a target file. An added benefit is that each sequence appears on a single line rather than having a line for every row of the display. You can maintain this original file for use in both high-level and assembly programs if the need for repeating the process ever arises.

The macro in **Listing 1** performs the following tasks:

- Prompts the user for a comment associated with this character.
- Creates a line consisting of a leader, data separated by a delimiter, a comment symbol, and the comment already entered.
- Takes the file name from the spreadsheet. If the file does not exist, the macro creates a file with the line appended to it. Each time the macro runs, it opens, adds to, and closes the file.
- Clears the entries in the LCD matrix and sets the top-left cell of the matrix as active, ready for the next character.

All the parameters represent data in the cells of the spreadsheet. The file name is in cell A1. (The macro appends the ".txt.") Cell B26 has the leader, B27 has the comment symbol, and B28 has the delimiter between the numbers in the file. You can use this data in assembler or C or some other language, so the **listing** generalizes. C would ignore the "/* db */," and you could universally replace it with "db" if you use an assembler. Similarly, you could globally modi-

fy the comment notation, " ;//" (with a space before the semicolon), in the text file as well. The trailing comma of the line of data is needed in C as part of a constant array but in assembler would generate an error. If you're using an assembler, the global search would look for the sequence " ;//" and replace it with a space and a semicolon. Because of the inconsistent way text editors deal with tabs, the **listing** avoids using the tab character. By modifying the cells, you can easily customize the format. You can implement other changes by modifying the macro, written in Visual Basic for Applications. The following is a sample line from a file:

/* db */ 4 , 12 , 4 , 4 , 4 , 4 , 14 ,;//this is a "1" on a 5×7 matrix.

A button on the spreadsheet allows you to run the macro with a single click (**Figure 1**), so you need not switch from the mouse to the keyboard to run the macro. You can also run the macros from Ctrl-key combinations. (In Excel, you should note that, to run a macro, you must have completed data entry into a cell.) The matrix's 10×16-cell format is also generalized. You can alter this format by entering the number of columns in B3 and the number of rows in B4 and clicking on the Shade Matrix button. This action activates a second macro that shades out the cells not in use. Clicking on the Update to File button triggers a pop-up window requesting a comment. You need not enter the comment symbol, because the macro automatically enters it. The macro then appends the line to the file. The unused rows do not appear in the file. You can download the Excel file in **Listing 1** from the Web version of this Design Idea at www.endmag.com.

REFERENCE

1. Bitti, Alberto, "Excel offers painless LCD initialization" (*EDN*, Sept 20, 2001, pg 98).

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LISTING 1–SAVE-CHARACTER EXCEL MACRO

```
Sub SaveCharacter()
'
' SaveCharacter Macro
' Macro recorded 11/16/01 by Aubrey Kagan
'
' Keyboard Shortcut: Ctrl+Shift+T
'
'if file does not exist then create it.
    Dim sFname As String
    Dim sX As String
    Dim iPoint As Integer
    Dim sComment As String
    Dim iUtil As Integer
    Dim iFileExists As Boolean

    sFname = Range("A1").Value
    sFname = sFname & ".txt"

    sX = Dir(sFname)
    If sX <> "" Then
        iFileExists = True
    Else
        iFileExists = False
        Open sFname For Output As #1
        'take the comment symbols an place the file name as the first
        'comment

        sX = Range("B27").Value & sFname
        Print #1, sX
        Close #1
        'file created and saved
    End If
    'now we print a range of values across the page
    'associated with the bytes for the pixels
    iPoint = 24
    iPoint = iPoint - (Range("B4").Value - 1)
    sX = iPoint
    'converting typ to string
    sX = "R" & sX
    sX = sX & "C14"
    'pointing at the start of the data
    Application.Goto Reference:=sX

    'get character description
        sComment = InputBox("Enter you comment for this Character", "Comment
Creation")

        Open sFname For Append As #1
        Print #1, Range("B26").Value;

        For iUtil = 0 To (Range("B4").Value - 1)
            sX = (iPoint + iUtil)
            sX = "R" & sX
            sX = sX & "C14"
            'placing the cursor at the data address
            Application.Goto Reference:=sX
            Print #1, ActiveCell.Value;
            Print #1, Range("B28").Value;
            'print value followed by the delimiter
        Next

        sComment = Range("B27").Value & sComment
        Print #1, sComment

        'ensure all files are closed
        Close
    'as a final step clear the page for the next character
        Range("D9:M24").Select
        Selection.ClearContents
        'move to the top left hand of screen
        'first deal with rows
        iPoint = 24
        iPoint = iPoint - (Range("B4").Value - 1)
        sX = iPoint
        'type conversion
        sX = "R" & sX & "C"
        'concantenate for rows and add C for columns
        iPoint = 13
        iPoint = iPoint - (Range("B3").Value - 1)
        sX = sX & iPoint
        'should do the conversion as well
        Application.Goto Reference:=sX

    End Sub
```

Unidirectional counters accumulate bidirectional pulses

Stephen Woodward, University of North Carolina, Chapel Hill, NC

QUADRATURE-OUTPUT incremental optical shaft encoders are popular in high-performance, bidirectional rotation-sensing applications. Available with resolution options extending beyond 2000 pulses/revolution, incremental encoders provide a fast, inexpensive, and reliable way to digitally read out bidirectional mechanical motion. The encoders are fast, too; you can usually operate them at 10,000 rpm and faster. However, the interface logic they need can sometimes be somewhat problematic. Such logic typically includes at least one long-bit-length (for example, 16-bit) bidirectional counter. Although several handy peripheral chips, such as the 8253, 8254, and 9511, are available that implement flexible *unidirectional* counting, *bidirectional*-counter chips are relatively scarce. ASICs exist that can provide the needed function, and hard-wired or programmable logic is a viable approach. Unfortunately, none of these alternatives is ideal from a cost or pc-board-area standpoint. The configuration in **Figure 1** combines the industry-standard 82C54 unidirectional counter-timer peripheral chip with simple software to provide a convenient interface of quadrature encoders with the ISA I/O bus. The technique digitizes bidirectional motion without tears.

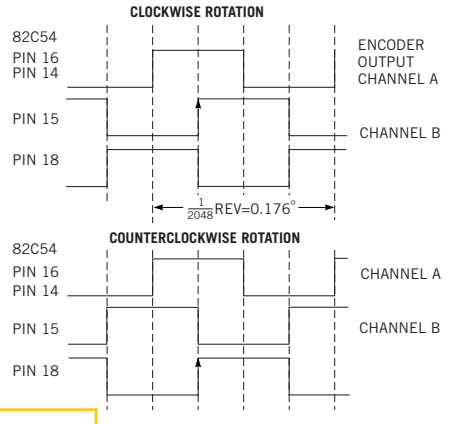

Figure 2 These timing signals illustrate the operation of the circuit in Figure 1.

As **Figure 2** illustrates, the trick is to use two unidirectional counters of the three that the 82C54 contains. You use one counter for each encoder-rotation direction. One of the encoder quadrature-output signals, A, drives the gate pins of both counters. This connection selectively enables counting once every encoder-output cycle. A couple of Schmitt-trigger inverter stages phase-split the other encoder output, B, into two complementary signals. One phase drives the trigger input of the clockwise counter (82C54, Counter 1); the other phase drives the trigger input of the

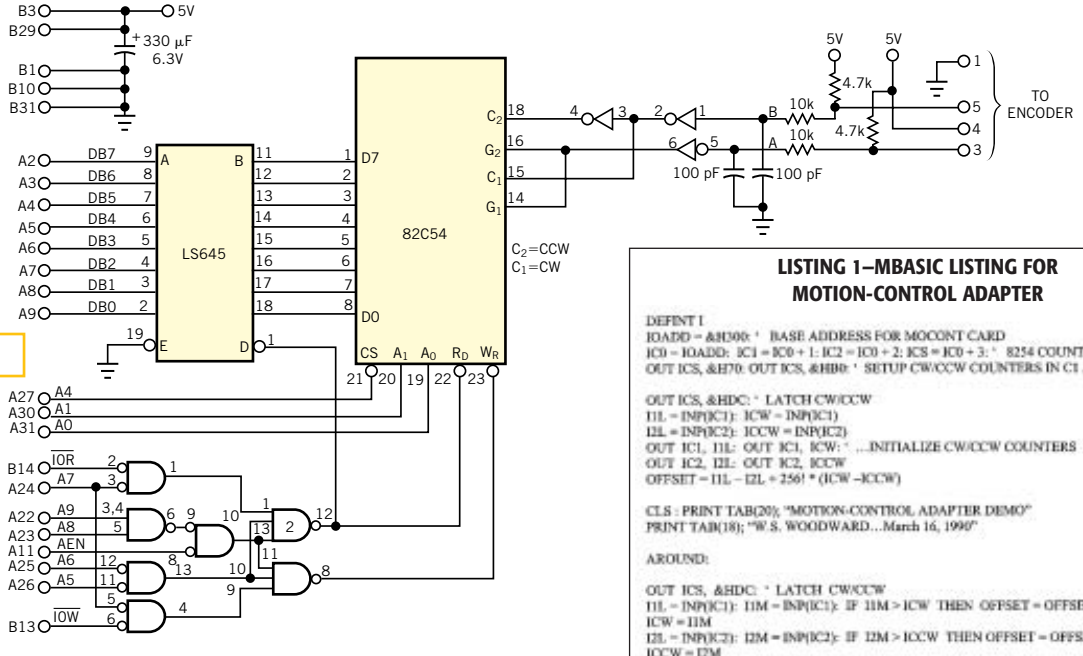

Figure 1 This technique uses unidirectional counters to encode bidirectional encoder signals.

LISTING 1—MBASIC LISTING FOR MOTION-CONTROL ADAPTER

```
DEFINT I
IOADD = &H300: ' BASE ADDRESS FOR MOCONT CARD
IC0 = IOADD: IC1 = IC0 + 1: IC2 = IC0 + 2: ICS = IC0 + 3: ' 8254 COUNTER ADDRESSES
OUT ICS, &H70: OUT ICS, &HB0: ' SETUP CW/CCW COUNTERS IN C1 AND C2

OUT ICS, &HDC: ' LATCH CW/CCW
I1L = INP(IC1): ICW = INP(IC1)
I2L = INP(IC2): ICCW = INP(IC2)
OUT IC1, I1L: OUT IC1, ICW: ' ...INITIALIZE CW/CCW COUNTERS
OUT IC2, I2L: OUT IC2, ICCW
OFFSET = I1L - I2L + 256! * (ICW -ICCW)

CLS : PRINT TAB(20); "MOTION-CONTROL ADAPTER DEMO"
PRINT TAB(18); "W.S. WOODWARD...March 16, 1990"

AROUND:

OUT ICS, &HDC: ' LATCH CW/CCW
I1L = INP(IC1): I1M = INP(IC1): IF I1M > ICW THEN OFFSET = OFFSET + 65536
ICW = I1M
I2L = INP(IC2): I2M = INP(IC2): IF I2M > ICCW THEN OFFSET = OFFSET - 65536
ICCW = I2M
LOCATE 3, 10: PRINT I1L - I2L + 256! * (I1M - I2M) -OFFSET

GOTO AROUND
```

counterclockwise counter (82C54, Counter 2). The result is that only the clockwise counter, Counter 1, is active during the active B transition during clockwise rotation, and only the counterclockwise counter, Counter 2, is active during counterclockwise rotation.

Listing 1, written in MBasic, suffices to periodically latch, read, and sum the counter contents to produce a continuous 32-bit readout of encoder position. You can download **Listing 1** from the Web version of this Design Idea at www.ednmag.com. The technique can easily accommodate pulse rates as high as 500 kHz. Passive RC filtering and Schmitt-trigger signal conditioning provide robust rejection of noise pickup in the encoder cabling. The design is thus suited for typical industrial motion-sensing applications.

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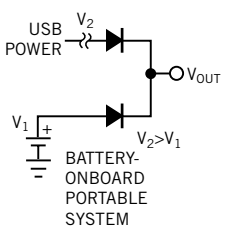
Build a UPS for USB devices

Mark Cherry and Jean-Claude Ailloud,
Maxim Integrated Products, Sunnyvale, CA, and France

Portable systems often include circuitry that derives power from an external source, such as USB. When the system disconnects from the USB supply, a battery takes over and supplies current via a dc/dc converter. A diode-OR connection (**Figure 1**) offers the easiest way to ensure that the supply voltage doesn't sag during this switchover to the battery. The diode's forward voltage drop, however, can reduce battery life and efficiency. The single-cell, boost-converter circuit with external PFET (**Figure 2**) is an improvement over the diode-OR connection. The PFET, Q_1, coupled with IC_1's internal gain block, forms a linear regulator. The USB power supply has a diode-OR connection to Q_1's source. Setting the boost converter's output to 3.4V allows the drain of Q_1 to regulate to 3.3V. This configuration produces negligible loss in Q_1.

Figure 1



A diode-OR connection is effective but lossy.

The bus-supply voltage available to USB devices ranges from 4.4 to 5.25V. When you connect the bus, it forward-biases D_1 and causes the boost converter to idle. The converter continues to idle as long as its output remains above the 3.4V regulation point. The bus supply serves the load and activates the current source to charge the battery. Adjusting R_1 allows you to set the current-source output to charge the nickel-metal-hydride cells at a level one-tenth the battery's capacity. Disconnecting the circuit from the USB supply causes the boost converter to cease idling and supply current to the load via the battery. **Figure 3** shows that the load current suffers no interruption during a switchover from USB to battery.

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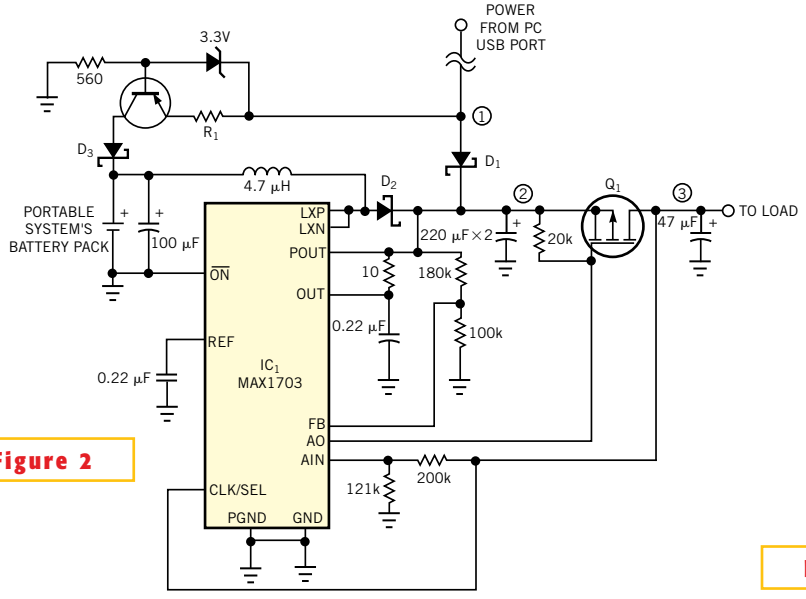


Figure 2

A boost-converter circuit is an improvement over the simple diode-OR connection.

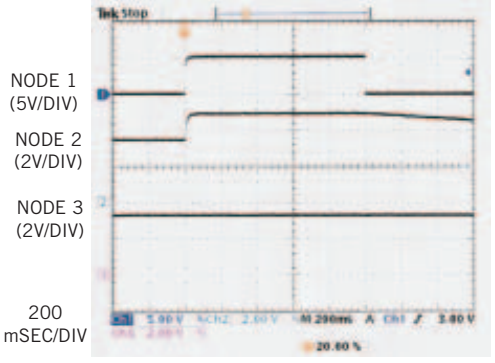


Figure 3

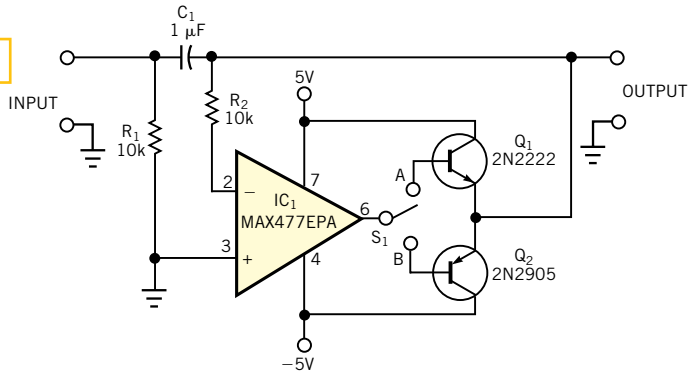
These waveforms (bottom trace, load voltage) show that the load current suffers no interruption during a switchover from USB to battery.

Circuit forms high-frequency polarity clamp

Shyam Tiwari, Sensors Technology Private Ltd, Gwallor, India

You need a negative signal clamp to protect an ADC against negative-going signals while measuring the positive pulse shape of the signal by digitizing the waveform. In other words, you must clamp negative signals at 0V. The circuit in **Figure** 1 can clamp either positive or negative pulses to ground. The circuit uses a fast MAX-477EPA amplifier to drive the Q_1 or Q_2 to clamp signals of either positive or negative polarity. Q_1 forces negative signals to a 0V level; Q_2 does the same for positive signals. You use an spdt switch to choose the transistor of interest. The circuit works over 1 kHz to 10 MHz. You can also make the clamp operate at frequencies as high as 100 MHz by replacing $C_1$with a 1-kΩ, 0.5W resistor. However, the output would need another MAX477EPA buffer amplifier to drive the 50Ω signal cable, because the circuit's output impedance increases to 1 kΩ.

Figure 1



This simple circuit clamps either positive or negative signals to ground.

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design ideas

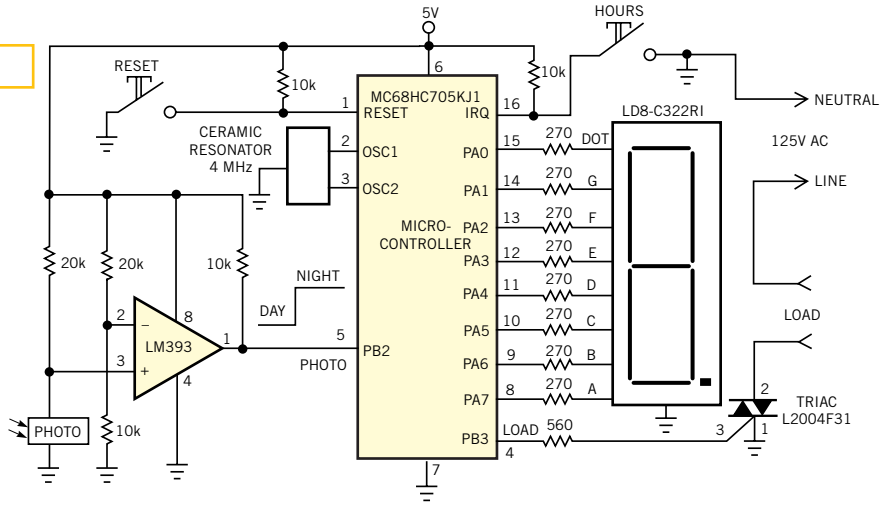
Edited by Bill Travis

Simple phototimer controls load

Abel Raynus, Armatron International, Melrose, MA

IN INDUSTRIAL and home applications, the need sometimes exists for a device that, after activation by some physical effect, such as light, temperature, or sound, switches a load on for a predetermined time. The load, such as a lamp, motor, solenoid, or heater, usually derives its power from the ac line. The phototimer in **Figure 1,** based on an inexpensive MC68HC705KJ1 microcontroller, is a simple and inexpensive way to satisfy this need. A load switches on when it becomes dark and stays on for an interval that an operator sets with the Hours pushbutton switch. A seven-segment LED display shows the interval. The time value is a function of the design objectives, the microcontroller software, and the display-interface complexity. The design in **Figure 1** is simple, because it needs only one pushbutton switch and a single-digit display.

Figure 1



When it becomes dark, this circuit turns the load on for a predetermined interval.

The heart of the design is the microcontroller software (**Listing 1**). The routine serves manual and automatic operating modes. The initialization process sets the manual, or continual, mode. This

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LISTING 1–ROUTINE FOR PHOTOTIMER-LOAD CONTROLLER

```
                        1
                        2  $list
0000                    3  $PAGEWIDTH 160
0000                    4          org MOR;    resistor osc and input pulldown
07F1                    5          fcb %00100000;
07F1      20            6  ******  I/O PORT BITS ****************************
                        7  LED      equ pA0
07F2                    8  g        equ pA1
07F2                    9  f        equ pA2
07F2                   10  e        equ pA3
07F2                   11  d        equ pA4
07F2                   12  c        equ pA5
07F2                   13  b        equ pA6
07F2                   14  a        equ pA7
07F2                   15  Photo    equ pB2
07F2                   16  Load     equ pB3
07F2                   17  ********** VARIABLES ****************************
00C0                   18          org RAM
00C0                   19  Treg     rmb 1 ;Time register
00C1                   20  Tcnt     rmb 1 ;Time counter
00C2                   21  cnt1h    rmb 1 ;counter for 1 hour
00C3                   22  cnt30s   rmb 1 ;counter for 30 sec
00C4                   23  cnt1s    rmb 1 ;counter for 1 sec
                       24  ******  7-segment CODE TABLE address *************
00C5                   25  adr7s    equ  ROMend+1-$0b ;for 11 constants
                       26  ******     INITIALISATION  ************************
0300                   27          org ROM
0300 [02] A6FF         28  init     lda    #$ff   ;set prtA as output
0302 [04] B704         29          sta    ddrA
0304 [05] 3F00         30          clr    prtA   ;
0306 [05] 1605         31          bset   3,ddrB ;set pB3 as output
0308 [05] 1701         32          bclr   Load,prtB ;set Load  off
030A [05] 3FC0         33          clr    Treg   ;clear
030C [05] 3FC1         34          clr    Tcnt   ;    all
030E [05] 3FC2         35          clr    cnt1h  ;      registers
0310 [05] 3FC3         36          clr    cnt30s ;              used
0312 [05] 3FC4         37          clr    cnt1s
0314 [02] 9A           38          cli            ;Interrupt enable
```

(continued on pg 94)

setting means, that after a 30-sec delay, the load switches on and stays on until you press the Reset pushbutton. The 30-sec delay allows you to change your mind and choose an automatic mode. During the manual mode, the display exhibits "C" for continual. The dot on the display lights every time the load is on, a useful feature when the timer and the load are far away from each other. By pressing the Hours pushbutton, you change the manual mode to an automatic one. In the automatic mode, the display exhibits a time delay in hours. When you press and hold the pushbutton, the digits increment automatically from 1 to 9 every second. This feature comes about by using counter modulo 9 in the external interrupt-service routine (lines 85 to 92 in **Listing 1**). You can download the software associated with this circuit from the Web version of this Design Idea at www.ednmag.com.

After the time-delay setting elapses, the microcontroller waits for night—in other words, for a high level on the Photo input—to switch on the load. During that wait, the dot in the display blinks in 1-sec intervals. When it becomes dark, the LM393 voltage comparator's output switches high and triggers the program to continue. The load switches on, and the dot in the display stops blinking and stays on. The display digit shows the elapsed working time. When this time expires, the load and the dot in the display switch off, and the display exhibits "E." You can stop the process at any time by pressing the Reset pushbutton. Otherwise, the microcontroller automatically repeats the entire sequence every night. The circuit in **Figure 1** is extremely flexible. The circuit can switch on the load using any physical effect just by changing the sensor on the comparator input. You can also modify the software for different time delays. As an example, you might want to display two-digit hours and two-digit minutes. In this case, you should use decoder/drivers, such as the CD4511 or MM74HC138, to configure an interface with the display.

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LISTING 1—ROUTINE FOR PHOTOTIMER-LOAD CONTROLLER (CONTINUED)

```
0315 [03] BEC0          39  main    ldx     Treg      ;Treg --> X
0317 [06] CD0363        40          jsr     display   ;Time --> display
031A [06] CD03A8        41          jsr     dly30s    ;delay 30 sec
031D [04] 3DC0          42  mode    tst     Treg      ; Treg = 0?
031F [03] 274D          43          beq     manual
0321 [05] 1100          44          bclr    LED,prtA     ;LED off
0323 [05] 1701          45          bclr    Load,prtB    ;Load off
0325 [05] 050130        46  Auto    brclr   photo,prtB,blink;is it a day?
0328 [05] 1100          47          bclr    LED,prtA     ;LED off
032A [06] CD03A8        48          jsr     dly30s       ;delay for 30 sec
032D [05] 050128        49          brclr   photo,prtB,blink;is it a day?
0330 [05] 1601          50          bset    Load,prtB    ;Load on
0332 [05] 1000          51          bset    LED,prtA     ;LED on
0334 [03] B6C0          52          lda     Treg         ;Treg --> Tcnt
0336 [04] B7C1          53          sta     Tcnt
0338 [06] CD03B4        54  work    jsr     dly1h        ;delay for 1 hour
033B [05] 3AC1          55          dec     Tcnt         ;decrement Tcnt
033D [03] 2707          56          beq     TimeEnd      ;time is expired
033F [03] BEC1          57          ldx     Tcnt         ;Tcnt --> X
0341 [06] CD0363        58          jsr     display      ;new Time --> display
0344 [03] 20F2          59          bra     work
0346 [05] 1701          60  timeEnd bclr    Load,prtB    ;Load off
0348 [02] A60A          61          ldx     #$a          ;"E" --> display
034A [06] CD0363        62          jsr     display
034D [05] 0401FD        63  night   brset   photo,prtB,night;wait for a dawn
0350 [06] CD03B4        64          jsr     dly1h        ;delay for 1 hour
0353 [05] 0401F7        65          brset   photo,prtB,night;wait for a dawn
0356 [03] 20BD          66          bra     main
                        67  ********************************************
0358 [06] CD039C        68  blink   jsr     dly1s     ;delay 1 sec
035B [03] B600          69          lda     prtA
035D [02] A801          70          eor     #%00000001
035F [04] B700          71          sta     prtA
0361 [03] 20C2          72          bra     Auto
                        73  ********************************************
0363 [05] D607C5        74  display lda     adr7S,x ;code,x --> Acc
0366 [04] B700          75          sta     prtA    ;Acc --> prtA
0368 [05] 070102        76          brclr   Load,prtB,disEnd ;is Load off?
036B [05] 1000          77          bset    LED,prtA ;LED on
036D [06] 81            78  disEnd  rts             ;return from display
                        79  ********************************************
036E [05] 1000          80  manual  bset    LED,prtA    ;LED on
0370 [05] 1601          81          bset    Load,prtB   ;Load on
0372 [03] 20A9          82          bra     mode
0374 [06] CD0392        83  ExtInt  jsr     dly01s  ;debouncing delay 100 ms
0377 [03] 2F12          84          bih     m3      ;if IRQ=1,end of Interrupt
0379 [03] BEC0          85  m0      ldx     Treg    ;Treg -->X
037B [02] A309          86          cpx     #9      ;Treg > 9?
037D [03] 240F          87          bhs     m1
037F [05] 3CC0          88          inc     Treg    ;Treg + 1
0381 [03] BEC0          89  m2      ldx     Treg    ;Treg --> X
0383 [06] CD0363        90          jsr     display ;Treg --> display
0386 [06] CD039C        91          jsr     dly1s   ;delay 1 sec
0389 [03] 2EEE          92          bil     m0      ;is IRQ-pin still low ?
038B [05] 120A          93  m3      bset    IRQR,ISCR ;IRQ reset
038D [09] 80            94          rti               ;return from ExtInt
038E [05] 3FC0          95  m1      clr     Treg    ;0 --> Treg
0390 [03] 20EF          96          bra     m2
0392 [02] A680          97  dly01s lda #128T       ;100 ms delay
0394 [03] 5F            98  lp1     clrx
0395 [03] 5A            99  lp2     decx
0396 [03] 26FD         100         bne lp2
0398 [03] 4A           101         deca
0399 [03] 26F9         102         bne lp1
039B [06] 81           103         rts
                       104 ************************************
039C [02] A60A         105 dly1s   lda #10T   ;0,1s x10=1sec delay
039E [04] B7C4         106         sta cnt1s
03A0 [06] CD0392       107 d1s     jsr dly01s
03A3 [05] 3AC4         108         dec cnt1s
03A5 [03] 26F9         109         bne d1s
03A7 [06] 81           110         rts
                       111 ************************************
03A8 [02] A61E         112 dly30s  lda #30T ;1s x30=30sec delay
03AA [04] B7C3         113         sta cnt30s
03AC [06] CD039C       114 d30s    jsr dly1s
03AF [05] 3AC3         115         dec cnt30s
03B1 [03] 26F9         116         bne d30s
03B3 [06] 81           117         rts
                       118 ************************************
03B4 [02] A678         119 dly1h   lda #120T ;30s x120=1 hour
03B6 [04] B7C2         120         sta cnt1h
03B8 [06] CD03A8       121 d1h     jsr dly30s
03BB [05] 3AC2         122         dec cnt1h
03BD [03] 26F9         123         bne d1h
03BF [06] 81           124         rts
                       125 ************************************
07C5                   126          org    adr7s
07C5       9C60DAF2    127          fcb    $9c,$60,$da,$f2,$66
           66
07CA       B63E0FE      128          fcb    $b6,$3e,$e0,$fe,$e6,$9e
           E69E
                       129 ************************************
07FA                   130          org    VECTORS+2
07FA       0374        131          fdb    ExtInt
07FE                   132          org    VECTORS+6
07FE       0300        133          fdb    init
```

Delay line upgrades vintage scope

Robert Houtman, Blaine, WA

Vintage triggered-sweep oscilloscopes find use in many applications. However, they have no internal delay line, so they can't display the pulse that triggers the sweep. Moreover, early laboratory scopes contain delay lines having insufficient delay to display such pulses during a uniform portion of the sweep. With such oscilloscopes, the true pulse shape remains a mystery. You can circumvent these limitations if you add an external delay line and equalizer. The scope can then display the exact trigger-point trace. The instrument then becomes easier to use, and the measurements become more trustworthy. For every additional microsecond of equalized cable, the scope can display a microsecond of pretrigger information. **Figure 1** shows the components you need to implement these improvements on a Philips PM3230 10-MHz oscilloscope. The components are a wideband amplifier to restore the signal to its original level and provide a trigger; a 750-nsec delay cable; and a passive, two-stage equalizer.

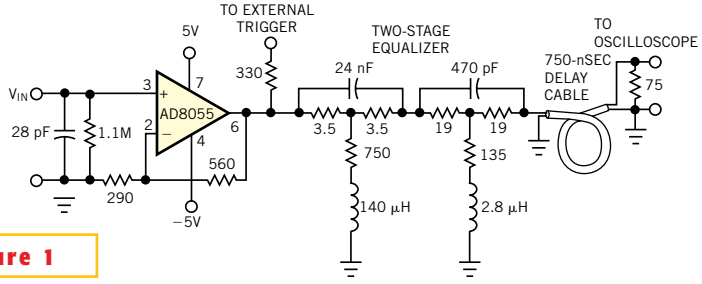

Figure 1 This circuit modifies vintage oscilloscopes having no internal delay line.

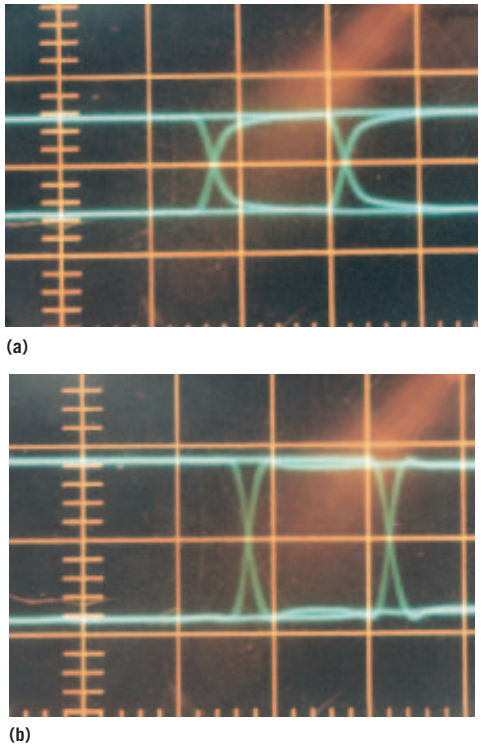

Figure 2 The step response through the 750-nsec cable (a) and the complete network, including the cable (b), differs.

CATV cables, such as RG6U, RG59U, and others, are commonly available at garage sales and second-hand stores. You connect the 75Ω cables with solid or foam dielectrics using standard CATV connectors to make the 750-nsec delay line. A low-impedance driver displays the bipolar step response of the delay line, as the eye pattern in **Figure 2a** shows. The delay line transmits approximately 65% of the signal at audio frequencies, because of resistive losses. The losses increase at higher radio frequencies, because of the skin effect in the conductor. The theoretical form for the step response that the skin-effect loss causes is a complementary error function, $\mathrm{cerf}(kl/\sqrt{t})$ (**Reference 1**). The time, t, refers to the start of the step after traversing the cable of 160m length. Computer evaluation of this function shows the constant to be $k=2.6\times10^{-7}(\mathrm{sec})^{0.5}/\mathrm{m}$ for best agreement with the step response in **Figure 2a**. You cannot adequately correct this functional form by using the usual single-bridged-T filter. You therefore apply time-domain methods to obtain the two-stage, pole-zero-cancellation equalizer in **Figure 1** (**Reference 2**). This double-bridged-T filter corrects the cable's phase and amplitude distortion over a 10-MHz band.

Each of these two filters is basically a resistive attenuator, but fast steps can bypass the attenuation during a time constant, τ. For short times, the equalizer's input port sees a load of only the 75Ω cable via the capacitor, which presents a short circuit at high frequencies. The inductor presents an open circuit at high frequencies, so the resistors have no effect for short times. Eventually, as t surpasses τ in the step response, the capacitor and inductor yield to the resistive attenuator while presenting the 75Ω load to the equalizer's input. With only the first, τ=180-nsec filter, the step response becomes a more finely rounded waveform. With the second, τ=25-nsec filter, the step response is a sharp step, limited only by the oscilloscope's bandwidth. Each filter resides in a reclaimed CATV signal-splitter box. You can connect these 75Ω constant-resistance filters at various locations along the delay line without incurring reflections. You can therefore use this arrangement to fine-tune the passive components to eliminate residual reflections, using time-domain reflectometry.

The AD8055-based amplifier has greater-than-100-MHz bandwidth, fully adequate for the 10-MHz oscilloscope. Its input impedance is 1 MΩ in parallel with 30 pF to match the oscilloscope's input and its low-capacitance probes. **Figure 2b** shows the final eye pattern, using the amplifier, the two-stage equalizer, and the 750-nsec delay cable. This pattern is essentially identical to the eye pattern that ensues using the oscilloscope without the circuit in **Figure 1**, except for the 750-nsec temporal shift. You

can see the benefit of the circuit in **Figure 3**. Trace A shows the original impulse response of the oscilloscope without the circuit. Trace A is merely an uninteresting, featureless trace. For Trace B, the input impulse passes through the amplifier to the external-trigger input and then through the equalizer and delay cable to the oscilloscope's input. Because its delay is longer than the intrinsic delay of the oscilloscope in starting its sweep, a clean pulse of approximately 20 nsec appears on the display. You can now use the complete unit as a 10-MHz laboratory oscilloscope.

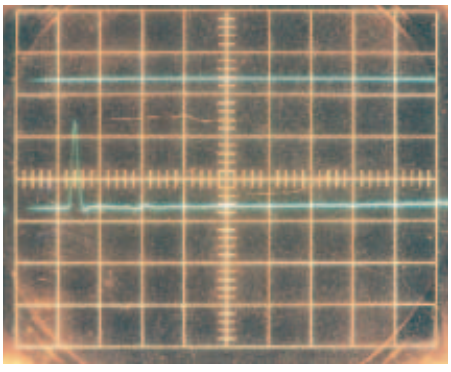

Figure 3 Traces A and B show the impulse response, respectively, without and with the delay network.

You can define an input impulse as an even function composed purely of cosine waves of zero phase. However, the cable's impulse response is simply the derivative of the waveform in **Figure 2a** and acquires a long, slow tail. This impulse response is thus no longer an even function, so its composite cosine waves have evidently acquired various phase shifts accruing to the cable. **Figure 3** illustrates that the circuit in **Figure 1** corrects these phase shifts and amplitude variations. Trace B shows a short, symmetrical pulse with no tail, an even function as similar as possible to the input impulse using this oscilloscope.

References

1. Nahman, NS, "The measurement of baseband pulse risetimes of less than 10^{-9} second," *Proceedings of the IEEE*, Volume 55, No. 6, June 1967, pg 855.

2. Houtman, Hubert, "1-GHz sampling oscilloscope front-end is easily modified," *Electronic Design*, Sept 18, 2000, pg 175.

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Circuit reduces negative-voltage stresses on control IC

Michael Day, Texas Instruments Inc, Dallas, TX

In a synchronous, buck switching power supply, the two FETS and the output inductor meet at the phase node (**Figure 1**). The phase node often connects directly to the control IC. The voltage on this node swings from the input voltage to some voltage lower than ground. If the voltage goes too far below ground, the ESD structures or other circuitry within the control IC can become forward-biased, causing currents to flow through the chip's substrate. These unwanted currents can cause erratic behavior and damage to the IC under certain circumstances. Although it is impossible to keep the phase node from going below ground, it is necessary to keep the voltage at the control IC from going so far negative that it adversely affects or damages the IC.

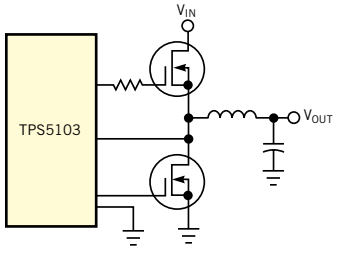

Figure 1 This classic buck regulator suffers from excessive negative phase-node voltage.

Trace A in **Figure 2a** shows the phase-node voltage waveform with V_{IN}=12V, and V_{OUT}=3.5V at 8A. When the top FET is on, the output current flows through that FET and the inductor to the output. During this time, the phase-node voltage is equal to V_{IN}. The bottom FET must remain off until after the top FET fully turns off. When the top FET turns off, the current then flows from ground, through the bottom FET, and through the output inductor. Dead time is the time lag between turning off the top FET and turning on the bottom FET. During the dead time, the current flows through the body diode of the bottom FET, and the phase-node voltage is approximately −1V, depending on the current levels and the FET parameters. When the bottom FET turns on, the current flows through the FET structure rather than through the body diode. During this time, the voltage is a function of the output current and the resistance of the FET.

During the dead time, the negative voltage coupled with parasitic ringing can apply a negative voltage that exceeds the maximum voltage ratings of the control IC. Trace B in **Figure 2b** shows the phase node when the top FET turns off. The output current flows through the body diode of the bottom FET, and the voltage drop across the FET is −0.76V. With the ringing in the circuit, the phase-node voltage can exceed −1V, a voltage applied directly to the control IC. When the bottom FET turns on, the voltage drops to approximately −0.1V (8A× 0.013Ω). Adding a Schottky diode in parallel with the bottom FET helps, but a Schottky diode is large and expensive and has little effect on the voltage. Trace C in **Figure 2b** shows the voltage that occurs with the addition of a large D-Pak MBRD835L Schottky diode. The diode reduces the voltage to −0.6V. With ringing, the control IC sees −0.7V.

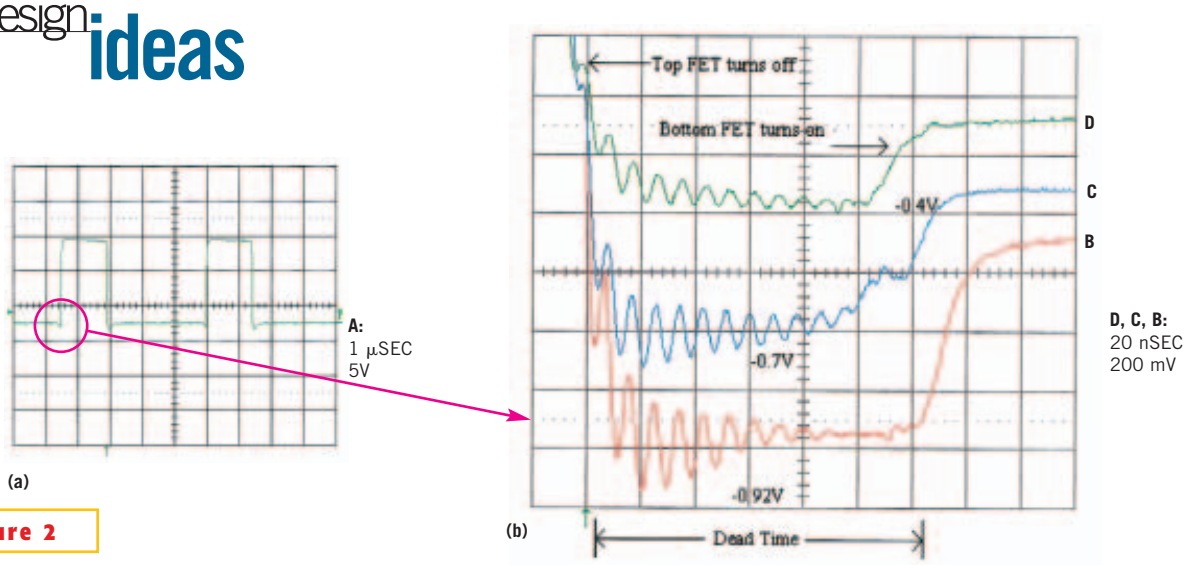

Figure 2

Expanding the dead-time waveforms (a) leads to three scenarios (b): the unadorned buck regulator (Trace B), adding a Schottky diode (Trace C), and the simple solution in Figure 3 (Trace D).

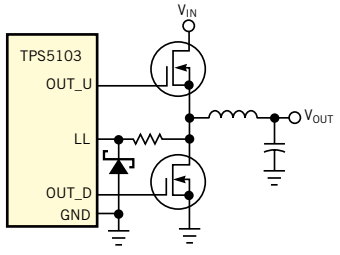

Figure 3

Moving one resistor and adding a small Schottky diode minimizes the phase-node voltage.

The circuit in **Figure 3** is small and inexpensive and significantly reduces the phase-node voltage at the control IC. The gate-drive resistor moves from the gate to the source of the top FET. Following the current from the IC as it charges and discharges the gate capacitance of the top FET shows that moving the resistor has no effect on the circuit operation. An SOT-23 or an SOD-123 Schottky diode with a current rating of 0.5A connects to the control IC. As you can see in Trace D of **Figure 2b**, when the voltage across the FET's body diode goes to −1V, the Schottky diode clamps the voltage on the IC to approximately −0.3V. The full output current flows through the FET, and the gate-drive resistor limits the current through the Schottky diode. This solution is small and inexpensive and prevents erratic operation or damage to the power-supply control IC.

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Track multisite temperatures on your PC

Clayton Grantham, National Semiconductor, Tucson, AZ

The low-cost circuit in **Figure 1** allows you to track four remote temperatures with thermistor sensors through the parallel port on your PC. This four-zone thermometer instrument has a temperature range of −40 to +90°C and a resolution of better than ±1°C. You can calibrate its accuracy to within 1°C over a 0 to 50°C span and within 3°C over a −40 to +90°C span. Thermistors are low-cost, passive, rugged components, making them a good choice for temperature sensing. The signal-conditioning hardware in **Figure 1** performs a simple voltage division to partially linearize the thermistors. Temperature data in the form of thermistor voltages goes into Excel macros, and software performs a fifth-order-equation fit using calibration coefficients to convert the data into Celsius temperatures. This Design Idea focuses on the electronics in Zone 1; the other zones behave similarly. You can implement one, two, three, or all four zones without software modification.

All components have low power (quiescent current) consumption to minimize LPT1 sourcing requirements. Four LPT1 outputs at D0 (Zone 1), D2 (Zone 2), D4 (Zone 3), and D6 (Zone 4) power this application. The hardware typically requires less than 162 µA of current per zone. Parallel-port drivers within your PC generally source at least 400 µA. Supervisory circuit IC_1 monitors the voltage from the LPT1 port. The reset output signal of IC_1 goes back to the parallel port at S7 for software error-checking at initialization. The software ascertains that the hardware is present and that the minimum voltage from D0 of the LPT1 port is greater than approximately 4.65V. Most PCs have a 5V parallel-port interface, but a few have only 3.3V available. For 3.3V PCs, you need to scale the voltage options of the components you use.

IC_2 is a voltage reference for both the RT_1-R_7 voltage divider and the ADC, IC_3. Inasmuch as IC_2 is common to the divider and the ADC, you obtain accurate ratiometric analog-to-digital conversion, and gain, offset, and thermistor-interchangeability errors are at a minimum. The low temperature coefficient of IC_2

(grades are available with lower than 10 ppm/°C) ensures that the circuit exhibits high accuracy in the environments that a portable PC encounters. You should also select R_4 and R_7 with thermal performance in mind. A 0.1% tolerance, 25-ppm/°C metal-film resistor is a good choice. If you intend to use the circuit in a temperature-controlled lab, then you can use less expensive components. RT_1 operates in a zero-power resistance mode, in which self-heating errors are negligible. RT_1 and R_7 form a voltage divider that only slightly linearizes the exponential equation of the NTC thermistor's negative-resistance-versus-temperature relationship: $R_T=R_{T0}\exp[(T_0-T)/(T\times T_0)]$. The software performs further curve fitting.

IC_3 and IC_4 (the ADC block) perform the voltage-measurement function. IC_4, a rail-to-rail op amp, buffers the R_6-C_3 lowpass filter. The serial output of IC_3 (D0) connects to the parallel port at S3. The converted (8 bits) voltage representing the temperature data, sampled from the divider voltage, goes to the parallel port. C0 of the parallel port controls the timing of IC_3's clock input. C1 of the parallel port controls IC_3's CS input; a negative-going front starts the conversion. Resistors R_1, R_2, and R_3 help provide the logic interface between IC_3 and the parallel port. Pulling the thermistor connections either above the PC's 5V supply level or below ground could result in damage to the circuit, the PC, or both. R_4 and R_6 provide some protection. However, to be completely safe, you should isolate the thermistors from any external voltage potential. With no thermistor connected, the temperature reading assumes the zero-voltage temperature, which is −40°C.

IC_1 also has a manual reset that provides direct user control for external triggering. If you depress the momentary switch, S_1, and select the "Trig" button on the user form, then the circuit performs a temperature measurement. The hardware turns off when the user form clos-

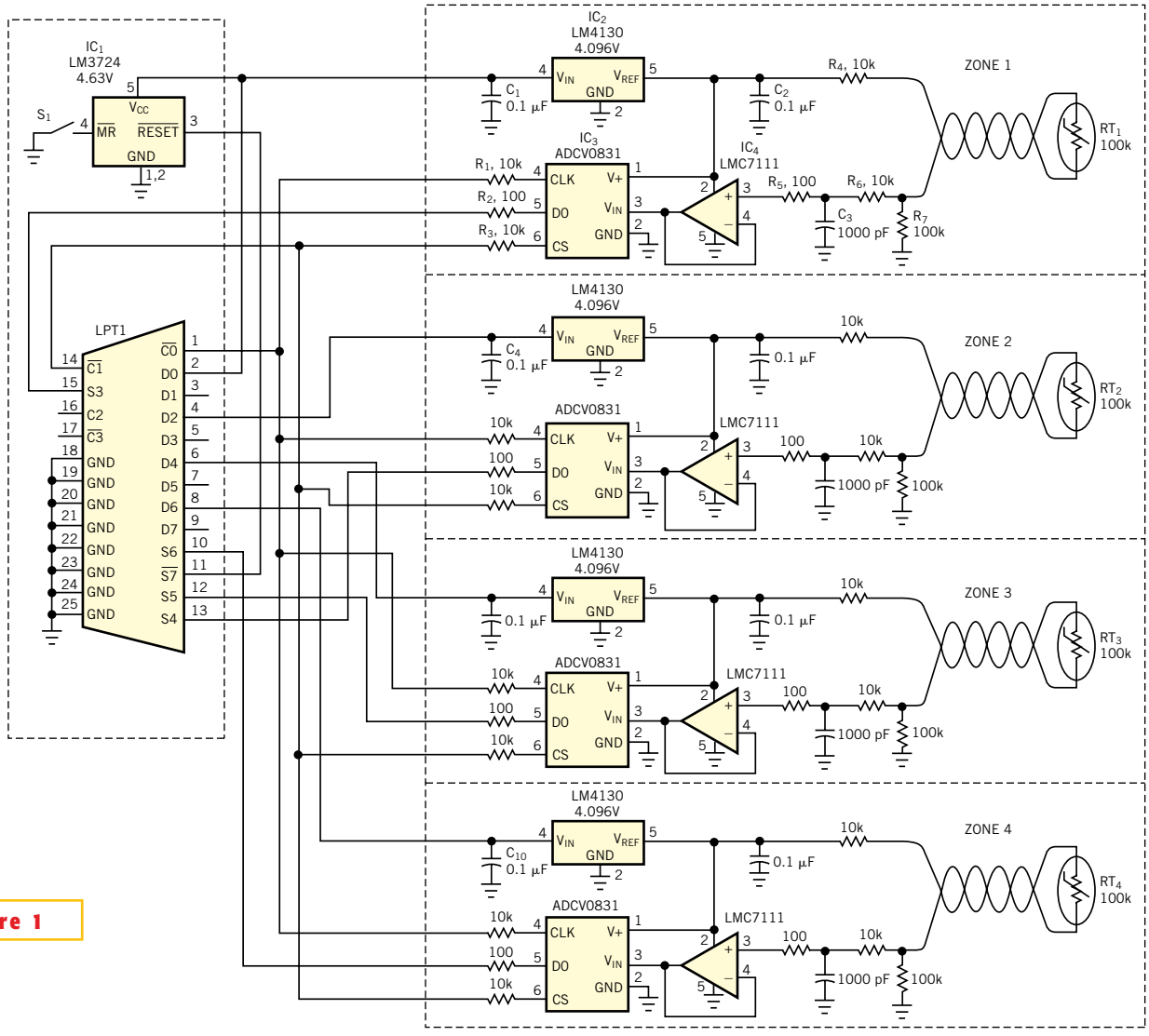

Figure 1

This PC-based thermometer derives its power from the parallel port and uses thermistors to sense four temperature zones.

es. The program control resides in Excel (running under Office 2000) macros that perform I/O through the LPT1 port of the PC. The program uses a free file "Input32.dll" to bit-wise-control the parallel port's digital I/O. The author of the .dll file is Jonathan Titus, editorial director of *Test and Measurement World*. You load QuadZone.xls with its macros, connect the circuit of **Figure 1** to the parallel port, and then run the *ControlPanel* macro. A user form (**Figure 2**) pops up, overlaying the spreadsheet, and connects temperature-measurement actions with the electronics. Your possible options using the user form are single-temperature measurement, multiple-temperature measurements separated by user-defined time intervals, linked measurements that append the data to an Excel spreadsheet, and externally triggered single-temperature measurements. You can download the spreadsheet and the .dll file from the Web version of this Design Idea at www.ednmag.com.

Figure 2 The user form, which floats in front of an Excel spreadsheet, measures the temperature of four thermistors connected to LPT1.

The user form displays a single quad-zone temperature measurement when you press the Update button on the user form. Measurement data links to the cells from columns A to G (named "data") in the spreadsheet when you press the Linked button. When you press the Loop button, the circuit samples measurement data in user-defined intervals. S_1 externally triggers measurement data if you press the Trig button. By using macros within Excel, all the graphing, analysis, and data-storage utilities common to Excel are available for familiar usage. The macros in the .xls listing contain the basic interface features for capturing the signal-conditioned thermistor-sensor signals. Within Module 1, the declaration of Input32.dll needs to include its directory path. The code for input/output of temperature data is within the user-form module.

The macros also include a software-calibration routine that steps users through a temperature-calibration sequence. With the thermistor inside a calibrated oven, you right-click on the user form to initiate calibration. The "cal" spreadsheet of **Figure 2** stores the raw calibration data. The "FitChart" chart plots this raw data and displays a fifth-order-polynomial trend-line equation. The user-form code uses the equation's coefficients to scale and display the temperatures in the user form.

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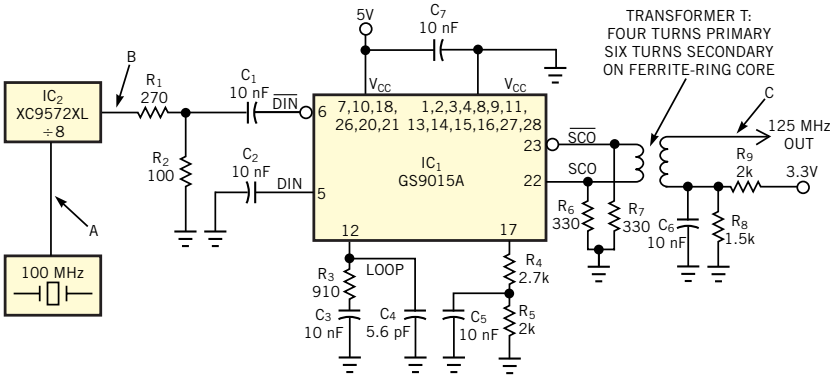
Edited by Bill Travis

Circuit allows high-speed clock multiplication

Lukasz Sliwczynski and Przemyslaw Krehlik, University of Mining and Metallurgy, Krakow, Poland

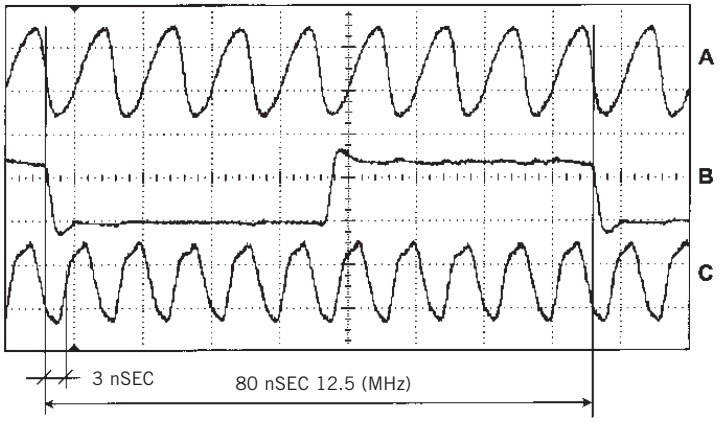
In theory, synchronous clock multiplication is an easy task. A simple PLL with two digital dividers—one inserted just after the VCO (voltage-controlled oscillator) and the second one placed directly at the input of the phase detector—may do the job. The flexibility of such a configuration allows for clock multiplication by any rational number. However, a problem emerges if you want to multiply a high-frequency clock. Standard, integrated PLLs, such as the 74HC/HCT4046 and NE564, do not accommodate such fast clock signals; they're limited to frequencies lower than approximately 60 MHz for the NE564. Although you can implement almost all PLL subcircuits by using fast programmable logic, such as CPLD or FPGA circuits from Xilinx (www.xilinx.com), a big problem exists in providing the proper high-frequency VCO. Two obvious possibilities exist: Order the VCO from a company specializing in high-frequency circuits, or build it yourself. The first approach can be costly; the second requires specialized knowledge and can be frustrating for an inexperienced designer. The circuit in **Figure 1** offers yet another possibility.

Figure 1



Using this simple circuit, you can easily and cheaply multiply high-frequency clock signals.

Figure 2



This scope photo shows some key waveforms in the circuit of Figure 1.

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The circuit is based on IC_1, Gennum Corp's (www.gennum.com) GS9015A clock-recovery IC, an ECL-based circuit that can operate at frequencies to approximately 400 MHz. You normally use such an IC to extract clock information from a digital NRZ data stream with the aid of an input divider. The clock-recovery circuitry is in principle a form of PLL with a special type of digital phase comparator. The comparator allows for VCO phase adjustment only when high-to-low or low-to-high transitions are present in the input signal. This property of the

clock-recovery circuit allows you to exploit it as a clock multiplier. If you apply a signal with 50% duty cycle instead of a normal NRZ data stream to the input of the clock-recovery circuit, the circuit attempts to interpret the signal as a sequence of N consecutive zero and one symbols and controls its VCO in such a way as to produce a clock transition for each symbol. The result is a multiplication of the input frequency by the factor 2N. You set the actual multiplication coefficient by setting the VCO's free-run frequency close to the desired output clock frequency. To avoid locking of the clock-recovery circuit to some undesired multiplication coefficient, you should make the VCO's tuning range narrow.

This design is applied to a 4B5B encoder, which needs to derive a 125-MHz clock from a 100-MHz master-clock signal; therefore, it needs a multiplication factor of 5/4. To realize this operation, you must first divide the 100-MHz clock by 8 and then multiply the result by 10. (Note that only even multiplication coefficients are possible using the concepts in this Design Idea.) **Figure 2** shows some key waveforms the circuit produces. The complete design implements the remaining part of the encoder with IC_2, a 3.3V XC9572XL CPLD IC to match logic levels. Resistor R_3 and capacitors C_3 and C_4 form the loop filter, and resistors R_4 and R_5 set the free-run frequency of the VCO. The circuit in **Figure 1** is simple and easy to build. The only trimming it requires is the initial setting of the VCO's free-run frequency (close to 125 MHz). You perform this trim by observing the output waveform with an oscilloscope and adjusting variable resistor R_5 with R_2 shorted.

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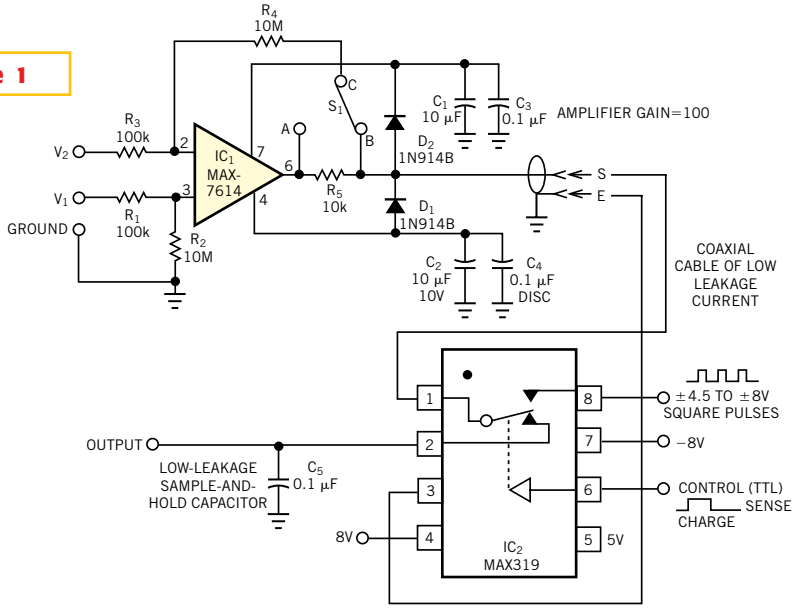
Differential amp needs no power source

Shyam Tiwari, Sensors Technology Private Ltd, Gwalior, India

A TRUE-DIFFERENTIAL, power-source-free, high-input-impedance amplifier with bipolar output would present distinct advantages in remote devices. Such an amplifier, with its bipolar output, would be a better choice than a unipolar, 4- to 20-mA device. It would also improve on common-mode performance. In **Figure 1**, a Maxim MAX319 analog switch, IC_2, feeds the power from the coaxial signal cable to the charge-holding capacitors, C_1 and C_2. The analog switch injects both positive- and negative-polarity signals into the charging circuit when its Control signal has a high (TTL) level. At the same time, the output uses a sample-and-hold capacitor to retain the last analog signal during the charging cycle. Thus, the circuit never loses the signal, as long as the charging and sensing cycles maintain timing within certain limits.

You can increase the values of C_1 and C_2 if the sensing time is considerably greater than the charging time. Switch S_1 places the feedback resistor, R_4, either in a direct connection to the sample-and-hold capacitor, C_5, or before R_5 to form an R_5-C_5 lowpass filter. In either case, R_5 is a protective resistor during the charging period, ensuring 10-kΩ load resistance for IC_1, a low-bias-current, low-power MAX7614 amplifier. This amplifier is an improved version of the ICL7611. This amplifier circuit was useful for thermocouple-signal amplification without cold-junction correction. You can also use it for bipolar, low-current signal amplification with a range of ±10 pA to ±1 nA, using only R_4 for the current-to-voltage conversion.

Figure 1



A high-impedance differential amplifier is useful in remote locations, because it requires no local power supply.

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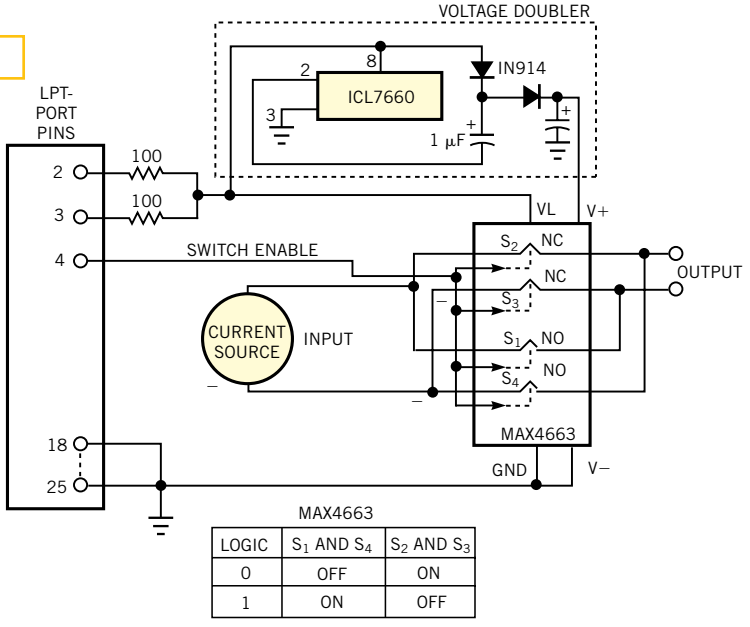
Printer port activates CMOS switches

J Jayapandian, IGCAR, Tamil Nadu, India

THE COST-EFFECTIVE design in **Figure 1** provides control for CMOS switches without the need for an external power supply. Analog switches such as those in the MAX4663 are ideal for use in low-distortion applications. They are preferable to electromechanical relays in automatic test equipment or other applications in which you need current switching. The CMOS switches use lower power, consume less board space, and are more reliable than electromechanical relays. The MAX4663 quad switch features 2.5Ω maximum on-resistance, 5-nA maximum leakage current at 85°C, and −56-dB off-state isolation at 1 MHz. They also offer break-before-make switching. The switches operate from a 4.5 to 36V supply or from dual ±4.5 to ±20V supplies.

In **Figure 1**, the switches mount in and derive power from the PC's LPT port. The design provides as much as 50 mA of current, with current-source compliance as high as 10V. The circuit uses a simple voltage-doubler circuit, the negative-voltage-converter ICL7660, for the separate V^+ supply and the V_L logic supply. The current source can supply as much as ±200 mA at 10V. **Figure 1** shows a current-reversal application in a low-temperature-resistivity experiment. The design draws only a few tens of microamperes from the PC's parallel port. The MAX4663 CMOS switches have complementary pairs (normally open and normally closed). This configuration simplifies the design, with single-enable-bit operation (the switch-enable inputs are shorted together as a single enable). You can download a LabView Virtual Instrument program from the Web version of this Design Idea at www.ednmag.com. The program latches the LPT1 port at the address 0x378 with data for forward and reverse operation of the switches. At the LPT port, the D0 and D1 bits (pins 2 and 3) power the circuit in **Figure 1**. Bit D2 (pin 4) sets the switch-enable/disable function. For data word 0x03, bit D2 is low, enabling the normally open contacts; for data word 0x07, and D2 goes high, enabling the normally closed contacts.

Figure 1



MAX4663

LOGIC	S_1 AND S_4	S_2 AND S_3
0	OFF	ON
1	ON	OFF

The LPT port powers a current-reversal circuit, using CMOS analog switches.

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Circuit improves on temperature measurement

Alexander Bell, Infosoft International Inc, Rego Park, NY

WHEN CURRENT PULSES with a stable I_{HIGH}/I_{LOW} ratio modulate a semiconductor junction, the ensuing voltage difference (for example, ΔV_{BE} for a bipolar transistor) is a linear function of the absolute (Kelvin) temperature, T. You can use this truism to make accurate temperature measurements. Technical literature has thoroughly covered the relationship (**references 1** to **4**) and has numerous implementations. This Design Idea suggests some areas for improvement and design variations on the basic idea. The principal equation describing the phenomenon is as follows: $\Delta V = 86.4 \times T \times \ln(I_{HIGH}/I_{LOW})$, expressed in microvolts. Setting the current ratio $I_{HIGH}/I_{LOW} = 10$ results in ΔV of approximately 200 µV per degree. The key issue in the practical implementation of the idea is to switch current with a highly stable I_{HIGH}/I_{LOW} ratio, which you can do by using a number of discrete components. This Design Idea suggests a digitally controlled and integrated approach (**Figure 1**).

The current switching with a stable

I_{HIGH}/I_{LOW} ratio, comes from a DAC with current outputs. The typical DAC has two current outputs—a direct I_1 and a complementary I_2. These outputs allow for simultaneous dual-channel temperature measurements. The current ratio I_{HIGH}/I_{LOW} is a function of the input digital code, D_I; you could program this code using a microcontroller. Obviously, you can use the circuit for single-channel temperature measurements, by simply ignoring the second output. If you need more than two channels, then use additional DACs or use a multiphase DAC (**Reference 5**). The circuit in **Figure 1** works as follows: The output currents, I_1 and I_2, are functions of the input digital code, D_I, and the input voltage, V_{IN}:

$I_1=(V_{IN}/R_{EQ})\times(D_I/2^N)$, and

$I_2=(V_{IN}/R_{EQ})\times(2^N-D_I)/2^N$,

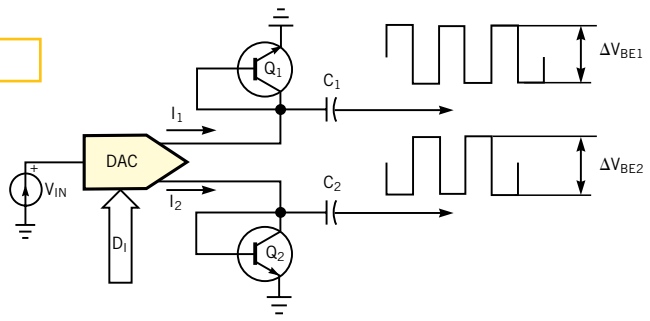
where R_{EQ} is the equivalent transfer resistance of the DAC, and D_I is the decimal equivalent of the input binary code.

The full measurement cycle consists of two phases, switching codes from D_1 to D_2. Assuming $D_1>D_2$, then the current ratio I_{HIGH}/I_{LOW} for output I_1 is equal to D_1/D_2. The current ratio for the second output I_2 is equal to $(2^N-D_2)/(2^N-D_1)$. For a 10-bit DAC (N=10), choosing $D_1=931$ and $D_2=93$, the ratio I_{HIGH}/I_{LOW} on both outputs is 10.01, which is close to the "standard" (**references 3** and **4**). For an 8-bit DAC, these numbers are $D_1=233$ and $D_2=23$, which results in a ratio $I_{HIGH}/I_{LOW}=10.13$ on both outputs. It's important that the ratio be substantially immune to variations in the input voltage, V_{IN}. Thus, any unregulated voltage source is suitable for the circuit. The source needs only short-term stability during the measurement cycle. Besides, many modern DACs integrate on-chip voltage references.

You should note that other I_{HIGH}/I_{LOW} ratios are applicable. Moreover, in general, it is unnecessary to have the same current ratios for both outputs. Thus, you could set the sensitivity to different values for the two channels. Higher ratios result in greater sensitivity, but self-heating effects impose certain limitations on I_{HIGH}, and noise levels set a lower limit on I_{LOW}. Thus, 100 and 10 µA are typical values for general-purpose bipolar transistors. As most general-purpose R-2R DACs have R_{EQ} of 10 to 100 kΩ, you should choose the proper value for V_{IN} (typically 2.5 to 10V). Alternatively, to obtain the desired I_{HIGH}, you could use an additional series resistor, R_S (not shown in **Figure 1**), connected between the voltage source and the DAC input. The R-2R ladder has an equivalent input resistance, R, which does not change with the digital code. With the additional series resistor, the equivalent transfer resistance becomes $R+R_S$. Note that this series resistor may be of almost any type, because its impact on the current ratio's accuracy is limited.

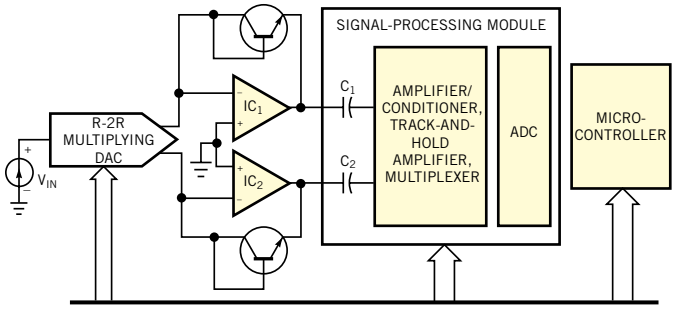
In a practical implementation, you should take into consideration the finite value of V_{BE} on the DAC's output, because its variation with temperature could affect the accuracy of the measurement. If the DAC has internal current sources, you can use the circuit of **Figure 1** as-is, because the V_{BE} has a limited effect on the current ratio. In the case of using an R-2R DAC, the circuit in **Figure 2** is more appropriate. The two op amps, IC_1 and IC_2, maintain virtual grounds on both current outputs, thus preserving the high accuracy of the current ratios. The rest of the circuit in **Figure 2** performs ΔV_{BE} measurements. You can implement that portion of the circuit by using an amplifier/conditioner, a track-and-hold amplifier, and an ADC controlled by any general-purpose microcontroller. **References 3** and **4** offer hints on implementation.

Figure 1



The DAC modulates transistors Q_1 and Q_2 with its two current outputs; ΔV_{BE} is a linear function of absolute temperature.

Figure 2



The two op amps, IC_1 and IC_2, provide virtual grounds for both current outputs of the DAC.

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3. Steele, Jerry, "Sense temperatures without Calibration, *Electronic Design*, may6 13, 1998, pg 130.
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Add voice commands to your CAD system

Alexander Bell, Infosoft International, Rego Park, NY

THE FIRST TIME I ACTIVATED the Language Bar (Speech Tools) in my Microsoft Word 2002 and started dictating this Design Idea, the on-screen title displayed "cat" instead of "CAD." By using the "Add/Delete Words" feature, I've trained the system to recognize the "CAD" acronym. This was my first experience with the MOSR (Microsoft Office Speech Recognition) tool, which is part of the latest Microsoft Office XP package. Its main operational modes are dictation and voice command. This Design Idea shows how to add a practical VCI (voice-command interface) to the simple CAD system inherent in MS Word 2002 applications. **Reference 1** described a simple version of such a CAD for schematic entry. You can download some macros from the Web version of this Design Idea from www.ednmag.com. The macros, grouped and stored in the MyCAD.dot file, extend CAD functions:

- Module "mod_View" contains macros to set the drawing environment.
- Module "mod_Symbol" contains macros to perform operations on Symbol objects.

The next level of CAD-system improvement is to add the custom VCI, enabling you to run macros via voice commands. Before use, the system prompts you to use the "Voice Training" session, which lasts approximately 15 minutes. As you read the text on the screen, the system analyzes your verbal patterns to build the Default Speech Profile. A longer session results in greater accuracy of speech recognition. The "Add/Delete Words" feature enables the MOSR engine to recognize special terms and technical jargon. Formatting the title provides a good example of practical use of the MS Word 2002 built-in Voice Commands, which correspond to its Menu and Toolbars buttons' Text. First, I selected the whole sentence by saying "select all," then I converted it to boldface by saying "Bold." Then I changed the font to Arial by saying "font," and, when the drop-down menu appeared, I pronounced "Arial."

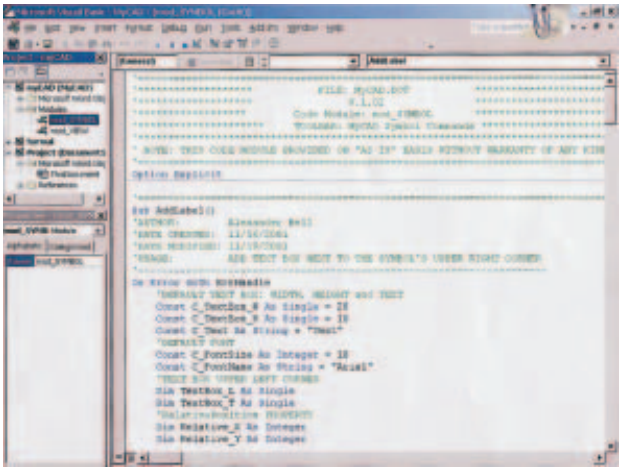

Figure 1 This Visual Basic Editor screen has the template file MyCAD.dot with two standard modules.

Finally, I set the font size to 14 points by saying "font size" and then "14," and I then underlined the title by saying "underline." You can add custom VCI by following several steps:

First, start MS Word 2002 and open a new file. Go to the Visual Basic Editor screen (shortcut: Alt+F11); add two standard modules, "mod_View" and "mod_Symbol"; and copy the macros you downloaded to the appropriate modules. The screen should look like the snapshot in **Figure 1**. From the "Debug" menu item, select "Complete Project", and then close the Visual Basic Editor window and save the file under the name "MyCAD.dot" using the "Save As" menu option. Add a custom toolbar by selecting from the menu "Tools—Customize—Toolbars—New." When a prompt appears, type the name for the new toolbar as "MyCAD Symbol Commands" and make it available to "MyCAD.dot." Add toolbar buttons related to the macros stored in MyCAD.dot. For each button, edit the button text; it defines the Custom Voice Command. The toolbars should finally look like the snapshot in **Figure 2**. Save the file and close MS Word 2002. You can consult Microsoft Office Help utility for more details on how to add custom toolbars and buttons.

Put the file MyCAD.dot into the MS Word or MS Office start-up directory. Typically, the path is "C:\Program Files\Microsoft Office\Office10\Startup." Then, start MS Word 2002, enable the macros in MyCAD.dot upon the system prompt, open a new document, and test

TABLE 1–VCI-TEST RESULTS (100 SAMPLES PER COMMAND)

	Voice commands	Correct execution	Nonrecognized	Misinterpreted
Custom commands	Grid lines	100	0	0
	Add labels	100	0	0
	Flip horizontal	100	0	0
	Increase	100	0	0
	Reduce	100	0	0
	Rotate right	99	1	0
Built-in commands: menu and toolbars-button text	File	100	0	0
	Edit	99	1	0
	View	99	1	0
	Insert	100	0	0
	Tools	100	0	0
	Help	98	2	0
	Bold	95	4	1
	Underline	100	0	0
	Cancel	100	0	0

the VCI with both built-in and custom voice commands. It's advisable to use a set of highly phonetic, distinctive words or phrases for VCI. If not, distortion and noise can lead to misinterpretation of the voice command by confusing it with another voice command. I tested the CAD with a VCI on a PC clone with a 600-MHz Athlon CPU. The system has 256 Mbytes of SDRAM-133 and runs Microsoft Office XP Professional under the Windows 2000 operating system. The voice-command execution delay is approximately 1 sec. For faster execution, you can use a faster CPU. For audio input, this design uses an inexpensive multimedia microphone. **Table 1** shows sample test results for both built-in and custom commands.

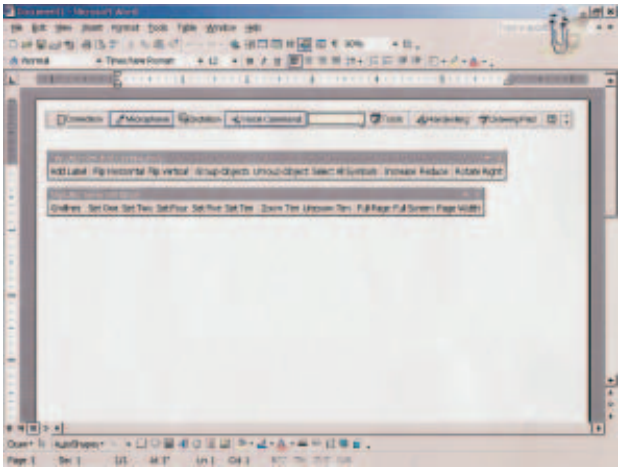

Figure 2 A Microsoft Word 2002 display has a language bar and two custom toolbars.

The accuracy increases to almost 100% for the sample set of commands when you use a Plantronics (www.plantronics.com) headset with noise-cancellation features that comes with Microsoft's SideWinder game package. For more information on natural-language input technology in Office XP, refer to Microsoft Guidelines on the Web. The Web site has a link, "Hardware Guidelines for Speech Technologies." Note that, when you enable macros in MS Word or other applications, some macros could cause harmful actions, and some may contain viruses. You use the macros at your sole risk without warranties. To use the macros in the "mod_Symbol" section, you should uncheck the box "Automatically create drawing canvas when inserting AutoShapes." Go to the tabbed Dialogue: "Tools—Options—General."

Reference

1. Bell, Alexander, "Add CAD functions to Microsoft Office," *EDN*, March 21, 2002, pg 94.

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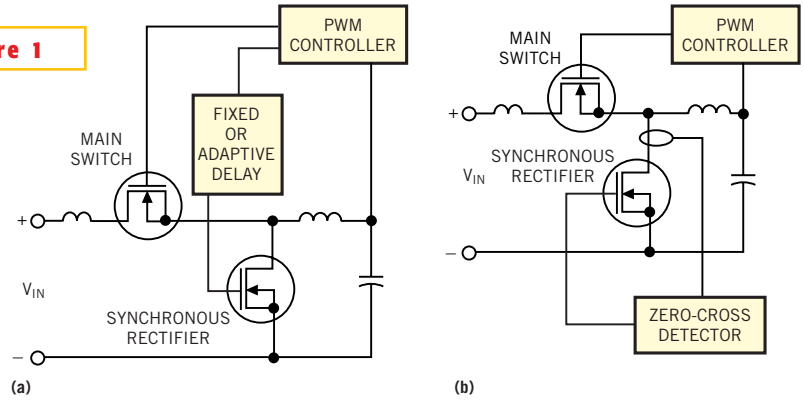
Edited by Bill Travis

Method provides self-timing for synchronous rectifiers

Giampaolo Carli, SAE Power Co, Saint-Lazare, Quebec, PQ, Canada

Synchronous rectifiers are MOSFETs, driven in such a way as to perform a rectifying function. They often take the place of diodes in the output-rectification stage of switching power converters, because of their lower on-state power loss. In power circuits, synchronous rectifiers are often complicated to use because of timing issues. Some techniques attempt to predict the correct timing by following the same drive signal that controls the main switching element of the circuit. Other techniques sense the current in the FET in various ways and then act on that information. **Figures 1a** and **1b** show simplified representations of these alternative techniques, applied to the forward/buck topology. During the off-time of the main switch, the rectifier conducts from source to drain. At the beginning of the switching cycle, the main switch turns on and begins driving current into the rectifier. Eventually, the current in the rectifier falls to zero and begins to reverse, flowing from drain to source. This instant is the optimum time to turn off the rectifier.

Figure 1



These topologies often exhibit a delayed turn-off of the synchronous rectifier, resulting in considerable reverse current. The current-reversal timing depends on loading conditions (a). The zero-cross current causes the rectifier to turn off too late (b).

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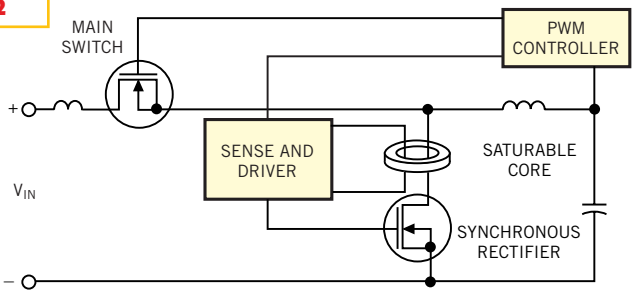
Unfortunately, if the signal from the control circuit appears at this time, the synchronous rectifier turns off only after various delays (especially, the MOSFET's turn-off delay). Because a large di/dt is involved in the turn-off, the undesirable consequence is that the rectifier turns off only when considerable reverse current is flowing. If you use the concept in **Figure 1a** with a fixed delay, the turn-off of the synchronous rectifier rarely occurs at the optimum time, because the current-reversal timing depends on loading conditions. Adaptive-delay techniques that compensate for changes in delay with load are complex. The concept in **Figure 1b** has similar complications. The zero-cross current detector is often relatively slow, so, in addition to the cited FET delays, it causes the synchronous rectifier to turn off too late. **Figure 2** shows a simple way to modify the concept in **Figure 1b**. In this case, you introduce a saturable core with an additional sense winding in the drain connection of the rectifier. With some minor additional circuitry, this single component accomplishes by itself the two main functions necessary to eliminate the turn-off-delay problem.

The first function is to determine the instant that the current falls close to zero. At that time, the core comes out of saturation and blocks voltage. This voltage also appears on the additional winding, flagging to the sense circuit that it must immediately turn off the MOSFET. The second function is to significantly slow the di/dt of the current during this crucial turn-off time. The saturable core's operation allows wider tolerances in timing and more flexibility in the design of the synchronous-rectifier driver, resulting in far fewer and less expensive components. The core can be small, even for high-power applications, and should be of nonsquare-loop ferrite material. Regular power ferrite is much less expensive and lossy than its square-loop counterparts. The nonsquare-loop material al-

lows the core to come out of saturation when the current is still slightly positive in the rectifier, thus giving a slight advance warning.

Because of the nonlinear response of the saturable core, the secondary sense winding has far fewer turns than the corresponding linear sensor in **Figure 1b** and virtually no loss in the sensing and clamping circuits for its secondary current.

Figure 2



A low-cost, saturable core in the drain circuit of the synchronous rectifier introduces a "self-timing" feature in the circuit.

These considerations improve response speed and reduce losses in the high-current outputs. Note that this simple circuit is versatile; you can apply it to various switches and rectifiers in most power-circuit topologies. The concept can even improve on well-known soft-switching techniques.

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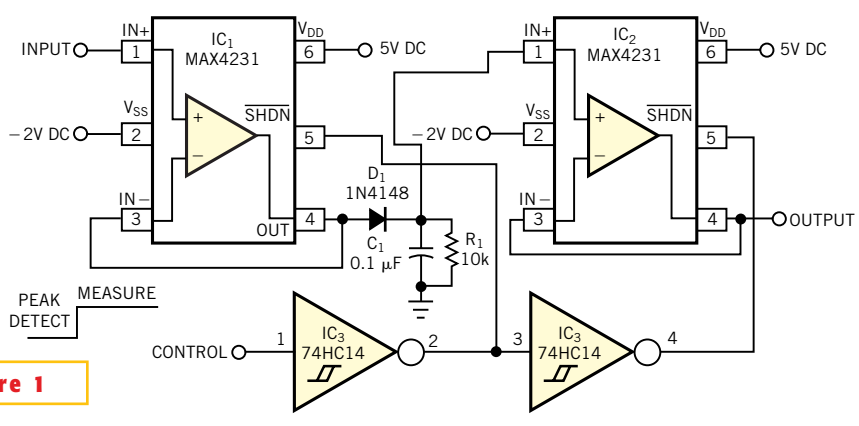
Sampling peak detector has shutdown feature

Shyam Tiwari, Sensors Technology Private Ltd, Gwalior, India

You face a serious problem in using a slow ADC with a fast peak detector. The circuit in **Figure 1** allows a slow ADC to measure a fast, sampled signal peak. The 100-MHz peak detector for ultrasonic-pulse sampling uses a fast MAX4231 amplifier from Maxim (www.maxim-ic.com). This amplifier has a shutdown feature that facilitates power savings without losing the sampled information. When the circuit samples a peak with a low-TTL-control input, the output of the peak-detector amplifier shuts off, and the output amplifier switches on to measure the output signal. This technique reduces power consumption by nearly 50%, because only one of the amplifiers is active at any given time. **Table 1** shows the circuit functions and the amplifier modes as a function of the control input's status.

Figure 1



This circuit allows you to use a slow ADC to measure fast peaks and saves power to boot.

TABLE 1–CIRCUIT FUNCTIONS AND AMPLIFIER MODES

Function	Amplifier 1	Amplifier 2	Control input
Signal-peak sampling	On	Off (shutdown)	TTL 0 (0V)
Peak measurement	Off (shutdown)	On	TTL 1 (2.4 to 5V)

The most important advantage of the circuit is that it prevents sampling of another input peak before a measurement takes place. The first peak-detector amplifier—in shutdown mode—does not permit the reading to change. This feature helps a slow ADC to monitor a high-speed sampled peak in a desired sampling interval, an impossible operation with a conventional peak-detecting circuit. You select the R_1 and C_1 values for the desired time constant to hold the peak and then let it decay according to the RC time constant. If peak decay is undesirable, then you can use a transistor switch (not shown) without R_1 to discharge the capacitor to ground before sampling a new input-signal peak.

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Circuit provides bidirectional, variable-speed motor control

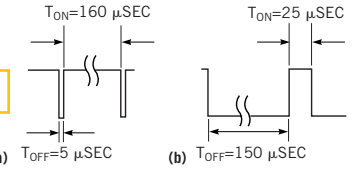
Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

DURING THE DEVELOPMENT of systems that include small motors, a simple, bidirectional motor controller with speed adjustment may be helpful. **Figure 1** shows such a controller. The circuit uses everyday components whose tolerances and ratings are unimportant as long as they sustain the required voltage, current, and power. The circuit's advantages are low cost, small size, flexibility, and ready availability. You can assemble it in less than an hour on a board measuring approximately 75×100 mm; its height is less than 12 mm. A transistor-based H-bridge allows two directions of rotation. A chopper controls the upper arms of the H-bridge, thereby enabling the speed adjustment. To start the rotation in one direction, you must connect one of the inputs (In CW or In CCW) to 0V. You can do this through switches, transistors, or open-collector TTL circuits, for example. If both inputs are high (no command), transistors Q_2 and Q_4 do not conduct, and the motor stops. The motor receives a slight braking action from the pulsing Q_1 and Q_3 transistors.

If one input is low (connected to 0V)—for example, In CW or In CCW—the corresponding transistor, Q_2 or Q_4, conducts, with base current limited by R_1 and R_4. The pulse signal to the base of Q_1 or Q_3 short-circuits to 0V, thus shutting off Q_1 or Q_3. On the opposite side, Q_4 or Q_2 does not conduct, but Q_3 or Q_1 receives pulses from the chopper through D_2 or D_1 and R_6 or R_5. Thus, Q_3 or Q_1 conducts each time transistor Q_5 is on. The chopper uses a 555 timer circuit, IC_1, connected as an astable multivibrator. The zener diode, D_7, and R_{10} limit IC_1's power-supply voltage to the maximum allowable: 15V. The timing capacitor, C_2, charges through R_{11}, the upper part of the potentiometer R_{12}, and zener diode D_7. The discharge takes place through the lower part of R_{12}. Using β for the position of R_{12}'s wiper (middle: β=0.5; down: β=0; up: β=1), the charging time is $T_{ON}=0.693C[R_{11}+R_{12}(1-\beta)]$, and the discharge time is $T_{OFF}=0.693\beta CR_{12}$.

The total time of one period of the chopper is thus $T_{ON}+T_{OFF}=0.693C[R_{11}+R_{12}(1-\beta+\beta)]=0.693C(R_{11}+R_{12})$. The output signal on Pin 3 is a square wave with nearly fixed frequency and adjustable duty cycle. In **Figure 2a**, the potentiometer's wiper is fully down (β=0). In **Figure 2b**, the wiper is fully up (β=1). Q_5 and Q_6 adapt the voltage level to drive the bases of Q_1 and Q_3, which conduct only in the time when the output (Pin 3) of the 555 is high (T_{ON}). This conduction adjusts the rotational speed. Diodes D_3 to D_6 protect the transistors Q_1 to Q_4 against inductive voltage peaks. The fuse, F_1, protects the whole circuit against overcurrent conditions. Capacitor C_3 between V_{CC} and ground acts as a kind of energy tank that filters out the current peaks. The circuit was a help in determining speeds or gear ratios to use during test and adjustment of prototypes on small machine tools. The transistors should preferably be Darlington types, adapted to the power-supply voltage and the motor current. (Don't forget the high inductance of the motor.) Select resistor R_{10} and the zener diode according to the power-supply voltage, V_{CC}.

Figure 2



The position of the wiper on the speed-control potentiometer determines the duty cycle of the chopper circuit. When it is fully down, β=0 (a); when it is fully up, β=1 (b).

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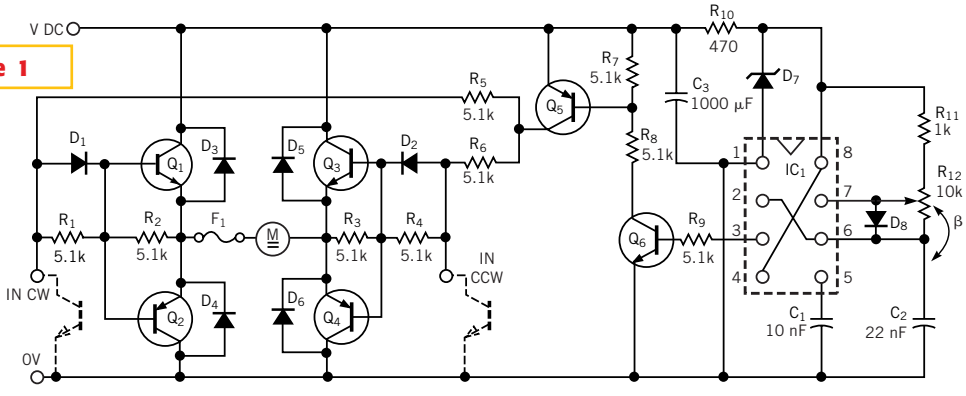
Figure 1



NOTES:
Q_1, Q_3=TIP142.
Q_2, Q_4=TIP147.
Q_5=BC161, BC556, 2N3906.
Q_6=BC160, BC546, 2N3904.
IC_1=555 TIMER.
D_3 TO D_6=BYV26E.
D_1, D_2, D_8=1N4148, 1N4007.
D_7=15V, 0.4W ZENER.

You can set a motor's rotational direction and speed using this simple circuit.

Software reset uses I²C I/O port

Bob Marshall, Philips Semiconductors, Sunnyvale, CA

You can use the circuit in **Figure 1** to allow the I²C or SMBus to control device resets in a system by using the PCA9554 I²C I/O-port IC. Normally, a reset function takes an active-low signal. On power-up of the PCA9554, the IC sets all the I/O pins as inputs. The 4.7-kΩ pull-down resistor on each I/O ensures that all the active-low reset pins are initially in a low state during power-up. You can now program the I²C controller to bring all or some of the external devices out of the reset condition. **Figure 2** shows additional details of the I/O internal structure. The PCA-9554 has four internal registers. Register 0 is the input-port register. Register 1 controls the output-port register. Register 2 is a polarity-inversion register, and Register 3 is the configuration register. All the registers, except Register 2, are initially set to all logic ones (high).

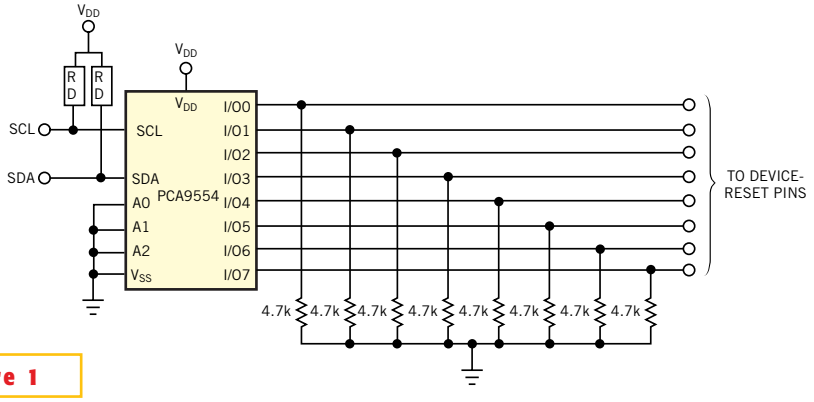


Figure 1

This circuit allows the I²C or SMBus to control device resets in a system.

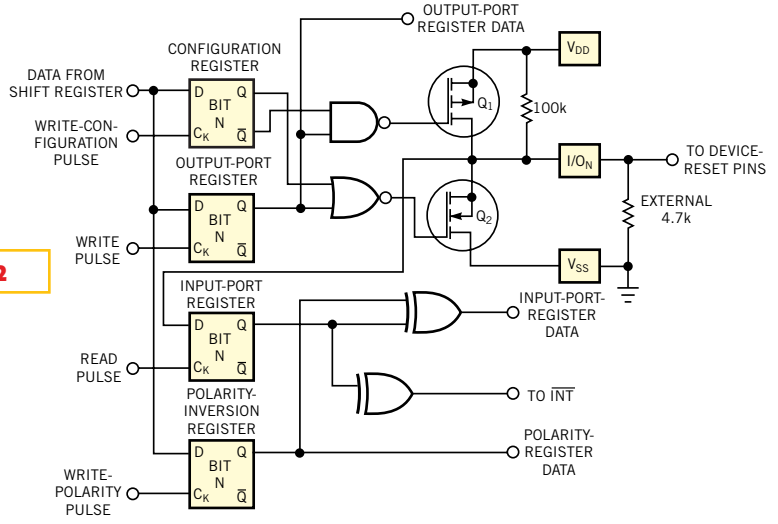


Figure 2

The details of the I/O structure of the circuit in Figure 1 show four internal registers.

When you apply power to V_{DD}, an internal power-on reset holds the PCA9554 in its initial state until V_{DD} reaches approximately 1.5V. The power-on condition sets all the I/O pins as inputs, so Q_1 and Q_2 are off. The IC has a 100-kΩ internal pull-up resistor on each I/O pin. The 4.7-kΩ external pull-down resistors hold all the attached devices in a reset state. The I²C bus can now control which devices can come out of the reset state. The I²C bus uses unique addresses for slave devices on the bus. The PCA9554 uses an address, 0100xxx R/Wn, where xxx is the level of A2, A1, and A0. To communicate with the PCA9554, the bus master must first send the device address, a command byte that addresses one of the four internal registers, and then the data. After each byte sent from the I²C master, the slave device automatically generates an acknowledge signal on the I²C bus. The master then sends the next byte. The command sequence to bring all the devices out of reset at once is:

ST: Start bit generated by the master;
40: Write to slave address (A0 to A2 are all low in this example);
03: Write the next byte to the configuration register;
00: Write 00 to the configuration register, which sets all I/O as outputs;
SP: Stop bit generated by the bus master.

The default condition of the output register is all logic ones (high). If you want to bring devices out of the reset state one at a time, simply change the pattern written in the configuration register. Any bit left at logic one in the configuration register keeps the corresponding output low (in reset). To place any device into reset, the I²C bus simply writes a logic one into the corresponding bit in the configuration register. Another feature of the PCA9554 is that it remembers the last command byte. Subsequent writes to the configuration register require only a 2-byte operation, provided that no other command register is addressed. For example, the following command sequence brings four devices out of reset (devices attached to I/O0 through I/O3) and then, on the subsequent write, brings the rest of the four devices out of reset:

ST: Start bit generated by the master;
40: Write to slave address (A0 to A2 are all low in this example);

03: Write the next byte to the configuration register;
F0: Set I/O0 through I/O3 as outputs;
SP: Stop bit generated by the master;
40: Write to slave address;
00: Set all I/O as outputs;
SP: Stop bit generated by the master.

If you want to control more than eight devices, you can use the 16-bit I/O-port PCA9555 IC. Using the A0 to A2 address pins and the PCA9555, you can control as many as 128 devices, using the I^2C bus or the SMBus. You can find additional information about the I^2C bus, including the bus specification, at www.semiconductors.philips.com/buses/i2c/support/. For information about the SMBus, you can go to www.smbus.org/specs/.

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Supply uses ac to generate 5V, power-on reset

Greg Sutterlin, Maxim Integrated Products, Sunnyvale, CA

THE NEED OFTEN ARISES for a low-cost logic supply for powering microcontrollers and related circuitry in "white-goods" products, such as industrial controllers and sensors. These applications usually include 24 or 115V ac or higher levels of ac voltage for conversion to 3.3 or 5V dc. The simplest approach to generating low-current logic-supply levels is to apply the rectified and filtered ac input to a high-input-voltage linear regulator. However, power dissipation in the regulator can be considerable, even for modest load currents. A standard shunt regulator also dissipates notable amounts of power in the limiting resistor. A switching regulator minimizes power dissipation, but that type may be impractical for cost-sensitive designs. As an alternative, consider the ac-coupled approach in **Figure 1**. The circuit suits applications in which 24V ac is available. With proper safety precautions, you can apply the circuit to double-insulated white goods and other products that require a logic supply for control or monitoring functions.

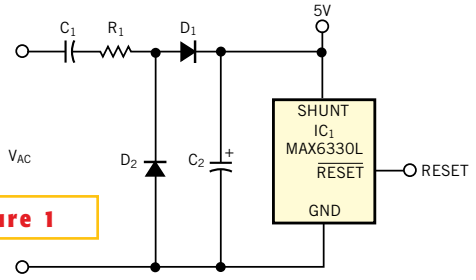

Figure 1

This SOT-23 IC with low-cost external components provides a combination of power-on reset and an efficient logic supply.

To transfer energy to the regulator with negligible power loss, the circuit uses a coupling capacitor in conjunction with an IC containing a shunt regulator and power-on-reset circuitry. Available with 50-mA maximum output-current capability in 3, 3,3, and 5V shunt-voltage versions, IC_1 also includes a power-on-reset function. Because IC_1 is an active shunt versus a passive zener diode, you must rectify the ac voltage before applying it. Typically, a capacitor follows the rectifier to hold the charge during off cycles. The design in **Figure 1** uses a simple half-wave rectifier to save cost. C_1 is the transfer capacitor, and C_2 stores energy. D_1 acts as a half-wave rectifier, and D_2 discharges the transfer capacitor during negative cycles. R_1 limits surge current during the discharge of C_1 and, if applicable, during high-voltage transient testing.

Several simplifications help to approximate the available output current. Assume 0V forward drops in the diodes and 0V shunt voltage in the IC regulator. With, for example, a 60-Hz sinusoidal input of 24V rms amplitude (V_{PEAK}= 33.94V), you calculate as follows:
Peak current in C_1 is $I_{PEAK}(C_1)= C_1(dV_S/dt)=C_1[V_{PEAK}(d\sin(\omega t)/dt)]= C_1[\omega V_{PEAK}(\cos\omega t))]=C_1\omega V_{PEAK}$.

Thus, with C_1=3 µF, ω=377.1 radians/sec, and V_{PEAK}=33.9V, I_{PEAK}=38.4 mA. The rms charge current (I_{RMS}) in C_1 is

$$I_{RMS}(C_1)= \sqrt{1/T\int_0^{T/2}\left[(C_1(\omega)V_{PEAK}\cos(\omega t))^2 dt\right]};$$

$$I_{PEAK}(C_1)= C_1(V_{PEAK})d\sin(\omega t)/dt = C_1(\omega)V_{PEAK}.$$

Thus, for T=16.7 msec, I_{RMS}=19.1 mA. By adjusting the value of C_1, you can limit peak-current levels to the value of maximum MAX6330 shunt current, 50 mA, and achieve an output of 20 mA or so. The voltage rating of C_1 must be able to withstand the maximum input voltage. Because peak currents are limited to I_{PEAK}, practically any small-signal diode can serve as the half-wave rectifier, D_1. D_2 discharges C_1 during the negative portion of the cycle. The current rating of D_2 depends on the value of V_{PEAK} and the selected value, 50Ω, of surge-limiting resistor R_1. The maximum reverse voltage on D_1 and D_2 is ($V_{SHUNT}+V_{DIODE}$). C_2 acts as a storage capacitor that maintains load current during the negative portion of the cycle. To calculate its value, use the following approximation based on the allowable level of ripple voltage (V_{RIPPLE}): $C_2=(I_{LOAD}\times T/2)/V_{RIPPLE}$. With V_{RIPPLE}= 150 mV, T/2=8.3 msec, and I_{LOAD}=10 mA, C_2=550 µF.

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More on two-transistor circuit

In a recently published Design Idea, Jim Hagerman proposes a two-transistor circuit that claims to replace the LTC4300 hot-swappable, two-wire LTC4300 bus buffer ("Two-transistor circuit replaces IC," *EDN*, Feb 7, 2002, pg 104). I feel compelled to point out that the LTC4300 offers numerous advantages over this circuit for both buffering and hot-swapping the I^2C bus.

The NPNs in Hagerman's circuit provide no capacitive buffering between the card and the backplane, which allows card capacitance to add directly to backplane capacitance. The LTC4300 isolates card capacitance from the backplane capacitance, making it possible to meet the 400-pF specification.

The LTC4300 further aids in meeting rise-time requirements by providing boost pull-up current circuits on all four SDA and SCL pins. This feature allows users to choose weaker pull-up resistors on the bus that reduce power consumption and increase noise margin while still meeting system rise-time requirements.

When hot-swapping the card, the Hagerman solution immediately connects the card bus to the backplane bus with no regard for the condition of either node. The LTC4300 monitors the backplane side for a Stop Bit or Bus Idle and the card side for logic-high states before connecting the buffers. This approach ensures that no data transaction is occurring during the instant of connection.

Although I do not doubt the attractiveness of Hagerman's idea, I felt it was important for your readers to appreciate the additional benefits of the LTC4300.

Todd Nelson
Product Marketing Manager
Mixed Signal Business Unit
Linear Technology Corp

Routine automates pattern/sequence detection

K Venkatachalam, Murugesh Rajiah, and Vijayakrishnan Rousseau, Tata Elxsi Limited, KR Puram, Bangalore, India

Sequence detection is a common operation in many communication and security systems. Some good examples are HDLC-flag identification and signature analysis. As the complexity of the system increases, designing circuitry for sequence detection becomes tedious and laborious. Using the software tool in this Design Idea, you can generate HDL code in VHDL or Verilog formats for both Mealy and Moore machines for any sequence of arbitrary length. The tool additionally presents options for inferring the sequence-detector state machine in one of the popular encoding styles, such as one-hot, binary, and Gray. Let S0 to Sn−1 be the states of a Mealy machine for n-bit sequence detection. The key to any state-machine design is to find the next state transition, which is a function of the input and the current state. Any state Sm ($0 \le m \le n-1$) indicates that the m bit of the n-bit sequence has been detected so far.

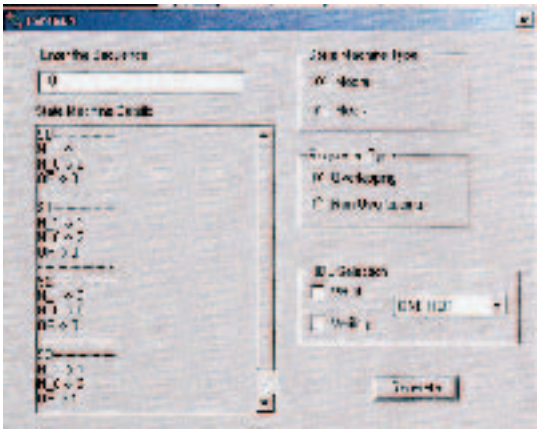

Figure 1 These are the options available for the sequence-detection method.

The state machine switches from Sm to Sm+1 on detecting an input that matches the next bit of the sequence. Otherwise, the state machine stays in the same state or switches one of the previous states. The state machine's status depends on the currently received bit and the previously received bits. If this pattern of bits matches the pattern of bits successfully detected in any of the previous states, then the state machine switches to that state. **Listing 1** is the pseudocode of the algorithm for determining the next state transition from any state Sm (where m can assume values of 0 to n−1). Let the n-bit sequence be represented as an array of bits called SEQ. The index of the array ranges from 0 to n−1. In the pseudocode, the state machine generally switches from Sm to Sm+1 on detecting an input that matches the next bit in the sequence. But this is not the case for the last state. For nonoverlapping sequence detection, the state machine switches from the last state to the initial state (S0) upon detecting the last bit of the sequence. On the other hand, for an overlapping sequence detection, the state machine either stays in the last state or switches to one of the previous states upon detecting the last bit of the sequence. The routine determines the state-machine behavior in the same way as it determines the next state transition for an input that doesn't match the next bit of the sequence. Refer to the "while" loop of the "if" and "else" blocks of the pseudocode.

For both overlapping and nonoverlapping sequence detection, the output switches high from the last state when the

method detects the last bit of the sequence. You could generate a Moore machine by following the same concepts. The only difference would be that the number of states is one more than that of a Mealy machine. Moreover, the output depends only on the states and not on the input, and it goes high only in the last state where the sequence has been successfully detected. This tool can no doubt help a designer to focus on high-level designs, rather than intricate design details. You can extend the idea to detecting double sequences, such as start-of-frame and end-of-frame sequences, and sequences having more than one bit as inputs. You can download **Listing 1** and an executable file that creates a GUI (**Figure 1**) for the sequence detection from the Web version of this Design Idea at www.ednmag.com.

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LISTING 1—ROUTINE FOR DETECTING SEQUENCES

```
if (SEQ[m] == 1)
{
        Next state transition on input 1 = Sm+1.
        Let p = m.   //p is a variable.
        while (p! = 0)
        {
                Form a p-bit sequence comprising of the last p-1 bits received and 0.
                if(the p bit sequence obtained == the first p bits of the sequence)
                        break;
                p--;
        }
        Next state transition on input 0 = Sp.
}
else if(SEQ[m] == 0)
{
        Next state transition on input 0 = Sm+1.
        Let p = m.
        while (p! = 0)
        {
                Form a p-bit sequence comprising of the last p-1 bits received and 1.
                if(the p bit sequence obtained == the first p bits of the sequence)
                        break;
                p--;
        }
        Next state transition on input 1 = Sp.
}
```

Edited by Bill Travis

Digital potentiometer programs and stabilizes voltage reference

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

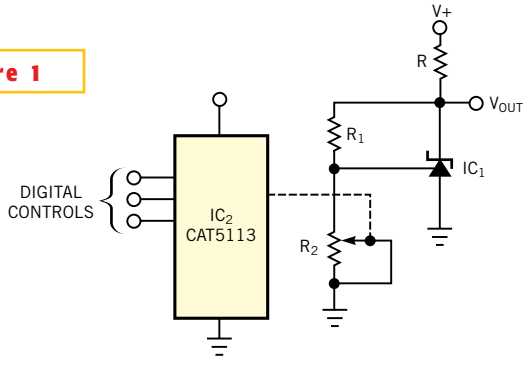
The potentiometer portion of a mixed-signal, digitally programmable potentiometer adds variability to an analog circuit, and its digital controls provide programmability. You can use a digital potentiometer in two ways in an analog circuit. You can use it as a two-terminal variable resistance, or rheostat, or as a three-terminal resistive divider. Although both ways bring variability to the analog circuit, the three-terminal implementation usually brings other important characteristics as well. For example, a programmable voltage reference has two implementations. The circuit in **Figure 1** is a voltage reference whose output, V_{OUT}, depends on the 1.25V reference of the shunt regulator, IC_1, R_1, and the programmable resistance $R_2=pR_{POT}$. The value of p varies from 0 to 1; it represents the proportional setting of the wiper from one end, 0, to the other, 1. For this circuit, $V_{OUT}=1.25V(1+pR_{POT}/R_1)$. As p varies from 0 to 1, V_{OUT} varies from 1.25V to some maximum value established by R_1 and the potentiometer's end-to-end resistance, R_{POT}. The temperature coefficient of V_{OUT} is proportional to those of the LM4041CIZ regulator's 1.25V reference, R_1, and R_{POT}. The temperature coefficient of the reference voltage and a quality resistor are lower than 100 ppm/°C. However, the temperature coefficient of R_{POT} is not guaranteed and can run in the hundreds of parts per million per degrees Celsius. Thus, the temperature stability of R_{POT} has adverse effects on the temperature coefficient of V_{OUT}. The programmable voltage-reference circuit in **Figure 2** uses the potentiometer as a three-terminal device. For this circuit,

$$V_{OUT}=1.25V\left\{1+\frac{pR_{POT}}{(1-p)R_{POT}}\right\}$$

$$=1.25V\left(\frac{1}{1-p}\right).$$

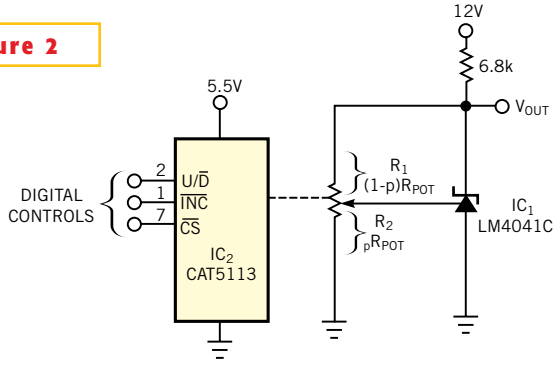
This implementation shifts the temperature dependence of V_{OUT} on the potentiometer from the high temperature coefficient of R_{POT} to the potentiometer's low ratiometric temperature coefficient of 20 ppm/°C. It also reduces component count and cost and increases programming accuracy. The 15% accuracy of R_{POT} is the dominant factor in the accuracy of V_{OUT} in the circuit of **Figure 1**. In the circuit of **Figure 2**, the potentiometer's 1% linearity is the dominant factor in the accuracy of V_{OUT}. For the values shown in **Figure 2**, the 100-tap CAT5113 digitally programmable potentiometer provides for a variable, temperature-stable V_{OUT} of 1.25 to 5.5V ($0\le p\le 0.77$). The measured data correlates to better than 1% with the calculated values.

Figure 1



In this circuit, the potentiometer's temperature coefficient adversely affects that of V_{OUT}.

Figure 2



This circuit has low component count, low temperature coefficient, and enhanced programming accuracy.

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Add voice command to virtual instrumentation

Alexander Bell, Infosoft International Inc, Rego Park, NY

Debates still persist in the engineering community about the relative merits of analog and digital controls of instrumentation. Meanwhile, a revolutionary new type of control—voice-command control—is gaining acceptance in many application areas (**Reference 1**). This Design Idea focuses on the practical implementation of the Voice Commander voice-command interface in a virtual-instrumentation project. The beauty of the method lies in the fact that a single Microsoft Excel file, vScope VC.xls, encapsulates the entire voice-command system. The Excel file comprises two worksheets, vScope and vScopeData; two standard code modules; and a small portion of code in the This Workbook code module. You can download the relevant software from the Web version of this Design Idea at www.ednmag.com. Using the terminology and the concept of modern multitiered software architecture, the voice-command method embraces the user-interface and the business-logic layers.

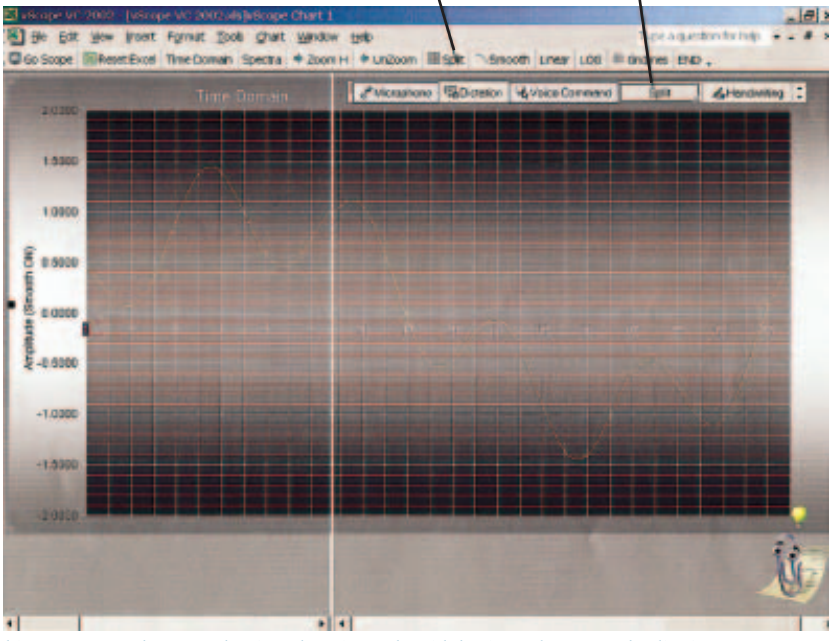
The simulated-data layer is in the vScopeData worksheet. Column A contains the samples' ordinal numbers (i=1, 2, ...64), Column B contains simulated signal-amplitude samples (V=sin(6.28×2×i/64)+0.5cos(6.28×10×i/64)), and columns C and D contain calculated complex-FFT and signal-amplitude spectra, respectively. By adding the actual data source (signal samples captured by a data-acquisition board or database query for historical data analysis) and linking it to Column B, you can expand the technique to a "full-flavored" virtual instrument or analytical tool with voice-command interface.

The vScope worksheet contains the Chart Object (called "Chart1" in the downloadable macros), formatted to emulate the actual oscilloscope screen (**Figure 1**). A custom toolbar appears at the top of the display, which contains control buttons. The buttons are associated with macros that execute when you press the button or say the com-

Figure 1

LANGUAGE TOOLBAR IN MS EXCEL 2002 IS SHOWN IN A VOICE-COMMAND MODE. (THE USER ENTERED THE "SPLIT" CUSTOM COMMAND.)

TEMPORARY CUSTOM TOOLBAR IS DYNAMICALLY CREATED ON THE FILE_OPEN EVENT.



This screen snapshot uses the time-domain mode with horizontal zoom and split-view on to see signal details at the beginning and end of the scale.

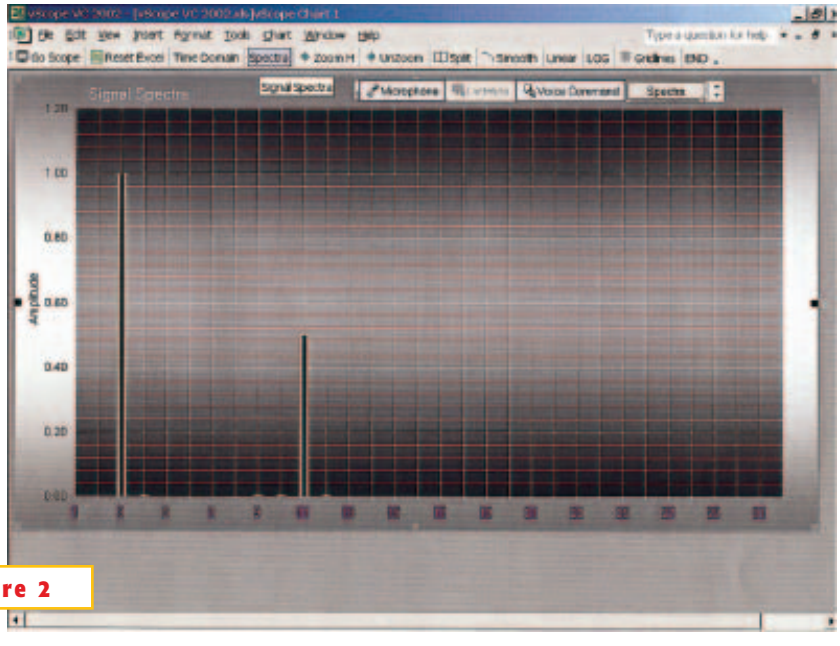


Figure 2

These signal-amplitude spectra correspond to a 64-point FFT with 32 spectral components.

mand, corresponding with button's caption. Note that the voice-command feature is available only in the latest Excel 2002 Office application. **Table 1** shows the list of custom commands. The Chart Object dynamically links via macros to the simulated data in the vScopeData worksheet. The Business Logic portion of the routine is programmed in VBA (macros) and partially in Excel worksheet functions. It contains a 64-point FFT, based on the Excel add-in functions. To use this feature, install Analysis Tool-VBA from the Tools-Add-Ins menu item. You can expand the business-logic and user-interface layers by including different digital-filtering and windowing techniques and by adding multiple channels, for example.

TABLE 1–VOICE-COMMAND DESCRIPTIONS

Voice command	Description
Go scope	Customize screen settings to maximize viewing area
Reset Excel	Reset standard Excel screen settings
Time Domain	Time-domain mode
Spectra	Show signal-amplitude spectra
Zoom H	Zoom horizontal axis
Unzoom	Unzoom horizontal axis
Split	Toggle split-screen mode on/off
Smooth	Toggle line smoothing on/off
Linear	Use linear scale (vertical axis)
Log	Use logarithmic scale (vertical axis)
Grid lines	Turn major/minor gridlines on/off (three-state logic)
End	Close file without saving and end the vScope session

Upon opening the Demo file, a temporary custom toolbar appears at the top of the display (**Figure 1**). In Excel 2002, activate the speech tools: Go to the Tools—Speech—Speech Recognition menu item and then choose the Voice Command mode. In this mode, you can enter the command either by saying it or by clicking the button on the toolbar. For example, by clicking on or saying "go scope," you can maximize the view by temporarily removing some standard screen components. You can restore the components by clicking or by saying, "reset Excel." The Split command allows you to open two pseudowindows with independent horizontal scrolling. This feature lets you see the rising and falling edges of the long, or horizontally "zoomed," signal at the same time. When you say, "spectra," the signal-amplitude spectra screen appears (**Figure 2**). You can use this technique with Excel 95, 97, and 2000, but you must use the custom toolbar instead of voice commands. Note that when you enable macros in Excel or other applications, some macros could perform potentially dangerous and harmful actions, and some may contain viruses. The code for this Design Idea is on an as-is basis without warranty of any kind. The vScope VC.xls file is for demo purpose only, and commercial use of this file is prohibited.

REFERENCE

1. Bell, Alexander, "Add voice commands to your CAD system," *EDN*, May 2, 2002, pg 77.

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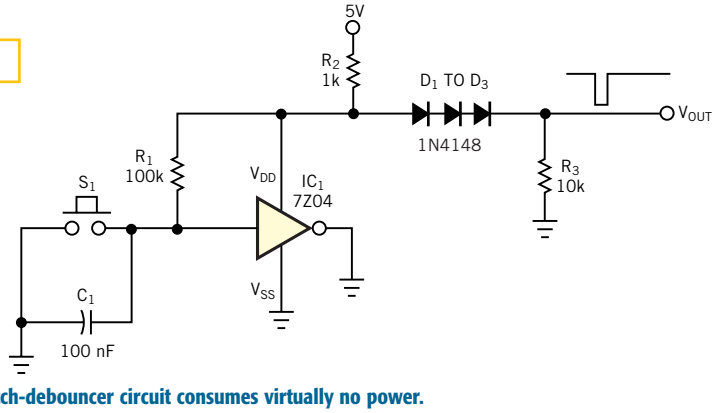
Switch debouncer uses only one gate

Steven Robertson, Anritsu Co, Morgan Hill, CA

THE CIRCUIT IN FIGURE 1 produces a single debounced pulse each time you press S_1. Moreover, the circuit uses only logic power from the remote pull-up resistor, R_2. You can use the circuit to detect when a key is pressed in a nonenergized device, such as a device in a system that's just coming up from standby. The circuit operates as follows: Assume that you have not yet pressed S_1 and that C_1 is in a charged state. Under these conditions, R_1 drives IC_1 toward V_{SS} (ground), causing the IC to consume virtually no power. This action allows V_{OUT} to remain near 5V. However, when you press S_1, C_1 rapidly discharges and drives IC_1 toward V_{DD}. Under these circumstances, IC_1 conducts heavily, pulling V_{OUT} near 0V until R_1 charges C_1 enough to again drive IC_1 toward V_{SS}. Once C_1 charges sufficiently, IC_1 goes to V_{SS} and stops drawing power. This action unloads V_{DD} and causes V_{OUT} to return to a high state. D_1 to D_3, in conjunction with R_3, shifts the level of V_{OUT} for improved compatibility with CMOS logic.

Figure 1



This switch-debouncer circuit consumes virtually no power.

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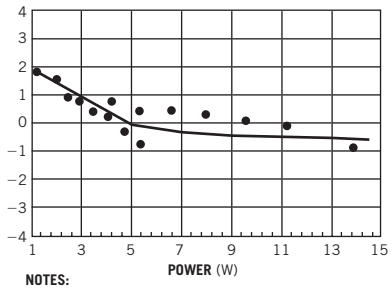
Power meter is ±1% accurate

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

Power meters provide an early warning of thermal overload by monitoring power consumption in high-reliability systems. Power monitoring is especially suitable for motor controllers, industrial heating systems, and other systems in which the load voltage and current are both variable. The power meter/controller in **Figure 1** uses the principle that power is the product of voltage and current. The typical accuracy of the circuit is better than ±1%. A current sensor, IC_2, measures output current, and a four-quadrant analog-voltage multiplier, IC_1 and IC_3, generates the product of output voltage and current. An optional unity-gain inverter, IC_4, inverts the inverted multiplier output. This power meter is most accurate for multiplier inputs (J_1 and J_2) of 3 to 15V. Select the current-sense resistor as follows: $R_{SENSE}=1/P$, where R_{SENSE} is in ohms, and P is the output power in watts. If power delivery to the load is 10W, for example, you would choose $R_{SENSE}=0.1\Omega$.

Figure 2



The measured power is better than ±1% accurate for power levels of 3 to 14W.

The circuit in **Figure 1** has a unity-gain transfer function, in which the output voltage is proportional to load power. For instance, the output voltage is 10V when the load power is 10W. To change the transfer-function gain, change the sense resistor as follows: Gain=$10R_{SENSE}$. For the circuit in **Figure 1**, **Figure 2** compares power-measurement error with load power. Note that accuracy is better than ±1% for load power of 3 to 14W. For proper operation, you must first calibrate the analog multiplier according to the following procedure. Remover jumpers J_1 (X input) and J_2 (Y input) before calibration.

- X-input offset adjustment: Connect a 1-kHz, 5V p-p sinusoidal signal to the Y input, and connect the X input to ground. Using an oscilloscope to monitor the output, adjust R_X for an ac null (zero amplitude) in the sinusoidal signal.
- Y-input offset adjustment: Connect a 1-kHz, 5V p-p sinusoidal signal to the X input, and connect the Y input to ground. Using an oscilloscope to monitor the output, adjust R_Y for an ac null (zero amplitude) in the sinusoidal signal.
- Output-offset adjustment: Connect both X and Y inputs to ground. Adjust R_{OUT} until the dc output voltage is 0V.
- Scale factor (gain): Connect both X and Y inputs to 10V dc. Adjust R_{SCALE} until the output voltage is 10V dc.
- Repeat the preceding steps as necessary.

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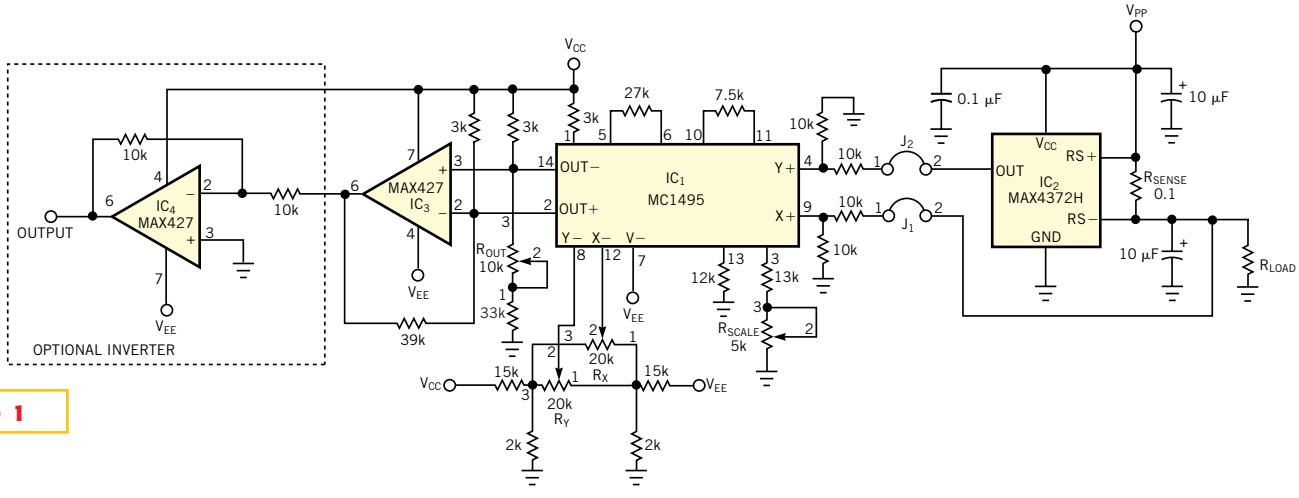
Figure 1



This power meter, whose output voltage is proportional to load power, achieves ±1% accuracy.

Circuit controls brightness of multiple displays

Stephan Goldstein, Analog Devices, Wilmington, MA

I recently needed to control nine seven-segment displays for a microcontroller's serial port. The complication I faced was the need to provide a continuous brightness adjustment for all the digits—from completely dark to fully bright. I couldn't easily use the obvious solution of a string of 74HC595 serial-to-parallel converters driving the segments through series resistors, because I would have needed a variable power supply for the displays—an inefficient and inelegant approach. I considered using software to control the duty cycle of the displays' drive signal, but as a long-time analog-circuits guy, I felt honor-bound to find a way that wouldn't require writing any more code. Besides, I'd used up all the I/O pins on my microcontroller, so a software solution would have entailed changing processors. Allegro Microsystems (www.allegromicro.com) offers several parts for driving common-anode displays. Each includes a serial-data interface and an on-chip control loop that sets equal on-currents for all the segments, using a single resistor to ground. I selected the Allegro A6275E (**Figure 1**), which neatly matches up one chip per display digit. Now, I had to simultaneously vary nine resistors.

I cheated, of course. Instead of varying the resistors, I moved their apparent ground point with a simple analog control circuit comprising a dual op amp, a power MOSFET, and a few passive components. IC_{1A} provides a buffered version of the A6275's nominal 1.23V reference voltage to the top of the potentiometer, preventing the potentiometer's loading from affecting the segment currents of the "master" A6275. IC_{1B} drives Q_1's gate and forces Q_1's drain voltage to be equal to the voltage at the potentiometer's wiper. This action varies the voltage across the 909Ω resistor between (almost) ground and the reference voltage and yields a smooth intensity control from maximum (20 mA for a 909Ω resistor) to zero. The slight variations in A6275 reference voltages and the tolerances of the 909Ω resistors add to the normal variations in intensity from digit to digit, but these variations were unnoticeable in my application.

One important point to note is the connection of IC_{1B}: The feedback from Q_1's drain goes to the IC's noninverting input. The MOSFET adds an inversion inside the main loop, so using the op amp's noninverting input as the feedback point results in overall negative feedback. C_1 and R_3 create the loop's dominant pole, and R_2 isolates Q_1's gate capacitance to ensure that IC_{1B} doesn't oscillate. Allegro cautions against excessive capacitance at the A6275's reference pin, so I used R_5 to isolate IC_{1A}'s input capacitance from this point. IC_1 must have a rail-to-rail output, its input must operate down to the negative rail, and it must operate with a total supply span of 5V. Q_1 needs to have low on-resistance with 5V gate drive. Using the STP30NE06L from ST Microelectronics (www.stmicroelectronics.com) was probably overkill at 0.045Ω, but the price was right at less than $1. The remaining components are noncritical. You may want to experiment with different potentiometer tapers; in my case, an audio taper gave a pleasing "feel" to the brightness control.

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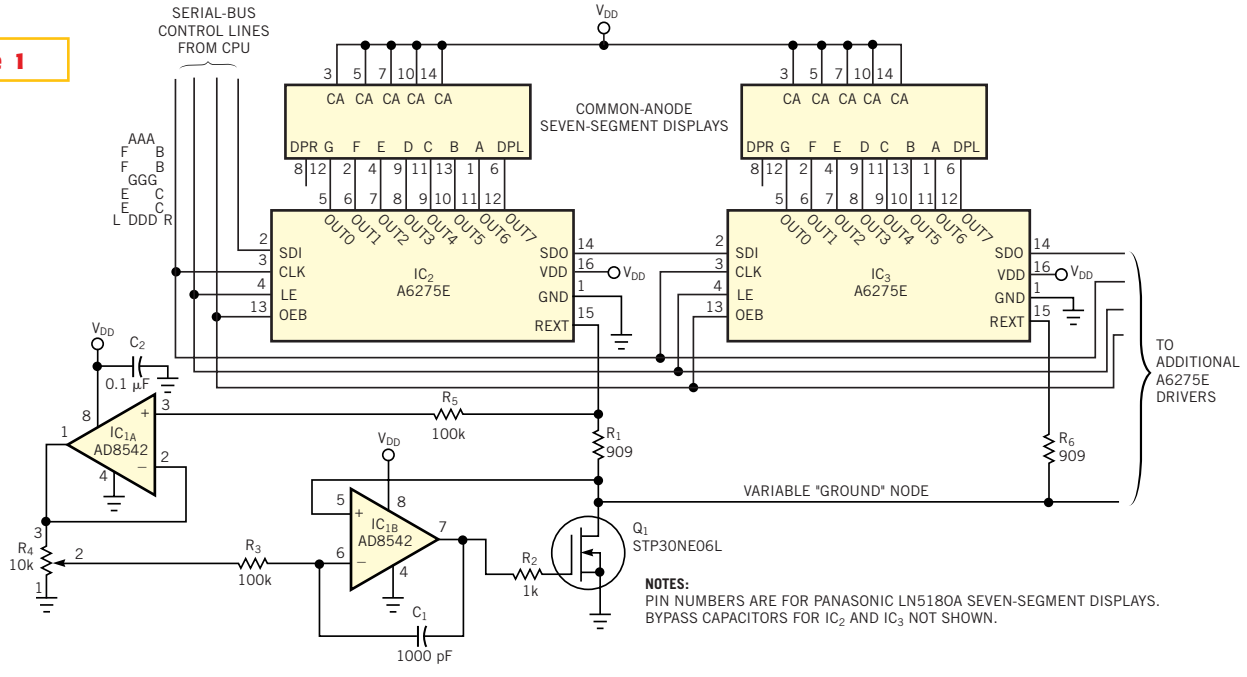
Figure 1



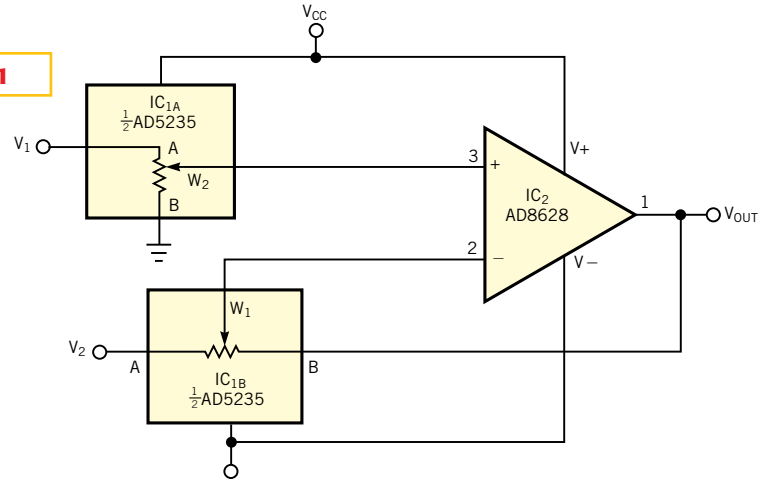
An analog control loop provides an adjustable "ground" node to control the current flowing through the resistors that set the segment currents.

Difference amplifier uses digital potentiometers

Reza Moghimi, Analog Devices, San Jose, CA

You sometimes need to measure a small signal in the presence of a large common-mode signal. Traditional instrumentation amplifiers that use two or three op amps in their internal structure find common use in these applications. The circuit in **Figure 1** presents an alternative approach that is useful when low cost and low drift are important, but when you don't need high precision. The circuit uses IC_1, a dual 1024-position AD5235 digital potentiometer with nonvolatile memory. It also uses IC_2, an AD8628 autozero amplifier to form a difference amplifier with a gain of 15. The programming capability of the AD5235 allows you to perform gain setting and trimming in a single step. Autozero amplifiers, such as the AD8628 and the AD855x family, are the best choices in these types of applications. They have high dc accuracy and add negligible errors to the output. The long-term stability of the autozero amplifiers eliminates the need for repeated calibration. With a minimum common-mode rejection ratio of 140 dB for the autozero amplifier, the resistor match is the limiting factor in most circuits. The transfer function of the circuit in **Figure 1** is:

Figure 1



A low-cost difference amplifier uses digital potentiometers to set the gain.

$$V_{OUT} = \frac{R_{W1B2}}{R_{W1A2}}\left[\frac{\left(1+\frac{R_{W1B2}}{R_{W1A2}}\right)}{\left(1+\frac{R_{W2A1}}{R_{W2B1}}\right)}V_2 - V_1\right], \quad (1)$$

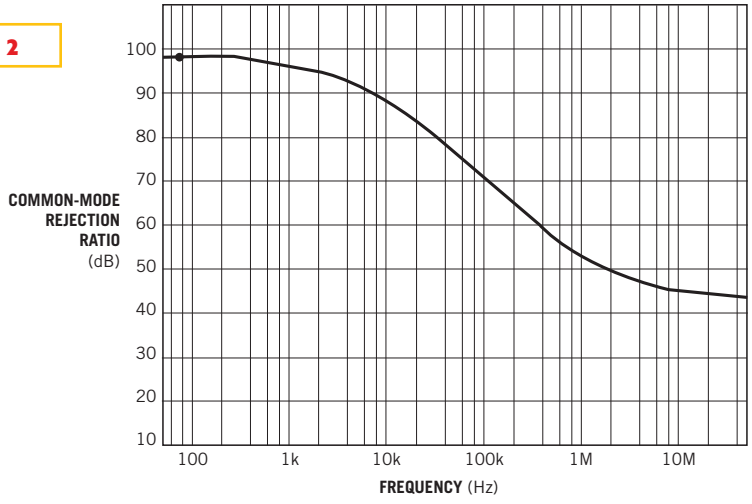
where R_{AnBn} = nominal end-to-end resistance; R_{WnBn} = terminal resistance, W to B: $R_{WB} = R_{AB} \times D/2^N$; R_{WnAn} = terminal resistance, W to A: $R_{WA} = R_{AB} - R_{WB} = R_{AB}(1 - D/2^N)$; D = decimal equivalent of the binary word; and N = number of bits.

A special situation arises when $(R_{W1B2})/(R_{W1A2}) = (R_{W2A1})/(R_{W2B1})$. The transfer-function equation reduces to

$$V_{OUT}\frac{R_{W1B2}}{R_{W1A2}}(V_2 - V_1). \quad (2)$$

You can see that the output is the difference of the two inputs times a gain factor that you can set to any desired gain, including unity. **Equation 2** holds true because the same chip integrates all the resistors; therefore, their values match tightly. The low-frequency common-mode rejection ratio is approximately 98 dB (**Figure 2**). Because of the tight matching, the circuit can achieve a temperature coefficient of 15 ppm/°C. Although the circuit has lower performance than precision instrumentation amplifiers, it is adequate for many low-cost applications.

Figure 2



A plot for common-mode rejection ratio versus frequency for the circuit in Figure 1 yields a figure of 98 dB.

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Switching regulator forms constant-current source

Stefan Strozecki, Institute of Telecommunications, Bydgoszcz, Poland

Many applications require current sources rather than voltage sources. When you need a high-current source, using a linear regulator is inadvisable, because of the high power dissipation in the series resistor. To solve the wasted-power problem, you can use a switch-mode regulator. The circuit of **Figure 1** uses IC_1, an LM2576 adjustable regulator. It needs only a few external elements and has an adjustable sensing input, which you use for controlling the output current. Resistor R_{SC} is a current sensor. IC_{2A}, one-half of a TL082 op amp, operates as a difference amplifier. When $R_1=R_2=R_3=R_4$, the output voltage is proportional to the current flowing in R_{SC}. Good common-mode rejection and a wide common-mode voltage range are important, because the amplifier works with large, changing common-mode signals.

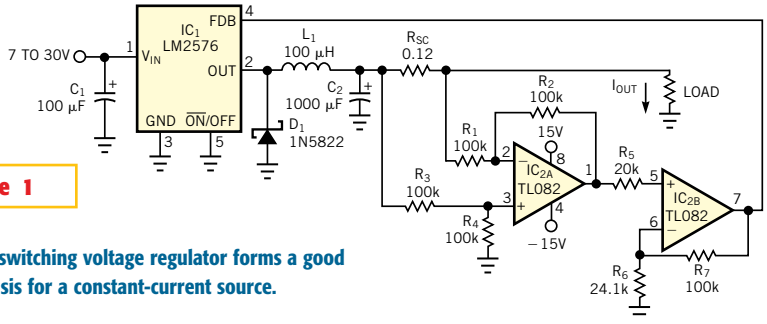

Figure 1

A switching voltage regulator forms a good basis for a constant-current source.

The second half of the TL082 op amp, IC_{2B}, operates as a noninverting amplifier. The required gain depends on the output current you need: $G=V_{REF}/V_{SC}$, where G is gain, V_{REF} is the voltage on the sensing input of the LM2576, and V_{SC} is the voltage across R_{SC}. Note that $V_{SC}=I_{OUT}R_{SC}$, where I_{OUT} is the output current. For example, if $I_{OUT}=2A$ and $R_{SC}=0.12\Omega$, then $V_{SC}=0.24V$. Typically, for the LM2576, $V_{REF}=1.237V$. So, you can obtain the gain of the noninverting amplifier from the gain equation: $G=5.15V/V$. The overall gain of the noninverting amplifier is $G=1+R_7/R_6$. If $R_7=100\ k\Omega$ and $G=5.15$, you can solve for R_6 (24.1 kΩ). When you need a precise output current, you can replace the fixed resistor, R_6,with a series connection of a fixed resistor and a potentiometer. Tests showed that the output current is practically constant with varying loads. For example, the 2A output current changed less than 1% for an output-voltage range of 0.3 to 15V.

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design ideas

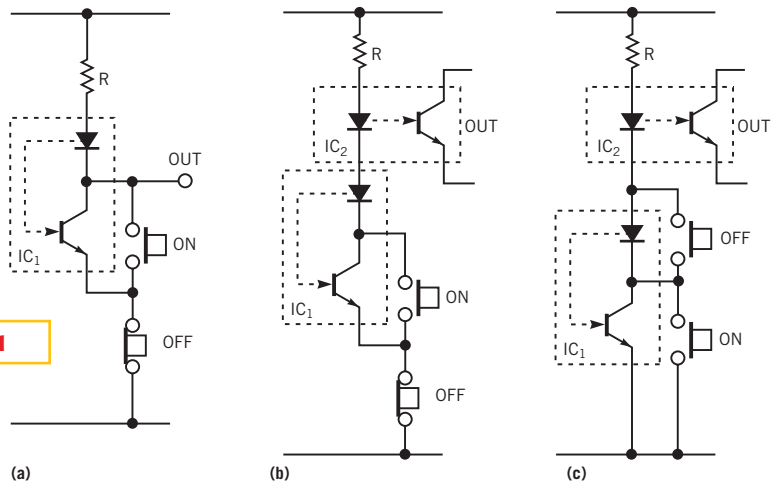
Edited by Bill Travis

Optocouplers are handy for motor drive

Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

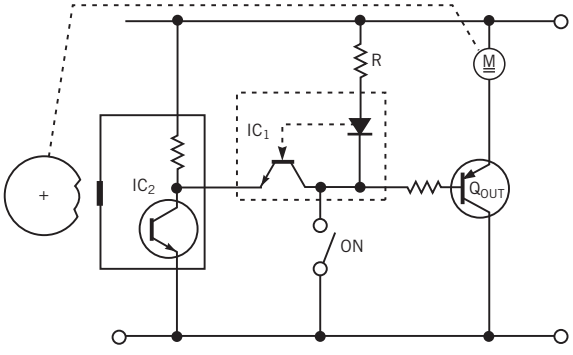
FIGURE 1A SHOWS a latching circuit based on an optocoupler, IC_1. If the off switch remains closed, pressing the on switch powers the LED in the optocoupler. Thus, the transistor in IC_1 turns on. You can now release the on switch, and the transistor remains on. You must adapt the current-limiting resistor, R, to the power-supply voltage and the optocoupler's characteristics. To turn off this latch, press the off switch, thereby cutting the current path. The output of this circuit comes directly from the collector of the transistor. If you need an isolated output, you can use the circuit in **Figure 1b**, which works similarly to the circuit in **Figure 1a**. **Figure 1c** shows a similar circuit but with an NO (normally open) switch for both the off and on switches. Shorting the LED in IC_1 turns off the transistor in IC_1. Thus, IC_2 also turns off. Note that simultaneously pressing both the off and the on buttons turns on the output. But be aware that pressing the off button reduces the voltage across the circuit below the resistor by 1 to 2V; you must consider this fact when you calculate the value of R.

Figure 1



Various optocoupler-latching circuits are suitable for motor control. In (a) and the isolated circuit (b), simply pushing the on button turns on the circuit. In (c), you push both buttons simultaneously.

Figure 2



A notched cam controls a proximity switch, which determines the motor's stop positions.

Figure 2 is a simplified schematic of an application in which a motor must always stop at a defined position. "Simplified" means that it shows only the parts needed for illustrating the optocoupler's role and omits protection, correct polarization, and a braking circuit, for example. IC_1 is the latching optocoupler. IC_2 is an npn-transistor, NO proximity switch. The proximity switch is on when metal is near its sensing area. A cam with a notch mounts on the motor axis. The motor should stop when the notch pass-

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es the sensing area of the proximity switch. Closing the on switch turns on transistor Q_{OUT}, thus allowing the motor to rotate, regardless of the status of the rest of the circuit. When you open the on switch, two things can happen:

- The notch is near the sensing area of the proximity switch. IC_1 and IC_2 are both off, so Q_{OUT} receives no base current. Therefore, the motor does not rotate.
- Metal is near the sensing area of the proximity switch, turning on the switch. The LED and, therefore, the transistor, in IC_1 are still both on. Thus, the motor continues to rotate until the notch nears the sensing area of the proximity switch. At this point, the motor ceases to rotate.

All circuits were tested using a PC814 optocoupler from Sharp (www.sharp.co.jp). (The circuit in **Figure 2** has been running for a few months on several machines.) Optocouplers, such as the 4N33, with accessible transistor bases are more difficult to use in this application. Of course, these circuits cannot replace all relays. But they are convenient and effective in applications in which the current and voltage are in the range of optocouplers. (You can add some amplification by adding some power Darlington transistors.) The main advantages of these types of circuits are that they are low-power, have no mechanical noise, have no switch bounce, cost only about 50 cents, require no critical components, and measure less than 6×10 mm.

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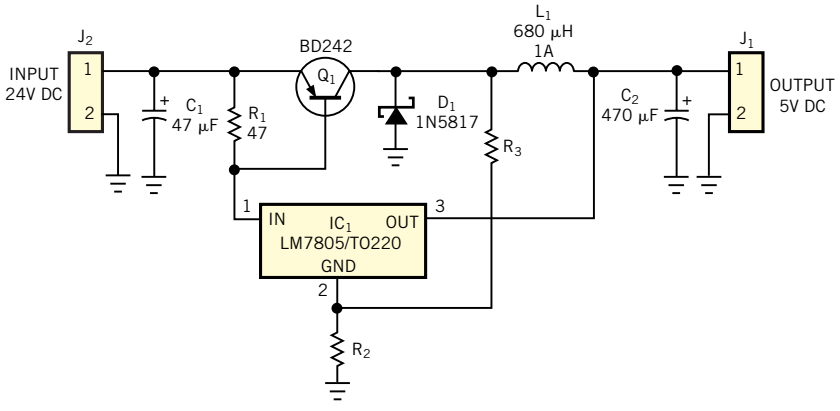
Linear regulator=low-cost dc/dc converter

Susanne Nell, Breitenfurt, Austria

THE CIRCUIT IN **Figure 1** is a good choice if you need a power supply with high efficiency and you don't want to use expensive dc/dc-converter ICs. The heart of the circuit is IC_1, the common, inexpensive LM7805 linear regulator. The external switch is a pnp transistor; the circuit can easily source more than 1A output current. As an additional feature, the switching circuit automatically turns off if the load draws no or only a few milliamperes of currents. Under these conditions, the circuit works as a normal linear regulator. When you first apply input voltage, current flows through resistor R_1 and through the LM7805 to the output. Current also flows through the emitter-base junction of Q_1 and turns on the transistor. The current through inductor L_1 now rises, and the output capacitor, C_2, charges. When the output reaches the rated output of the linear regulator (5V for the LM7805), the regulator switches off its output .

Figure 1



You can use a linear regulator in a switching circuit to configure an inexpensive dc/dc converter.

Now, transistor Q_1 switches off, because the LM7805 cuts off Q_1's base current. When the switch turns off, the voltage across the inductor changes polarity, and current flows through diode D_1. The current delivers more charge to C_2, until all the energy stored in L_1 transfers to C_2. If a load is present at the output, the load current discharges C_2. When the output voltage drops a few millivolts below the 5V output voltage of the LM7805, the LM7805 again starts sourcing current to the load. This action switches on Q_1, and the cycle starts again. Under light- or no-load conditions, all the output current flows through the LM7805, and Q_1 always stays off. You can adjust the switcher's start current by selecting the value of R_1.

You can also use this circuit for output voltages greater than 5V. You can replace the LM7805 with an LM7812 or an LM7815 to obtain 12 or 15V at the output. For these higher voltages, you should add resistors R_2 and R_3. These resistors add some hysteresis to the circuit, reducing the switching frequency. Typical values are 2.2 and 2.2 kΩ, respectively. With the circuit in **Figure 1**, you can attain efficiency approximately of 75% when you convert 24V to 12V. If you use a 5V regulator, efficiency drops to 65%, but that figure is still better than that of a pure linear regulator.

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Make eight-channel measurements through an LPT port

J Jayapandian, IGCAR, Tamil Nadu, India

THE CIRCUIT IN **Figure 1** represents a simple and cost-effective way to obtain eight-channel analog-signal acquisition through a PC's LPT port. IC_1, a 12-bit, serial-output MAX187 ADC, operates from a single 5V supply and accepts analog inputs of 0 to 5V. IC_2, an eight-channel MAX338 analog multiplexer, also operates from a single 5V supply. The circuit acquires eight analog inputs and displays eight independent digital readouts in a Microsoft Windows environment. The MAX338 connects one of eight inputs to a common output through the control of a 3-bit binary address. The design requires no external power supply; it instead derives power from the LPT port's data lines D4, D5, and D6 (pins 6 to 8 on the DB-25 connector). The low-power design consumes less than 1-mA of operating current. You derive the positive supply, V+, and the logic supply, V_L, by using IC_3, a simple, ICL7660-based voltage-doubler circuit. The ICL7660 is a negative-voltage converter. The bits D0 through D3 (pins 2 to 4 on the connector) provide the channel-selection function. The controlling software in this design uses National Instruments' (www.natinst.com) LabView Version 6.0 graphics language. The software allows for channel selection through the Data port (0x378) and collects the ADC's serial data through one of the bits in the LPT1 Status port (0x379). (The Status port uses Pin 15 on the connector, the LPT port's Error input.) You can download the LabView software from the Web version of this Design Idea at www.ednmag.com.

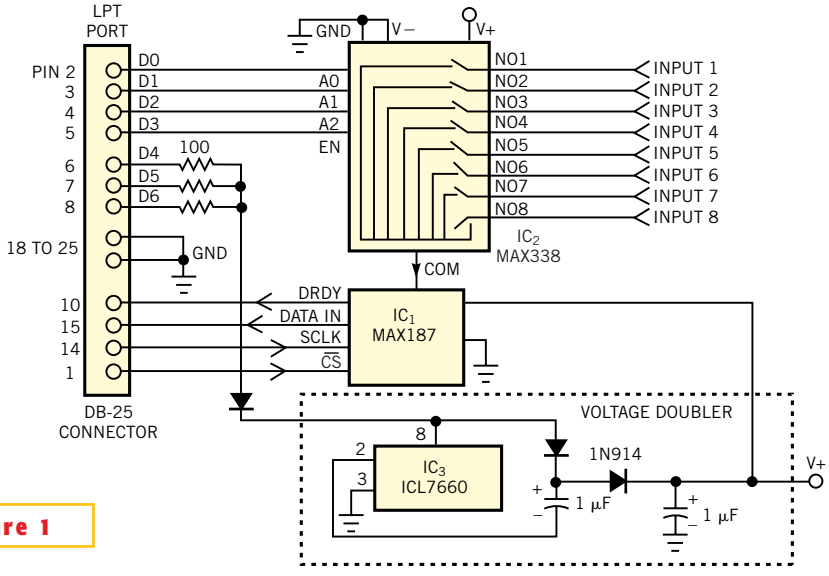
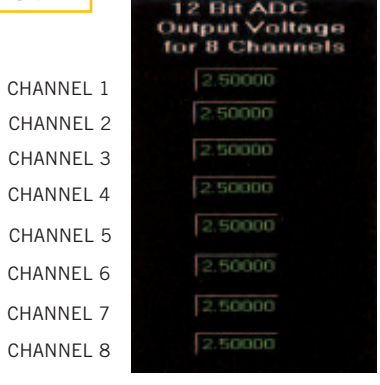


Figure 1

You can obtain eight-channel analog measurements through a PC's LPT port.

Figure 2



This front-panel view represents a LabView Virtual Instrument for an eight-channel ADC.

Once the ADC completes the conversion, its Data Ready pin switches from high to low. The DRDY output of the ADC connects to the LPT's port Pin 10 on the connector (the Acknowledge input). The controlling software senses the DRDY signal through the Status port (0x379) on Pin 10 and sets the ADC's chip-select pin $\overline{CS}$ to low, through Pin 1 (Data Strobe output) in the Control port (0x37A). The routine then receives the MSB (most-significant bit) from the ADC. After receiving the MSB, the software generates the serial-clock output (SCLK) through Pin 14 (Auto Line Feed output) in the Control port (0x37A) and then receives the remaining 11 bits from the ADC. Upon reception of all 12 bits, the $\overline{CS}$ input goes high to enable the ADC to accommodate new data in its tristate output buffer. The sequence continues, and the digital panel meter displays the acquired data. One input of the LPT port (control port 0x37A, Pin 15) acquires the serial, 12-bit data. The controlling software shifts most of the bits left, according to the bit position, and some of the bits right (because the serial data is in the fourth bit of the data in the status port (0x379)). The software sets other bits to zero.

Finally, a logical OR function of the 12 bytes/words delivers the 12-bit pattern of the acquired signal. For example, the 12th bit (MSB) appears as the first bit for transfer. This bit must be set as the 12th

position of the word; hence, the data received through the fourth bit, D3, must shift left through seven positions to be assigned as an 11th bit, and so on. In this sequence of data structuring, once the fourth bit (LSB 4) of the 12-bit pattern appears, it needs no shifting, because it is an actual D3 bit. The third bit, D2, requires shifting in the right position by one, and the D1 and D0 bits need right-shifting by two and three, respectively. This method of shifting and finally performing a logical-OR operation delivers the exact 12-bit data pattern from the serial data received through one line of the parallel port.

D0 through D3 bits in the Data port (0x378) enable the channel selection. For each channel selection, the cited sequence of acquiring the data and conditioning it provides eight independent digital readouts. The downloadable LabView Virtual Instrument program (newmulti_MAX187.vi) is a self-explanatory graphics program for the data-acquisition process. In the program, a time delay of 125 µsec between SCLK and the serial-data read sets the data-transfer rate at 4 kHz. This time delay allows the read cycle to read exactly at the midpoint of the data bit to avoid improper data reads. You can reduce the time delay for faster data acquisition. **Figure 2** shows the front-panel view of the LabView Virtual Instrument.

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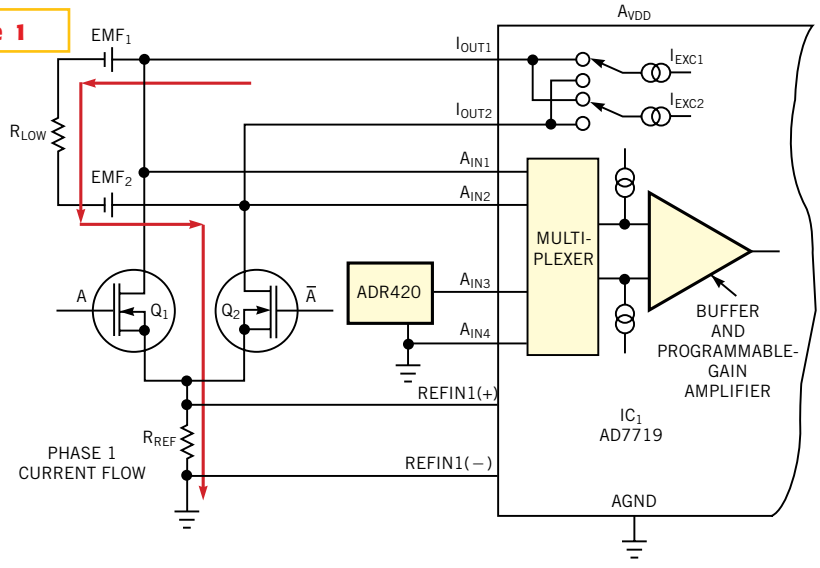
Eliminate thermoelectric EMF in low-ohm measurements

John Wynne, Analog Devices, Limerick, Ireland

When two different-metal conductors connect together in a loop and one of the junctions is at a higher temperature than the other, an electrical current flows through the loop. The magnitude of this current depends on the type of metals involved and the temperature differential of the junctions. When you open such a loop, a thermoelectric voltage appears across the open ends. Again, the phenomenon depends on the type of metals involved and the temperature differential of the junctions. The junction of the two metals forms a thermocouple, so the thermoelectric voltage is a thermocouple voltage.

When you try to measure small voltages or low impedances, thermal EMFs (electromagnetic fields) are likely to cause errors in the readings. A standard way that digital-multimeter manufacturers deal with the problem is to initially take one reading and then to reverse the excitation and take a second reading. Reversing the current excitation through a low-value resistor or thermocouple junction reverses the polarity of the desired signal but does not affect the polarity of the unwanted EMF voltages. Subsequently averaging the two readings eliminates the thermoelectric EMFs from the final result (**Reference 1**). **Figure 1** shows IC_1, an AD7719 ADC measuring a low-value resistor, R_{LOW}. The diagram also shows two thermoelectric EMFs, EMF_1 and EMF_2, representing summations of all the thermoelectric EMFs on the way from and to the ADC and the resistor. These EMFs would normally cause an error if you were to take a single measurement of R_{LOW}.

Figure 1

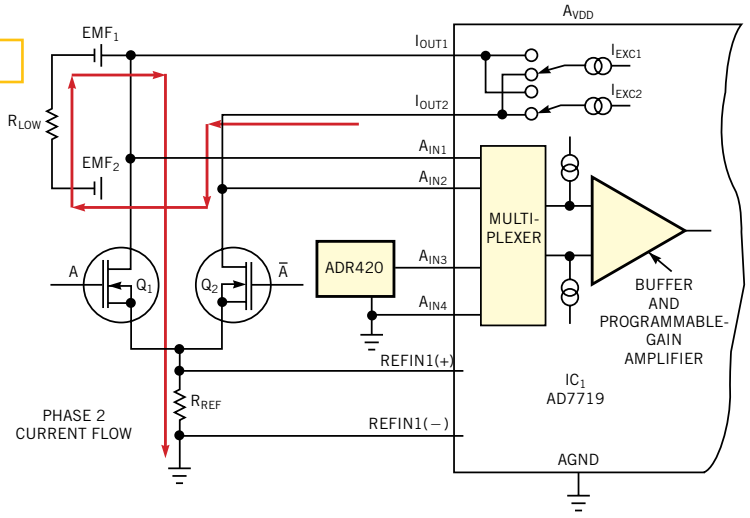


In this configuration, the excitation current flows in R_{LOW} from top to bottom.

However, you can program each of the AD7719's two current sources, I_{EXC1} and I_{EXC2}, to appear at either of the package pins, I_{OUT1} and I_{OUT2}. This feature allows you to reverse the excitation current

through the low-value resistor. You can thus take two measurements and eliminate the effects of EMF_1 and EMF_2. To increase the excitation current and thereby increase the measurement sensitivity, the two internal 200-μA excitation currents appear in parallel with each other. Thus, a single 400-μA current source makes up the excitation current, I_{EXC}, in this design. Transistors Q_1 and Q_2 steer the excitation current through the reference resistor, R_{REF}, to ensure that the same polarity reference voltage always appears, regardless of the excitation-current direction. Port pins P1 and P2 (not shown) of the AD7719 drive the transistors in antiphase mode. A value of 6.8 kΩ for R_{REF} is suitable and ensures a typical ratiometric reference voltage of 2.5V.

Figure 2



In this configuration, the excitation current reverses, and flows from the bottom of R_{LOW} to the top.

Figures 1 and **2** show the current flow in each phase of a measurement. During Phase 1, the excitation current flows out of I_{OUT1}, through R_{LOW}, and through R_{REF} via Q_2 to ground. During Phase 2, the excitation current flows from I_{OUT2}, through R_{LOW}, and through R_{REF} via Q_1 to ground. During Phase 1, $V_{DIFF(PHASE1)} = V_{AIN1} - V_{AIN2} = V_{EMF1} - V_{EMF2} + (I_{EXC})(R_{LOW})$. You now switch the current sources. During Phase 2, $V_{DIFF(PHASE2)} = V_{AIN1} - V_{AIN2} = V_{EMF1} - V_{EMF2} - (I_{EXC})(R_{LOW})$. You now combine the two measurements in software to cancel the thermoelectric EMFs: $V_{DIFF} = V_{DIFF(PHASE1)} - V_{DIFF(PHASE2)} = (I_{EXC})(R_{LOW})$.

Finally, you need to turn this ratiometric measurement into an absolute one. You achieve this result by measuring a known voltage using the "unknown" ratiometric reference voltage. Taking a reading of this known voltage but with an unknown reference allows you to infer the unknown reference value and, hence, the absolute value of V_{DIFF} on pins A_{IN1} and A_{IN2}. An absolute voltage reference, such as an ADR420, supplying 2.048V output, provides the known voltage. It connects to the second pair of differential inputs, A_{IN3} and A_{IN4}, and into the main 24-bit ADC channel.

Reference

1. *Low Level Measurements, Fifth Edition*, Keithley.

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Parallel port controls arbitrary-waveform generator

Art Kay, Texas Instruments Inc, Tucson, AZ

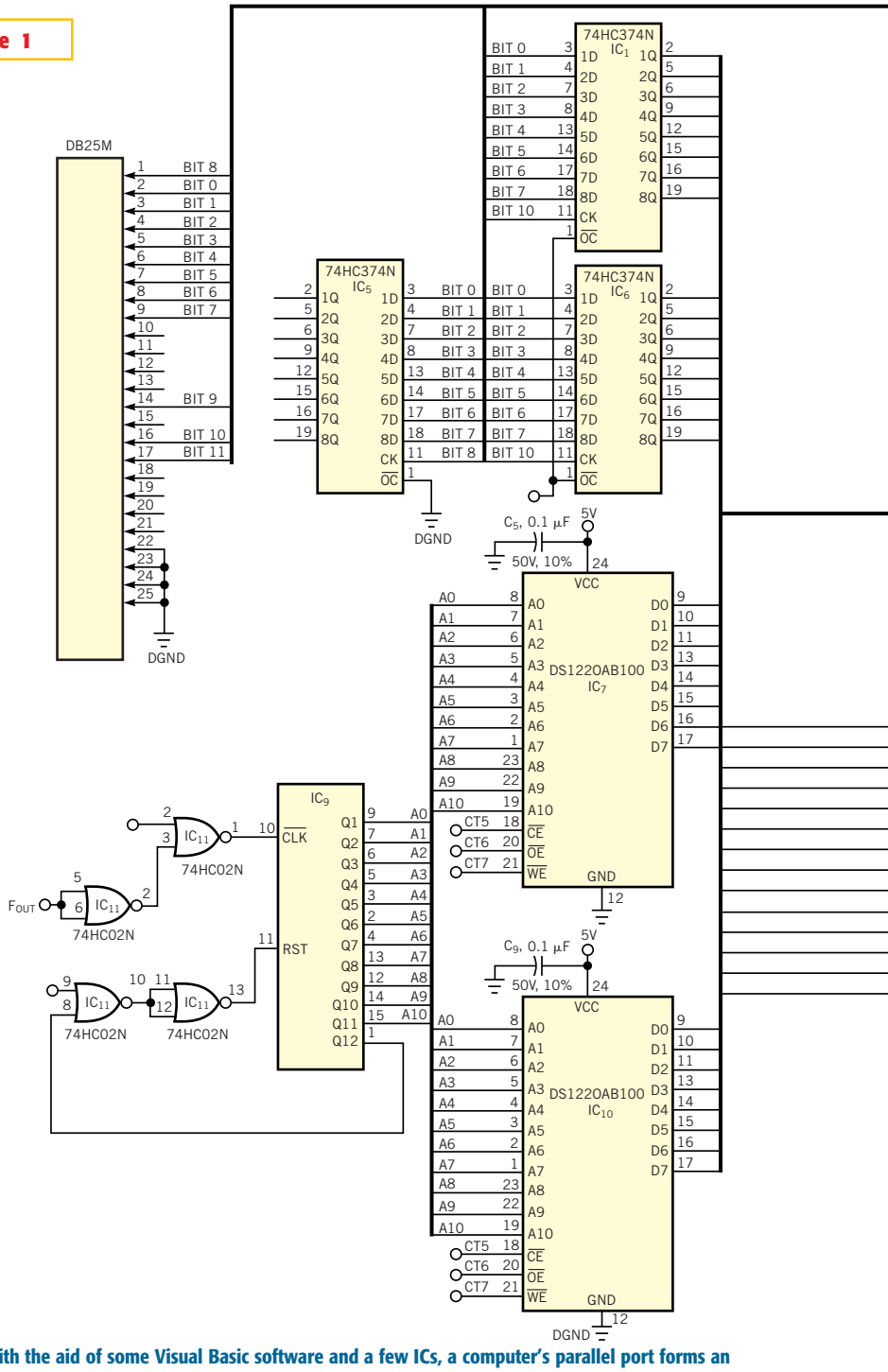
You can use the parallel port of your PC and a few additional components to generate a powerful, easy-to-use arbitrary-waveform generator. By using a Visual Basic program with the circuit in **Figure 1**, you can generate any waveform (for example, sinusoid, triangle, amplitude- or frequency-modulated, or exponential decay) by simply entering its characteristic equation. For this circuit, the parallel port connects to four latches (IC_1, IC_2, IC_5, and IC_6). IC_5 provides control signals, IC_1 and IC_6 transfer data to the memory, and IC_2 controls a VFC (voltage-to-frequency) converter. During the load-waveform operation, the waveform data transfers from the parallel port via latches IC_1 and IC_6 to the memory chips IC_7 and IC_{10}. The binary counter, IC_9, increments the memory addresses in sequence to allow loading each memory location with a unique 16-bit binary word. Each binary word corresponds to a waveform data point. During the load-waveform operation, the memory's configuration allows writing information to it (for example, ~OE=1, ~WE=0).

During the output-waveform operation, latches IC_1 and IC_6 disconnect from the bus, and the memory delivers the stored data (for example, ~OE=0, ~WE=1). For each accessed location, one of the binary words stored during the load-waveform operation transfers to IC_8, a DAC7621. This transfer causes the DAC to deliver one output point in the waveform. The VFC causes IC_9 to clock through all possible addresses. IC_{11} resets the counter when the memory sequences through all possible addresses. When IC_9 resets to zero, the waveform begins to repeat itself. Thus, each waveform comprises 2048 data points. The number of points, N, and the clock frequency, C, control the frequency of the arbitrary waveform: $f_{AWG}=1/NT_C$, where T_C is the period of the clock frequency.

IC_2, IC_3, and IC_4 form a circuit that adjusts the clock frequency, C, via the par-

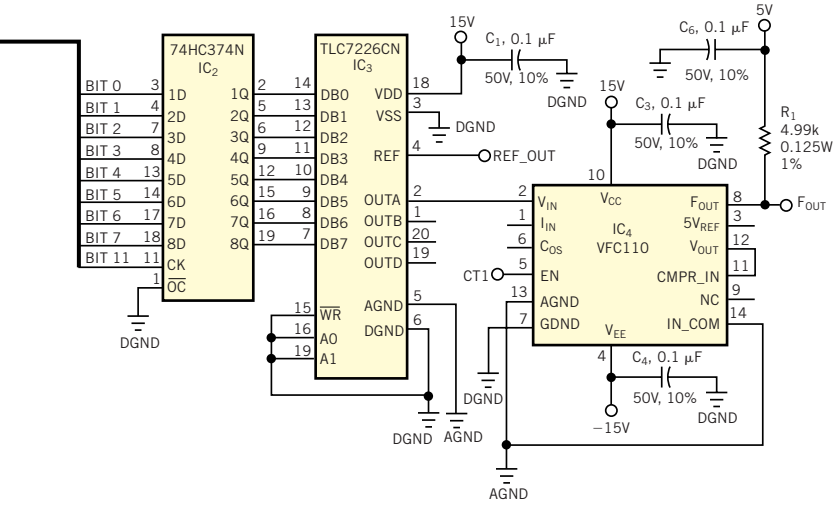
(text continued on pg 104)

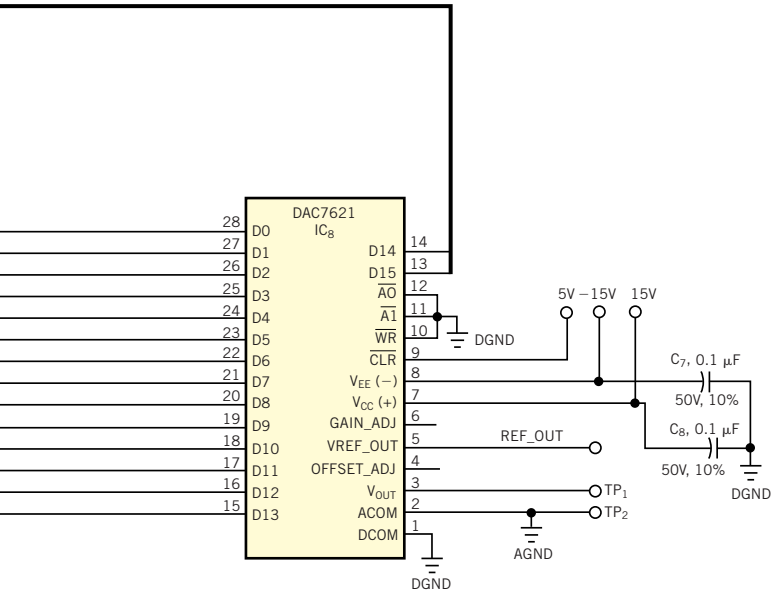
Figure 1

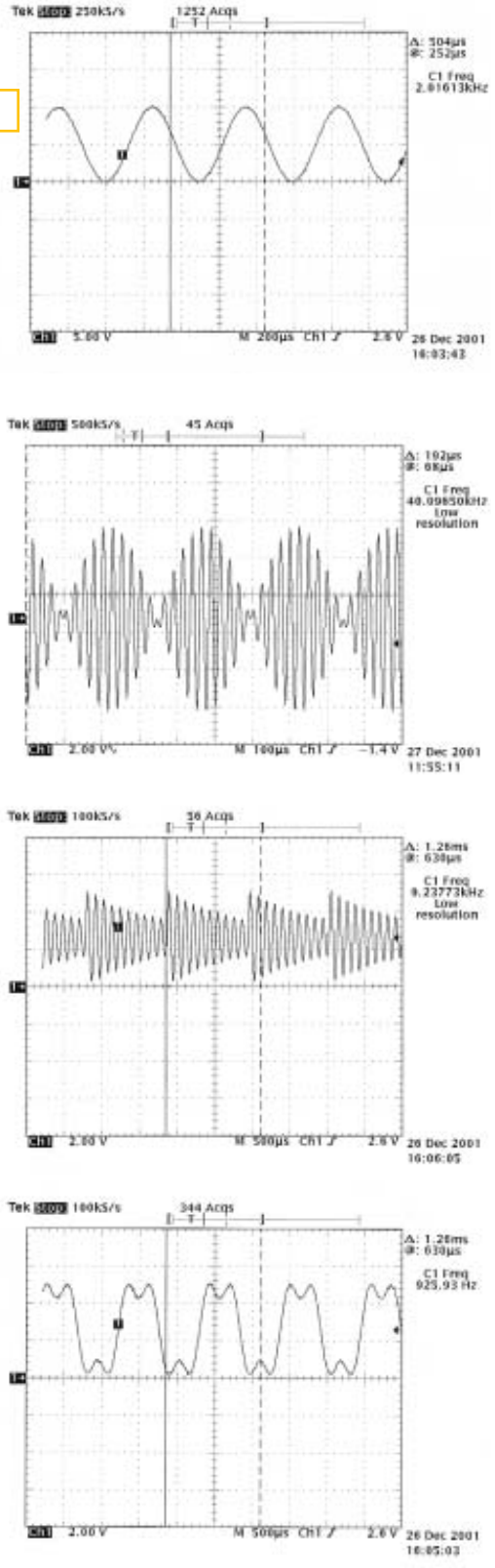


With the aid of some Visual Basic software and a few ICs, a computer's parallel port forms an effective arbitrary-waveform generator.

Figure 2







Depending on the points stored in memory, the circuit in Figure 1 can generate virtually any waveform.

allel port. The clock rate C controls the frequency of the arbitrary waveform. The output frequency of IC_4, a VFC110 VFC, is directly proportional to its input voltage. With a full-scale input of 10V, the VFC110 delivers 4 MHz. IC_3 provides a voltage output of 0 to 10V, thus providing frequency control from near 0 Hz to 4 MHz. The voltage output of IC_3 receives its programming via the parallel port, thus allowing computer control of the clock rate. Thus, the circuit provides a frequency range of 7.6 Hz (1/(2048×64 μsec)) to 125 kHz (1/(32×250 nsec)). **Figure 2** shows various sample outputs of the circuit. You can download the software files associated with this Design Idea from the Web version of the article at www.ednmag.com.

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The Wien-bridge oscillator is reborn

Michael Fisch, Agere Systems, Longmont, CO

In 1940, William Hewlett and David Packard launched a product from a garage. The product was a Wien-bridge oscillator. It consisted of a single-pole highpass filter in series with a single-pole lowpass filter. To keep the gain constant, the circuit used an incandescent pilot light to provide AGC (automatic gain control). As is true for all incandescent bulbs, the pilot light has nonlinear resistance. When you turn on the circuit, the cold lamp's resistance is low, resulting in high gain. As the gain increases, the resistance of the warming lamp increases. Thus, the lamp provides an AGC function. The circuit has been in use for more than 60 years and is still in use. The only problem with the Wien-bridge oscillator is that below unity gain it does not function. When working for a telephone company, I had to develop a 20-Hz, high-voltage sine-wave ringer circuit. The circuit had to be adjustable from 20 to 200V p-p. The most difficult part was that I had to adjust the oscillator's gain to a value below unity.

The basic oscillator had to have gain slightly greater than unity to make the positive-feedback network oscillate. It also needed an AGC loop to control the greater-than-unity gain. So, I added a third loop around the oscillator and dubbed it a voltage-controlled, regulated-output feedback circuit. The end result (**Figure 1**) is a simple push-pull circuit. By adding D_1, a zener diode, to another feedback loop, I maintained the amplitude even when I adjusted the gain to a value lower than unity. The 5.2V zener diode maintains the gain. The result is that when the gain falls below unity, the amplitude tries to decrease but cannot do so, because the zener-diode voltage pulls it back up. IC_2, the LT1056AN amplifier serves as a driver for the two LEDs, which alternately turn on and off at the frequency of the oscillator. IC_1, an LT1012AN amplifier has very low offset voltage. IC_3, a high-voltage TI/Burr-Brown (www.ti.com) amplifier, produces the final output of 20 to 200V. The final result—a major breakthrough—is a Wien-bridge sine-wave oscillator that you can adjust below unity gain, and the circuit still maintains its AGC.

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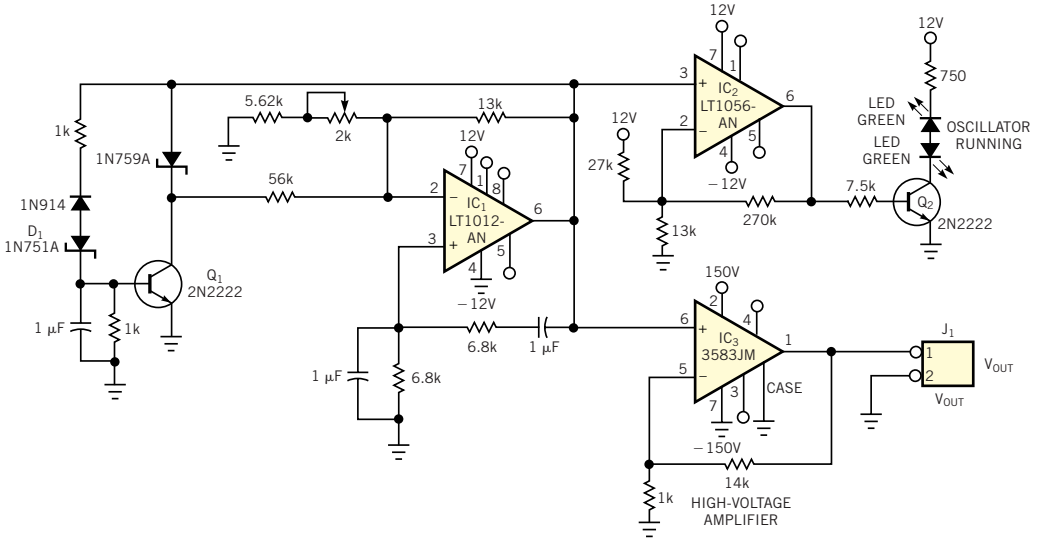
Figure 1



This Wien-bridge oscillator is, according to the author, the first oscillator that can function at gains below unity.

Optical sensor needs no tweaking

Ron Mancini, Texas Instruments, Bushnell, FL

THE TRANSFER GAIN of optical sensors spans a 16-to-1 ratio because of variations in the LED, phototransistor, ambient temperature, and optical path. The wide transfer-gain variation complicates output-resistor selection in dc-coupled circuits. You must size the output resistor to prevent high transfer gains from causing output-stage saturation, but low transfer gains yield low output-voltage swings with low-value resistors. You usually need to make adjustments to match the dc output voltage to the transfer gain, and reliable operation requires readjustment under extreme temperature and dust conditions. The circuit in **Figure 1** eliminates the need for adjustments. The circuit uses dc-coupled feedback to control the current in the output resistor. Hence, the output voltage is predictable and constant.

The op amp's input current and the current in D_3 is negligible, so $I_1=I_2$, and the output voltage is 2.7V when the phototransistor is on (light path unbroken). The output voltage is 0V when the phototransistor is off (light path broken). The op amp's output-voltage swing accommodates the variation in transfer gain. This output voltage assumes the value required to make the LED current times the transfer gain equal to the phototransistor's emitter current. The input-current equation is as follows:

$$I_1=\left(\frac{V_{CC}-V_{REF}}{R_1}\right)=\left(\frac{5-3}{20\,k\Omega}\right)=100\ \mu A.$$

The range of transfer gain is 80 to 5: $5\le I_3/I_2\le 80$. The op amp's output-voltage range is limited, especially with the high output-current requirement, thus the design uses a TLC071 that can source 20 mA at 3.5V in this design:

$$R_{3MAX}\le\left(\frac{V_{OUTMAX}-V_{D1}}{I_{3MAX}}\right)=\left(\frac{3.5-0.7}{8\,mA}\right)=350\Omega.$$

When the light is blocked, the phototransistor's emitter current goes to zero. The input current, I_1, can't flow into Q_1 because it is off, so the op amp heads for the positive rail. If the op amp's output stage saturates, the recovery time is unpredictable, so you insert the zener-diode combination D_2 and D_3 to prevent saturation. As the op amp's output voltage approaches 3.4V ($V_{D2}+V_{D3}$), the diodes clamp the output voltage, thus preventing saturation. $R_3=270\Omega$ so that it can supply adequate LED current without incurring op-amp saturation. When this circuit drives a saturated logic circuit, you should buffer the output with a hysteresis gate or a comparator with hysteresis.

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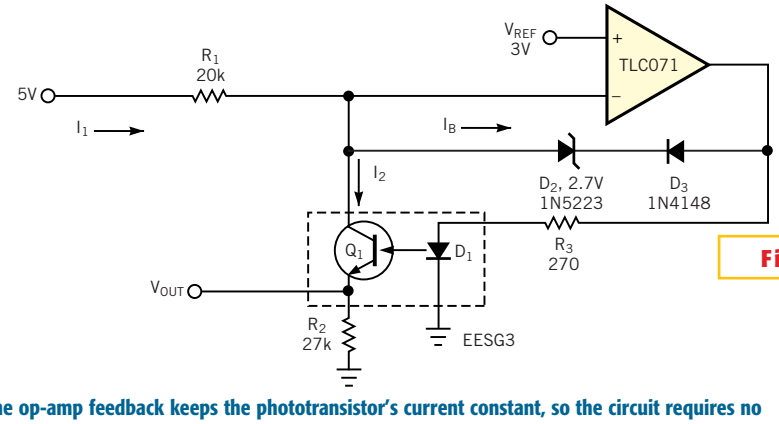


Figure 1

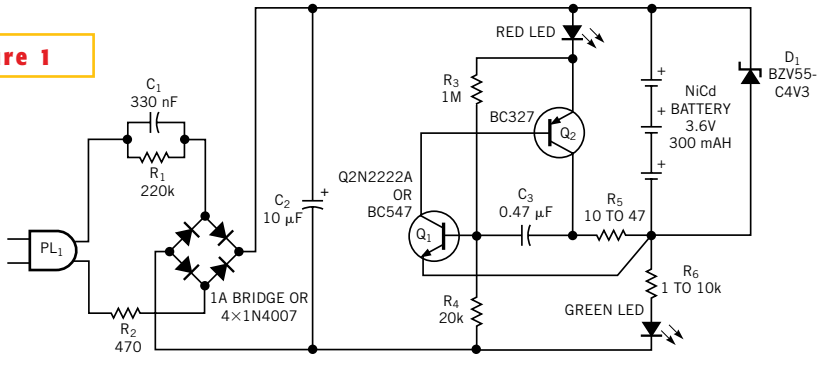
The op-amp feedback keeps the phototransistor's current constant, so the circuit requires no adjustments for transfer gain.

Power-line outage flashes red alert

Vasiliy Borodai, Zaporozhje, Ukraine

This Design Idea expands on a circuit in a previous one to configure a power-outage detector with a flashing alarm (**Figure 1**, **Reference 1**). The circuit plugs into a mains outlet and uses trickle-charged nickel-cadmium batteries. The green-LED monitors the presence of line voltage. The BZV55-C4V3 zener diode, D_1 protects the batteries against overvoltage. Voltage bias from R_6 and the green LED keeps Q_1 off, so the Q_1-Q_2 RC oscillator remains off. When a power outage occurs, capacitor C_2 discharges in approximately 2 to 3 seconds, and the dc bias disappears. Now supplied by the batteries, the RC oscillator starts, and the red LED flashes at a rate of approximately 2 Hz. R_3 and C_3 set the flashing frequency. You can use an infrared LED instead of the visible LED. The infrared LED couples with an infrared receiver to provide a convenient remote alarm.

Figure 1



A green LED indicates normal power-line voltage; a flashing red LED denotes a power outage.

Reference

1.Terrade, J M, "Free-line indicator stops interruptions," *EDN*, Dec 7, 2000, pg 187.

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design ideas

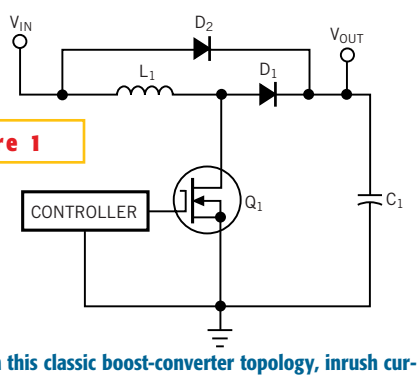
Edited by Bill Travis

Current-sensing scheme improves PFC on/off sequences

Joël Turchi, On Semiconductor, Toulouse, France

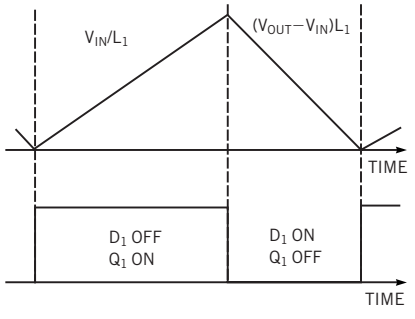
PFC (power-factor-correction) preconverters typically use the step-up, or boost, configuration, because this type of converter is relatively easy to implement (**Figure 1**). However, this topology requires the output voltage to be higher than the input voltage. When this condition is not the case—for example, with on/off sequences or under load conditions—some inrush current flows through the boost inductor and diode to abruptly charge the output capacitor. For instance, before start-up, the output capacitor discharges. When you plug in the PFC stage, the output capacitor attempts to charge resonantly to twice V_{IN}. During this sequence, the current can largely exceed the levels obtained during normal operation. Too often, these uncontrolled inrush currents make PFC-stage designers nervous during on/off reliability tests. Except for On Semiconductor's (www.onsemi.com) MC33260, which monitors the entire loop current, available controllers cannot detect this overcurrent state. These controllers may turn on the power switch while a huge and potentially destructive current flows through the inductor.

Figure 1



In this classic boost-converter topology, inrush currents can unduly stress the power-MOSFET switch.

Figure 2



Boost-converter operation occurs in two phases.

In the boost structure of **Figure 1**, the controller turns the power switch, Q_1, on and off to control the L_1 inductor current. **Figure 2** illustrates two phases:

- Switch Q_1 is on. The boost structure's input voltage (V_{IN}, the rectified ac-line voltage) appears across the inductor, L_1, which charges linearly.
- Switch Q_1 is off. The diode, D_1, turns on and drives the inductor current toward the output capacitor, C_1. The inductor current ramps down with a slope equal to $(V_{OUT}-V_{IN})/L_1$. V_{OUT} must be higher than V_{IN} to properly discharge the inductor.

If V_{IN} exceeds V_{OUT}, an inrush current flows through L_1 and D_1 and charges output capacitor C_1. Designers generally place a diode, D_2, between V_{IN} and V_{OUT}. This diode conducts a major part of the inrush current, thus improving the safety of the first power-switch turn-on. However, when the output voltage is in the neighborhood of V_{IN}, the current that ramps up during this first switch-on time generally cannot significantly decay during the off-time. As a consequence, the following turn-on operation may occur while the inductor is still charged. Moreover, if V_{OUT} needs several switching cycles to significantly charge (for example, under heavy load conditions), the power MOSFET faces a succession of stressful turn-ons that may jeopardize the circuit's reliability.

When you cannot use the MC33260, you can use the circuit in **Figure 3** to improve the reliability of the PFC stage. You can test this configuration using the MC33262. Typically, the current-sense resistor, R_1 connects between the power MOSFET's source and ground, and the

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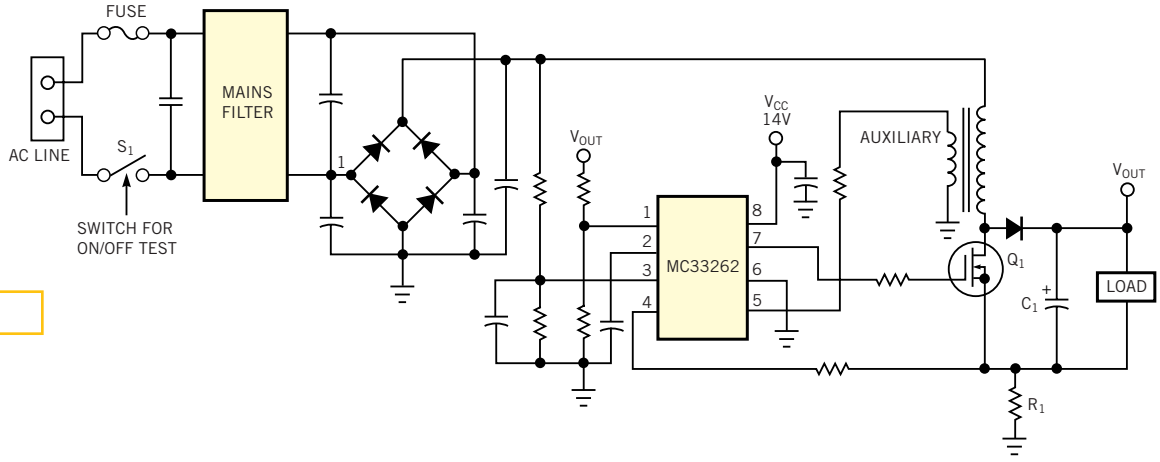

Figure 3

In this circuit, a modification in the placement of the current-sensing resistor increases the robustness of the PFC preconverter.

negative terminal of the output capacitor, C_1, connects to ground. As a result, R_1 senses only the power-switch current. In the modified circuit of **Figure 3**, the output capacitor's charging current also passes through R_1. As a result, the sense resistor senses the entire inductor current. The MC33262 keeps the power switch off as long as the sensed current is higher than the setpoint that an internal multiplier establishes. When the sensed current is below this setpoint, the MOSFET turns on upon core-reset detection. If detection is impossible, a 600-µsec watchdog timer reactivates the power switch. In the case of on/off sequences, the core-reset information is generally unavailable, and the MOSFET turns on in the following cases:

- 600 µsec after the preconverter switches on, regardless of the inductor current, in the traditional application, or
- once the coil current measures lower than setpoint in the modified application.

Figure 4 clearly shows that no switching takes place when the input current is high, as long as the current is higher than the setpoint. In **Figure 3**'s example, the situation is even better. In effect, the 600-µsec timer delays the power switch's turn-on even after the current-sensing block allows the turn-on, so the MOSFET finally switches on when the inductor current is zero. You can see that the modified application schematic increases the power dissipated in the current-sense resistor. In effect, the losses are $P_{MODIF}=1/6R_{SENSE}(I_{PKMAX})^2$, where R_{SENSE} is the current-sense resistor (R_1 in **Figure 3**), and I_{PKMAX} is the maximum inductor peak current (obtained at the top of the sinusoid). In this application, you can compute the losses using the following equation:

$$P_{TYP}=\frac{1}{6}R_{SENSE}(I_{PKMAX})^2\left(1-\frac{1.2V_{AC}}{V_{OUT}}\right), \quad (1)$$

where V_{AC} is the rms input voltage and V_{OUT} is the output voltage. The relative increase in dissipation then conforms to the following equation:

$$\frac{P_{MODIF}-P_{TYP}}{P_{TYP}}(\%)=\frac{120V_{AC}}{V_{OUT}-1.2V_{AC}}. \quad (2)$$

From **Equation 2**, you can determine that if $V_{AC}=90V$ and $V_{OUT}=400V$, the dissipation increases by 36%. If $V_{AC}=180V$ and $V_{OUT}=400V$, the dissipation increases by 117%. The simple modification of the sensing resistor's location significantly increases the robustness of the PFC preconverter during on/off tests at the price of a reasonable increase of the power dissipation in the sensing resistor.

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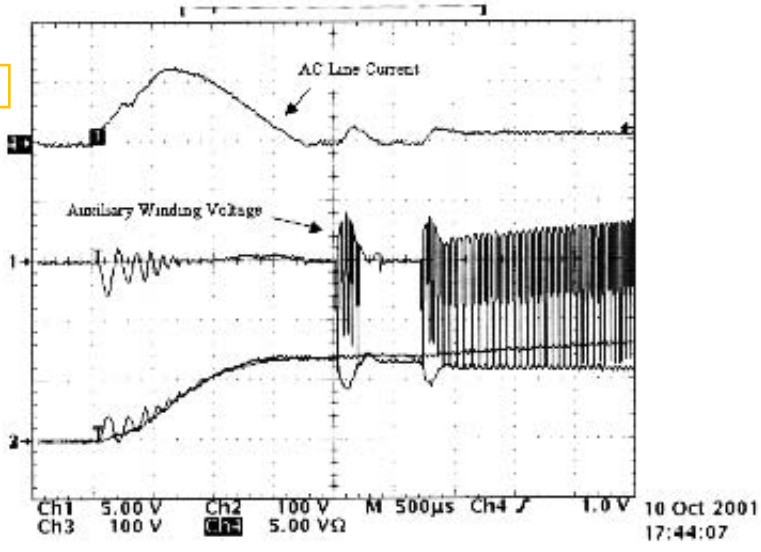
Figure 4



No switching occurs when the input current is high; a 600-µsec timer delays the power switch's turn-on.

Reset generator uses "fleapower"

Philip Simpson, Maxim Integrated Products, Reading, UK

When a processor-controlled device must operate reliably, designers often choose to periodically reset the processor rather than rely on a watchdog configuration. In low-power systems, this periodic-reset circuit can consume a large part of the system's current budget or may fail to operate at low voltages. The circuit in **Figure 1** generates a low-going reset pulse of 100-µsec duration. The circuit consumes less than 1-µA operating current and operates from 1.8 to 5V supplies with little variation in the output period. The circuit is an adaptation of a normal relaxation oscillator. The circuit has a differentiator and diode clamp on the output to generate the 100-µsec low-going pulse. You can adjust the period of the output waveform by varying R_1, C_1, or both. You can adjust the pulse width of the low-going reset pulse by varying R_P, C_P, or both, or you can change the polarity by repositioning D_1. **Figure 2a** shows the comparator's output waveform, which has a period of approximately 1.3 sec. The period varies from 1.308 sec with a 4.5V supply to 1.306 sec with a 1.8V supply. **Figure 2b** shows details of the low-going reset pulse, which takes the shape of the output of a normal relaxation oscillator. The reset pulse is 100 µsec wide at its 30% point on the exponential curve.

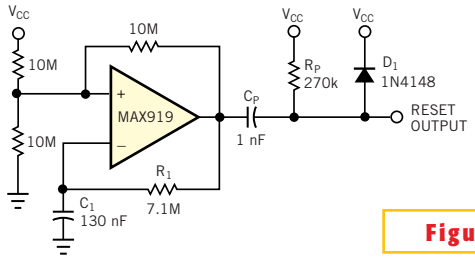


Figure 1

This reset circuit consumes less than 1 µA and delivers a 100-µsec-wide reset pulse every 1.3 sec.

The 350-nA supply current, the 1.8 to 5.5V supply range, and the SOT-23 package make the MAX919 ideal for this application. Measurements for the circuit reveal lower than 1-µA operating current. This low consumption would allow the circuit to operate from a single AA lithium cell for 250 years. With judicious component choice, the circuit can generate periods from milliseconds to minutes. To ensure good temperature stability, you should use metal-film types for R_1 and R_P and NP0 types for C_1 and C_P. Assuming a reset-logic threshold of 30% of the supply rail, you can use the following formulas to adjust the output pulse width and period: pulse width≃$0.36R_PC_P$, and period≃$.4R_1C_1$.

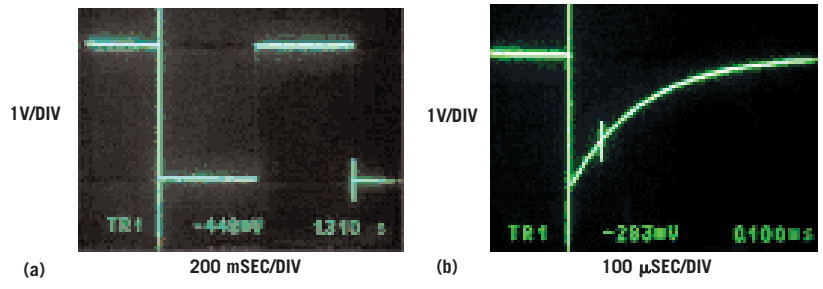


Figure 2

The comparator in Figure 1 produces a square wave with a period of 1.3 sec (a); the output differentiator yields a low-going pulse of 100-µsec width at its 30% point (b).

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Voltage-to-current converter drives white LEDs

Susanne Nell, Breitenfurt, Austria

You sometimes need to drive a white LED from one 1.5V battery. Unfortunately, the forward voltage of a white LED is 3 to 4V. So, you would need a dc/dc converter to drive the LED from one battery. Using the simple circuit in **Figure 1**, you can drive one white LED or two series-connected green LEDs, using only a few components. The circuit is a voltage-to-current converter, which converts the battery voltage to a current that passes through the LED. You can adjust this current and, thus, the brightness of the LED, by varying resistor R_3. If you turn on switch S_1, resistor R_2 feeds base current to transistor Q_2. Q_2 turns on, and its collector current, via R_3, turns on Q_1. Now, the current through inductor L_1 increases. The slope of the increase is a function of the value of L_1 and the battery voltage. The current through L_1 increases until it reaches a maximum value, which depends on the gain of Q_1. Because the value of R_3 sets the base cur-

rent drawn from Q_1, Q_1's collector current is also limited.

Once the current through L_1 reaches its maximum value, the slope of the current through L_1 changes. At that instant, the voltage on L_1 switches to a negative polarity forced by the changed slope. This negative voltage traverses capacitor C_1 and turns off Q_2, which in turn turns off Q_1. The negative voltage on L_1 increases until it reaches the forward voltage of the LED. The peak current through inductor L_1 now flows through the LED and decreases to zero. Now, Q_2 switches on again, via the current through R_2, and the cycle starts again. By adjusting resistor R_3, you can set the peak current through L_1 and the peak current through L_1 flows through the LED. Different forward voltages of the LEDs yield different on-times (duty cycles) but the same peak current through the LED. With the values shown in **Figure 1**, the circuit oscillates at a frequency of approximately 30 kHz and delivers a 20-mA peak current through the LED. The duty cycle depends on the ratio of the battery voltage to the forward voltage of the LED. One advantage of this circuit is that it requires no series-limiting resistor for the LED. The peak current through the LED is a function of the value of R_3 and the gain of Q_1.

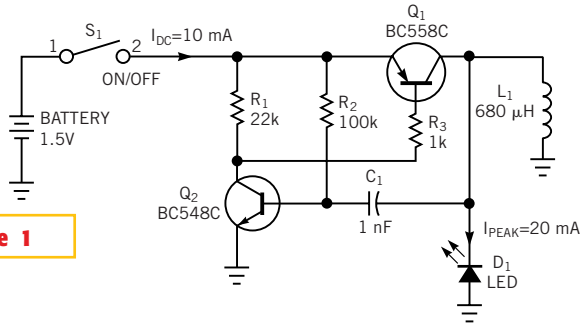

Figure 1

You can eschew expensive dc/dc converters by using this inexpensive circuit to drive a white LED from a single battery cell.

The brightness of an LED is a linear function of the current through the LED. So, adjusting the value of R_3 also adjusts the brightness of the LED.

It doesn't matter which LED you use; the forward voltage on the LED always increases until the peak current through

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Use time-domain analysis of Zobel network

Noël Boutin, Université de Sherbrooke, PQ, Canada

A Zobel network is useful in making a reactive load appear as a pure resistance to a driving source prone to stability problems (**Reference 1**). A typical situation is an audio power amplifier driving a loudspeaker, modeled at first approximation as an inductance and a series resistor (**Figure 1a**). The addition of a series R_2C network in parallel with the series R_1L network forms a Zobel network (**Figure 1b**). If you select the proper values of R_2 and C, the driving source sees a purely resistive load. **Reference 2** discusses the computation of the total impedance, Z_L, of the Zobel network:

$$Z_L = \frac{R_1\left[s^2\left(LC\frac{R_2}{R_1}\right)+s\left(R_2C+\frac{L}{R_1}\right)+1\right]}{s^2(LC)+sC(R_2+R_1)+1},$$

from which you find that the following conditions must prevail: $R_2=R_1$ and $C=L/R_1^2$. Designing the Zobel network in the time domain, rather than in the transformed-s domain, yields an easier way to arrive at the same result. Moreover, the method provides a better understanding of the reasons why the driver sees a purely resistive load with a Zobel network.

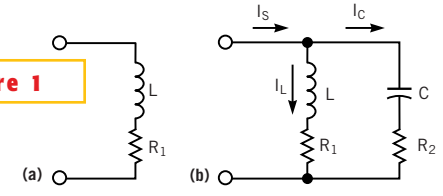

Figure 1

A first-approximation model of a loudspeaker is an inductance and a resistor in series (a); the addition of a series RC network (b) makes the speaker look purely resistive to the driving source.

Without loss of generality, let the driving source be an ideal V-volt step-function voltage source. If the load were purely resistive, the source current, I_S, would also be a step function. In the absence of the series R_2C network, the current flows only through the series R_1L load, starting from a zero value and exponentially increasing toward a final value. The time constant in this case is $\tau_1=L/R_1$. For the source to supply a step current, you must add another branch that draws a current, I_C, such that it compensates for the slow-rising load current, I_L. Adding the series R_2C network meets that requirement. The current, I_C, flowing through that network is instantaneously equal to V/R_2 and then decreases exponentially to zero with a time constant $\tau_2=R_2C$. For the sum of the current, I_L, flowing through the series R_1L network and the current I_C flowing through the series R_2C network to yield a step current I_S, R_2 must equal R_1 and τ_2 must equal τ_1. That is, $R_2=R_1$ and $R_2C=L/R_1$.

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1. Zobel, OJ, "Distortion Correction in Electrical Circuits with Constant-Resistance Networks," *Bell Systems Technical Journal*, July 1982, pg 438.
2. Albean, D, "Zobel network tames reactive loads," *EDN*, Dec 21, 1995, pg 82.

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Circuit improves further on first-event detector

Vasiliy Borodai, Zaporozhje, Ukraine

THE CIRCUITS IN **Figure 1** have certain advantages over those in a previous Design Idea (**Reference 1**). The first-event detector with autoreset (**Figure 1a**) consists of N sets of monostable multivibrators, using 4001 logic circuits with LEDs attached. After any player (1 through N) presses a pushbutton, the corresponding monostable multivibrator switches on, and its associated LED lights. The voltage at Point A changes to a level of nearly 2V (the forward voltage of the LED). After that instant, no other player can change the situation by pressing a pushbutton, because, to switch, the monostable multivibrators need a voltage exceeding 4V. After an interval of 0.5RC (nearly 15 sec for R=1 MΩ and C=33 µF), the monostable multivibrator returns to its previous state, and the circuit is ready for its next first-event detection. **Figure 1b** shows another first-event detector with autoreset, using 4011 logic ICs. This circuit is a mirror image of the circuit in **Figure 1a** and operates similarly.

REFERENCE

1. Arendt, Lawrence, "Circuit improves on first-event detection," *EDN*, Aug 16, 2001, pg 106.

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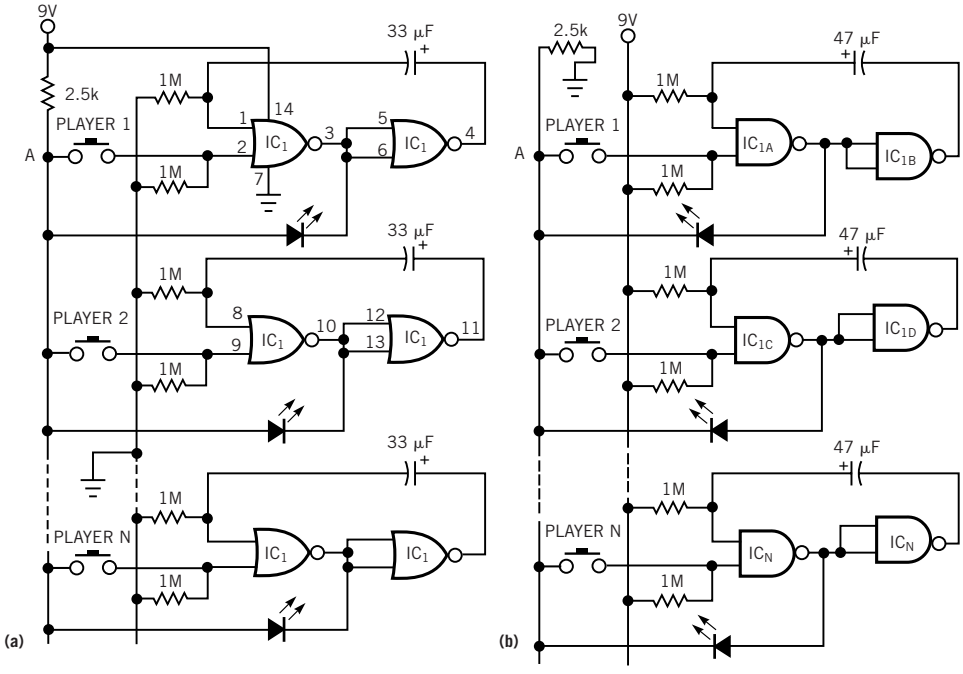
Figure 1



Monostable multivibrators and LEDs form the heart of these first-event detectors with autoreset.

Delay line has wide duty-cycle range

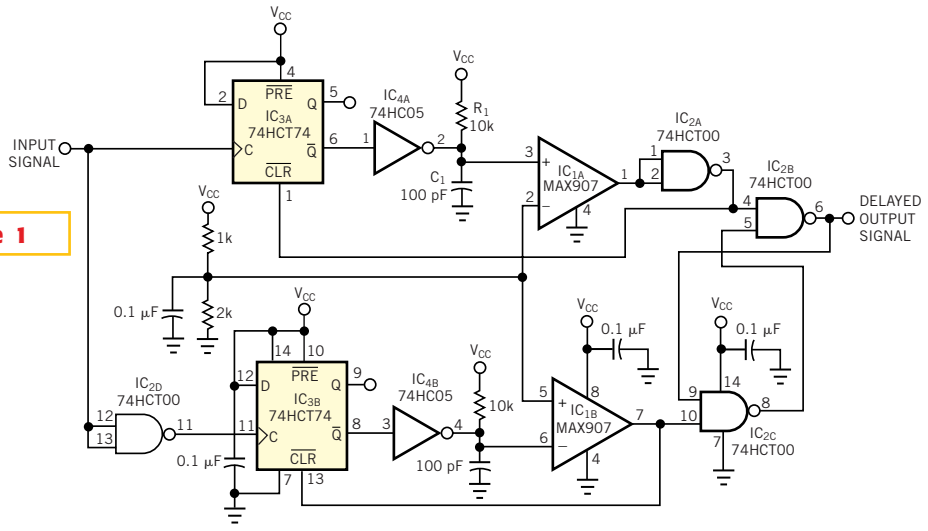
John Guy, Maxim Integrated Products, Sunnyvale.CA

TODAY'S DIGITAL DELAY LINES can process pulses no shorter than their delay times, and that restriction confines the devices to applications in which the duty cycle remains near 50%. A limited range of available delays (2 to 100 nsec per tap) further limits their use. Longer delay is available with one-shot multivibrators of standard digital-logic families, but those devices do not retain duty-cycle information. As an example, a PWM control circuit (**Figure 1**) must handle relatively long delays while retaining information about the input duty cycle. The upper half of this dual-path, precision one-shot works on the input signal's rising edge. The rising edge triggers the D flip-flop, IC_{3A}, to drive IC_{4A}'s input low. IC_{4A} has an open-drain output; the output therefore rises exponentially according to the single R_1C_1 time constant. IC_{1A} compares the output with a dc voltage equal to 67% of V_{CC}, producing a conveniently scaled delay equal to R_1C_1.

The output of comparator IC_{1A} drives the set input of an RS latch (IC_{2B} and IC_{2C}). It also feeds back to the input flip-flop, thereby resetting the flip-flop in anticipation of the next rising edge. The lower half of the circuit in **Figure 1** works in a similar fashion, but it triggers on the input's falling edge and drives the reset

input of the RS latch. You can test the circuit with a 100-kHz input signal and a nominal delay of 1 µsec. When the input duty cycle varies from 10 to 90% (limits imposed by test equipment), the duty-cycle error is less than 0.1%. You can obtain this performance with unmatched components. The circuit produces accurate pulse widths for pulses as narrow as 20 nsec. To ensure accuracy, the timing capacitors should be NP0 types with 5% tolerance, and the resistors should be 1% accurate. The MAX907 comparator from Maxim (www.maxim-ic.com) provides the high input impedance, high precision, and low propagation delay the circuit requires. For most applications, 74-HC/HCT logic is fast enough to minimize propagation-delay errors. Note the inclusion of a NAND gate connected as an inverter, IC_{2A}, which enhances accuracy by equalizing the propagation delays in each channel.

Figure 1



Based on a precision dual comparator, this delay line generates accurate duty cycles.

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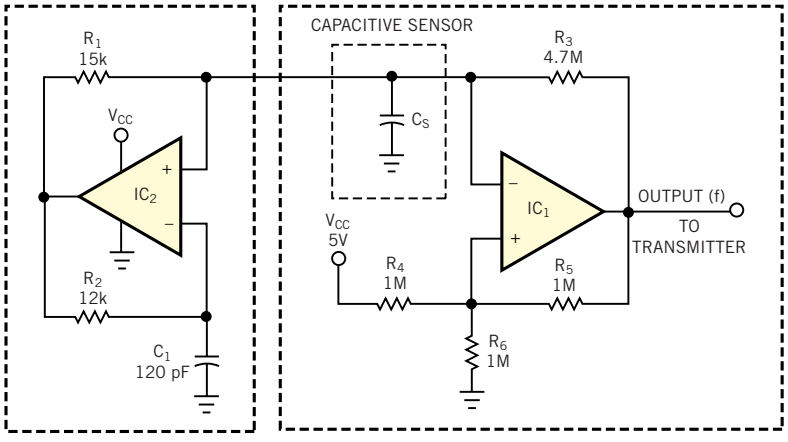
design ideas

Edited by Bill Travis

Improved frequency modulator uses "negatron"

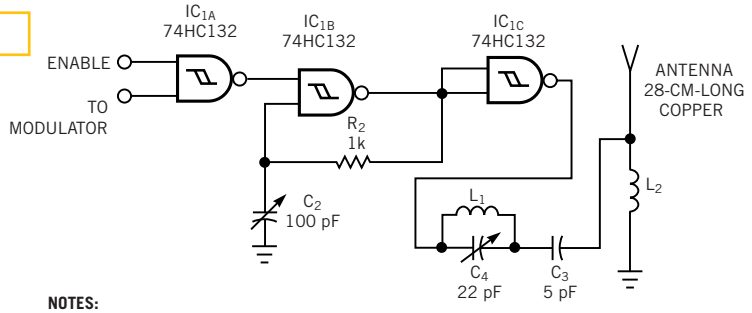
Alexander Bell, Infosoft International, Rego Park, NY

You can improve a capacitive-sensor circuit with a modulator and an RF transmitter (**Reference 1**) by modifying the modulator portion to obtain better accuracy. More improvements result from adding a "negatron" circuit, a configuration that uses equivalent negative capacitance. **Reference 2** gives some insight into the uses of negative impedance. The circuit in **Figure 1** works with the RF transmitter of **Reference 1** (**Figure 2**) as follows: The modulator uses op amp IC_1 in a standard flip-flop configuration (with the addition of the bias resistor R_4, because of single-supply operation). The negatron portion of the circuit uses op amp IC_2. The output frequency, f, of the modulator without the negatron is a function of the time constant $\tau_M=R_3C_S$. Thus, the frequency is a function of the physical value of the input (for example, pressure or humidity). The potential accuracy and stability of the modulator in **Figure 1** are greater than those of the modulator in **Reference 1** because of the low input capacitance and temperature coefficient of the LTC1124 op amp and the high stability of the R_4-R_6 voltage threshold.



NOTE: OP AMPS=LTC1124s.

Figure 1 **The modulator portion provides improved performance over the circuit in Reference 1; the negatron increases sensitivity and resolution.**



NOTES:
L_1 IS SIX TURNS OF 22-GAUGE WIRE WITH 5-MM DIAMETER.
L_2 IS 18 TURNS OF 22-GAUGE WIRE WITH 5-MM INNER DIAMETER.

Figure 2 **This simple transmitter from Reference 1 allows you to remotely measure physical phenomena.**

Adding the negatron portion in **Figure 1** increases the relative sensitivity of the frequency modulator. The equivalent capacitance of the negatron is $C_N=-C_1(R_2/R_1)$. Assuming the physical value of the input causes the change ΔC (compared with the sensor's initial capacitance, C_0), the relative output-frequency change without the negatron (for small ΔC) is $\Delta f/f_0=\Delta C/C_0$. With the negatron added, the equation is: $\Delta f/f_0=\Delta C/(C_0-C_1(R_2/R_1))$. The result is higher relative sensitivity because of the reduction in the denominator value. The value of C_N is ap-

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proximately −100 pF for the circuit in **Figure 1**. In other words, a given change in the input value causes a greater relative-frequency deviation. Note that adding the negatron changes the equivalent time constant: $\tau = R_3(C_S - C_1(R_2/R_1))$. You can make value adjustments in R_3 to obtain the desired initial frequency, f_0. Also, note that the measured values of f_0 and Δf may differ from the calculated ones because of parasitics and the input capacitance of the op amp.

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1. Tiwari, Shyam, "Low-cost relative-humidity transmitter uses single logic IC," *EDN*, Nov 8, 2001, pg 116.

2. Belousov, Alexander, "Negative impedance improves capacitive sensors," *EDN*, March 30, 1995, pg 82.

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Get buck-boost performance from a boost regulator

Tom Gross, Linear Technology Corp, Milpitas, CA

THE SEPIC (single-ended, primary-inductance-converter) topology is generally a good choice for voltage regulators that must produce an on output voltage that falls in the middle of the input-voltage range, such as a 5V output from a 2.7 to 6V input, The topology has some disadvantages, however. The efficiency of a SEPIC circuit fares worse than that of buck and boost regulators, and SEPIC designs often involve the use of large, complex magnetic components, thereby complicating the design task. **Figure 1** shows a simple and efficient alternative topology. When the input voltage is lower than the output voltage, the circuit operates as a normal boost regulator. The inductor, L_1, stores energy when switch Q_1 is on and the boost diode, D_1, is reverse-biased. While D_1 is off, the output capacitor, C_1, delivers the load current. When Q_1 turns off, L_1 reverses its polarity, thereby forward-biasing D_1. L_1 then charges C_1 and delivers current to the load. The inductor voltage adds to the input voltage to generate the output voltage.

The low-battery comparator in IC_1, which usually checks battery levels, monitors the output voltage through its LBI pin. IC_1's internal comparator output switches low (sinking current). This action turns the p-channel Q_1 fully on, cre-

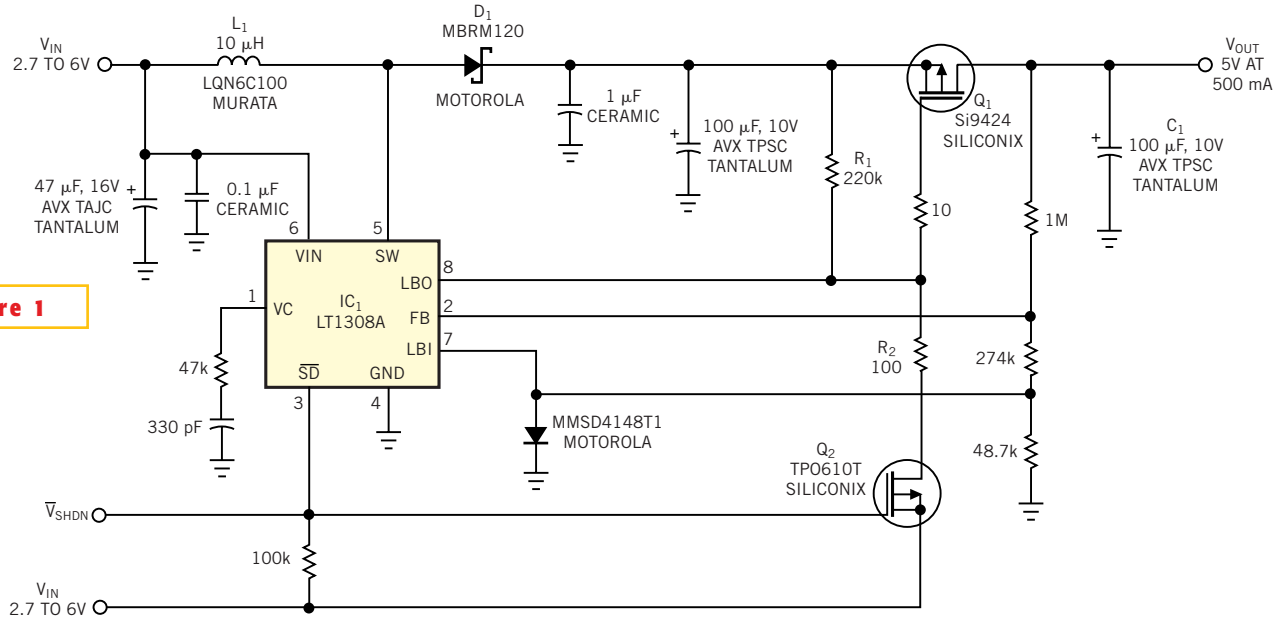
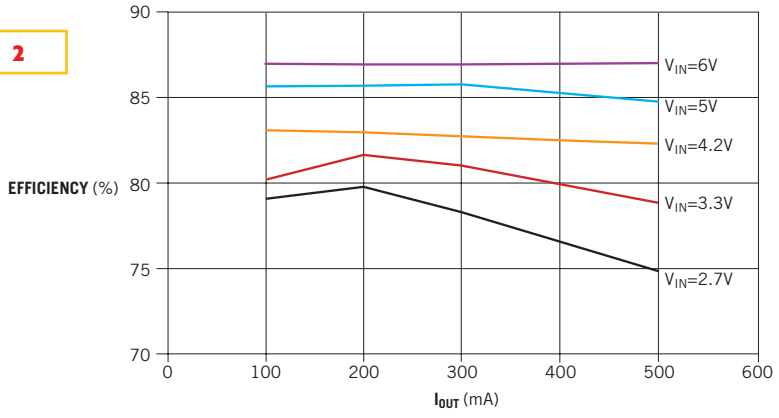


Figure 1

This circuit can both boost and step down the output voltage, depending on whether the input voltage is lower or higher than the output voltage.

ating a low-impedance path to the output. When the input voltage is the same value as or greater than the output voltage, the circuit functions like a linear regulator. In this case, the internal comparator's output assumes a high-impedance state. The voltage at the gate of Q_1 begins to pull up through R_1, a 220-kΩ resistor, so Q_1 begins to turn off. This action forces the output voltage to decrease, and the comparator eventually again switches states from high to low (sinking current). The comparator's low state causes the output voltage to rise again, and the cycle repeats. Thus, the circuit begins to operate as a linear regulator, with Q_1 acting as the pass transistor.

Figure 2



The efficiency of the circuit in Figure 1 depends on whether the circuit acts as a boost converter or a linear regulator.

The circuit can also disconnect the input-to-output current path, unlike a conventional boost regulator. The shutdown signal connects to the gate of Q_2, a logic-level, p-channel MOSFET, as well as to IC_1's shutdown ($\overline{SD}$) pin. When the shutdown signal goes low, it turns off IC_1 and turns on Q_2. This action delivers V_{IN} (via R_2, a 100Ω resistor) to the gate of Q_1, thereby turning off the transistor. Hence, the shutdown operation disconnects the input-to-output current path. **Figure 2** shows how the efficiency of this linear-boost regulator depends on its mode of operation. When the input voltage is lower than the output voltage, the efficiency of the regulator is that of a boost regulator. When the input voltage exceeds the output voltage, the circuit operates as a linear regulator in which efficiency is approximately V_{OUT}/V_{IN}.

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Circuit transmits ARINC 429 data

Steve Woodward, University of North Carolina, Chapel Hill, NC

THE ARINC (Aeronautical Radio Inc) 429 specification defines the air transport industry's hardware and protocol standards for the transfer of digital data between avionics systems. Circuitry that can implement elements of the 429 spec is often an essential part of control and sensor electronics intended for the aviation environment. ASIC chips for this purpose are commercially available, but they typically require nonstandard power supplies (for example, ±15V) and wide parallel interfaces. Therefore, it's sometimes inconvenient to accommodate them in 5V microcontroller-based designs. The circuit in **Figure 1** serves the Tx (transmit/output) portion of the 429 spec. The design implements a high-speed ARINC-429-compliant transmit function using a single 5V supply rail and 74HC series chips.

TABLE 1—FORMAT OF SPI BITS

		SPI bit							
Byte	ARINC field	7	6	5	4	3	2	1	0
1	Label	L	L	L	L	L	L	L	L
2	LS data	N	N	N	N	N	N	SDI	SDI
3	Data	N	N	N	N	N	N	N	N
4	Parity+MS data	OPB	SSM	SSM	N	N	N	N	N
5	Spacer byte	0	0	0	0	0	0	0	0

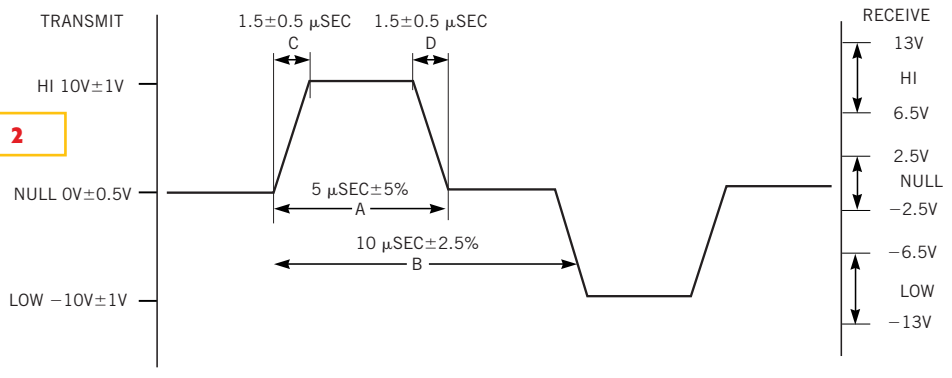
L…L = ARINC label (most-significant bit transmitted first)
SDI = ARINC source/destination identifier
N…N = 19 data bits (may include SDI and SSM fields; transmit least-significant bit first)
SSM = ARINC sign/status matrix
OPB = Odd parity bit (makes total count of "1" bits in the 32-bit word odd)

The physical transmission medium for the 429 standard is 78Ω shielded, twisted-pair cable that uses a complementary, differential bipolar RZ (return-to-zero) waveform (**Figure 2**). The voltages are the net differentials that the biphase drive develops: For example, the differential is 10V when you drive the Data A signal in **Figure 1** to 5V and the Data B signal to −5V. In addition to the signal levels, a 429 system must closely control the rise and fall times to conform to the specification. This control limits both in-

tra-cable signal crosstalk and EMI radiation that might interfere with sensitive aircraft communication and navigation systems. The operation of the transmitter in **Figure 1** centers around IC_1, a 4-bit×16-word FIFO memory. The serial ARINC bit stream comes from the microcontroller's synchronous serial-peripheral interface (SPI); the C input of IC_1 buffers the data stream. In addition, the D input of IC_1 serves as a buffered ARINC-enabled bit (the microcontroller's J port, bit 2). When low, this bit disables the ARINC transmitter logic and permits other system peripherals to use the SPI hardware.

Bits A and B of IC_1 go unused. The 100-kHz ARINC high-speed baud rate comes from the 1-MHz reference supplied to the IC_{3A} divide-by-10 circuit. The 100-kHz signal drives IC_1's shift-out (SO) pin and the IC_2 pulse gate. The presence of bits in the IC_1 FIFO (indicated by QR=1) resets the ARINC RDY bit in IC_{3B} and enables IC_{3A}. If IC_1's D bit (Pin 10) is also high, it gates the 100-kHz square wave to the IC_4 multiplexer. This action causes the sequential gating of −5, 0, and 5V onto the A/B data-output signals in ARINC-compatible waveforms. The LRC network at the output ensures compliance with the 429 requirements for rise and fall times. The circuit must process five 8-bit SPI bytes to generate each 32-bit, 429-compliant output word. **Table 1** shows the format of the SPI bits. The first four bytes in **Table 1** combine to form a 32-bit ARINC 429 word. The 32-bit word, reading from right to left, starts with byte 1 (again, reading from right to left), then tacks on byte 2, and so on.

Figure 2



The ARINC spec imposes rigid requirements on waveforms.

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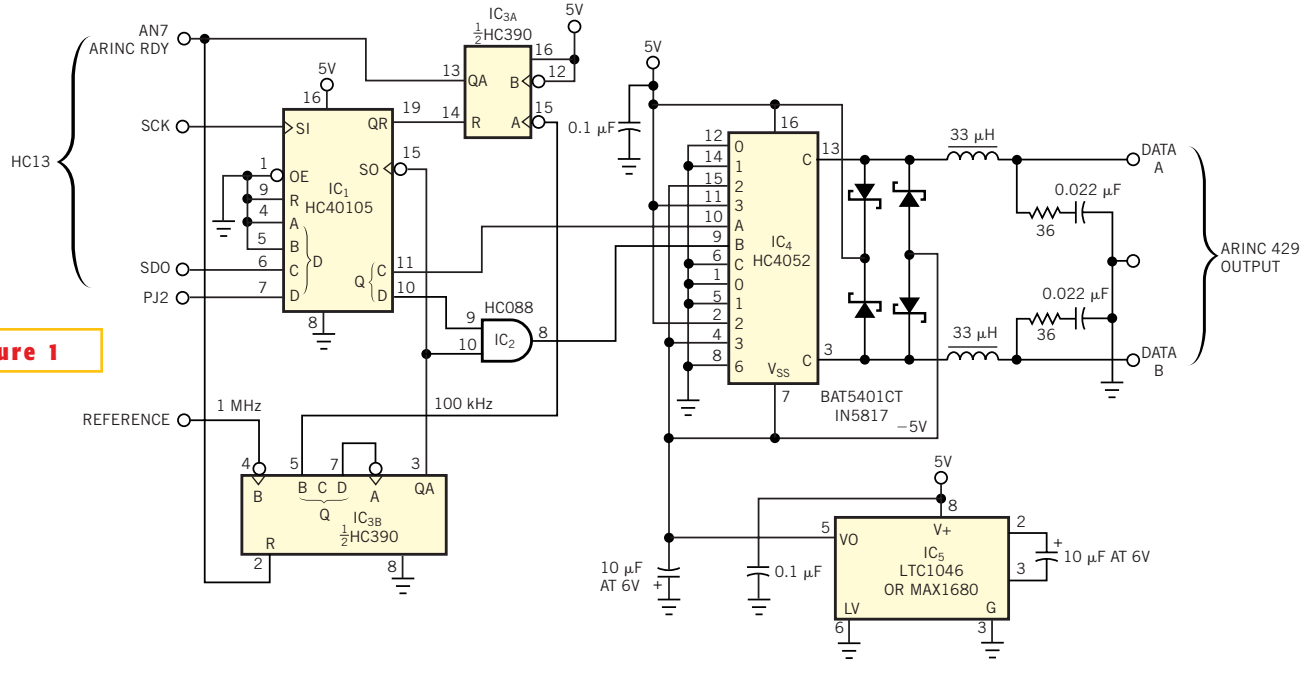
Figure 1



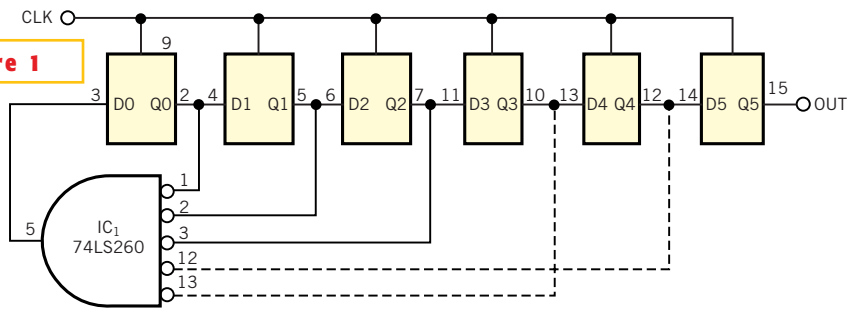
This ARINC 429 transmitter operates from a single 5V supply and meets all timing requirements of the 429 spec.

Circuit divides frequency by N+1

Bert Erickson, Fayetteville, NY

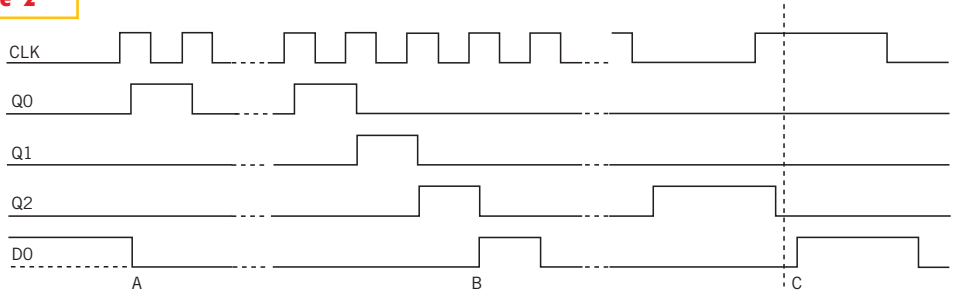
Digital frequency dividers usually use flip-flop stages that connect the $\overline{Q}$ pin to the D data-input pin of the following stage. This configuration creates a binary waveform that you can feed back to the input. You can divide any integer lower than 2^N with minimal stages, where N is the number of stages. These dividers can easily select one frequency from 100 for a receiver. However, as the applied clock rate approaches the ratings of the devices, decoding spikes appear. As a result, you'd be ill-advised to use the dominant pulse in such a waveform for clocks or strobes. The divider in **Figure 1** uses a ring configuration, and the stages connect Q-to-D, without using the $\overline{Q}$ output, to provide a binary sequence. Consequently, the circuit can divide only by N+1, but it produces a clean waveform at an applied clock rate that's substantially higher than you can apply to conventional binary dividers using flip-flops from the same process families.

Figure 1



This N+1 divider displays no decoding spikes, even at high clock rates. The added NOR circuit ensures proper start-up.

Figure 2



These waveforms illustrate the operation of the N+1 divider; note the propagation delay from the NOR gate in Section C.

If the last Q in a cascade of 74xx174 flip-flops connects to the D input, the loop becomes a shift-register ring counter. Moreover, the circuit can operate at a clock rate higher than that of any other configuration. Unfortunately, when you turn on the power or ground the reset pin, all Q outputs go low and remain low when you apply the clock. To circumvent installing a preset circuit that must operate at a high clock rate, you can place one NOR gate with its propagation delay in the loop. This addition ensures that the divider always starts and continues to function properly. Because this gate receives inputs from all stages at once, it features parallel carry and has the properties of a parallel-carry counter. For simplicity, **Figure 1** does not show the reset line, and you can delete the broken feedback lines, providing that you ground the corresponding input pins. You can take the output from any Q pin and use an additional stage, such as Q5, for a buffer. Although the output of the NOR gate resembles one of the Qs, you should not use it as an output.

Figure 2 shows the timing diagram for the divider. Section A of the diagram shows the state of D0 and the Q outputs in the start-up condition before the first and second clock pulses arrive. Note that when the power turns on or when the reset pin connects to ground, the Q outputs are all low, and D0 is high. D0 then transfers to Q0 on the rising edge of the first clock pulse. Section B of the diagram shows the output for a repetitive sequence starting with Q0. Section C is an expanded representation of the end of the sequence. Note that Q2 falls after the clock pulse rises. Then, with all Q outputs low, D0 rises a short time later to allow the sequence to repeat. D0's transfer can take place only after the next clock pulse rises. This factor creates an additional time slot to make the total N+1. Section C shows the propagation delay attributable to the NOR gate—approximately 10 nsec for most logic-circuit families and less than 5 nsec for the F and S series. This propagation delay is the only additional delay in the loop. A comparison of the output waveforms with those from a 74xx90 divide-by-5 counter shows prominent decoding spikes from this counter. The N+1 divider had no spikes and operates at a much faster clock rate.

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Maintain precise timing with PC's speaker logic

DS Oberoi, CEDTI, and Harinder Dhingra, GCET, Jammu, India

Precise timing control is paramount in data acquisition and analysis and especially in digital-signal processing. The easiest way of maintaining timing control in a PC is to use delay loops. The disadvantage of this implementation is that the delay loop's elapsed time depends on the system's operating frequency. Hence, a program works accurately with a single operating frequency, but you must modify it for other frequencies. You can use add-on cards to achieve timing control, but they're costly, and, for simple operation, they remain underused. This Design Idea explores another way to obtain timing control. You can implement a stable delay loop with the aid of the PC's speaker logic. In PC/AT architecture, a 16-bit 8255 timer/counter IC is available, and the IC's operating frequency of 1.1931817 MHz is fixed across the entire range of PC families. You can use this fixed-frequency feature to implement a delay loop.

In PC/AT architecture, Counter 0 serves as a system timer and to maintain the time of day. Counter 1 generates pulses and serves as the DRAM refresh-rate generator. The PC uses Counter 2 for sound generation through the PC's speaker. Only Counter 2 is available for an implementation of the delay loop. You can enable or disable Counter 2 by setting bit 0 of the 8255's Port B to 1 or 0, respectively. For our purposes, Counter 2 operates as a rate generator (in Mode 2 operation). In this mode, the counter automatically decrements by one count with every counter clock pulse (1/1.1931817 MHz=0.838095 μsec= counter_count_time). Hence, the total period that Counter 2 can measure is approximately 54.92 msec (65,536×0.838905 μsec). **Listing 1** gives the details of implementing the delay loop. You can download **Listing 1** from the Web version of this Design Idea at www.ednmag.com.

The software sets Counter 2 to operate in Mode 2 by setting the control-word value to 0b4h and by writing this control-word data to the control-register port (043h). A routine called delay_loop() actually implements the delay loop. The routine first configures Counter 2 by writing the control word in the control register. Then, the program loads Counter 2 with starting (ffffh) data at address 042h in a 2-byte operation. The routine then enables the counter by setting bit 0 of the 8255's port B (in other words, port 61h) to one. Once enabled, Counter 2 automatically decrements by one count every 0.8380958 μsec. Before calling the delay routine, the software computes the total of Counter 2's count required for the desired delay (desired_delay_time). A "while" loop repeatedly reads back Counter 2's data from its input port (042h) in a 2-byte operation.

The two bytes combine to produce 16-bit data (counter_data). This data helps to compute the elapsed counts (count_elapsed); as soon as the required count is reached, the software exits this loop. The routine disables Counter 2 by setting bit 0 of the 8255's port B to 0 before returning to the calling program. Thus, it achieves the desired delay. Because the count depends on a fixed operating frequency across the entire PC family, you can use this method to implement a precise and stable timing loop. You can achieve delays of approximately 20 μsec to 54.9 msec. The software is in Turbo C++ and assembly language and was tested it in MS-DOS mode on a 450-MHz Pentium II computer.

LISTING 1–DELAY-LOOP ROUTINE

```
#include <conio.h>
#include <dos.h>
#define counter_count_time 0.0008380958 /* Counter2's single count period(mS) */
#define read_port 0x378                 /* Address of Read Port       */

unsigned counter_data, count_elapsed, required_count;
float desired_delay_time;

void delay_loop(unsigned delay_count);
main()
{
        desired_delay_time=0.9;     /* Delay Time in milli second */
  /* Find how many counts are required for the desired delay */
        required_count = desired_delay_time/counter_count_time;
        for (;;)
        {
         ; /* Place the desired statements here, before delay */
         ;

         delay_loop(required_count); /* Call The Delay Routine */

         ; /* Place the desired processing statements here, after delay */
         ;
        }
}

/* Delay Routine starts here */
void delay_loop(unsigned delay_count)
{
        count_elapsed = 0;
        asm mov al, 0b4h    /* Set the counter2 operation */
        asm out 043h,al
        asm mov al, 0ffh    /* Load the intial count as ffffh          */
        asm out 042h, al    /* completed in two cycles         */
        asm out 042h,al
        asm mov al, 01h     /* Enable the  counter and Start the ON period */
        asm out 061h, al

/* Counter data is read till,  desired counts are not  obtained          */
        while (count_elapsed < required_count)
        {
          asm in al, 042h       /* Get LSB      */
          asm mov cl, al
          asm in al, 042h             /* Get the MSB    */
          asm mov ah, al
          asm mov al, cl              /* Two bytes, combined to get 16 bit data*/
          asm mov counter_data , ax
          count_elapsed = (0xffff- counter_data); /* Calculate the elapsed counts  */
        }
/* Disable the counter2 */
          asm mov al, 00h
          asm out 061h, al
}
```

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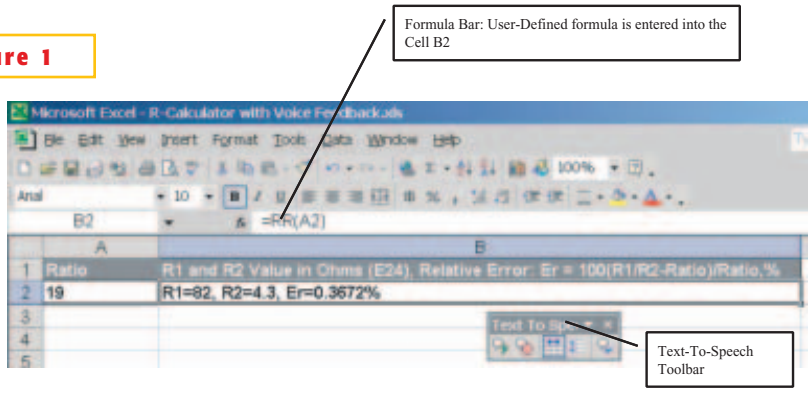
Voice feedback enhances engineering calculator

Alexander Bell, Infosoft International Inc, Rego Park, NY

The screen shot in **Figure 1** represents a Microsoft Excel 2002 worksheet designed to implement VFI (voice-feedback interface) for an engineering calculator. The voice-interface technique has both practical and educational aspects. It automates the common task of finding the values of two resistors for a given ratio. It also demonstrates the latest advances in natural-language programming technology with an example of the technology's actual implementation in CAD/CAE systems. A single user-defined function RR (resistor ratio) encapsulates both the computation engine and the VFI. The function uses VBA (Visual Basic for Applications) with the code placed in the standard code module of Excel File (**Listing 1**). You can download **Listing 1** and the Excel worksheet from the Web version of this Design Idea at www.ednmag.com.

Figure 1



Cell A2 serves for data (ratio) entry; cell B2 contains the user-defined formula 5RR(A2). In automatic calculation mode, every time you enter a new ratio value in A2, the system recalculates R_1, R_2, and Relative Error.

The core search algorithm, which contains outer and inner loops, sequentially

LISTING 1—CODE MODULE FOR VOICE FEEDBACK

```
Option Explicit

Function RR(ByVal Ratio As Variant) As String
'** AUTHOR: ALEXANDER BELL
'** DATE : 02/02/02
'** USAGE : FIND THE RESISTORS' VALUE R1 AND R2 FROM E24 SERIES WHICH MAKES THE
BEST
'**       : APPROXIMATION FOR GIVEN RATIO, BASED ON CRITERIA: MIN(ABS(RATIO-R1/R2)).
'**       : FORMULA LIMITATIONS: 1=< RATIO < 100 000 000.
'**       : NOTE: RETURN RESISTORS' VALUES ARE SHOWN IN OHMS
On Error GoTo ErrorHandle
   Const MAX_ORDER As Integer = 8  '** CONST USED TO SET LIMIT FOR RATIO (<100 000 000)
   Dim R1 As Double, R2 As Double  '** RESISTORS' VALUE VARIABLES
   Dim dblError As Double          '** ERROR OF APPROXIMATION VARIABLE
   Dim I As Integer, J As Integer  '** LOOP COUNTERS
   Dim dblMantissa As Double       '** MANTISSA VARIABLE
   Dim intOrder As Integer         '** ORDER VARIABLE
   Dim arrE24 As Variant           '** VARIABLE REFERENCING TO E24 VALUES ARRAY
   Dim str_MSG As String           '** VARIABLE CONTAINING THE VOICE NOTIFICATION TO
USER

'** DATA VALIDATION WITH VOICE FEEDBACK
'*************************************************
If CStr(Ratio) = "" Then
   str_MSG = "PLEASE, ENTER THE NUMERIC VALUE."
   Application.Speech.Speak str_MSG, True
   Exit Function
End If
If Not IsNumeric(Ratio) Then
   str_MSG = "WRONG ENTRY: PLEASE, ENTER THE NUMERIC VALUE."
   Application.Speech.Speak str_MSG, True
   Exit Function
End If
If Ratio < 1 Then
   str_MSG = "WRONG ENTRY: RATIO MUST BE MORE OR EQUAL 1, OTHERWISE USE THE
INVERSE VALUE."
   Application.Speech.Speak str_MSG, True
   Exit Function
End If
If Ratio >= 10 ^ MAX_ORDER Then
   str_MSG = "WRONG ENTRY: RATIO NUST BE LESS THAN " & CStr(10 ^ MAX_ORDER)
   Application.Speech.Speak str_MSG, True
   Exit Function
End If

'** E24 SERIES ARRAY. LAST VALUE (10) IS INCLUDED TO SIMPLIFY THE SEARCH
ALGORITHM
arrE24 = Array(1, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.8, 2, 2.2, 2.4, 2.7, _
      3, 3.3, 3.9, 4.3, 4.7, 5.1, 5.6, 6.2, 6.8, 7.5, 8.2, 9.1, 10)

'** CALCULATE ORDER AND MANTISSA FOR GIVEN RATIO
intOrder = Int(Log(Ratio) / Log(10))
dblMantissa = Ratio / (10 ^ intOrder)
'** SET RESISTORS INITIAL VALUES
R1 = 1: R2 = 1
dblError = Abs(R1 / R2 - dblMantissa)

'** LOOP THROUGH E24 ARRAY TO FIND R2 AND R1 MANTISSA RESULTING IN A MIN ABS
ERROR
'** NOTE: THIS ALGORITHM RETURNS R1 MANTISSA WHICH IS ALWAYS BIGGER OR
EQUAL R2
For I = LBound(arrE24) To UBound(arrE24)
   For J = LBound(arrE24) To I
      If Abs(arrE24(I) / arrE24(J) - dblMantissa) < dblError Then
         R1 = arrE24(I)
         R2 = arrE24(J)
         dblError = Abs(arrE24(I) / arrE24(J) - dblMantissa)
      End If
   Next J
Next I

'** CALCULATE R1 VALUE IN OHMS AND RELATIVE ERROR IN (%)
R1 = R1 * 10 ^ intOrder
dblError = (R1 / R2 - Ratio) / Ratio

'** RETURN RESULT STRING: RESISTORS' VALUES IN OHMS, RELATIVE ERROR IN %
RR = "R1=" & CStr(R1) _
      & ", R2=" & CStr(R2) _
      & ", Er=" & Format(dblError, "0.0000%")
'** SEND "OK" VOICE NOTIFICATION TO USER AND EXIT FUNCTION
str_MSG = "OK. "
Application.Speech.Speak str_MSG, True
Exit Function
ErrorHandle:
'** IN CASE OF ERROR RETURN EMPTY STRING AND SEND THE ERROR VOICE
NOTIFICATION TO USER
   RR = ""
   str_MSG = "UNANTICIPATED ERROR IN CALCULATIONS."
   Application.Speech.Speak str_MSG, True
End Function
```

tests each pair of values, R_1 and R_2, to find the best approximation of the target ratio. In other words, the algorithm tries to minimize the absolute error: (ABS (R_1/R_2-Ratio)). The values of R_1 and R_2 come from the E24 EIA-standard series, but you can apply the same algorithm to any other standard series, such as E48, E96, or E192. The VFI sends the status-notification message in a verbal form instead of showing the Message Box. The VFI uses the built-in Excel 2002 Speech Object with the following syntax:

Application.Speech.Speak
<String Variable or Constant>, True,

where <String Variable or Constant> contains the actual spoken text, and the second property is set to True for asynchronous mode. **Listing 2** is an example of voice-error notification in the case that you enter non-numeric data as the ratio (data-validation error message):

LISTING 2–VOICE-ERROR NOTIFICATION

```
IfNot IsNumeric(Ratio) Then
  Str_MSG5"Wrong ENTRY: PLEASE, ENTER THE NUMERIC VALUE."
  Application.Speech.Speak str_MSG, True
  Exit Function
End If
```

Using the technique is simple. Open Excel File, switch to the Visual Basic Editor window (press Alt-F11), add the standard module, and paste the code from **Listing 1**. From the Debug menu item, choose Compile VBA Project, save the file with any name, and close the Visual Basic Editor window. Make sure you activate the text-to-speech tools (in the menu: Tools—Speech—Show Text To Speech Toolbar). Check whether you are in automatic- or manual-calculation mode (in the menu: Tools—Options—Calculation). Set the mode to automatic; otherwise, you'd have to use the F9 key to force a new calculation every time you enter a new ratio value. Choose any cell (for example, A2 in **Figure 1**) for the ratio (data-entry cell) and another cell (for example, B2) to display the results. Enter the formula =RR(A2) into cell B2. Now, every time you enter a new ratio value into cell A2, the system automatically calculates and displays R_1, R_2, and Relative Error, and sends the status voice notification. The notification is either "OK" to confirm the successful completion of the calculation or an error notification in the case of a data-validation or computation error. Note that some macros in Microsoft Office applications could result in potentially dangerous and harmful actions, and some may contain viruses. You use the macros at your own risk without warranties of any kind.

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design ideas

Edited by Bill Travis

Simple circuit provides motor-feed control

Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

Because we needed a small grinding machine, we modified an old milling machine that lacked a control system. The table of the grinding machine needed only to move back and forth with adjustable feed. Using an existing dc servoamplifier, a servo motor, and limit switches, we devised the circuit shown in **Figure 1**. Because the motor had no tachometer, we used part of the motor voltage as feedback. We reduced the feedback voltage from the motor to approximately 8V by using the resistors R_1 to R_3. (Motor voltage=60V, maximum amplifier input=10V, R_1=R_2=33 kΩ, and R_3=10 kΩ.) This feedback voltage feeds back to the speed-command differential-voltage input. You must be careful with the feedback-signal polarity to avoid an uncontrolled runaway of the motor. The actual command voltage connects to the tachometer input, which is not differential. Using the appropriate gain and control-loop adjustments available on most drivers, you can obtain good motor response. This design uses the ±15V the driver supplies to power the control circuit. Switch S_1 enables manual and automatic modes. For both modes, potentiometer P_1 reduces the control voltage, and C_1 filters it. Two LEDs, D_1 and D_2, show in which direction the axis moves. This indication can be especially useful in automatic mode if the potentiometer is turned to its zero position. The driver becomes disabled in one direction when the inputs +Limit or −Limit no longer connect to 15V; that is, when the limit switches LS+ or LS− (located at each end of travel) become activated. The following describes the operation of the two modes:

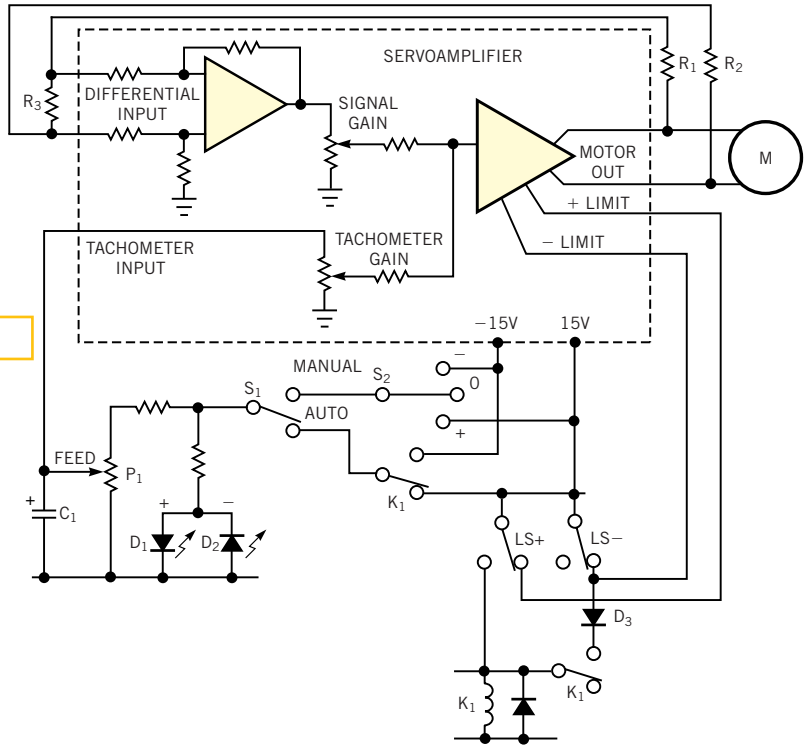

Figure 1 A defunct milling machine served as the platform for this grinding-machine motor controller.

- In manual mode, the momentary switch S_2, selects 15V or −15V. If you use two separate switches, take care to avoid shorting both power supplies together.
- In automatic mode, the polarity of the voltage depends on the setting of relay K_1. Upon power-up, K_1 is off; thus, a positive voltage goes to the driver. The motor moves in the positive direction until limit switch LS+ activates. At that instant, the driver is disabled (for the positive direction), and the relay, K_1, energizes. K_1 holds itself on through its

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contact, diode D_3, and the limit switch, LS−. You need the diode to avoid feeding voltage to the −Limit input through the activated LS+ limit switch. The motor now runs in the opposite direction until the limit switch LS− activates. At that instant, the driver is disabled (for the negative direction), and relay K_1 turns off. The cycle begins anew.

The values of the components the circuit uses depend principally on the selected servoamplifier and motor, thus **Figure 1** shows no values. The machine has worked satisfactorily in two shifts for more than two years. During this period, contrary to our expectations, we never readjusted the servoamplifier.

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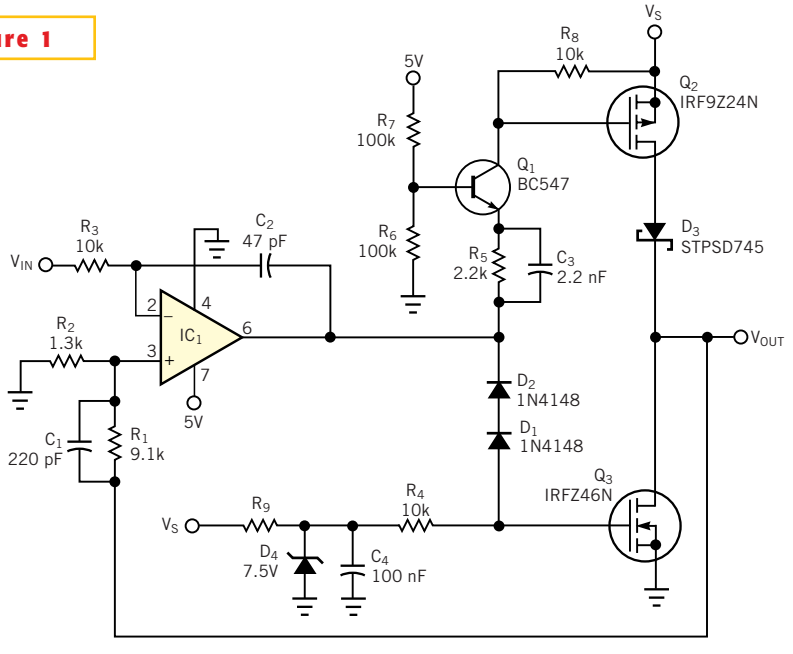
Linear power driver works from single supply

Tom Gay, Darmstadt, Germany

In low-power, single-supply analog applications, it is often desirable to maintain precise control of voltages much greater than the positive-supply rail. The circuit in **Figure 1** allows you to amplify the input voltage, V_{IN}, by a factor, A, which resistors R_1 and R_2 set. The output voltage, V_{OUT}, equals AV_{IN}, where $A=R_2/(R_1+R_2)$. The op amp receives its supply from a single 5V source, and the discrete output stage operates from a rectified voltage, V_S, from a power source that meets the requirements of the application. When the circuit neither sinks nor sources current, the op amp's output settles to a voltage higher than 1.9V (Q_1 is completely off) but lower than the threshold voltage of the n-channel FET, Q_3, minus 1.2V (two diode drops). When V_{IN} rises from a given state, the op amp's output voltage drops and gradually turns on Q_1. This action results in a voltage drop across R_8, turning on Q_2. This process continues until the voltages at the op amp's two inputs match. A decreasing V_{IN} causes the op amp's output voltage to rise to the point at which Q_3 conducts enough to pull down V_{OUT}. Capacitors C_1, C_2, and C_3 are necessary to prevent oscillation.

Figure 1



This simple circuit allows you to control voltages far in excess of the positive-supply rail.

The circuit, useful as a power driver for pulse generators, offers rise and fall times of less than 15 µsec, virtually independently of the supply voltage, V_S. You can test the design with op amps LMC7101, LT1013, and AD8551. All these op amps deliver load currents as high as 5A at voltages as high as $V_S=40V$. One important feature of the design is its insensitivity to component tolerances. The values for R_1 and R_2 in **Figure 1** yield A=8. The value of R_9 depends on V_S. You could use a logic-level FET, such as the IRLZ34N for Q_3; you can then omit the components D_1, D_2, D_4, R_4, R_9, and C_4. In this case, the op amp's output connects directly to the gate of Q_3, and you must reduce the value of R_6 to lower the base voltage of Q_1 to maintain the "idle window" in which both Q_1 and Q_3 are off. The op amp's input-voltage range must include ground. D_3 is necessary only in cases in which sources connect to the output. D_3 prevents reverse current flow from the external source through Q_2. Such a situation can arise when the circuit serves in a battery-charger application.

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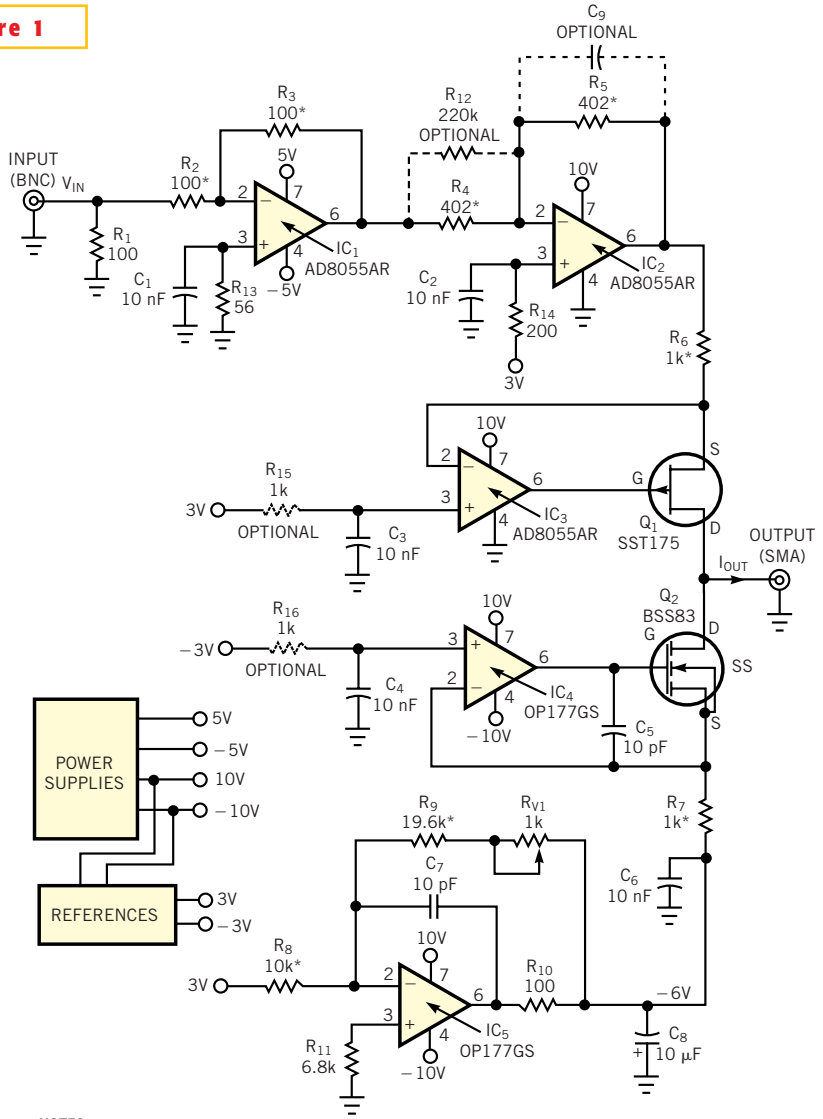
Circuit performs high-speed voltage-to-current, current-to-current conversion

Ali Mehmed, Nokia UK Ltd, Southwood, UK

THE CIRCUIT IN **Figure 1** performs active voltage-to-current conversion or acts as a variable-gain current mirror with high precision and bandwidth. A typical application is testing high-speed ICs or other devices that have inputs designed to be driven from current-steering DACs to enable a modulated voltage source to control the devices. The circuit thus simplifies the testing of such devices in isolation, because modulated voltage sources are readily available, but modulated current sources generally are not. A further use of the circuit could be for easy and precise control of a current-controlled, variable-gain amplifier by using an adjustable dc voltage source at the input. **Figure 1** shows the circuit configured as a voltage-to-current converter. The overall "gain" with the component values shown is 1 mA/V, but you can easily realize other gains by altering the component values. Note that the output of the circuit can both source and sink current.

Starting at the input, V_{IN}, because the input of amplifier IC_1 is at virtual ground, the parallel combination of R_1 and R_2 provides a 50Ω termination for the input signal. IC_1 then inverts this signal with a gain of R_3/R_2. Amplifier IC_2 provides a gain of $-R_5/R_4 = -1$ to the signal received from IC_1, but its noninverting input is tied to the 3V reference. Therefore, its output and the top of the current-sense resistor, R_6, is offset by 6V with respect to ground when V_{IN} is zero. The current source comprises amplifier IC_3 and the p-channel JFET, Q_1. The choice of a JFET, rather than a bipolar transistor, ensures very high speed, zero dc error, and almost perfect linearity in the output-current characteristic. The JFET is an SST175 from Vishay/Siliconix (www.vishay.com); it has a guaranteed I_{DSS} current of 7 mA, high speed, and low

Figure 1



NOTES:
1. RESISTORS MARKED WITH * ARE 0.1% TOLERANCE.
2. ALL OTHER RESISTORS ARE 1% TOLERANCE.
3. DECOUPLING FOR ICs IS NOT SHOWN.

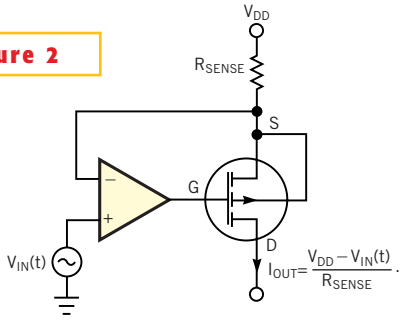
This versatile circuit can serve either as a voltage-to-current converter or as a variable-gain current mirror.

capacitance. Amplifier IC_3 clamps the voltage at the source of Q_1 and the bottom of R_6 at 3V. With no signal input, therefore, Q_1 passes a constant quiescent bias current of 3 mA into the 3-mA constant-current sink involving IC_4 and Q_2. The output current of the circuit, which comes from the drains of Q_1 and Q_2, is zero. When V_{IN} assumes a level ΔV_{IN} above ground, the voltage at the top of R_6 increases by the same amount. So the current through R_6 and, thus, the output current, I_{OUT}, increases by an amount $\Delta V_{IN}/R_6$, equivalent to 1 mA/V.

This circuit differs from the traditional precision current-source topology (**Figure 2**) in that, the op amp in **Figure 1** clamps the *bottom* end of the sense resistor at a *constant* voltage rather than being varied in response to the input signal. Instead, the voltage at the *top* end, which would normally be connected to a fixed voltage, varies in response to the input signal. Furthermore, because Q_1 is always conducting, its gate-voltage variations are typically less than 200 mV in response to changes in V_{IN}. The result is that no nasty current spikes transfer to the output via Q_1's gate-channel capacitance when V_{IN} makes a step to or from zero. In a traditional circuit, because there is no current sink, the op amp must completely turn off the FET when the output current must be zero. In doing so, the op amp's output slews several volts to saturation near its positive supply rail, transferring a high-amplitude current spike onto the output. A spike of the opposite polarity and similar magnitude is created when the op amp has to recover from saturation and slew in the opposite direction to again turn on the FET.

The 3-mA constant-current sink comprises amplifier IC_4 and n-channel MOSFET Q_2. IC_4 clamps the voltage at the top of current-sense resistor R_7 at −3V. Because the voltage-reference circuit fixes the bottom of R_7 at −6V, the quiescent current through Q_2 remains steady at 3 mA, equal to the current through Q_1 when V_{IN} is zero. When V_{IN} assumes a level ΔV_{IN} below ground, the voltage at the top of R_6 decreases by the same amount; the current through Q_1 then falls below 3 mA; and the current

Figure 2



This topology represents a traditional voltage-controlled current source.

sink obtains the balance of its current, $\Delta V_{IN}/R_6$, from the load.

The −6V reference that fixes the bottom of R_7 derives from amplifier IC_5's applying a nominal gain of −2 to the 3V reference. You should trim the −6V reference by means of R_{V1}, such that the output current is zero in the absence of an input signal; the quiescent currents in Q_1 and Q_2 are then equal. Note that this single adjustment entirely calibrates the signal path, canceling out the effects of resistor tolerance, amplifier dc errors, and any tolerance in the ±3V references but not the effects of finite open-loop gain. To ensure maximum bandwidth in the signal path, the amplifiers are AD8055-ARs from Analog Devices (www.analog.com). These amplifiers can tolerate a total supply voltage of only 10V, so you must operate IC_1 from a split ±5V supply and IC_2 and IC_3 from a single-ended 10V supply, because their inputs are 3V above ground.

You can obtain optimum dc accuracy and stability by using an OP177GS amplifier for IC_4 and IC_5 and a high-quality reference IC, such as the AD780BR, for generating the 3V reference. You generate the −3V reference by applying a fixed gain of −1 to the 3V, using an inverting circuit similar to that used in **Figure 1** for deriving the −6V reference. You should use 0.1% tolerance resistors where shown, and you can optionally include R_{12} to provide 0.11% of additional gain to compensate for the finite open-loop gain of amplifiers IC_1 and IC_2. You can further optimize the dc stability by including R_{15} and R_{16}, although the prototype does not use these resistors. In tests, without C_9, the bandwidth of the circuit with a 1V peak-to-peak sinusoidal input was 80 MHz when the circuit drove a resistive 100Ω load. The output rise and fall times with the same load and a 1V, 2.5-nsec input step are just 5.5 and 4.8 nsec, respectively, with no overshoot, as measured with a 500-MHz oscilloscope. The typical output compliance ranged from 1.7V to −2.8V. The maximum undistorted output-current swing extended from +2.1 to −2.1 mA.

For optimum frequency response and linearity, you should use the circuit to drive a virtual-ground load; in other words, you should use a high-bandwidth op amp configured as an current-to-voltage converter. If you use any other load, which must have low impedance in any case, and it is partly capacitive, you may need a small capacitor, C_9, across R_5 to optimize the overall transient response of the circuit at the expense of some speed. You can also configure the circuit to operate as a current-to-current converter with an overall gain of 0.1 mA/mA by omitting R_1, replacing R_2 and R_{13} with 0Ω, and increasing the value of R_{12} to 470 kΩ. You can use this configuration, for example, to scale the outputs from commercial current-steering DACs that typically have full-scale outputs in excess of those that ASIC inputs need. Thus, you could test an ASIC with current-driven inputs by using such a circuit between each input and each DAC output. Note that, in this configuration, amplifier IC_1 is configured as a current-to-voltage converter with a gain of 0.1V/mA and presents a virtual-ground to the DAC outputs, a load that normally ensures optimum linearity performance from the DACs. The circuit supports both current-sourcing and current-sinking DACs, because the circuit can source as well as sink current. For high-speed operation, you may need a small capacitor across R_3 to cancel the effect of the DAC's output capacitance and any stray capacitance.

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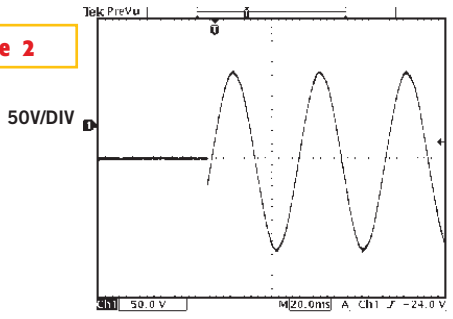
Chip recorder customizes phone ringer

Don Schelle and Ted Salazar, Maxim Integrated Products, Sunnyvale, CA

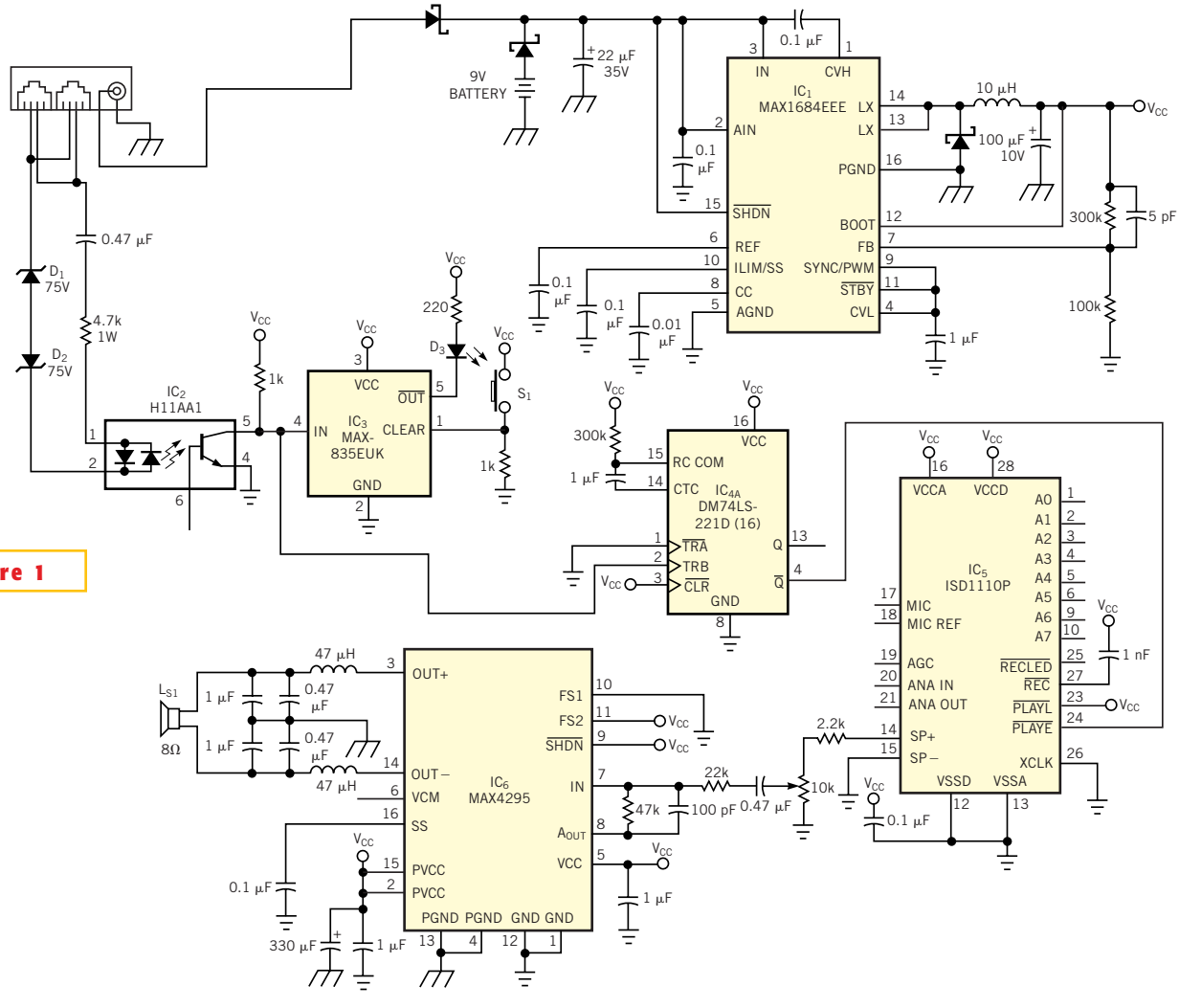
Companies usually purchase one type of telephone for all employees, which is understandable, especially if they obtain a discount for buying in quantity. One ringer sound for everyone can pose a problem, though, if the sound of a ringing phone makes a dozen people pause and look at their telephones. Equally annoying is the absence of a visual message indicator. Obliging everyone who suspects they may have a message to lift the handset and listen for a special message tone is far from ideal. By placing a circuit in series with the telephone, you can customize a phone ringer without modifying the phone (**Figure 1**). The heart of the ringer is a chip-recorder IC, IC_5, which can play as much as 10 seconds of telephone-quality recorded sound.

Figure 2



The ringer signal of a typical telephone exceeds 200V p-p.

Figure 1



This circuit plays as much as 10 seconds of recorded sound in place of the ring from a telephone. It also indicates when someone has called.

A high-efficiency stepdown converter, IC_1, allows the circuitry to operate from a supply voltage of 5 to 14V.

An optocoupler and associated front-end circuitry monitor the line, sensing when the line receives a high-voltage ringer signal (**Figure 2**). Zener diodes D_1 and D_2 prevent the on-hook voltage from activating the optocoupler. Comparator IC_3 latches LED D_3 on when a call is received, and a pushbutton switch, S_1, clears the comparator. The circuit shown in **Figure 3** records as much as 10 seconds of sound in the chip recorder's proprietary multilevel EEPROM. A switch-mode, Class D audio amplifier, IC_6, maintains high efficiency and delivers adequate power to an 8Ω speaker; even a PC speaker will work.

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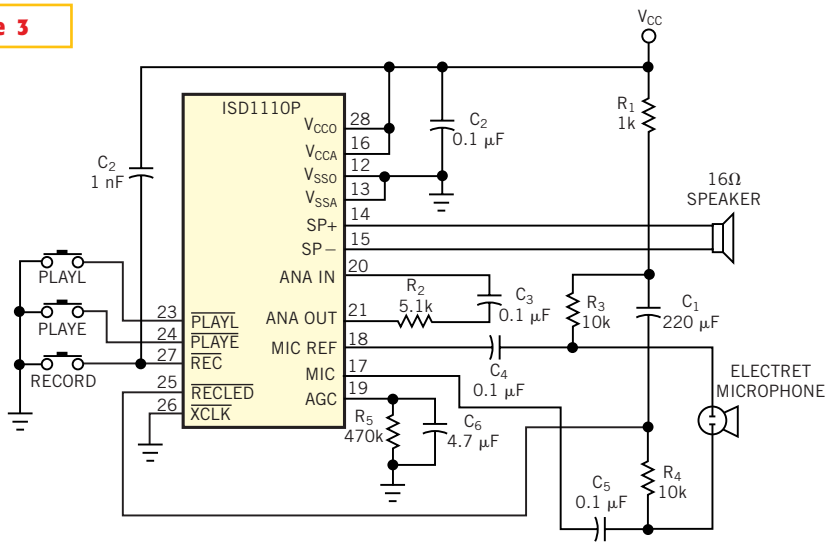
Figure 3



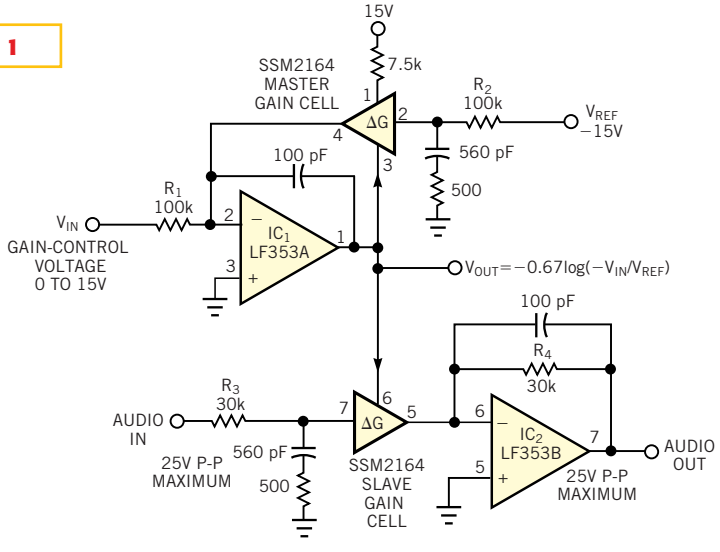
Using the EEPROM internal to IC_5 in Figure 1, this circuit records as much as 10 seconds of sound.

Op amp linearizes attenuator control response

Mike Irwin, Shawville, PQ, Canada

Professional-audio equipment commonly uses Analog Devices' (www.analog.com) high-performance, quad-voltage-controlled SSM2164 attenuator. The control response is −30 dB/V, with 0V producing unity gain. Attenuation increases as the applied control voltage increases in the positive direction. The circuit in **Figure 1** extends the range of applications for this versatile chip by providing a simple means of linearizing the control response. The result is an amplifier with gain directly proportional to the control voltage. In addition, the circuit also functions as a simple logarithm generator. You can use a single SSM2164 to make two high-quality, linear voltage-controlled amplifiers using this method. The four gain cells in the SSM2164 are tightly matched, current-in, current-out transconductance multipliers. The control response of each gain cell is: gain = $10^{(-V/0.67)}$. The cells are noninverting structures.

Figure 1



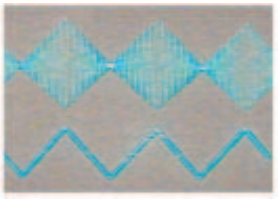
You can obtain both a gain-controlled output and a logarithmic output using this configuration.

Each voltage-controlled amplifier uses two gain cells. A "master" cell in the feedback loop of an op amp generates a logarithmic voltage output in response to a linear voltage input. This log voltage then goes to the control pin of the second

(matching) "slave" cell, which processes the audio signal. Op amp IC_1 maintains its inverting input at virtual ground by servo-controlling the gain of the master SSM2164 cell, which connects to the negative reference voltage. The output of IC_1 is a logarithmic function of the input: $V_{OUT} = -0.67\log[(-V_{IN}R_2)/(V_{REF}R_1)]$. V_{IN} is the gain-control voltage, and V_{REF} is the negative reference voltage. V_{OUT} then drives the control pin of the slave cell. Substituting the expression for V_{OUT} for V in the expression for gain yields the following: $\text{gain} = (V_{IN}R_2)/(V_{REF}R_1)$, which is the desired linear response.

Op amp IC_2 converts the slave cell's output current to an audio voltage with a gain of R_4/R_3. The overall expression for the gain is: $\text{gain} = (V_{IN}R_2R_{4)}/(V_{REF}R_1R_3)$. If $R_1 = R_2$ and $R_3 = R_4$, the expression reduces to: $\text{gain} = V_{IN}/V_{REF}$, and gain (in decibels) $= 20\log(V_{IN}/V_{REF})$. Setting V_{IN} to 15V and V_{REF} to −15V produces unity gain with the indicated component values. The gain decreases smoothly to −70 to −80 dB as the control voltage decreases (**Figure 2**). The voltage-controlled amplifier then shuts off completely (attenuation = 100 dB) when the control voltage drops to within a few millivolts of 0V. Negative voltages make the output of IC_1 swing close to the positive rail, but IC_1 promptly comes off the rail when the control voltage returns to the 0 to 15V range. The circuit produces no audible clicks and works well at lower supply voltages, such as ±5V.

Figure 2



The lower trace is a 0 to 3V triangle wave, which you use to modulate the 10-kHz sine wave in the upper trace. Note the linear modulation envelope.

For best performance, IC_1 should be a low-offset, low-input-current unit, and IC_2 should be a high-quality, low-noise audio op amp. However, you can obtain reasonably good performance with inexpensive op amps, such as the TL072 and LF353. The prototype unit achieved a control range of 75 to 80 dB, using an OP-290 for IC_1. The control-voltage feedthrough on the audio output is minimal, varying 10 to 20 mV when you sweep the gain through a 70-dB range. The noise and distortion performance is excellent, because the design uses the gain cells in the standard configuration in the SSM2164 data sheet.

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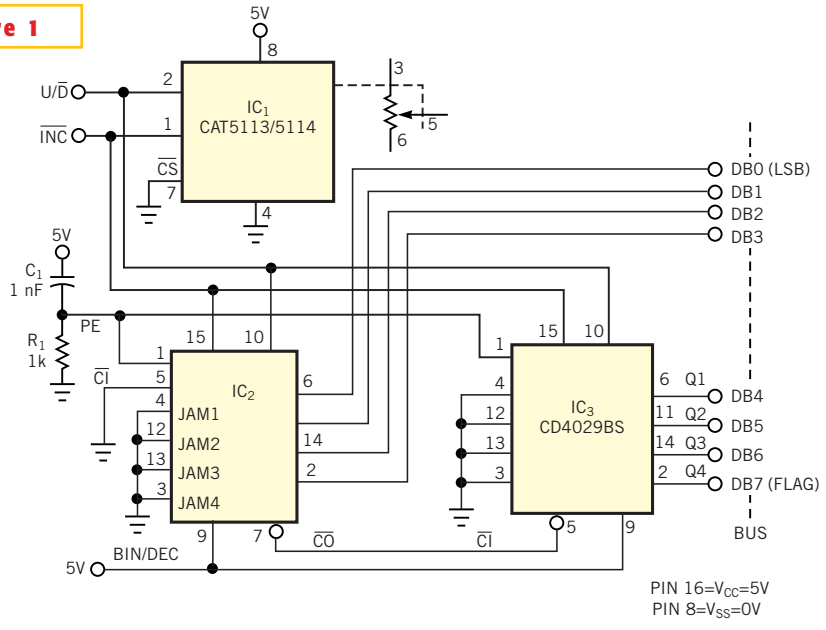
design ideas

Edited by Bill Travis

Where is the wiper?

Chuck Wojslaw and Dave Gillooly, Catalyst Semiconductor, Sunnyvale, CA

Figure 1



Two up/down counters keep track of a digitally programmable potentiometer's wiper position.

You enjoy significant advantages when using DPPs (digitally programmable potentiometers) with increment/decrement serial interfaces. Programming the serial interface is simple and fast, and you can adjust the potentiometer in real-time applications. The interface, however, provides no information about wiper position, and this information is important in some applications. If, for example, you use the potentiometer to control a parameter in a closed-loop, real-time application, the data reflecting the final wiper settings can be valuable in evaluating both the product performance and the circuit design. The circuit in **Figure 1** keeps a digital record of the DPP's wiper position by using two presettable CD4029 up/down counters, IC_2 and IC_3. The counters monitor the control signals $\overline{INC}$ and U/$\overline{D}$ of the DPP, IC_1.

During power-up, the wiper assumes position $(00)_{10}$, which it takes from previously programmed nonvolatile memory. Also during power-up, R_1 and C_1 differentiate the 5V power supply; this differentiated signal serves to preset the binary counters to $(0000\ 0000)_2$. Thus, the DPP and the external IC_2/IC_3 counters are at the same point after power-up. The level-sensitive up/down signal establishes the direction of movement of the DPP's wiper and the direction of the count. The edge-sensitive $\overline{INC}$ signal advances both the wiper and the counter. The $\overline{INC}$ pin of the DPP responds to negative-edge triggering, and the clock input of the counter responds to positive-edge triggering. If the signal driving the $\overline{INC}$ line is a pulse (a common occurrence), the two inputs are compatible.

The Q outputs of the counters (DB0 to DB7) indicate in binary notation the location of the wiper. You can use the same circuit, using two counters, for DPPs having as many as 256 taps. The DPP does not "wrap around" when the wiper advances to its upper or lower limit. The counters, however, do wrap around. To identify the case in which the digital counter is not in synch with the DPP, you can use the MSBs of the counters as flags. DB7 can serve as a flag for the 32-tap CAT5114 and the 100-tap CAT5113. You can change the initial count during power-up to something other than zero by preprogramming the DPP and setting high and low levels on the JAM inputs of the digital counters to the desired value.

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PLD code creates PWM generators

Clive Bolton, Bolton Engineering Inc, Melrose, MA

The PLD (programmable-logic-device) code in **Listing 1** creates arbitrary-resolution, pulse-width-modulated (PWM) generators. PWM generators are useful as low-bandwidth D/A converters in hardware of microprocessor-based systems. When you pass it through a simple RC lowpass filter, a PWM waveform becomes a voltage that's approximately equal to the PWM duty cycle times the supply voltage. In practical systems, the driving hardware is imperfect, so the minimum value is never zero, and the maximum value never equals the positive-voltage rail.

The software module in **Listing 1** automatically generates the required hardware from two compile-time parameters: PWM_WIDTH and AVALUE. PWM_WIDTH sets the number of possible steps in the PWM comparison. For example, 6 bits yields 2^6, or 64, steps. AVALUE sets the value at which the PWM initializes upon power-up or reset (set to one-half scale in the example in **Listing 1**).

The module has two major sections: a holding register, which stores the PWM value, and a counter, which generates the PWM waveform. You can update the holding register independently of the PWM counter. The holding register's value automatically strobes into the PWM counter when the counter overflows. The module takes the CLOCK, ACLR, ENABLE, WRITE, and DATA[PWM_WIDTH-1..0] inputs. CLOCK is the master system clock; all signals other than ACLR must be synchronous with the clock's rising edge. ACLR initializes the hardware to the power-up state and loads AVALUE into the holding register. When ENABLE=0, the PWM output becomes 0 (off); when ENABLE=1, the PWM generator produces the PWM waveform at the Q output. Asserting WRITE for one clock cycle strobes the data presented on DATA[PWM_WIDTH-1..0] into the holding register. The PLD code uses Altera's (www.altera.com) AHDL high-level design language; you can directly compile the code

LISTING 1—AHDL CODE FOR PWM GENERATOR

```
INCLUDE "LPM_COUNTER.INC";
INCLUDE "LPM_COMPARE.INC";
INCLUDE "LPM_FF.INC";

PARAMETERS
(
      PWM_WIDTH         = 6,        -- Bits (set to 6 for testing)
      AVALUE                  = B"100000" -- Async reset value
);

SUBDESIGN pwm
(
      clock                         :     INPUT;
      aclr                          :     INPUT;
      enable                              :     INPUT = VCC;            -- zeros
PWM output
      write                         :     INPUT;            -- writes into
holding register

      data[PWM_WIDTH-1..0]    :     INPUT;
      q                               :     OUTPUT;

--    period_pulse                  :     OUTPUT;           -- for debug and ext
sync
--    cout                          :     OUTPUT;

)
VARIABLE
      pwm                           :     LPM_COUNTER WITH (LPM_WIDTH =
PWM_WIDTH,
                                                              LPM_DIRECTION
= "DOWN");
      cntr                    :     LPM_COUNTER WITH (LPM_WIDTH = PWM_WIDTH,
                                                              LPM_DIRECTION
= "DOWN");
      pwm_ff                        :     SRFF;
      pwm_reg                       :     LPM_FF WITH (LPM_WIDTH = PWM_WIDTH,
LPM_AVALUE = AVALUE);
      pwm_precut              :     NODE;
      period_pulse                  :     NODE;       -- for debug and ext sync
      cout                          :     NODE;

BEGIN

      ASSERT
            REPORT "PWM_WIDTH: %" PWM_WIDTH
            SEVERITY INFO;

      % PWM Holding Register %
      pwm_reg.clock     = clock;
      pwm_reg.aset      = aclr;
      pwm_reg.enable    = write;
      pwm_reg.data[]    = data[];

      % PWM Counter %
      cntr.clock  = clock;
      cntr.aclr   = aclr;
      cntr.cnt_en = enable;
      period_pulse = DFF(cntr.cout, clock, !aclr, VCC);

      % PWM Counter %
      pwm.clock   = clock;
      pwm.aclr    = aclr;
      pwm.sload   = cntr.cout;
      pwm.data[]  = pwm_reg.q[];
      pwm.cnt_en  = enable;
      cout = pwm.cout;

      % PWM Output F/F %
      pwm_ff.clk  = clock;
      pwm_ff.clrn = !aclr;
      pwm_ff.s    = !cout AND period_pulse;     -- turn FF on at beginning of
interval
      pwm_ff.r    = cout OR !enable;      -- turn off at carry overflow.
      pwm_precut  = pwm_ff.q;


      q     = DFF(enable AND pwm_precut,
                                          clock, !aclr, VCC);
END;
```

into any of Altera's PLDs. Using an EP1K10TC100-3 PLD, a design with parameters set to the default values in **Listing 1** operates as fast as 139 MHz. Although we wrote the code for Altera's devices, you can readily translate the design structure and flow into VHDL or Verilog. You can download **Listing 1** from the Web version of this Design Idea at www.edn.com.

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Square-wave modulator has variable frequency and pulse width

Michael Fisch, Agere Systems, Longmont, CO

A few years ago, I worked at a disk-drive company. We had a plating facility that required square waves to drive the high-voltage plating operation. The challenge was that the square wave's pulse width had to be variable, along with the duty cycle. Also, the amplitude of the pulses had to be adjustable. The circuit in **Figure 1** satisfies all these criteria. The circuit delivers a unipolar (adjustable from 0 to 12V) pulse with adjustable frequency and pulse width. The first half of a dual, retriggerable monostable multivibrator, IC_{1A}, generates the frequency of the pulse train. The 100-kΩ potentiometer, R_1, along with R_2 and C_1, sets the adjustable frequency. R_3, R_4, and C_2 set the adjustable pulse width in the second section of the multivibrator, IC_{1B}. The ac-coupled op amp, IC_{2A}, running open-loop, delivers a ±12V pulse output. D_1 and D_2 clamp the negative-going excursions of the pulse train to ground. The other half of the op amp, IC_{2B}, serves as a level shifter that allows amplitude control over the range 0 to 12V. You can modulate the amplitude at low frequency by varying the amplitude-control voltage.

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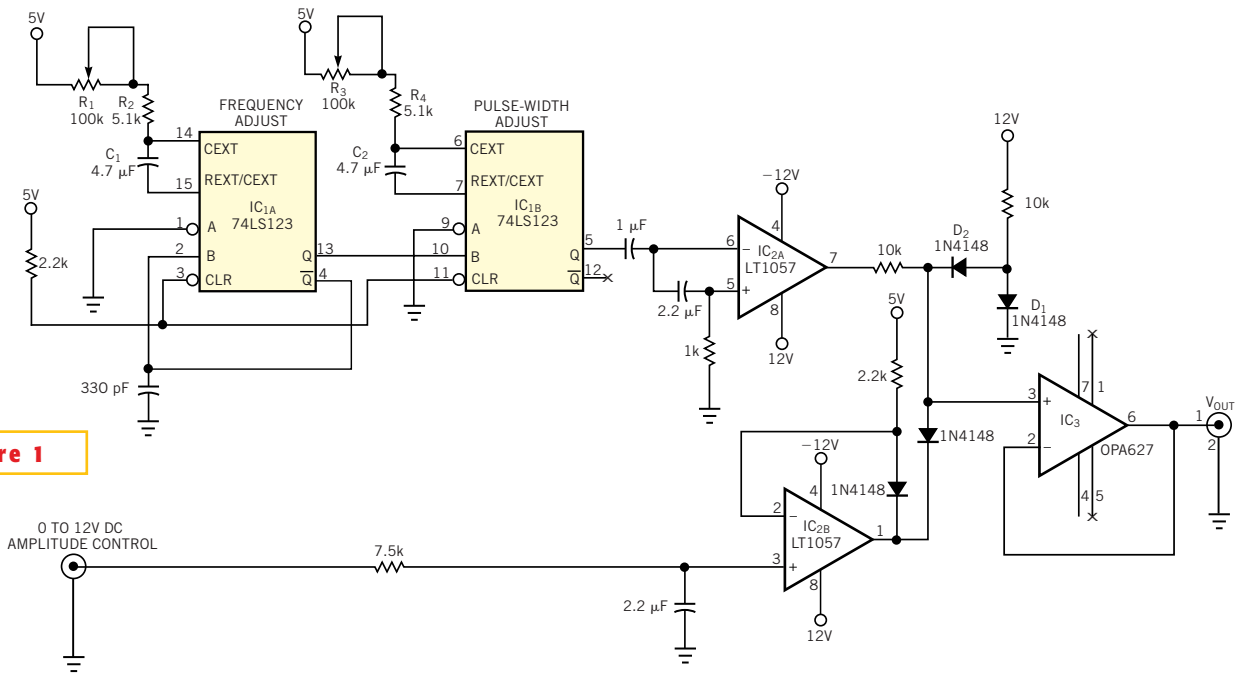


Figure 1

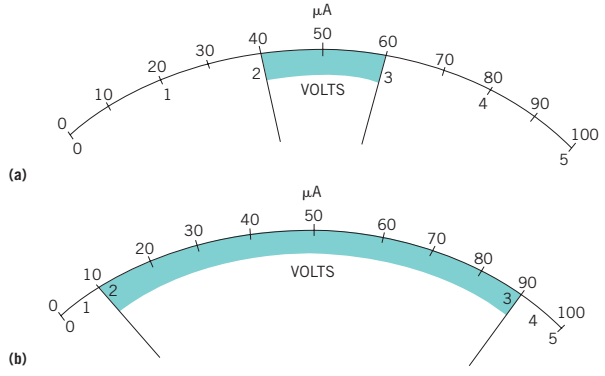
This variable-frequency circuit allows amplitude modulation of its pulse-train output.

Expanded-scale indicator revisited

Abel Raynus, Armatron International Inc, Melrose, MA

THE VISUALIZATION AID that a previous Design Idea describes allows only the expansion of the upper end of the scale (**Reference 1**). But what can you do if, according to your project requirements, you need to expand the middle region of the scale? **Figure 1a** illustrates the challenge. A voltmeter comprises a 100-μA dc meter and a series resistor. The voltage under test, V_{TEST}, ranges from 0 to 5V. The voltage changes between 2 and 3V (the "green zone") are of interest. But at the same time, you cannot ignore the voltages from 0 to 2V and from 3 to 5V, and you need to be able to observe these voltages. With a linear scale, the green zone consumes only 20% of the full-scale range. Your objective is to expand this zone to 80%, leaving 10% at the lower end and 10% at the upper end of the scale (**Figure 1b**). The circuit in **Figure 2** solves the problem. The window comparator, IC_1, controls the variable impedance of the voltmeter. Analog switches S_1 and S_2 provide a contact-logic AND function and put resistor R_2 in parallel with R_1 only upon closure of both switches. This closure occurs when V_{TEST} is between the threshold voltages V_{T1} and V_{T2} (**Figure 3**). You can calculate the resistor values as follows:

Figure 1



In a, the 2 to 3V "green zone" occupies only 20% of the scale; in b, this zone expands to 80%.

$$R_1=\frac{2V}{10\,\mu A}=200k\Omega;$$

$$R_1\|R_2=\frac{3-2V}{90-10\,\mu A}=12.5k\Omega;$$

$$R_2=\frac{R_1\bullet R_1\|R_2}{R_1-R_1\|R_2}=\frac{200\bullet 12.5}{200-12.5}=13.3\,k\Omega.$$

You can calculate resistors R_3, R_4, and R_5 from the equations for the threshold voltages:

$$V_{T1}=\frac{R_5}{R_3+R_4+R_5}V_{CC};$$

$$V_{T2}=\frac{R_4+R_5}{R_3+R_4+R_5}V_{CC}.$$

In this case, $V_{CC}=5V$, $V_{T1}=2V$, $V_{T2}=3V$; hence, $R_3=R_5=200\,k\Omega$, and $R_4=100\,k\Omega$.

REFERENCE

1. Raynus, Abel, "Indicator features expanded scale'" *EDN*, Feb 21, 2002, pg 86.

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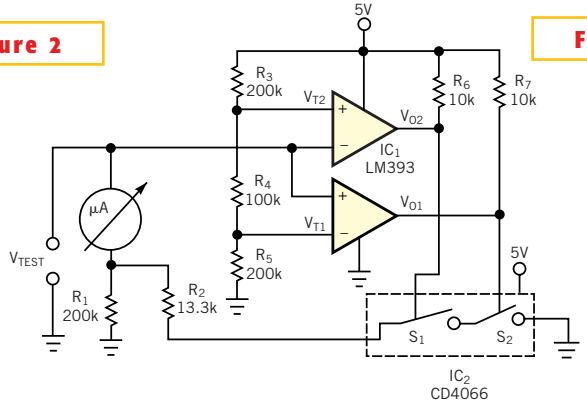
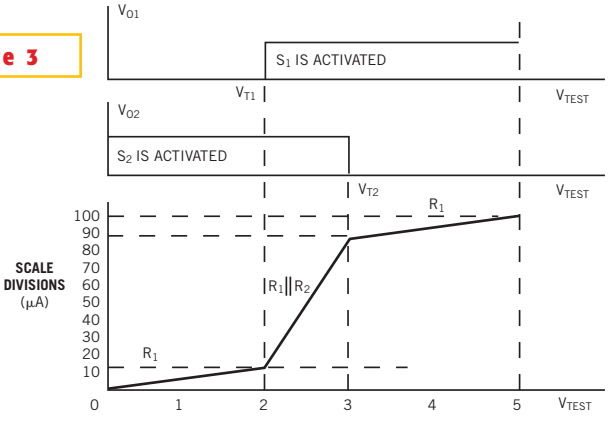
Figure 2



A window comparator and two analog switches collaborate to expand the green zone in Figure 1.

Figure 3



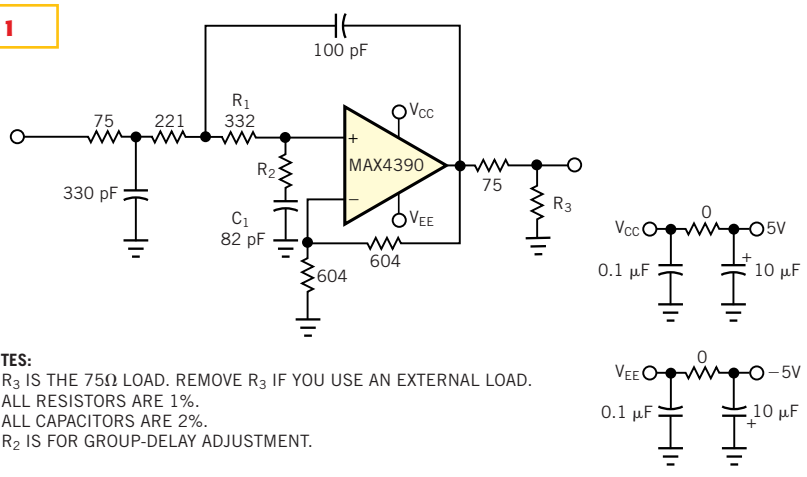
Within the thresholds of the window comparator, R_2 connects in parallel with R_1 to expand the scale of the voltmeter.

Butterworth filter has adjustable group delay

William Stutz, Maxim Integrated Products, Sunnyvale, CA

THE SALLEN-KEY REALIZATION of a 5.25-MHz, three-pole Butterworth filter has a gain of 2V/V and can drive 75Ω back-terminated coax with an overall gain of 1 (**Figure 1**). Used to reconstruct component-video (Y, Pb, Pr) and RGB signals, this filter has an insertion loss greater than 20 db at 13.5 MHz and greater than 40 db at 27 MHz (**Figure 2**). Like the antialiasing filter before an ADC, this filter removes the higher frequency replicas of a signal following a DAC. To preserve quality in the video waveform, you should minimize group-delay variations in the filter and any group-delay differential between filters. That requirement mandates a means for adjusting the filter's group delay without affecting its bandwidth. In **Figure 1**, the addition of R_2 in series with C_1 and R_1 creates a lag-lead network.

Figure 1

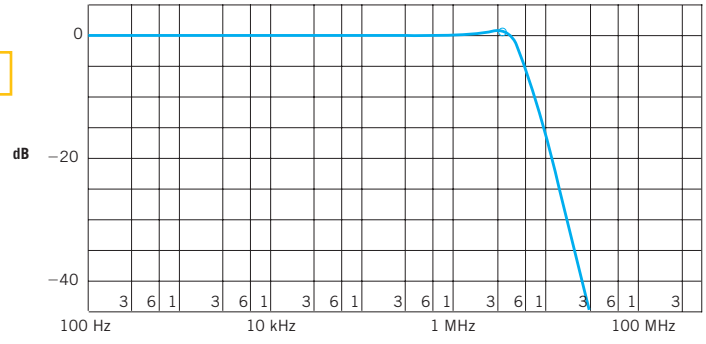


NOTES:
1. R_3 IS THE 75Ω LOAD. REMOVE R_3 IF YOU USE AN EXTERNAL LOAD.
2. ALL RESISTORS ARE 1%.
3. ALL CAPACITORS ARE 2%.
4. R_2 IS FOR GROUP-DELAY ADJUSTMENT.

This three-pole Butterworth video-reconstruction filter has adjustable group delay.

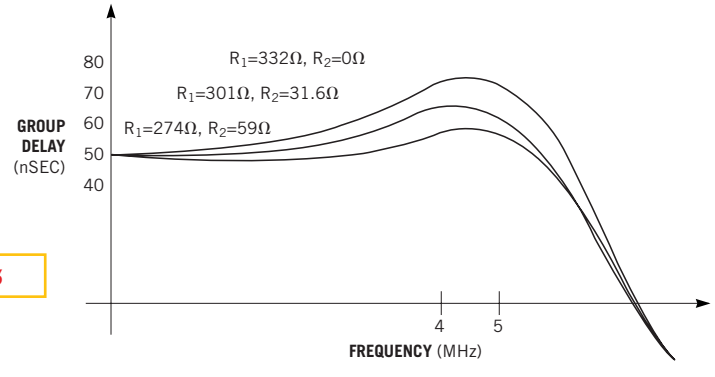
Keeping the sum of R_1 and R_2 constant and equal to the original R_1 value preserves bandwidth by preserving the dominant-pole frequency. Increasing the R_1 value, on the other hand, introduces a "lead" term that lowers group delay by reducing the rate of change in phase. For $R_2=0\Omega$ and $R_1=332\Omega$ in the circuit shown, the average group-delay variation over the filter bandwidth is about 25 nsec. Raising R_2 to 31.6Ω and lowering R_1 to 301Ω decreases the variation to approximately 15 nsec, and setting $R_2=59\Omega$ with $R_1=274\Omega$ decreases it to approximately 7 nsec. The last case has a less-than 0.5-dB effect on band-edge selectivity but does not change the filter's 3-dB bandwidth (**Figure 3**).

Figure 2



The typical filter response for the circuit of Figure 1 is $R_1+R_2=332\Omega$.

Figure 3



Selected values of R_1 and R_2 allow control of group-delay variation over the filter's passband.

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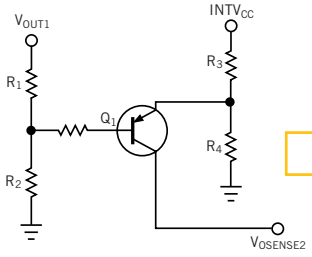
Single transistor sequences multiple supplies

David Chen, Linear Technology Corp, Milpitas, CA

Many DSP chips, microprocessors, FPGAs, and ASICs require multiple power supplies that must deliver different voltages in a specific start-up sequence. Out-of-sequence voltages can cause excessive input current, logic errors, or even device failure. To sequence different supplies, a common approach is to regulate a lower voltage from a higher voltage using a linear regulator. Another approach is to use a series of Schottky diodes. Although simple in concept, these approaches can be expensive and difficult to implement in applications that require more than two power supplies. **Figure 1** shows a simple, low-cost approach that requires only one pnp transistor to provide the necessary logic. **Figure 2** shows a dual power supply that uses the described circuitry to sequence the outputs.

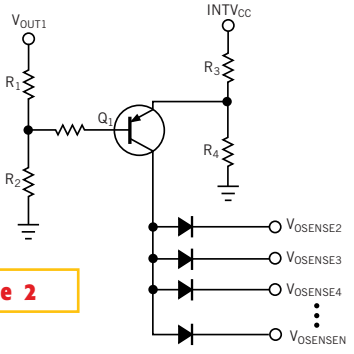
When V_{OUT1} is low, $V_{OSENSE2}$, the voltage

Figure 1



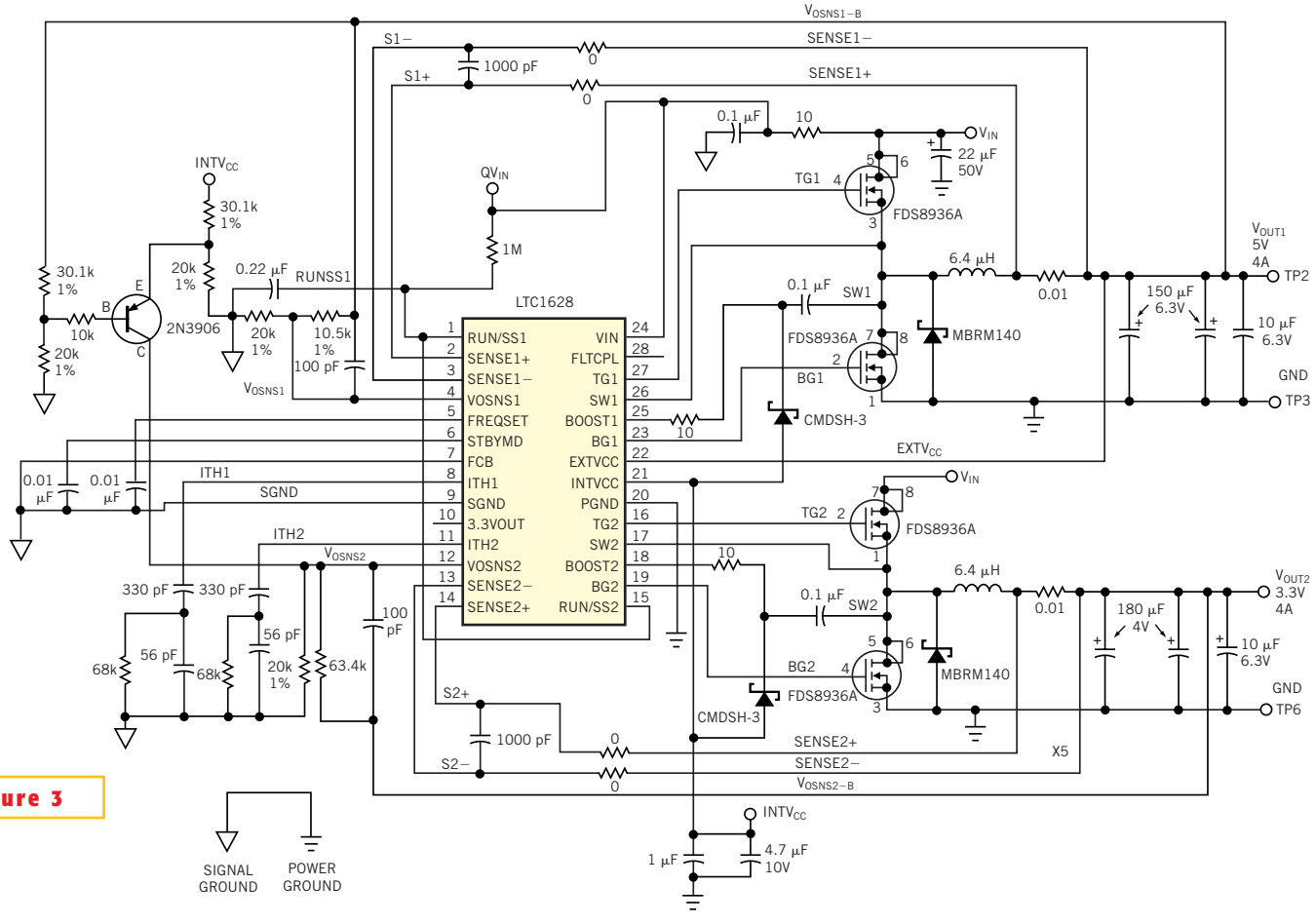
A simple one-transistor circuit synchronizes two outputs.

Figure 2



You can obtain multiple-output sequencing by adding ORing diodes.

Figure 3



This dual-output supply uses the simple circuit in Figure 1.

feedback for V_{OUT2}, goes high, and the second supply, V_{OUT2}, shuts off (**Figure 3**). When V_{OUT1} approaches its nominal level, Q_1 turns off. Q_1 then relinquishes control of $V_{OSENSE2}$, and V_{OUT2} resumes its normal start-up process. The process is similar for power-down sequencing. When V_{OUT1} is high, V_{OUT2} operates normally. When V_{OUT1} goes from high to low, $V_{OSENSE2}$ goes high and shuts off V_{OUT2}. More specifically, R_3 and R_4 set the clamping voltage for the $V_{OSENSE2}$ pin when V_{OUT1} is low, and R_1 and R_2 determine the V_{OUT1} voltage level at which Q_1 turns off. In cases of multiple supplies, you need only add ORing diodes at the collector of Q_1 (**Figure 3**). The design uses an LTC1628 dual-output controller. You can see the sequenced-output waveforms in **Figures 4a** (at turn-on) and **4b** (at turn-off).

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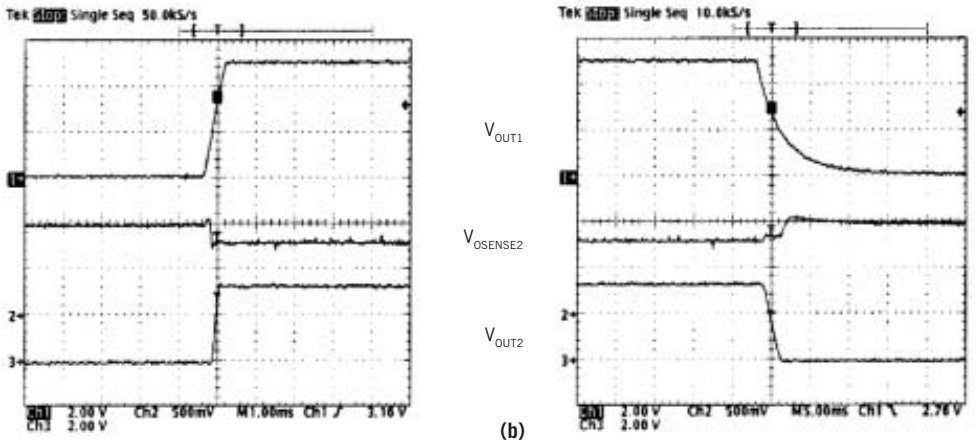
Figure 4



These supply-voltage waveforms occur at turn-on (a) and turn-off (b).

Edited by Bill Travis

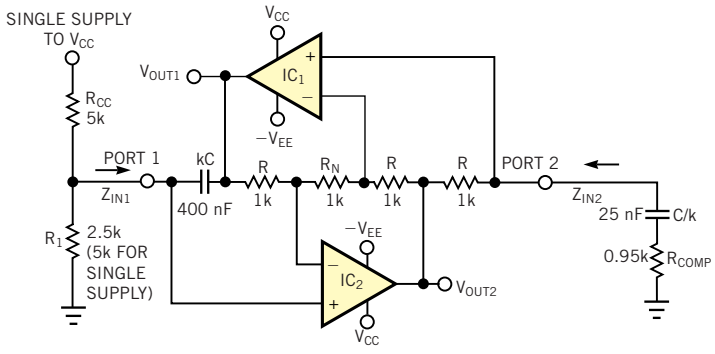
GIC resonator has inherent amplitude control

Lutz von Wangenheim, University of Applied Sciences, Bremen, Germany

THE CIRCUIT IN **Figure 1** is based on a classic GIC (generalized impedance converter). The sine-wave-oscillator circuit has inherent amplitude stabilization and normally operates from dual power supplies. However, if you connect an additional resistor, R_{CC}, to V_{CC}, you can operate the circuit with one supply (with $V_{EE}=0V$). You can adjust the oscillation frequency by varying R_1. R_{COMP} ensures oscillation and does not affect the oscillation frequency. The remaining passive components are four equal-value resistors, R, and two capacitors, kC and C/k, where k is a scaling factor. This modification of the classic GIC structure incorporates an additional resistor, R_N, between both inverting op-amp inputs. The GIC topology has excellent high-frequency properties and thus finds extensive use in active-filter circuits. The GIC structure can simulate a grounded inductance or a grounded FDNR (frequency-dependent negative resistance).

You can explain the function of the circuit by starting with the GIC input impedance at either Port 1 or Port 2. A straightforward analysis of the circuit yields the input impedance at Port 1:

Figure 1



A GIC-based resonator provides inherent amplitude control and low distortion.

$$Z_{IN1} = -\frac{1}{\omega^2 C^2 R} - \frac{1}{j\omega kC}\left(\frac{R_N}{R} - \frac{R_{COMP}}{R}\right).$$

Note that, for $R_{COMP}=R_N$, the expression for Z_{IN1} represents the input impedance of an ideal FDNR. The FDNR, together with an ohmic shunt resistance from Port 1 to ground, forms a tuned circuit with the inherent capability to oscillate. In reality, however, the oscillation would die out because of parasitics arising from lossy capacitors and imperfect amplifiers. The circuit in **Figure 1** compensates for these losses by using the second portion of Z_{IN1}, representing a negative capacitance for $R_{COMP}<R_N$. In practice, you should choose $R_N=R$ and a resistor ratio, R_{COMP}/R, close to unity (for example, $R_{COMP}/R=0.95$ to 0.98). If you perform the analysis at Port 2 of the circuit, the input impedance, Z_{IN2}, represents an ideal inductance in series with a negative resistor. Shunting this impedance with a capacitor-resistor branch (C/k and R_{COMP} in **Figure 1**) creates a lossless LC tank circuit. This tank circuit can oscillate if you satisfy the condition $R_{COMP}<R$. The circuit starts reliably and oscillates at the following frequency:

$$f_0 = \frac{1}{2\pi C\sqrt{RR_0}}.$$

For the circuit values in **Figure 1**, IC_2 saturates, providing a clipped sinusoidal signal at V_{OUT2}. V_{OUT1} is a filtered version of that signal. Thus, no extra circuitry is necessary for amplitude stabilization. However, the quality of the sinusoidal signal at V_{OUT1} depends on the Q factor of the resonator circuit, as the following equation states:

$$Q = \frac{k \bullet \sqrt{RR_0}}{R_N - R_{COMP}}.$$

For the values shown, a quality factor $Q>100$ results with a capacitance scaling factor $k=4$, $C=100$ nF, and $(R_N - R_{COMP})=50\Omega$. V_{OUT1} provides a signal with a total harmonic distortion lower than 1% at $f_0=1$ kHz. The peak-to-peak amplitude of the sinusoidal signal is approximately 1V lower than the total supply-voltage span.

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Three parts provide tenfold increase in switcher current

Wayne Rewinkel, National Semiconductor, Sunnyvale, CA

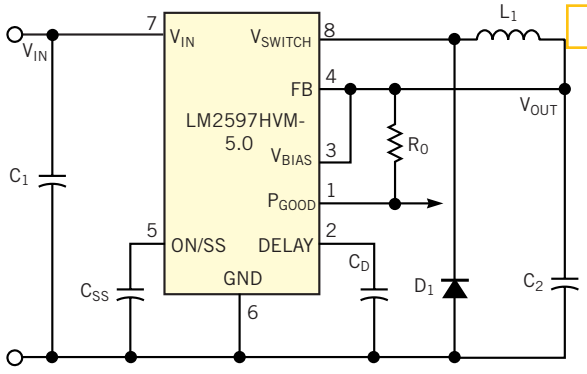
Industrial-control circuits often derive their power from widely varying sources that can exceed the 40V maximum rating of popular switching ICs. This Design Idea presents a simple, flexible, and inexpensive buck switcher that converts an input voltage as high as 60V to 5V at several amps. The circuit is unique in that it boosts current with almost no compromise in performance, size, or cost. It should be of interest to anyone who has ever searched for a simple step-down switcher with an output current or input voltage exceeding that of off-the-shelf devices. Such a search usually entails a far more complex and costly solution than the one this Design Idea presents. National Semiconductor's (www.national.com) LM2594HV and LM2597HV both feature 60V maximum input, 150-kHz operation, 0.7A peak output, and on/off capability. The 2597 adds soft start, delay, a power-good flag, and a pin you can use to bootstrap most of its bias current from V_{OUT}. Although both devices are single-chip switchers, you can also use them as driver-controllers with only slight modifications to their standard buck-regulator circuit configurations. **Figure 1** shows the 2597HVM in a typical 5V, 0.5A configuration that uses all the IC's features. **Figure 2** shows the higher current configuration with only three additional components to boost output current to more than 6A.

As a bonus, the circuit in **Figure 2** also provides overcurrent and short-circuit protection for Q_1. The rugged self-protection features of the IC also apply to Q_1, provided that the transistor has sufficient heat sinking; L_1 stays out of saturation if you select R_1 properly. If the peak current in R_1 produces a voltage drop large enough to cause Q_1 to saturate, then the IC experiences an overcurrent condition, causing its internal protection modes either to disable the switch for the remainder of the pulse period or to skip pulses. Q_1 needs to be a fast switch to minimize switching losses. The transistor also needs to have minimal storage time to avoid pulse skipping at low duty cycles. **Table 1** shows circuit performance at its maximum input voltage, 60V, under a variety of output conditions. The **table** also includes component values and ratings necessary to select sources for L_1, C_1, and C_2.

Efficiency for test conditions of V_{IN}=60V and I_{OUT}=2 to 6A measures 77% for V_{OUT}=5V and rises to 87% for V_{OUT}=12V. Efficiency is highest for the V_{IN} range of 30 to 40V, where its peak is 2% higher than the values in **Table 1**. Power dissipation is almost evenly divided among L_1, D_1, and Q_1, so you should space these components to avoid hot spots and provide heat-sinking for as much as 3W each at maximum current and voltage. A good layout should include lots of ground plane and short, wide traces on high-current paths. Output voltages other than 3.3, 5, and 12V are also available by substituting the adjustable version of the 2597. This IC requires an added resistor pair from V_{OUT} to the FB pin to ground. Calculate resistor-divider values to set the FB pin at 1.23V for the desired output voltage. Although this design example uses the LM2597HVM-5.0, you can easily apply this current-boost technique using only three additional parts to any of National's second-generation buck devices, effectively extending their output-current capability more than tenfold. You need not use HV devices for applications with a maximum input voltage lower than 40V. The following seven steps provide a simplified procedure to select component values for a wide range of operating conditions, including those that **Table 1** lists:

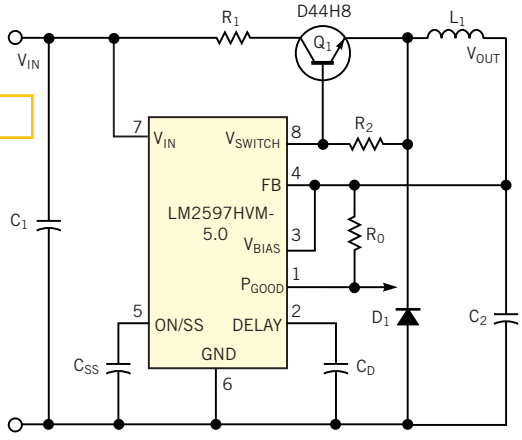
1. Choose R_1 to drop 1.5V at the inductor's peak operating current of I_{OUT}+20%. A higher current peak can

Figure 1



This classic buck-regulator circuit efficiently steps down voltage.

Figure 2



You can increase output current more than tenfold with the addition of only three components.

TABLE 1–EFFICIENCY VERSUS OUTPUT VOLTAGE AND CURRENT

Efficiency (%)	V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	R_1 (Ω)	R_1 (W)	R_2 (Ω)	Q_1 D4448	D_1 (V at A)	L_1 (µH)	L_1 ESR (Ω)	L_1 LSAT (A)	C_1 (µF)	C_1 ESR (Ω)	C_2 RMS (A)	C_2 (µF)	C_2 ESR (Ω)	C_2 RMS (A)
77	60	5	1	1	0.06	4.7	D4448	60/1	68	0.13	1.2	100	0.22	0.5	100	0.22	0.12
78	60	5	2	0.5	0.15	4.7	D4448	60/3	47	0.086	2.4	220	0.11	1	220	0.11	0.2
77	60	5	4	0.33	0.5	4.7	D4448	60/6	34=68×2	0.065	4.8	470	0.065	1.8	470	0.065	0.3
77	60	5	6	0.22	0.7	4.7	D4448	60/6	20=10×2	0.056	7.2	680	0.047	2	680	0.047	0.6
85	60	12	1	1	0.16	4.7	D4448	60/1	150	0.25	1.2	100	0.22	0.6	100	0.22	0.11
86	60	12	2	0.5	0.42	4.7	D4448	60/3	94=47×2	0.17	2.4	220	0.11	1	220	0.11	0.2
87	60	12	4	0.33	1.5	4.7	D4448	60/6	DMT2-79	0.07	4.8	470	0.065	1.7	470	0.065	0.25
88	60	12	6	0.22	2	4.7	D4448	60/6	DMT2-47	0.04	7.2	680	0.047	2.4	680	0.047	0.4

force Q_1 to saturate, causing the IC to deliver base current in excess of 0.7A to Q_1. This action triggers the IC's pulse-by-pulse current limit and protects the IC, Q_1, and the load from further excessive current. An output short circuit causes the IC to reduce its clock frequency, protecting D_1 and L_1 from high continuous peak current. The power dissipated in R_1, which can be a significant part of the total loss, subtracts from the dissipation in Q_1, allowing for a smaller heat-sink requirement. This dissipation is:

$$R_1(I_{OUT})(I_{OUT})(V_{OUT}/V_{IN}).$$

2. Choose R_2 to be small enough to quickly turn off Q_1 but not so small that it diverts much needed drive current away from Q_1 and causes early current limit. A value of 4.7Ω (the value that **Table 1** uses) is a good trade-off value for most applications.

3. Choose Q_1 to be a fast switch with V_{CE} rating greater than 60V and I_{CE} rating of two times the desired current peak. This ratio generally provides a high beta over the working-current range. The D44H8 works well to more than 6A output in a TO-220 package and more than 2A in an SOT-223 package.

4. Choose D_1 to be a Schottky diode rated for the maximum values of V_{IN} and I_{OUT}. D_1 dissipates much of the total power loss when $V_{IN} >> V_{OUT}$, so look for a diode rated at less than 0.5V forward drop.

5. Choose $L_1 = 47\ \mu H/\sqrt{I_{OUT}}$ for V_{OUT}=3.3V, $68\ \mu H/\sqrt{I_{OUT}}$ for V_{OUT}=5V and $150\ \mu H/\sqrt{I_{OUT}}$ for V_{OUT}=12V. Choose the nearest L_1 value with a saturation and working current rating greater than I_{OUT}. Coilcraft's (www.coilcraft.com) SMT DO5022 family works well for output current to 1 or 2A, but you need larger cores for currents greater than 3A. You can tie these SMT inductors in series or in parallel to extend their use to 3 to 4A. They're also available in stacked-core versions for higher current use. Through-hole inductors, such as Coilcraft's DMT2-xx family, are physically larger but provide lower losses, especially for output current greater than 5A.

6. Choose C_1 for ripple-current rating and C_2 for low ESR. A minimum capacitance value for $C_1 = C_2/10 \geq 100\ \mu F \times I_{OUT}$ works well at low current, but, as current rises to several amps, you need larger values to meet ESR and ripple-current requirements. Ripple-current rating depends on several variables, but a conservative choice is half the maximum output current for C_1 and one-fourth the maximum output current for C_2. High ripple-current capability may require paralleling several capacitors for C_1. Select C_2 to have ESR less than $0.1\Omega / I_{OUT}$ to keep the V_{OUT} peak-to-peak ripple less than 50 mV. Choose capacitors by looking at those targeting high-temperature use in switching power supplies with published ESR and ripple current ratings. Then, select a voltage rating higher by at least 50% than the expected operating voltage.

7. R_0, C_{SS}, and C_D are optional. You can leave these pins open if you don't intend to use them. You can shut off the circuit by pulling Pin 5 low and then turn it on again with soft-start by allowing Pin 5 to float high. Refer to the 2597 data-sheet graphs for C_{SS} and C_D values necessary to set the desired soft-start and power-good flag delay times.

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IC maintains uniform bias for GaAs MESFETs

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

The gate-turn-on threshold voltage for GaAs MESFETs (gallium-arsenide metal-semiconductor field-effect transistors) varies considerably from part to part, even within a given lot. That behavior makes biasing difficult, especially if you want to design the device into a high-volume product. To overcome this drawback, you can introduce a current sensor that monitors the bias current and provides feedback to the gate input (**Figure 1**). IC_1 combines a current sensor and an error amplifier. Intended as a power-control IC for power amplifiers, it senses the drain-source current, I_{DS}, at the source; compares and integrates the difference between voltage drops across R_{SENSE} and R_{G1}; and feeds back an output voltage to the MESFET gate. The feedback adjusts I_{DS} until the two voltage drops are equal, thereby achieving uniform source current, regardless of the MESFET's gate-threshold characteristics. The expression for drain-source current is:

$$I_{DS}=\frac{V_{PC}\bullet R_{G1}}{4\bullet R_{G3}\bullet R_{SENSE}}.$$

Figure 1

Current through R_{G1} depends on a voltage, V_{PC}, with respect to the negative supply, V_{EE}, applied to the power-control input at Pin 4. You can implement V_{PC} with a voltage divider, a reference, or a variable-voltage source. Because the gate voltage is negative with respect to the source, you must modify IC_1's supply voltage to ensure a negative gate drive for the MESFET: Connect the V_{CC} pin to ground and the ground pin to V_{EE}. You can easily modify this uniform-bias circuit for biasing bipolar transistors and MOSFETs, as well.

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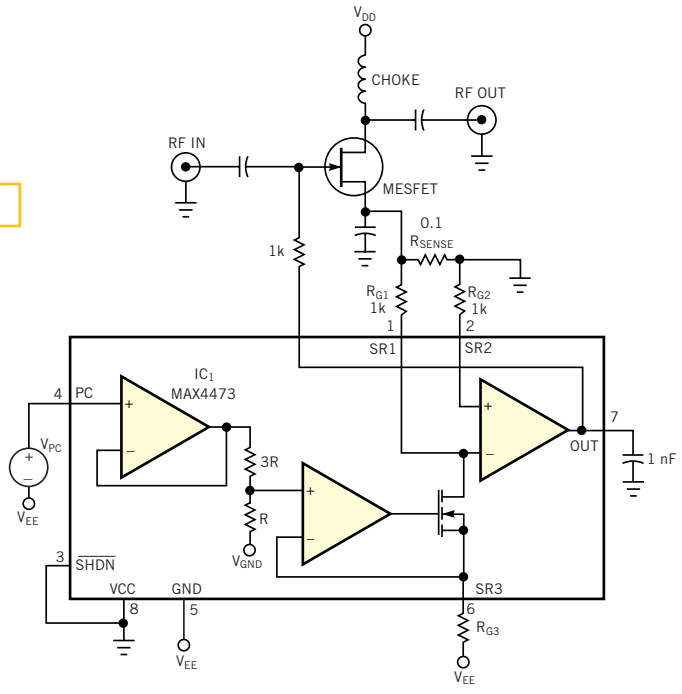


A smart-bias IC ensures uniform bias for GaAs FETS in high-volume products.

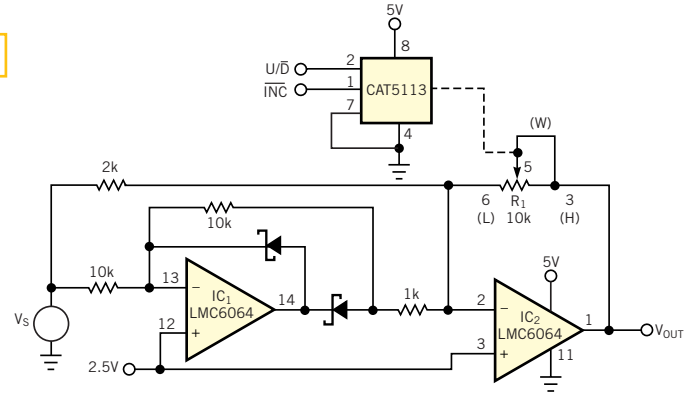
Add gain to an absolute-value amplifier

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

THE ABSOLUTE-VALUE AMPLIFIER is a basic building block in test-and-measurement and signal-processing applications. The addition of a DPP (digitally programmable potentiometer) adds another dimension, G (gain), to this key circuit. Because the gain is programmable, you can use the circuit as an absolute-value amplifier (G>1) or an absolute-value attenuator (G<1). The single-supply circuit in **Figure 1** comprises IC_1, which is an inverting amplifier for positive-polarity signals only, and IC_2, the summing amplifier. For the summing amplifier, R_1 represents a programmable, variable resistance. This resistance is modeled as $pR_2=p(10\ k\Omega)$, where p varies from 0 to 1/99 to 99/99 and represents the relative wiper setting from one end of the potentiometer (0) to the other end (1). For input voltages above the reference, for example, $V_S>2.5V$ and for voltages below the reference, $V_S<2.5V$, $V_{OUT}=2.5V+|p5V_S|=2.5V+|GV_S|$.

The potentiometer, a Catalyst 5113, has 100 taps and an increment/decrement interface. For this DPP, the circuit gain varies from 5/99 to 5. The measured accuracy of the circuit is approximately 1% for moderate values of gain (0.5 to 4) and for a characterized end-to-end resistance, R_{POT}. During power-up, the wiper goes to its stored value in nonvolatile memory. This stored value establishes the default value of the gain after power-up. The basic idea for this absolute-value circuit came from **Reference 1**.

Figure 1



Attenuate or amplify with this variable-gain absolute-value circuit.

REFERENCE

1. Cipri, Teno, "Absolute-value comparator touts accuracy, size," *EDN*, March 7, 2002, pg 124.

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Use a PIC for automatic baud-rate detection

Ross Fosler, Microchip Technology, Chandler, AZ

AUTOMATIC BAUD-RATE DETECTION is desirable in many applications. Microchip's (www.microchip.com) standard USART module that the company embeds in most of its PIC microcontrollers lends itself to a simple and easily implemented automatic baud-detection scheme. The PIC18FXX2 data sheet defines the following baud rate in bits per second:

$$X = \frac{F_{OSC}}{16 \times B} - 1;\ B = \frac{F_{OSC}}{16(X+1)}, \quad (1)$$

where X is the value for the baud-rate generator and F_{OSC} is the input clock frequency.

Figure 1 represents a general-case signal typically seen on the RX pin of a PIC microcontroller. The time, p, is the number of instruction cycles from the end of the start bit to the beginning of the stop bit. This definition allows you to relate baud rate, B, to the total time it takes for the RX pin on the microcontroller to see eight bits of data. Eight is a convenient figure for a binary machine. Basically,

$$p = \frac{8}{B}\frac{F_{OSC}}{4};\ B = \frac{2F_{OSC}}{p}. \quad (2)$$

The term $(F_{OSC}/4)$ is the instruction rate of a PIC microcontroller. The term 8/B is the eight bit-times that the RX pin sees. Relating the two baud-rate equations,

$$B = \frac{2F_{OSC}}{p} = \frac{F_{OSC}}{16\,(X+1)};\ X = \frac{p}{32} - 1. \quad (3)$$

The simplified result leads to a simple equation that you can easily implement on a PIC microcontroller. Count the total numbers of instruction cycles for eight bit-times. Divide the result by 32. (In other words, shift the count right five times.) Add a rounding bit. Then, decrement the value by one. Finally, load the SPBRG register with the result to synchronize the PIC microcontroller to the incoming baud rate. It is important to select the right control signal so that the microcontroller samples the correct number of bits. For this implementation, the signal

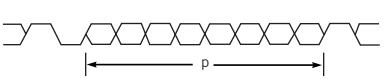

Figure 1 This bit stream is a general-case signal typically appearing on the RX pin of a PIC microcontroller.

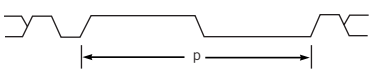

Figure 2 For the baud-rate-detection scheme, this waveform represents an ideal control signal.

in **Figure 2** is an ideal control signal. You take measurements from the rising edge, and the pulse is symmetric. **Figure 3** shows the simplified program flow for the baud-rate detection.

It is useful to know the valid frequency range for a baud rate, SPBRG value, and tolerable error. The following **equation** defines error as follows:

$$E(B_C) = \frac{B_C - B}{B}, \quad (4)$$

where B is the desired baud rate and B_C is the calculated or actual baud rate. Substituting **Equation 1** for B_C and using algebra leads to the following result:

$$F_{OSC} = (E+1)(X+1)(16)(B). \quad (5)$$

E is the error used to determine the maximum and minimum frequencies for a chosen baud rate and SPBRG value. For example, a good value for E would be 62%. Evaluating **Equation 5** for the high and low limits of error E yields a valid oscillator operating range. For most SPBRG values, common baud rates, and the most common clock frequencies, operating ranges overlap each other from one SPBRG to the next. Thus, the automatic baud-detection scheme synchronizes with the source for most of the common conditions. However, some errors and clock frequencies never have a valid SPBRG (X) value.

To approach this problem, you must compare the maximum frequency for an SPBRG value with the minimum frequency of the next SPBRG. The value at which they're equal is the border between continuous and discontinuous operation for any given input frequency. The following two equations express this equality and the continuity barrier:

$$(E_H+1)(X)(B)(16) = (E_L+1)(X+1)(16)(B). \quad (6)$$

$$X_{LOW} = \frac{(E_L+1)}{(E_H+1)-(E_L+1)}. \quad (7)$$

Thus, for any given frequency and a defined error, the automatic baud-detection scheme always generates a good SPBRG value if it is above X_{LOW}. Of course, you must select the frequency and baud rate such that SPBRG is less than or equal to 255, the largest value that SPBRG supports. For example, for a 2% error, the lowest SPBRG value before certain clock frequencies become a problem is 25. A bootloader is an excellent example of an application for this baud-rate-detection scheme. The simple implementation uses minimal resources. It synchronizes to a baud rate within one transmitted byte, and you can most likely successfully synchronize it to any standard baud rate, especially 9600 bps.

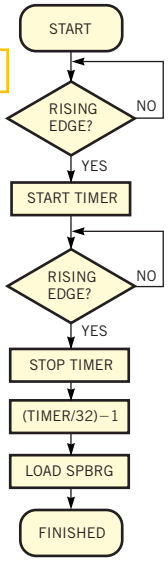

Figure 3 This program-flow diagram illustrates the principles of the baud-rate-detection technique.

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Design low-duty-cycle timer circuits

Phil Rogers, Texas Instruments Inc, Rockwall, TX

Designing astable circuits using the industry-standard 555 timer is a straightforward process when duty cycles are 50% or greater. However, you must overcome the many pitfalls of low-duty-cycle circuits to arrive at a desired result. Using only ideal components eases the design, but the components themselves are hard to obtain. Nonideal components get in the way of the easy-to-use standard equations and greatly multiply the tolerances. This Design Idea uses the TLC555 CMOS timer. You can use other versions of the popular 555 timer with appropriate variations in the given parameters. For a standard, greater-than-50%-duty-cycle, low-frequency design (**Figure 1**), you would use the following design equations:

$$t_H = C \bullet (R_A + R_B) \bullet \ln(2);$$

$$t_L = C \bullet R_B \bullet \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A + R_B)}{(R_A + 2R_B)}.$$

Charging current for the timing capacitor flows through R_A and R_B until the capacitor voltage reaches the upper threshold voltage of $0.667V_{CC}$. The capacitor then discharges through R_B and an internal transistor to the lower threshold voltage of $0.333V_{CC}$. Because R_B is present in both the charging and the discharging cycles, you can't implement duty cycles lower than 50% in this configuration. These idealized equations also ignore several factors that slightly degrade the results for the higher range of duty cycles but greatly influence the results of low-duty-cycle designs. These factors include propagation delays and the on-resistance of the internal discharge transistor. All these factors are supply-voltage-dependent. Another factor for low-duty-cycle designs that does not apply to high-duty-cycle designs is the effect of the R_B bypass diode, D_1 (**Figure 2**), required to implement the design.

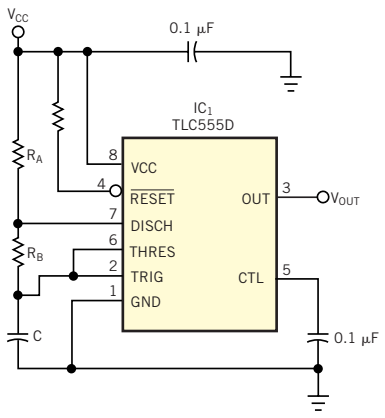

Figure 1 This classic 555-based timer is valid only for duty cycles greater than 50%.

Adding a bypass diode across R_B allows for designs with duty cycles lower than 50%. During the charging cycle, current flows through R_A and bypasses R_B through the diode. During discharge, current flows through R_B and the internal discharge transistor as usual. Because R_B is now present only in the discharge cycle, you can tailor the duty cycle to any desired point over the full range. Again, using ideal components, the timing equations are simple:

$$t_H = C \bullet R_A \bullet \ln(2);$$

$$t_L = C \bullet R_B \bullet \ln(2);$$

$$\text{DUTY CYCLE} = \frac{(R_A)}{(R_B)}.$$

The factors you must consider in obtaining a design that agrees with calculations include the:

- diode forward voltage,
- propagation delays,
- discharge-transistor on-resistance,
- ratio of R_A to on-resistance, and
- leakage resistance of the control-pin capacitor.

Diode forward voltage depends on the current flowing through the diode. This current can range from a few hundred microamps to tens of milliamps. For a fixed design, you can obtain this voltage from manufacturers' curves or actual measurements you make by applying the desired current through the diode. You can also use the diode equation:

$$I = I_S(e^{qV/kT} - 1).$$

Or, in terms of voltage:

$$V_F = \frac{1}{0.026} \bullet \ln\left(1 + \frac{I}{I_S}\right) = 38.46 \bullet \ln\left(1 + \frac{I}{I_S}\right).$$

This voltage subtracts from the charging voltage during the charging cycle and affects the charge-ramp time. Propagation-delay times from the THRES (threshold) and TRIG (trigger) inputs to DISCH (discharge) add directly to the period. These delays depend upon supply voltage. The formulas for the propagation delays (in nanoseconds) are:

$T_{PHL} = -0.0162V_{CC}^5 + 0.8207V_{CC}^4 - 16.205V_{CC}^3 + 155.62V_{CC}^2 - 31.88V_{CC} + 1558$; $T_{PLH} = -0.0102V_{CC}^5 + 0.5044V_{CC}^4 - 9.6825V_{CC}^3 + 89.622V_{CC}^2 - 401.04V_{CC} + 807.97$.

Discharge-transistor on-resistance also varies with supply voltage. This resistance affects the discharge current. Also, when you use low-value resistors for R_A (for low-duty-cycle designs), the combination of R_A and the on-resistance yields a voltage divider that affects the discharge voltage. The on-resistance formula for resistance in ohms is:

$$R_{ON} = 59.135V_{CC}^{-0.8101}.$$

Typically, you'd place a small capacitor on the control pin that connects to the upper internal-divider node. This capacitor has only a slight effect on the threshold-trigger voltages. The leakage resistance of the ceramic capacitor is approx-

imately 9 MΩ. This value is high but still accounts for approximately a 1.5% drop in the trigger voltages because of the 80-kΩ divider resistors that the window-comparator circuit uses. When you take all the cited parameters into account, the design equations become considerably more complicated:

$$t_H = C \bullet R_A \bullet \ln\left[(3 - e^{-t_{PHL}/(R_{ON} \bullet C)}) \bullet \left(\frac{2 \bullet V_{CC}}{(2 \bullet V_{CC} - 3 \bullet V_F)}\right)\right] + t_{PHL};$$

$$t_L = C \bullet (R_B + R_{ON}) \bullet \ln(3 - e^{-t_{PHL}/(C \bullet R_A)}) \bullet 2.38 \bullet \left(1 - \left[\frac{1 - \left(\frac{3 \bullet R_{ON}}{(R_A + R_{ON})}\right)}{2 - \left(\frac{3 \bullet R_{ON}}{(R_A + R_{ON})}\right)}\right]\right) + t_{PLH}.$$

These equations include all the known parameters to obtain a nominal design using the TLC555 timer. Tolerances in each of the parameters cause additional variations that you must consider. In addition, you must consider the effects of temperature variations. After you obtain all this knowledge, the simple 555 timer presents a major math problem. However, thanks to modern computers, you can eliminate much of this tedious math using an Excel spreadsheet. It shows the results of calculations both with and without the bypass diode and includes the tolerancing parameters. You can download the spreadsheet from the Web version of this Design Idea at www.edn.com.

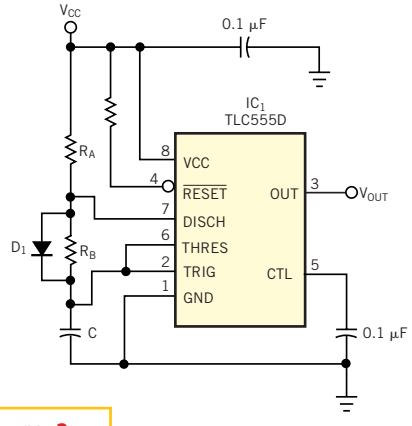

Figure 2

The simple addition of a bypass diode makes this timer circuit valid for low duty cycles.

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design ideas

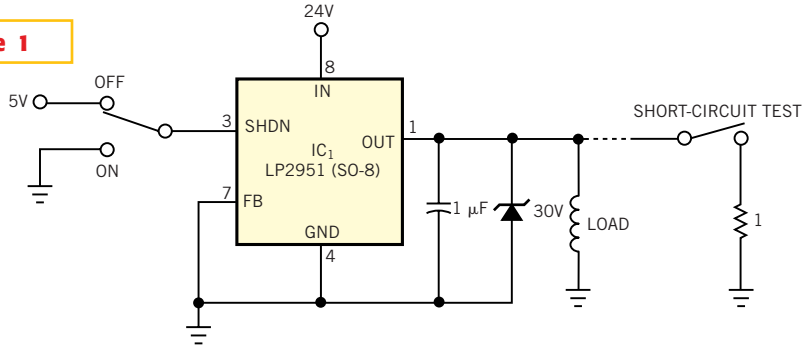
Edited by Bill Travis

High-side driver has fault protection

Carl Spearow, Tokyo Electron, Gilbert, AZ

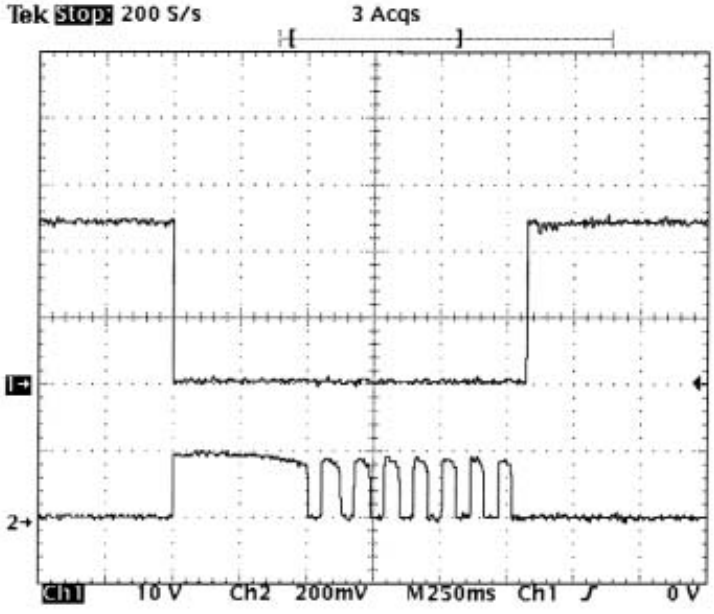
High-side drivers find common use in driving grounded solenoid coils and other loads. Short-circuit protection for such drivers is essential for avoiding damage from wiring faults and other causes. Polymer fuses are generally too slow, and discrete current-limiting circuits are large and cumbersome. The circuit in **Figure 1** uses a small, low-dropout linear regulator as a high-side switch and provides inherent current limiting and thermal shutdown. The regulator comes in an SO-8 package. The zener diode provides transient protection, and the output capacitor ensures stability of the circuit. The circuit can drive a 24V load at 100 mA. These are adequate specs for many solenoid valves, relay coils, and other moderate loads. During a short circuit, the regulator limits the current to 160 mA. This current causes the die to overheat and enter a thermal-shutdown state. Upon removal of the short circuit, the device cools down and resumes normal operation. The top trace in **Figure 2** is the output voltage during a 1.3-sec short circuit. The bottom trace is the short-circuit current, which limits itself at less than 200 mA. Note that the regulator goes into thermal shutdown after 500 msec, and the IC then toggles on and off until removal of the short circuit.

Figure 1



This simple high-side driver provides current limiting as well as transient protection.

Figure 2



In the bottom trace, the output current limits itself to 160 mA during a short circuit.

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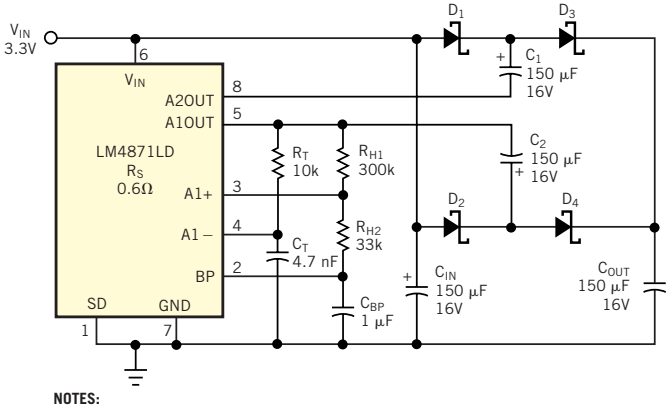
Boost 3.3V to 5V with tiny audio amplifier

Wayne Rewinkel, National Semiconductor, Santa Clara, CA

THIS CHARGE-PUMP CIRCUIT quietly converts a 3.3V source to 5V at 500 mA (**figures 1** and **2**). National's (www.national.com) LM4871LD power amplifier makes this design idea both possible and practical, thanks to its low output resistance, low cost, compact size, and high dissipation capability. Its output resistance has an average value of 0.6Ω: 0.5Ω to ground and 0.7Ω to V_{IN}. Because it is a CMOS IC, each output can swing to its rail, limited only by the resistance of the output transistor. The leadless lead-frame package has a footprint smaller than an SO-8 but provides a θ_{JA} of 56°C/W when soldered to a board with 1 sq in. of 1-oz copper exposed. This high thermal conductivity couples with low output resistance to allow the 4871 to continuously deliver nearly 1A from each of its two outputs while operating at its full rated ambient temperature of 85°C. Internal thermal shutdown protects the device from overloads, and a shutdown pin allows you to power down the device to less than 1 µA.

Figure 1



NOTES:
1. D_1 AND D_2: MBRS120T3.
2. C_1 AND C_2 ESR<11Ω.

You can use a tiny audio amplifier to boost 3.3V to 5V with respectable current capability.

Figure 2 shows the full circuit schematic, including the equivalent internal components. Amplifier IC_1 is configured as an RC oscillator similar to a 555 timer. R_T charges C_T to the voltage set by the resistor divider R_{H1} and R_{H2}, causing the amplifier to switch states, aided by the positive feedback from the R_H resistors. The remaining internal feedback and biasing resistors connected to IC_2 configure it as a simple inverter with bias at mid-supply. The amplifier outputs switch rail-to-rail out of phase with a 50% duty cycle at a frequency approximated by the following equation:

$$\frac{1}{f} = 4\ \mu SEC + \frac{4R_TC_T}{\left(\frac{R_{H1}+R_{H2}}{R_{H2}}\right)},$$

$$f = 44 \text{ TO } 53 \text{ kHz}.$$

You can calculate the output voltage across C_{OUT} from the following equation:

$$V_{OUT} = 2\left(V_{IN} - V_{DIODE} - I_{OUT}R_S - I_{OUT}(ESR) - I_{OUT}/Cf\right)$$
$$= 2(3.3 - 0.35 - 0.3 - 0.05 - 0.062) = 5.08V,$$

where I_{OUT} is the average output current, V_{DIODE} is the diode voltage drop at I_{OUT}, R_S is the source resistance of IC_1 and IC_2, ESR is that of C_1 and C_2, and C is the value of $C_1 = C_2$.

The following equation approximates the effective output resistance at the load:

$$R_{OUT} = 2\left(R_S + R_{DIODE} + ESR + 1/Cf\right) =$$
$$2(0.6 + 0.15 + 0.11 + 0.07) = 1.9\Omega.$$

Component values as shown in **Figure 1** provide a circuit that can produce 5V at 0.5A from a 3.3V source at a conversion efficiency of 78%. If necessary, you can obtain tighter regulation figures at slightly lower output current by adding a low-dropout linear regulator, such as the LP3961. At a 500-mA load it introduces a drop of only 150 mV. Its addition provides good line and load regulation over the range I_{OUT}=0 to 500 mA (**Figure 3**). You can also use the circuits of **figures 1** and **3** to provide 3.3V at 500 mA from a 2.5V source.

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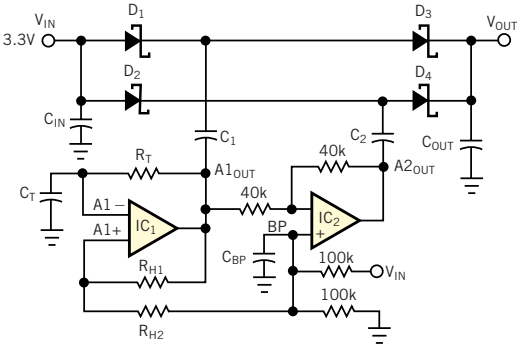
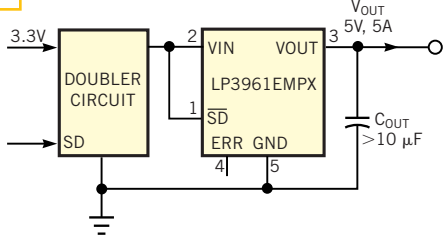
Figure 2



This equivalent circuit shows the innards of the LM4871LD audio amplifier.

Figure 3



You can tighten voltage-regulation specs in Figure 1's circuit by adding a linear regulator.

Add a signal-strength display to an FM-receiver IC

José Miguel-López, RF Center Ltd, Barcelona, Spain

The Philips (www.semiconductors.philips.com) TDA7000 integrates a monaural FM-radio receiver from the antenna connection to the audio output. External components include one tunable LC circuit for the local oscillator, a few capacitors, two resistors, and a potentiometer to control the variable-capacitance-diode tuning. The IC has an FLL (frequency-locked-loop) structure. The filtered output of the FM discriminator frequency-modulates the local oscillator to provide negative-feedback modulation. The result is compression of the signal at the output of the mixer. Thus, the IF bandpass filter and the FM discriminator deal with narrowband FM signals. For a compression factor of K=3, the original FM bandwidth reduces to 180/3=60 kHz. So, you need neither ceramic filters nor complex LC tank circuits to realize the IF filter. A simple active filter using op amps can fulfill the task. The IC incorporates a correlation muting system that suppresses interstation noise and spurious responses arising from detuning. The muting circuit uses a second mixer. Its output is available at Pin 1; you can use it to drive a detuning indicator. You can add a signal-strength display to the TDA7000 using the circuit in **Figure 1**.

You can obtain the information related to the intensity of the received signal at the output of the IF filter (IC_1, Pin 12). You can easily process this voltage with common op amps, because the IF signal is centered on 70 kHz. The voltage at Pin 12 is dc-coupled to an amplifier, IC_2. Next, an envelope detector, IC_3, yields a dc voltage proportional to the received-signal strength. The Siemens (www.siemens.com) TCA965 window discriminator, IC_4, compares this envelope voltage with a voltage derived from R_1, R_2, and R_3 for the window's center (and R_4 and R_5 for the window's half-width). Three LEDs show the result of the comparison (Low, OK, Good), but the display is valid only if the tuning is correct. If it's correct, the voltage at IC_1, Pin 1 reaches its maximum value, and the LM311 comparator, IC_5, enables the TCA965.

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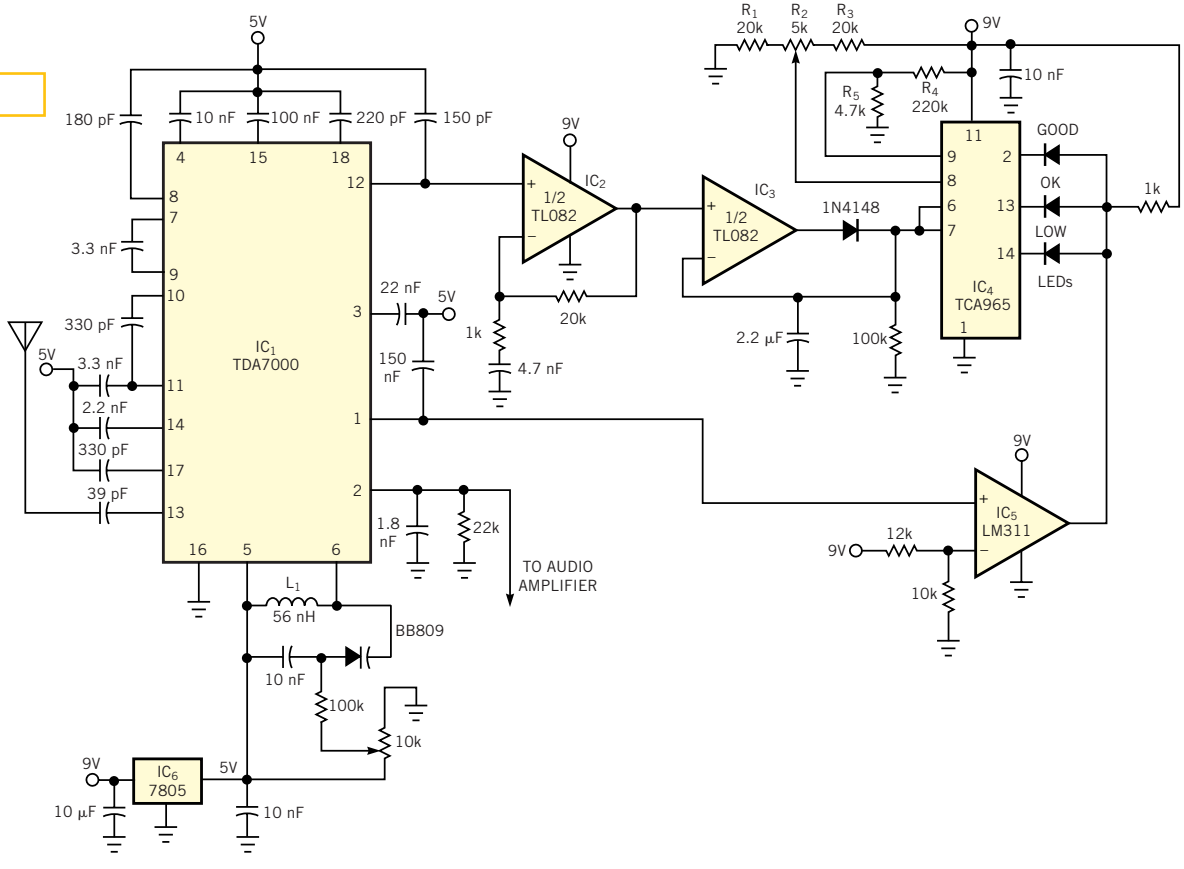
Figure 1



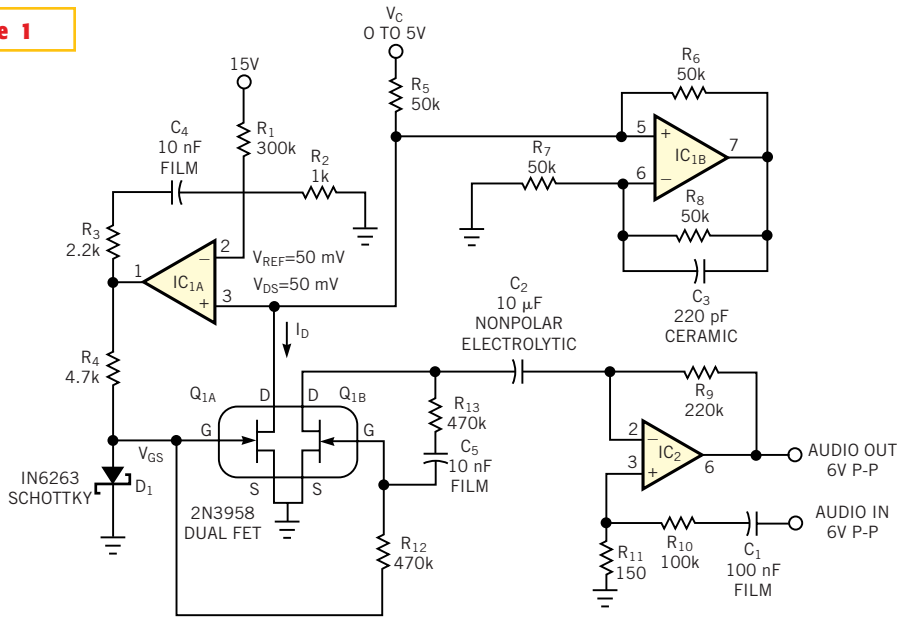
You can easily add a signal-strength indicator to the Philips TDA7000 FM-receiver IC.

Op amp linearizes response of FET VCA

Mike Irwin, Shawville, PQ, Canada

FETs find common use in VCAs (voltage-controlled amplifiers) and attenuators, in which the FET serves as a variable resistance. A control voltage applied to the gate sets the channel resistance and overall circuit gain. You frequently need to select individual FETs because of wide spreads in FET characteristics. The circuit in **Figure 1** uses a master-slave servo technique with a matched-FET pair to implement voltage-controlled variable gain. This gain is a linear function of the applied control voltage, V_C. In contrast with variable-gain circuits using a single FET as the gain-control element, the circuit in **Figure 1** exhibits minimum gain for V_C=0V and features a linear increase in gain with increasing V_C. The self-biasing operation of the circuit also compensates for unit-to-unit variations in the FET characteristics, thereby making device selection less critical.

Figure 1



This voltage-controlled amplifier has a dynamic range of −55 to 0 dB.

The circuit maintains the drain voltage, V_{DS}, of Q_{1A} at a low value (V_{REF}=50 mV) to ensure that the FET operates in the resistive region of its I_D versus V_{DS} characteristic curve. Op amp IC_{1A} servos the V_{GS} of Q_{1A} to maintain V_{DS} at V_{REF}, while Q_{1A} sinks the current from the Howland current source IC_{1B}. The sourced current is I_D(mA) =V_C/R_5(kΩ), where V_C is the control voltage. The channel resistance, R_D, in kilohms is then $R_D=V_{REF}/I_D=0.05/I_D=0.05\times R_5/V_C$. The same V_{GS} applies to Q_{1B} through R_{12}. Because Q_1 is a well-matched monolithic dual FET, Q_{1A} and Q_{1B} have identical channel resistance, R_D. V_{GS} varies from approximately 370 mV (which D_1 limits to prevent gate-source conduction) to V_P (approximately −1.7V for the 2N3958) as V_C varies from 0 to 5V. IC_2 is a variable-gain, noninverting amplifier, in which the controlled R_D of Q_{1B} sets the gain: Gain=$1+R_9/R_D=1+R_9/(V_{REF}\times R_5/V_C)$.

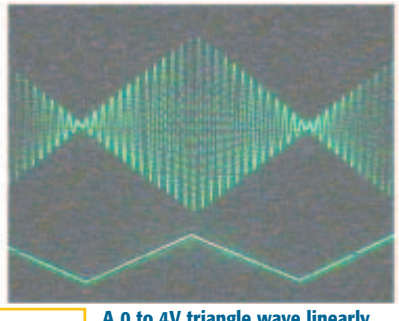


Figure 2 A 0 to 4V triangle wave linearly modulates the 500-Hz audio input.

The maximum gain is $1+R_9/R_0$. R_0 is the minimum channel resistance for V_{GS}=0V, approximately 450Ω for the 2N3958. The minimum gain is unity, when the FET does not conduct ($V_{GS}=V_{PINCHOFF}$). The circuit attenuates the audio-input signal level to lower than 10 mV p-p. This attenuation minimizes distortion in the FET and also sets the clipping level at the output of IC_2. R_{13} and C_5, in combination with R_{12}, reduce distortion at higher signal levels. With the values shown, the gain increases linearly from −55 to 0 dB as V_C varies from 0 to 5V. The circuit accepts a 6V p-p input signal. **Figure 2** shows the result of modulating a 500-Hz sine wave with a 0 to 4V triangle wave.

For best performance, IC_1 should be a low-offset, low-input-current unit, such as the OP-290. IC_2 should be a high-gain-bandwidth-product, low-noise amplifier, such as the NE5534. You can successfully use inexpensive units, such as the LF353 and LF351, at reduced gains. You can also operate the circuit from ±5V supplies (with R_1 changed to 100 kΩ), using an OP-290 for IC_1 and a TL031 for IC_2. The maximum supply current for ±5V operation is 0.33 mA, showing that low-power operation is possible.

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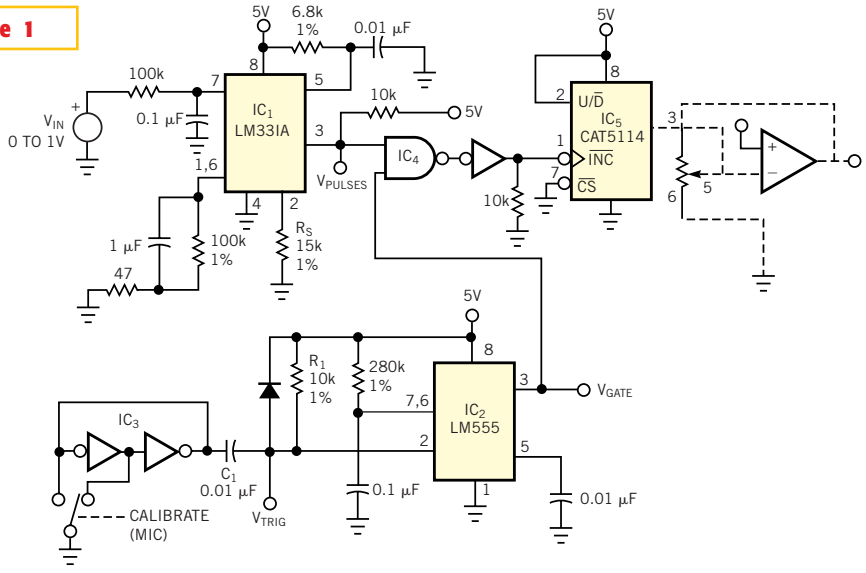
Convert voltage to potentiometer-wiper setting

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA, and Chris Wojslaw, Conexant Systems, Newport Beach, CA

THE CIRCUIT IN **Figure 1** converts an analog input voltage, V_{IN}, to a proportional wiper setting of a DPP (digitally programmable potentiometer). The potentiometer's wiper setting, which varies from position 0 through 31, corresponds to the input voltage, which varies from 0 to 1V dc. The CAT5114, IC_5, is a 32-tap potentiometer with an increment/decrement interface. V_{IN} typically models the output voltage of a sensor whose value sets a parameter of an analog circuit in the signal-processing portion of a system. The basic principle of the circuit is to convert the input voltage to a number of pulses and let each pulse advance the potentiometer's wiper within a certain period of time. IC_1 is a voltage-to-frequency converter. This circuit converts the 0 to 1V dc input voltage to an output frequency, V_{PULSES}, that varies from 0 to 1 kHz.

Figure 1



You can convert an analog voltage to a wiper setting in a digitally programmable potentiometer.

This free-running oscillator advances the wiper of the potentiometer for only 31 msec, established by V_{GATE} and the AND function of IC_4. V_{GATE} is the output of the one-shot multivibrator, IC_2. The one-shot receives its trigger from a calibrate switch or an external signal. The hex inverters of IC_3 debounce the calibrate switch. R_1C_1 differentiate the voltage-level shift generated by the switch to provide a nominal 100-µsec trigger, V_{TRIG}, to IC_2. V_{TRIG} could also be a processor-generated logic signal. The 31-msec gating signal is chosen to correspond to the highest tap position of the potentiometer at the highest frequency of the voltage-to-frequency converter. For a 100-tap potentiometer, the gating signal measures 99 msec for the same sensitivity of the voltage-to-frequency converter. You can trim the 15-kΩ resistor, R_S, to match the timing of the 331 converter to the pulse width of the 555.

Tap position 00 of the digitally controlled potentiometer is stored in the DPP's nonvolatile memory and the potentiometer's up/down control is set to up. When the DPP powers up, the IC recalls wiper setting 00 from nonvolatile memory. When you depress the calibrate switch, the wiper increments from 00 to a setting corresponding to the input voltage, V_{IN}. You can use the three-terminal resistive network of the potentiometer to control the gain of an amplifier (shown in broken lines in **Figure 1**), a parameter of a filter, or the coefficient of a mathematical operator.

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Make a DAC with a microcontroller's PWM timer

Mike Mitchell, Texas Instruments Inc

MANY EMBEDDED-microcontroller applications require generation of analog signals. An integrated or stand-alone DAC fills the role. However, you can often use PWM signals for generating the required analog signals. You can use PWM signals to create both dc and ac analog signals. This Design Idea shows how to use a PWM timer to simultaneously create a sinusoid, a ramp, and a dc voltage. A PWM signal is a digital signal with fixed frequency but varying duty cycle. If the duty cycle of the PWM signal varies with time and you filter the PWM signal, the output of the fil-

ter is an analog signal (**Figure 1**). If you build a PWM DAC in this manner, its resolution is equivalent to the resolution of the PWM signal you use to create the DAC. The PWM output signal requires a frequency that is equivalent to the update rate of the DAC, because each change in PWM duty cycle is the equivalent of one DAC sample. The frequency the PWM timer requires depends on the required PWM signal frequency and the desired resolution. The required frequency is $F_{CLOCK}=F_{PWM}\times 2^n$, where F_{CLOCK} is the required PWM-timer frequency, F_{PWM} is the PWM-signal frequency, and n is the desired DAC resolution in bits.

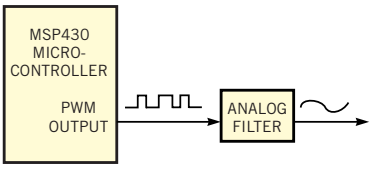


Figure 1

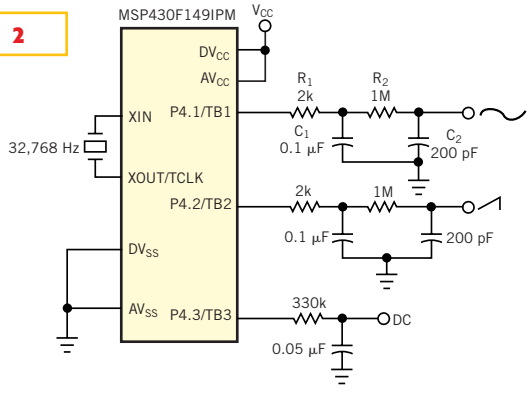
A PWM signal passing through a filter yields and analog signal.

Figure 2 depicts a circuit that delivers a 250-Hz sine wave, a 125-Hz ramp, and a dc signal. The desired sampling rate is 8 kHz (32 samples for each sine-wave cycle (16× oversampled), and 64 samples for each ramp cycle (32× oversampled)). These figures result in a required PWM-signal frequency of 8 kHz and a required PWM clock frequency of 2.048 MHz. It is usually best for the PWM signal frequency to be much higher than the desired bandwidth of the signals to be produced. Generally, the higher the PWM frequency, the lower the order of filter required and the easier it is to build a suitable filter. This design uses Timer B of the MSP430 in 16-bit mode and in "up" mode, in which the counter counts up to the contents of capture/compare register 0 (CCR0) and then restarts at zero. CCR0 is loaded with 255, thereby giving the counter an effective 8-bit length. You can find this register and others in a DAC demonstration program for the MSP430 microcontroller. You can download the program from the Web version of this Design Idea at www.edn.com.

CCR1 and output TB1 produce the sine wave. CCR2 and TB2 generate the ramp, and CCR3 and TB3 yield the dc value. For each output, the output mode is the reset/set mode. In this mode, each output resets when the counter reaches the respective CCRx value and sets when the counter reaches the CCR0 value. This scheme provides positive pulses equivalent to the value in CCRx on each respective output. If you use the timer in 8-bit mode, the reset/set output mode is unavailable for the PWM outputs because the reset/set mode requires CCR0. The timer's clock rate is 2.048 MHz. **Figure 3** shows the sine and ramp waveforms. The sine wave in this example uses 32 samples per cycle. The sample values are in a table at the beginning of the program. A pointer points to the next value in the sine table, so that, at the end of each PWM cycle, the new value of the sine wave is written to the capture/compare register of the PWM timer.

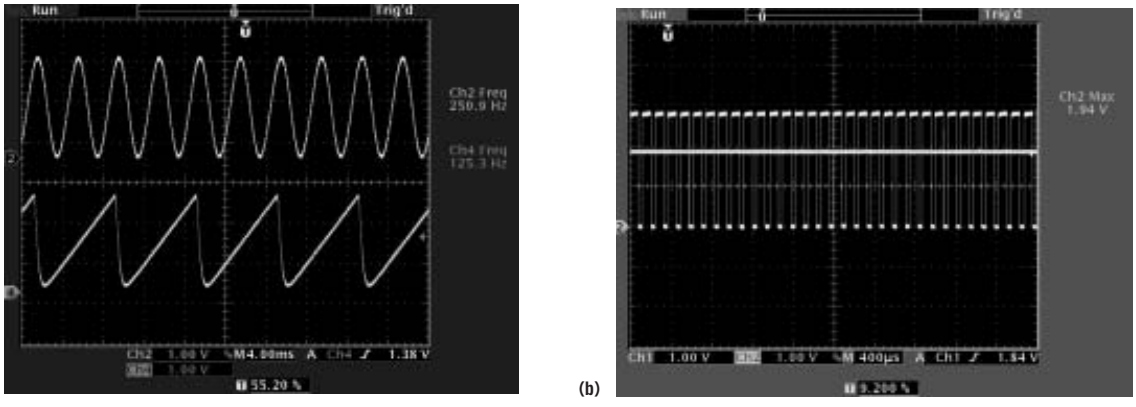
The ramp in this example does not require a table of data values. Rather, the ramp simply increments the duty cycle for each cycle of the PWM signal until it reaches the maximum and then starts over at the minimum duty cycle. This gradual increase in PWM-signal duty cycle results in a ramp voltage when the signal passes through a filter. You control the dc level by simply setting and not changing the value of the PWM-signal duty cycle. The dc level is directly proportional to the duty cycle of the PWM signal. **Figure 2** shows the reconstruction filters used for each signal in this example. The filter for the ac signals is a simple two-pole, stacked-RC filter, which is simple and has no active components. This type of filter necessitates a higher sampling rate than would be re-

Figure 2



A microcontroller and some passive filters produce a sine wave, a ramp, and a dc signal.

Figure 3



(a) (b)

The microcontroller's PWM timer produces an ac signal (a) and a dc signal (b) of a sine wave and a ramp with 8-bit resolution.

quired if the filter had a higher order. With the type of filter shown in **Figure 2**, you should use at least a 16× oversampling rate.

The filter yields its best response when $R_2 >> R_1$. Also, setting the cutoff frequency too close to the bandwidth edge causes a fair amount of attenuation. To reduce the amount of attenuation in the filter, set the cutoff frequency above the bandwidth edge but much lower than the frequency of the PWM signal. The filter for the dc value serves for charge storage rather than ac-signal filtering. Therefore, it uses a simple, single-pole RC filter. **Figure 4** shows the software flow for the DAC. After a reset, the routine stops the watchdog timer, configures the output ports, and sets up the clock system. Next, the software calls a delay to allow the 32,768-Hz crystal to stabilize to calibrate the DCO (digitally controlled oscillator).

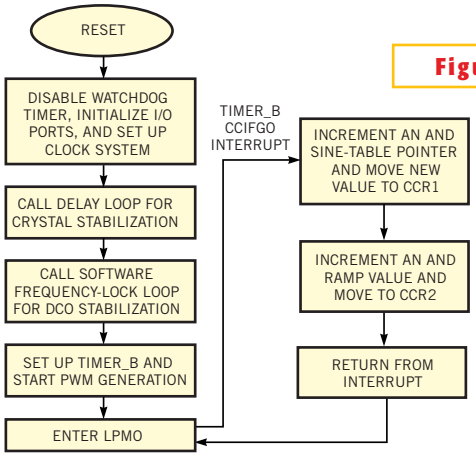


Figure 4

This software flow diagram shows how the PWM timer generates the sine and ramp signals.

Next, the routine calls the calibration routine to set the operating frequency to 2.048 MHz. After the DCO calibration, the program sets up Timer_B, CCR1 and CCR2 for PWM generation and then starts the timer. Finally, the MSP430 goes into low-power mode 0 (LPM0) to conserve power. The CPU wakes up to handle each CCIFG0 interrupt from the PWM timer and then re-enters LPM0. (See **references 1**, **2**, and **3** for more information on the DCO and the MSP430 family.)

References

1. MSP430x13x/14x data sheet, Texas Instruments document SLAS-272.

2. MSP430x1xx Family User's Guide, Texas Instruments document SLAU049.

3. "Controlling "the DCO of the MSP430x11x," Texas Instruments document SLAA074.

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design ideas

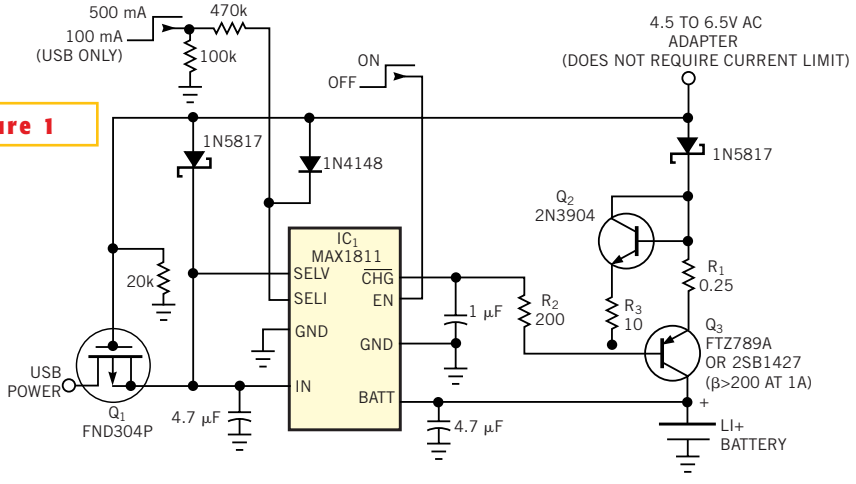
Edited by Bill Travis

Add current boost to a USB charger

Len Sherman, Maxim Integrated Products, Sunnyvale, CA

THE POPULAR USB INTERFACE can charge a portable device while transferring data. But for high-capacity batteries, the 500-mA output current of USB hosts and powered hubs greatly extends the charging time. (Unpowered USB hubs supply no more than 100 mA.) Thus, a system that accepts charging power from an ac adapter as well as the USB port is more convenient. Such a system can charge from a notebook USB port when you're traveling, yet can charge faster via the adapter when you're at home or in the office. An external transistor current source adds dual-input capability to a single-chip lithium-cell charger (**Figure 1**). The chip, IC_1, operates alone when you connect to USB power and allows you to pin-program it for a maximum charging current of either 500 or 100 mA. When you plug in an ac adapter, which the 600-mA components set, the external-transistor current source, Q_2 and Q_3, turns on and sets IC_1's charging current to 500 mA. Because IC_1 and Q_2 both charge the battery under that condition, the total charging current is 1100 mA.

Figure 1



This battery charger delivers 100 or 500 mA (selectable) to a single lithium cell when USB power is connected and charges at 1100 mA (settable via R_1 or R_2) when ac power is present.

Q_2 and Q_3 form a current limiter for the ac adapter. The limiter allows Q_2 and R_1 to pass the additional 600 mA. When the voltage drop across R_1 exceeds that across R_2, which R_2 and R_5 set, Q_2 begins to turn off. Q_2 cancels V_{BE}, enabling R_1 to more accurately set the maximum current. Voltage across R_3 sets the reference voltage, and the output current limits when the voltage drop on R_1 matches the voltage on R_3. Q_3 should have a beta higher than 200 at 1A, so that IC_1's $\overline{CHG}$ pin can sink enough current to turn on Q_3. High beta also minimizes error in the transistor current source. When IC_1 changes from current mode to voltage mode at approximately 4.15V, IC_1's $\overline{CHG}$ output turns off the transistor current source. IC_1 remains on and finishes off the taper to full charge. It also remains on and continues to function when USB power is gone and only ac power remains.

IC_1 also controls the prequalification current, which is the current level necessary to safely recover deeply discharged cells at low battery voltage. The $\overline{CHG}$ output assumes a high-impedance state during cell prequalification to ensure that the external current source remains off, and that the prequalification current of approximately 50 mA comes only from IC_1. When you plug in the ac power, Q_1 turns off to prevent back-feeding the USB input. You install Q_1 "backward" with the drain connected to USB input side, so that USB power remains connected to the IN pin (IC_1 pin 4) via Q_1's body diode, even when Q_1 is off.

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Transistor linearly digitizes airflow

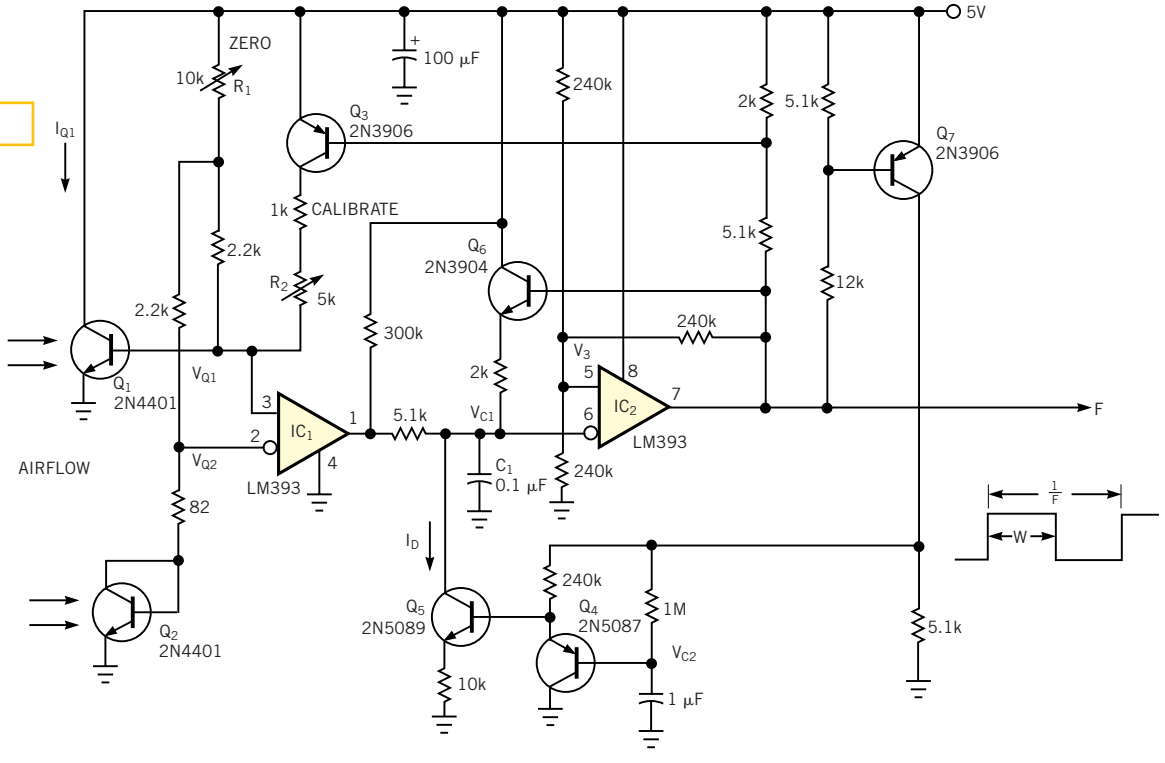
Steve Woodward, University of North Carolina, Chapel Hill, NC

A sensitive and reliable way to measure airflow is to take advantage of the predictable relationship between heat dissipation and air speed. The principle of thermal anemometry relies on King's Law, which dictates that the power required to maintain a fixed differential between the surface of a heated sensor and the ambient air temperature increases as the square root of air speed. The popular hot-wire anemometer exploits this principle, but it suffers from the disadvantage of using a specialized and fragile metallic filament, the hot wire, as the airflow sensor. The circuit in **Figure 1** avoids this disadvantage by using a pair of robust and inexpensive transistors instead of a flimsy wire for airspeed sensing. The Q_1/Q_2 front end of the circuit borrows from an earlier Design Idea (**Reference 1**). Just as in the 1996 circuit, the circuit in **Figure 1** works by continuously maintaining the condition $V_{Q1}=V_{Q2}$. To perform this task, the circuit must keep Q_1 approximately 50°C hotter than Q_2.

V_{BE} balance requires this temperature difference, because Q_1's collector current, I_{Q1}, is 100 times greater than that of Q_2, I_{Q2}. If Q_1 and Q_2 were at the same temperature, this ratio would result in V_{Q1}'s being greater than V_{Q2} by approximately 100 mV. Proper control of I_{Q1} establishes differential heating that makes Q_1 hotter than Q_2. The method thus exploits the approximate −2-mV/°C temperature coefficient of V_{BE} to force V_Q balance. The resulting average, I_{Q1}, proportional to the average power dissipated in Q_1, is the heat-input measurement that forms the basis for the thermal air-speed measurement. Calibration of the sensor begins with adjustment of the R_1 zero-adjust trim. You adjust R_1 such that, at zero airflow, $V_{Q1}=V_{Q2}$ with no help from Q_3. Then, when moving air hits the transistors and increases the heat-loss rate, V_{Q1} increases and causes comparator IC_1 to release the reset on C_1. C_1 then charges until IC_2 turns on, generating a drive pulse to Q_1 through Q_3.

The resulting squirt of collector current generates a pulse of heating in Q_1, driving the transistor's temperature and V_{BE} back toward balance. Proper adjustment of R_2 calibrates the magnitude of the I_{Q1}-induced heating pulses to establish an accurate correspondence between pulse rate and air speed. Now, consider measurement linearization. The square-root relationship of King's Law makes the relationship between heat loss and air speed nonlinear. You must iron the kinks out of the air-speed-calibration curve. You might achieve linearization in software, of course. However, depending on

Figure 1



Using a simple transistor as sensor, this circuit yields a digitized, linear measurement of air speed.

the flexibility of the data system the anemometer works with, a software correction is sometimes inconvenient. Another earlier Design Idea (**Reference 2**) presented an analog solution to linearization. But if you want the advantages of a digital, pulse-mode output—that is, noise-free transmission over long cable runs—you need a different fix.

The circuit in **Figure 1** provides both linearity and a digital output. The average heat the pulses deposit in Q_1 is $H=5V\times I\times F\times W$, where I is the amplitude of the Q_1 current pulses (adjusted with R_2), F is the output frequency, and W is the pulse width. W is inversely proportional to I_D, the discharge current that ramps down V_{C1} and controls the on-time of IC_2. Q_4 and Q_7 average the output duty cycle to generate a control voltage for Q_5 and thus make W a function of F. In fact, the feedback loop this arrangement establishes implicitly makes $W=K/(W\times F)$, where K is a calibration constant determined by the component values. Therefore, $W^2=K/F$, and $H=5\times I\times F/\sqrt{K/F}$. This expression yields $F=(H/5I)^2/K$, making F the desired function of H^2 and thus linearizing the relationship between frequency and air speed.

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1. Woodward, Steve, "Self-heated transistor digitizes airflow," *EDN*, March 14, 1996, pg 86.
2. Woodward, Steve, "Transistor and FVCs make linear anemometer," *EDN*, Sept 26, 1996, pg 72.

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Make a truly linear RF-power detector

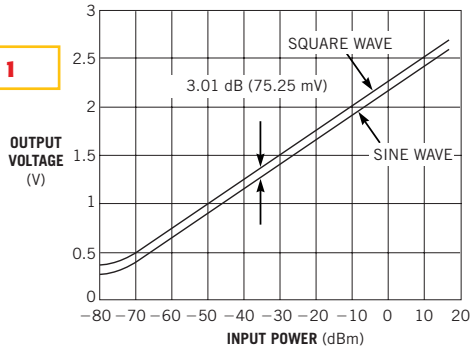
Victor Chang and Eamon Nash, Analog Devices, Wilmington, MA

MODERN HIGH-PERFORMANCE transmitters require accurate monitoring of RF power, because most cellular standards depend on strict power-transmission levels to maintain an effective network. Regulation of transmitted-signal strength also lets you build lower cost systems. **Figure 1** shows a waveform-independent circuit that provides a linear measurement of RF power. Sophisticated modulation schemes, such as CDMA (code-division multiple access) and TDMA (time-division multiple access) have obsoleted traditional approaches to RF power. Diode-based detectors have poor temperature stability, and thermal detectors have slow response times. Logarithmic amplifiers are temperature-stable and have a high dynamic range, but they exhibit a waveform-dependent response. This response causes the output to change with modulation type and, in the case of spread-spectrum technology, channel loading.

Power detection must be waveform-independent in systems that use multiple modulation schemes. These include point-to-point systems that are configurable to transmit QPSK (quadrature-phase-shift keying), 16QAM (quadrature amplitude modulation), and 64QAM, for example, and spread-spectrum systems such as CDMA and W-CDMA (wide CDMA). A logarithmic amplifier in an automatic-gain-control loop can regulate the gain of a variable-gain power amplifier, but the output voltage is waveform-dependent, because the logarithmic amplifier does not respond to the rms level of the signal. For example, sine- and square-wave inputs that have the same rms voltage levels have different logarithmic intercepts (**Figure 2**). You could use calibration factors to correct this intercept difference in a multistandard system.

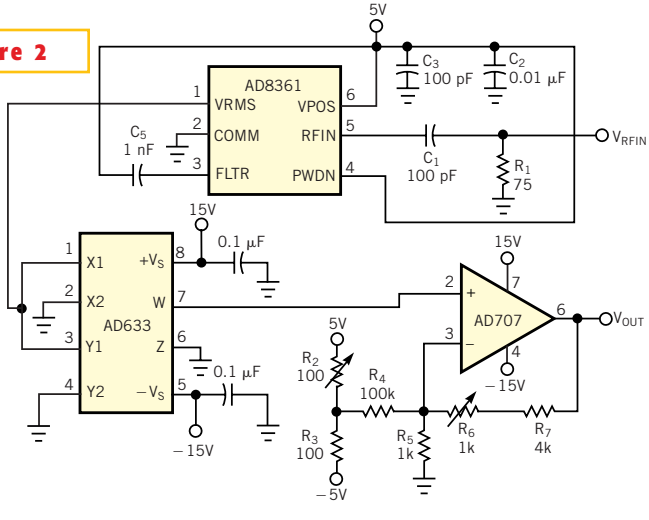
An alternative solution (**Figure 1**) uses the AD8361, a high-frequency true-power detector. Unlike the logarithmic amplifier, the AD8361 is an rms-to-dc converter and, therefore, responds to the

Figure 1



This circuit provides an output voltage that is linearly proportional to the input power in watts.

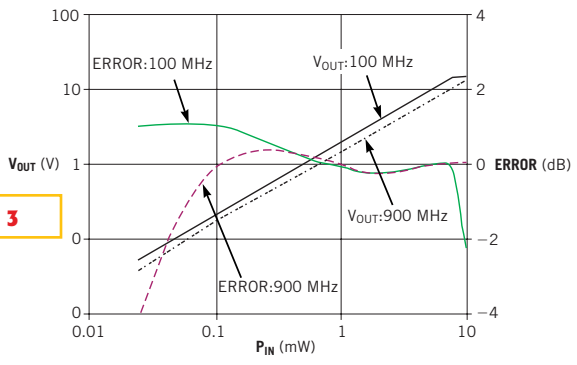
Figure 2



Log amps detect signals over a wide dynamic range, but are not rms-responding.

input rms voltage. Hence, a sine wave, a square wave, or any other input with the same rms level produces the same dc output, allowing you to incorporate waveform-independent measurement into a multimodulation system. With the addition of a multiplier, the circuit delivers an output voltage that is proportional to the input power level in watts. You can easily adjust gain and offset for this power meter with an op-amp circuit, thus providing an output scaled in volts per watt. A complex RF waveform feeds the input of the AD8361.

Figure 3



The circuit in Figure 1 responds to rms signals, independent of waveform.

The multiplier squares the dc output to produce a voltage proportional to the power dissipated in the 50Ω input impedance of the circuit. The AD633 multiplier squares the rms output of the AD8361 and divides by 10. The AD707 provides a maximum gain of 6 [$G=(R_5+R_6+R_7)/R_5$]. This value is lower than the gain of 10 that you would need to exactly cancel the effect of the multiplier scaling and allows the circuit to have a wider dynamic range, because the output would saturate with a smaller input with a gain of 10. You can easily adjust all circuit offsets with potentiometer R_2. **Figure 3** shows measurements made with this power meter. The graphs plot the output voltage and error for input signals at frequencies of 100 and 900 MHz. The detector operates at frequencies as high as 2.7 GHz.

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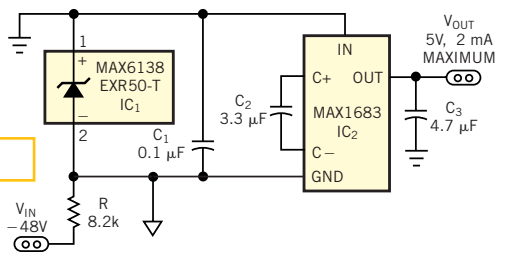
Simple circuit provides 5V gate bias from −48V

Will Hadden, Maxim Integrated Products, Sunnyvale, CA

A small and simple circuit derives 5V from the −48V rail that telecomm applications typically use (**Figure 1**). Useful for gate bias and other purposes, the 5V supply delivers as much as 5-mA output current. A shunt reference, IC_1, defines −5V as ground reference for a charge pump, IC_2. The charge pump doubles this 5V difference between system ground and charge-pump ground to produce 5V with respect to the system ground. The shunt reference maintains 5V across its terminals by regulating its own current, I_S. I_S is a function of the value of R. The current through R, I_R, is reasonably constant and varies only with the input voltage. I_R, the sum of the charge-pump and shunt-reference currents ($I_R=I_{CP}+I_S$), has maximum and minimum values set by the shunt reference.

Figure 1



This small, simple circuit produces 5V at 5 mA from a −48V input.

The shunt reference sinks as much as 15 mA and requires 60 µA minimum to maintain regulation. Maximum I_R is a function of the maximum input voltage. To prevent excessive current in the shunt reference with no load on the charge-pump output, use the maximum input voltage (−48V−10%=−52.8V) to calculate the minimum value of R. The maximum reference sink current, 15 mA, plus the charge pump's no-load operating current, 230 µA, equals the maximum I_R value, 15.23 mA. Thus, $R_{MIN}=(V_{IN(MAX)}-V_{REF})/I_{R(MAX)}=3.14\ k\Omega$.

Choose the next-highest standard 1% value, which is 3.16 kΩ. You calculate the guaranteed output current for the charge pump at the minimum line voltage: −48V+10%=−43.2V. The charge pump's maximum input current is $I_{CP}=(V_{IN(MIN)}-V_{REF})/R-I_{SH(MIN)}=(43.2-5)/3.16-90\ \mu A=12$ mA, where 90 µA is the minimum recommended operating current for the shunt reference. Assuming 90% efficiency in the charge pump, the output current is $I_{OUT}=(I_{CP}/2)\times 0.9=(12/2)\times 0.9=5.4$ mA. You halve the charge-pump current, because the output voltage is twice the input voltage. Be sure that R can handle the wattage under no-load conditions. A 1W resistor suffices in this example.

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Circuit provides laser-diode control

Michael Fisch, Agere Systems, Longmont, CO

Laser diodes are sensitive to ESD, rapid turn-on currents, and overvoltage conditions. To address those problems, the simple laser-diode controller in **Figure 1** has several functions. The first part of the circuit comprises an 8.2V zener diode, D_1 that forms the heart of a constant-voltage source for the laser diode. Next, IC_{1A}, half of a dual FET-input op amp, forms an inverting integrator to slow the turn-on time. To turn on the laser diode, IC_{1B}, the other half of the op-amp IC, triggers the base of Q_2. This transistor forms a constant-current source for the laser diode. You can monitor the laser-diode supply voltage and the sense-diode current and voltage. You use these parameters as inputs to the differential amplifier, IC_{2A}, the first half of another dual FET-input op amp. When an overvoltage condition occurs, the difference amplifier detects the condition, and its output drives IC_{2B}, configured as an open-loop comparator. You set the threshold by using the potentiometer, R_1. Zener diode D_2 provides a constant-voltage source for that threshold setting. When the voltage reaches the threshold, the output triggers the base of Q_1, which instantly shuts down IC_{1B}, which in turn shuts down the laser diode.

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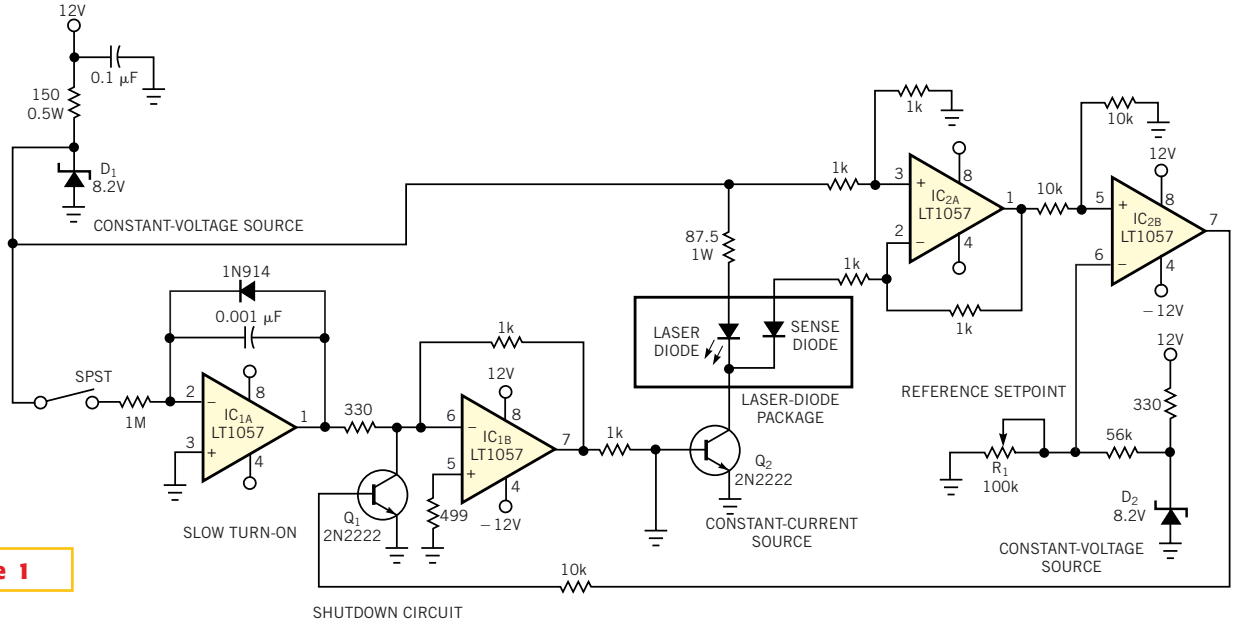


Figure 1

Constant voltage and current and slow turn-on time are the keys to laser diodes' survival.

One amplifier has two gain figures

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

The single-supply circuit in **Figure 1** is an inverting amplifier with two outputs—one for positive output voltages, $V_{OUT(POS)}$, and the other for negative output voltages, $V_{OUT(NEG)}$. Steering diodes D_1 and D_2 split the amplifier, IC_1, output into the two output polarities relative to the 2.5V reference. The gain of the inverting amplifier for each of the two polarities features independent programming, using Catalyst's (www.catsemi.com) 100-tap, digitally programmable potentiometers DPP_1 and DPP_2. You configure the potentiometers as variable resistances and model them as $(1-p)R_{POT}$, where p represents the proportional position of the wiper as it moves from one end (p=0) of the DPP to the other end (p=1). R_{POT} is the potentiometer's end-to-end resistance. In terms of p, the gains of the circuit are

If $R_1 < R_{POT}$, the gain values can be less

$$V_{OUT(POS)} = -\frac{(1-p_1)R_{POT1}}{R_1} V_{IN}$$

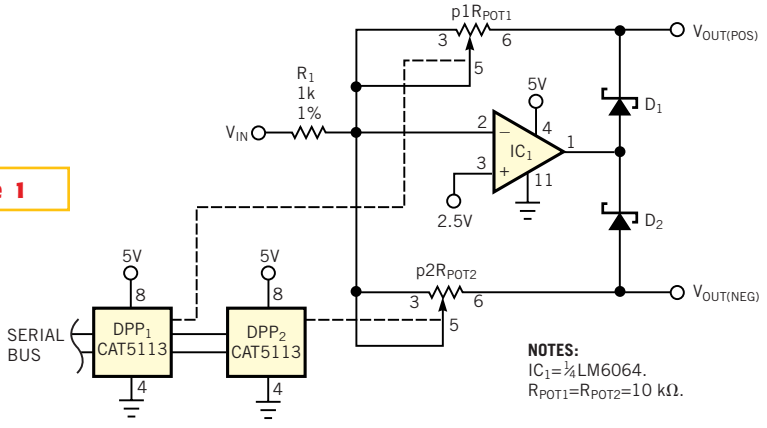
FOR $0 < V_{IN} < 2.5V$, and

$$V_{OUT(NEG)} = -\frac{(1-p_2)R_{POT2}}{R_1} V_{IN}$$

FOR $2.5V < V_{IN} < 5V$.

than one, one, or greater than one. For the circuit values shown, you can program the two gains from approximately $^1/_{10}$ to 10. If you characterize the potentiometer, the measured accuracy of the circuit is approximately 1%. This implementation of the circuit uses only six components and is appropriate for signal-processing applications.

Figure 1



Using digitally programmable potentiometers, you can obtain two distinct gain figures from one amplifier.

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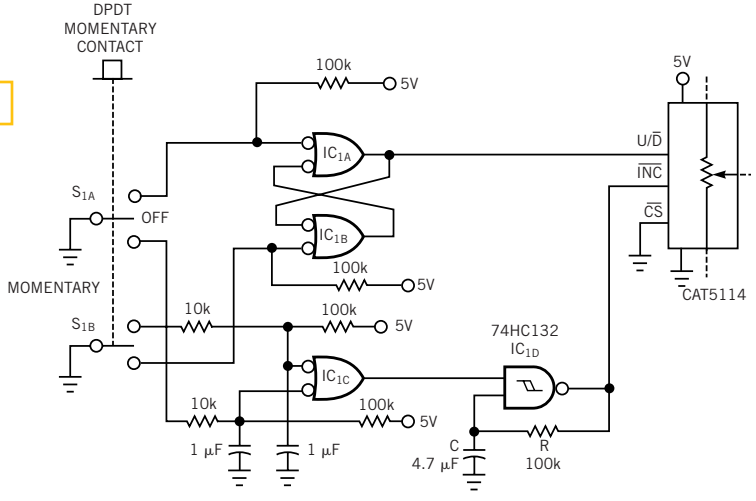
Single switch controls digital potentiometer

Jim Bach, Delphi Delco Electronics Systems, Kokomo, IN

THIS DESIGN IDEA is an evolution and simplification of another (**Figure 1**, **Reference 1**). Replacing the three inverted-input NOR gates with their logical equivalents, positive-input NAND gates, makes these three gate symbols consistent with the fourth, which was drawn as a positive-input NAND gate. The 74HC132's data sheet describes the device as a quad, two-input NAND gate with hysteresis.

As the earlier design also describes, you can activate the DPDT rocker switch, S_1, to produce either a "count-up" or a "countdown" effect at the digital potentiometer, CAT5114. Moving the switch up causes S_{1A} to ground the input of IC_{1A}, thus causing the NAND-gate flip-flop, IC_{1A} and IC_{1B}, to switch high, thereby commanding the CAT5114 to count up. At the same time, S_{1B} causes the 1-µF capacitor on IC_{1C}'s upper input to discharge through a 10-kΩ resistor. Eventually the output of IC_{1C} also switches high, thus enabling the oscillator comprising IC_{1D}. Similarly, moving the switch down causes S_{1B} to ground the input of IC_{1B}, thus causing the NAND-gate flip-flop to

Figure 1



This is the original circuit, as published in Reference 1.

TABLE 1–SUMMARY OF SAVINGS

Component	Figure 1 count	Figure 4 count	Savings
ICs	Two	Two	Zero
Resistors	Seven	Four	Three
Resistor values	Two (10 kΩ, 100 kΩ)	One (100 kΩ)	One
Capacitors	Three	Two	One
Capacitor values	Two (1 µF, 4.7 µF)	Two (0.1 µF, 4.7 µF)	One lower value and cheaper
Switches	One DPDT	One SPDT	Single-pole and cheaper

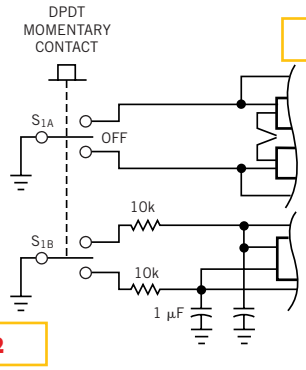


Figure 2

You can restructure the switch-interface circuit of Figure 1 as shown.

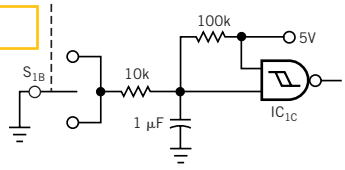


Figure 3

You can simplify the oscillator-enable structure, as shown.

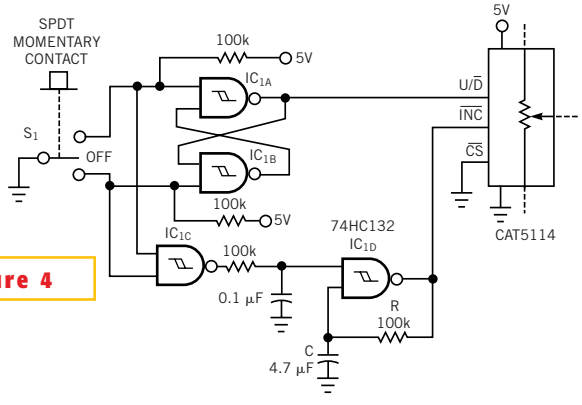


Figure 4

This circuit uses fewer and cheaper components than the circuit in Figure 1.

switch low, thereby commanding the CAT5114 to count down. At the same time, S_{1A} causes the 1-µF capacitor on IC_{1C}'s lower input to discharge through a 10-kΩ resistor, thereby eventually enabling the oscillator comprising IC_{1D}.

The first step in simplifying this design is to rearrange the connections of S_1 so that the A and B sections are not cross-connected between operating the flip-flop and the oscillator-enabling circuit. You can rewire the interface structure as shown in **Figure 2**. This circuit uses S_{1A} to control the flip-flop, whereas S_{1B} controls the oscillator-enable circuit. This step does nothing directly to reduce the parts count of the circuit; however, it does make the subsequent step more obvious. The next step in the simplification is to recognize that the two RC networks on the inputs of IC_{1C} both do the same thing but in opposite switch positions. As far as IC_{1C} is concerned, either switch position performs the same function; that is, to debounce the switch contacts and eventually enable the oscillator. Thus, you need only one RC network, and you can tie it to *both* of S_{1B}'s active positions (**Figure 3**). Moving the switch in either direction discharges the 1-µF capacitor through the 10-kΩ resistor, eventually causing the output of IC_{1C} to switch high, thus enabling the oscillator. When you release the switch, S_{1B} goes to the open, or off, state, and the 1-µF capacitor recharges through the 100-kΩ resistor, thus turning off the oscillator.

The last simplification step stems from realizing that the sole purpose of IC_{1C} and the RC filter on its input is to generate a high state whenever switch S_1 is in either of its active positions. True, the RC filter does debounce the switch contacts; however, the actual switch- closure information available at S_{1B} is also available at S_{1A}. Thus, you can simply use IC_{1C} to directly monitor the S_{1A} contacts. You can move the RC filtering to the input of IC_{1D}. This step allows you to simplify S_1, changing it from a DPDT to a SPDT configuration, which means you can use a cheaper switch. Because the RC debounce filter now connects to a low-impedance gate output, IC_{1C}, you can increase the R, thus reducing the amount of C you need to form the same time constant. Thus, you can use smaller, cheaper capacitors. You can also use the same resistor value, 100 kΩ, in all four locations, eliminating the need to inventory two resistor values. The final circuit appears in **Figure 4**. **Table 1** summarizes the savings in component count and cost.

REFERENCE

1. Wojslaw, Chuck, "Single switch controls digital potentiometer," *EDN*, Feb 7, 2002, pg 100.

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Instrumentation amp makes noninverting integrator

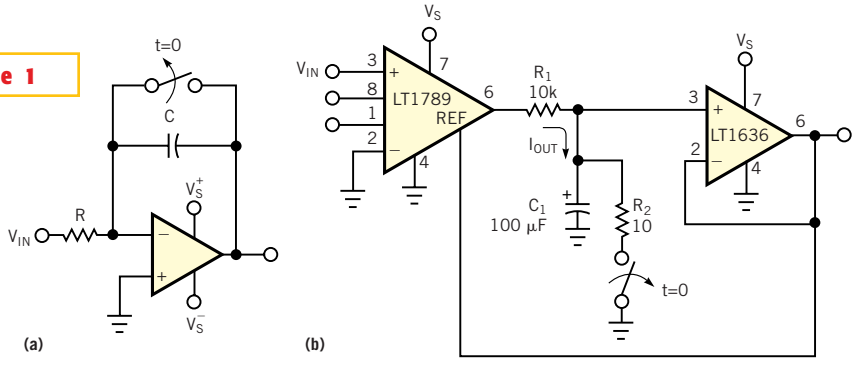
Glen Brisebois, Linear Technology Corp, Milpitas, CA

FIGURE 1A SHOWS the classic implementation of an integrator. The circuit has two properties that may be undesirable in same applications: It necessarily inverts, and it requires a split-supply or midsupply reference. **Figure 1b** shows an implementation of an integrator that uses an LT1789 instrumentation amplifier. This integrator does not invert, and it works with a single supply. In addition, because it has a positive-only output swing, the integrator capacitor can be a high-value, polarized electrolytic unit, as shown. Most of the circuit operates as a voltage-controlled current source. The

LT1789 is a precision micropower instrumentation amplifier that can operate from 3 to 36V total-supply spans.

With a gain setting of 1, with pins 1 and 8 open, the voltage between the inputs also appears between the Output and Reference pins. The Output pin connects to one side of R_1, and the voltage on the other side of R_1 drives the Reference. The input voltage, V_{IN}, appears across R_1, causing the current-source action, with $I_{OUT} = V_{IN}/R_1$. Dumping this current into a capacitor produces the integrator action, with the time constant R_1C_1. The LT1636 buffers the output voltage on C_1, thereby eliminating the loading effects of approximately 200 kΩ of the LT1789's Reference pin and any downstream circuitry. The wide, single-supply range and micropower operation make the circuit suitable for battery-powered systems. As a positive-output-only integrator, this circuit is not generally applicable inside control loops. Suitable applications include accumulators, adjustable ramp generators, and voltage-to-frequency converters.

Figure 1



The classic integrator in a inverts and requires split supplies. The circuit in b is noninverting and works with a single supply.

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design ideas

Edited by Bill Travis

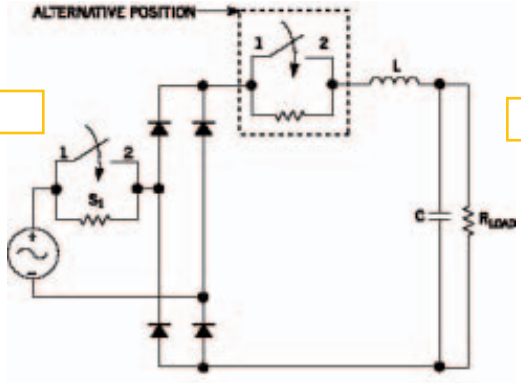
Passive circuit limits inrush current

Sunil Tiwari and Mangesh Borage, Centre for Advanced Technology, Indore, India

You would normally limit the inrush current during start-up of a rectifier circuit with a capacitor output filter by using the circuit in **Figure 1**. You insert a high resistance in series with the ac input or the dc output of the rectifier and then short-circuit the resistance with a switch once the filter capacitor is sufficiently charged. In this scheme, you need an additional timer relay or sensing circuit to control the closure or opening of the switch. Moreover, the switch carries the full load current during normal operation. As an alternative, the simple, passive circuit in **Figure 2** for inrush-current limiting uses commercially available components and presents advantages in size and cost. The resistance-switch arrangement inserted in series with the filter capacitor, instead of in the main power line, limits inrush current in this circuit. The current rating of the switch can therefore be much lower. A switch, S_1, short-circuits the charging resistor, R_1. This switch represents the contact of a commercially available dc relay. The relay senses the voltage on capacitor C; thus, the switch operates automatically.

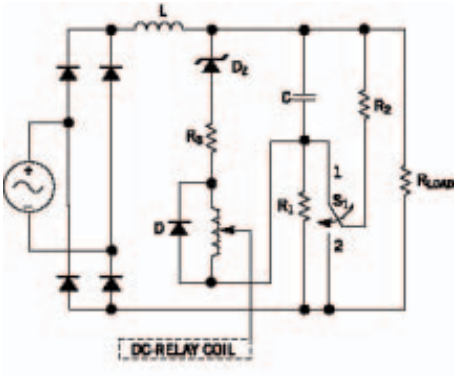
R_1 limits the peak inrush current and also determines the start-up delay. The

Figure 1



In this classic inrush-limiting circuit, the switch carries the full load current during normal operation.

Figure 2



In this inrush-limiting circuit, the current rating of the switch is considerably reduced.

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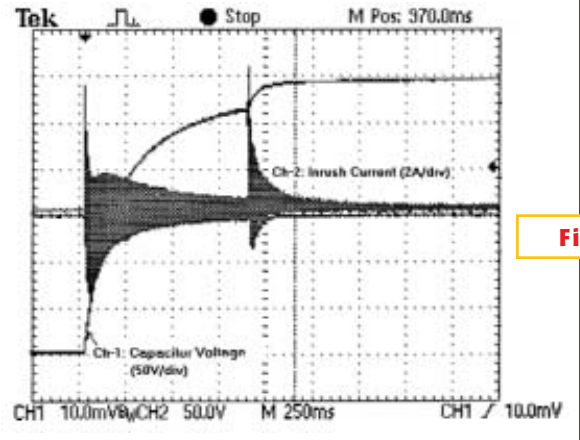

Figure 3

The circuit in Figure 2 limits the inrush current to a safe value of approximately 6A.

relay's changeover contact either short-circuits R_1 when the capacitor is sufficiently charged or connects R_2 across the capacitor to speed its discharge in the off condition. For jitter-free operation of the relay, you need suitable hysteresis between closure and opening. Too little hysteresis results in malfunction of the circuit in the presence of momentary dips. Too much hysteresis leaves the circuit unprotected against heavy inrush currents upon reclosure of the relay. You can incorporate suitable hysteresis by adding zener diode D_Z and resistor R_3 in series with the relay coil. The following equations describe the operation of the circuit in **Figure 2**:

Dc pickup voltage:

$$V_{DCP} = V_{CP}\frac{(R_C + R_3)}{R_C} + V_Z;$$

Dc dropout voltage:

$$V_D = I_Z(R_C + R_3) + V_Z;$$

and hysteresis:

$$V_{DCP} - V_D = V_{CP}\frac{(R_C + R_3)}{R_C} - I_Z(R_C + R_3),$$

where V_{CP} is the relay-coil pickup voltage, R_C is the relay-coil resistance, V_Z is the zener-diode breakdown voltage, and I_Z is the zener-diode knee current.

Commercial-grade components have variations in their parameters. These variations can affect the dc pickup and dropout voltages. For minimum sensitivity to variations in V_{CP}, R_C, and I_Z, you should make R_3 as low as possible. Tolerances in V_Z and R_3 have an insignificant effect on the circuit; however, I_Z is temperature-dependent, and its effect on dropout voltage is significant. **Figure 3** shows the experimental results. The prototype uses the following component values: C=2000 µF (nonpolar), R_1=36Ω, R_2=4.7 kΩ, R_3=12 kΩ, V_Z=110V, I_Z=3 mA, V_{CP}=65V, and R_C=10 kΩ.

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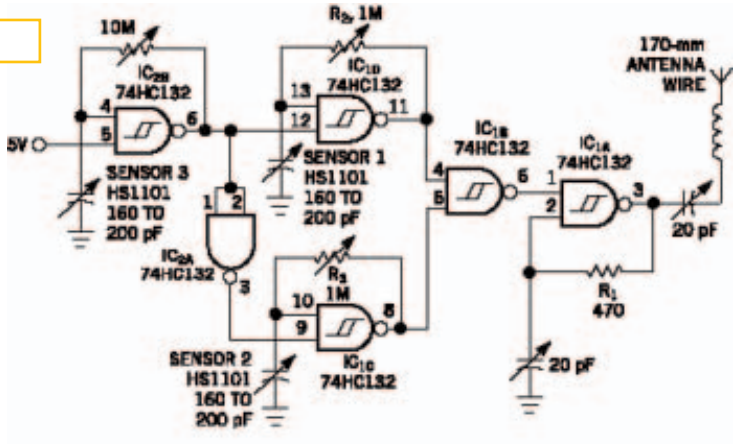
Transmitter senses triple relative-humidity figures

Shyam Tiwari, Sensors Technology Ltd, Gwalior, India

THE CIRCUIT IN **Figure 1** is a triple, relative-humidity sensor and radio transmitter. Sensors 1 and 2 form two gated oscillators with natural frequencies of 10 and 5 kHz, respectively, at relative humidity of 50%. The gated oscillators use variable resistances R_2 and R_3, respectively. Together, these two oscillators generate FSK-modulated outputs at output of IC_{1B}, Pin 6. The oscillator for Sensor 3 causes switching of the FSK signal at IC_{2B}. IC_{2B}'s natural frequency is 1 kHz at relative humidity of 50%. As the HS1101's capacitance changes from 160 to 200 pF (180 pF at relative humidity of 50%), the oscillator frequencies change by approximately ±20% for relative humidity of 0 to 100%). You can tune the RF generator, IC_{1A}, to the desired frequency of 27 to100 MHz for FM transmission. The following represents various ways to monitor the signals at the receiver end (not included in the design):

- Sensor 3 signal is the FSK-modulated signal at the receiver: 1 kHz±20% for relative humidity of 0 to 100%.
- Sensor 1 signal is the top FSK frequency, 10 kHz, on the carrier wave. It measures 10 kHz±20% for relative humidity of 0 to 100%.

Figure 1



Using FSK modulation, you can generate three independent relative-humidity measurements with one circuit.

- Sensor 2 signal is the bottom FSK frequency, 5 kHz, on the carrier wave. It measures 5 Khz±20% for relative humidity of 0 to 100%.
- The difference between the top and the bottom FSK modulating frequencies provides the difference in the relative-humidity signals.

You can replace the Sensor 3 circuit with any TTL oscillator circuit with a range of 100 Hz to 1 kHz. You can then generate the frequency from any other type of sensor. This frequency then becomes available at the receiver without affecting the relative-humidity signals from sensors 1 and 2. You can even use a TTL-based ASCII output to replace the Sensor 3 circuit to pass the ASCII data along with relative-humidity signals.

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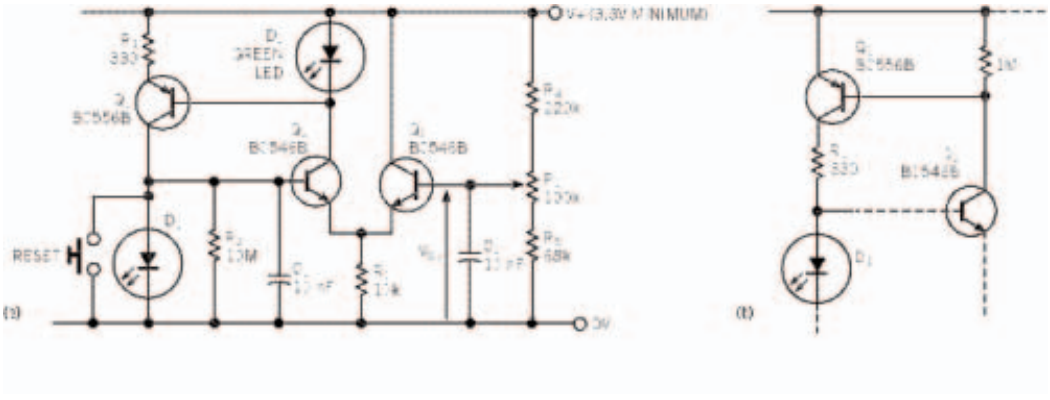
Latching light detector is frugal with power and parts

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

THIS IDEA DEMONSTRATES three uses for the humble LED. The circuit in **Figure 1a** forms a simple light detector that latches and turns on an LED when the ambient light exceeds a preset limit determined by potentiometer P_1. LED D_1 is both the indicator and the light detector. All junction diodes exhibit some degree of photosensitivity. Light-emitting diodes are photovoltaic in that they generate a small voltage in response to light with suitable spectral content. Provided that they have light loads, some LEDs can generate more than 1V in adequate light conditions. The Q_2-Q_3 differential pair acts as a comparator. At low light levels, the photovoltage that D_1 generates is lower than Q_3's base voltage, V_{B3}, and Q_1 and Q_2 are both off. When the light falling on D_1 exceeds the threshold that P_1 sets, Q_2 begins to conduct, thereby biasing the second LED, D_2, which acts as a voltage reference (the third function of an LED). Q_1 now turns on, sourcing current to D_1, which illuminates.

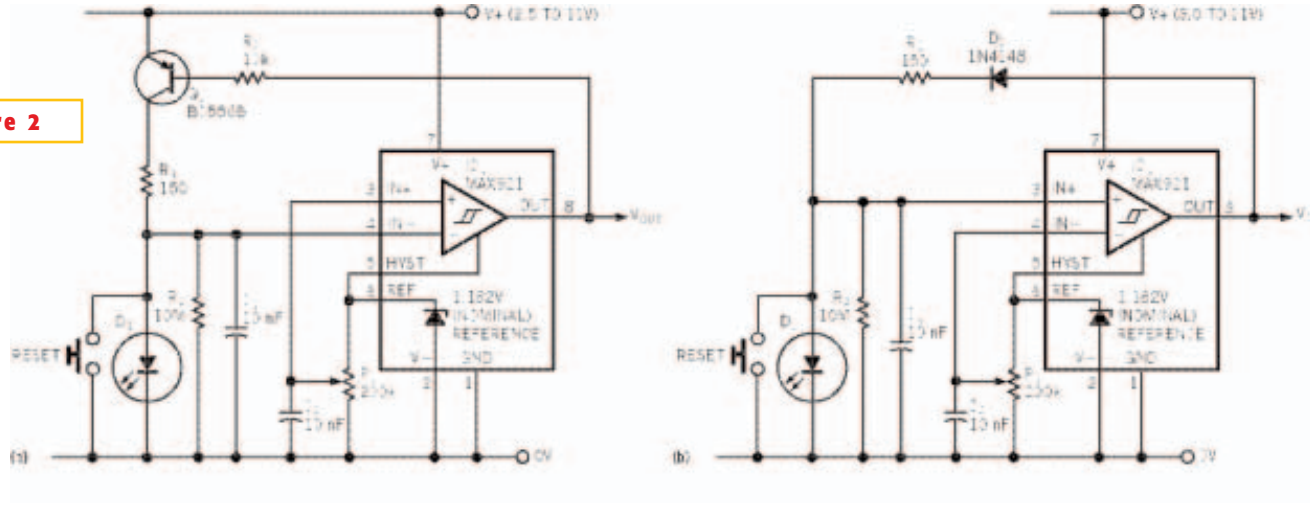
Regenerative action around Q_1 and Q_2 ensures that the circuit makes a rapid transition into the latched state. The circuit stays latched, and D_1 remains illuminated even if the light level falls below

Figure 1



This circuit uses LEDs as both light-detecting and -indicating devices (a). A modification replaces the voltage-reference LED, D_2, by a resistor (b).

Figure 2



This circuit avoids trip-point changes as a function of supply voltage (a). A modification works from slightly higher supply voltages (b).

the trip point. You can reset the circuit by short-circuiting D_1. Because Q_1 is off in the unlatched state, D_1's only load is R_2 and Q_2's base current. Provided that Q_2 has adequate beta and R_3 is fairly large, the loading is negligible. You can use R_2 and C_1 to reduce D_1's sensitivity and provide a degree of filtering. You may need such filtering in noisy environments, such as monitoring the light from fluorescent tubes. With adequate forward current, most green LEDs drop approximately 1.7V, so, in the latched state, approximately 1V appears across R_1. A value of approximately 330Ω sources 3 mA into D_1, providing adequate brightness. For obvious reasons, you should not expose the voltage-reference LED, D_2, to light. If necessary, you can omit D_2 by modifying the circuit (**Figure 1b**). For battery-powered applications, the values of R_4, R_5, and P_1 should be fairly large to ensure minimal current drain in the unlatched condition. If you need a broad threshold range, you should select the values to provide a range of V_{B3} from approximately 0.6 to 1.4V.

You need to experiment to find the optimum LED to act as photodetector. Tests on more than 50 LED color samples produced a range of unloaded output voltage varying from a low of 135 mV to more than 1V in overcast sunshine. A green LED with a clear lens produces almost 1.5V on a dull afternoon. The circuit can work from supply voltages as low as 3.3V, guaranteeing operation from three cells. In the off state, current drain is minimal. The circuit in **Figure 1a** consumed just 88 µA in the unlatched state. Although simple and effective, the circuit suffers the disadvantage that its trip point varies with changes in supply voltage. Also, the trip point's lower limit cannot be less than the 600 mV or so to bias Q_1 and Q_2. The circuit in **Figure 2a** remedies these problems. The circuit uses IC_1's internal bandgap reference to generate a stable threshold. Because the MAX921 (www.maxim-ic.com) comparator's input-voltage range includes the negative rail, you can set the trip point at 0 to 1.18V (the value of the internal reference), thus allowing D_1 to work over a wider range of light levels.

Power requirements are minuscule. The circuit operates from supplies as low as 2.5V (the MAX921's minimum supply voltage), and, in the off state, the only current drain comes from P_1 and IC_1's quiescent supply current. The prototype's total off-state current was just 7.8 µA. You can use the comparator's rail-to-rail output voltage at V_{OUT} as a digital signal and feed it to other systems to indicate light conditions. The comparator output can source more than 10 mA with little reduction in high-level voltage, thus allowing you to slightly simplify the circuit (**Figure 2b**). However, in this version, you must accommodate the voltage drop across D_2, so the minimum supply voltage becomes approximately 3V. Alternative devices you can consider for IC_1 include the Linear Technology (www.linear-tech.com) LTC1440 and the Telcom (www.telcom-semi.com) TC1031.

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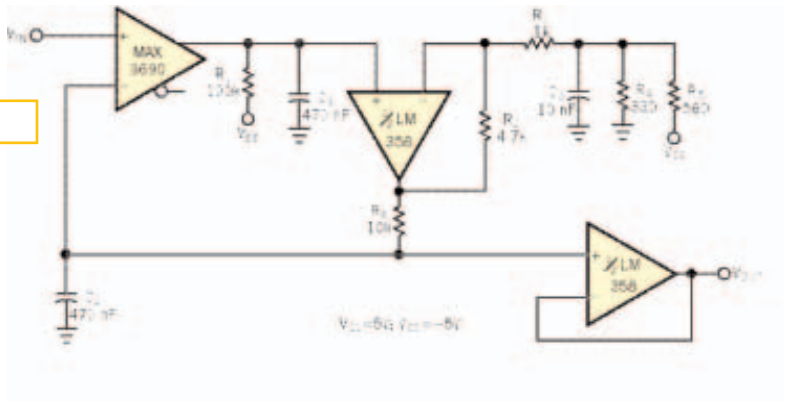
High-speed peak detector uses ECL comparator

Przemyslaw Krehlik and Lukasz Sliwczynski, Institute of Electronics, Krakow, Poland

Professional electronics designers often use peak-detector circuit sin such applications as amplitude measurement, automatic gain control, and data regeneration. You can build a simple and fast peak detector from a serial diode and a shunt capacitor, but it suffers from serious inaccuracy that stems from the diode's forward-voltage drop. On the other hand, precise detectors based on op amps are rather slow. They are therefore not well-suited for measuring pulses of a few nanoseconds' duration. The circuit in **Figure 1** offers both good accuracy and good dynamic performance. The main

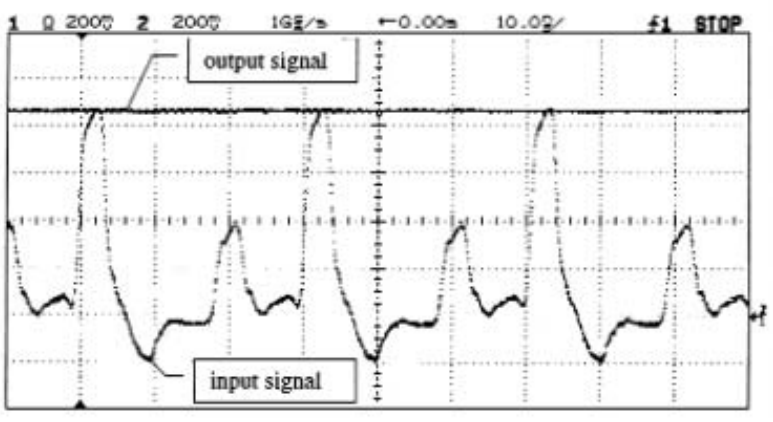
Figure 1



This circuit uses an ultrafast ECL-output comparator to measure the peak value of input signals.

part of the detector is the ultrafast MAX9690 (www.maxim-ic.com), ECL-output comparator. Because the circuit does not internally pull down the output emitter follower, you can use the circuit as a rectifier that charges capacitor C_1. The circuit amplifies and level-shifts the voltage from the capacitor and feeds it back to the negative input of the comparator. When the signal appears at the peak detector's input, capacitor C_1 charges until the feedback voltage at the comparator's negative input becomes equal to the peak value of the signal under measurement; thus, the peak detection occurs. The second op amp forms an output buffer.

Figure 2



The circuit in Figure 1 yields a dc value equal to the positive peak of the input signal.

In this design, the measured peak voltage should be 0 to 2.5V. The detector's accuracy depends on the pulse duration and duty cycle. For example, 1V rectangular pulses having 3-nsec duration and 5% duty cycle produce 5%-low readings. Similar inaccuracy occurs for 10-nsec pulses having 0.1% duty cycle. The accuracy is much better for longer pulse durations, greater duty cycles, or both. The circuit measures pulses lasting for some tens of nanoseconds and having repetition frequency of approximately 1 MHz. To deal with pulses having a lower repetition rate, you should increase the values of C_1 and C_2. That increase would, however, result in longer settling time. Another important element is the discharging resistor, R_1. A value of 100 kΩ for R_1 is appropriate for operation with low-duty-cycle pulses, but you may need lower values for fast tracking with varying input-signal amplitudes. You can also configure a minimum-value peak detector. In this case, you should use the inverting output of the comparator and also reconfigure the amplifier/shifter for inverting operation. **Figure 2** shows an example of the circuit's operation. The circuit correctly measures the peak value of the applied input signal, although the input pulses are quite short and have nearly triangular tips.

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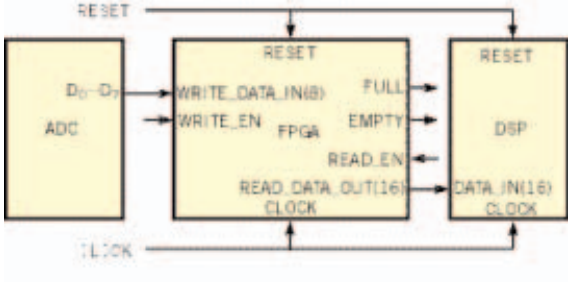
Simple FIFO provides data-width conversion

David Lou, Ghent University, Ghent, Belgium

Many designs require FIFO elastic buffers to form a bridge between subsystems with different clock rates and access requirements. However, in some applications, you need FIFO buffers for data conversion. One example is the case in which you need to connect an 8-bit ADC to a 16-bit data-bus microprocessor through a FIFO buffer (**Figure 1**). Unfortunately, most currently available FIFO buffers are unsuitable for this application. This Design Idea describes how to implement a common clock (synchronous version) for an FPGA-based FIFO for data-width conversion with different-width read and write data ports. You can implement this FIFO using a Xilinx (www.xilinx.com) Spartan II Series FPGA. The method uses an on-chip DLL (delay-locked-loop) macro, distributed memories, and simple counter logic (**Figure 2**).

Figure 1



This block diagram is an example of a system using a FIFO between an ADC and a microprocessor chip.

The width of the input data of the FIFO is 8 bits; however, the width of the output data is 16 bits. You use only one common clock for both read and write actions. The trick is to use a clocked DLL, which not only minimizes clock skews, but also offers a double-frequency output clock. So, you can implement a double data rate for the input data, write_data_in. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, efficiently eliminating the delay from the external input port to the individual clock loads within the device. Instead of using block memory, this design employs distributed memory to hold the data in FIFO. In fact, choosing block memory or distributed memory depends on how important this FIFO is in your system. If it is not critical, you may want to consider using distributed memory.

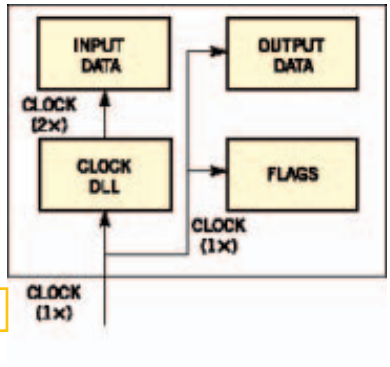


Figure 2

This FPGA uses an on-chip DLL, distributed memory, and simple counter logic.

You can put the memory anywhere you like within the FPGA. If you insist on using block memory, you can easily modify the VHDL code. You can just use some RAM macros to replace distributed memories. You can download the VHDL code for the FIFO from the Web version of this Design Idea at www.ednmag.com. FIFOs commonly use Gray-code counters or linear-feedback shift registers as read or write counters. To minimize the logic size, this design uses only two integers ranging from 0 to 7 together with a carry for the counters. When the read and write counters are equal and the carry is zero, the FIFO is empty. When the write counter plus one is equal to the read counter and the carry is one, the FIFO is full.

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Measure open-circuited cables using a multimeter

Ron Duffy, Agilent Technology, Colorado Springs, CO

You can use a multimeter with capacitance-measurement capability to measure the length of wire or cable to an open circuit. The capacitance of a pair of wires (or a wire to a shield) is directly proportional to the length of the wire. If you know the capacitance per foot of wire, then you can calculate how far it is to the open circuit. To determine the capacitance per foot, take a trip to the hardware store, use a known length of wire, and measure the capacitance with the multimeter. You must zero the multimeter's capacitance function before making any measurements. To zero the meter, select the capacitance function and separate the leads. Then, make the measurement and simply divide the total capacitance of the wire or cable by the total length to determine the capacitance per foot. Once you have this figure, and you're sure that the suspect wire or cable carries no power or signals, you can measure the capacitance, C. The wire length in feet to the open circuit is C divided by the capacitance per foot.

TABLE 1–CAPACITANCE CHARACTERISTICS OF COMMON WIRES AND CABLES

Type	Total capacitance (nF)	Total length (ft)	Capacitance per ft (pF)	Resolution (in.)	Range (ft)
Twisted pair, 18 gauge	41	1100	37.3	32.2	2682.9
16-3 SJ	0.1	5	20	6	500
Category 3 phone, PVC	21.6	1000	21.6	55.56	4629.6
Category 3 phone, plenum	22.1	1000	22.1	54.3	4524.9
14-2 NMB	5.26	250	21	5.7	475.3
16-gauge speaker	0.98	30	32.7	3.67	306.1
18-gauge speaker	0.91	30	30.3	3.96	329.7
24-gauge speaker	1.69	75	22.5	5.33	443.8
20-gauge twin lead	0.68	100	6.8	17.65	1470.6
RG-6	0.47	25	18.8	6.38	531.9
RG-8			29.5	4.07	339
RG-25			50	2.4	200
RG-59			21	5.71	476.2

The resolution depends on the range and resolution of the multimeter. The lowest range of a multimeter is usually 10 nF. The resolution in that range is 10 pF. The multimeter steps up by a factor of 10 each time it changes range. The higher ranges allow you to measure longer wires, but, as **Table 1** shows, the resolution decreases by a factor of 10 for each higher range. (Note the measurements on wires longer than 1000 ft.) All but the last three entries in **Table 1** measure the lengths of wire or cable and then calculate. The last three entries are from a coaxial-cable chart.

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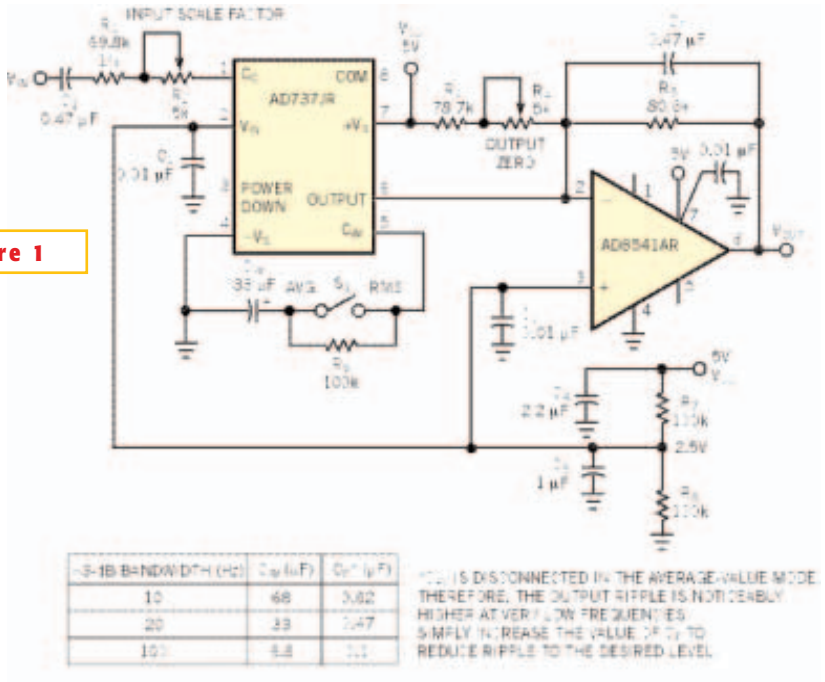
Circuit measures true-rms and average value

Charles Kitchin and Lew Counts, Analog Devices, Wilmington, MA

THE CIRCUIT IN **Figure 1** measures both the true-rms value and the rectified average value of an ac signal. This design uses two low-cost ICs in SOIC packages and consumes only 180 µA of quiescent current. Operating from a single 5V supply, the circuit has an input dynamic range of less than 30 mV to greater than 3V rms. Sine-wave accuracy is good (**Table 1**), and bandwidth is approximately 100 kHz, depending on input level. The circuit can also measure a 1V rms, crest-factor-of-five pulse train with lower than 1%-of-reading error. Most ac measurements use rectified-average-value circuits. Although these can be accurate if you calibrate their scale factor to read the rms value of one waveform, such as a sine wave, they exhibit large errors if you use them for other waveform types. In contrast, the rms value of an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Therefore, the rms value is independent of waveform shape or duty cycle; it's often useful for measuring the power of a complex ac waveform.

Figure 1



You can measure both true-rms and average-rectified values with this circuit.

Average-responding and rms measurements have traditionally used different circuits. However, in some cases it may be useful to know both the rms and the rectified average value of an ac waveform. The ratio of rms to rectified average value is one way to determine the characteristics of a waveform without actually seeing it on an oscilloscope. For example, the rms/average-value ratio is 0.707V/0.636V or 1.11 for a 1V peak undistorted sine wave, 1.0 for a symmetrical square wave, 1.155 for a triangular wave, and 1.253 for Gaussian noise. An AD737 rms-converter IC drives an AD8541AR micropower op amp (**Figure 1**). Resistors R_7 and R_8 form a voltage divider to allow operation from a single supply voltage or battery. Capacitors C_4 and C_5 bypass any signal currents on V_{CC} or $V_{CC}/2$ to ground. The rms-converter IC has two inputs: a high-impedance ($10^{12}\Omega$) input (at Pin 2) and an 8-kΩ, wide-dynamic-range input via Pin 1. The rms converter's full-scale input range is normally 200 mV. You can greatly increase this range by adding an external resistance—in this case, resistor R_1 and trimming potentiometer R_2—between the signal input and Pin 1. This addition has the added advantage of increasing the circuit's input impedance.

TABLE 1—1-kHz SINE-WAVE ACCURACY

V_{IN}	V_{OUT} rms	V_{OUT} (rectified average value)
3	2.9999	2.6762
1	1.0027	0.8947
0.3	0.30201	0.2698
0.1	0.10082	0.09947
0.03	0.0296	0.02956

Note: V_{IN} is in ac volts rms as monitored by Keithley 191 in ac mode. Supply=5V dc.

The AD737JR measures the true-rms value when switch S_1 connects its averaging capacitor, C_{AV}, to Pin 5. The averaging capacitor performs the "mean" portion of the rms function. Removing C_{AV} by opening S_1 converts the circuit to rectified-average-value operation. Resistor R_6 allows a small leakage current to flow past the switch, keeping the capacitor charged and preventing any large surge currents from flowing into or out of C_{AV} when the switch is closed. The AD737JR drives the AD8541AR op amp with a negative-flowing output current. The op amp operates as a current-to-voltage converter and also inverts the signal, providing an output voltage that swings more positive with increasing input levels. Resistor R_5's value of 80.6 kΩ matches the effective input resistance of the AD737 ($R1+R_2+8$ kΩ), so that input/output scaling is 1-to-1. Resistor R_3 and trimming potentiometer R_4 cause a current to flow from the supply to the op amp's summing junction. This action offsets the op amp's output, such that the circuit's output is approximately 0V with no voltage applied. Note that this circuit has a maximum supply-voltage limit of 5.5V; you can extend operation to 12V by substituting an OP-196GS op amp for the AD8541AR. Circuit calibration is easy:

Adjust trimming potentiometer R_4 to mid-scale and set S_1 for rms.

1. Apply a 2.000V rms, 1-kHz sine-

wave input signal.

2. Adjust R_2 until the circuit's output voltage is 2.000V dc.
3. Reduce the input to 100 mV rms and adjust offset trimming potentiometer R_4 for a reading of 100 mV dc.
4. Repeat Step 2.

Because the dc-offset circuitry is ratiometric, it remains calibrated with modest variations in supply voltage. The measured power-supply-rejection ratio of this circuit over a 4.5 to 5.5V supply range is approximately 61 dB. The measured errors versus crest factor for a 5V supply and a 1V rms, 100-µsec pulse are: crest factor=3, error=0.67%; crest factor=5, error=0.98%; and crest factor=10, error=4.7%. Some additional points to consider: The peak rms value of a sine wave is 0.707V peak, and the peak rectified-average value is 0.636V. This ratio of 0.707V-to-0.636V is equivalent to an 11% scale-factor difference between the two measurement methods. If you want this circuit to accurately read the rms value for sine waves in the rectified-average-value mode, S_1 can be a two-pole switch. The second pole can connect a 523-kΩ, 1% resistor in parallel with R_1 to increase the scale factor in the average-value mode. However, the true rectified-average value is more useful in most cases.

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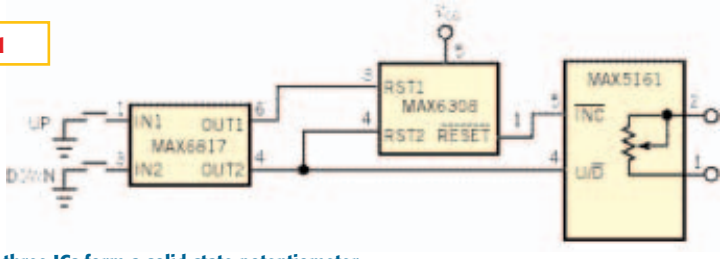
Electronic-potentiometer system has pushbutton interface

Gene Warzecha and Roger Griswold, Maxim Integrated Products, Sunnyvale, CA

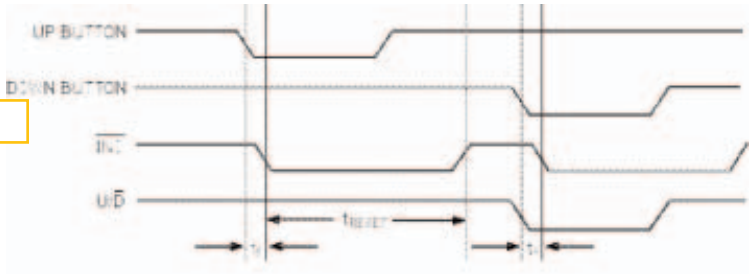
As systems grow smaller, it becomes increasingly attractive to replace mechanical potentiometers with electronic potentiometers, which are smaller and less expensive silicon equivalents. A common interface for such devices comprises a Chip-Select, Increment and, Up/$\overline{\text{Down}}$ line. CS activates the device and, on a rising edge of $\overline{\text{INC}}$ steps the wiper in a direction that the U/$\overline{\text{D}}$ pin indicates. The simple circuit of **Figure 1** uses two pushbuttons—one for up and one for down—and a few tiny silicon devices to implement a debounced, ESD-protected electronic-potentiometer system. The normally open pushbutton switches feed into the MAX6817, an ESD-protected switch debouncer in an SOT-23 package. It has internal pullup resistors on the inputs and buffered, noninverting CMOS outputs. In the absence of a switch closure, the normally open switches hold the MAX6817 outputs high. In turn, that condition ensures a low state for the active-low, push-pull output of the MAX6308, an SC70 reset device with two reset inputs that are independent of the V_{CC} pin.

Figure 1



These three ICs form a solid-state potentiometer.

Figure 2



Closing either pushbutton in Figure 1 increments the potentiometer's output in a direction that the MAX5161's U/$\overline{\text{D}}$ input indicates.

The reset device must have extra reset inputs rather than a manual-reset input, because the glitch-immunity protection of manual-reset inputs is not adequate to guarantee proper operation. The MAX-5161 is a 32-tap, linear-taper electronic potentiometer in an SOT-23 package with the standard $\overline{\text{INC}}$-U/$\overline{\text{D}}$ interface. (The electronic potentiometer pulls the CS input high internally.) Its setup requirement is 50 nsec, meaning that the U/$\overline{\text{D}}$ signal must be stable for 50 nsec preceding a rising edge at the $\overline{\text{INC}}$ pin. The transient-filtering circuitry internal to the MAX6308 introduces a delay that satisfies the setup requirement. The delay, t_r, is typically 10 to 30 µsec (**Figure 2**). $\overline{\text{INC}}$ goes high again only after the reset time-out interval expires. For the MAX6308, that interval (t_{RESET}) is factory-preset with a value as short as 1 msec.

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design ideas

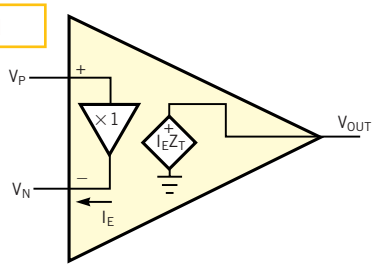
Edited by Bill Travis

RF oscillator uses current-feedback op amp

Victor Koren, Tioga Technologies Ltd, Tel Aviv, Israel

A current-feedback amplifier is a well-known component with many uses. Its basic block diagram shows that its input stage is a voltage follower—in practice, a symmetrical emitter follower (**Figure 1**). The configuration samples the output current, converts it to voltage across a large impedance, and amplifies it to the output using a high-power, low-output-impedance amplifier. The idea is to use the amplifier's input stage as a voltage follower in a basic Colpitts oscillator. This circuit uses the noninverting input of the current-feedback amplifier as the follower input and the inverting input of the amplifier as the follower output. You use the output amplifier to obtain a relatively high-power buffered output. The circuit in **Figure 2** shows a basic Colpitts oscillator that uses the amplifier's input-voltage follower as the active element of the oscillator.

Figure 1



In a typical current feedback amplifier, the input stage is a voltage follower.

Take note of two aspects of this oscillator circuit: First, back-to-back diodes connect across the resonator to limit the oscillations to a specific level, thus maintaining the linearity of the voltage follower. Second, the voltage follower output connects to the resonator tap through resistor R_{OSC} to improve the linearity and define the feedback magnitude. The value of R_{OSC}, 330Ω, lets you obtain soft clipping operation of the diodes across the resonator (V_{RES}=1V p-p, which is 0.5V peak across each diode). **Figure 3** shows V_{RES}, the measured voltage at the top of the resonator. R_F is the amplifier's feedback resistor; the amplifier's manufacturer recommends its value. This design uses the LM6181 from National Semiconductor (www.national.com), and the value of R_F is 1 kΩ.

It is easy to calculate the output voltage: V_{RES}=1V p-p, and $V_{INV}=V_{RES}$=1V p-p. The voltage-buffer gain is unity: $V(R_{OSC})=V_{INV}-V_{RES}/2$. The voltage at the resonator tap is $V_{RES}/2$, because the resonator capacitors are equal in value. $V(R_{OSC})=V_{RES}-V_{RES}/2$=0.5V p-p. $I(R_{OSC})=V(R_{OSC})/R_{OSC}$. $I(R_F)=I(R_{OSC})$. The negative feedback nulls the amplifier's inverting-input current. $V_{OUT}=V(R_F)+V_{INV}=R_F\times I(R_F)+V_{INV}=1000\times(0.5/330)+1$=2.51V p-p. If you need more voltage, you can add R_G—in this case, 100Ω—from the inverting input to ground. $I(R_G)=V_{INV}/R_G$. Now, the current through R_F is the sum of the currents through R_{OSC} and R_G. So, $V_{OUT}=V(R_F)+V_{INV}=R_F\times I(R_F)+V_{INV}=1000\times(0.5/330+1/100)+1$=12.51V p-p. **Figure 4** shows the measured output voltage.

The LM6181's maximum output current is 100 mA, so it can easily drive a current of ±63 mA p-p (±6.3V/100Ω) into a total load of 100Ω (50Ω output-termination resistor and 50Ω load resistor). The voltage across the 50Ω load is 3.15V peak, or 2.23V rms, which is close to 20 dBm (100 mW). This power level can directly drive high-level diode double-balanced mixers, or it can drive a higher power amplifier while delivering a clean sinusoidal waveform. You can modify the resonator circuit to accommodate differ-

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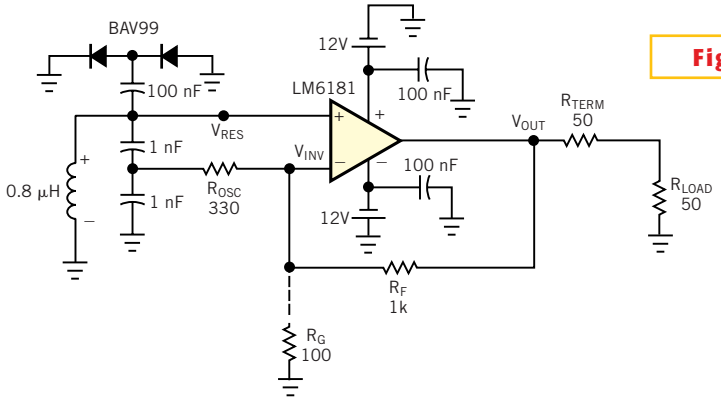
Figure 2



This Colpitts oscillator uses a current-feedback amplifier to provide a clean sinusoidal output.

ent tuning elements. You can use the circuit as a crystal oscillator by changing the inductor to a crystal and changing the resonator capacitors to an appropriate value, such as 2×68 pF. You need a high-value, such as 10-kΩ, bias resistor from the noninverting input to ground to provide bias current to this input.

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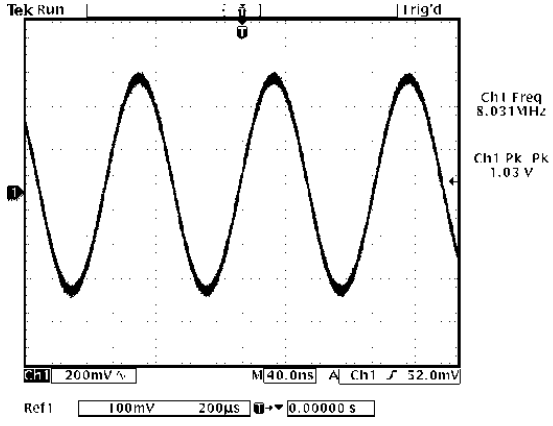


Figure 3 This clean sinusoid is the signal at the top of the resonator, V_{RES}, in Figure 1.

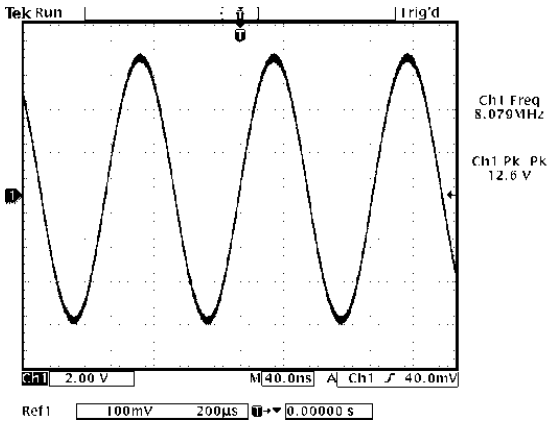


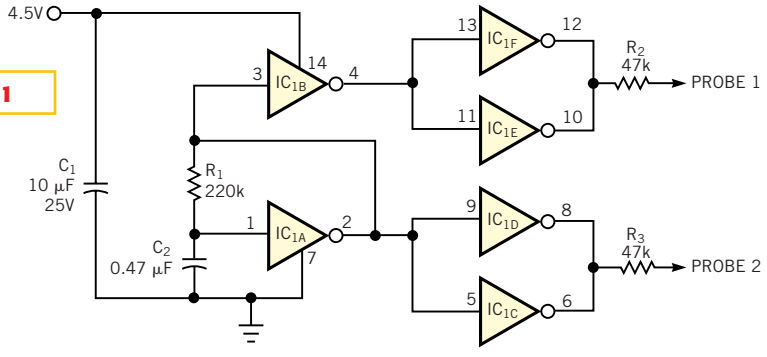
Figure 4 The Colpitts oscillator in Figure 2 produces a pure sinusoidal output.

Simple tester checks LCDs

D Prabakaran, NL Polytechnic College, Tamil Nadu, India

Manufacturers of electronic equipment use LCDs for calculators, watches, mini-videogames, and pagers, for example. In comparison with LED-based displays, which consume power on the order of tens of milliwatts, an LCD consumes only a few microwatts. The LCD thus saves power by a factor of approximately 1000. Checking an LED is as simple as checking a semiconductor diode but, in the case of LCDs, involves some added complexity. An LCD requires an ac electric field to excite the organic compound in the display. Applying a dc voltage could permanently damage the LCD. The circuit in **Figure 1** is a simple configuration to test the performance of an LCD. The circuit produces biphase square waves with negligible dc content. The circuit is based on a CD40106 hex Schmitt-trigger inverter. The circuit comprises an oscillator, IC_{1A}; a phase splitter, IC_{1B}; and a pair of buffer/drivers comprising IC_{1C}/IC_{1D} and IC_{1E}/IC_{1F}.

Figure 1



This simple circuit tests LCDs by producing a biphase square wave with no dc component.

The buffers and drivers connect to test probes through 47-kΩ series resistors, which protect the IC in the event of short circuits. With the component values shown in **Figure 1**, oscillator IC_{1A} provides a square-wave frequency of approximately 45 Hz. The circuit can operate from 3 to 5V. To test any segment of an LCD, touch the backplane using either of the two test probes while touching the segment with the other probe. If the segment under test is operational, it will light up. If the LCD under test is a multiplexed type, then all segments, which are connected, will glow if they are operational. Usually, the rightmost or leftmost connection is the backplane of the LCD. If it is not, you have to find it by trial and error.

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Circuit drives mixed types and quantities of LEDs

Mark Pearson, Maxim Integrated Products, Sunnyvale, CA

Portable systems often use LEDs of different colors and in varying quantities of each color. Some examples are white for the display backlight, green for keypad illumination, and red for power. Typically, the LEDs derive power from at least two power supplies: one for "standard" LEDs (red and green) and one for white LEDs. (White LEDs exhibit a higher forward voltage.) The keypad and other indicator LEDs have current-limiting resistors associated with them. To eliminate these resistors and drive groups of dissimilar LEDs from the same source, you can regulate the current through multiple strings. Four strings of varying LED types derive power from a single power source (**Figure 1**). The circuit mixes LEDs of different forward-bias requirements, yet keeps the loads reasonably well-balanced through use of a current mirror comprising transistors Q_1 through Q_4. It also eliminates the need for a separate current-limiting "ballast" resistor on each LED or string of LEDs and provides a common control point (IC_1's ADJ pin) for adjusting the LED intensities.

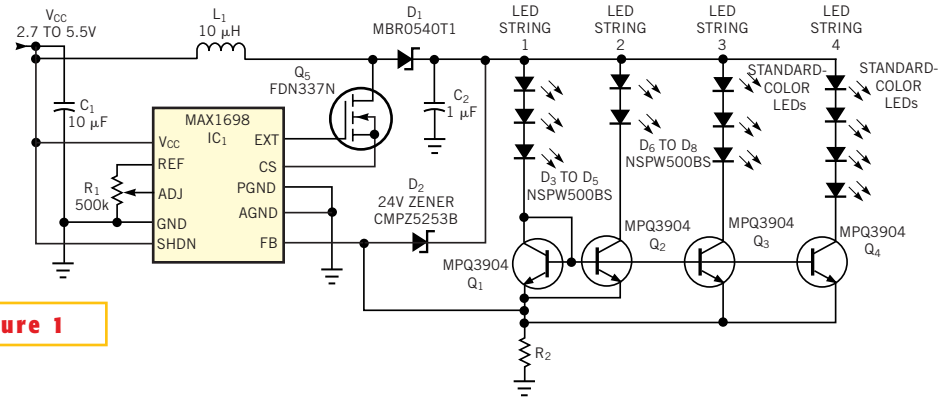

Figure 1

In this LED-driver circuit, a switching converter, IC_1, and associated components lets you mix LED quantities and types.

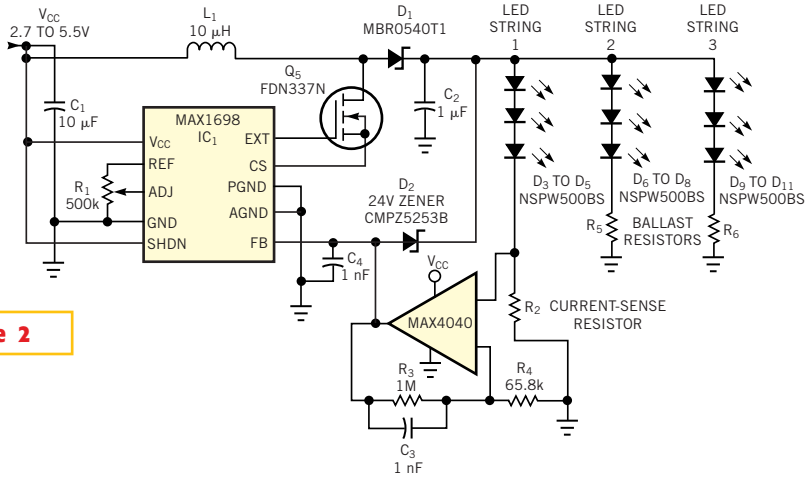

Figure 2

Modifying Figure 1 as shown reduces the overall power dissipation in a standard application.

Transistors Q_2 through Q_4 mirror the current in the diode-connected transistor, Q_1. Note that the Q_1 current-set string (LEDs D_3 through D_5) should have an equal or larger voltage than that of subsequent LED strings. (If it doesn't, the current-mirrored strings may have too little voltage overhead to function properly.) You can easily meet that requirement in the first string by placing either LEDs with larger forward voltage drops, such as the approximate 2.8 to 3.7V range of white LEDs, or more similar LEDs. Then, the circuit can easily accommodate the subsequent strings with lower voltage burdens. The matched-transistor current mirrors maintain a constant and equal current in all LEDs, regardless of quantity and type. That configuration allows the use of a single power supply and a single point for adjusting LED brightness.

Any power difference between the reference string and a mirrored string dissipates in the current-mirror transistor for that string: P_{MAX} (transistor)$=(V_{OUT}-300mV-V_{LEDs})\times I_{LEDMAX}$. The current-sense resistor value is $R_2=300\ mV/I_{LEDMAX}$, where I_{LEDMAX} is the sum of currents from all the strings. (For a comprehensive circuit and parts list, refer to Maxim's MAX1698 (www.maxim-ic.com) EvKit data sheet.)

When driving the same LEDs without the current mirror, you can reduce power dissipation in the sense resistor and ballast resistors by substituting a micropower op amp across the current-sense resistor (**Figure 2**). That circuit improves efficiency by reducing the resistor values and their associated loss. Increasing the gain of the current-sense signal by approximately 16 allows an equivalent reduction in the value of R_2 and the ballast resistors. A typical value for R_2 is 15Ω, which represents a loss of 18 mW: $(20\ mA)^2\times 15\Omega$ for each of three resistors. If $R_2=R_5=R_6=0.931\Omega$, then the resistor power loss drops to 1.12 mW. The op amp draws only 20 µA maximum, which represents a dissipation of 100 µW.

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MOSFET serves as ultrafast plate driver

Clive Bolton, Bolton Engineering Inc, Melrose, MA

The circuit in **Figure 1** provides a 20-MHz square wave across a set of highly capacitive ion-deflection plates in an experimental instrument. To get the required deflection, the plate voltage must be 20 to 30V, much higher voltage than conventional logic or driver families can provide. To minimize artifacts, the rise and fall times must be very fast, with a minimum of overshoot and ringing. Identical circuits, phased 180° apart, drive the plates. The driver uses a Directed Energy (www.directedenergy.com) DEIC420 high-speed MOSFET gate driver to drive a 1000-pF capacitive load from 0 to 25V in less than 5 nsec. With smaller loads of a few hundred picofarads, the rise time decreases to approximately 3 nsec. Series resistors R_1 and R_2 control the output rise and fall times, allowing you to trade off the rise and fall times against overshoot and ringing. A high-speed Analog Devices (www.analog.com) ADUM1100BR ferromagnetic signal isolator prevents system ground loops by providing dielectric isolation for the input signal; you could also use high-speed optocouplers. A low-power MC78L05CD regulator provides power for the signal-isolator output stage.

A snubber network, composed of a thin-film, high-power resistor R_3 in a TO-220 package and high-quality NP0 capacitors C_1 and C_2, terminates the load at the plates. You empirically determine snubber values by observing the radiated field on an RF spectrum analyzer using a passive RF probe. You "tune" the snubber network to reduce higher order signal harmonics. Note that placing an oscilloscope probe on the outputs significantly increases the observed higher order harmonics, indicating that adding the probe to the circuit increases ringing and overshoot. The DEIC420 is mounted in a high-speed, high-power package that minimizes lead inductance. The part requires multiple bypass capacitors at each of its power pins. You should choose the capacitors so that their self-resonant frequencies do not significantly overlap. Having a full ground plane and using high-speed and RF-signal-layout techniques are critical to the proper operation of this circuit. The input must be well-isolated from the output. Double-pulsing, ringing, and even oscillation may occur if you don't strictly follow these practices. The tracks or cabling between the driver and the load should be impedance-controlled and should be as short as possible. The DEIC420 requires good heat-sinking when you operate it at high speeds and high voltages. When operating at 20 MHz from a 25V supply, the two drivers and snubber together dissipate 130W.

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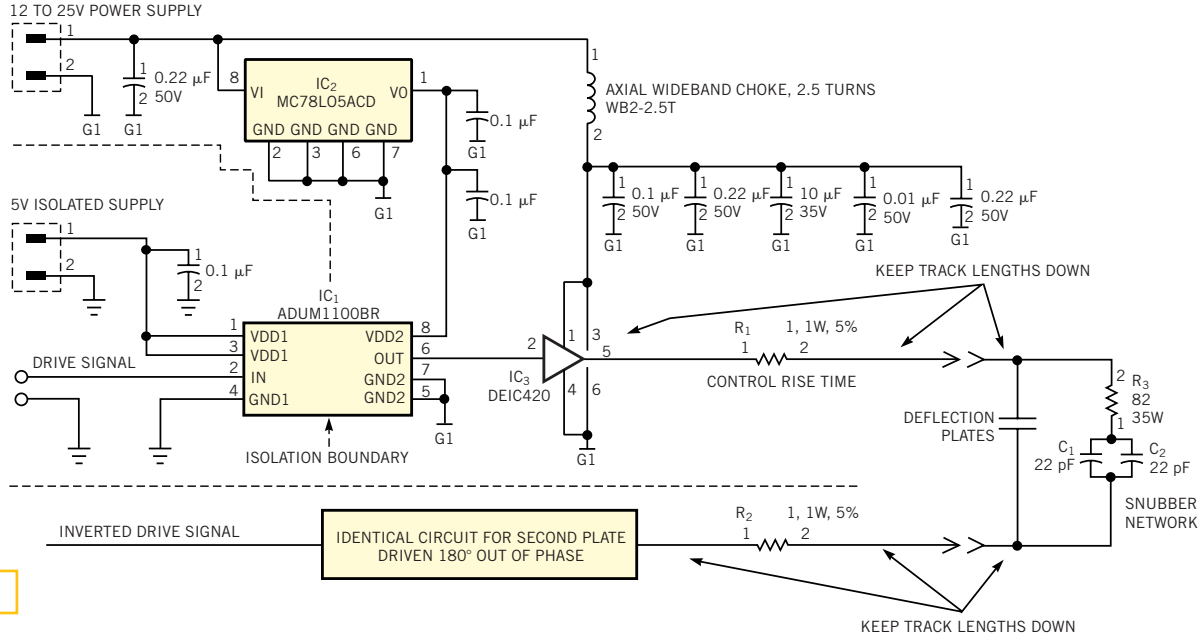


Figure 1

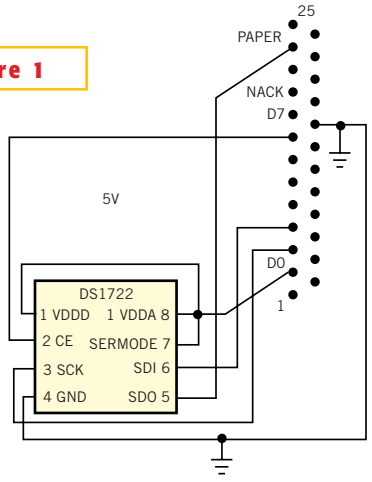
You can use a high-speed, MOSFET-driver IC to drive ion-deflection plates.

Parallel port provides high-resolution temperature sensing

Martin Connors and Mike Foote, Athabasca University, AB, Canada

HIGH-RESOLUTION temperature sensing at low cost is possible using only one chip attached to the PC's parallel port (**Figure 1**). The Dallas Semiconductor (www.dalsemi.com) DS1722 digital thermometer allows measurement resolution as fine as 0.0625°C in digital form and with linear response. The accuracy specification is only 2°C, but you can improve this figure by careful calibration. Moreover, the accuracy spec is unimportant in applications in which you measure only changes in temperature or in which you must closely maintain a noncritical temperature. The measurement range is −55 to +120°C, the part can use either three-wire or SPI interface, and the cost is approximately $1. The eight-pin part is available in SO or µSOP packaging and in large quantities as a flip-chip measuring only about 1 mm sq.

Figure 1



The DS1722 connects to a PC's parallel port through a male DB-25 connector, seen from the pin side.

In this application, the chip attaches directly to the PC's parallel port through a male DB-25 connector. Because the device draws a maximum of 0.5 mA, the port can supply the power, and its supply range tolerates variations in voltage levels that may exist on varying ports. The chip is in SPI mode with the SCK

LISTING 1—TURBO C FOR DATA-TRANSFER CYCLE

```
#include <stdio.h>
#include <dos.h>
#include <conio.h>
#include <process.h>
#include <alloc.h>

#define VDD_ON  0x01  /* power to PIC through VDD_ON on pin 2 (D0) */
#define SCK     0x02  /* serial clock for SPI provided by PC      */
#define PCSDO   0x04  /* serial data out from PC on Data bit 2    */
#define PCSDI   0x20  /* note this is on Status register (bit 1)  */
#define SSOUT   0x40  /* =CE, active high, not low as for PIC SPI */
#define MCLR_HI 0x80  /* MCLR* on pin 9 (Data bit 7) normally high */
#define OPERATE VDD_ON | MCLR_HI  /* normal operation of DS1722   */
/* adjust these to match the CPU speed */
#define DELTIME 10000          /* settling time after transfers */
#define SECDELA 10000000       /* to get about 1 s sampling     */

void dodelay(long);
void outportd(unsigned char);
int dport,sport;

void main(void)
{
unsigned char LSB,transfer(unsigned char,unsigned char);
char MSB; /* note this is signed */
void outportd(unsigned char outbyte);
int i,j,it;
float T;

/* LPT1 port addresses */
if(!(dport = peek(0x40,0x08)))
 { printf("\n\n\nLPT1 not available... aborting\n\n\n"); exit(1); }
sport = dport + 1; /* status port address */

/* initialize the Printer DATA Port for PIC operation */
/* includes putting SCK in the neutral 0 position: ~ is bitwise negation */
outportd(OPERATE&~SSOUT);

printf("hit key to stop list\n");
transfer(0x80,0xE8);  /* initialize DS1722 */
for(j=0;j<20;j++)
 { if(kbhit()) break;
   printf(" config %X: ",transfer(00,0));   dodelay(SECDELA);
   printf(" LSB %X: ",LSB=transfer(0x01,0)); dodelay(SECDELA);
   printf(" MSB %X: ",MSB=transfer(0x02,0)); dodelay(SECDELA);
   printf("T=%10.4f\n",T=MSB+(float)LSB/256.);
 } /* for loop */
}

unsigned char transfer(unsigned char outbyte,unsigned char outdata)
{ /* output address byte on Data2, data byte, getting inbyte on Status5 */
  unsigned char outmask,inbyte,statusmask;
  int ibit;
  inbyte=0x00;
/* raise SSOUT for 2 byte transfer, SCK also in lowered neutral position */
  outportd(OPERATE|SSOUT);
  for(ibit=0;ibit<8;ibit++)                  /* output outbyte  */
  { outportd(OPERATE|SCK|SSOUT);             /* raise clock SCK */
    outmask=outbyte&0x80; outbyte=outbyte<<1;
    if(outmask)outportd(OPERATE|SCK|PCSDO|SSOUT);   /* output of 1 or  */
      else outportd(OPERATE|SCK|SSOUT);             /* of 0 on PCSDO   */
    if(outmask)outportd(OPERATE|PCSDO|SSOUT);       /* lower clock SCK */
      else outportd(OPERATE|SSOUT);                 /* retaining data  */
  }
  for(ibit=0;ibit<8;ibit++)                  /* output outdata  */
  {                                          /* & input inbyte  */
    outportd(OPERATE|SCK|SSOUT);             /* raise clock SCK */
    outmask=outdata&0x80; outdata=outdata<<1;
    if(outmask)outportd(OPERATE|SCK|PCSDO|SSOUT);   /* output of 1 or  */
      else outportd(OPERATE|SCK|SSOUT);             /* of 0 on PCSDO   */
    if(outmask)outportd(OPERATE|PCSDO|SSOUT);       /* lower clock SCK */
      else outportd(OPERATE|SSOUT);                 /* retaining data  */
    statusmask=inportb(sport);               /* read status port*/
    statusmask=statusmask&PCSDI;             /* mask input line */
    inbyte=inbyte<<1; inbyte=inbyte&0xFE; inbyte|=statusmask>>5;
  }
/* lower SSOUT at end of 2 byte transfer, lower SCK to neutral position  */
  outportd(OPERATE&~SSOUT);
  return inbyte;
}

void outportd(unsigned char outbyte)
{ dodelay(DELTIME); outportb(dport,outbyte); dodelay(DELTIME); }

void dodelay(long deltime)
{ long i; for(i=0; i<deltime; i++) ; }
```

clock signal supplied by the PC; in this way, data-transfer timing is noncritical. A simple Turbo C program (**Listing 1**) running in DOS mode effects the data-transfer cycle in the PC, whereas the transfer is automatic in the chip upon reception of SCK. The routine reads a low byte and a signed high byte and creates a floating-point value by simply adding the low byte, divided by 256, to the high byte. In the highest resolution mode, which this design uses, a data read can occur only every 1.2 sec, and you should adjust the timing loops accordingly. You may also need to adjust the settling time, DELTIME, depending on the speed of the PC you use. The sample program prints the bytes transferred as well as the temperature, and you can easily modify it. The data sheet explains the use of the configuration register and changes to make if you need a higher data rate with lower resolution. You can download **Listing 1** from the Web version of this Design Idea at www.ednmag.com.

The data transfer takes place beginning with the write of an address byte to the chip's SDI in the order A7 to A0 (high bit to low bit). If A7 is high, a write takes place; otherwise, a read occurs. For a write, D7 to D0 route to the chip's SDI. For a read, D7 to D0 are available on the chip's SDO. The program always uses both SDI and SDO and ignores whichever it doesn't need. For example, data goes to the chip's SDI even during a read, but the chip ignores this data. Each byte transfers as 8 bits, and each transfer involves the following steps:

1. The PC raises D1/SCK and places 0 or 1 on D2 for the chip's SDI.
2. The PC then reads PAPER.
3. Finally, the PC drops D1/SCK.

This action repeats for each bit of the pair of bytes being transferred (one in, one out). By using the other parallel port's output pins as chip selects, you could string together several devices. You can also use these pins to control a heater by use of a switching transistor or an SCR. With this scheme, you can achieve high-resolution temperature control with minimal parts and a simple program. Alternatively, if you need only low accuracy, you can implement a very-low-cost thermostat with this part.

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design ideas

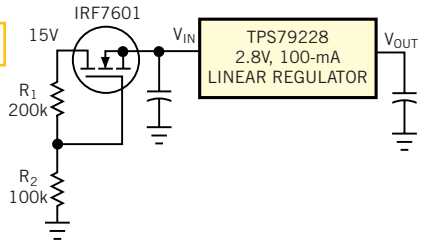
Edited by Bill Travis

Extend the input range of a low-dropout regulator

Jeff Falin, Texas Instruments, Dallas, TX

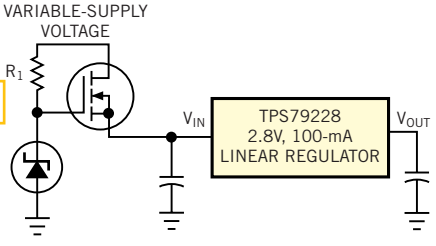
Because of process limitations, all ICs have an input-voltage limitation. This limitation can be cumbersome when you try to step down a high supply voltage to a lower, regulated voltage using a dc/dc converter, such as a linear regulator. Adding a FET to the input of a linear regulator creates a dc/dc converter with a wider input-voltage range than the range of the regulator alone. The excess voltage and, therefore, power occurs in the FET.

Figure 1



You can use a MOSFET switch to expand a low-dropout regulator's input-voltage range.

Figure 2



A zener diode provides fixed gate drive to the MOSFET when the input voltage varies significantly.

Figure 1 shows an IRF7601 n-channel MOSFET on the input of a TPS79228 2.8V, 100-mA, low-noise, high-power-supply rejection ratio low-dropout regulator. R_1 and R_2 provide a bias voltage to the gate of the MOSFET, and the load current determines the voltage at the source of the MOSFET. (In other words, the FET's on-resistance adjusts to accommodate the load current.) In this example, the maximum power-supply voltage is 15V, but the TPS79228 has a maximum recommended operating input voltage of 5.5V, so this design uses a MOSFET with a 20V breakdown voltage.

To determine the minimum bias voltage for the gate of the MOSFET, you need the MOSFET's drain-current, I_D,-versus-gate-source voltage, V_{GS}, data-sheet curves. For the IRF7601, the curves indicate that the device needs V_{GS} slightly below 1.5V for 100-mA output current. Because the maximum dropout voltage of the regulator is 100 mV at 100 mA, the regulator's input voltage must stay above 2.9V. Therefore, you must bias the gate of the MOSFET to at least 1.5V+2.9V=4.4V. Thus, when the MOSFET provides 100 mA, its source voltage does not drop below 2.9V. The maximum gate-bias voltage is simply the maximum recommended operating voltage for the regulator, or 5.5V. This voltage provides more than enough gate drive to provide the regulator's 1 µA of quiescent current during shutdown mode. Although you can bias the gate between 4.4 and 5.5V, this design uses a bias voltage of 5V to account for variations in the threshold voltage. Maximum power dissipation for the FET is 100 mA×(15V−2.9V)=1.21W. The IRF7601, in a Micro 8 package, can handle this power figure at an ambient temperature of 55°C.

The circuit in **Figure 2** is slightly more complicated but may be necessary if the input voltage varies significantly. A zener diode replaces the R_2 in **Figure 1** and provides a fixed gate drive to the MOSFET. You select the output voltage of the zener diode in a manner similar to that explained above. Either of the two methods is acceptable for creating a dc/dc converter with a wider input-voltage range than the converter IC allows. The single-MOSFET solution is the simplest and least expensive solution. The MOSFET biased with a zener diode is the best choice when the supply is unregulated.

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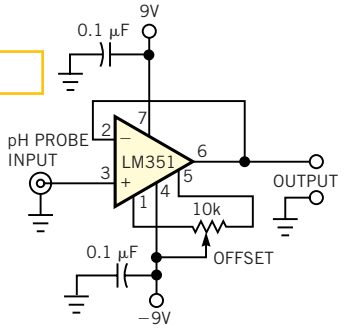
Convert your DMM to a pH meter

Bill Donofrio, Nu-Products, Cordova, TN

It's often necessary to know the acidity of a solution to control a process. Even inexpensive pH meters can be relatively costly, and many of the inexpensive models have no output that you can readily connect to a computer interface. A simple solution to this problem is to attach a pH probe to a high-impedance input of an op amp and read the output with a digital voltmeter (**Figure 1**). Then, convert these readings to pH units using a calculator that can calculate the slope of a line. To calibrate the system, you can use pH standards. Generally, you would use three standards: 4-, 7-, and 10-pH units. These standards are inexpensive and available at any chemical-supply house. The calibration procedure is as follows:

1. Short the input leads together and adjust the offset potentiometer such that the output reads 0 mV.
2. Place the pH probe in each standard and record the output (in millivolts) for each standard.
3. Enter the values in your calculator and determine the slope of the line.

Figure 1



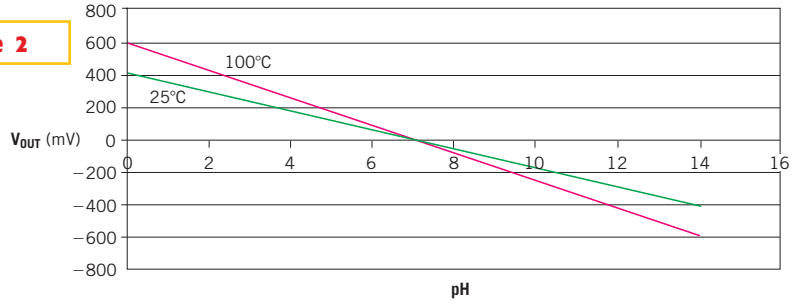
This simple pH tester uses a digital voltmeter and a calculator to determine the slope of a line.

Figure 2 shows a typical plot of pH versus millivolt output. (Note that pH is temperature-dependent; you have to recalibrate if the temperature changes.)

If you want to measure directly in pH units, you can use the circuit in **Figure 3**. At approximately 24°C, the equation for the slope of the line is $Y=-0.017X+7$. To obtain readings in tenths of volts, you multiply the equation by 10. The new equation is $10Y=-0.17X+70$. The circuit in **Figure 3** comprises three sections. The voltage using the LM351 provides the high-impedance input. The inverting amplifier using one-half of the LM353 controls the slope. It multiplies the LM351's output by −0.17. The other half of the LM353 functions as a summing amplifier and controls the Y intercept by adding 70 mV to the input signal. When you build this circuit, solder the BNC directly to the op amp's input pin. This connection prevents slightly conductive pc boards from affecting the impedance levels of the probe. Another point to remember is to remove the pH probe from the unit when power is off.

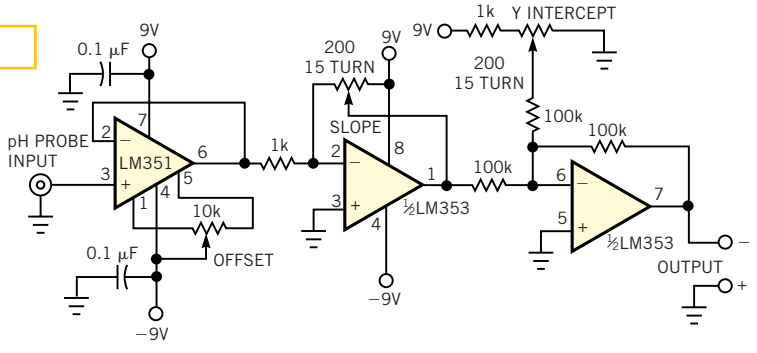
To calibrate the circuit, first short the inputs together and adjust the offset potentiometer to obtain 0-mV output from the LM351. To calibrate the circuit for pH units, place the pH probe into a pH standard. Measure the voltage at the output of the LM351. Multiply this voltage by 0.17 and adjust the slope potentiometer until the output of the second op amp reads this inverted (negative) value. Then, connect the meter to the output of the circuit and adjust the Y-intercept potentiometer until the circuit yields the pH of the standard you use. (For example, a pH of 10.1 reads 0.101V.) To tweak the circuit, place the pH probe in other standards and adjust the Y-intercept potentiometer. Note again, if the temperature changes, you must recalibrate. The accuracy of this circuit is generally ±0.1 pH units. When you order pH probes, you should order low-impedance units. This circuit uses Cole-Parmer (www.coleparmer.com) U-59001-65 probes.

Figure 2



Available pH probes produce a linear slope of output voltage versus pH.

Figure 3



With this circuit, you can directly measure pH units.

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AVR microcontroller makes improved motor controller

Anthony Di Tommaso, Cranberry Township, PA, and George Simonoff, Petersburg, OH

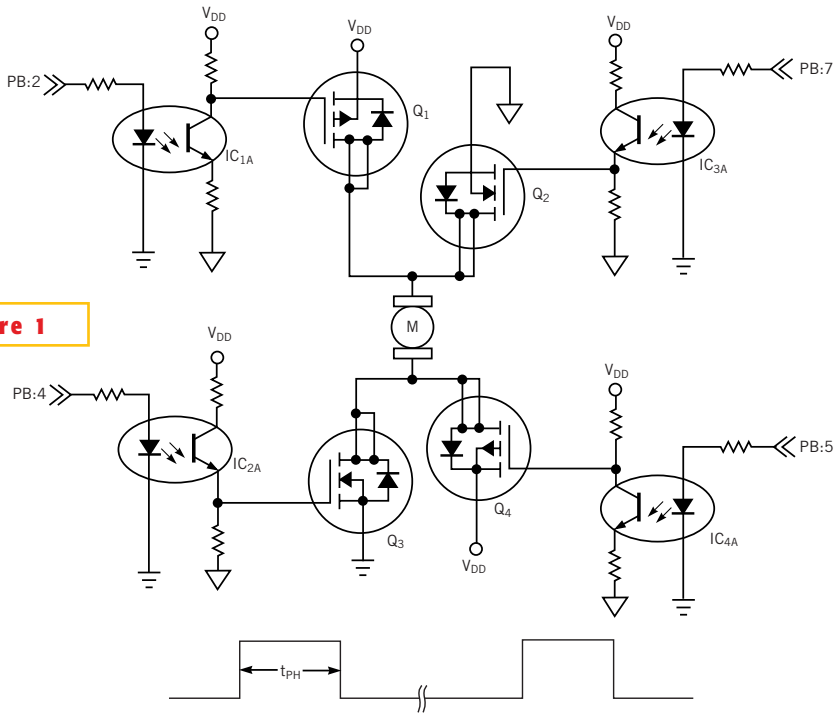
The circuit in **Figure 1** provides a novel method of reading the pulse train using an Atmel (www.atmel.com) AVR processor, from a typical radio-controlled receiver, and to determine the velocity of a motor. To capture the pulse train from a typical receiver, you need an external interrupt that triggers based on a rising and a falling edge. Three timers are also necessary: one 16-bit, free-running timer to determine the period of the input pulse and two 8-bit timers con-

LISTING 1—MOTOR-CONTROL C LISTING

```
#include <io.h>
#include <interrupt.h>
#include <signal.h>

unsigned char c17;                  //Used to indicate the present direction of motion.
unsigned short s23;                 //Used to hold the 16 bit Timer 1 count.

SIGNAL(SIG_INTERRUPT4)
{
volatile unsigned char ptr;
unsigned char lower_byte;
unsigned char upper_byte;

        lower_byte = 0;             //Clear bytes in anticipation of receiving
        upper_byte = 0;             //new data.
        c17 |= 0x04;                //Set global for control is with receiver.
        ptr = inp(EICR);            //Get present state of EICR.
        if ((ptr & 0x01) == 0)      //If falling edge capture enabled, then ...
        {
                c17 |= 0x08;                    //Indicate arithmetic operation can proceed
                lower_byte = inp(TCNT1L);       //Move low part of count to low byte.
                upper_byte = inp(TCNT1H);       //Move high part to high byte.
                s23 = upper_byte;               //Create 16 bit word that represents period
                s23 <<= 8;                      //of pulse.
                s23 += lower_byte;
        }
        else                                    //If rising edge capture enabled, then ...
        {
                c17 &= 0xF7;                    //Indicate arithmetic operation should wait
                outp(0,TCNT1H);                 //Reset timer counter register.
                outp(0,TCNT1L);                 //When writing to 16 bit timer, must write
                                                //to upper register first.
        }
        ptr = inp(EICR);                        //Change state of last bit of EICR
        ptr ^= 1;                               //in order to be able to trap on the
        outp(ptr,EICR);             //opposite edge.
}

int initialize(void);
int receiver_cntrl(void);

int main(void)
{

        initialize();                           //Call initialize in order to set
                                                //up registers and peripherals.
        s23 = 0;                                //Initialize useful variables,
        c17 = 0;                                //some that are global and some
                                                //that are local to main.
        while (1)
        {
                receiver_cntrl();
        }
}
int initialize(void)
{
        //Timer 0 Setup Code
        outp(0x61,TCCR0);       //No prescale to clk, enable PWM, clear PWM output
        outp(0,OCR0);           //Set output compare register to 0.
        outp(0,TCNT0);                  //Set timer counter to 0.
        //Timer 1 Setup Code
        outp(0,TCCR1A);         //Set clk source as clk/8, compare timer to overflow
        outp(0x0A, TCCR1B);     //Set output compare register to 0xFF00.
        outp(0xFF, OCR1AH);     //Not used, however.
        outp(0,OCR1AL);         //Set output compare register to 0.
        outp(0,TCNT1H);         //Set timer 1 counter to 0.
        outp(0,TCNT1L);
        outp(0x10,TIMSK);       //Enable timer overflow interrupt.
        //Timer 2 Setup Code
        outp(0x61,TCCR2);       //No prescale to clk, enable PWM, clear PWM output
        outp(0,OCR2);           //Set output compare register to 0.
        outp(0,TCNT2);                  //Set timer counter to 0.
        //External Interrupts Setup Code
        outp(0x10,EIMSK);       //Enable interrupts for externals 0 through 4.
        outp(0x03,EICR);        //The rising edge between two samples of INT4
                                //generates an interrupt.
        outp(0x80,ACSR);        //Disable comparator.
        //Port B Setup Code
        outp(0xff,DDRB);        //Set initial direction of port pins to output.
        outp(0,PORTB);                  //Set initial state of pins.
        //Port D Setup Code
        outp(0x0,DDRD);         //Set initial direction of port pins to input.
        outp(0xff,PORTD);       //Set initial state of pins.
        //Port E Setup Code
        outp(0,DDRE);           //Set initial direction of port pins to input.
        outp(0,PORTE);                  //Set initial state of pins.

        sei();                  //Globally enable all active interrupts.

        return(0);
}
int receiver_cntrl(void)
{
volatile unsigned char ptr;

        c17 &= 0xF7;            //Enable receiver mode
        s23 -= 0x01EE;          //Set up map range
        if ((s23 >= 0xF0) && (s23 <= 0x110))    //See if s23 is in the deadband.
        {                               //If so, then stop the motor.
                ptr = inp(PORTB);       //Get present state of output drivers.
                ptr &= 0xDB;    //Block movement by setting PB:2 and PB:5 to 0
                outp(ptr,PORTB);        //Update state of driver.
                outp(0,OCR0);   //Set PWM0 to 0% disabling forward.
                outp(0,OCR2);   //Set PWM2 to 0% disabling reverse.
                c17 &= 0xFC;    //Modify global to indicate direction is stop.
        }
        else if ((s23 > 0x110) && (s23 <= 0x1FF))       //See if s23 is in fwd range
        {                                               //If so, then proceed with fwd.
                if ((c17 | 0xFD) == 0xFD)               //If global indicates present
                {                                       //direction is not reverse. then ...
                        outp(0,OCR2);   //Block reverse by shutting down PWM2.
                        outp(ptr, PORTB);       //Update value of port B.
                        ptr = (volatile unsigned char)s23;      //Assign movement to ptr.
                        outp(ptr, OCR0);        //Assign PWM to new movement value.
                        ptr = inp(PORTB);       //Get present state of port B.
                        ptr |= 0x04;    //Indicate that the direction is forward.
                        outp(ptr,PORTB);        //Update the value of the port.
                        c17 |= 0x01;    //Set global bit to indicate forward.
                        c17 &= 0xFD;    //Set global bit to not indicate reverse.
                }
        }
        else if ((s23 >= 0) && (s23 < 0xF0))    //See if s23 is in rev range
        {                                       //If so, then proceed with rev.
                if ((c17 | 0xFE) == 0xFE)       //If global indicates present
                {                               //direction is not forward, then ...
                        outp(0,OCR0);   //Block forward by shutting down PWM0.
                        ptr = inp(PORTB);       //Get present value of port B.
                        ptr &= 0xFB;    //Stop forward by setting driver to 0.
                        outp(ptr,PORTB);        //Update value of port B.
                        ptr = -(volatile unsigned char)s23;//Assign movement to ptr.
                        outp(ptr, OCR2);        //Assign PWM to new movement value.
                        ptr = inp(PORTB);       //Get present state of port B.
                        ptr |= 0x20;    //Indicate that the direction is forward.
                        outp(ptr,PORTB);        //Update the value of the port.
                        c17 |= 0x02;    //Set global bit to indicate reverse.
                        c17 &= 0xFE;    //Set global bit to not indicate reverse.
                }
        }
        return(0);
```

figured as PWMs (pulse-width modulators) for driving the motor in both forward and reverse. Finally, two digital outputs act in concert with the PWMs to move the motor. You can find all these features in an AVR microcontroller. Assuming that you use a typical transmitter and receiver, such as a pair from Futaba (www.futaba.com), the range of pulse width, t_{PH}, should vary from 1 to 2 msec for full reverse and full forward, respectively. If the Timer 1 clock-source frequency is 500 kHz, the number of counts possible between full reverse and full forward is 500, beginning at 500 for a pulse width of 1 msec and ending at 1000 for a pulse width of 2 msec. A pulse width of 1.5 msec identifies no-input or full-stop conditions. **Listing 1** provides an example of this motion-control application.

Figure 1



An Atmel AVR microcontroller provides a novel method of controlling a motor.

Subtract 494 ($1EE) from the value of Timer 1, captured after the falling edge of the pulse, assuming that the pulse is positive-going and that, at the rising edge of the pulse, the value of the counter resets. The range of values between full reverse and full forward becomes 6 to 506 ($6 to $1FA). Forward motion is $101 to $1FA, with $101 providing the least forward motion and $1FA providing the most forward motion. Reverse motion ranges from $FF to $6, with $FF providing the least amount of reverse motion and $6 providing the most amount of reverse motion. If negated, the reverse range becomes $01 to $FA. If you use the lower byte of the adjusted Timer 1 value directly to set the output comparison registers OCR0 or OCR2 of Timer 0 or Timer 2, you can use as much as 98% of the range of input values to the PWM. You can choose which PWM-configured timer to use based either on where the value occurs in the range or on the upper byte. Note that when the upper byte is 1, the direction is forward; when the upper byte is 0, the direction is reverse. You can download the C-based **Listing 1** from the Web version of this Design Idea at www.ednmag.com.

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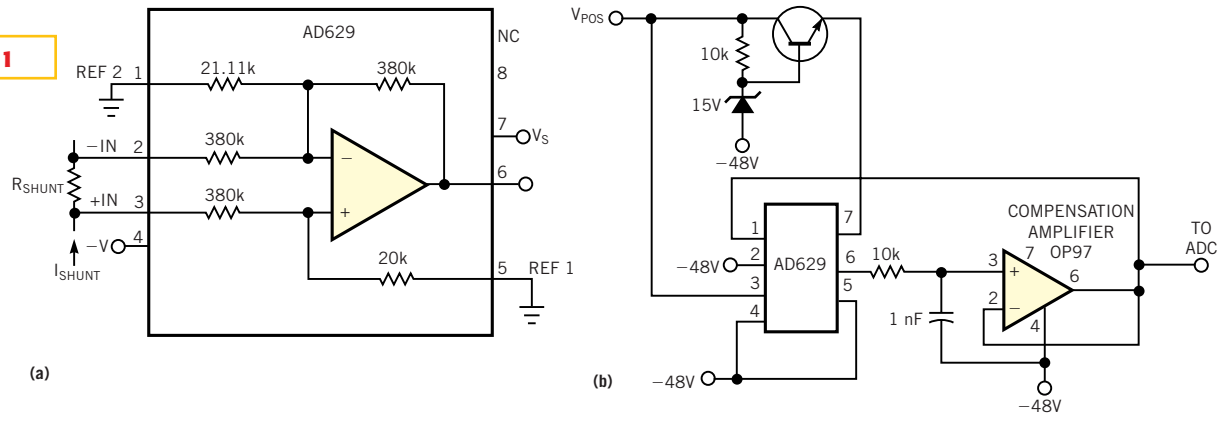
Precision circuit closely monitors −48V bus

Paul Smith and Jim Staley, Analog Devices, Wilmington, MA

Ever-greater complexity in communications systems has spurred a need for power-supply management. POTS (plain-old telephone systems) obtain power from −48V supplies backed by arrays of batteries in central offices and distributed throughout copper lines. Although nominally −48V, the voltage on the lines can vary from −40 to −80V, and the voltage is subject to surges and fluctuations. Supply regulation at the source has little effect on remote voltage levels. Equipment failures resulting from surges, brownouts, or other line faults may sometimes be undetectable. Capturing power-supply information from remote communications equipment requires precise measurement of the voltages—sometimes in outdoor temperatures. High-common-mode, voltage-difference amplifiers have been useful in monitoring current. However, you can also use these versatile components as voltage dividers, enabling remote monitoring of voltage levels as well.

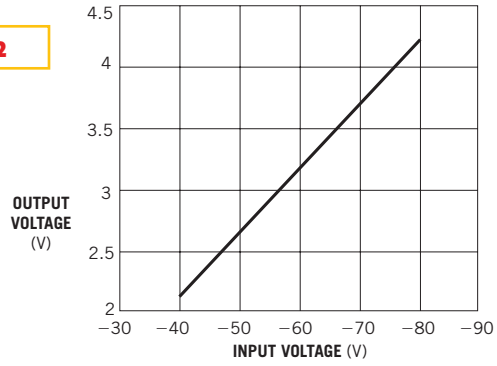
Figure 1a shows the basic circuit connections when you use a difference amplifier for high-line current sensing. With the addition of a few parts, you can operate this amplifier in a negative-supply system. **Figure 1b** shows a precision monitor using just two ICs and deriving its power from the −48V supply. All you need to power the circuit are a transistor and a zener diode to reduce the supply voltage for the amplifiers. The AD629

Figure 1



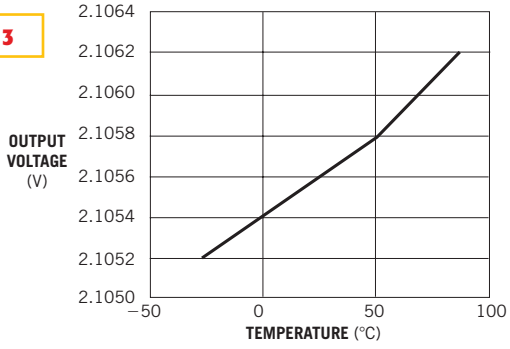
A basic monitoring circuit (a) uses a difference amplifier for high-line current sensing; the complete circuit (b) requires just two ICs.

Figure 2



The circuit in Figure 1b produces an output that's a linear function of the negative supply voltage.

Figure 3



Temperature drift in the circuit of Figure 1b is negligible.

shown in **Figures 1a** and **1b** is a self-contained, high-common-mode, voltage-difference amplifier with unity gain. Connected as shown, however, it reduces the differential-input voltage by approximately 19, thus acting as a precision voltage divider. You need an additional amplifier for loop stability. The circuit features several advantages over alternative approaches. The laser-trimmed divider resistors exhibit essentially perfect matching and tracking over temperature. Linearity errors from −40 to −80V are nearly immeasurable. **Figures 2** and **3** show the linearity and temperature-drift curves for the monitoring circuit.

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PLD code reveals pc-board revisions

Clive Bolton, Bolton Engineering Inc, Melrose, MA

The PLD (programmable-logic-device) code in **Listing** 1 implements a pc-board-level revision-detection system that detects whether PLD pins are shorted together on a pc board. It is often advantageous to field a single PLD programming file that works for several generations of physical hardware. The PLD needs to understand what the board revision is, so that it can enable or disable functions, pins, or both to external circuitry. If a designer has not placed physical straps to indicate a pc-board-revision level from the start, it may be difficult to add them later. In PLD families that have no integral pin-pullup or -pulldown resistors, redefining previously unused pins as inputs means that these pins float, either causing erratic operation or indicating an improper pc-board-revision level.

TABLE 1—PATTERN-GENERATOR ACTIONS

State	REV_OUT line	REV_IN[x] lines
0	Tristated	Drive low
1	Tristated	Tristated
2	Drive with pattern	Look for pattern
3	Tristated	Tristated

The software module generates a short, simple pattern, such as a square wave, onto a driver pin, REVO_OUT. The input-detection pins, REVI_IN[x], look for this pattern. If they detect the full pattern on a pin, the module indicates that the pins are connected by setting the respective Q[x] high. If they do not detect the full pattern, the module sets the Q[x] line low. The pattern generator avoids leaving the revision-detection inputs floating by alternately driving and tristating the REVO_OUT and REVI_IN[x] lines (**Table 1**). If you drive the circuit at more than a few megahertz, the parasitic pin capacitance of a few picofarads is sufficient to ensure that the REV_I[x] pins stay low, even while they are tristated. When the detection cycle is finished, the COMPLETE line goes high.

The module generates the required hardware from two compile-time parameters: LPM_WIDTH and CHANNELS. LPM_WIDTH sets the number of times the detection cycle runs (for example, 5 bits yields 2^5, or 32 cycles), and CHANNELS sets the number of strap inputs. Note that this function does not include tristate buffers; you must instantiate them at the design top level. The REVO_EN and REVI_EN pins enable the REVO_OUT and the REVI_IN[x] tristate buffers, respectively. The PLD code is written in Altera's (www.altera.com) high-level design language (AHDL); you can directly compile it into any of Altera's PLDs. An implementation of the design with the parameters set to the default values takes 16 logic cells in an Altera EP1K50BC256-3—less than 1% of the device—and runs at rates as high as 185 MHz. Although the code is written for Altera's devices, the design structure and flow are readily translatable into VHDL or Verilog.

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LISTING 1—AHDL CODE FOR REVISION DETECTION

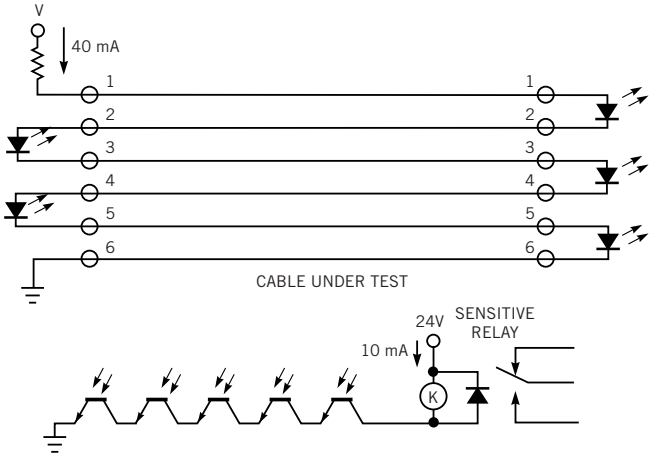
```
% TITLE rev_detect.tdf: AHDL file                                        %
% path: f:\project3\altera\rev_detect.tdf                                 %
% (c) 2002 Bolton Engineering, Inc. All rights reserved                   %
% size of 16 LCs in 1K10-3, 185MHz clk operation                          %
% 02/18/02. Code started, tested, and entered into RCS                    %

INCLUDE "lpm_counter.inc";

PARAMETERS  (
      LPM_WIDTH    = 5,   -- in bits; sets the length of time for detection
      CHANNELS     = 1          -- number of strap inputs (1 or more)
);

SUBDESIGN rev_detect
(
      clock                         :     INPUT;             -- global clk
      aclr                          :     INPUT;

      revi_in[CHANNELS-1..0]  :     INPUT;             -- strap inputs for all
"inputs"
      revi_en                             :     OUTPUT;            -- tristate
enable

      revo_out                      :     OUTPUT;            -- strap output
      revo_en                             :     OUTPUT;            -- tristate
enable

      q[CHANNELS-1..0]        :     OUTPUT;            -- 1 if connected, 0 if
N.C.
      complete                      :     OUTPUT;
)
VARIABLE
      phase_cntr                    :     LPM_COUNTER WITH (      LPM_WIDTH
= 2,

      LPM_DIRECTION = "UP");
      seq_cntr                      :     LPM_COUNTER WITH (      LPM_WIDTH
= LPM_WIDTH,

      LPM_DIRECTION = "UP");
      dffe_q[CHANNELS-1..0]   :     DFFE;
      complete_unr                  :     NODE;
BEGIN
      -- at 0, drive strap "inputs" only
      -- at 1, drive nothing
      -- at 2, drive strap output only
      -- at 3, drive nothing
      phase_cntr.clock  = clock;
      phase_cntr.aclr         = aclr;
      phase_cntr.cnt_en = !complete;

      revi_en           = DFF( (phase_cntr.q[] == 0) OR complete, clock, !aclr,
VCC);
      revo_en           = DFF( (phase_cntr.q[] == 2) OR complete, clock, !aclr,
VCC);

      seq_cntr.clock          = clock;
      seq_cntr.aclr           = aclr;
      seq_cntr.cnt_en         = !complete_unr AND phase_cntr.cout;
      complete_unr            = seq_cntr.cout;
      revo_out                = seq_cntr.q[0];

      complete                = DFF(complete_unr, clock, !aclr, VCC);

      FOR i IN 0 to (CHANNELS-1) GENERATE
            dffe_q[i].clk     = clock;
            dffe_q[i].prn     = !aclr;
            dffe_q[i].ena     = revo_en AND !complete;
            dffe_q[i].d       = dffe_q[i].q AND (revi_in[i] XNOR revo_out);
            q[i]              = dffe_q[i].q;
      END GENERATE;

END;
```

Simple method tests cables

Jim Keith, Bell-Mark Technologies, Dover, PA

ENGINEERS HAVE LONG KNOWN how to test a cable for continuity by simply connecting all conductors in series and checking with an ohmmeter. This method is sometimes impractical, however, because it cannot check for short circuits. The method shown in **Figure 1** solves the short-circuit problem. Connecting LED indicators at each shorting loop provides a visual indication. The beauty of this scheme is that any short circuit causes at least one LED to extinguish. You can then diagnose the malfunction by the visual signature of the LEDs. Taking the method one step further, let the LEDs be the emitters of photocouplers. Connecting the phototransistors in series provides a simple go-no-go test that requires no visual observation. Note that the 2V LED forward-voltage drop presents a challenge when you're testing a cable with a large number of conductors, so be sure to apply a high enough voltage.

Figure 1



This simple cable-testing method tests for continuity as well as short circuits.

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Edited by Bill Travis

DPPs make nonvolatile microvolt DAC

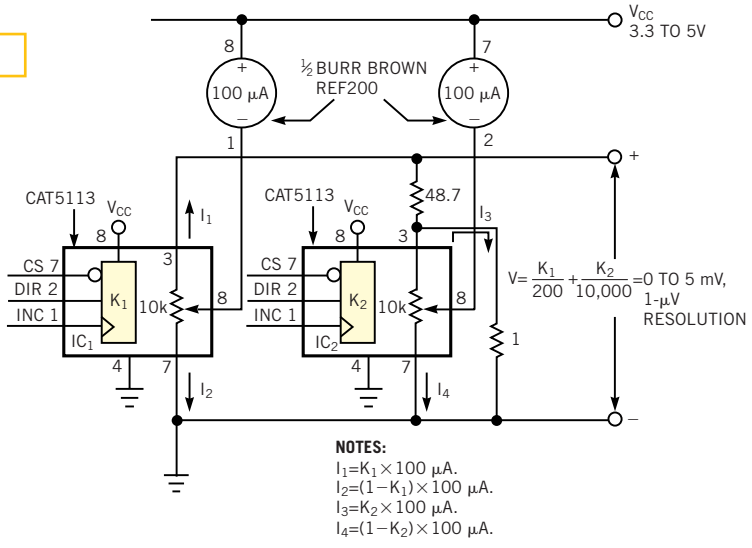
Stephen Woodward, University of North Carolina, Chapel Hill, NC

The availability of a seemingly limitless variety of monolithic DAC chips makes it easy to implement most digital-to-analog-conversion applications with a single off-the-shelf device. Sometimes, an unusual set of requirements necessitates a multichip approach, however. One example of such a requirement is the need for nonvolatility of the DAC's setting in power-up and -down cycles. Another example is the need for output resolution and stability at less than 1 µV. The circuit in **Figure 1** combines inexpensive DPPs (digitally programmed potentiometers) from Catalyst Semiconductor (www.catsemi.com) with precision current references from Burr-Brown (www.ti.com) to achieve both nonvolatility and less-than-1-µV performance. Accurate simulation of the signals from high-temperature platinum-rhodium-based thermocouples requires less-than-1-µV performance. These temperature sensors have Seebeck coefficients of only 6 µV/°C. Therefore, only voltage sources with 1-µV-level stability and precision can simulate such sensors.

To achieve such low output drift would normally require the use of active circuit elements, such as chopper-stabilized amplifiers, with offset temperature coefficients not much higher than 1 nV/°C. The circuit in **Figure 1** takes a different approach by using current division and a passive and, therefore, inherently drift-free output that needs no amplifiers. Each half of the REF200 sources a 100-µA reference current. The twin currents each connect to the wiper of DPPS, IC_1 and IC_2. There, they split into two currents (for example, I_1 and I_2) in a wiper-to-total ratio, K_1, which the programmed setting of the DPP determines. $I_1=K_1\times100$ µA, and $I_2=(1-K_1)\times100$ µA. I_1 passes through the series combination of the 48.7Ω resistor and the 1Ω output resistor and thereby generates the output voltage: $V=K_1(50\Omega\times100\ \mu A)=0$ to 5 mV as K_1 varies from 0 to 1. The operation is straightforward and drift-free. Unfortunately, the resolution with a single potentiometer is inadequate for many precision applications.

IC_1, a CAT5113, like other DPPs, offers the versatility of an uncommitted resistance element and nonvolatility of the setting. Its resolution, however, is only 100 steps, which is slightly worse than 7 bits and equivalent to 50 µV in this circuit. You therefore incorporate a second DPP, IC_2, in the converter. IC_2's output current acts into the 1Ω load for a 50-to-1 resolution enhancement over IC_1 alone. IC_2 thus adds a 0- to 100-µV contribution to V. Hence, the composite output is $V=K_1/200+K_2/10{,}000$ with a 5-mV span and 1-µV resolution. The circuit is an ideal approach for such applications as the simulation of thermocouple signals in precision temperature-measurement and -control systems.

Figure 1



Digitally programmed potentiometers combine to form a novel, microvolt-level DAC.

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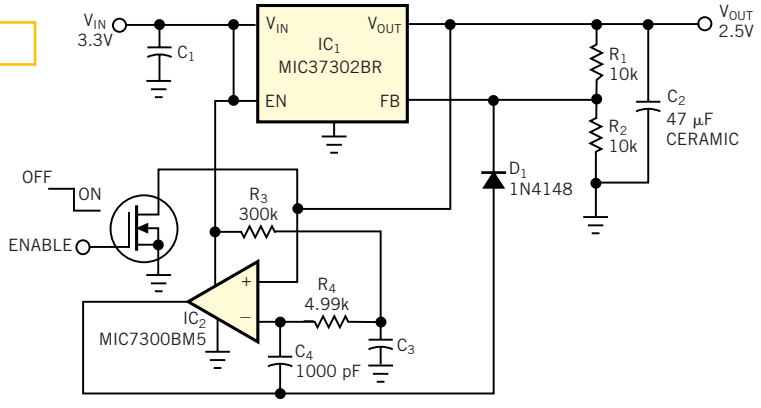
Circuit manages power-up sequencing

Martin Galinski, Micrel Semiconductor, San Jose, CA

Power sequencing poses a unique problem in power management. Because improper sequencing may cause damage to many types of processors, power-up sequencing of these devices is critical. Devices that may require power-up sequencing control include FPGAs, ASICs, and DSP chips. These devices can require tracking I/O and core voltages. Requirements for power-up sequencing may change according to device type and manufacturer, so it's important that you review sequencing requirements for each device. This design use Xilinx's (www.xilinx.com) power-up requirements for the Spartan-II and Spartan-IIE families. The I/O voltage must reach full supply voltage in 2 to 50 msec. Also, the slew rate of the supply voltage must not exceed 900 mV/msec but must exceed 50 mV/msec. The circuit in **Figure 1** addresses these issues, allowing for consistent and reliable power-up sequencing.

The power-up sequencing circuit uses an RC (R_3 and C_3) timing network to control the slew rate of the output during turn-on. IC_2 compares the output of the low-dropout regulator with the voltage at the RC network. It then adjusts the output of the regulator, via the feedback voltage, to match the RC charge voltage. When the voltage between R_3 and C_3 reaches the low-dropout regulator's regulation voltage, the output of IC_2 pulls low, reverse-biasing D_1, thereby removing the power-up sequencing circuit from the control loop. R_4 and C_4 provide compensation to maintain a smooth voltage during the turn-on cycle. R_1 and R_2 provide the output regulation voltage. You can calculate R_1 and R_2 from the following expression: $R_1 = R_2 (V_{OUT}/1.240 - 1)$. **Figure 2** shows slewing characteristics of the output with various values of C_3.

Figure 1



This circuit controls the power-up sequencing for Xilinx's Spartan ICs.

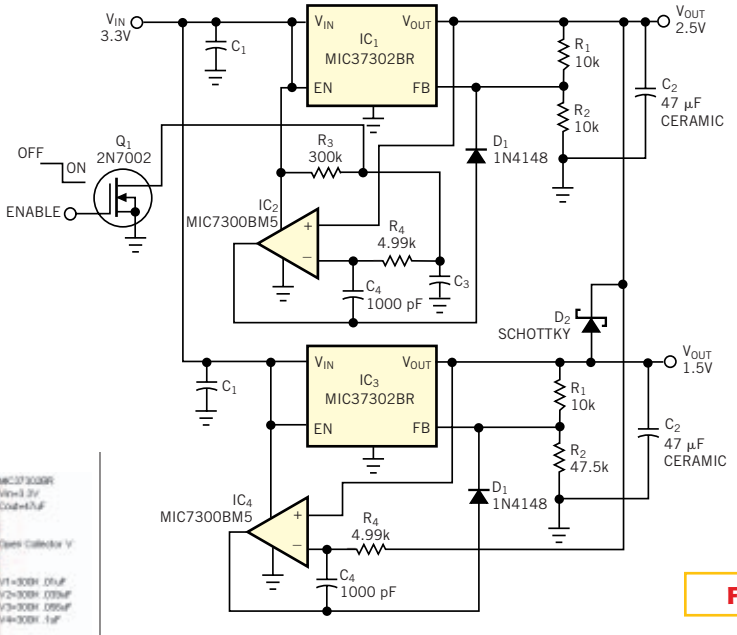


Figure 3

This circuit controls the I/O and core-voltage power-on and power-off sequencing.

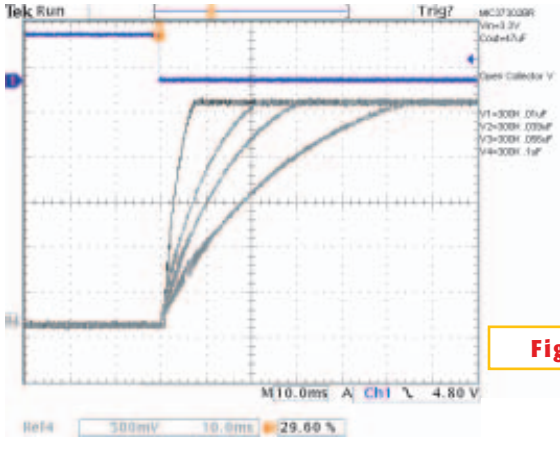


Figure 2

C_3 controls the rise time of the output of Figure 1's circuit.

Figure 3 is an I/O and core-voltage-sequencing circuit. Instead of using an RC charge voltage to control the turn-on, IC_3 of the core regulator compares the output of the I/O during turn-on and matches the core voltage until it reaches the regulation voltage. **Figure 4** shows the I/O and core voltages during the power-on cycle. Equally important is the power-down cycle. The I/O voltage must never reach 0.6V below the core voltage. This condition can forward-bias the substrate diode, damaging the processor. D_2, a Schottky diode with a forward voltage drop of 0.4V, keeps the I/O voltage from dropping 0.6V below the core voltage during the power-down cycle (**Figure 5**).

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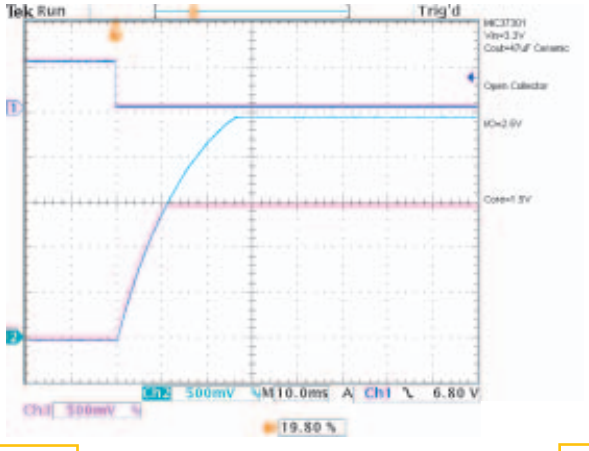


Figure 4

The I/O and core voltages have controlled rise times during the power-on phase.

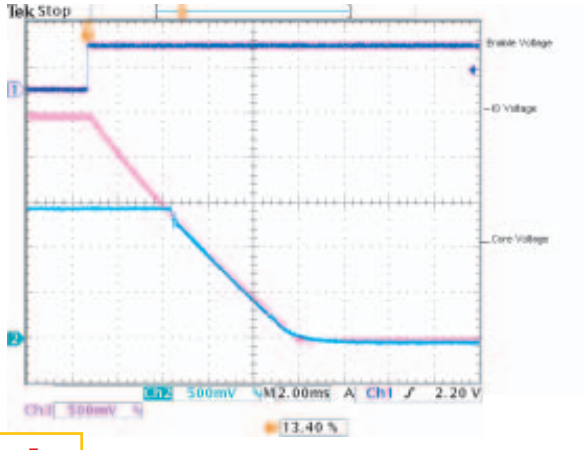


Figure 5

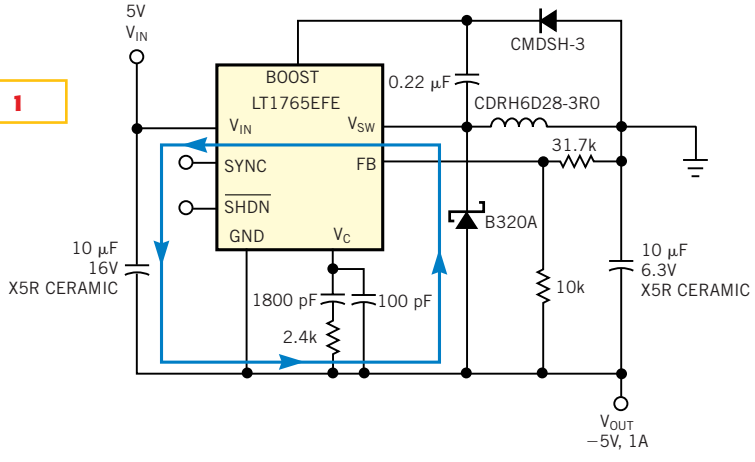
A Schottky diode keeps the I/O voltage from dropping 0.6V below the core voltage.

Lower dc/dc-converter ripple by using optimum capacitor hookup

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Low-ripple-voltage positive-to-negative dc/dc converters find use in many of today's high- frequency and noise-sensitive disk drives, battery-powered devices, portable computers, and automotive applications. Like a positive buck converter, a positive-to-negative converter can have low output-ripple voltage if you place the bulk input capacitor between V_{IN} and V_{OUT} rather than between V_{IN} and ground. A common misconception is that positive-to-negative converters in the first configuration have noisy outputs. This configuration actually solves noise problems rather than introducing them. In either configuration, the V_{IN} and ground pins of the IC connect to V_{IN} and V_{OUT}, respectively (**figures 1** and **2**). Therefore,

Figure 1



This +5-to-−5V converter with the bulk input capacitor between V_{IN} and V_{OUT} has low output ripple. The high-di/dt path, indicated here with blue lines, does not include the output capacitor.

placing the input capacitor between V_{IN} and V_{OUT} is equivalent to placing it between the IC's V_{IN} and ground pins (**Figure 1**). The other, commonly accepted method of placing the bulk input capacitor between V_{IN} and ground (**Figure 2**) significantly increases the output-voltage ripple (**figures 3** and **4**). To make matters worse, this configuration requires an additional high-frequency bypass capacitor between the V_{IN} and ground pins of the IC.

In simple positive-to-negative converters, such as those in **figures 1** and **2**, the output-voltage ripple is

$$\Delta V_{OUT(P-P)} = ESR_{COUT} \times \Delta I_{COUT(P-P)}.$$

Low-ESR output capacitors, such as ceramics, help to minimize the output-voltage ripple in dc/dc converters. For a given output-capacitor ESR, you can further reduce the output-voltage ripple by minimizing the current ripple that the output capacitor is forced to absorb. In **Figure 2**, the output capacitor is part of the high-di/dt switching-current path, making the output voltage ripple proportionately larger. With the bulk input capacitor placed as shown in **Figure 1**, the peak-to-peak ripple current in the output capacitor is equal to the peak-to-peak ripple current in the inductor: $\Delta I_{COUT(P-P)} = \Delta I_{L(P-P)} = (V_{IN} \times$ duty cycle$)/(f_{SW} \times L)$, where $\Delta I_{COUT(P-P)}$ = output ripple current, $\Delta I_{L(P-P)}$ = inductor ripple current, and f_{SW} = switching frequency.

When the bulk input capacitor is placed as shown in **Figure 2**, the peak-to-peak ripple current in the output capacitor is much higher than the inductor's ripple current alone; it is almost equal to the inductor's ripple current plus the input capacitor's ripple current: $\Delta I_{CIN(P-P)} = I_{L(P)} = I_{OUT} + I_{IN} + \Delta I_{L(P-P)}/2$, and $\Delta I_{COUT\ (P-P)} \sim \Delta I_{L(P-P)} + \Delta I_{CIN(P-P)}$. With much lower output-capacitor ripple current, the output capacitor in the circuit in **Figure 1** can be much smaller than that of the circuit in **Figure 2**. Also, it needs to handle much less rms ripple current (approximately equal to peak-to-peak ripple current divided by the square root of 12). Another advantage of removing the output capacitor from the high-di/dt switching loop (by judicious placement of the input capacitor) is a greatly simplified layout. You must place the high-di/dt components in **Figure 1** in the smallest loop possible to minimize trace inductance and the resulting voltage (noise) spikes. With one fewer component to worry about in the layout, you can more easily create a noise-free circuit using the layout in **Figure 1** than it is using the one in **Figure 2**.

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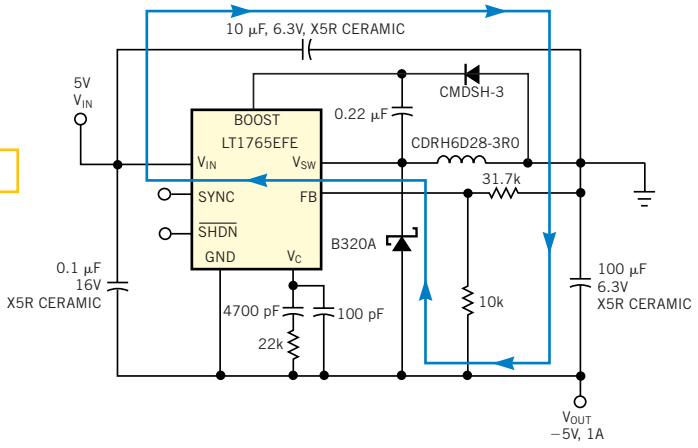


Figure 2 This +5-to–5V converter with the bulk capacitor between V_{IN} and ground has much higher output ripple than the circuit in Figure 1. The high-di/dt path, indicated here with blue lines, includes the output capacitor, thus increasing output ripple.

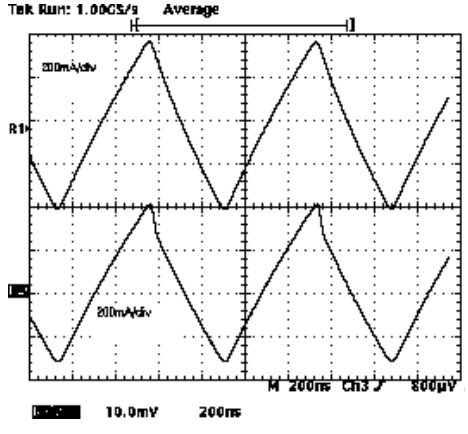


Figure 3 In the circuit in Figure 1, the output capacitor's peak-to-peak current ripple is equal to the inductor's peak-to-peak ripple with 1A output.

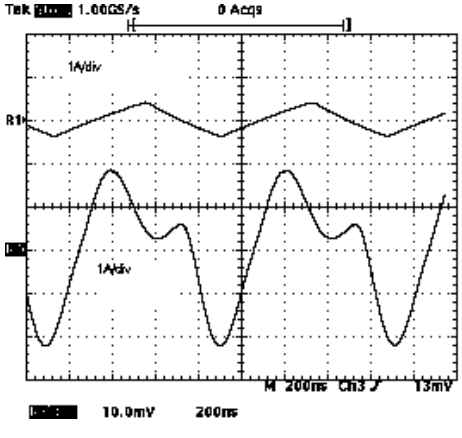


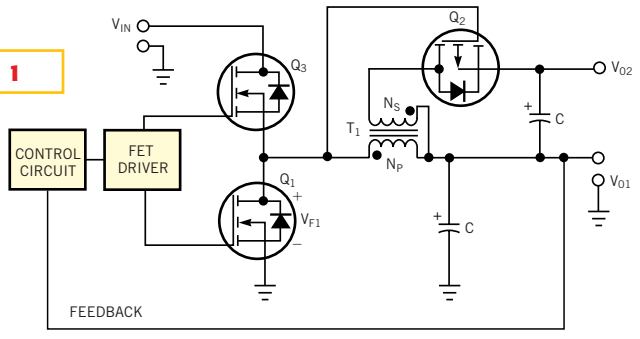
Figure 4 In the circuit in Figure 2, the output capacitor's peak-to-peak current ripple is five times as high as the inductor's peak-to-peak ripple and, therefore, five times as high as the current ripple shown in Figure 3 with 1A output.

Add an auxiliary voltage to a buck regulator

John Betten, Texas Instruments, Dallas, TX

You often need more than one regulated output voltage in a system. A frequently used and reasonably simple way to create this auxiliary output voltage is to add a second winding to the output inductor, creating a coupled inductor or a transformer, followed by a diode to rectify (peak-detect) this output voltage. The biggest drawback of this approach is that the diode's voltage drop varies with temperature and load current and can have a 2-to-1 variation, resulting in poor output-voltage regulation. This problem becomes more critical as output voltages decrease and may require the addition of a linear regulator. The circuit shown in **Figure 1** is an alternative approach that replaces this diode with Q_2, a p-channel FET. The circuit works as follows:

Figure 1



This synchronous buck converter has an auxiliary-output winding.

During the conduction time of FET Q_1, the voltage across the primary winding of transformer T_1 clamps to the voltage, $V_{OUT}+V_{F1}$, where V_{F1} is the voltage drop across FET Q_1. Through transformer action, the voltage on the secondary winding of inductor L_1 is equal to the turns ratio between the windings times the voltage across the primary winding. The output capacitor on the auxiliary output, V_{02}, then charges to the peak of the secondary-winding voltage. FET Q_2 turns off when Q_3 turns back on to prevent the output capacitor from discharging. The secondary voltage floats; you can add it to the main output voltage by tying one end of the secondary winding to the main output. You can also tie it to ground for an output voltage lower than V_{01}, if desired. The equation that defines the auxiliary-output voltage for the circuit in **Figure 1** is:

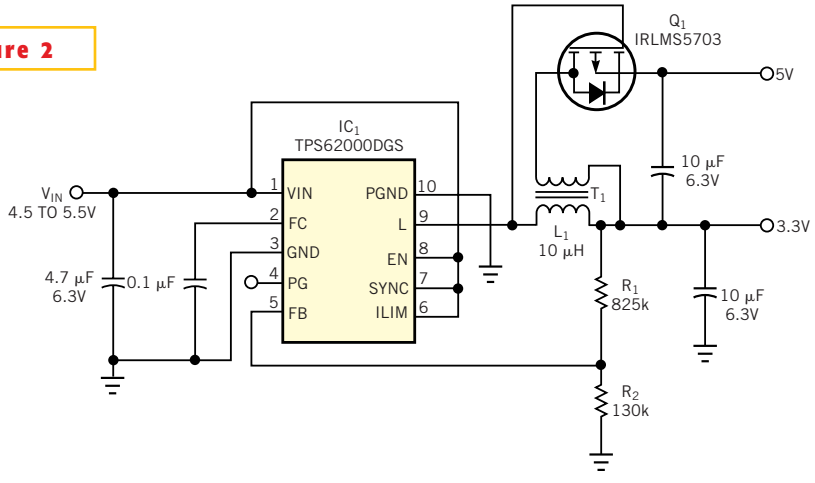
$$V_{02}=V_{01}\left(1+\frac{N_S}{N_P}\right)+\left(V_{F1}\times\frac{N_S}{N_P}-V_{F2}\right).$$

The second half of this equation represents a voltage-error term between FETs Q_1 and Q_2. To cancel out the error attributable to the FET voltage drops, you need to make the voltage drop of FET Q_2 equal to $V_{F2}=V_{F1}\times(N_S/N_P)$, where N_S/N_P is the transformer's turns ratio. Because these FET voltages are a function of the output currents and the on-resistance of the FETs, you can select the on-resistance of FET Q_2 by using the following equation:

$$R_{Q2}=R_{Q1}\times\frac{N_S}{N_P}\times\left[(1-d)\left(1+\frac{I_{01}}{I_{02}}\right)-d\times\frac{N_S}{N_P}\right],\ \text{where}\ d=\frac{V_{01}}{V_{IN}}.$$

In **Figure 2**, the main output voltage is 3.3V, yielding an inductor primary voltage when Q_1 is conducting equal to only 3.44V, because of the low voltage drop across FET Q_1. Thus, if you wanted a 5V output, the secondary winding would need to develop an additional 1.7V, necessitating a 2-to-1 step-down turns ratio. The desired on-resistance of the FET internal to IC_1 from the above equation should be 0.16Ω to cancel the voltage drop across Q_1 at maximum loads and while operating from a 5V input voltage. This example uses a 0.20Ω FET with a voltage drop equal to only 88 mV. This choice allows for good voltage matching between FETs Q_1 and the FET internal to IC_1, resulting in excellent error cancellation, less power loss, and better overall output-voltage regulation than diode rectification provide. An added benefit of this approach is that you can use it with controllers that have integrated switching FETs, because you don't need access to Q_1 and Q_3 gate drives. Measured results, although varying both outputs' loads over their full operational range, showed less than a ±3% variation in the

Figure 2



This circuit is similar to the one in Figure 1, but uses an integrated buck-converter IC.

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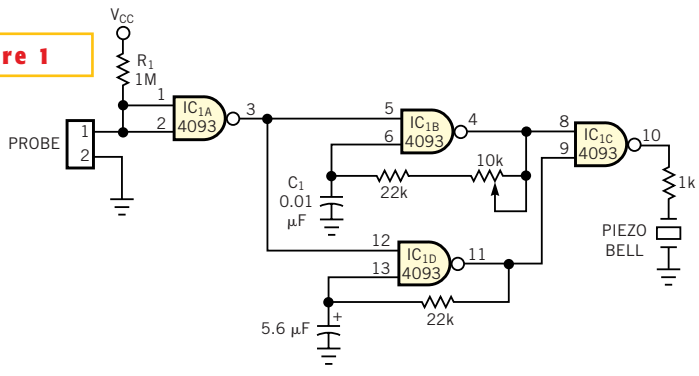
Circuit checks "swamp-cooler" water level

Daniel Krones, Precision Design Services, Sky Forest, CA

A "swamp cooler" is an easy way to obtain effective air conditioning, especially in hot and dry climates, if a water source is readily available. Although most units are very reliable, the storage-reservoir control usually uses a single level-detector component. Failure of this component can lead to serious water damage. The circuit of **Figure 1** provides a simple, inexpensive backup alarm signal if the water level exceeds the preset height. The circuit uses a single Schmitt-trigger IC to detect the water level, using the conductivity of the water to drop the input level of IC_{1A}. A 1- to 10-MΩ resistor is suitable for R_1. You might have to experiment to determine a suitable value, depending on the conductivity of the water supply.

Figure 1



Detect water level in a swamp-cooler reservoir with this simple circuit.

The highest practical vale of R_1 provides the widest range. The NAND gates IC_{1B} and IC_{1D} implement gated oscillators to create a pulsed tone to drive the piezoelectric-bell audible alarm. Current consumption in the off state is lower than 10 µA, thus allowing the use of a simple battery to drive the circuit. A button-cell lithium watch battery is sufficient. The small physical size and wiring simplicity of the circuit allow you to simply glue the unit to the side of the cooler. Use a short piece of twin-lead, 300Ω transmission line for the electrodes.

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design ideas

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DPP adds versatility to VFC

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

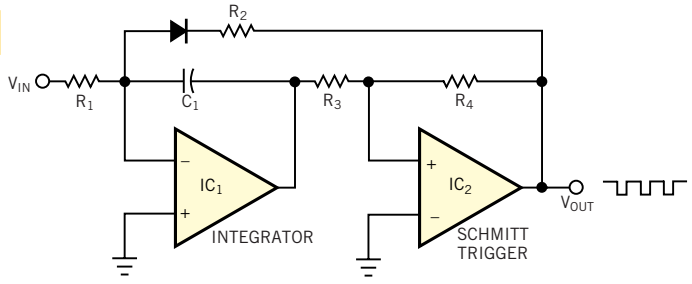
THE BASIC VFC (voltage-to-frequency converter) in **Figure 1** comprises an integrator (IC_1) and a Schmitt-trigger circuit (IC_2). The integrator converts the dc input voltage, V_{IN}, to a linear voltage ramp, and the Schmitt trigger sets the limits of the integrator's output voltage. Feedback around both circuits provides the condition for oscillation. The DPP (digitally programmable potentiometer) in **Figure 2** adds programmable limits to the Schmitt trigger and adds two powerful features to the VFC. First, the scale or conversion factor is programmable, and, second, for a fixed dc-input voltage, the converter is a programmable oscillator. The frequency, f_0, of the single-supply converter in **Figure 2** is:

$$f_o = f_{BASE}\frac{(1-p)}{p}\frac{(V_{IN}-2.5V)}{5V};$$

$$0<p<0.5, \text{ and } 2.5V<V_{IN}<5V,$$

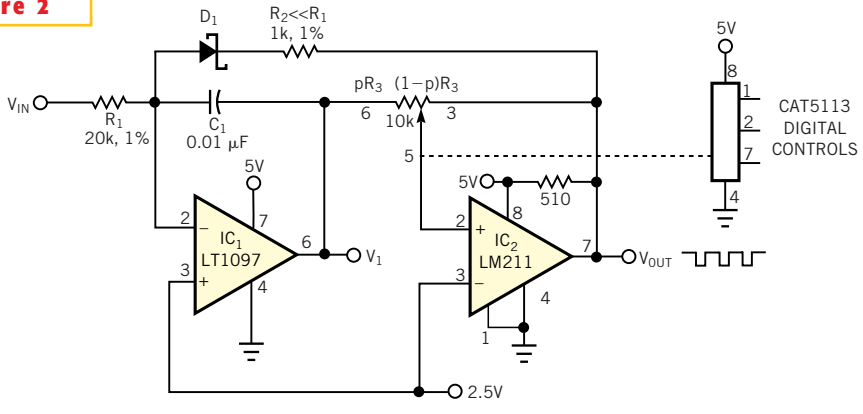
where $f_{BASE}=1/2\pi R_1C_1$, and p is the relative position of the wiper from one end (0) of the DPP to the other end (1). For the100-tap Catalyst (www.catsemi.com)

Figure 1



This schematic depicts a basic voltage-to-frequency converter.

Figure 2



Using a digitally programmable potentiometer, you can vary the scale factor of this voltage-to-frequency converter.

5113 potentiometer, the range of the scale-factor term (1-p)/p is 1 to 99 with a resolution and accuracy of approximately 1%. For the values shown in **Figure 2**, the practical range of frequencies is 500 Hz to 25 kHz. Higher bandwidth, rail-to-rail CMOS versions of IC_1 and IC_2, and a greater R_1/R_2 ratio can extend the accuracy and range of the circuit. The automated, accurate setting of the scale factor saves manufacturing test time and eliminates the need for expensive, accurate resistors and capacitors. The scale factor relates to the ratiometric temperature coefficient of the DPP and hence is minimally temperature-dependent. You can use the circuit as a programmable oscillator when V_{IN} is fixed and the potentiometer's wiper setting changes the limits of the Schmitt trigger.

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Power circuit terminates DDR DRAMs

Ron Young, Maxim Integrated Products, Sunnyvale, CA

DDR (DOUBLE-DATA-RATE) SDRAMs find use in high-speed memory systems in workstations and servers. The memory ICs operate with 1.8 or 2.5V supply voltages and require a reference voltage equal to half the supply voltage ($V_{REF}=V_{DD}/2$). In addition, the logic outputs terminate with a resistor to the termination voltage, V_{TT}, which equals and tracks V_{REF}. V_{TT} must source or sink current while maintaining $V_{TT}=V_{REF}\pm 0.04V$. The circuit of **Figure 1** provides the termination voltage for both 1.8 and 2.5V memory systems and delivers output current as high as 6A. IC_1 includes a step-down controller and two linear-regulator controllers and operates with input voltages of 4.5 to 28V.

IC_1's fixed-frequency, 200-kHz PWM controller maintains the output voltage by sourcing and sinking current. Maximum sink current equals the maximum source current, though the sink current has no current limiting. When sinking current, the device returns some current to the input supply. To implement the tracking function, one of IC_1's extra linear-regulator controllers is configured as an inverting amplifier. This amplifier compares $V_{DD}/2$ (created by R_1 and R_2) with V_{REF} from IC_1 and generates an error signal that connects via R_3 to IC_1's FB pin, thereby forcing V_{OUT} to track $V_{DD}/2$. A 10-mA load, R_4, is necessary to bias the inverting amplifier for accurate tracking. V_{OUT} can track $V_{DD}/2$ for V_{DD} in the range 1 to 4V.

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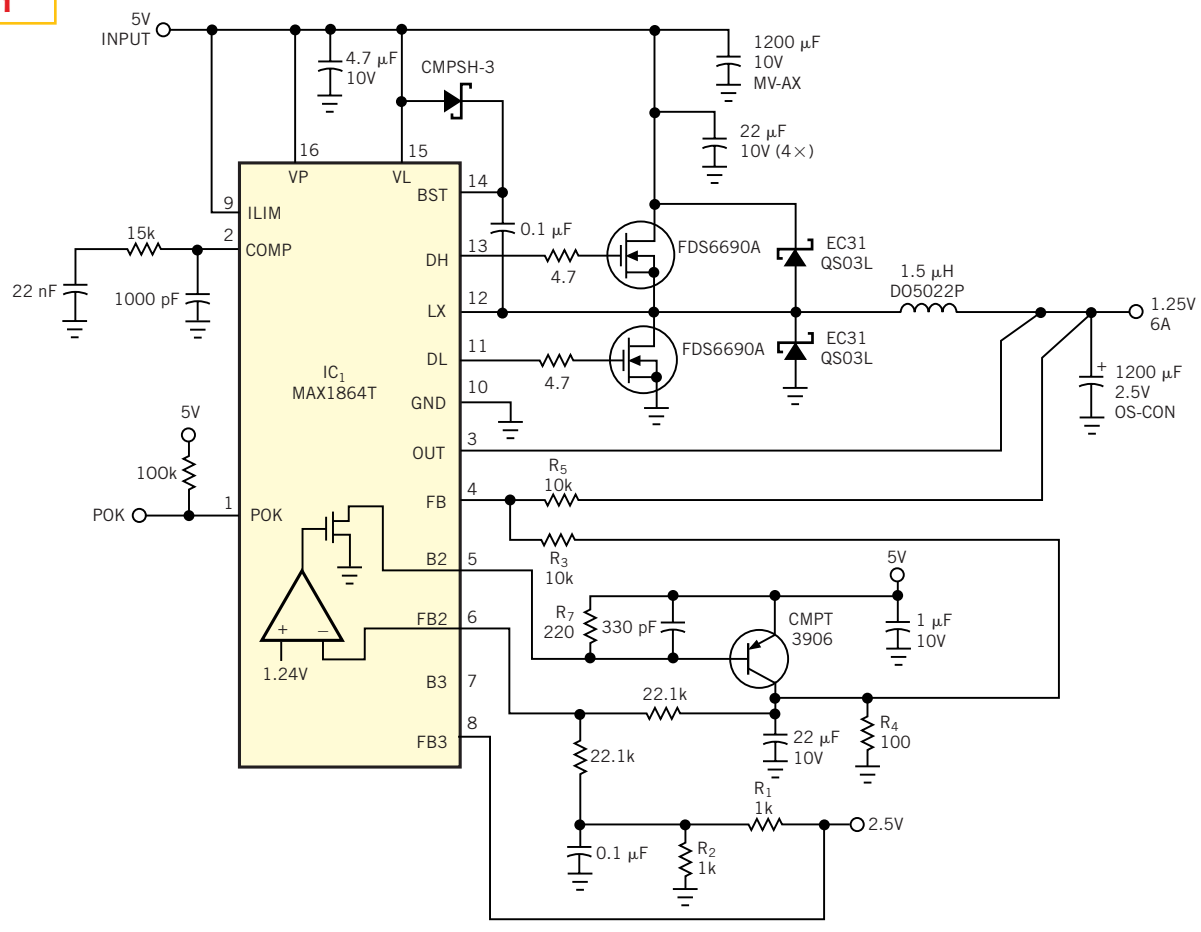
Figure 1

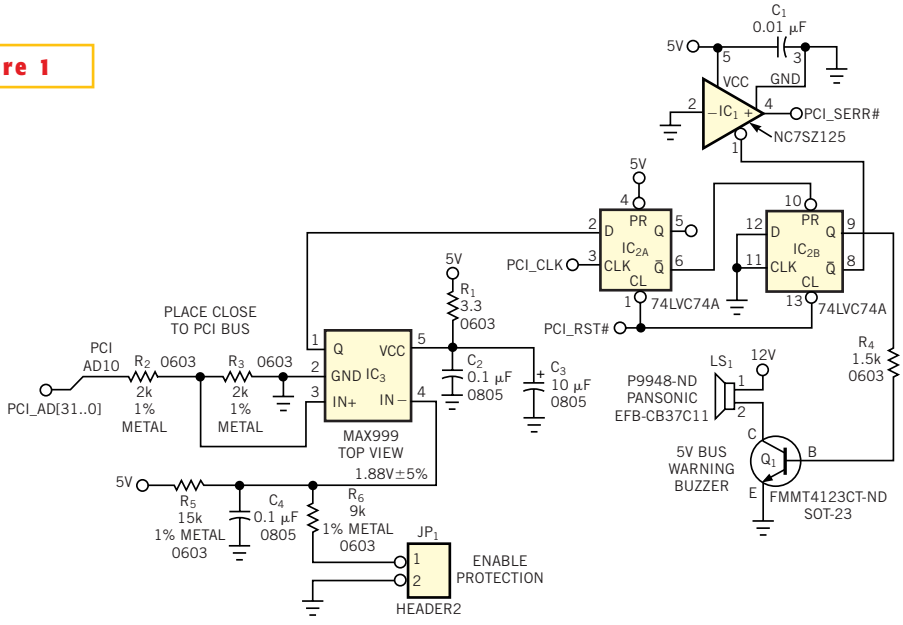


This circuit generates the termination voltage for DDR synchronous DRAMs.

Circuit protects bus from 5V swings

Said Jackson, Equator Technologies Inc, Campbell, CA

Figure 1



This circuit provides both an audible alarm and an error flag when an overvoltage condition exists.

THE CIRCUIT IN **Figure 1** automatically detects voltage and protects a bus, such as a 3.3V-limited PCI bus, from 5V signal-level swings. You can also use the circuit to determine bus-voltage swings within one bus-cycle for setting appropriate termination voltages of protection diodes or termination resistors. Today's deep-submicron VLSI-manufacturing techniques sometimes require circuits to limit I/O voltages to 3.3V signal swings. Connecting such circuits to a bus with 5V level-swing cards could damage the circuitry. The circuit in **Figure 1** can accurately and—within one bus cycle—detect a level swing larger than 3.3V on any bus and, upon a fault situation, generate a reset signal and an alarm output to notify the user and the system of this fault. Some of the novel circuit features include a highly accurate synchronous-detection capability to avoid false alarms arising from large signal overshoots, high impedance and low capacitive loading of the bus, automatic system shutdown during fault conditions, and a single-cycle response time.

This circuit successfully operates in products using the high-performance 3.3V MAP-CA processor family from Equator Technologies (www.equator.com), but you can use it in other high-speed 3.3V or even lower voltage systems. Equator's latest generation chips are 5V-tolerant, but you can adjust the circuit to protect other 1.8 and 2.5V chips. The circuit uses IC_3, an ultrahigh-speed Maxim (www.maxim-ic.com) MAX999 comparator with 4.5-nsec propagation delay, T_{PD}, to constantly compare a signal line, PCI_AD10 in case of a PCI bus, to a reference level of 3.8V. This reference voltage is an optimal compromise between 5V signals clamped by 3.3V protection diodes and the normal-operation 3.3V signals. Once the voltage exceeds this reference level for an entire bus clock period, the system turns on an alarm buzzer connected to Q_1.

The circuit generates a signal that can reset the system, or it can generate a system-error signal. Because the alarm-register memory, IC_{2B}, serves as an asynchronous register, you can switch the alarm off only by removing power from the system or by asserting the reset signal. To avoid false triggering by signal overshoot and undershoot, a flip-flop-based register, IC_{2A}, samples the comparator output only during the rising edges of the bus clock. This method allows for a generous 33-nsec period at 33 MHz for the bus signal to settle down before being sampled. Lowpass filtering by sensor resistors R_2, R_3 and the 3- to 5-pF parasitic capacitance on Pin 3 of IC_3 limit the maximum clock speed of this circuit. The traces connecting to Pin 3 of IC_3, R_2, and R_3 thus must be as short as possible and may limit the bus speed to approximately 40 to 50 MHz. Symmetrically lowering the resistance of R_2 and R_3 increases the maximum bus speed to a theoretical 7-nsec cycle time (greater than 140 MHz) at the expense of a higher signal-loading current on the bus.

In the case of monitoring a PCI bus, Pin 3 of comparator IC_3 monitors signal PCI_AD10. Every PCI device asserts this signal at least once during PCI enumeration, but you can monitor other signals if necessary. This method guarantees recognition of a 5V PCI device shortly after the BIOS starts enumerating the PCI bus during system boot. IC_{2A} then latches the comparator's, IC_3, Q-output Pin 1 during the rising edge of the PCI clock. This action asserts flip-flop IC_{2B}, which in turn enables buzzer LS_1 and generates an open-collector, low-active, system-error signal through IC_1. You could use this error signal to automatically remedy the fault condition by disabling the offending circuit on the bus. The sense and reference resistors R_2, R_3, R_5, and R_6 should be metal-film 1% types. The 5V reference voltage connected to R_5 determines the accuracy of the trip voltage, and today's power regulators have sufficient accuracy so that you can use a 5V system-power line as the reference voltage, obviating the need for a special 5V-reference generator. Removing jumper JP_1 disables the circuit.

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Use a 555 timer as a switch-mode power supply

Aaron Lager, Masterwork Electronics, Rohnert Park, CA

Most switch-mode power supplies rely on a PWM (pulse-width-modulated) output that is controlled via voltage feedback. A 555-timer IC can inexpensively perform PWM. The circuit in **Figure 1** shows how to turn a 555 PWM circuit into an switch-mode power supply with only one simple equation. The design uses two 555s. IC_1, in astable mode, triggers IC_2 in PWM mode. IC_1 is set to oscillate at approximately 60 kHz at a high duty cycle. The output is low for only approximately 2.5 µsec to trigger the PWM circuit and then goes high for the rest of the period. The PWM circuit has a maximum pulse width of approximately 85 µsec, and it becomes shorter, depending on the control voltage from the feedback circuit. You can reduce the chip count by using a 556 or another continuous-trigger source. The input must be ($1.5V_{OUT}$+Margin), so for 5V output you need 9V minimum input. If you use CMOS chips and small timing capacitors C_1 and C_2, you can keep the operating current low. Thus, you can use a simple zener-diode regulator for the 555 and increase the input voltage to more than 30V. The input-voltage limit is a function of how much power the zener supply can handle while delivering 5 to 10 mA to the 555s.

Q_1 has low $R_{DS(ON)}$ and low V_{GS} and can handle more than 40V. D_1 clamps any voltage spikes, such as those that occur when a large current flow ceases, causing a large magnetic field to be left in the inductor. You should select D_1 according to the output voltage you need. For 5V output, use a 5.6V zener diode, for example. IC_3, R_1, R_2, and V_1 form the feedback circuit to set the output voltage. The output-voltage equation is $V_{OUT}=V_1(R_1/R_2+1)$. The TL431 is a popular part for setting a voltage reference and can easily create the 1.25V shown for V_1. You can supply 5V at 1.5A with an input of 9 to 40V. At voltages higher than 12V, you can add a 10V zener-diode supply for the chips. The zener supply only slightly reduces the efficiency. With 12V input, 5V, 1.5A output efficiency is approximately 70%, and it drops to 65% with a 40V input and a zener circuit. The zener diode's influence is more noticeable at lower current levels; at a 50-mA load the efficiency drops to approximately 50%.

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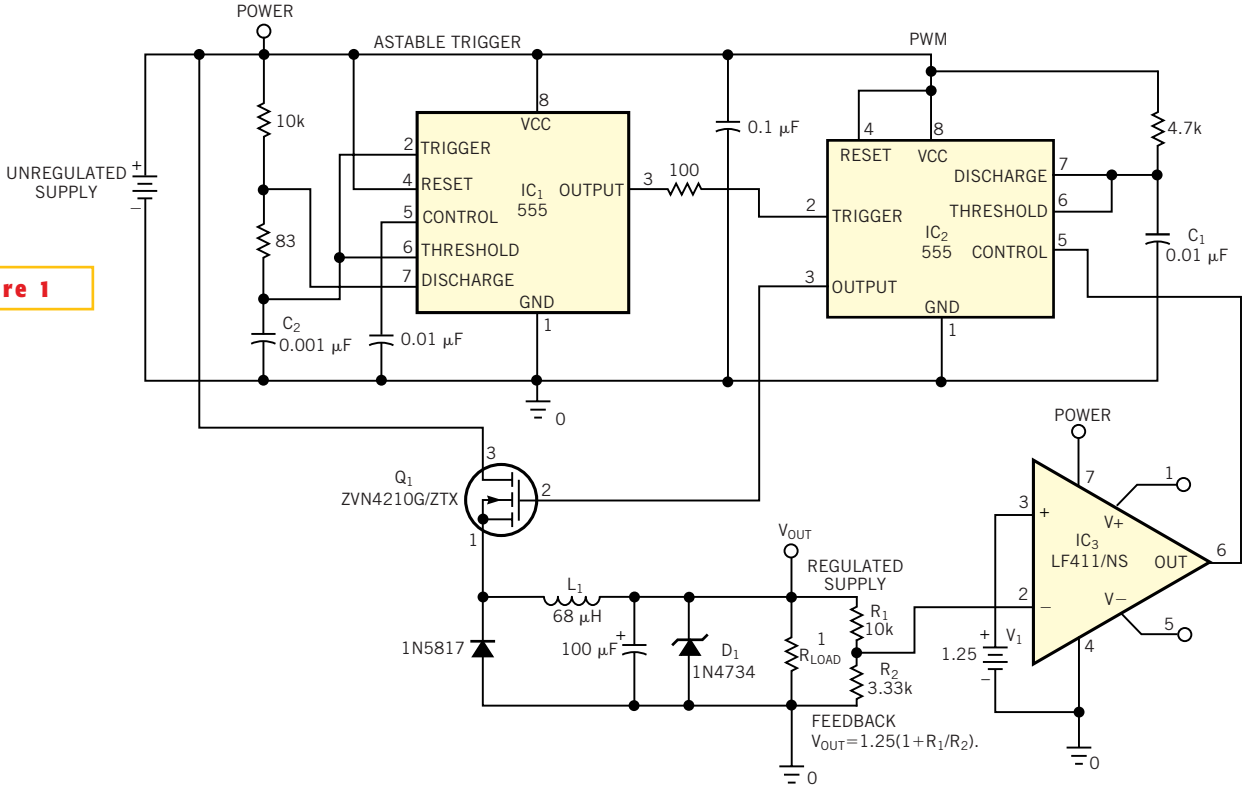
Figure 1



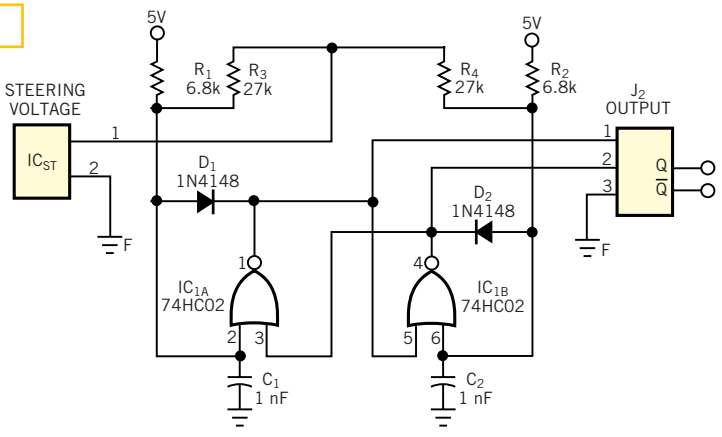
Here's one more use for the ubiquitous 555 timer: a switch-mode power supply.

VCO uses programmable logic

Susanne Nell, Breitenfurt, Austria

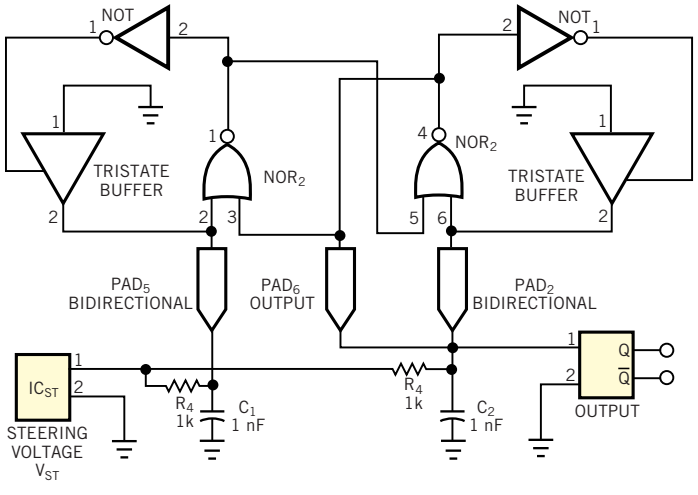
A VCO (voltage-controlled oscillator) is an analog circuit, so you cannot find it in the libraries for the design of digital programmable chips. When you need such a circuit for synchronization or clock multiplication, you need to find a circuit that works with the standard digital functions, such as AND and NAND. Several possibilities exist for building variable-frequency oscillators. For example, you can change the frequency using a varactor diode. Unfortunately, these diodes have a small change of frequency per volt. So, the standard Pierce oscillator with one inverter and capacitors is not useful for these applications. Another idea is to use a Schmitt-trigger inverter and to vary the charging resistor. This method can work, but the hysteresis of the IC usually has a wide tolerance, so the selected inverter chip has a large influence on the frequency.

Figure 1



This unique VCO, implemented with discrete logic, has a wide tuning range.

Figure 2



This VCO uses an EPLD and has high gain, expressed in kilohertz per volt.

For these reasons, this design modifies a two-NOR-gate RC oscillator (**Figure 1**) to function as a VCO. For almost all pure-CMOS circuits, the switching point between high and low states is approximately $V_{CC}/2$. This point does not depend on the device. Using this circuit, you can obtain a wide frequency-tuning range. The output is a square wave with a 50% duty cycle. At power-on, both capacitors C_1 and C_2 are uncharged, and IC_{1A} has a low output. Thus, the output of IC_{1B} is high, and C_2 charges with the time constant R_2C_2. The additional charging current from IC_{ST} and R_4 also influences this charging time. When the voltage on C_2 reaches $V_{CC}/2$, IC_{1B} switches to a low state. Now, the output of IC_{1A} switches high, and C_1 charges with time constant R_1C_1, influenced by IC_{ST} and R_3. The low signal at the output of IC_{1B} forward-biases D_2 and quickly discharges C_2.

This circuit produces a 50% duty cycle if $C_1=C_2$, $R_1=R_2$, and $R_3=R_4$. The values of R_4 and R_3 and the steering voltage, V_{ST}, determine the VCO's gain in kilohertz per volt. The circuit in **Figure 2** yields the highest possible value for the VCO's gain. The circuit uses an Altera (www.altera.com) EPLD (erasable programmable-logic device), the EPM3032. Tristate buffers replace the diodes in **Figure 1**, and the charging resistors connect directly to the steering voltage. This configuration produces the highest possible VCO gain: approximately 700 kHz/V for the component values shown. You can switch off the VCO by using a steering voltage lower then $V_{CC}/2$. You can implement this circuit using almost all programmable-logic devices with CMOS inputs. You can also use steering voltages much higher then the supply voltage of the programmable chip, because the voltage on the input of the chip never goes higher then $V_{CC}/2$. This fact makes the circuit suitable as a voltage-to-frequency converter with a high input-voltage range.

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Controlling slew times tames EMI in offline supplies

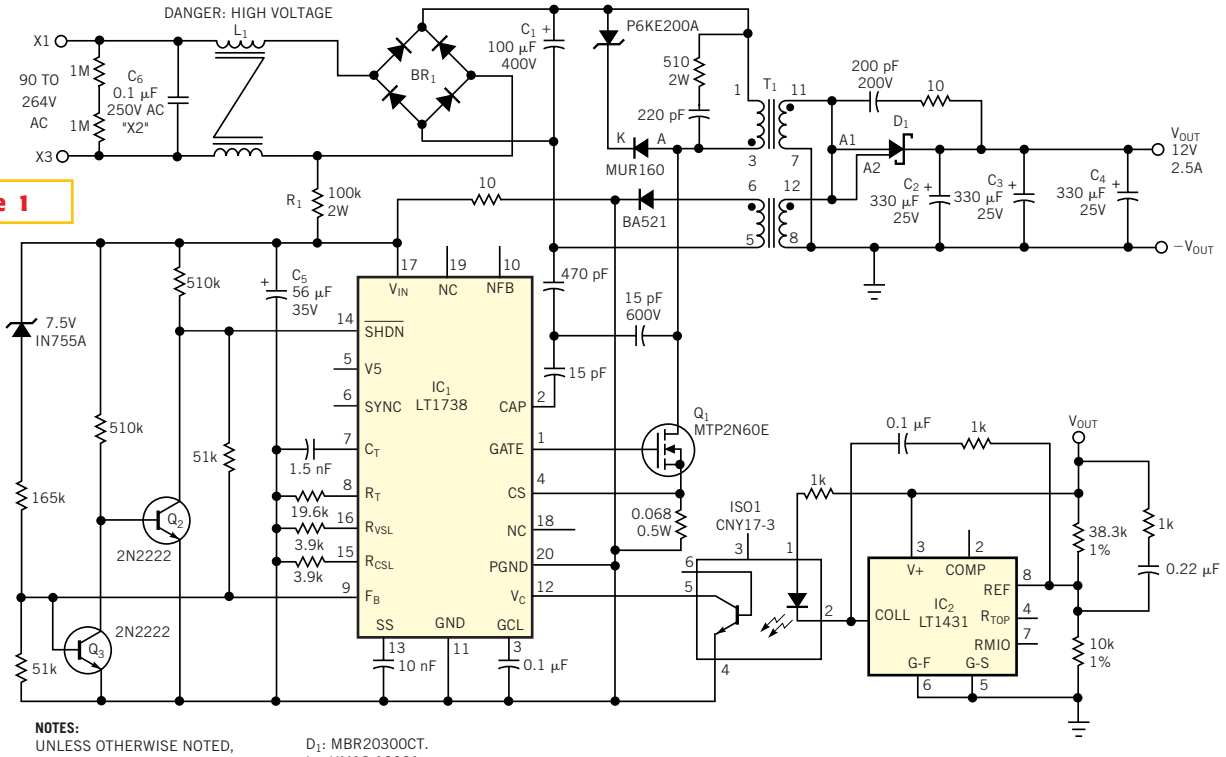
David Canny, Linear Technology Corp, Milpitas, CA

EMI from offline switching power supplies typically causes all sorts of problems for power-supply designers. You may need a large EMI filter to meet FCC emission requirements. Switchers for high efficiency produce high-frequency switching noise that can propagate through the rest of the system and cause problems. Board layout is critical, requiring considerable experimentation, even for experienced designers. The low-noise circuit in **Figure 1** significantly reduces the complexity of these issues by continuous, closed-loop control of the voltage and current slew rates. High-frequency noise suppression is particularly important for medical devices because they don't require the ac-line-to-earth ground capacitors ("Y" capacitors) that typically suppress this noise. The absence of these capacitors allows medical devices to easily comply with the more stringent low-leakage-current healthcare specifications of UL544, UL2601, and CSA22.2.

Figure 1 shows a 30W (12V output at 2.5A) offline power supply. IC_1, an LT1738 low-noise switching regulator in a flyback topology, drives Q_1 and continuously controls the current slew using the resistor at the R_{CSL} pin. The IC controls the voltage slew using the resistor at the R_{VSL} pin and the capacitance at the CAP pin. IC_2, an LT1431 programmable reference, and the optocoupler close the isolated loop back to the LT1738. The circuit achieves current limit by sensing the current through a 68-mΩ resistor at the CS pin. Q_2, Q_3 and their associated circuitry provide undervoltage lockout with hysteresis. During start-up, the $\overline{SHDN}$ pin stays low until C_5 charges to 12V via R_1. The LT1738 then turns on and subsequently obtains most of its operating power from T_1's auxiliary winding. The feedback goes directly to the LT1738's V_C pin rather than to the F_B pin because the optocoupler provides the feedback gain that the LT1738's internal feedback amplifier typically provides. C_6 and L_1 attenuate the low-frequency harmonics of the LT1738 switching frequency.

You can see the benefits of the circuit by measuring its ac-line-conducted EMI and then comparing these measured results with those for basically the same circuit with the LT1738 replaced with a

Figure 1



NOTES:
UNLESS OTHERWISE NOTED,
ALL RESISTORS: 1206,5%.
BR_1: GENERAL INSTRUMENTS WO6G.
C_2, C_3, AND C_4: SANYO MV-GX.
D_1: MBR20300CT.
L_1: HM18-10001.
T_1: PREMIER MAGNETICS POL-15033.

A 30W offline power supply passes FCC Class B emission requirements without line-to-earth-ground capacitors.

generic switcher. The only circuit-parameter difference is that, unlike the LT1738, the generic switcher doesn't actively control the switching current and voltage slew rates. **Figure 2** shows the frequency spectra for both circuits. You can see by the respective frequency spectra that the LT1738-based circuit generates emissions well within FCC Class B requirements, whereas the circuit with the generic part results in emissions that exceeds FCC Class B allowable emissions by a significant margin.

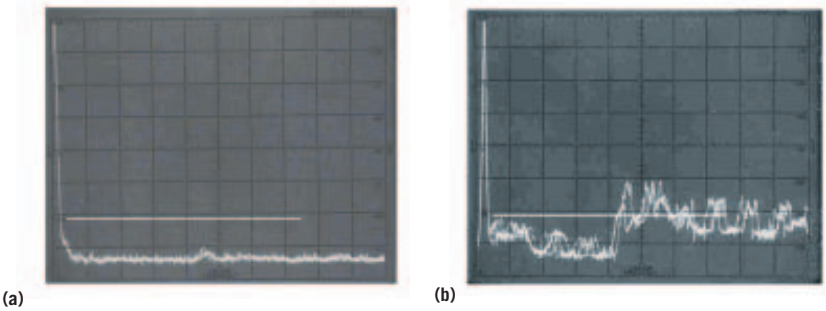


Figure 2 In these 50-MHz-wide spectral plots, areas under horizontal lines indicate acceptable FCC Class B emission requirements. The spectral plot for the LT1738-based circuit (a) shows emissions well within FCC Class B requirements, unlike the plot for the generic switcher (b).

Another benefit of the circuit in **Figure 1** is that the output voltage noise comprises the fundamental ripple with practically no high-frequency components. You can attenuate this ripple voltage if desired to less than 300 μV using a 100-μH, 100-μF LC filter on the output. The generic switcher, on the other hand, produces more output noise because the high-frequency noise passes to the output with little attenuation through the parasitic capacitance of the output filter's inductor. The circuit in **Figure 1** minimizes noise and EMI by controlling the voltage and current slew rates of the external n-channel MOSFET. This circuit is well-suited for offline power supplies in medical devices because the absence of Y capacitors results in low leakage current to earth ground in compliance with health-care specifications.

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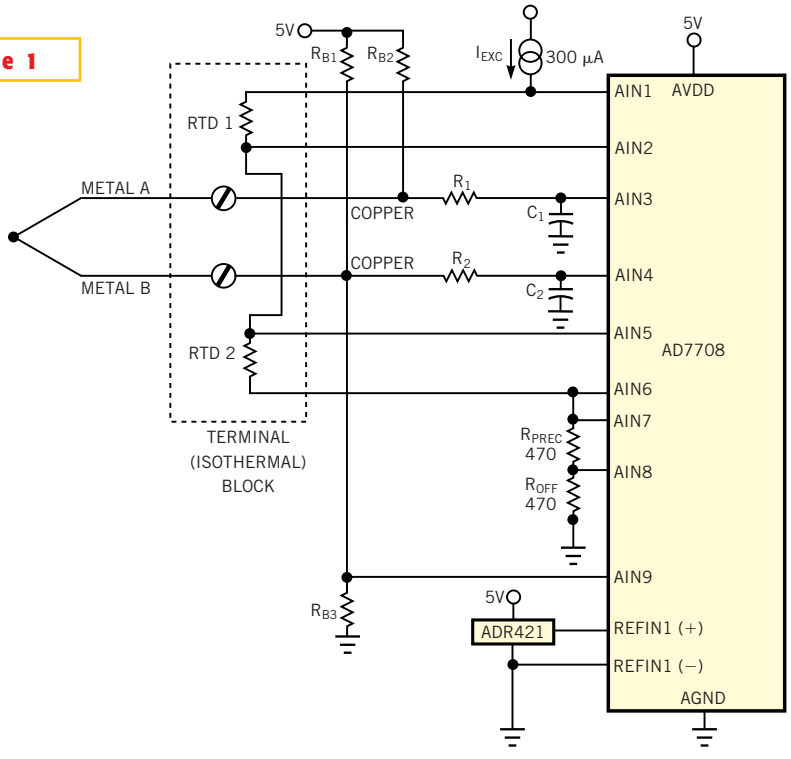
Edited by Bill Travis

Circuit provides cold-junction compensation

Mark Maddox, Analog Devices, Wilmington, MA, and
John Wynne, Analog Devices, Limerick, Ireland

THE ACCURACY OF ANY CIRCUIT or system that uses a thermocouple to determine the temperature of a process is limited by the accuracy of the method used to perform cold-junction compensation. In a thermocouple measurement, two wires of dissimilar metal join together at the "hot," or measurement, junction. The isothermal termination of the thermocouple wires provides a second "cold," or reference, junction. The potential across the thermocouple is proportional to the temperature difference between the two junctions. Thus, to determine the absolute temperature of the hot junction, you must also know the absolute temperature of the cold junction. Tables of thermocouple voltage versus temperature use the assumption that the cold junction is maintained at 0°C. A somewhat impractical way to use these tables is to place the cold junction into an ice bath. A more practical way is to measure the temperature of the cold junction and then add an equivalent voltage to the one developed by the hot junction. You then find the temperature of the hot junction in the thermocouple tables.

Figure 1



This circuit provides accurate cold-junction compensation in temperature-measurement systems.

A key issue to address is how to thermally bond the RTDs (resistance-temperature detectors) to the terminal block, which is the cold junction. If the temperature along the terminal block is constant, you could use a single sensor, thermally bonded to the block. If a linear temperature gradient exists along the terminal block, you could use a sensor at both ends of the block. This method allows for interpolation of the temperature at various points along the block. If the temperature gradient is nonlinear, you can add an electrically isolated copper strip along the length of the block to minimize the nonlinearity. In the extreme case, you could use a temperature sensor per thermocouple pair with each sensor, thermally bonded to its respective junction.

The design in **Figure 1** uses a multichannel, high-resolution ADC to measure the thermocouple voltage and the resistance of two RTDs at the cold junction. Using the data from the ADC, a microprocessor determines the temperature of

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the cold junction, the amount of cold-junction compensation to apply, and, then, the temperature of the hot junction. Performing the cold-junction compensation in software allows users to use mixed thermocouple types and is both flexible and universal. The AD7708 digitizes the signals from the thermocouple and from two three-wire RTD sensors, which measure the cold-junction temperature at both ends of the terminal block. The terminal block is local, so you can ignore the wiring resistance between the ADC and the RTDs. It is easier to obtain precision resistors and voltage references than precision current sources, so the RTDs and the 470Ω precision resistor, R_{PREC}, connect in series, and all obtain excitation from the same current source, I_{EXC}. The voltage generated across R_{PREC} determines the exact value of the excitation current. Hence, the current source need not be particularly stable over temperature. R_{OFF} offsets input pair AIN7/-AIN8 by more than 100 mV from ground. R_{OFF} is also a 470Ω resistor but need not be a precision resistor. The ADR421's 2.5V precision voltage reference directly drives the REFIN1(+)/REFIN1(−) inputs.

With I_{EXC} set to 300 μA and the internal programmable-gain amplifier set to the 40-mV full-scale range, the ADC produces usable resolution of 2.4 μV. With 100Ω RTDs, it accurately resolves a 0.02°C temperature differential between the two ends of the terminal block and has an absolute accuracy of ±0.01°C for either measurement. The differential analog input pair, AIN1/AIN2, of the AD7708 reads an input voltage equal to I_{EXC}(RTD 1), where RTD 1 represents the resistance of the first RTD element. A second differential input pair, AIN5/AIN6, reads an input voltage equal to I_{EXC}(RTD 2), where RTD 2 represents the resistance of the second RTD element. One source of error pertains to the RTDs themselves. The most common type is the 100Ω platinum RTD with a resistance-temperature coefficient of 0.00385Ω/Ω/°C. It is available in accuracy-tolerance classes A and B (or DIN A and DIN B), which specify both the initial accuracy at 0°C and the interchangeability over the operating range. The Class A specification is ±(0.15±0.002|t|), where t is the specified interchangeability temperature; the Class B specification is ±(0.3±0.005|t|).

It is possible to buy two Class A, 100Ω platinum RTDs from the same manufacturer and find that one is reading 0.2°C high at 25°C and the other is reading 0.2°C low at 25°C. Thus, you have an apparent 0.4°C difference before you even commission t. One way to combat this initial error is to request a matched pair of RTDs from the manufacturer. Leading RTD manufacturer Heraeus Sensor (www.4hcd.com) makes available PRTDs (platinum RTDs) that Heraeus sorts into tolerance groups with maximum Δt =±0.05°C over 0 to 100°C. A lower cost solution and one that uses off-the-shelf RTDs is to use the offset and gain registers on the AD7708 ADC to calibrate each of the RTD errors. Noise pickup may be an issue if the hot junction of the thermocouple is a long distance from the measurement electronics. The very-high-input-impedance buffer inside the AD7708 allows the addition of lowpass filters R_1-C_1 and R_2-C_2 to the AIN3/AIN4 inputs to attenuate high-frequency-noise pickup in the wiring.

A single-ended analog-input channel, AIN9, and three burnout resistors, R_{B1} through R_{B3}, provide both thermocouple open-circuit, or burnout, and short-circuit-detection functions by forcing the dc bias levels of AIN3/AIN4 away from their normal operating levels of approximately 2.5V. A thermocouple short-circuit fault condition from either Metal A or Metal B to ground pulls the voltage across R_{B3} to 0V. A thermocouple open-circuit fault condition on either Metal A or Metal B causes the voltage across R_{B3} to move to 1.66V. You can program either of these voltage levels (converted by AIN9) to raise an alarm signal.

A more difficult fault condition to detect is the condition in which the two thermocouple wires short only to each other. In this case, a new thermocouple junction forms at the location of the short circuit, and the junction behaves like a normal thermocouple. The only way to detect this fault condition is to implement a rate-of-change alarm in software. If the two wires short together at the exit of the thermo-well, the new thermocouple junction may well experience much the same temperature that the original thermocouple junction experienced. This fault condition is difficult to spot. However, if the short circuit occurs a long distance from the original thermocouple junction, then this new junction may be at a different temperature from that of the original junction and produces a rate of change that channel does not normally see. You can use this abnormal change to flag an alarm condition.

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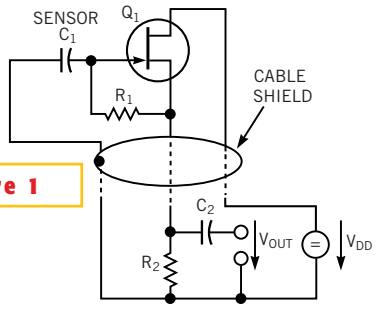
Solve low-frequency-cutoff problems in capacitive sensors

Julius Foit, Czech Technical University, Prague, Czech Republic

One of the first problems a capacitive-sensor analog designer must face is the low-frequency cutoff. Theoretically, you must fulfill just one simple requirement: a sufficiently large input resistance of the preamplifier's first stage. In practice, however, many problems lurk behind the seemingly straightforward design rules. First, the preamplifier's active device must have a defined dc operating point. Using field-effect devices renders the dc input current of the first active device (a JFET or a MOSFET) so low that you can neglect it in most cases. On the other hand, the circuit must

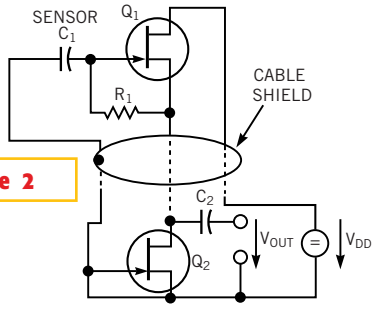
have some dc-path-creating resistor to present the required dc potential to the input electrode. Assuming that a typical miniature capacitive sensor, such as a high-quality capacitive microphone, has a small capacitance of 20 to 50 pF, for example, the resistor value to obtain a cutoff frequency as high as 50 Hz would be on the order of 10^8 to $10^9\Omega$. Resistors with such high values are difficult to find in SMD formats, are expensive, have poor accuracy and stability, and are large and noisy. Moreover, further difficulties appear when the capacitive sensor requires an external polarization voltage. Such a polarization voltage may have a value of 100V or more. This voltage must connect to the sensor via a separate circuit, and it sometimes creates problems if the need to have at least one side of the sensor grounded emerges. And, as in all similar cases, the preamplifier should be as close to the sensor as possible. It should consume minimal space, need few connecting leads, and produce as little heat as possible. The circuit in **Figure 1** represents one possible approach to meeting these challenges.

Figure 1



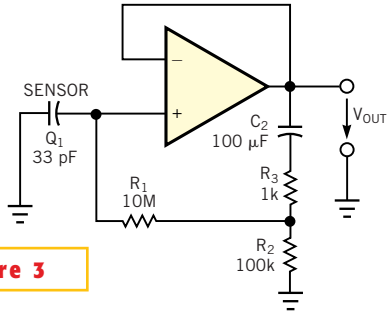
The JFET in this circuit effectively multiplies the value of R_1.

Figure 2



The second JFET, Q_2, in this circuit replaces R_2 in the circuit of Figure 1.

Figure 3



An operational amplifier provides yet another means to achieve high impedance for capacitive sensors.

The circuit uses electronic multiplication of the gate resistor, R_1, value via positive feedback through the source-follower action of JFET Q_1. The multiplication factor is $\alpha = g_{fs}R_2$. (Note: g_{fs} is the real part of the differential forward transfer admittance in common-source connection.) Assuming a typical value of $C_1 = 33$ pF, reasonable values of $R_1 = 10$ MΩ and $R_2 = 10$ kΩ and assuming a conservative value of $g_{fs} = 5$ mA/V (typical in the JFET type BF245B at $V_{GS} = 0$V and $V_{DS} = 15$V), you obtain the following low-frequency cutoff:

$$f_L = \frac{1}{2\pi C_1 R_1 g_{fs} R_2} = 9.6 \text{ Hz}.$$

With this method, notwithstanding the extremely small sensor capacitance and conservative values of all other components, you obtain a respectable cutoff frequency. At the same time, to get the required high polarizing voltage to the sensor while keeping one side connected directly to ground, you can use a supply voltage, $V_{DD} = V_{DS} + V_{POLARIZING} = 115$V, where $V_{POLARIZING} = I_D R_2$, and I_D is the JFET's drain current at the selected V_{DS} and $V_{GS} = 0$. Thus, you provide a polarizing voltage of 100V to the sensor. Other advantages of the circuit are obvious at the first glance: Only two elements of the circuit, R_1 and Q_1, must be connected directly at the sensor's location. Both these components are readily available, and they are physically small (usually considerably smaller than the sensor itself), so they pose no space problems. The heat the JFET produces—150 mW—is low enough to be negligible in most applications. The circuit needs only three wires for connection, and one of them can also serve as cable shielding. The connecting cable can be quite long; its maximum length is limited primarily by its capacitance, which determines the upper cutoff frequency. In most applications, the upper cutoff frequency of the sensor itself is low enough to permit a rather long cable. The only minor disadvantage of the circuit lies in its total power consumption, mostly dissipated in R_2 (1W in this case).

In cases not requiring a high polarizing voltage, the value of R_2 might become too small to obtain a sufficiently large multiplication factor, α. Then, another JFET, Q_2, can replace R_2 (**Figure 2**). This JFET has its gate shorted to its source and operates as a constant-current source. You can calculate the R_1 multiplication factor α from the same formula as for **Figure 1**, with the R_2 value replaced by the value of $R_{OUTQ2} = 1/g_{DSQ2}$. You must lower the overall supply voltage, V_{DD}, accordingly to provide the same operating point for Q_1. The processing stage, the amplifying stage, or both immediately following the preamplifier should not have too small a differential input resistance; this resistance appears in parallel with R_2 or Q_2, so it reduces the multiplication factor, α. A noninverting input of an operational amplifier easily satisfies this requirement.

Choosing a less common but still reasonable value of $R_1 = 100$ MΩ pushes the low-frequency cutoff below 1 Hz with no other changes in the circuit necessary. The dynamic range of the preamplifier is respectable. The maximum permissible positive swing of the input voltage is equal to the forward threshold voltage of Q_1's gate-insulating pn junction multiplied by the same multiplication factor, α, as the input resistance. In the circuit of **Figure 1**, with the cited component values, at a 300K temperature and $V_{CC} = 115$V, the permissible swing exceeds 5V peak. The JFET alone determines the noise figure; hence, it is rather low. The maximum permissible negative swing of the input voltage is usually much larger. A second possible solution of the low-frequency-cutoff problem in capacitive-sensor analog preamplifiers appears in the case of electret-biased sensors. These sensors need no external polarizing voltage, thus simplifying the overall power-sup-

ply design. In these cases, you can achieve an even larger multiplication factor of the biasing resistance by applying unity positive voltage feedback in an operational amplifier (**Figure 3**).

To obtain a full unity positive voltage feedback in the circuit, the value of R_3 should be zero. A minor complication exists, however. To prevent dc instability (bistable flip-flop behavior), a dc path in the positive-feedback circuit must not exist. C_2 is the dc-blocking device. Unfortunately, C_2 introduces another pole in the transfer function of the circuit. To render its effects negligible, C_2 would need an uncomfortably large value. As long as you are prepared to sacrifice a bit of the otherwise extremely large R_1-value multiplication factor, α (theoretically equal to the open-loop voltage gain of the operational amplifier, or 105, typically), you can use a C_2 value several orders of magnitude smaller under the condition that doing so introduces some additional damping into the circuit by means of a nonzero value of R_3. R_2 is necessary to provide a correct dc potential (quiescent operating-point conditions) for the noninverting input of the operational amplifier.

A detailed analysis of the circuit in terms of stability and its response to harmonic and step-signal drive is rather lengthy. You can base the analysis on the rules of general active-filter theory, or you can simulate the circuit behavior with any of the common simulation tools, such as Spice. By an intelligent choice of passive-component values, you can easily control the circuit's behavior in terms of low-frequency cutoff. Thus, you can obtain a maximally flat frequency response or a maximally flat transient response or set a predetermined amount of overshoot in the response to a step input, for example. The operational amplifier must have quiescent dc currents of both inputs as low as possible. CMOS op amps are best in this respect. The circuit of **Figure 3** requires a somewhat larger space for components in the immediate vicinity of the sensor, as well as four instead of three connecting leads. On the other hand, it is less sensitive to external loads than are the circuits in **figures 1** or **2**.

The op amp in **Figure 3** is a TS271, a CMOS op amp from STMicroelectronics (www.stmicroelectronics.com). The low-frequency cutoff is at 7 Hz, and the step-response overshoot is 0%. With larger values of C_2 and smaller values of R_3, you can easily achieve a low-frequency cutoff of 0.1 Hz or lower. The circuit in **Figure 3** is well-suited for micropower applications. Using a micropower CMOS operational amplifier, you can reliably obtain 10 years of unattended operation with standard passive components and just a single coin-sized lithium cell as the power source. The properties of the operational amplifier fully determine the high frequency cutoff and dynamic range of the circuit in **Figure 3**.

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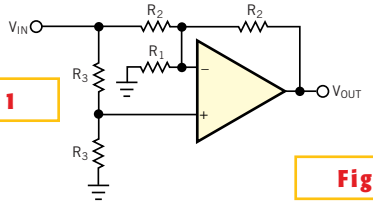
Noninverting op-amp circuit has simple gain formula

José Carrasco and Ausias Garrigós, Universidad Miguel Hernández, Elche, Spain

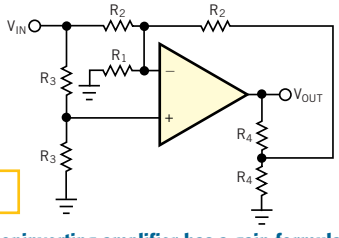
Basic textbooks describe inverting and noninverting amplifiers based on operational amplifiers. These amplifiers have different gain equations. Whereas in the inverting configuration, the gain is the ratio of the feedback and input resistances, in the noninverting amplifier, the gain ratio has an added term. In some designs and for the sake of simplicity, it would be desirable to have a simple, proportional gain ratio (for gains above and below unity) for both inverting and noninverting amplifiers. The noninverting amplifier in **Figure 1** has a simple, proportional formula for the gain: $V_{OUT}=V_{IN}(R_2/2R_1)$. This gain is proportional to a resistor ratio and can take any value. R_3 has no influence on the gain. If you need a noninverting amplifier with a gain ratio identical to that of an inverting amplifier, the circuit in **Figure 2** fills the bill. Its close-approximation gain formula is $V_{OUT}=V_{IN}(R_2/R_1)$.

Figure 1



This noninverting amplifier has a simple, proportional gain formula.

Figure 2



This noninverting amplifier has a gain formula identical to that of an inverting amplifier.

However, in the circuit of **Figure 2**, some restrictions in the choice of R_4 arise. The accuracy of the gain formula of the circuit depends on R_4's being much lower in value than R_1 or R_2. Nevertheless, comparing the exact expression for the gain and the above approximation proves that R_4 is 10 times lower in value than R_1 or R_2, whichever is smaller, and the gain error the approximation gives is less than 5%. For an exact computation, the error is equal to $R_4/2\times(1/R_1-1/R_2)$. For the selection of R_4, you should take into account the fact that most op-amp ICs have maximum output currents of approximately 20 mA.

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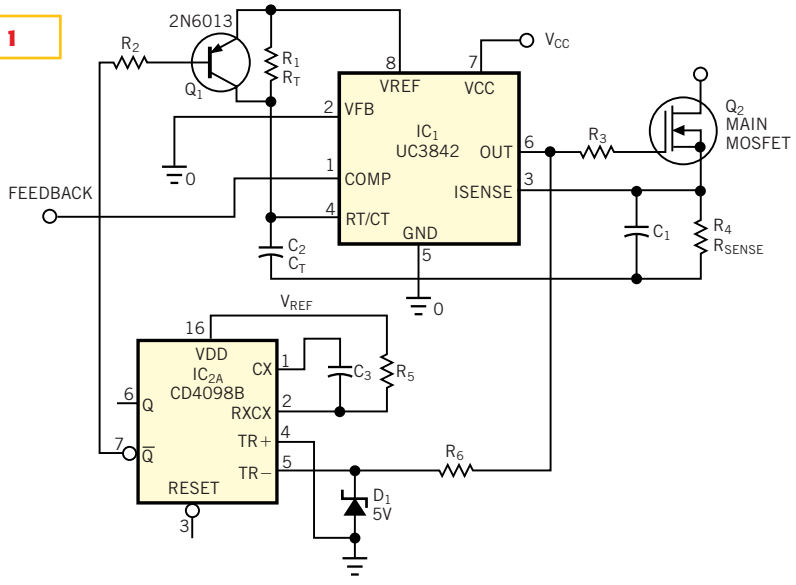
Controller IC and one-shot form resonant controller

C Rajan, Centre for Advanced Technology, Indore, India

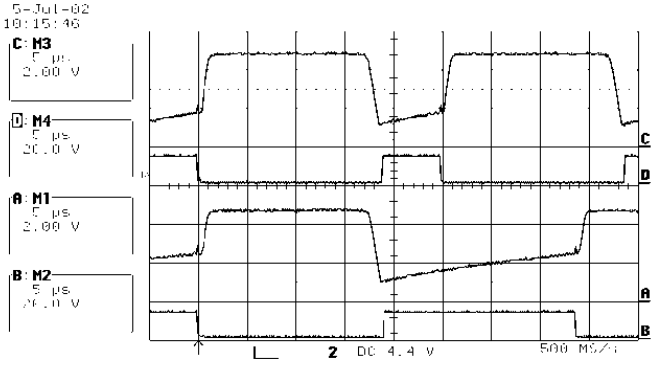
Resonant power supplies are popular because of high efficiency, low noise, and compactness. You can implement a resonant buck or boost converter using a single switch. The regulation of the output in such a converter derives from using a constant on or off time and a variable frequency. The UC1864 controller IC (Texas Instruments, www.ti.com) meets all the requirements for a single-switch quasiresonant converter. But you also can achieve this performance with the inexpensive and popular UC3842 current-mode controller in conjunction with a one-shot multivibrator. This circuit gives the desired current-mode operation along with constant off-time, variable-frequency operation. **Figure 1** shows the controller circuit, configured as a resonant flyback converter for high-voltage generation. For the implementation of this function, the current-mode controller should have 100% duty cycle; thus, you can use the UC3842 or 3843. This circuit uses the 3842. The operation of the circuit is as follows.

Figure 1



This resonant flyback configuration uses only a controller IC and a one-shot multivibrator.

Figure 2



These waveforms typify operation at low (traces C and D) and high (traces A and B) duty cycles.

The output of IC_1, the UC3842, is in a high state until the internal current-sense comparator goes high, and then the output of the IC switches low. As the output voltage goes low, IC_2, the negative-edge-triggered one-shot CD4098B, triggers, and it generates a pulse. The pulse duration is a function of the values of R_5 and C_3, and this time interval is the constant off-time of the UC3842. The $\overline{Q}$ output of the one-shot sinks the base current of transistor Q_1 during this period, and so the transistor conducts. This action adds a 5V pulse to the ramp at the RT/CT pin (Pin 4). This voltage remains at 5V until the pulse ends and $\overline{Q}$ goes high. As it goes high, Q_1 turns off, but the voltage across CT is 5V, which is higher than the upper threshold of the RT/CT pin, so the internal circuitry pulls the pin's voltage to zero, and a fresh ramp and a fresh cycle start.

You must select RT and CT in such a way that the output voltage goes low before the ramp voltage reaches its upper-threshold level. If not, a glitch can occur in the output, arising from the time constant consisting of the output resistance of Q_2 and CT. **Figure 2** shows the voltage waveforms at low and high duty cycles. Traces D and C show the output and RT/CT-pin voltages, respectively, at a low duty cycle and, hence, high frequency. Traces B and A show the same voltages, but at a higher duty cycle (low frequency). You can see that the off-time is fixed in both conditions, and only the frequency changes to achieve the desired duty cycle. The voltage at the RT/CT pin gives a clear view of how the circuit modifies the ramp. This control circuit generates a 2-kV, 5-mA dc power supply using a resonant flyback scheme, and it performs well.

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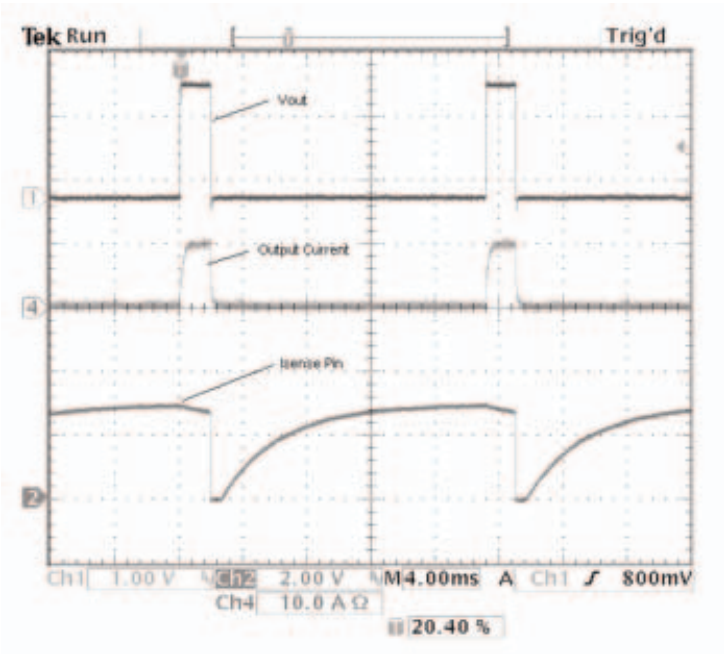
Circuit folds back current during fault conditions

Martin Galinski, Micrel Semiconductor, San Jose, CA

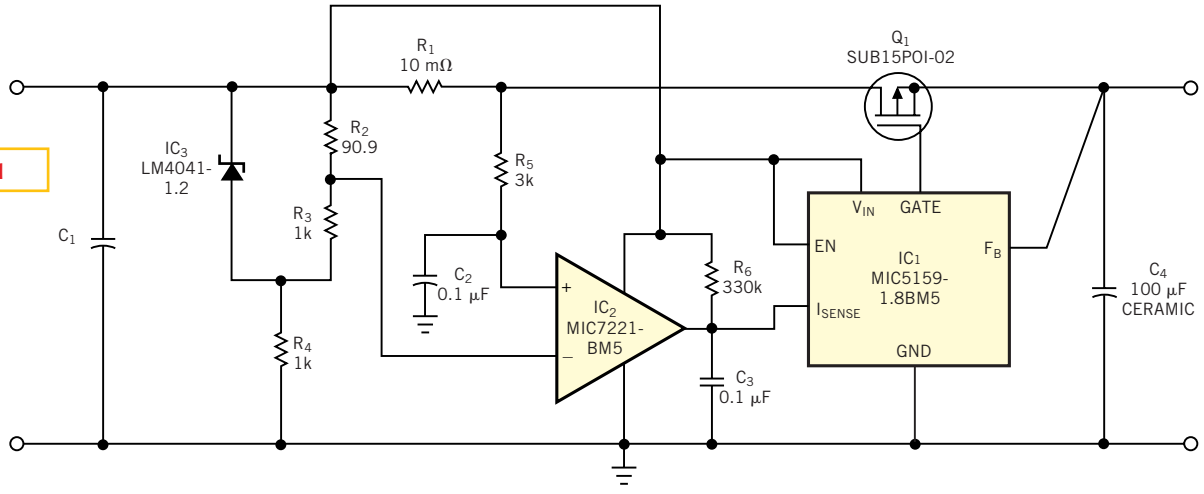
You can use monolithic linear regulators at currents lower than 5A for most applications. Most manufacturers of these devices integrate current-limiting and thermal shutdown to prevent damage during fault conditions. For currents greater than 5A, most linear supplies use controllers that allow the user to select the pass element to handle different current requirements. Although these linear controllers may offer current limiting, they generally don't support thermal shutdown. This limitation requires the design to handle the maximum power dissipation and maintain an acceptable junction temperature in the pass element. For example, assume that you use a 1.8V, 8A linear supply operating from a 2.5V rail. The power dissipation in the pass element equals $(V_{IN}-V_{OUT})\times I_{OUT}=(2.5V-1.8V)\times 8A=5.6W$. Over the specified temperature range, the pass element must be able to dissipate this amount of power and have a junction temperature lower than the maximum allowable for that device. This approach probably requires three to four D-Pack-size MOSFETS. A big problem arises when you examine power dissipation in a sustained short circuit. Then, the pass element must accommodate 20W of dissipation. It would require 10 D-Pack-size MOSFETs to maintain an acceptable junction temperature. Thus, you must overdesign the supply, increasing cost and board size to

Figure 2



The circuit in Figure 1 cycles current in the event of a fault condition.

Figure 1



This circuit provides foldback current-limiting, thus reducing the power-handling requirements of the pass element.

survive a possible fault condition. The circuit in **Figure 1** solves the problem of current-limit power dissipation.

The circuit uses a separate control loop that "folds back" the currents during a fault condition without involving the problems of linear-foldback current limiting. Linear foldback can have problems tripping the current limit during start-up and returning to full load after a fault condition disappears. These problems tend to lock up the regulator in current-limited state. IC_3 provides a high-side reference below the supply voltage and places this voltage on the inverting pin of comparator IC_2. The comparator compares this reference signal with the MOSFET side of R_1. When the current exceeds the current-limit threshold, IC_2's inverting-input voltage is greater than that of the noninverting input. This state causes the comparator to pull the current-sense pin on IC_1 low. You can calculate the current-limit threshold as follows:

$$\text{CURRENT LIMIT} = \frac{V_{IN} - \left(V_{IC3} \times \frac{R_2}{R_2 + R_3}\right)}{R_1};$$

$$\text{CURRENT LIMIT} = \frac{2.5 - \left(1.225 \times \frac{90.9}{90.9 + 1000}\right)}{10\ \text{m}\Omega};$$

$$\text{CURRENT LIMIT} = 10.207\,\text{A}.$$

When the current-sense pin drops 50 mV below the input, the regulator turns the output off. This action then causes the current to go to zero, creating a high condition on the output of the comparator. The comparator has an open collector; therefore, the I_{SENSE} pin charges at the RC charge rate of R_6 and C_3. The output of the regulator remains off, drawing no current, until the I_{SENSE} pin charges to 50 mV below V_{IN}. At this point, the output turns on. R_5 and C_2 provide a delay before re-engaging the current limit. This delay prevents the current required for charging the output capacitors from prematurely tripping the current limit. It also gives the circuit time to stabilize and to determine whether it can deliver the output current that the load demands. If the load is still too heavy, the current limit re-engages. **Figure 2** is an oscilloscope photo of this circuit in operation. This cycling of current, although periodically delivering maximum current, integrates over time into a lower average current. You can calculate average current as a ratio of on- to off-time: $I_{AVG} = I_{PK} \times (T_{ON}/T_{OFF}) = 10.2\text{A} \times (2\text{msec}/17\text{msec}) = 1.2\text{A}$. This reduced average current equates to a reduction in power dissipation. At 1.2A, the power dissipation decreases to 3W.

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design ideas

Edited by Bill Travis

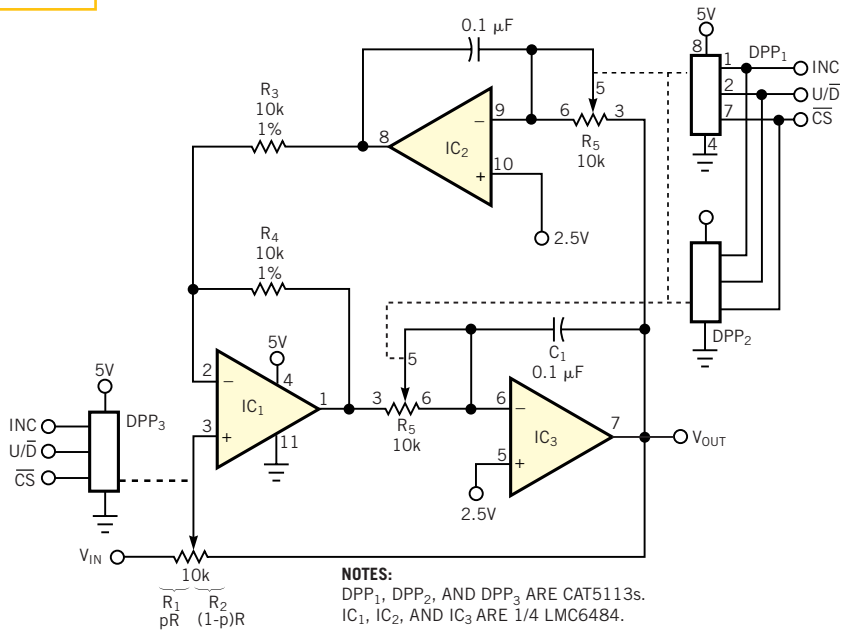
DPPs program key parameters of bandpass filter

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

THE THREE-AMPLIFIER implementation of the state-variable filter in **Figure 1** provides for second-order bandpass, highpass, and lowpass responses. The strength of the circuit, however, is in the bandpass response (V_{OUT}/V_{IN}), in which it's easy to achieve high gain (G) and high Q. These two characteristics are important in applications in which selectivity is a key parameter in the filter. The application value of the circuit becomes even greater when DPPs (digitally programmable potentiometers) control and vary the bandpass filter's center frequency, f_0, and passband gain, G. The independent control of a bandpass filter's parameters is a rarity among traditional filter-circuit techniques.

For the filter, IC_1 functions as a summing amplifier, and IC_2 and IC_3 function as integrators. Three potentiometers, DPP_1, DPP_2, and DPP_3, program the center frequency and passband gain of the filter. The 100-tap Catalyst potentiometers, DPP_1 and DPP_2, are electronically ganged to program the frequency, f_0, and DPP_3 programs the gain, G. The center frequency is $f_0=1/(2\pi R_5C_1)=1/(2\pi pRC_1)$, and the gain is $G=R_2/R_1=(1-p)/p$, where p represents the relative position of the wiper from one end (0) of the potentiometer to the other end (1). R represents the DPP's end-to-end resistance. The gain and Q are related by $Q=(1+G)/2$. The increment/decrement interface of the CAT5113 DPP allows for real-time, closed-loop applications, in which you can continuously vary the center frequency of the filter to track an input signal or to accommodate a system-level requirement. For the values shown, the center frequency varies from less than 200 Hz to more than 6 kHz with gain values as high as 25.

Figure 1



Using digitally programmable potentiometers, you can control a passband filter's center frequency and gain.

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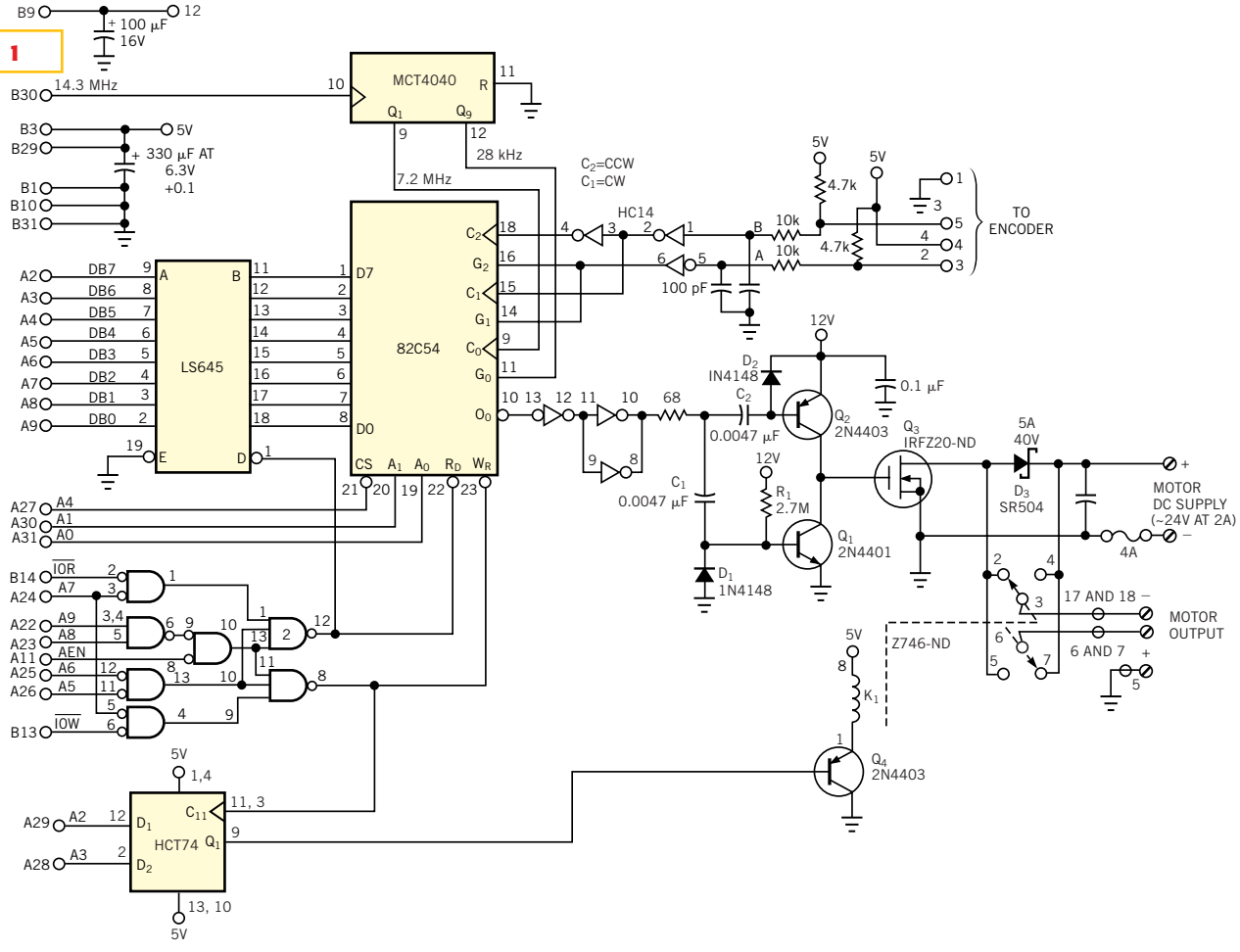
Encoder and PC make complete motor-control system

Steve Woodward, University of North Carolina, Chapel Hill, NC

THIS DESIGN IDEA COMBINES a simple ISA-bus-resident interface circuit; a garden-variety PC; a high-resolution optical shaft encoder; and a PWM-controlled, 0.05-hp, brushed, permanent-magnet dc motor to make a high-precision and high-power motion-control system. The system sequences the precise rotation of an evacuated steel bell jar several feet in diameter, such as those used in molecular-beam spectroscopy (**Figure 1**). Although the speed of the intermittent rotation of the jar isn't fast, the system needs large torques to overcome the friction of a large O-ring seal that is subjected to tens of tons of atmospheric pressure. Moving against this drag requires a heavy-duty drive that energizes a 48W (24V, 2A) motor. A different choice of MOSFET in **Figure 1** would allow the system to handle even heavier loads.

The quadrature-output, incremental optical shaft encoder that this Design Idea uses is popular in high-performance, bidirectional, rotation-sensing applications. Incremental encoders provide an inexpensive and reliable means for digital readout of bidirectional mechanical motion. They're usable to 10,000 rpm and higher. However, the interface logic they need can sometimes be problematic. Such logic typically includes at least one 16-bit or longer bidirectional counter. Several handy peripheral chips, such as the 8253, 8254, and 9511, are available that implement *unidirectional* counting, but *bidirectional* counter chips are comparatively scarce. ASICs can provide the

Figure 1



This block of bidirectional logic and a PC comprise a complete motion-control system.

needed functions, and hard-wired or programmable logic is a viable, though component-count-intensive, option.

Unfortunately, none of these options is ideal from either a cost or a pc-board-area standpoint. This alternative combines the industry-standard 82C54 unidirectional counter-timer peripheral chip with simple software to create a convenient interface between quadrature encoders and the ISA PC I/O bus. Thus, you can easily digitize bidirectional motion. The trick is to use two of the three unidirectional counters in the 82C54—one for each encoder-rotation direction. **Reference 1** describes the logic involved in detail. This Design Idea expands upon the material in **Reference 1** by closing the motion-control loop with an 8-bit-resolution, digital PWM motor-speed-control circuit. The PWM modulator consists of counter-timer 0 (CT0) of the 82C54, operating in retriggerable-one-shot mode and controlling the Q_1-Q_2 drivers for the MOSFET, Q_3.

The HC4040 provides a 7.2-MHz clock to CT0 and triggers CT0 at 28 kHz (7.2 MHz/256). The result is a variable-duty-factor PWM waveform at CT0's output (O_0). Q_1 and Q_2 buffer and boost the waveform to 12V p-p and apply the boosted waveform to the gate of MOSFET Q_3. The MOSFET then modulates the 24V-dc motor-supply rail and thus generates a more-than-95%-efficient, programmable motor-speed control. The motor's armature inductance combines with flyback diode D_3 to filter the high-frequency components of the 28-kHz PWM waveform and to extract the dc component. Minimizing the time the MOSFET spends between full-off and -on states is critical to the efficiency of this PWM circuit, as in all power-handling topologies.

The Q_1-Q_2 driver circuit achieves fast MOSFET on/off transition times of approximately 10 nsec, as well as minimal 12V supply-power consumption. The driver circuit achieves these two goals by avoiding saturation-induced cross-conduction of Q_1 and Q_2. The circuit avoids the cross-conduction by taking advantage of the fact that Q_3's gate presents an almost entirely capacitive load to the Q_1-Q_2 pair. Therefore, although currents of approximately 100 mA into Q_3's gate are necessary during on/off transitions to ensure efficiency-promoting speed, the drive requirement drops to zero between transitions. The circuit takes advantage of the situation by using capacitive drive to Q_1 and Q_2. Coupling capacitors C_1 and C_2 deliver robust base drive during rise and fall edges but virtually no drive after the transitions. Hence, the circuit avoids cross-conduction of the bipolar transistors. Meanwhile, R_1 provides just a trickle of dc bias to Q_1, so that Q_3 and, therefore, the motor stays off before the programming of the 82C54, regardless of whatever arbitrary state the IC may assume after power-up. Q_4 is a pnp transistor that controls the direction-reversing relay, K_1. **Listing 1** is an MBasic demo program for the motion-control system. You can download the software from the Web version of this Design Idea at www.ednmag.com.

LISTING 1—MBASIC DEMO PROGRAM FOR MOTION CONTROL

```
DEFINT I
IOADD = &H300: ' BASE ADDRESS FOR MOCONT CARD
IC0 = IOADD: IC1 = IC0 + 1: IC2 = IC0 + 2: ICS = IC0 + 3: ' 8254 COUNTER
ADDRESSES
IREV = 4: ' MOTOR-REVERSE BIT

OUT ICS, &H12: ' PROGRAM PULSE-WIDTH GENERATOR IN C0
OUT ICS, &H70: OUT ICS, &HB0: ' SETUP CW/CCW COUNTERS IN C1 AND C2

OUT IC0, 5: 'START PULSE-WIDTH GENERATOR
OUT ICS, &HDC: 'LATCH CW/CCW
I1L = INP(IC1): ICW = INP(IC1)
I2L = INP(IC2): ICCW = INP(IC2)
OUT IC1, I1L: OUT IC1, ICW: '...INITIALIZE CW/CCW COUNTERS
OUT IC2, I2L: OUT IC2, ICCW
OFFSET = I1L - I2L + 256! * (ICW - ICCW)

CLS : PRINT TAB(20); "MOTION-CONTROL-ADAPTER DEMO"
PRINT TAB(18); "W. S. Woodward...March 16, 1990"
PRINT "POSITION=": PRINT : PRINT : PRINT
PRINT "HIT '1' TO SLOW BY 4 STEPS OUT OF 256"
PRINT "     '2' TO SLOW BY 3"
PRINT "     '3' TO SLOW BY 2"
PRINT "     '4' TO SLOW BY 1"
PRINT "     '5' TO SPEED UP BY 1 STEP"
PRINT "     '6' TO SPEED BY 2"
PRINT "     '7' TO SPEED BY 3"
PRINT "     '8' TO SPEED BY 4"
PRINT
PRINT "     'R' TO STOP AND REVERSE"
PRINT
PRINT "     'T' TO INVERT SPEED SETTING"


AROUND:

OUT ICS, &HDC: 'LATCH CW/CCW
I1L = INP(IC1): I1M = INP(IC1): IF I1M > ICW THEN OFFSET = OFFSET + 65536
ICW = I1M
I2L = INP(IC2): I2M = INP(IC2): IF I2M > ICCW THEN OFFSET = OFFSET - 65536
ICCW = I2M
LOCATE 3, 10: PRINT I1L - I2L + 256! * (I1M - I2M) - OFFSET

IKEY = INSTR(" 1234-5678RT", UCASE$(INKEY$)) - 6: IF IKEY <= -5 THEN GOTO AROUND
IF IKEY = 5 THEN IKEY = -ISPEED + 1: IC1 = IC1 XOR IREV: IC2 = IC2 XOR IREV: IC0
= IC0 XOR IREV: ICS = ICS XOR IREV
IF IKEY = 6 THEN IKEY = (ISPEED XOR 255) - ISPEED
ISPEED = ISPEED + IKEY: IF ISPEED > 0 AND ISPEED < 256 THEN OUT IC0, ISPEED ELSE
ISPEED = ISPEED - IKEY
GOTO AROUND
```


Reference

1. Woodward, Steve, "Unidirectional counters accumulate bidirectional pulses," *EDN*, April 11, 2002, pg 72.

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Use PSpice for behavioral modeling of VCOs

Dobromir Dobrev, Jet Electronics, Sofia, Bulgaria

PSpice, a member of the Spice family for PC users, is becoming a standard tool for analog and mixed analog-digital simulation. Many analog designers are familiar with the software of Design Center, Design Lab, and OrCad (www.orcad.com) PSpice and use the software in their everyday lives. This Design Idea should be helpful to those who design and simulate PLL systems at a behavioral level. A basic PLL system comprises a phase detector, a loop filter, and a VCO (voltage-controlled oscillator), connected in a negative-feedback loop. The phase detector produces a voltage that, after low-pass-filtering by the loop filter, becomes an error voltage, V_E, applied to the control input of the VCO to set the angular frequency, (ω). When $V_E=0$, the VCO oscillates at some initial frequency, ω_0, called the frequency offset or free-running frequency. The output frequency of the VCO is:

$$\omega(t)=\omega_0+G_{VCO}V_E(t). \quad (1)$$

Here,

$$G_{VCO}=\frac{d\omega}{dV_E}=2\pi\frac{df}{dV_E}=2\pi g_{VCO}, \quad (2)$$

where G_{VCO} is the VCO's voltage-to-radian frequency gain in radians per second per volt and g_{VCO} is the VCO's voltage-to-frequency gain in hertz per volt. Consider a sinusoidal voltage with amplitude V_{AMPL}, argument $\theta(t)$, and dc offset V_{OFF}:

$$V(t)=V_{AMPL}\sin(\theta(t))+V_{OFF}. \quad (3)$$

The argument $\theta(t)$ is the time integral of the angular frequency:

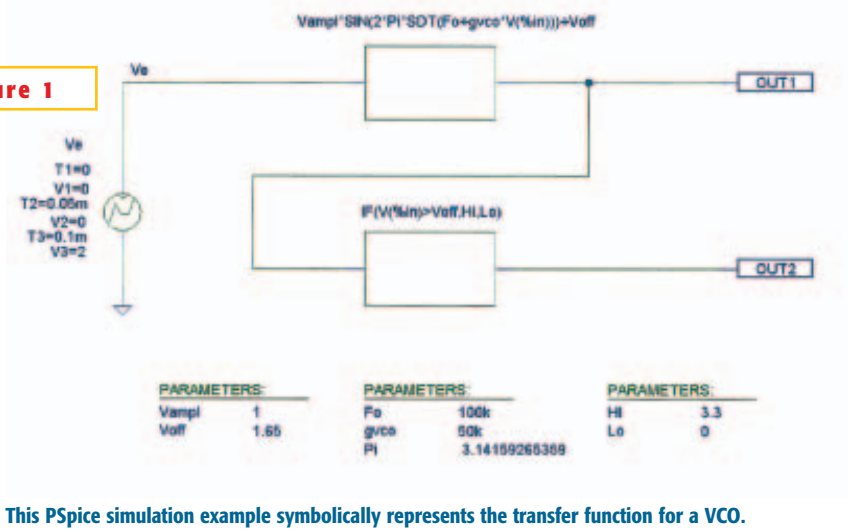
$$\theta(t)=\int\omega(t)dt+\theta(0). \quad (4)$$

Assuming ω is constant and substituting $\theta(t)$ in $V(t)$ yields the popular form:

$$V(t)=V_{AMPL}\sin(\omega t+\theta(0))+V_{OFF}. \quad (5)$$

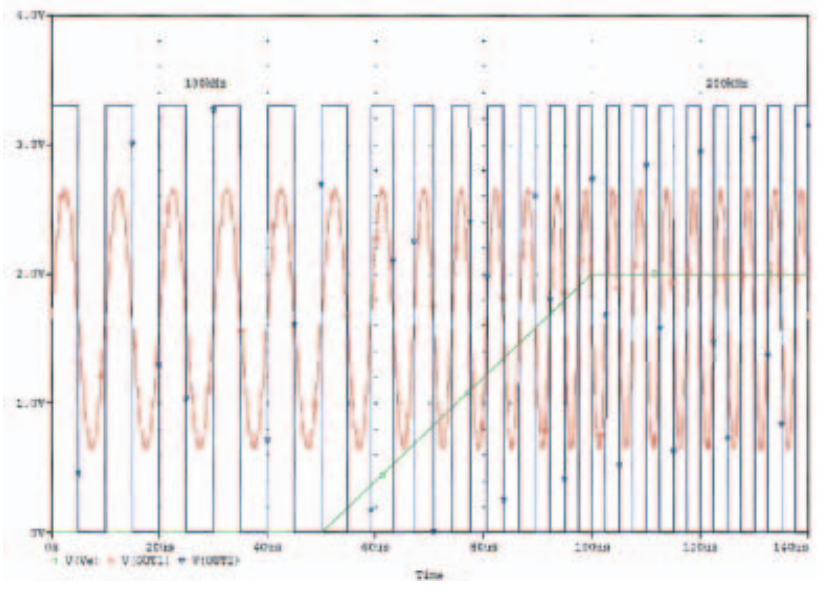
If ω is not constant, the general form is:

Figure 1



This PSpice simulation example symbolically represents the transfer function for a VCO.

Figure 2



A simulation example shows the results for the behavioral model of a VCO.

$$V(t)=V_{AMPL}\sin\left(\int(\omega(t)dt+\theta(0))\right)+V_{OFF}. \quad (6)$$

Replacing $\omega(t)$ with **Equation 1** and considering $\theta(0)=0$, you obtain the VCO's transfer function:

$$V_{VCO}(t)=V_{AMPL}\sin\left(\int(\omega_0+G_{VCO}V_E(t))dt\right)+V_{OFF}=V_{AMPL}\sin\left(\omega_0t+G_{VCO}\int V_E(t)dt\right)+V_{OFF}. \quad (7)$$

Equation 7 is the heart of the VCO's time-analysis modeling. Thus, you can easily perform VCO behavioral modeling, using the ABM1 part from the Analog Behavioral Modeling Symbol Library abm.slb (abm.olb in OrCad Capture). You can simply write the formula for the transfer function, adapted for PSpice. **Figure 1** shows the PSpice representation of the process. **Figure 2** shows a simulation example, in which V_E is the VCO's input voltage, and $V_{(OUT1)}$ is the output voltage. Because most phase detectors (types I, II, and III) use a digital input signal, you can easily obtain a digital VCO-output waveform using the conditional expression above the lower box in **Figure 1**. The simulated curve is $V_{(OUT2)}$, also shown in **Figure 2**. Finally, for loop-gain evaluation in ac analysis, you simply model the VCO in the frequency domain in an ideal integrating unit, using the Laplace form $T_{VCO}(s)=G_{VCO}/s$. Most obvious behavioral VCO models are based on a real circuit concept. Thus, they comprise many elements—for example, controllable sources, capacitors, and others. Hence, the models are complicated. This modeling is simple without involving superfluous computation resources.

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Circuit delivers high voltage swing from lower supplies

Bruce Carter and Ron Shakery, Texas Instruments, Dallas, TX

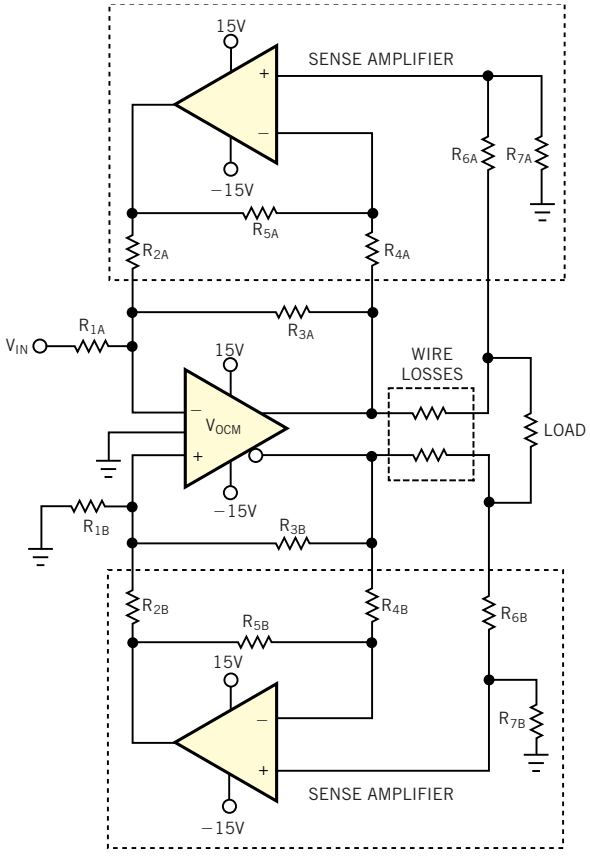
The need for higher voltage swings in applications such as test-and-measurement instruments is constantly increasing, but the power supplies impose limitations on the operational amplifier rails make the high-voltage need a challenge for designers. How do you deliver high-voltage swings to a load without increasing the voltage levels of the power supplies of the operational amplifier? In other words, for example, how can you produce a ±16V or greater signal swing across the load using only ±15V power supplies? The circuit in **Figure 1** uses a fully differential amplifier to offer an answer to this problem. Fully differential amplifiers enable you to deliver an output-voltage swing beyond the rails into the load. One of the common problems in working with operational amplifiers is the limit that the power-supply rails impose. The standard since the days of analog computers has been ±15V. Analog computers are gone, but their legacy remains in the power-supply voltages. These voltages find widespread use in transducer interfaces and applications in which voltage swing and dynamic range are of primary importance.

This ±15V supply voltage notwithstanding, applications exist that require a higher swing range beyond the power-supply limits. Typical ±15V operational amplifiers are seldom optimized for rail-to-rail operation, and their useful output-voltage range may be only 24 to 26V. Many audio consoles use older technology 741 op amps with ±18, ±20, and even ±22V power supplies to obtain more voltage swing and, therefore, more dynamic range from their systems in light of this limitation. The op amps in these systems often run hot and have heat sinks. The advent of fully differential op amps has given designers a better way to extend the output-swing range. Fully differential operational amplifiers 40 to 50 years ago were tube or discrete-transistor units. They have recently re-emerged as a way to interface to fully differential A/D converters and applications in which the load needs differential drive for better swing range or to reduce the noise effects in the systems.

The outputs of fully differential op amps have a characteristic that makes them useful for doubling the swing. The two outputs are 180° out of phase: When one output swings positive, the other swings negative and vice versa. The net effect is similar to what happens in a bridged amplifier: The effective output-voltage range doubles. The price of doubling this output-voltage swing is that you can no longer connect the output load to ground. Designers of automotive audio amplifiers are familiar with this concept: Audio-power bridged amplifiers have a fully differential output. Many installers have learned the hard way that the minus speaker connection cannot connect to ground. When the output voltage doubles, power quadruples. This feature is useful for audio power amplifiers in a limited-power-supply-voltage application.

To illustrate the advantage of fully differential outputs, assume that a fully differential op amp has a voltage-rail limitation of ±13V when operated from ±15V supplies. The absolute- maximum output range of each output is ±13V. But when the top output is at 13V, the bottom output is −13V: (13V)−(−13V)=26V. When the top output is −13V, the bottom output is 13V. As a result, the output voltage is (−13V)−(13V)=−26V. Therefore, the output-voltage range is

Figure 1



Similar to a bridged audio amplifier, this op-amp circuit delivers output-voltage swings to the load beyond the span of the power supplies.

±26V, which enables the output to swing from −26V to +26V, resulting in a doubled voltage-swing range. Fully differential op-amp designs require that the two feedback loops be symmetrical; the components in the top and the bottom sections must be the same. In **Figure 1**'s schematic, the components in the top feedback path are labeled "A," and those in the bottom are labeled "B." When this design references a designator, the comment applies to both paths A and B.

The gain of the overall circuit is $V_{OUT}/V_{IN}=R_3/R_1$. The location of the load is often at the end of a balanced line. You cannot discount the effect of the wire; it affects the amplitude across the load, reducing the expected gain of the system. The sense lines help compensate for the voltage drop across the lines, resulting in the delivery of the targeted voltage to the load. The two sense amplifiers in the schematic are each composed of an op amp and resistors R_4 through R_7. R_2 acts as a summing component, adding small-signal amplitude equal to the voltage drop of the wire back into the input, boosting the op amp's output such that the expected gain appears at the load. If you make R_4 though R_7 equal in value to R_1, then it is easy to calculate R_2: It takes the same value as R_3. If R_4 through R_7 cannot be equal to R_1, then R_3 should be proportional to R_2. You should be aware that the resistors in the sense amplifiers change the load characteristics. For 600Ω audio-distribution systems, this fact is less of a problem than it is in 50Ω systems. You should be aware, however, of the output-drive characteristics of your operational amplifiers, if you wish to deliver the exact desired voltage swing to the load.

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design ideas

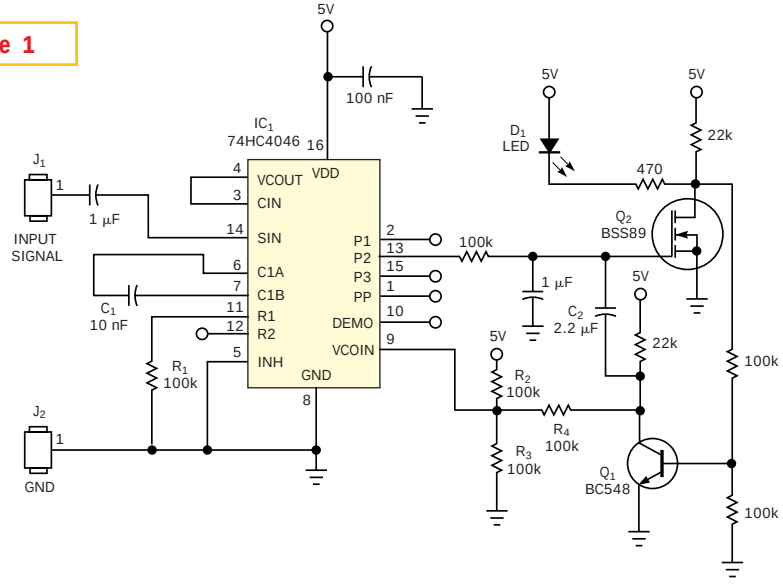
Edited by Bill Travis

Frequency comparator has status output

Susanne Nell, Breitenfurt, Austria

The original application for the circuit in **Figure 1** was to check the number of revolutions of an engine with only one LED as an indicator. The measurement of the number of revolutions usually involves sensors with a frequency output proportional to the number of revolutions. The circuit compares the frequency output of such a sensor with a lower and upper limit and gives a visual result, using one LED. If the frequency is below the lower limit, the LED remains unlit. If the frequency is between the limits, the LED blinks at a constant rate, and if the speed is higher than the upper limit, the LED stays permanently lit. Although a microcontroller can do this job, it is sometimes better to use an analog circuit—for example, if the frequency you want to check is too high for a simple controller. The circuit in **Figure 1** uses one standard, inexpensive IC, and you need not write any software. It is also less costly than a comparable microcontroller-based circuit.

Figure 1



This analog frequency comparator uses an LED to indicate upper and lower frequency limits.

The main part is IC_1, a 74HC4046 PLL chip. With a 12V supply, you can also use the CD4046 without an additional voltage regulator. The chip contains an oscillator, a phase comparator, and one amplifier for the input signal. The input signal connects to the input of the phase comparator with its integrated ac amplifier. The circuit compares this amplified signal with the VCO frequency. This frequency is adjustable, using C_1, R_1, and the voltage on Pin 9. If the frequency of the input signal is lower than that of the VCO, the output of the phase comparator (Pin 13) is low. In this case, Q_2 is off, Q_1 is on, and the LED is off, indicating "low frequency." Resistors R_2, R_3, and R_4 determine the voltage on Pin 9 and the lower frequency limit switching point. If the frequency of the input signal increases and reaches the value of the VCO's frequency, the phase comparator's output switches high.

This high-level output turns Q_2 on and Q_1 off. With Q_1 off, the voltage of the VCO increases to a second higher value determined by R_2 and R_3, and the VCO generates the frequency for the high-limit switching point. If the frequency of the input signal is between these two limits, the phase comparator generates a rectangular waveform. The feedback capacitor, C_2 determines the frequency of this waveform. With a value of 2.2 µF for C_2, you can achieve a frequency of approximately 1 Hz. This frequency is the blinking rate for the LED. If the frequency of the input signal increases to a point higher than the upper VCO frequency value, the phase comparator output stays high, and the LED turns on permanently. With the values shown in **Figure 1**, the lower and upper frequency limits are 3.81 and 7.35 kHz, respectively.

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Envelope follower combines fast response, low ripple

Harry Bissell, Royal Oak, MI

Envelope followers extract amplitude information from complex audio waveforms. The resulting dc voltage often drives nonlinear stages, such as voltage-controlled amplifiers or filters. You must make a careful trade-off between the speed of response to a rapidly changing input signal and the amount of ripple in the dc output that you can tolerate. If the system is too slow, the output has low ripple but badly distorts the envelope shape. If it's too fast, ripple can modulate the nonlinear stages, causing audible distortion products. Audio sources, such as a guitar, pose special problems. The instrument has an attack of a few milliseconds and a long decay time. The musician may "mute" the strings at any time, causing the normal exponential decay to terminate abruptly. The waveform is sometimes unsymmetrical and may have multiple zero crossings. The fundamental frequency range is typically from approximately 80 Hz to 1.5 kHz. Previous circuits have used a full-wave bridge and a large averaging filter. A filter time constant sufficient to reduce ripple makes the circuit unable to follow rapid changes in amplitude. Peak-detecting circuits can follow the rapid attack and provide low ripple during the exponential decay but cannot follow the rapid decay of a muted string. The design in **Figure 1** features fast attack and low ripple with minimal filtering, and it can follow a rapid decrease in signal (mute).

The circuit uses three identical peak-hold circuits in parallel that reset in a round-robin fashion. The circuit applies the input signal to all three stages simultaneously. As each stage resets in turn, the two remaining stages still hold the last peak voltage. Diodes select the highest held voltage at the output of each peak-hold stage. A small RC filter smoothes the step response as the peak-hold circuits reset, so a lower output voltage results. To ensure that one of the detectors holds the highest peak value for the entire input period, the reset clock period is slightly longer than one-half the period of the lowest input frequency. **Figure 2** illustrates typical circuit operation and

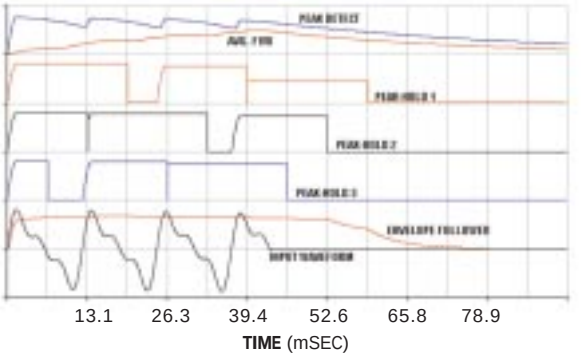
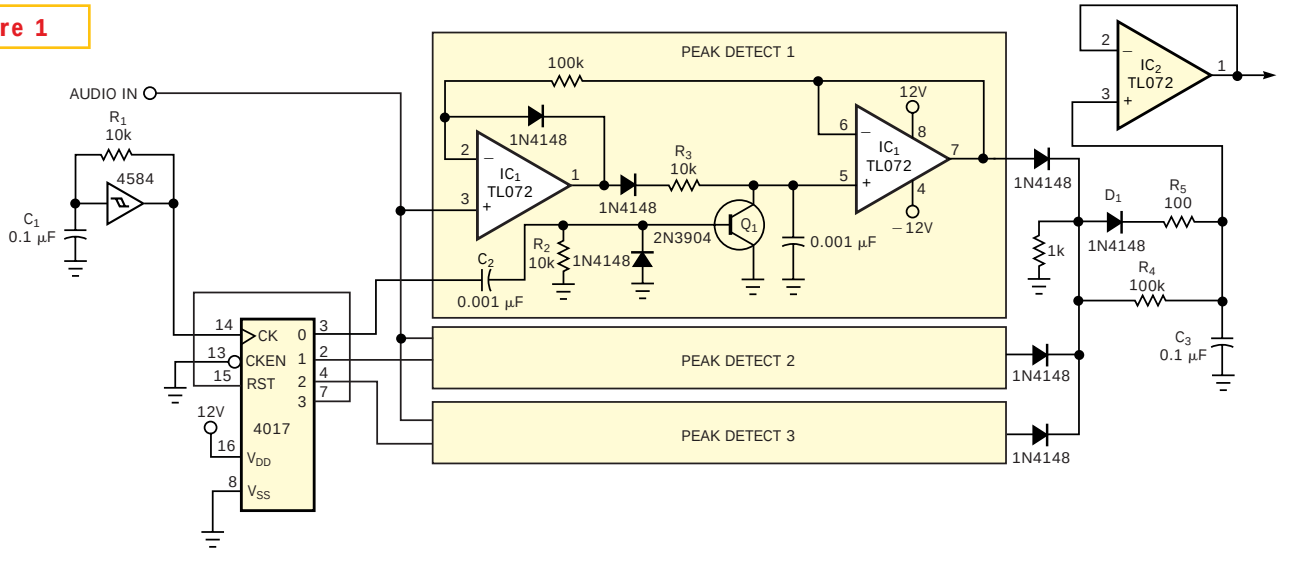


Figure 2 Waveforms of typical circuit operation show the improvement over full-wave average and peak-detecting circuits with similar time constants.

Figure 1



This envelope detector provides the seemingly contradictory features of fast response and low ripple.

shows the improvement over full-wave average and peak-detecting circuits with similar time constants. CMOS Schmitt inverter IC_1 forms the master reset clock, and C_1 and R_1 produce the desired period. CMOS counter IC_2 is a ring counter that provides the sequential reset pulses. The peak-hold circuit is a classic configuration with the addition of the reset circuit. R_2 and C_2 differentiate the rising edge of the reset pulse; this edge drives the base of Q_1. Series resistor R_3 prevents excessive op-amp current while Q_1 is conducting. The filter network comprising R_4, R_5, C_3, and D_1 provides minimal filtering to reduce the step changes in the output during unusually fast decay times.

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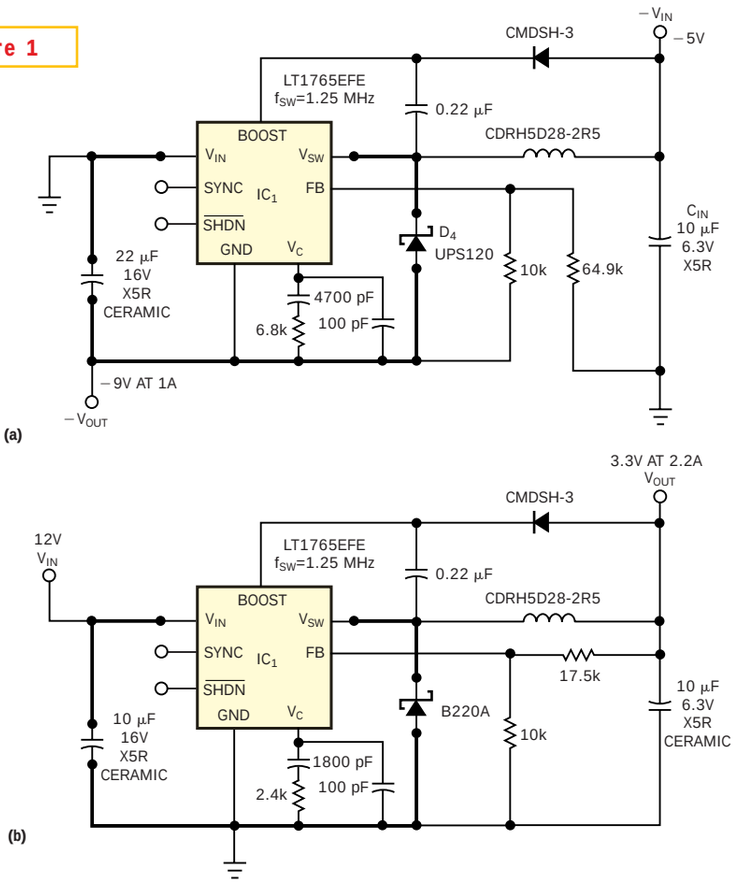
Positive regulator makes negative dc/dc converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Power-supply designers can choose from a plethora of available positive buck regulators that can also serve as negative boost dc/dc converters. Some buck regulators have a negative-feedback reference voltage expressly for this purpose, but ICs that have positive-reference feedback voltages far outnumber these negative-feedback regulators. You can take advantage of this greater variety of devices by using a positive buck switch-mode regulator to create an excellent negative boost converter. All you need are a few small modifications to the typical buck-converter configuration. **Figure 1a** shows a −5V-input to −9-output, 1.4A negative boost converter using the LT1765EFE positive-buck-converter, switch-mode regulator. This IC accepts 3 to 25V input, uses a 1.2V feedback voltage, and has an internal 3A power switch. The 1.25-MHz switching frequency of the LT1765EFE helps reduce the size of the inductor and input and output capacitors**. Figure 1b** shows a typical positive-buck-converter application for the LT1765EFE: a 12V-input to 3.3V-output, 2.2A dc/dc converter. **Figure 2** shows an efficiency plot for the regulator in **Figure 1a**.

Figure 1



The LT1765EFE positive buck converter can make a negative boost converter (a) or a positive buck converter (b).

In **Figure 1a,** the ground pin of the IC connects to the negative voltage V_{OUT}. This connection makes the negative-boost-converter configuration provide a positive voltage at the FB pin with respect to the ground pin of the IC. In this topology, the maximum input voltage rating of the IC has to be greater than the magnitude of output voltage for the negative boost converter. The IC must also have a minimum input-voltage rating that is less than the magnitude of the input voltage, to ensure that the circuit turns on upon power-up, because the output voltage can have an initial state of 0V.

Note that the maximum output current for the negative boost converter in **Figure 1a** is much lower than the maxi-

mum output current of the positive buck converter in **Figure 1b**, even though they use the same switch-mode-regulator IC. The buck-converter IC in both circuits has an internal power switch with a switch current rating of 3A. You choose the inductor based on maximum output current, peak switch current, and desired ripple current. First calculate the duty cycle (DC) and then calculate either the ripple current, I_{PP}, based on the chosen inductor, L, or the inductor value based on the desired ripple current. It is generally good practice to choose the inductor value so that the peak-to-peak ripple current is approximately 40% of the input current. These calculations are approximate and ignore the effect of switch, inductor, and Schottky-diode power losses. You calculate as follows:

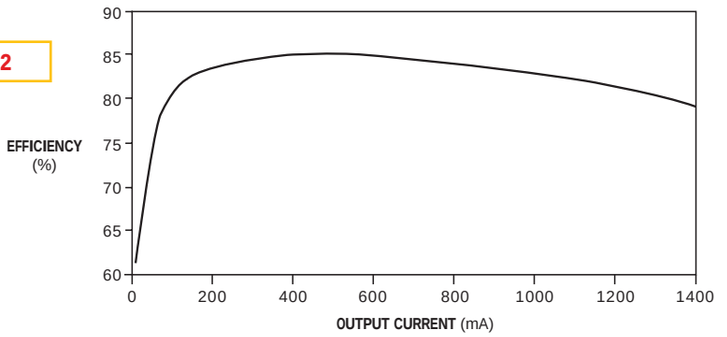
$DC=(V_{OUT}-V_{IN})V_{OUT}$; $I_{IN}\sim(V_{OUT}\times I_{OUT})/(V_{IN}\times\eta)$, where η is the overall efficiency. $I_{PP}=I_{IN}\times 40\%$; $I_{PP}=(DC\times V_{IN})/(f\times L)$, where f is the switching frequency; and $L=(DC\times V_{IN})/(f\times I_{PP})$.

Maximum inductor current, I_{LMAX}, is equal to the peak switch current in this configuration. The IC has a maximum switch current, I_{SWMAX}, of 3A, so the maximum inductor current must remain below 3A. To keep switch current below the maximum, you might need more inductance to keep the ripple current low enough. ($I_{LMAX}=I_{SWMAX}=I_{IN}+I_{PP}/2$.) Maximum output current, I_{OUTMAX}, is an approximation derived from the maximum allowable input current given the ripple current: $I_{OUTMAX}=(I_{SWMAX}-I_{PP}/2)\times(V_{IN}\times\eta)/V_{OUT}$. As in a typical boost converter, the input capacitor in the negative boost topology has low ripple current, and the output capacitor has high discontinuous ripple current. The size of the output capacitor is typically larger than that of the input capacitor to handle the greater rms ripple current:

$I_{CINRMS}=I_{PP}/\sqrt{12}$, and $I_{COUTRMS}=\sqrt{(1-DC)}\times(I_{IN}^2+I_{PP}^2/12)$.

The output capacitor's ESR has a direct effect on the output-voltage ripple of the dc/dc converter. Choosing higher frequency switch-mode regulators reduces the need for excessive rms ripple-current rating. Regardless, a low-ESR output capacitor, such as a ceramic, can minimize the output-voltage ripple of the negative boost converter: $\Delta V_{OUTPP}=I_{SWMAX}\times ESR_{COUT}$. **Figures 1a** and **1b** show the high-di/dt switching paths of the negative boost and positive buck dc/dc converters. You must keep this loop as small as possible by minimizing trace lengths to minimize trace inductance. The discontinuous currents in this path create high di/dt values. Any trace inductance in this loop results in voltage spikes that can render a circuit noisy or uncontrollable. For this reason, circuit layout can be just as important as component selection. Note that the layout of a negative boost regulator differs from that of a positive buck regulator, even though they use the same IC.

Figure 2



Efficiency of the negative boost converter in Figure 1a is as high as 85% and typically greater than 80%.

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Multiplexer amplifiers form large, multiplane-multiplexer structures

Bill Stutz, Maxim Integrated Products, Sunnyvale, CA

The variety of video sources available to a home-video-switching system has grown from a few composite inputs to many multisignal sources. These sources include cable, HDTV, satellite dishes, VCR, DVD, video games in broadcast, and multi-PC or graphic KVM (keyboard-video-mouse) applications. Each requires an N×M-to-1 multiplexer, in which M is the number of sources and N is the number of channels that make up the signal. As an example, 16 RGB or Y, Pb, and Pr sources require a 3×16-to-1 multiplexer. Constructing such a multiplexer is difficult, and programming the source selection requires that you combine the individual 16-to-1 multiplexer control with the three channels (**Table 1**). You can configure a group of analog multiplexers as a large, multiplane video multiplexer that easily selects

multichannel video sources, such as YC, RGB, and Y Pb Pr. The cited 3×16-to-1 multiplexer comprises six 8-to-1 multiplexers (**Figure 1**) controlled by a 4-bit binary code for source selection. (MAX4315 ICs include a 2V/V fixed-gain output buffer.)

The only external circuitry required is an SN7404 hex inverter for inverting the shutdown signals and 75Ω source and load resistors for implementing unity gain when driving a back-terminated load. Substituting a MAX4312 eight-channel video multiplexer with variable-gain output buffer allows variable gain and rejects input common-mode voltages. The high bandwidth and slew rate of these ICs make them ideal for selecting standard video and high-definition broadcast video, as well as graphics sources with UXGA and higher resolutions for KVM applications. The design requires no additional buffering, because the ICs can directly drive 150Ω back-terminated coaxial cable to within less than 0.75V of the supply rails, using single or dual supplies. Their 40-nsec switching speed and 10-mV p-p glitch voltage allow, in addition to source selection, insertion of on-screen display, closed captioning, and teletext in broadcast and graphics video.

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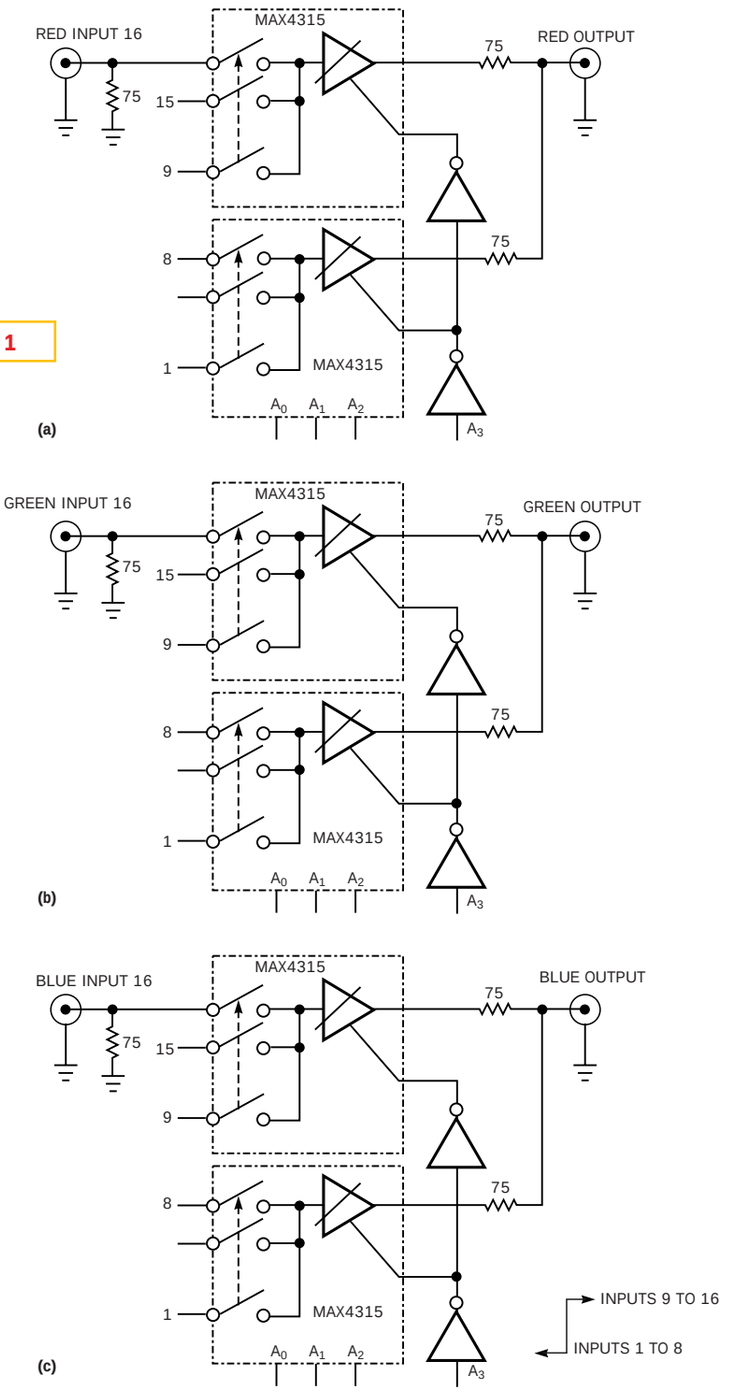
TABLE 1—SOURCE-SELECTION PROGRAMMING

RGB	A0	A1	A2	A3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

Figure 1



This multiplane multiplexer selects any one of 16 input signals, each of which comprises red (a), green (b), and blue (c) channels.

Circuit provides watchdog for microcontrollers

VM Holla, Bangalore, India

The watchdog circuit in **Figure 1** uses a single NAND Schmitt-trigger IC. The circuit is more cost-effective than dedicated, commercially available watchdog ICs. The circuit generates an active-high reset signal upon power-up and remains in a low state as long as the control input receives pulses. Whenever the pulsing at the control input stops, whether the circuit is in a high or a low state, the circuit emits a reset signal. Upon power-up, both inputs of gate IC_{1C} are low, forcing the Reset output to switch high and the $\overline{\text{Reset}}$ to go low. Thus, the outputs of both IC_{1B} and IC_{1D} are high. The high outputs charge the capacitors in the circuit, and, when both inputs of IC_{1D} reach a high level, the Reset output goes low, and $\overline{\text{Reset}}$ goes high. As long as the control input receives pulses, the outputs of IC_{1B} and IC_{1D} deliver pulses. The pulses hold the input of gate IC_{1C} high and the Reset output low.

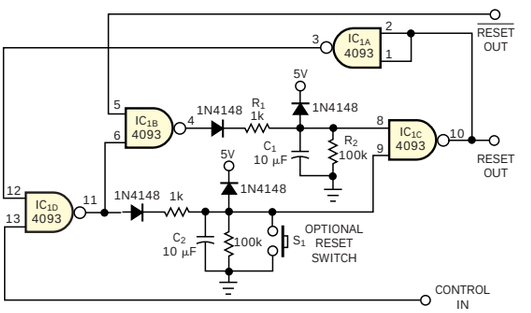


Figure 1 This watchdog-timer circuit is a cost-effective alternative to dedicated watchdog ICs.

When the control signal remains in a high state, C_2 begins discharging. When the control signal switches low, the Reset output goes high. The same scenario prevails with C_1 when the control signal remains low. You can choose the values of R_1, C_1, R_2, and C_2 as a function of the watchdog-time duration and the reset pulse width required. With the values shown, the circuit is appropriate for MCS51-family microcontrollers. The duration of the watchdog time is approximately 300 msec, and the reset pulse width is approximately 10 msec.

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Circuit translates I²C voltages

Peter Liu, Optron X, Allentown, PA

This Design Idea explores level-shifting an I²C bus from 5V/ground (positive domain) to ground/−5V (negative domain). In multisupply systems, you sometimes face a situation in which digital information stored in logic circuits running from 5V to ground needs conversion to analog signals referenced to a negative supply. Converting from digital to analog in the positive domain and then level-shifting to reference the negative rail introduces errors and results in a large component count. A better approach is to level-shift the digital data lines and convert with negative-referenced A/D converters. I²C is a bidirectional system employing a two-wire bus: one clock line and one data line. Pullup resistors and open-collector outputs establish dominant-low signaling. **Figure 1** shows a typical setup, in which the microcontroller is the master, and all the peripherals are slaves. Each device has a unique I²C address. The master always generates the clock, but, depending on

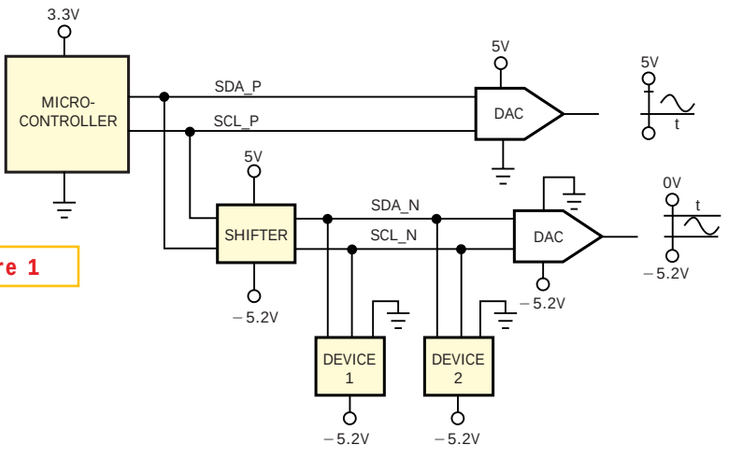
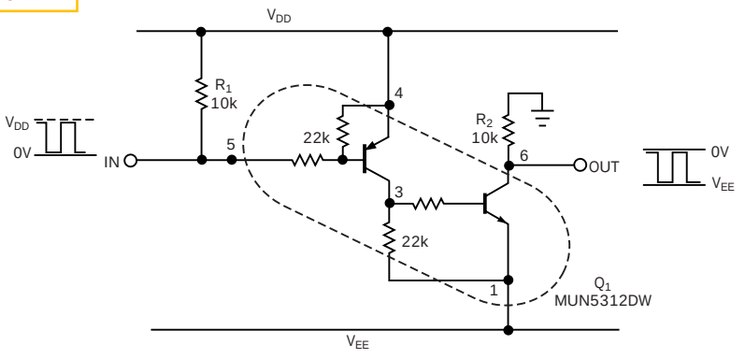


Figure 1 In this typical I²C configuration, the microcontroller is the master, and all the peripheral devices are slaves.

the desired direction of data flow, either the master or the slave could be the transmitter on the data line.

To understand the level-shifting procedure, consider the simple circuit in **Figure 2**. The circuit level-shifts the clock line unidirectionally. Q_1 comes with a pnp, an npn, and four bias resistors, all in one small SOT-363 package. R_1 provides the necessary pullup function in the positive domain, and R_2 does the same in the negative domain. The operation of the circuit is straightforward. When V_{IN} is set to V_{DD}, Q_1 remains off, so $V_{OUT}=0V$ (logic high). When V_{IN} is set to 0V, Q_1 is on, so $V_{OUT}=V_{EE}$ (logic low). This unidirectional circuit does not allow the master to detect when the slave holds the clock low. Therefore, if you desire I²C clock-extension (wait-stating), you would need a bidirectional level-shifting circuit.

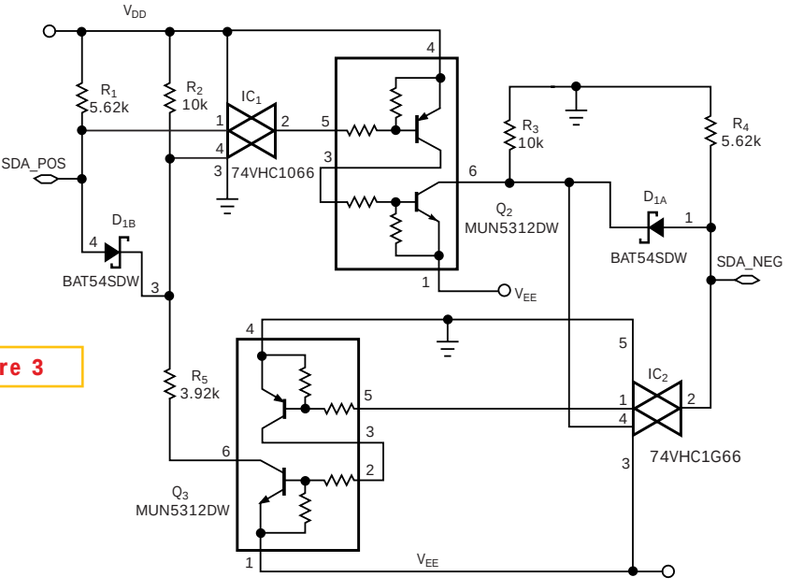
Figure 2



This transistor arrangement level-shifts the data or clock signals from positive to negative levels.

The data line needs a bidirectional circuit. Even when the master is transmitting, the master needs to detect when the negative-domain slave pulls the data line low on every ninth bit to acknowledge the transmitted byte. Also, when instructed, the slave may need to transmit data back to the master. In the slave-transmitter mode, the slave would have to detect when the master pulls the data line low on every ninth bit to acknowledge the transmitted byte. Despite this added complexity, you can still accomplish the task with just five SOT-363-size packages and five discrete resistors (**Figure 3**). To see that the circuit in **Figure 3** is topologically the same as the one in **Figure 2**, assume transmission gates IC_1 and IC_2 are on and ignore the lower half of the circuit for the moment. With SDA_POS set to V_{DD}, Q_2 is off, R_3 and R_4 pull up to 0V, resulting in SDA_NEG=0V (logic high). With SDA_POS set to 0V, Q_2 is on, so SDA_NEG~VEE (logic low).

Figure 3



A bidirectional level shifter translates data and clock signals from positive levels to negative levels, and vice versa.

Now, trace the return path from slave to master. With SDA_NEG set to 0V (logic high), Q_3 is off, and R_1 pulls SDA_POS up to V_{DD}. With SDA_NEG set to V_{EE} (logic low), Q_3 is on, and $R_1||R_2$ forms a voltage divider with R_5 to yield SDA_POS~0V. You select R_1, R_2, and R_5 to yield $V_{DD}=5V$ and $V_{EE}=-5.2V$. If desired, you could use additional transistors to construct the return path so that it doesn't depend on resistors to set logic levels. Transmission gates IC_1 and IC_2 and Schottky diodes D_{1A} and D_{1B} break the positive feedback path that would otherwise result when either master or slave pulls SDA to a logic low. Note that, without these components, Q_2 and Q_3 would form a latch. The circuit in **Figure 3** easily meets I²C timing requirements at a 50-kHz clock rate. For 100-kHz operation, it is best to use an MUN5311, which has 10-kΩ internal resistors instead of 22 kΩ. You can use the same bidirectional circuit in **Figure 3** for the clock signal, to cover all the I²C modes of operation.

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