Design Ideas from EDN

Small circuit forms programmable 4- to 20-mA transmitter
High-side current sensor monitors negative rail
Transconductance amp gives oscillator reciprocal response
Buck IC boosts battery voltage for white LED
Switched-capacitor IC and reference form elegant –48 to +10V converter
Buck converter handles battery-backup system
Circuit disconnects load from low-voltage supply
Circuit forms gamma-photon detector
Circuit ensures safety in power-on operation

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Supply delivers pin-programmable multiple references
Design an efficient reset circuit
One-shot provides frequency discrimination
Circuit forms novel floating current source
Circuit provides Class D motor control
Small, 915-MHz antenna beats monopole
Digital signal controls sine generator
Transmitter accurately transfers voltage input
Absolute-value circuit delivers high bandwidth
Microcontroller directs supply sequencing and control
Circuit provides leading-edge blanking
MOSFETs reduce crosstalk effects on analog switches
Grounded resistor tunes oscillator
Obtain higher voltage from a buck regulator

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LED driver delivers constant luminosity
Get more power with a boosted triode
White-LED driver touts high efficiency
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Active-clamp/reset-PWM IC becomes more versatile
Circuit provides hiccup-current limiting
Microcontroller provides SRAM battery backup
Positive regulator makes dual negative-output converter
Analog switch frees stuck I^2C bus

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Circuit level-shifts ac signals
Interface a serial 12-bit ADC to a PC

Code provides adjustable differential drive for robots
Microcontroller produces analog output
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Scheme adds sequencing and shutdown control to regulator
MathCAD functions perform log interpolation
Scheme improves on low-cost keyboard
ADC interface conditions high-level signals
Two op amps provide averaged absolute value

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Circuit controls microneedle etching
Circuit removes relay-contact bounce
Log-ratio amplifier has six-decade dynamic range
VCXO makes inexpensive dual-clock reference

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Rechargeable flashlight obsoletes lantern battery
Single cell flashes white LED
Hot-swap controller handles dual polarity
Temperature monitor measures three thermal zones
Two DDS ICs implement amplitude-shift keying
VCO produces positive and negative output frequencies
16-bit adjustable reference uses 8-bit digital potentiometers

design ideas

Edited by Bill Travis

Design makes handy audible circuit tracer

Jerry O'Keefe, Cupertino, CA

THE CIRCUIT TRACER in **Figure 1** is a handy tool for finding connectivity paths on a pc board. Because the sense voltage you use to measure the path is lower than a transistor's V_{BE} voltage, you can use the design in circuits containing semiconductor elements without affecting the measurement. The tracer's output takes the form of audio tones. An open circuit produces ticks at the rate of approximately one per second, and a short circuit results in a 2-kHz tone. An audible sensing device is ideal for a circuit tracer, because your eyes can focus on the circuit paths you're tracing and not on a meter movement. If you want to find the connections to a circuit point, a useful technique is to attach a lead to that point and just scan the other lead over the other sections of the circuit. When you hear a high-pitched tone, then you know that you have a pc-board connection.

With practice, you can quickly determine the quality of the circuit path by discerning the wide dynamic range of ticks to tones. You can also detect the presence of capacitors, which produce a sweeping tone as they charge. The circuit in **Figure 1** is sensitive enough to produce a noticeable audio change if you make contact with a circuit with wet fingertips. R_1 produces a 0.4-mA current to bias the current mirror comprising Q_1 and Q_2. Q_1, the resistance-sense transistor, is the heart of the circuit. The resistance between its emitter and V_{CC} determines C_2's charge current. Because C_2 receives current from a constant-current source, the waveform on the capacitor is a linear ramp. When C_2 charges and passes IC_1's threshold, IC_1 generates an output pulse. R_2 determines the discharge rate for C_2. IC_2, a 74C74, converts the NE555 pulses to symmetrical square waves to differentially drive the piezoelectric speaker. With normal, day-to-day use, the 9V battery should last approximately a year.

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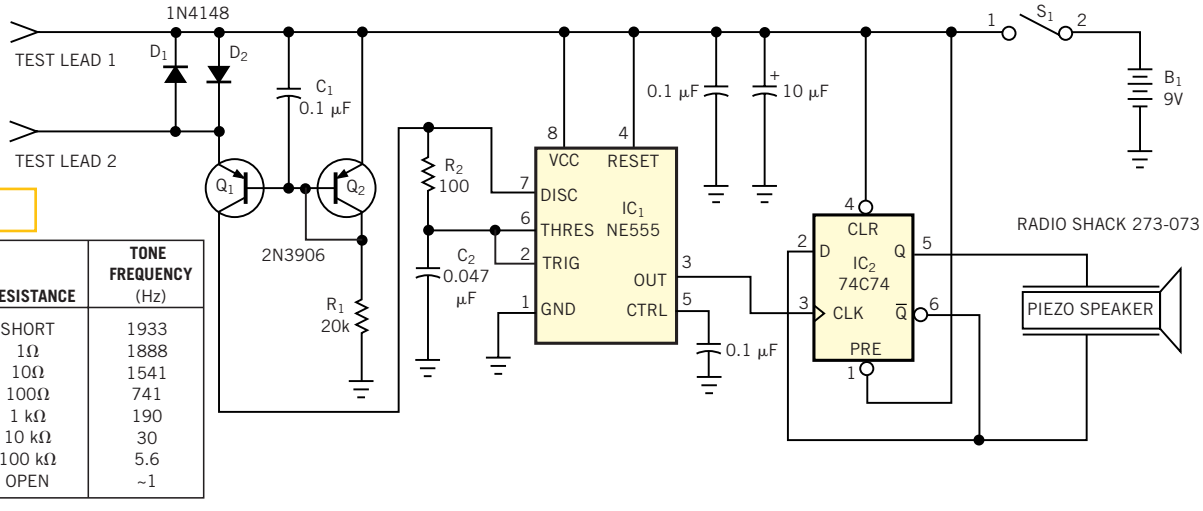


Figure 1

RESISTANCE	TONE FREQUENCY (Hz)
SHORT	1933
1Ω	1888
10Ω	1541
100Ω	741
1 kΩ	190
10 kΩ	30
100 kΩ	5.6
OPEN	~1

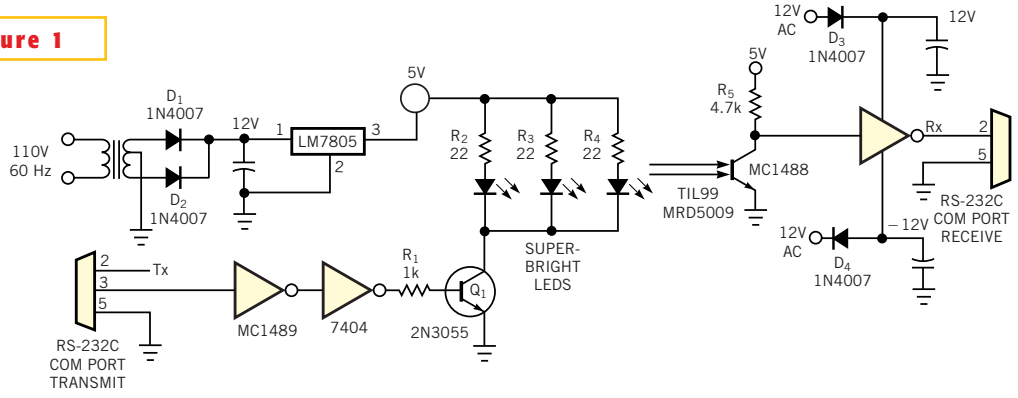
Use your ears to test continuity with this audible-tone circuit tracer.

Design a visible optical link for RS-232C communications

Shyam Tiwari, Sensors Technology Ltd, Gwalior, India

THE DESIGN in **Figure 1** is a visible optical link for those who need to see the transmitted data. An isolation figure of more than 5000V is a bonus. Tests of the system used the COM input of a data-acquisition system, as well as a standard PC's COM port. The MC1489 converts the RS-232C data to TTL signals. A 7404 gate then inverts the signal. The output of the 7404 drives Q_1, a 2N3055 power transistor. The transistor drives the set of three LEDs to form a light source. When no data exists on the RS-232C port, the LEDs remain off. When data transmission takes place, the LEDs glow at the rate of the data transmission. Keep the optical receiver 50 cm away from the LEDs to obtain maximum isolation. The MRD5009 phototransistor directly converts the light to a TTL output. (A TIL99 phototransistor also works well.) You should also isolate the power supply to the MRD5009/TIL99 and the MC1488 from the power supply of the receiver circuit. The MC1488 is a TTL-to-RS-232C converter.

Figure 1



This circuit provides a visible indication of RS-232C data transmission.

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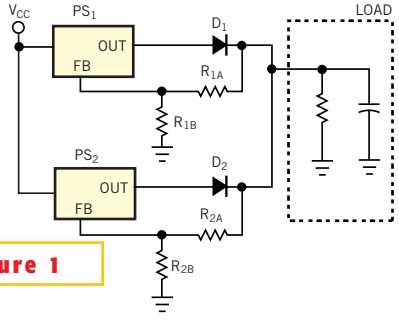
Hot-swap structure offers improved redundancy

Samuel Kerem, Corvus Corp, Columbia, MD

FOR REDUNDANCY PURPOSES, a number of power supplies, using ORing diodes, can work into the same load. During maintenance, when you can remove any power supply, the minimum possible power perturbation at the load is desirable. To compensate for the voltage drop across the ORing diodes, you must connect the power-supply feedback lines after the diodes, at the load. Thus, the feedback connection is common for all participating power supplies (**Figure 1**). Because of natural variations in each power supply, only the one with the highest V_{OUT} is active. The others, sensing the "higher" output voltage, try to reduce their own outputs, effectively turning off their regulation. If you remove the "active" module from the setup similar to **Figure 1**, it causes V_{OUT} to dip (**Figure 2**). **Figure 2a** applies to a linear module that comprises two regulators that have independent 3.339 and 3.298V output voltages. Both have loads of approximately 10Ω in parallel with 100 µF. **Figure 2b** applies to a boost configuration that comprises two regulators with 5.08 and 4.99V outputs, each loaded with approximately 2.5Ω in parallel with 100 µF. The sags and glitches in the voltages arise from the inevitable delay for another power supply to step in and to start the regulation. Costly power-supply bricks deal with this problem by using current-sharing techniques. The techniques provide roughly equal output-current distribution among all power modules, thus keeping all modules ac-

Figure 1



A standard redundant configuration of power-supply modules uses ORing diodes at the outputs.

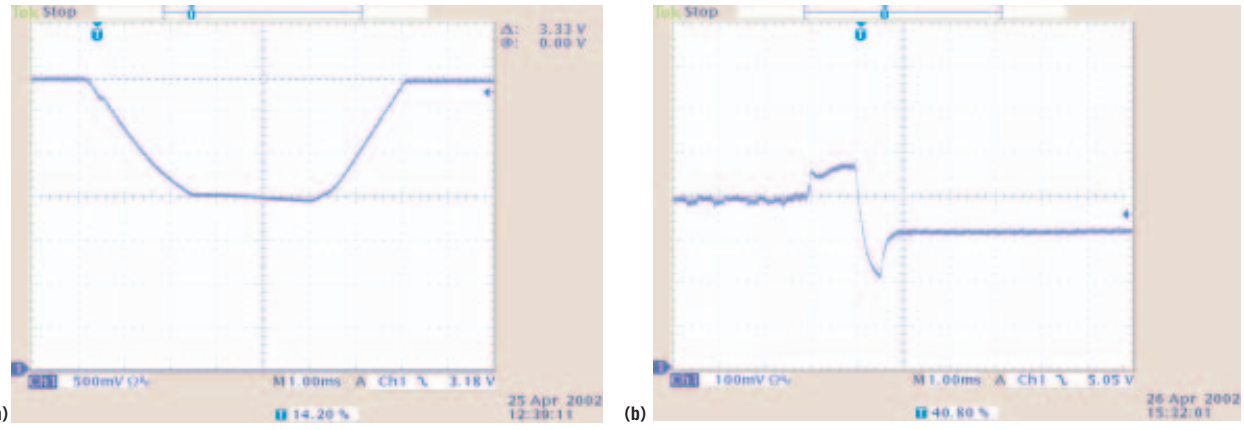


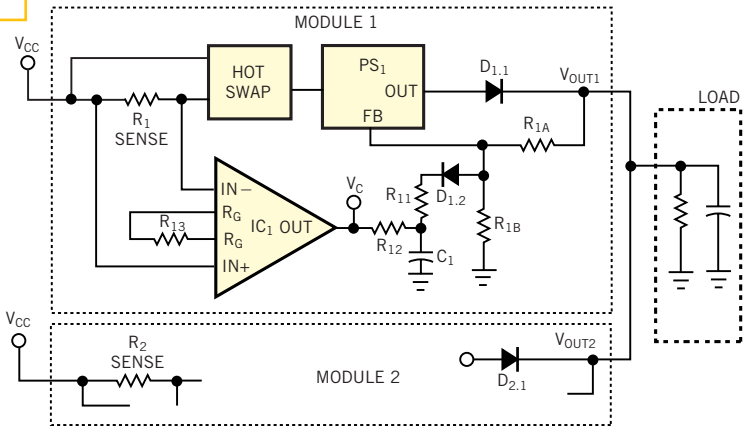
Figure 2

When you remove one supply from the redundant configuration, you incur sags (a) and glitches (b) in the output voltage.

tive. The configuration in **Figure 3** adds little cost to a power system. The improvements in performance are evident in **Figures 4a** and **4b**, representing the two types of redundant power-supply modules.

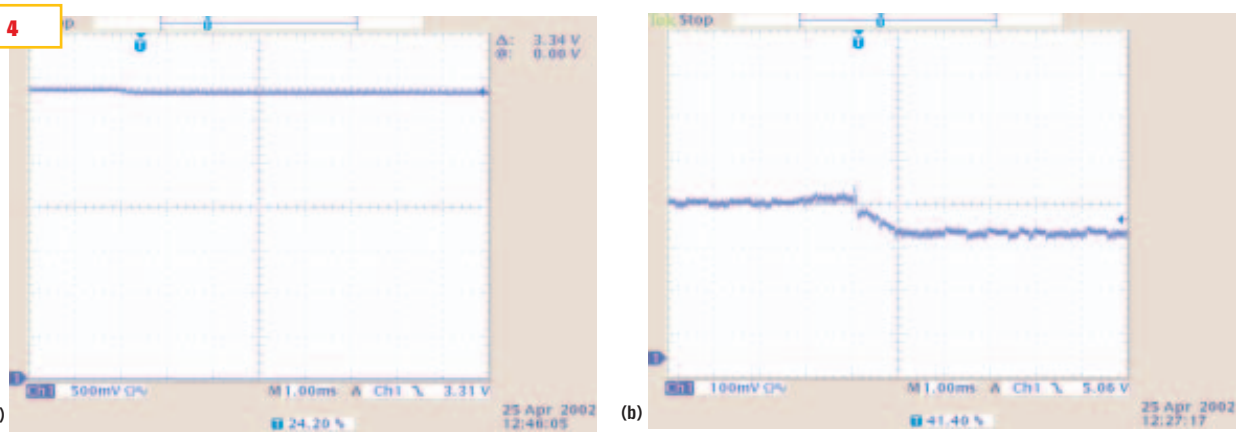
An instrumentation amplifier, IC_1, measures and produces a voltage, V_C, proportional to the current going into the regulator. V_C in turn controls V_{OUT}, pushing the regulator into active mode. For most adjustable controllers, $V_{OUT}=V_{REF}(1+R_A/R_B)$, where R_A is R_{1A}, and R_B is R_{1B} for module 1. If no current flows through R_{SENSE}, IC_1's output is close to ground, paralleling R_{1B} with the resistances of $D_{1.2}$, R_{11}, and R_{12}, thereby making R_B smaller and V_{OUT1} consequently higher. The increase needs only to compensate the V_{OUT} variation be-

Figure 3



The addition of an instrumentation amplifier and a few passive components provides sag- and glitch-free redundant performance.

Figure 4



Linear (a) and boost (b) regulators use the scheme in Figure 3 to eliminate sags and glitches in the output voltage.

tween same-configuration power supplies. This variation is only a few percentage points. If the current into the load rises, V_C also rises, reducing the current through $D_{1,2}$ and consequently reducing V_{OUT1}. When IC_1's output rises and differs from V_{FB} by less than the direct voltage drop across $D_{1,2}$, no current flows through $D_{1,2}$. Thus, V_{OUT1}, for any higher current, stays at the value the above equation defines. With the proper selection of R_3 (the instrumentation amplifier's gain-setting resistor), R_2 and R_1 from other modules provide the required current into the load from all power supplies, guaranteeing that they stay in active condition.

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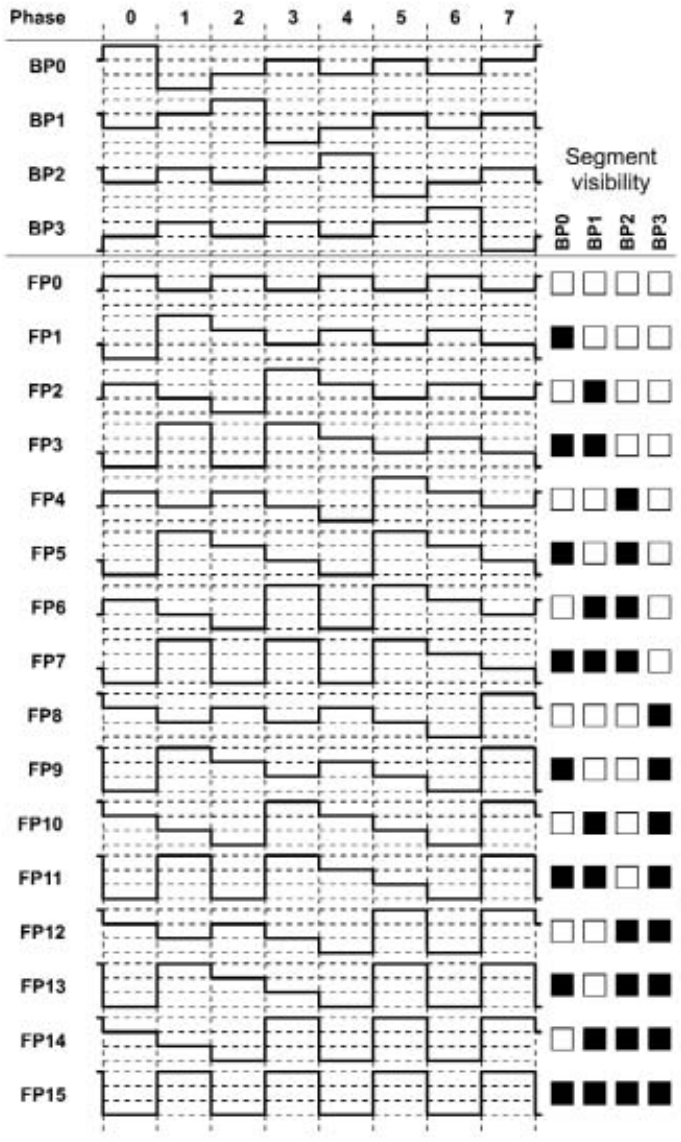
Embedded processor directly drives LCD

Daniel Malik, Motorola, Czech Republic

Driving a bare LCD does not necessarily require specialized interface circuitry or peripherals. This Design Idea describes an alternative drive scheme, which you can easily implement using the general-purpose outputs of a microcontroller. Many embedded-system applications need to interact with a user by displaying simple numeric or alphanumeric characters. Seven- or 14-segment LED displays are readily available at low cost and in many sizes. However, their relatively high power requirements and limited readability in direct sunlight restrict their use in battery-powered, portable devices. LCD modules driven by HD44780-compatible controllers offer simple interface characteristics, low power consumption, and good readability. However, their cost is relatively high, and their large dimensions sometimes preclude their use in small enclosures. Bare LCDs overcome these disadvantages. However, their drive requirements are usually nontrivial. **Figure 1** shows the usual waveforms you use to drive an LCD with four backplanes. The algorithm uses four discrete voltage levels for all LCD signals. Synthesis of such signals without dedicated peripherals or an external controller is difficult and requires many components. Fortunately for users of general-purpose microcontrollers without specialized on-chip peripherals, an alternative exists. **Figure 2** shows the alternative waveforms.

The algorithm uses only three voltage levels on the backplane pins and only two voltage levels on the front-plane pins of the LCD. Such waveforms are easy to synthesize using the general-purpose pins of

Figure 1



In the standard waveforms for driving LCDs, the algorithm uses four discrete voltage levels for all LCD signals.

a microcontroller. **Figure 3** shows a typical application of the alternative algorithm, using a general-purpose microcontroller. You implement the BPx (backplane) connections using general-purpose, tristatable outputs of the microcontroller. The FPx (frontplane) connections require only ordinary, general-purpose outputs. You obtain the $V_{DD}/2$ voltage on the BPx pins by tristating the microcontroller's pins. (You can usually obtain this result by configuring the pins as inputs.) Modern microcontrollers operate from a wide range of power-supply voltages. Altering the microcontroller's power-supply voltage is an effective way of adjusting the LCD's contrast. **Figure 4** shows examples of LCDs driven by general-purpose microcontrollers from Motorola (www.motorola.com). **Figure 4a** shows a display with two×11-segment organization; for **Figure 4b,** the organization is four×16 segments. **Figure 5** shows the modification of the waveforms for the smaller display of **Figure 4a**, using only two backplanes.

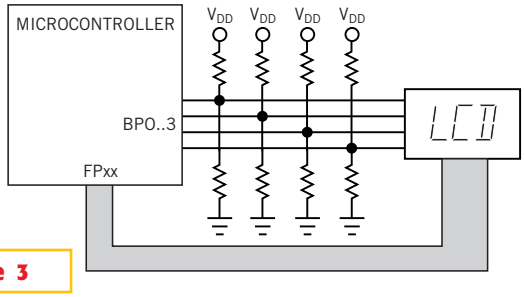


Figure 3

You can use a general-purpose microcontroller to drive any size LCD.

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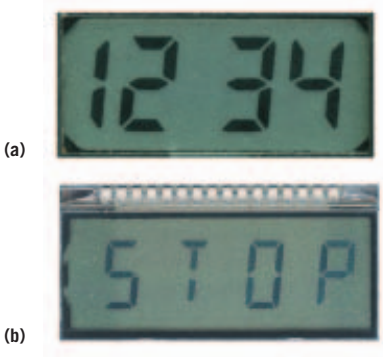


Figure 4

A general-purpose MC68HC908GP32 drives a two×11-segment LCD (a) and a four×16-segment LCD (b).

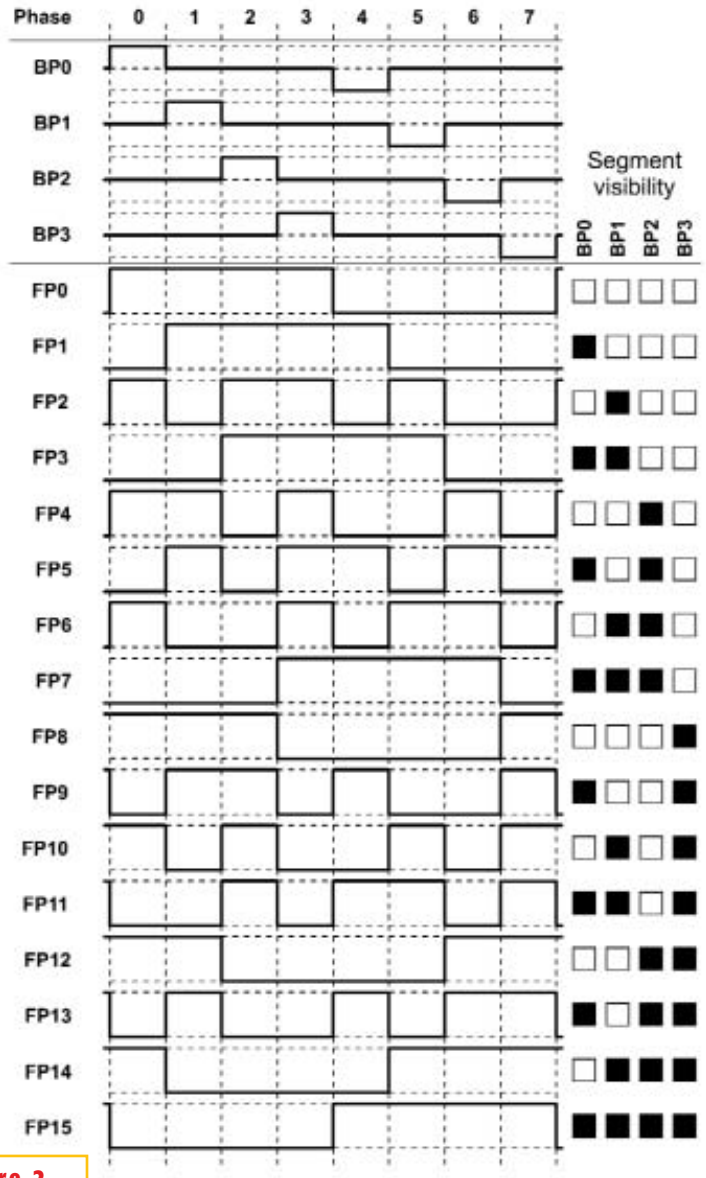


Figure 2

Alternative LCD-drive waveforms use only three voltage levels on the backplane pins.

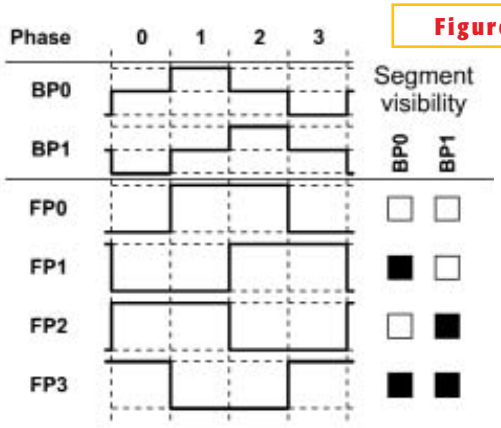


Figure 5

This modification of an LCD has only two backplanes.

design ideas

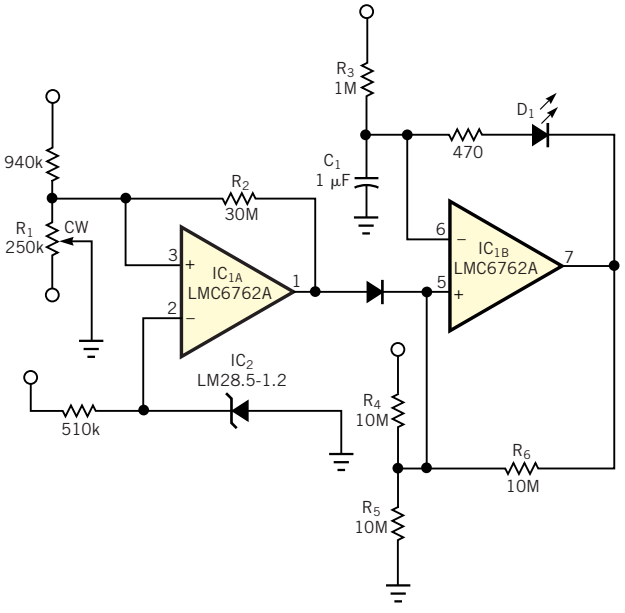
Edited by Bill Travis

Fleapower flasher draws less than 50 µA

Gary Butterfield, IEC Electronics Technology Center, Newark, NY

Some applications require a circuit to indicate that a battery's voltage has fallen below a certain value. However, if you don't frequently check the indicator, the low-battery indicator itself can easily discharge the battery. The circuit in **Figure 1** indicates when the battery voltage has dropped below a preset value. The circuit draws less than 50 µA, regardless of whether the indicator flashes. IC_{1A} operates as a simple comparator. IC_2, a low-current voltage reference, supplies the reference voltage to Pin 2 of comparator IC_{1A}. Resistor R_1 provides an adjustable trip point. A potentiometer setting of 124 kΩ yields a trip point of approximately 10.3V. When the power-supply voltage is above the trip point, IC_{1A}'s Pin 1 is high, forward-biasing diode D_1 and holding the flasher in the off state. R_2 provides approximately 300 mV of hysteresis for the detector. IC_{1B} provides the flashing of the LED. C_1 charges through R_3, and, when its voltage exceeds the voltage at IC_{1B}'s Pin 5, Pin 7 pulls low, discharging the capacitor through the LED. Resistors R_4 and R_5 provide a voltage reference, and resistor R_6 provides hysteresis of approximately one-third of the supply voltage.

Figure 1



This fleapower flasher indicates a low-battery condition with a flashing LED.

The circuit's current consumption is 45 µA at 10V, climbing to 48 µA at 12V. The state of the flasher does not affect current consumption, because the LED receives its power via the capacitor. You have to make a number of trade-offs to achieve this low current consumption:

For example, discharging the capacitor through the LED allows the circuit to reuse the capacitor's charge, instead of dumping it to ground. It also eliminates the current spikes that occur when driving the LED from the supply rail. However, the charge on the capacitor limits the resulting LED brightness, so you should use high-efficiency LEDs when possible.

Another trade-off is that the LED affects the minimum operating voltage because of the forward voltage drop of the diode. In the prototype, a red LED works down to a lower operating voltage of 4.3V. A yellow LED in the same circuit operates down to 6.4V. Additionally, the high resistances on the board, most notably the resistors attached to IC_{1B}'s Pin 5, require careful attention to board cleanliness. Small leakage currents can significantly affect circuit operation and current drain. You can reduce the values of these resistances to improve manufacturability at the expense of higher current consumption.

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PC-based configurable filter uses no digital potentiometers

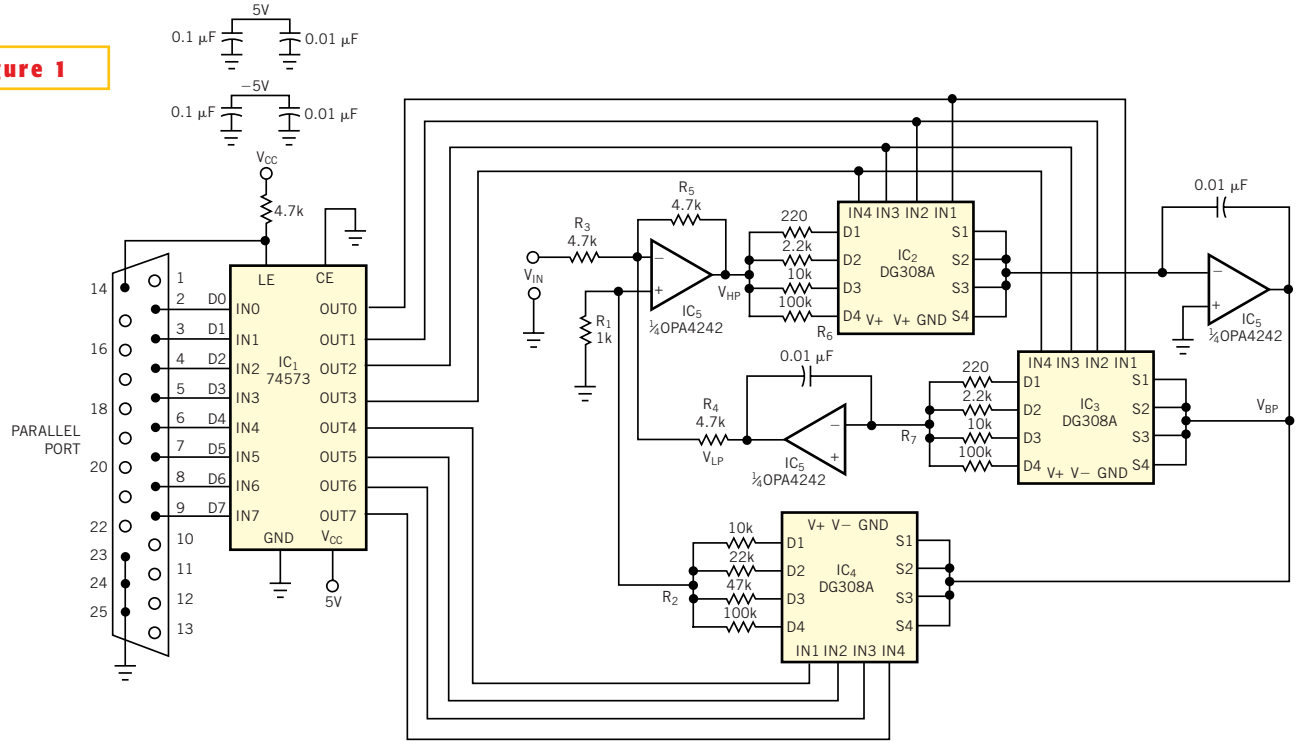
Saurav Gupta and Tejinder Singh, New Delhi, India

Modern instrumentation requires digital control signals. These signals come from a central microprocessor or, in modern context, the popular parallel or serial PC ports. In recent times, digital potentiometers have eliminated the hassles from this interface for the analog section. Designers can replace the resistors of the analog design with digital potentiometers, thus providing the necessary digital control. However, digital potentiometers suffer more severely from temperature-sensitive performance drifts than their manual counterparts, and they exhibit finite wiper-resistance effects. The design in **Figure 1** represents a multifunction, analog biquadrature design for automated mixed instrumentation. You can configure the design for both Q factor and center frequency via a PC's parallel port. The circuit requires no DACs or digital potentiometers. The circuit,

```
 Select Frequency(in Hz/sec)

        (1) 159          (6)  8110.0
        (2) 1591.5       (7)  30.68 K
        (3) 1750.7       (8)  32.20 K
        (4) 6366.0       (9)  37.00 K
        (5) 7957.0       (10) 38.70 K

Your Choice :6
Filter with Reconfigurable Characteristics

   Select Q (The Quality Factor)

        (1) 2.24         (9)  4.70
        (2) 2.50         (10)  5.36
        (3) 2.35         (11)  6.00
        (4) 2.65         (12)  6.38
        (5) 2.90         (13) 7.72
        (6) 3.12         (14) 11.01
        (7) 3.40         (15) 33.72
        (8) 3.72

Your Choice : 5
You Have Selected the Filter with
Frequency : 8110.00 Hz/sec
Quality Factor : 2.90
Bit Pattern : de (Hex),          1101 1110 (Binary)

Press
Enter : To Set the Switches
Esc   : To Exit

Chip Programmed Successfully!!
Press any key to exit
```

Figure 2 This user-friendly screen helps you configure the desired filter.

Figure 1



You can use a PC-configurable filter design to select both Q and center frequency.

based on a two-integrator configuration, provides simultaneous highpass, lowpass, and bandpass outputs.

By running simple code on the PC, you can choose from more than 150 programmable combinations of Q factor and center frequency (**Listing 1**). You can thus build a filter of desired parameters on the fly. The design uses quad analog switches DG308 from Maxim (www.maxim-ic.com) together with octal latches for programmability. A micropower precision op amp, OPA4242, from Burr-Brown (www.ti.com) makes up the analog-filter section. The software provides the data bits on ports pin 2 through 9, stored in the latch that controls the analog switches and, hence, selects the appropriate resistance combination to select the desired Q and f_0 values. The center frequency and Q values are: $f_0=[1/C_1C_2R_{P6}R_{P7}]^{1/2}$ and $Q=(1+R_{P2}/R_1)/3$, where R_{P2}, R_{P6}, and R_{P7} are PC-programmable resistances.

Data nibbles from port pins D2 through D5 provide ganged-switch settings for R_{P6} and R_{P7}, ensuring that they are always equal. Data nibbles correspon-

TABLE 1–DATA BITS FOR Q SELECTION

D9 (100k)	D8 (47k)	D7 (22k)	D6 (j10k)	Q
1	1	1	1	2.24
0	1	1	1	2.35
1	0	1	1	2.5
0	0	1	1	2.65
1	1	0	1	2.9
0	1	0	1	3.12
1	0	0	1	3.4
0	0	0	1	3.72
1	1	1	0	4.7
0	1	1	0	5.36
0	1	0	0	6
1	0	1	0	6.38
0	0	1	0	7.72
1	1	0	0	11.01
1	0	0	0	33.72

LISTING 1–C PROGRAM FOR PC-CONFIGURABLE FILTER

```
#include<dos.h>
#include<conio.h>
#include<stdio.h>
#include<process.h>
#define LPT 0x378       /* Data Port Address    */
#define CONT 0x37A      /* Control Port Address */
#define ESC 27
typedef unsigned char u08;
enum boolean {false,true};

/* Function Declarations */
void Chip_Program(u08);  /* To set the analog switches */
void showbits(u08);      /* To see bit pattern */
void DrLine(void);       /* Draw a Line */
void init(void);         /* Initializes the Parallel Port */

void main()
{
 int fch,ctr,qch;
 u08 pdat,tdat;
 float freq,qlty;
 init();
 do{
 clrscr();
 printf("RECONFIGURABLE UNIVERSAL FILTER  By Saurav Gupta & Tejinder Singh\n");
 DrLine();
 printf("   Select Frequency(in Hz/sec)\n");
 DrLine();
 printf("\t(1) 159 \t(6)  8110.0\n");
 printf("\t(2) 1591.5\t(7)  30.68 K\n");
 printf("\t(3) 1750.7\t(8)  32.20 K\n");
 printf("\t(4) 6366.0\t(9)  37.00 K\n");
 printf("\t(5) 7957.0\t(10) 38.70 K\n");
 DrLine();
 printf("Your Choice :");
 scanf("%d",&fch);
 }while(fch<1 || fch>10); /* Loop until a valid choice is entered*/

  switch(fch)
 {
  case 1 : freq=159; pdat=0x08; break;
  case 2 : freq=1591.5; pdat=0x04; break;
  case 3 : freq=1750.7; pdat=0x0C; break;
  case 4 : freq=6366; pdat=0x02; break;
  case 5 : freq=7957; pdat=0x06; break;
  case 6 : freq=8110; pdat=0x0E; break;
  case 7 : freq=30680; pdat=0x01; break;
  case 8 : freq=32200; pdat=0x05; break;
  case 9 : freq=37000; pdat=0x03; break;
  case 10: freq=38000; pdat=0x0F; break;
 }


 do{
 clrscr();
 printf("Filter with Reconfigurable Characteristics\n");
                                  C_code.txt
 DrLine();
 printf("   Select Q (The Quality Factor)\n");
 DrLine();
 printf("\t(1) 2.24\t(9)  4.70\n");
 printf("\t(2) 2.50\t(10)  5.36\n");
 printf("\t(3) 2.35\t(11)  6.00\n");
 printf("\t(4) 2.65\t(12)  6.38\n");
 printf("\t(5) 2.90\t(13) 7.72\n");
 printf("\t(6) 3.12\t(14) 11.01\n");
 printf("\t(7) 3.40\t(15) 33.72\n");
 printf("\t(8) 3.72\n");
 DrLine();
 printf("Your Choice :");
 scanf("%d",&qch);

 }while(qch<1 || qch>15);
  switch(qch)
 {
  case 1 : qlty=2.24; tdat=0xF0; break;
  case 2 : qlty=2.50; tdat=0xB0; break;
  case 3 : qlty=2.35; tdat=0x70; break;
  case 4 : qlty=2.65; tdat=0x30; break;
  case 5 : qlty=2.90; tdat=0xD0; break;
  case 6 : qlty=3.12; tdat=0x50; break;
  case 7 : qlty=3.40; tdat=0x90; break;
  case 8 : qlty=3.72; tdat=0x10; break;
  case 9 : qlty=4.70; tdat=0xE0; break;
  case 10: qlty=5.36; tdat=0x60; break;
  case 11: qlty=6.00; tdat=0x40; break;
  case 12: qlty=6.38; tdat=0xA0; break;
  case 13: qlty=7.72; tdat=0x20; break;
  case 14: qlty=11.01; tdat=0xC0; break;
  case 15: qlty=33.72; tdat=0x80; break;
 }
 pdat=pdat|tdat;
 printf("\nYou Have Selected the Filter with\n");
 printf("Frequency : %6.2f Hz/sec\nQuality Factor : %3.2f\n",freq,qlty);
 printf("Bit Pattern : ");
 showbits(pdat);
 printf("\n");
 DrLine();
 printf("\nPress \nEnter : To Set the Switches\nESC   : To Exit");
 if(getch()==ESC)
 exit(0);
 Chip_Program(pdat);
 printf("\n");
 DrLine();
 printf("Chip Programmed Successfully!!\nPress any key to exit");
 getch();
}

void DrLine(void)
{
 int ctr;
 for(ctr=0;ctr<50;ctr++)
  printf("%c",205);
  printf("\n");
}

void init(void)
{
 outport(CONT,0xFF);
 delay(100);
                                  C_code.txt
 outport(LPT,0x00);
 delay(100);
}

void Chip_Program(u08 pdat)
{
 outport(CONT,0x00);
 delay(200);
 outport(LPT,pdat);
 delay(200);
 outport(CONT,0xFF);
 delay(200);
}

void showbits(u08 num)
{
 int i,k,mask;
 printf("%x (Hex),\t\t",num);
 for(i=7;i>=0;i--)
 {
  if(i==3 || i==7 || i==11)
  printf(" ");
  mask=0x0001<<i;
  k=num & mask;
  k==0 ? printf("0"):printf("1");
 }
 printf(" (Binary)");

}
```

ding to pins D6 through D9 control the value of R_{P2}; hence, you use them for Q-value selection. For the given resistance values, **Table 1** shows the data bits for different values of Q (ranging from 2.24 to 33.72). **Table 2** shows the data bits for various center frequencies (159 Hz to 38.70 kHz). **Figure 2** shows the software front-end screen to make the selection. The design uses an 8.11-kHz filter with Q-factor 2.9 for demonstration and hardware validation. **Listing 1** gives the necessary back-end C code. The switches employed have a finite on-resistance, R_{DS}, of approximately 150Ω, which the design takes into account. For higher precision, you can use better switches having on-resistances of approximately 35Ω. Note that more switches provide a wider range from which to select. You can choose the resistances to suit the application's bandwidth range. You can download the filter software from the Web version of this Design Idea at www.edn.com.

TABLE 2–DATA BITS FOR CENTER-FREQUENCY SELECTION

D5	D4	D3	D2	f0 (kHz)
1	0	0	0	0.159
0	1	0	0	1.519
1	1	0	0	1.75
0	0	1	0	6.37
0	1	1	0	7.96
1	1	1	0	8.11
0	0	0	1	30.68
0	1	0	1	32.2
0	0	1	1	37
1	1	1	1	38.7

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Frequency source feeds entire lab

Mitchell Lee, Linear Technology Corp, Milpitas, CA

Plumbing a laboratory with a standard frequency makes a lot of sense if the lab uses multiple frequency counters, spectrum analyzers, and other frequency-dependent test equipment. Rather than spending time keeping all of the instruments' oscillators in calibration or buying expensive, high-precision oscillators, you can use the circuit in **Figure 1** to distribute a single calibrated frequency source to the external-reference input of each instrument. The circuit represents a simple, 10-MHz source and distribution amplifier. The output comes not from the emitter or collector of the Colpitts-oscillator transistor, Q_1, but rather from the current flowing in the 10-MHz crystal. The common-base stage, Q_2, converts this current into a voltage and establishes the correct dc level for the output amplifier, IC_1. This IC contains four gain-of-two buffers with 110-MHz, 3-dB bandwidth and can drive double-terminated 50 or 75Ω loads.

As **Figure 1** shows, the outputs use 75Ω impedance levels to take advantage of inexpensive F-type connector hardware and low-cost video coaxial cable. IC_1 also provides good isolation between its outputs, so that changes in loading on one output do not affect the other outputs. The circuit delivers more than 6 dBm to each termination. If high accuracy and low drift are critical needs, you can substitute Hewlett-Packard's (www.hp.com) HP10811A component oscillator for the Colpitts oscillator. Connect the HP10811A's output through a 510Ω resistor and a 10-nF coupling capacitor, directly to the emitter of Q_2. If you need more than four outputs, you can duplicate the IC_1 stage as many times as necessary.

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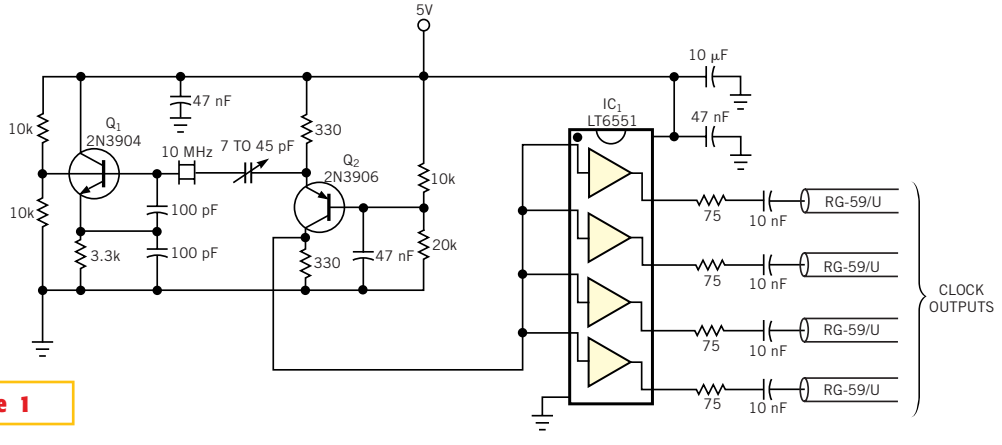


Figure 1

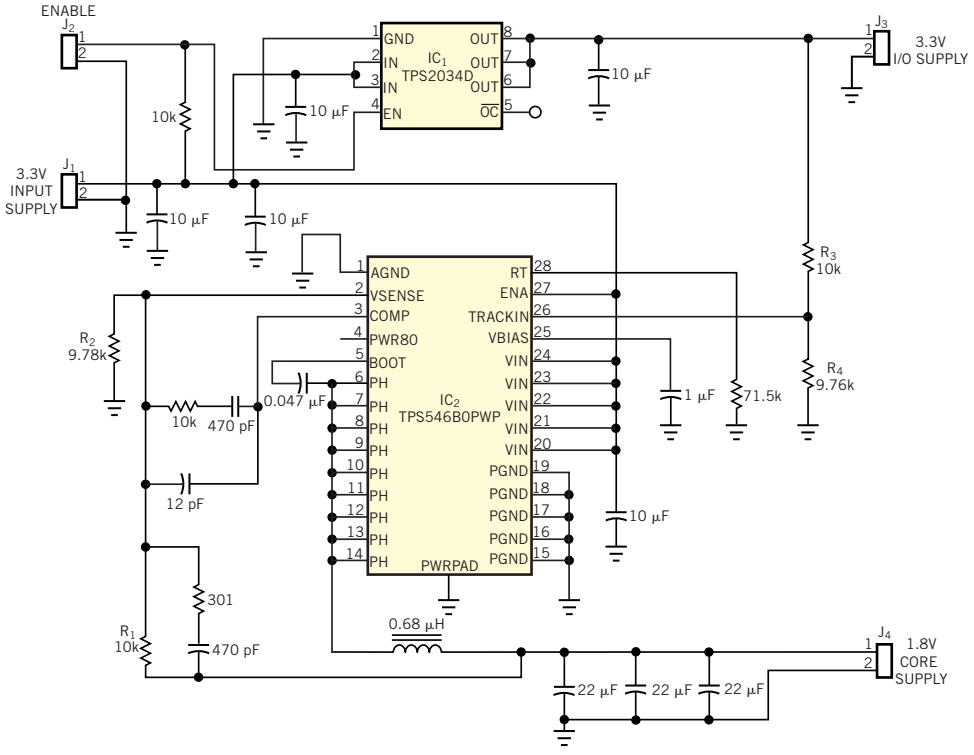
A laboratorywide distribution system is an alternative to multiple frequency sources.

Circuit sequences supplies for FPGAs

David Daniels, Texas Instruments, Dallas, TX

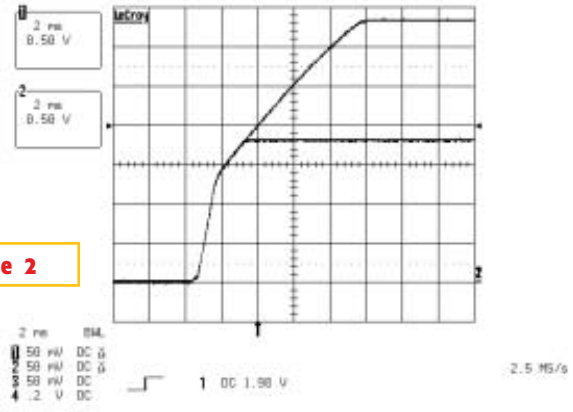
System designers must consider the timing and voltage differences between core and I/O power supplies (in other words, power-supply sequencing) during power-up and power-down. The possibility of a latch-up failure or excessive current draw exists when power-supply sequencing does not occur properly. The trigger for latch-up may occur if power supplies apply different potentials to the core and the I/O interfaces. FPGAs and other components with different sequencing requirements further complicate the power-system design. To eliminate the sequencing problem, you should min-

Figure 1



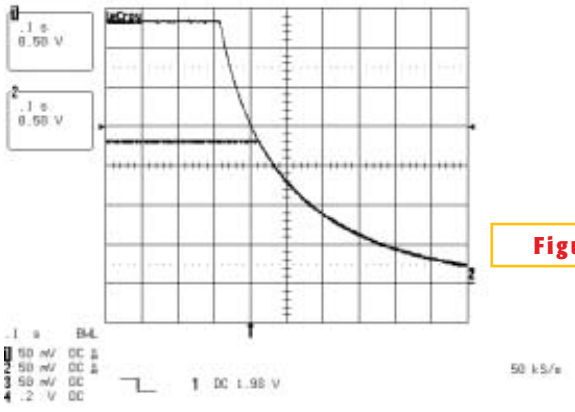
This power-supply-sequencing circuit eliminates latch-up problems and reduces FPGA start-up transient currents.

Figure 2



When the I/O-supply voltage decays, the core voltage gracefully follows suit.

Figure 3



As the I/O-supply voltage rises smoothly toward 3.3V, the core voltage clamps cleanly at 1.8V.

imize the voltage difference between the core and the I/O supplies during power-up and -down. The power supply in **Figure 1** regulates the 3.3V input voltage to the 1.8V core voltage and tracks the 3.3V I/O during power-up and -down to minimize the voltage differences between the supply rails.

The circuit in **Figure 1** comprises IC_1 and IC_2, a TPS2034 power switch and a TPS54680 step-down switching regulator, respectively. Component IC_1 is a high-side power switch that generates a slow ramp that IC_2 tracks during start-up. The ramp time of 6 msec minimizes the inrush currents to the bulk capacitors on the power-switch and supply outputs. The slow ramp minimizes the transient-current draw of the FPGA. The power switch ensures that the I/O voltage is not applied to the load before IC_2 has enough bias voltage to operate and generate the core voltage. Assuming that the input supply voltage is at 3.3V on J_1, floating the J_2 connector enables component IC_1. The I/O supply voltage, J_3, slowly rises until it reaches 3.3V. As the I/O voltage rises, the core voltage supply, J_4, rises accordingly until the voltage reaches 1.8V (**Figure 2**). The TPS54680 device incorporates an analog multiplexer on the TRACKIN pin to implement the tracking function.

During power-up and -down, when the voltage on the TRACKIN pin is lower than the internal reference of 0.891V, the voltage on the TRACKIN pin connects to the noninverting node of the error amplifier. When the TRACKIN pin is below 0.891V, the pin effectively functions as the switching regulator's reference. The resistor divider of R_3 and R_4 on the TRACKIN pin must equal the resistor divider of R_1 and R_2 in the feedback compensation to track with minimal voltage difference during power-up and -down. The TPS2034 has an on-resistance of 37 mΩ and can supply as much as 2A output current. The TPS54680 is a synchronous buck regulator that contains two 30-mΩ MOSFETs. Because the TPS54680 can source and sink as much as 6A load current at efficiencies greater than 90%, the output can track another power-supply rail during power-down. When the IC_1 device becomes disabled by shorting J_2 to ground, the I/O supply voltage decays, and the core supply voltage follows once the I/O voltage falls below the core voltage (**Figure 3**). Typically, Schottky diodes connect to the output of a dual power supply to clamp the voltage difference between the core and the I/O supplies during power-down, but most applications do not require the diodes with the power-supply circuit in **Figure 1**. Using this power-supply design reduces component count and increases reliability by eliminating the potential for latch-up and reducing FPGA start-up transient currents.

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design ideas

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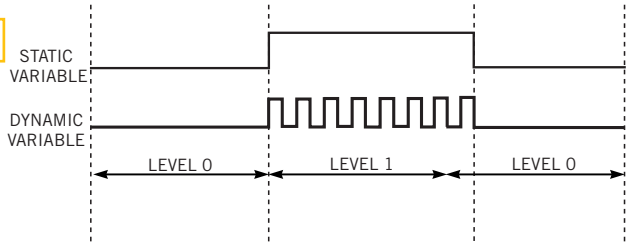
Oscillating output improves system security

Jorge Marcos and Ana Gómez, University of Vigo, Vigo, Spain

Many electronic-control systems have digital outputs that use transistors. One method of improving the security in these outputs is to use an oscillating signal to represent a logic-high state instead of a fixed voltage level (**Figure 1**). This type of signal, a *dynamic variable*, can drive the circuit shown in **Figure 2**. This circuit connects to the output transistor of the electronic-control system. The dynamic-variable signal connects to the output transistor, whose collector connects to a pulse transformer. If the system cannot produce pulses because of a fault, the relay deactivates. If a fault exists in the drive circuitry, the output system stays off. This solution guarantees the security function when one fault occurs. However, it does not guarantee the detection of all faults. However, you can use a DPDT relay and connect one of the contacts to one of the electronic-control inputs; thus, you can confirm the relay's activation or deactivation in the control program.

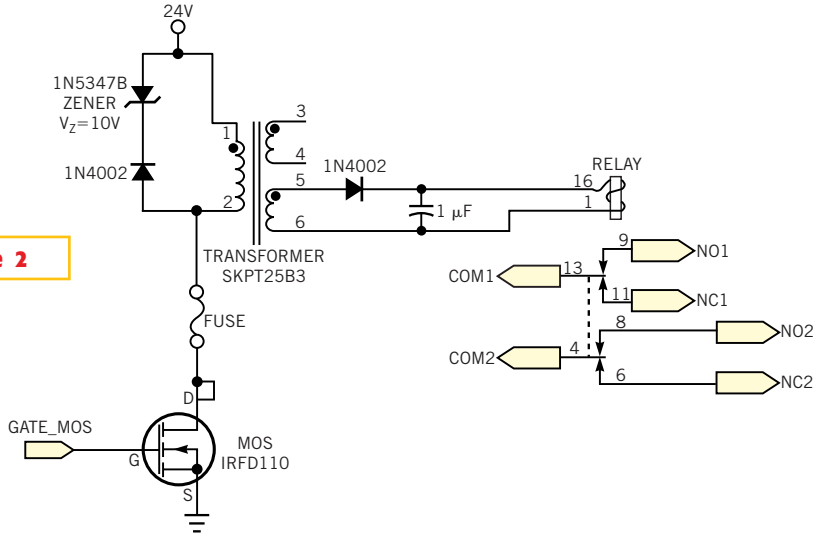
The circuit in **Figure 2** performs efficiently if the system can generate a frequency greater than 1 kHz to excite the pulse transformer. Many electronic systems that use an output transistor can generate a dynamic variable. Many systems, such as PLCs (programmable-logic controllers), have long cycle times and, thus, cannot generate signals of adequate frequencies. In these cases, you can obtain an appropriate signal using the low-frequency dynamic variable from the PLC. To accomplish that task, you must use an external oscillator and a pulse detector implemented with a monostable multivibrator. The oscillator produces a square-wave signal of a frequency that suits commercial pulse transformers. This signal drives the MOSFET when the pulse detector receives pulses from the PLC. Because the pulse detector can fail, you must duplicate the external circuit for redundancy. In this way, the final result is the same as that of **Figure 2**, except that the safe output comprises two relays.

Figure 1



You can improve the reliability of an electronic-control output by using an oscillating, instead of steady-state, signal to represent a logic-high state.

Figure 2



A "dynamic-variable" signal drives the output relay in this circuit.

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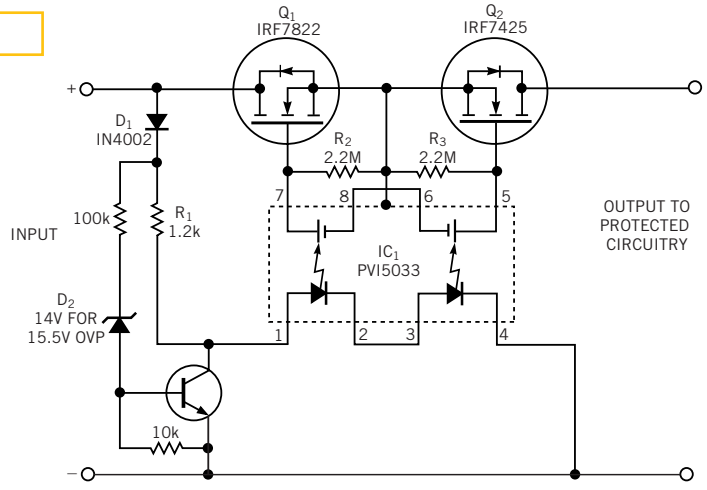
Polarity protector outperforms Schottky diodes

Mike Hovenga, BAE Systems, Austin, TX

THE POLARITY-PROTECTION circuit in **Figure 1** is a high-performance alternative to the usual series diode (often Schottky). The circuit incurs a much lower voltage drop than even the best Schottky diode. The circuit uses MOSFET devices because of their low on-resistance. For the transistors in this design, the combined on-resistance is 0.013Ω. With a 10A load, the voltage drop is 0.13V at 25°C. Compare this figure with forward-voltage drops of several hundred millivolts for Schottky diodes under the same conditions. You must use p- and n-channel transistors in series because of their intrinsic diodes. A photovoltaic isolator provides the appropriate gate drive to the MOSFETs. The performance is even better at lower currents. You can replace the two discrete transistors by a single-package, complementary-MOSFET pair, such as an IRF7389, which has a combined on-resistance of 0.108Ω. Resistors R_2 and R_3 are necessary to turn off the transistors when IC_1 turns off. R_1 provides a nominal 12V input.

Figure 1



This polarity-protection circuit incurs lower forward-voltage drop than the best Schottky diodes.

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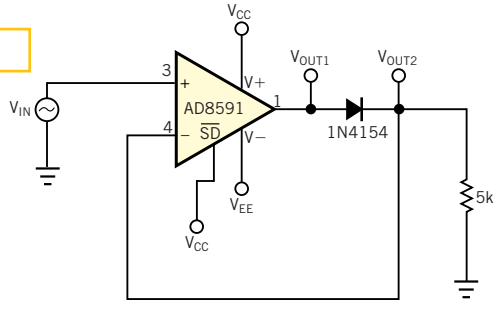
Circuit offers improved active rectification

Reza Moghimi, Analog Devices Inc, San Jose, CA

RECTIFIERS CONVERT ac signals to dc. You can combine a diode and a load resistor to create a half-wave rectifier, provided that the amplitude of the ac source is much larger than the forward drop of the diode (typically 0.6V). Unfortunately, you can't use this method to rectify signals that are smaller than a diode drop. For these applications, active rectifiers using amplifiers are available. The diode is inside the feedback loop of an amplifier (**Figure 1**). For V_{IN}>0V, the diode provides negative feedback, and the output, V_{OUT2}, follows the input (V_{OUT2}=V_{IN}). For V_{IN}<0V, the diode does not conduct, the amplifier is in an open-loop configuration, and V_{OUT2}~0V. **Figure 2** shows the response of the circuit in **Figure 1**. The output is shown in green; the input is shown in red.

Figure 1



This circuit is a typical half-wave-rectifier configuration.

If V_{IN}<0V, the amplifier behaves as a comparator. Its negative input is at a higher potential than its positive input, so its output, V_{OUT1}, saturates to V_{EE}. When the input again becomes positive, the amplifier has to recover from saturation and respond as quickly as its slew rate and saturation recovery time allow. This response takes some time, and the input may have changed by the time the amplifier is ready to respond to the positive input. The signals at V_{OUT1} (red) and V_{OUT2} (green) clarify this point (**Figure 3**). V_{OUT2} is the same waveform as

in **Figure 2**. Note the change in scale factor. V_{OUT1} is a diode drop higher for positive inputs and saturates to V_{EE} for negative inputs. The time delay in the response may result in a significant error in the output.

For example, an amplifier that has a slew rate of 2.5V/µsec and saturates to −2.5V takes at least 1 µsec to get ready to respond to positive inputs. During this time, the fast input has changed, so rectification starts at the wrong part of the input. One way to minimize this error is to use a high-slew-rate amplifier, but this solution comes at the expense of high power consumption. Another option is to use an inverting-amplifier configuration and two diodes, followed by a unity-gain inverting amplifier to obtain the noninverting rectification. This method appears in many textbooks. The circuit in **Figure 4** represents a one-stage, noninverting rectifier that improves the accuracy of the rectification and reduces the power consumption. In this circuit, an AD8561 amplifier acts as a comparator. The AD8591 performs the rectification.

When $V_{IN}>0V$, the output of the AD8561 is high, and the AD8591 acts as a follower. When $V_{IN}<0V$, the output of the AD8561 is low, and the AD8591 shuts down. This shutdown puts the output of the AD8591 into a high-impedance state, so it remains at approximately 0V, rather than saturating to V_{EE} as it did in the previous circuit. When V_{IN} goes positive, the amplifier comes out of shutdown and again follows the input. This turn-on time (the time it takes to come out of shutdown) is much shorter than the saturation recovery time and slew-rate limiting that occurs in the previous circuit. **Figure 5** shows the signals at the input (red) and output (green) of the improved rectifier circuit.

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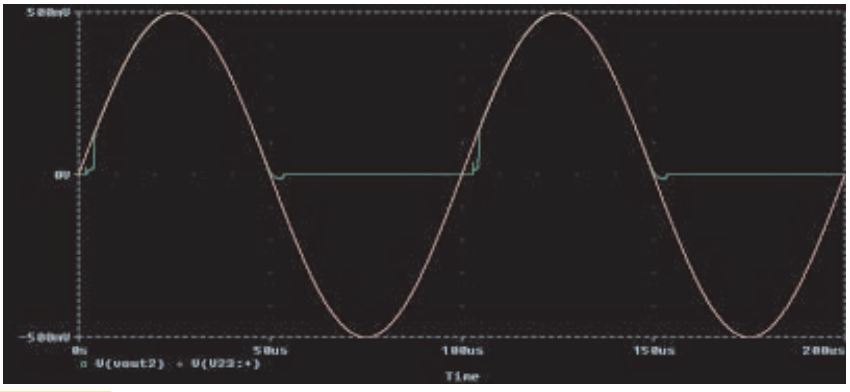


Figure 2 These signals appear at the input (red) and the output (green) of the circuit in Figure 1.

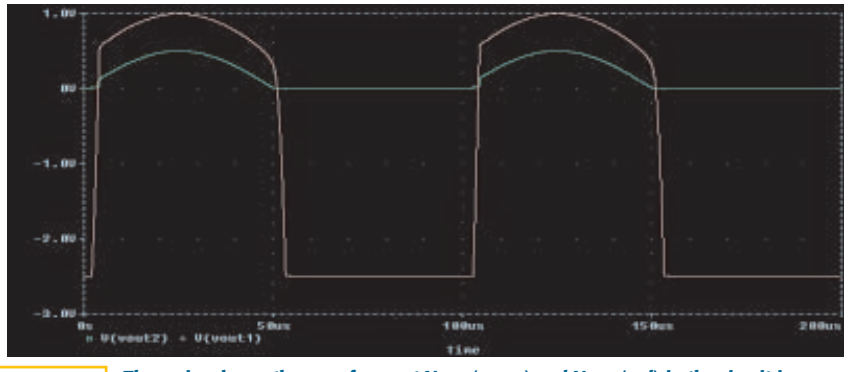


Figure 3 These signals are the waveforms at V_{OUT2} (green) and V_{OUT1} (red) in the circuit in Figure 1.

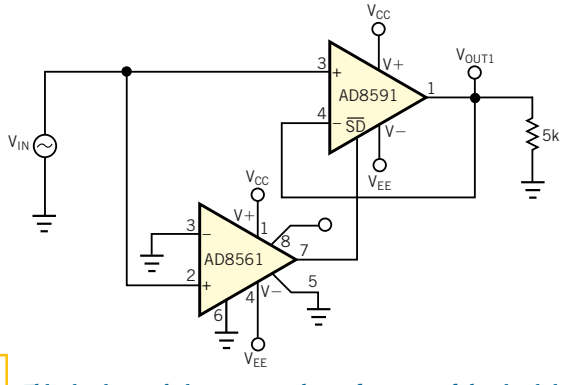


Figure 4 This circuit greatly improves on the performance of the circuit in Figure 1.

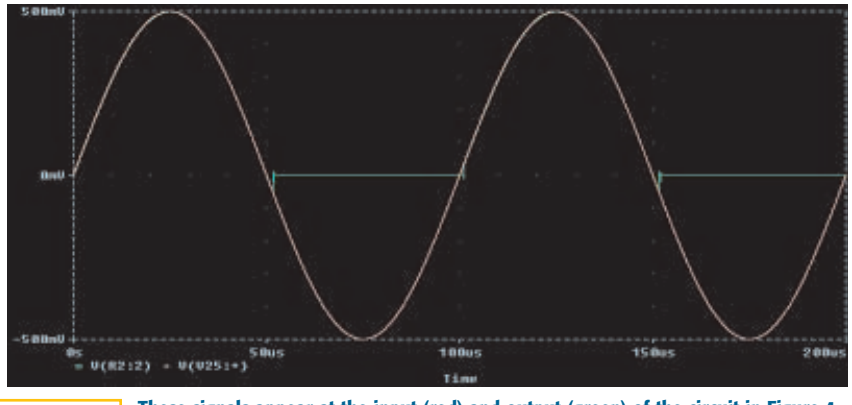


Figure 5 These signals appear at the input (red) and output (green) of the circuit in Figure 4.

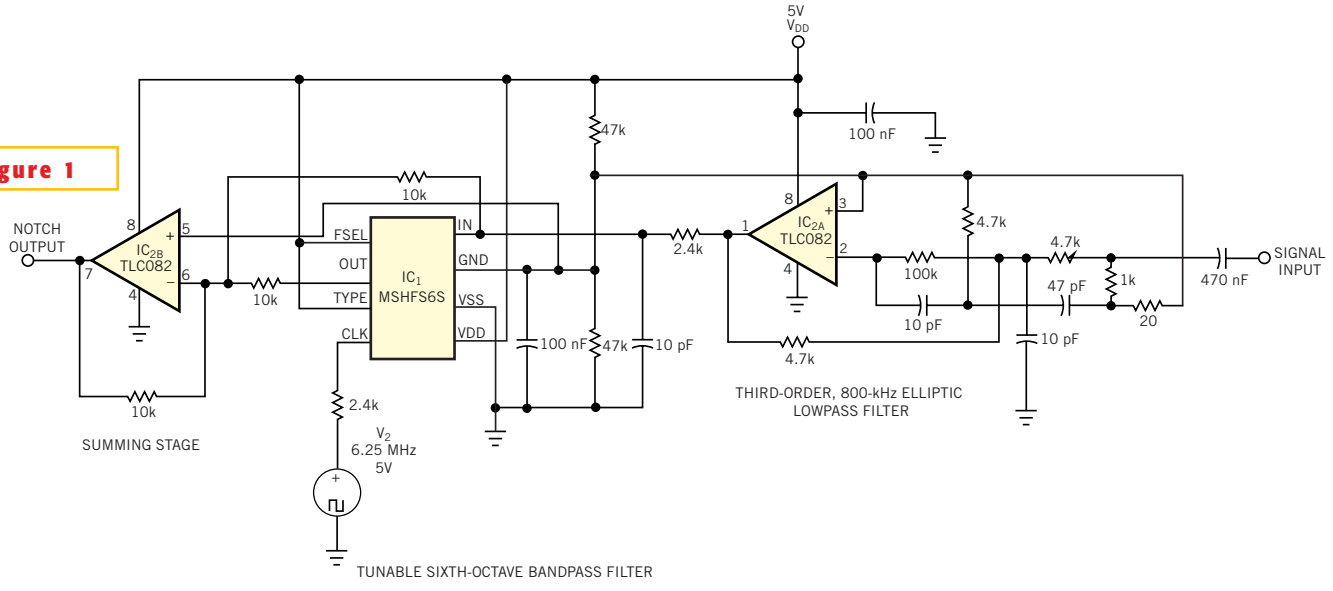
Build an adjustable high-frequency notch filter

John Ambrose, Mixed Signal Integration Corp, San Jose, CA

Although you can obtain universal, resistor-programmable switched-capacitor filters that are configurable as notch filters, most cannot operate at bandwidths higher than 100 kHz. Further, the typically 16- to 20-pin packages do not include a continuous-time, antialiasing filter to prevent spurious signals from appearing at the output. By using an eight-pin, dual operational amplifier and an eight-pin, switched-capacitor bandpass filter, you can construct a notch filter (**Figure 1**). IC_2, a TLC082 is a dual BiCMOS op amp, replacing the older JFET-input stage with lower noise CMOS but retaining the bipolar output for high drive capability. The gain-bandwidth product of the TLC082 is 10 MHz, allowing you to use it for filtering at frequencies as high as 1 MHz. The minimum ($V_{CC}-V_{EE}$) span with the TLC082 is 5V, unlike the older TL082, which required 6V. This supply span matches well with IC_1, an MSHFS6, with its 5V nominal operating voltage. Using half of the TLC082, you can construct a third-order, elliptic lowpass filter.

You set the passband ripple at approximately 5 dB to increase the out-of-band rejection. You set the continuous-time filter for 800 kHz, providing greater than 40 dB of rejection at 12.5 MHz. **Figure 2** shows the frequency response of the

Figure 1



An op amp and a switched-capacitor filter combine to form a highly selective notch filter.

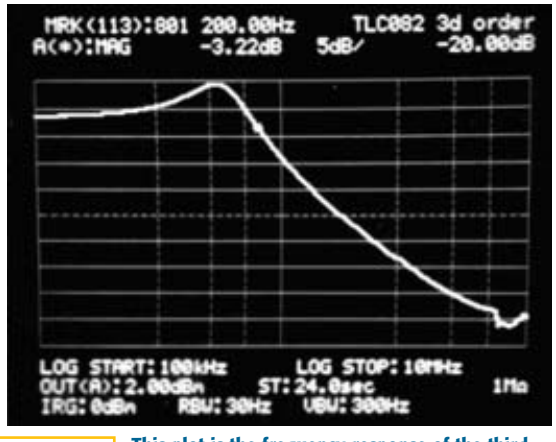


Figure 2 This plot is the frequency response of the third-order lowpass-filter stage.

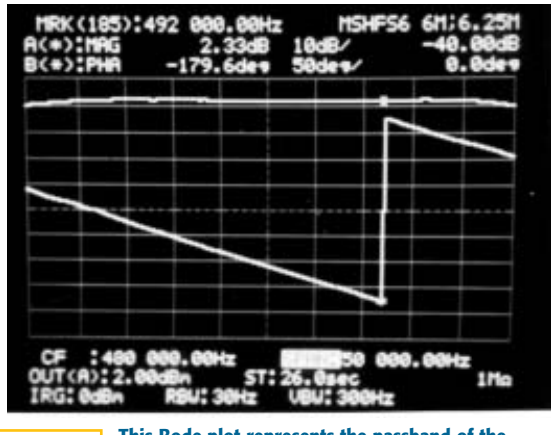


Figure 3 This Bode plot represents the passband of the MSHFS6 filter.

third-order lowpass filter using the TLC082. The MSHFS6 switched-capacitor selectable lowpass/bandpass filter with its 12.5-to-1 clock-to-corner ratio allows for distortion measurements to 6.25 times the notch center frequency before aliased signals cause measurement error. With the TLC082 lowpass filter set at 800 kHz, you can measure distortion products as high as the third harmonic. If the notch center frequency is always set lower than 260 kHz (MSFS6 clock at 3.3 MHz), then you can set the continuous-time lowpass filter corner to a lower frequency by adjusting the resistor and capacitor values. By summing the output of the bandpass filter with the input, cancellation of the input signal occurs at 180° phase shift in the passband. **Figure 3** shows the Bode plot of the passband of the MSHFS6 sixth-octave filter setting. The output of the other half of the TLC082 provides the notch-filter output. **Figure 4** shows the depth of the notch filter at −50 dB.

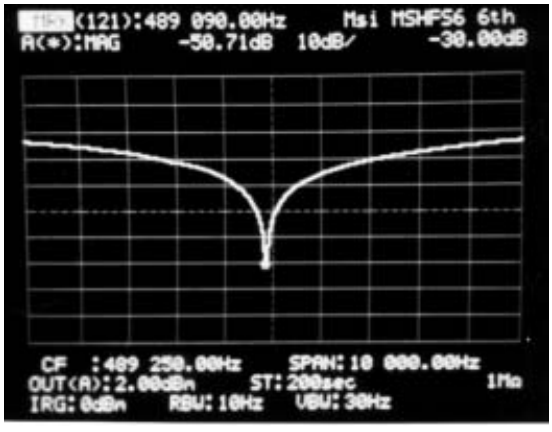


Figure 4 The circuit in Figure 1 delivers a −50-dB notch.

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Bootstrapping allows single-rail op amp to provide 0V output

Jim Williams, Linear Technology Corp, Milpitas, CA

Many single-supply-powered applications require amplifier-output swings within 1 mV—or even submillivolts—of ground. Amplifier-output-saturation limitations normally preclude such operation. **Figure 1**'s power-supply bootstrapping scheme achieves the desired characteristics with minimal parts count. IC_1, a chopper-stabilized amplifier, features a clock output. This output switches Q_1, providing drive to the diode-capacitor charge pump. The charge pump's output feeds IC_1's V− terminal, pulling it below 0V, thus permitting an output swing to and below ground. In **Figure 2**, the amplifier's V− pin (Trace B) initially rises at supply turn-on but heads negative when amplifier clocking commences at approximately midscreen. The circuit provides a simple way to obtain output swing to 0V, allowing a true "live-at-zero" output.

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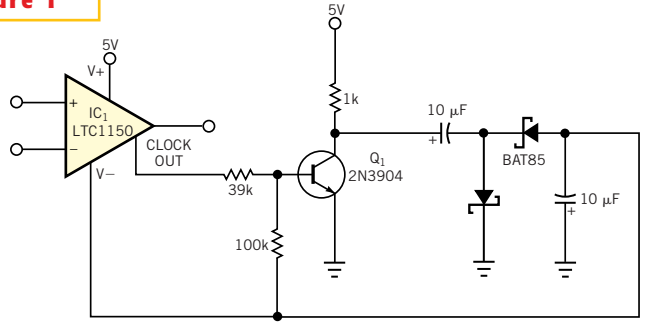
Figure 1



This configuration uses bootstrapping to allow a single-rail op amp to operate at 0V output.

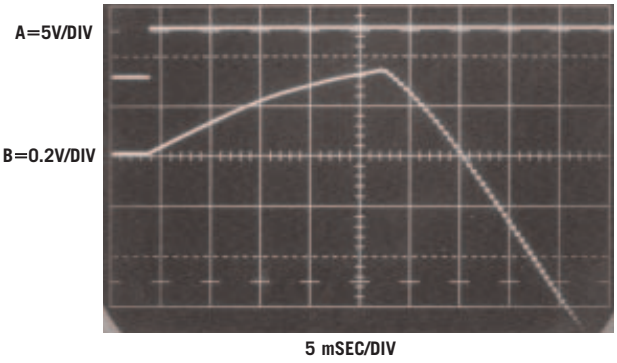


Figure 2 This start-up photo shows that the amplifier's V− pin (Trace B, midscreen) goes negative when the bootstrapping takes hold.

design ideas

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Build a precision deadband circuit

V Manoharan, Kochi, India

Deadband circuits find applications in servo-control systems. A precision current source and a half-wave inverting rectifier form a positive deadband circuit (**Figure 1**). The REF01, IC_1, is a precision 10V voltage reference. It forms a precision current source with the addition of a unity-gain buffer (IC_{2A}) and resistor R_1. IC_{2A} forces the ground pin (Pin 4) of IC_1 to assume the potential at IC_{2A}'s noninverting input. IC_1 forces its highly accurate reference voltage (10V) across R_1, so the current I_1 through R_1 is $10V/R_1$. Because the inverting input of IC_{2B} connects to the output of the current source, the feedback diode, D_1, becomes forward-biased with current I_1. The forward-biased diode keeps the output of IC_{2B} at approximately −0.6V. Because the cathode end of D_2 stays at virtual ground through R_3, D_2 remains reverse-biased. Hence, V_{OUT} remains at virtual ground (0V). Any positive voltage applied to V_{IN} further forward- and reverse-biases D_1 and D_2, respectively, and the output remains at 0V (deadband zone) for $V_{IN}>0V$.

Negative inputs tend to forward-bias D_2 and reverse-bias D_1. This bias situation occurs only when the current through R_2 (because of the negative V_{IN}) equals or exceeds $10V/R_1$. So, the output is 0V (deadband) until V_{IN} reaches a value equal to $-10R_2/R_1$. If you choose $R_1=20\,k\Omega$, V_{OUT} remains at 0V for $V_{IN}>(-5V)$; for $V_{IN}\leq(-5V)$, $V_{OUT}=(-V_{IN}-5V)$. **Figure 2** shows the transfer function for this scenario. C_1, C_2, and C_3 are decoupling capacitors for IC_1 and IC_2. R_4 reduces the offset voltage of IC_{2B} in the nondeadband region. You could realize an alternative straightforward circuit by prebiasing the inverting half-wave rectifier through a precision resistor connected to a voltage reference without using the unity-gain buffer, IC_{2A}. However, this alternative would increase the noise gain, thereby increasing the offset and noise at the output.

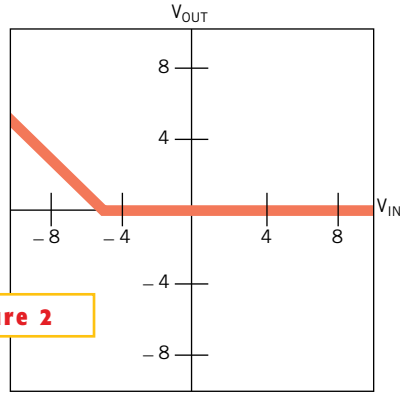

Figure 2

With $R_1=20\,k\Omega$, the circuit in Figure 1 is "dead" for input voltages higher than −5V.

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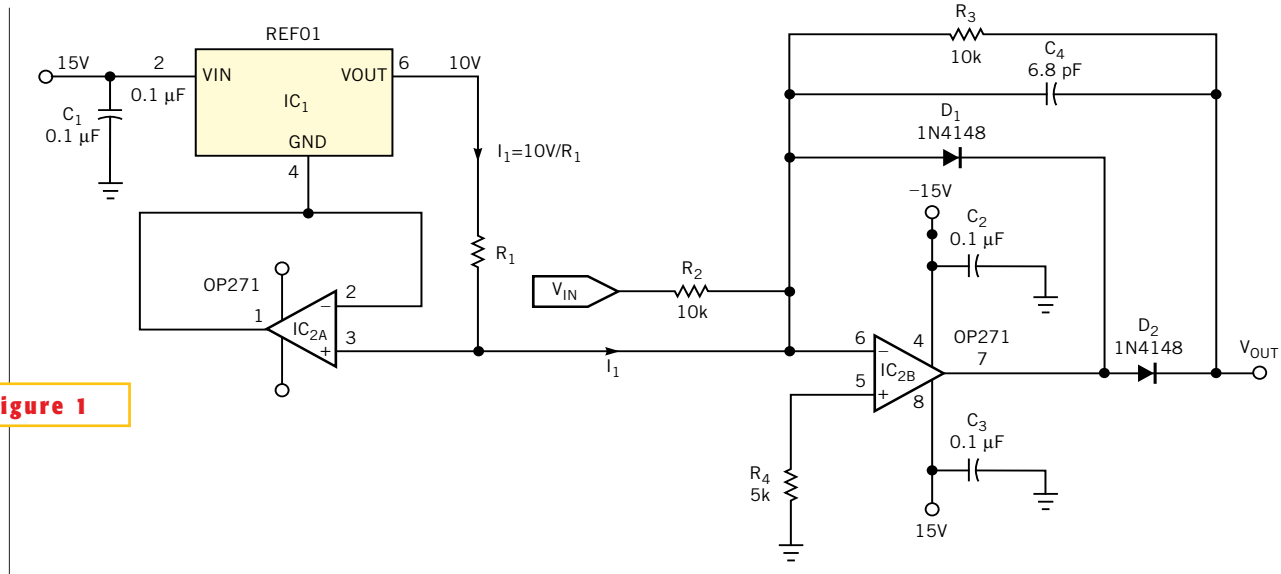


Figure 1

This circuit exhibits a deadband for signals more positive than an arbitrary voltage, which R_1 determines.

DDS and converter form signal generator

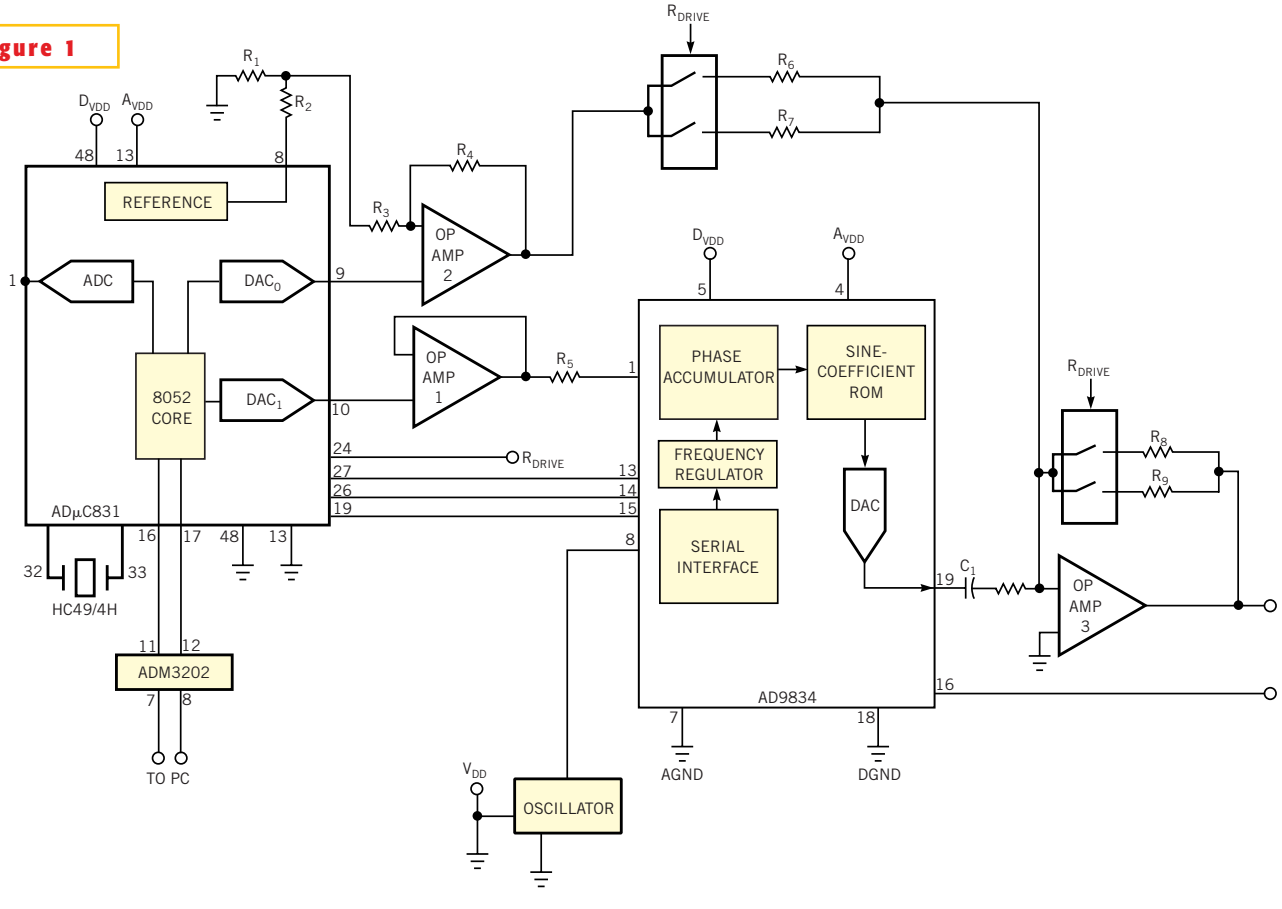
Colm Slattery, Analog Devices, Limerick, Ireland

Many applications require low-frequency signal generators that can deliver high-performance, high-resolution signals. This Design Idea presents a circuit that generates frequencies of 0 to 1 MHz. Sinusoidal, triangular, and square-wave outputs are available. You can achieve frequency resolution of better than 0.1 Hz and phase resolution of better than 0.1°; thus, you can program exact coherent frequencies. This feature is useful in digital modulation and frequency-tuning applications. The circuit uses the ADμC831 and AD9834 to generate the required frequencies (**Figure 1**). You can program the microcontroller from either a PC or a Unix-based workstation. You then program the AD9834 using a three-wire serial interface via the microcontroller. The interface word is 16 bits long.

You can program the AD9834 to provide sinusoidal, triangular, and square-wave outputs using the DDS (direct-digital-synthesis) architecture. The chip operates as an NCO (numerically controlled oscillator) using an on-chip, 28-bit phase accumulator, sine-coefficient ROM, and a 10-bit D/A converter. You typically consider sine waves in terms of their magnitude form, $A(t)=\sin(\omega t)$. The amplitude is nonlinear and is, therefore, difficult to generate. The angular information, on the other hand, is perfectly linear. That is, the phase angle rotates through a fixed angle for each unit in time. Knowing that the phase of a sine wave is linear, and, given a reference interval (clock period), you can determine the phase rotation for that period: $\Delta\text{Phase}=\omega\ dt$; $\omega=\Delta\text{Phase}/dt=2\pi f$, and $f=(\Delta\text{Phase}\times f_{MCLK})/(2\pi)$, where $dt=1/f_{MCLK}$, and f_{MCLK} is the master clock.

Using this formula, you can generate output frequencies, knowing the phase and master-clock frequency. The phase accumulator provides the 28-bit linear phase. The amplitude coefficients of the output sine wave are stored in digital format in the sine-coefficient ROM. The DAC converts the sine wave to the analog domain. If you bypass the ROM, the AD9834 delivers triangular waveforms instead of sinusoidal waveforms. A

Figure 1



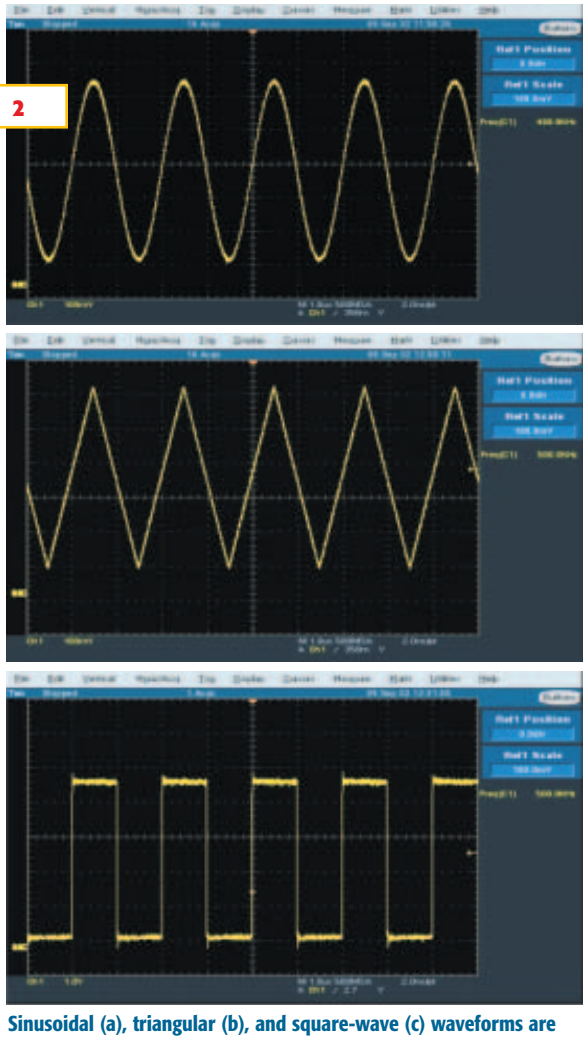
A DDS chip and a microcontroller combine to form a multiwaveform signal generator.

square-wave output is also available on the part. **Figure 2** shows the various waveforms available from the system. As shown in **Figure 1**, the sinusoidal/ triangular output waveforms are available on the IOUT pin (Pin 19); and the square wave output is available on the SIGN_BIT_OUT pin (Pin 16). You program the DDS by writing to the frequency registers. The analog output from the part is then: $f_{OUT}=f_{MCLK}/228\times$ (frequency-register word).

The outputs of the DDS have 28-bit resolution, so effective frequency steps on the order of 0.1 Hz are possible to a maximum of approximately 1 MHz. **Figure 2** shows the typical waveform outputs. Two phase registers are available that allow 12-bit phase resolution. These registers phase-shift the signal by: Phase shift $=2\pi/4096\times$(phase-register word).

A 50-MHz crystal oscillator provides the reference clock for the DDS. The output stage of the DDS is a current-output DAC loaded by an external resistor. A 200Ω resistor generates the required peak-to-peak voltage range. The output is ac-coupled through capacitor C_1. The MicroConverter contains two on-chip, 12-bit DACs. DAC_1 varies the current through R_5, adjusting the full-scale current of the DDS via the FSADJUST pin. The equation to control the full-scale current of the DDS DAC is: I_{OUT} (full-scale)$=18\times I\times R_5$.

Figure 2

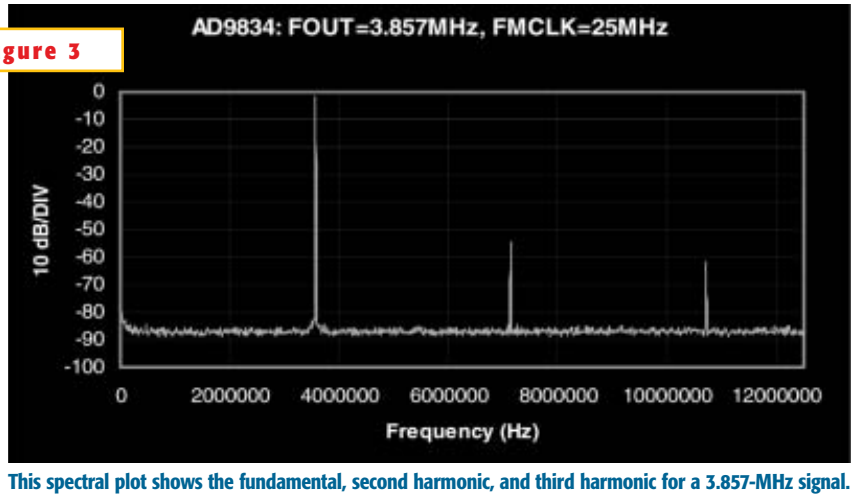


Sinusoidal (a), triangular (b), and square-wave (c) waveforms are all available from the circuit in Figure 1. The 500-kHz waveforms all use a 50-MHz sampling rate.

DAC_0, the internal reference of the MicroConverter, and op amp 2 allow for offset control of the output voltage of the DDS. You can program this dc offset to ±10 V at 10-bit resolution. When $R_1=R_2$ and the gain of op amp 2=8, then the output of op amp 2 is: $V_{OUT}=$ (DAC output$-(V_{REF}/2))\times 8$, yielding a ±10V range.

Resistors R_6 through R_9 allow for control of gain through op amp 3. The gain of the op amp is a function of resistor switching, which you enable using the R_{DRIVE} pin available on the MicroConverter. This operation allows for an effective programmable-output amplitude of approximately ±10V p-p. Thus, the circuit allows for programmable sinusoidal and triangular waves, including dc offsets, and the ability to set peak-to-peak amplitude of approximately ±10V. The square wave output on the SIGN_BIT_OUT pin has 0 to 5V amplitude. For low-frequency operation, a lowpass filter normally serves to filter reference-clock frequencies, spurs, and other images. For applications in which the output signal needs amplification, you should use a narrowband filter to filter out unwanted noise before the gain stage. A third-order filter would be good enough to remove most of the unwanted noise. **Figure 3** shows a typical spectral plot of the output. Applications for this circuit range from signal-waveform generation to digital modulation. You can use the system in frequency-sweeping and -scanning applications and in resonance applications that use the frequency as an excitation signal to determine circuit resonance. Another useful application is as a reference oscillator for a PLL system.

Figure 3



This spectral plot shows the fundamental, second harmonic, and third harmonic for a 3.857-MHz signal.

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48-input×16-output crosspoint IC eliminates the need for multiplexer amps

Mike Hess, Maxim Integrated Products, Sunnyvale, CA

Crosspoint switches are ideal for use in video-security systems, which accept multiple camera inputs while providing playback and multiple loop-through to multiple monitors. To provide video loop-through or monitor outputs, these systems often require additional multiplexer amplifiers that can drive standard video loads. Thus, one or more external multiplexer amps often follow a crosspoint-matrix switch. As an alternative, you can employ a 32×16 nonblocking crosspoint-matrix switch, whose 16 2-to-1 multiplexers eliminate the need for extra multiplexer amps (**Figure 1**). The internal 2-to-1 multiplexers appear before the video-output buffers, which can each directly drive a standard video load. That configuration eliminates the need for external multiplexer amps and their associated cost, space requirement, and power consumption.

The MAX4358 IC is a fully buffered, 32-input×16-output nonblocking crosspoint switch that includes 16 additional buffered analog-video inputs (OSDFILL) intended for the insertion of OSD (on-screen-display) information. ("Nonblocking" means that the IC can route any input to any output.) The 16 fully buffered OSDFILL analog inputs are identical to the 32 inputs of the buffered crosspoint-switch matrix, so the 16 additional video inputs can implement a single-chip, 48-input×16-output crosspoint-switch matrix. The output buffers feature programmable gain (A_V=1V/V or 2V/V). The programmability allows versatility in routing short video traces or driving video-transmission lines. Operating from dual ±3 to ±5V supplies or a single 5V supply, the device reduces power consumption by as much as 60% versus standard ±5V-only ICs.

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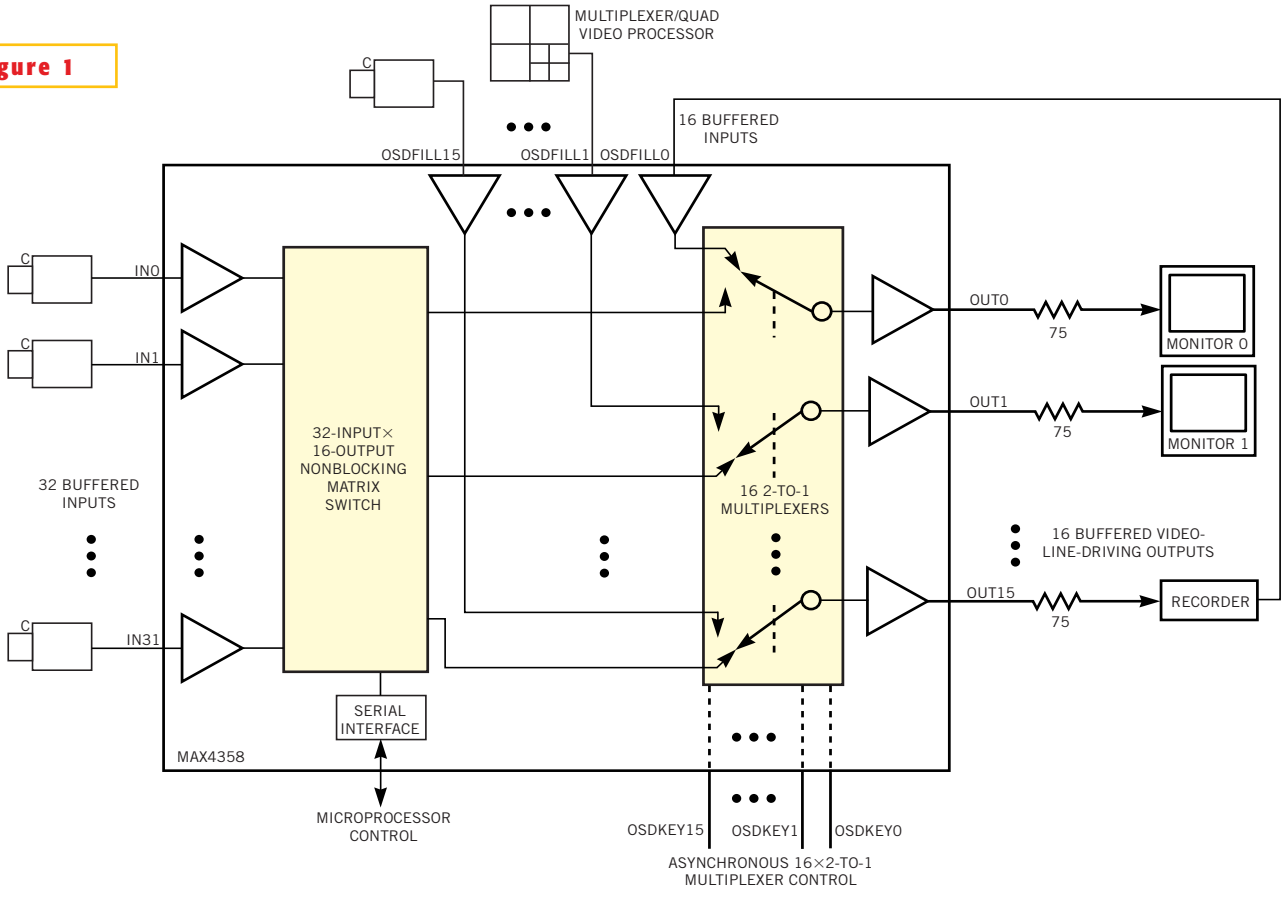
Figure 1



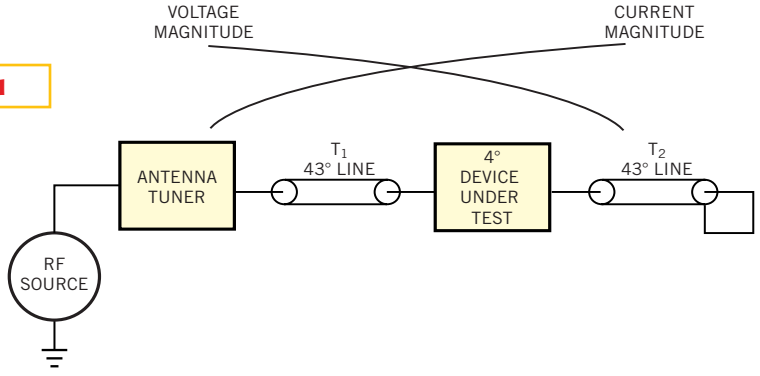
Internal buffers allow this IC to implement a 48-input×16-output matrix switch without the need for external multiplexer amps.

Transmission line tests 1-kW device using only 100W

David Cuthbert, Meridian, ID

A 13.56-MHz, ISM (industrial, scientific, and medical)-band RF-measurement device had the test requirement of a 50-hour, 1-kW burn-in. The device under test needed to be simultaneously stressed at an RF potential and RF current equivalent to 1 kW, but the only spare RF source at hand was a 100W RF generator. Besides, saving energy seemed important. The circuit in **Figure 1** develops 1 kW from the 100W RF source by storing energy in a transmission line. The circuit comprises two 43° sections (approximately 6 feet) of RG-213 coaxial cable with UHF connectors at each end. The device under test, which has an electrical length of 4°, connects between the two lines, T_1 and T_2, making the total line length 90°. An off-the-shelf amateur-radio antenna tuner matches the 50Ω RF generator to the line's input impedance.

Figure 1



As if by magic, this setup allows you to apply 1 kW to a device using only a 100W generator.

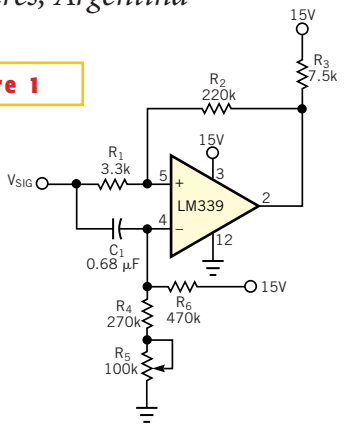
Circuit operation is simple. The RF energy connects to the line's input through the antenna tuner. The energy travels to the shorted end of the line, where it is reflected and travels back to the input. The reflected energy then reflects off the conjugate match, which the antenna tuner provides, and combines with the next

Filter allows comparison of noisy signals

Mario Milberg, CNEA, Buenos Aires, Argentina

When you need to compare the dc level of a noisy signal with a reference for further processing, the output of the comparator changes in a chaotic way when the dc level approaches that of the reference. You have a choice of two classic solutions to this problem: One is to add hysteresis to the comparator, but, if the noise level is high, the hysteresis must be correspondingly high. In this situation, you face a wide dead-band zone around the comparison trip point. The second solution is to add lowpass filtering to the noisy signal. This approach increases the response time, slowing down the system. This Design Idea proposes a third solution that avoids the cited drawbacks. In the circuit in **Figure 1**, the noise adds to the reference through a highpass filter, so the comparator's inputs see only the difference between the two dc levels: $V^+=V_{DCSIG}+V_{NOISE}+V_{HYS}$, $V^-=V_{DCREF}+V_{NOISE}$, and $V^+-V^-=V_{DCSIG}-V_{CREF}+V_{HYS}$, where V^+ is the voltage on the comparator's positive input, V^- is the voltage on the negative input, V_{NOISE} is the noise riding on the signal, and V_{HYS} is the hysteresis accruing from the positive feedback to the positive input.

Figure 1



By presenting the noise signal to both inputs of the comparator, this circuit can compare the dc levels of the signal and the reference.

C_1, R_4, R_5, and R_6 form the highpass filter, whose cutoff frequency is $f_C=1/[2\pi C_1(R_4+R_5)||R_6]$. The cutoff frequency should be lower than the lowest frequency of the noise band. R_1 and R_2 establish the still-needed small amount of hysteresis. R_3 is a pullup resistor for the open-collector output of the comparator. The comparator circuit worked successfully in a system that processes the fluctuating current generated by an ionization chamber in a neutron-flux measurement system.

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half-cycle of input energy to flow toward the short again. This process continues with the stored energy continuing to build until the circuit losses equal the generator power. Considering the circuit operation in terms of impedances reminds you that the input impedance of a shorted, lossless, 90° transmission line is infinite. At the shorted end of the line, V/I is zero, and, at the input of the line, V/I is infinite. At the center, where the device under test is located, the magnitude of V/I is equal to the characteristic impedance of the transmission line—50Ω in this case. The RF voltage and current are 90° out of phase, but that fact does not affect the burn-in of the device.

Consider how much line input power is required to develop 1 kW at the device under test. The loss of each 6-foot section of RG-213 is 0.025 dB, and the device-under-test loss is 0.05 dB. The loss for a wave traveling down the line is therefore 0.1 dB. The return loss, R_L, is twice this amount, or 0.2 dB, because the wave must travel down the line to the short circuit and return to the source. Now, you can calculate the reflected power, P_R, for an incident power, P_{IN}, of 1000W using the following formula: $P_R=(P_{IN})10^{(RL/10)}=(1000)10^{(-0.2/10)}=955W$.

So, when 1000W flows down the line, 955W returns to the input. The line input power required is equal to the incident power minus the reflected power, which is 1000−955, or 45W. Because the line loss and device-under-test loss are both 0.05 dB, half of the 45W loss is dissipated in the coax, and half is dissipated in the device under test. The measured antenna-tuner loss is 40W, which makes the total circuit loss 85W. You can determine the line's input impedance by calculating the line-input complex reflection coefficient (Γ) and solving for the input impedance using $\Gamma=10^{(RL/20)}=10^{(-0.2/20)}=0.9772$, and

$$Z_{IN}=\frac{Z_{LINE}(\Gamma+1)}{1-\Gamma}=\frac{50(0.9772+1)}{1-0.9772}\approx 4.3\ k\Omega.$$

The antenna tuner must match the 50Ω generator's output impedance to the 4.3-kΩ line-input impedance. You can confirm the circuit's operation by measuring the amplitude and phase of the device's voltage and current. The measurement uses an oscilloscope with voltage and current probes. A power meter at the device under test measures forward and reflected power of 1 kW. Because of the high circuit Q, you'll find that adjusting the RF-source frequency to obtain circuit resonance is easier than trimming cable lengths to obtain circuit resonance. The primary limiting factors with this circuit are the temperature rise of the coaxial cable and the losses incurred in the impedance-matching circuit. Coax having lower loss allows you to achieve a higher "power multiplication" and higher device-under-test power.

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design ideas

Edited by Bill Travis

Key-reading circuit saves I/O pins

Gustavo Santaolalla, Digital Precision Systems, Buenos Aires, Argentina

Some microcontroller applications usually use too many I/O pins to read keys or onboard switches; in many cases, few pins remain available for other uses. Some alternative ways to read keys yield more free pins. First, consider some ways to effect key reading. **Table 1** presents a comparison of four methods with references to circuit configurations (**figures 1**, **2**, **3**, and **4**). As you can see, the best choice for reading many keys is to use the A/D converter that is inherent in many microcontrollers. This option needs many lines of code and is not amenable to resistive buttons, such as flexible key pads (**Reference 1**). Another option is to read one key with one I/O port, but it needs as many pins as the keys to read.

Figure 4 shows another possibility, the subject of this Design Idea. In this configuration, the microcontroller reads six keys with only three lines of I/O pins. This method entails the use of a few external components. The idea is to turn one of the three lines into output, set it at logic 1, and use the other two lines as inputs. Then, the microcontroller scans each input for a logic 1, and, if it finds it, a key press has occurred. If not, it turns the next line into an output, sets it, and turns the other two into inputs, and so on. In this way, you can confirm each time a key press takes place. R_4, R_5, and R_6 are current-limiting resistors, and R_1, R_2, and R_3 are simple pull-down resistors. The circuit uses three LEDs for debugging.

Listing 1 shows the complete program. An MC68HC908JK3 tested the software, but the routine is probably applicable to other microcontrollers. The program has no debounce function; you

(continued on pg 120)

TABLE 1—VARIOUS KEY-READING SCHEMES

	No. of keys	No. of pins	Notes
Figure 1	N	No. of pins	16 pins=16 keys
Figure 2	N	N/8	With ADC, 16 keys=two pins
Figure 3	$N_{IN}XN_{OUT}$	NIN+NOUT	16 keys=eight pins (four inputs and four outputs)
Figure 4	N	N	16 keys=five pins (four more keys available)

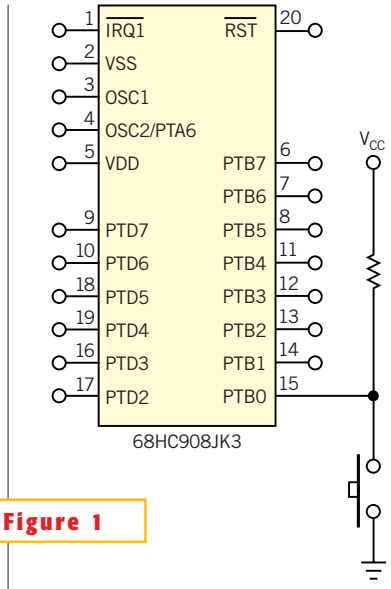


Figure 1

In this simple configuration, you need as many I/O pins as you have keys.

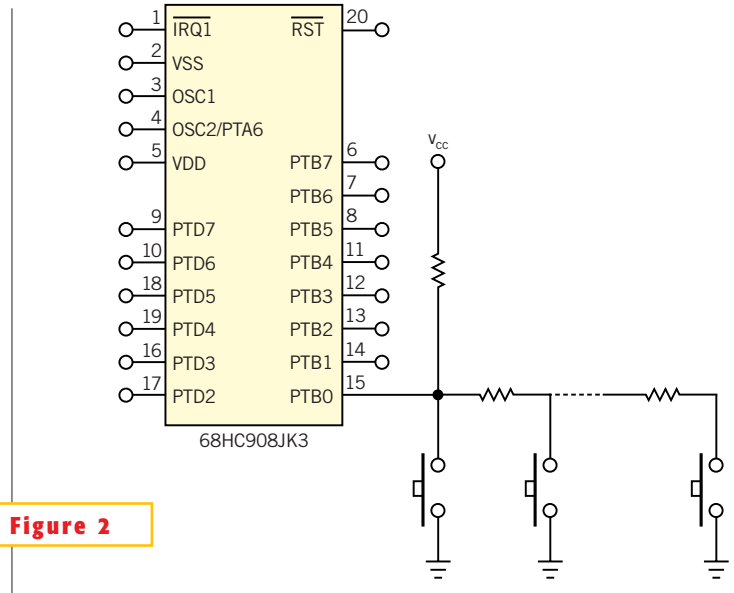
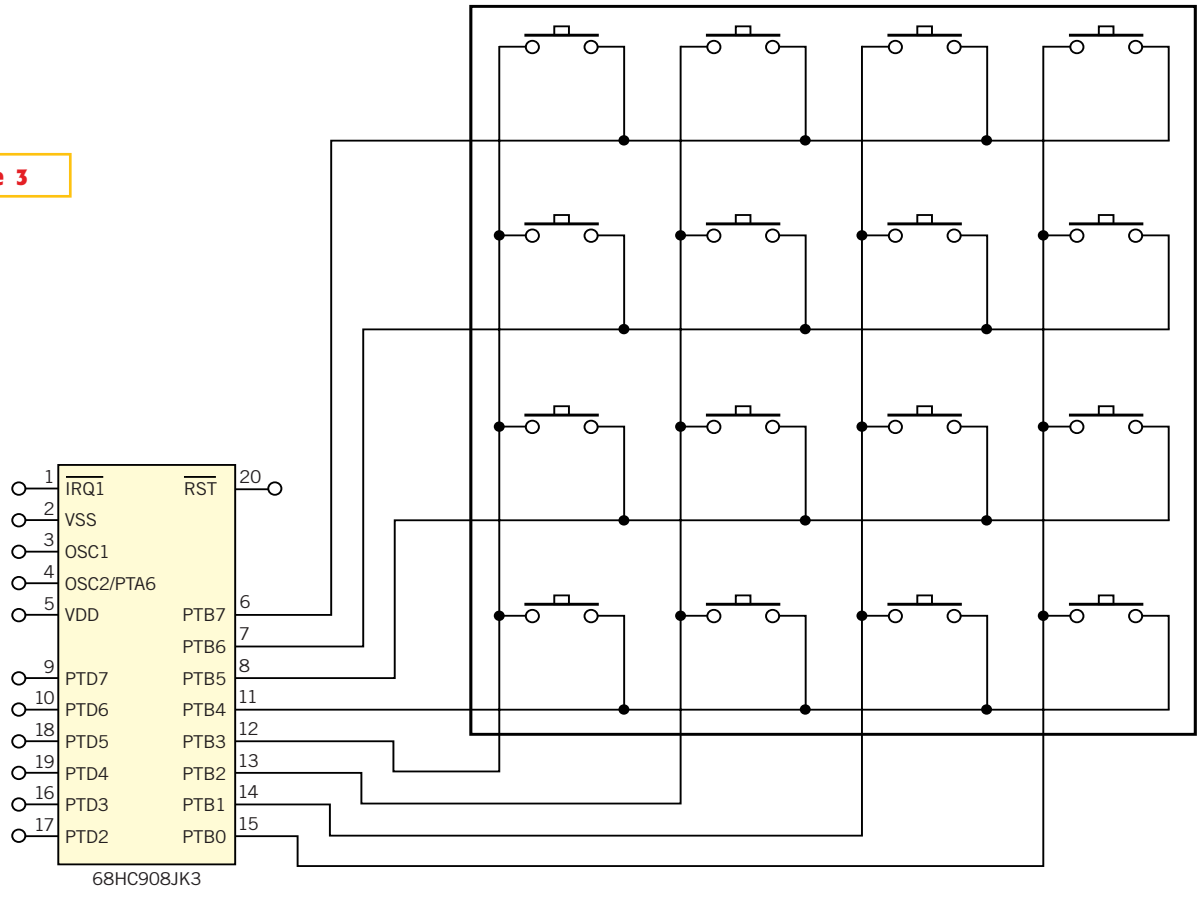


Figure 2

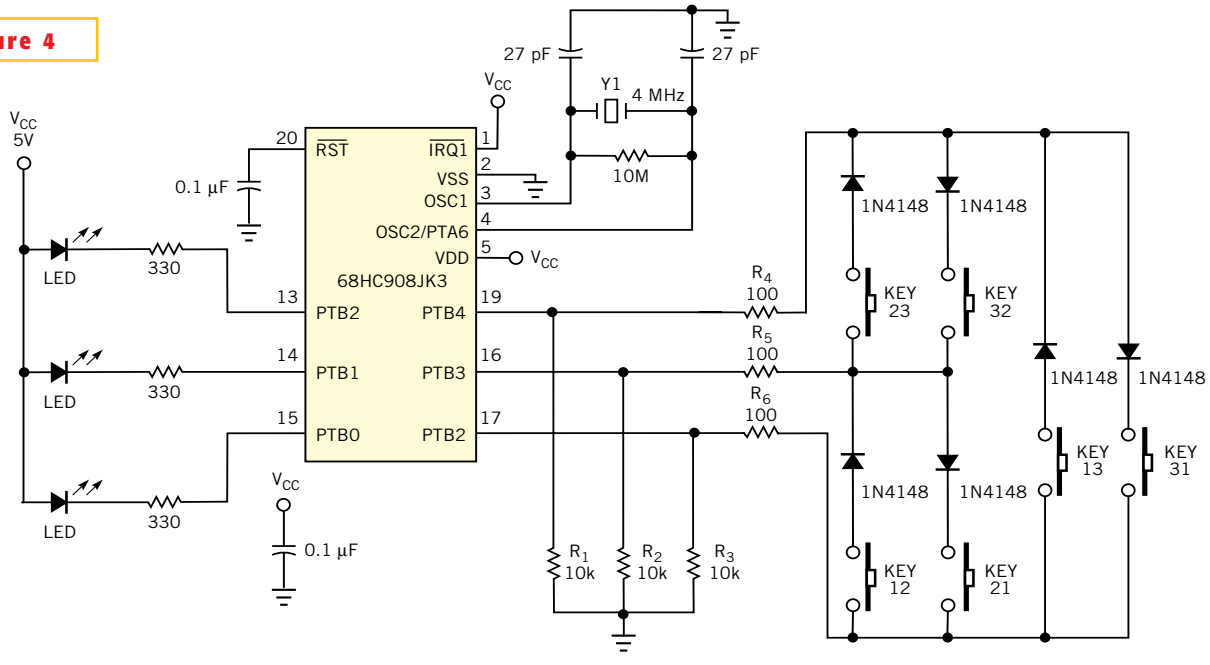
Using the microcontroller's internal ADC, you need only two I/O pins to control 16 keys.

Figure 3



In a matrix configuration, you need eight I/O pins to control 16 keys.

Figure 4



With an expansion of this scheme, five I/O lines control 16 keys with room to add four more keys.

(continued on pg 117)

can add it for a real application. The program shows the variable KeyVal on three LEDs. You can probably write more efficient code that that of **Listing 1**; the code shown is just for testing. **Table 1** shows how many pins you need to read 16 keys. As you can see, with the circuit in **Figure 4**, you need only five pins, but you can add four more keys. You can download **Listing 1** from the Web version of this Design Idea at www.edn.com.

REFERENCE

1. Motorola application note AN1775, www.motorola.com.

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LISTING 1—PROGRAM TO READ SIX KEYS AND DISPLAY RESULTS ON SIX LEDs

```
;*****************************************************************
; Botones.asm
; This program reads 6 keys and shows their value on six leds
; v1r0 220802 for D.I.
; Assembler: CASM08W from P&E Microcomputers Systems
; Target: HC908JK3
;*****************************************************************

;*****************************************************************
; EQUS
;*****************************************************************

PTA   EQU $0000   ; Ports and data direction
PTB   EQU $0001
PTD   EQU $0003
DDRA  EQU $0004
DDRB  EQU $0005
DDRD  EQU $0007

CONFIG1 EQU $001F  ; System configuration register
CONFIG2 EQU $001E  ; System configuration register

;equs PORT D:
k1      equ   2
k2      equ   3
k3      equ   4

;equs PORT D:
PKey    equ   PTD

;equs DATA DIRECTION PORT D:
DPKey   equ   DDRD

;Keys values
Key12   equ   1
Key13   equ   2
Key21   equ   3
Key23   equ   4
Key31   equ   5
Key32   equ   6

FlashBegin  equ  $EC00
RamBegin    equ  $0080

;Reserva de variables

        ORG   RamBegin
RamDeg  equ   *
KeyVal  rmb   1          ;key value
Last_Var equ  *

        ORG   FlashBegin

;*****************************************************************
; RESET
;*****************************************************************
Reset   equ   *
        jsr   Init_Hard      ;init ports
        jsr   Init_Soft      ;init soft
        cli

;*****************************************************************
; MAIN PROGRAM
;*****************************************************************
Main    equ   *
        jsr   ReadKeyPad     ;read keys
        tsta
        beq   Main           ;no key pressed
        sta   PTB            ;show KeyVal - just for debug
        jmp   Main

ReadKeyPad  equ  *
        clr   KeyVal
        bset  k1,DPKey       ;k1 output
        bclr  k2,DPKey       ;k2 input
        bclr  k3,DPKey       ;k3 input
        bset  k1,PKey        ;k1 = 1
        brclr k2,PKey,NOK12  ;k2 pressed ?
        bset  k2,PKey,*      ;yes, wait for unpressed
        lda   #Key12         ;accA = Key12
        bra   ENDRKP         ;return
NOK12   brclr k3,PKey,NOK13  ;k3, pressed ?
        bset  k3,PKey,*      ;yes, wait for unpressed
        lda   #Key13         ;accA = Key13
        bra   ENDRKP         ;return

NOK13   bclr  k1,DPKey       ;k1 input
        bset  k2,DPKey       ;k2 output
        bclr  k3,DPKey       ;k3 input
        bset  k2,PKey        ;k2 = 1
        brclr k1,PKey,NOK21  ;k1 pressed ?
        bset  k1,PKey,*      ;yes, wait for unpressed
        lda   #Key21         ;accA = Key21
        bra   ENDRKP         ;return
NOK21   brclr k3,PKey,NOK23  ;k3, pressed ?
        bset  k3,PKey,*      ;yes, wait for unpressed
        lda   #Key23         ;accA = Key23
        bra   ENDRKP         ;return

NOK23   bclr  k1,DPKey       ;k1 input
        bclr  k2,DPKey       ;k2 input
        bset  k3,DPKey       ;k3 output
        bset  k3,PKey        ;k3 = 1
        brclr k1,PKey,NOK31  ;k1 pressed ?
        bset  k1,PKey,*      ;yes, wait for unpressed
        lda   #Key31         ;accA = Key31
        bra   ENDRKP         ;return
NOK31   brclr k2,PKey,NOK32  ;k2, pressed ?
        bset  k2,PKey,*      ;yes, wait for unpressed
        lda   #Key32         ;accA = Key32
        bra   ENDRKP         ;return

NOK32   equ   $
ENDRKP  rts

Init_Hard   equ   $          ;1 -> output  / 0 -> input
        lda   #%11111111     ;as output
        sta   DDRA
        lda   #%11111111     ;as output
        sta   DDRB
        sta   PTB
        lda   #%11100011     ; k1,k2,k3 as inputs
        sta   DDRD
        rts

Init_Soft   equ   $
        lda   #%00000001
        sta   CONFIG1        ;cop disabled
        rts

not_used    rti

;*****************************************************************
; VECTORS
;*****************************************************************
        org   $FFDE
        fdb   not_used       ;adc conversion complete
        fdb   not_used       ;keyboard

        org   $FFF2
        fdb   not_used       ;tim overflow
        fdb   not_used       ;tim channel 1
        fdb   not_used       ;tim channel 0
        fdb   not_used       ;not used
        fdb   not_used       ;irq
        fdb   not_used       ;swi
        fdb   Reset
```

Synchronous buck circuit produces negative voltage

John Betten, Texas Instruments, Dallas, TX

MANY ELECTRONIC SYSTEMS require both positive and negative voltages to operate properly. Generating an efficient, low-voltage positive output from a higher voltage input typically entails the use of a synchronous buck regulator. But when generating a negative output voltage from a positive input voltage, you'd typically use a flyback topology, especially at higher output currents. The operation and control characteristics of a synchronous buck and a negative flyback (also called a buck-boost) differ significantly. **Figure 1** shows the basic components that a negative flyback circuit requires. When FET Q_1 turns on, the input voltage appears across inductor L_1 with no input current going to the load at this point. All the output current delivered to the load at this time comes from output capacitor C_1, because diode D_1 is reverse-biased. The current in the inductor continues building until the control circuit determines the proper time to switch off FET Q_1. At that point, the voltage polarity across inductor L_1 reverses in an attempt to maintain current flow, pulling the top side of the inductor

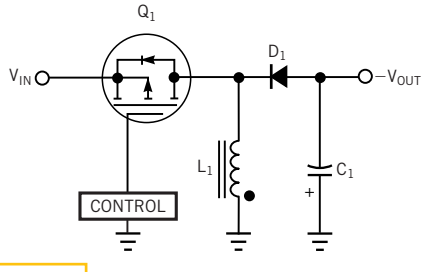

Figure 1

This flyback topology produces negative output voltage from positive inputs.

negative with respect to ground and forcing diode D_1 to conduct. The output voltage goes negative to within a diode drop of the inductor voltage.

The duty cycle at which the control circuit operates also differs from that of a synchronous buck. Although the operating duty cycle of a synchronous buck is $D=V_{OUT}/V_{IN}$, the negative flyback operates at $D=V_{OUT}/(V_{OUT}-V_{IN})$. For example, if the desired output voltage is half the input voltage, the synchronous buck runs at 50% duty cycle, whereas the negative flyback runs at 33% duty cycle. The comparisons between the simple negative flyback circuit of **Figure 1** and the synchronous-buck-controller negative flyback circuit in **Figure 2** are straightforward. In **Figure 2**, FET Q_2 mirrors the function of diode D_1 in **Figure 1** but with a decrease in the forward drop that occurs in the diode. This lower drop significantly improves efficiency. Diode D_3 conducts during the small dead time, when both FETs Q_1 and Q_2 are off, further reducing losses. The feedback voltage appears at the output ground through resistor R_1, because the control circuit is referenced to the negative output voltage. R_2 typically sets the output voltage to the desired level, because it does not change the feedback compensation network, as changing R_1 would. Desired changes to the input voltage, the output voltage, or both may necessitate an inductor-value change. The minimum inductor value is:

$$L_{MIN}=\frac{|V_{OUT}|(V_{INMAX})^2}{2f_{MIN}I_{OUTMIN}\left(|V_{OUT}|+V_{INMAX}\right)^2}.$$

Take note of certain limitations with using the controller in this type of implementation. Because the control circuit is referenced to the negative output-voltage rail, the controller must have an input-voltage rating greater than $V_{IN}+|V_{OUT}|$. The controller must also be rated for V_{IN} (minimum), which occurs at system power-up when the output voltage is zero. A controller that operates over a wide input-voltage range typically works best. The FET's drain-to-source rating must also withstand $V_{IN}+|V_{OUT}|$, and the FET carries peak currents that are greater than twice the output current. Low-resistance, fast-switching FETs produce the lowest losses. High efficiency is the major advantage of this circuit. Because the circuit uses n-channel FETs, as opposed to higher resistance and costlier p-channel parts, the circuit achieves peak efficiencies greater than 90%.

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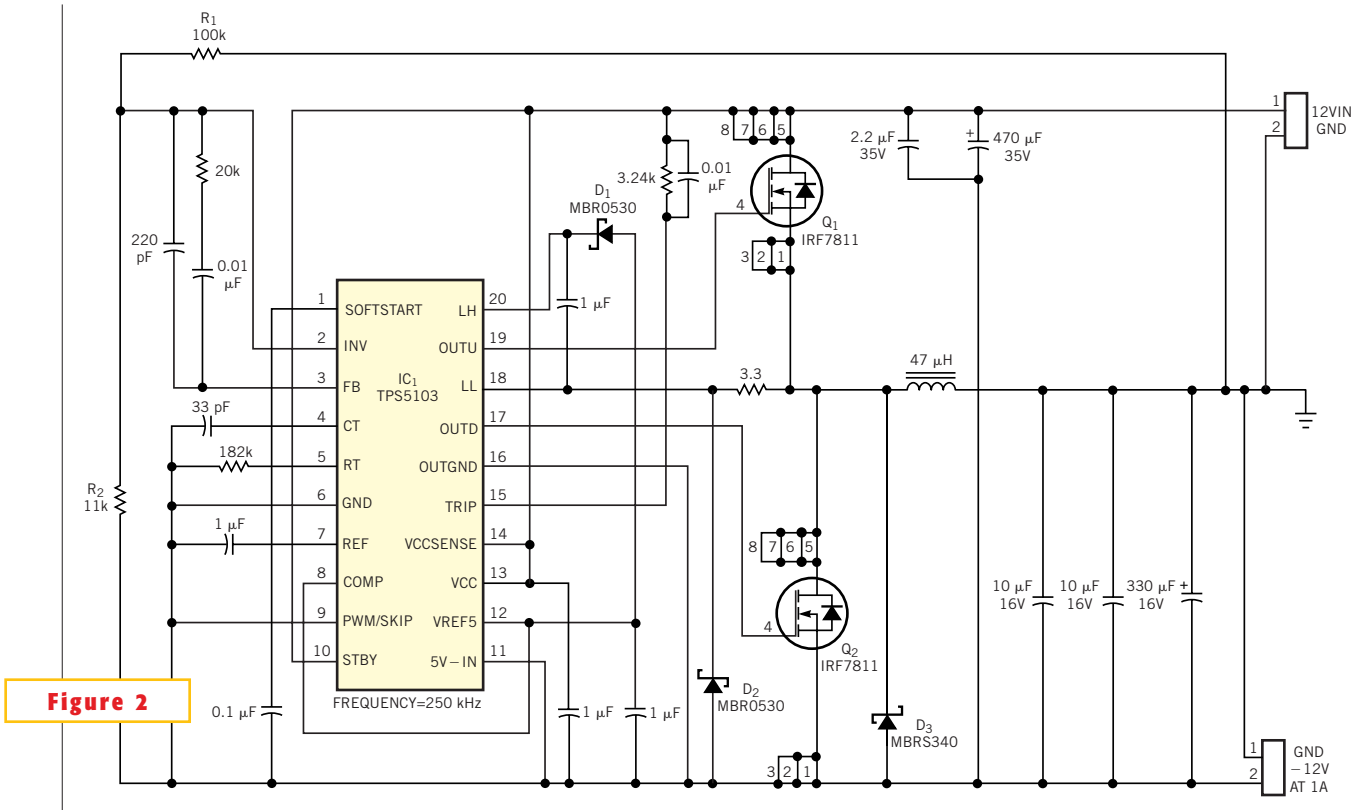


Figure 2

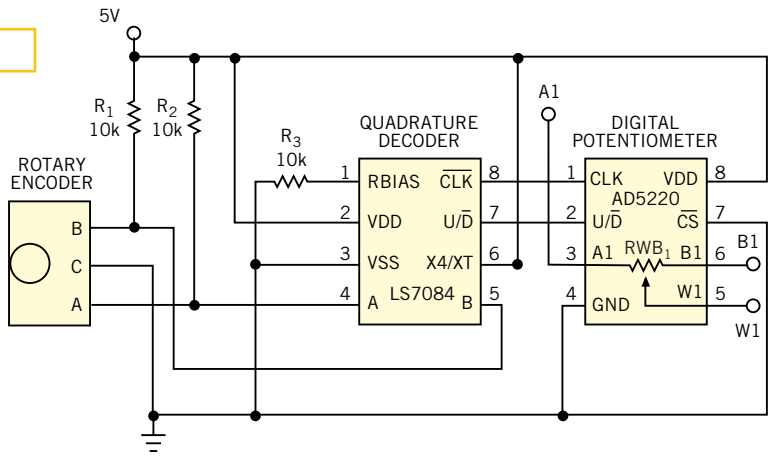
A synchronous buck controller forms the heart of this negative-flyback configuration.

Rotary encoder mates with digital potentiometer

Peter Khairolomour, Analog Devices, San Jose, CA

IN DEVELOPING ELECTRONIC systems, designers look for products or ideas that may benefit from the better performance, smaller size, lower cost, and improved reliability that an IC can offer. Toward that end, the digital potentiometer emerged as an alternative to its mechanical counterpart, the mechanical potentiometer. The digital potentiometer offers most of the cited advantages but falls short for users of mechanical potentiometers, who require a simple rotary interface for front-panel adjustment or calibration without external controllers. The circuit in **Figure 1** represents an attempt to combine the best of both worlds: the simplicity of a rotary interface and the performance of a digital potentiometer. The rotary encoder in this circuit is the RE11CT-V1Y12-EF2CS from Switch Channel (www.switchchannel.com). This type of rotary encoder has one ground terminal, C, and two out-of-phase signals, A and B (**Figure 2**). When the rotary encoder turns clockwise, B leads A (**Figure 2a**), and, when it turns counterclockwise, A leads B (**Figure 2b**).

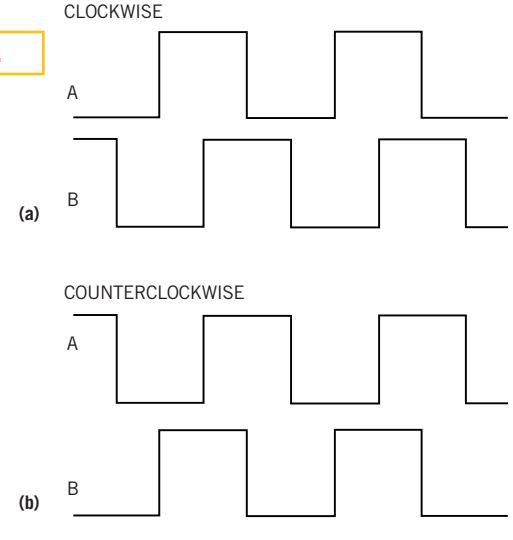
Figure 1



A quadrature decoder and a digital potentiometer form a simple rotary-encoder interface.

Signals A and B of the rotary encoder pass through a quadrature decoder (LS7084 from LSI Computer Systems, www.lsisci.com), which translates the phase difference between A and B of the rotary encoder into a compatible output, $\overline{CLK}$ and U/$\overline{D}$, that the AD5220 can accept. The AD5220 from Analog Devices (www.analog.com) is a 128- step, pushbutton digital potentiometer. It operates with a negative-edge-triggered clock, CLK, and an increment/decrement direction signal, U/$\overline{D}$. When B leads A (clockwise), the quadrature decoder provides the AD5220 with a logic-high U/$\overline{D}$. When A leads B (counterclockwise), the quadrature decoder provides the AD5220 with a logic-low U/$\overline{D}$. The quadrature decoder also produces a clock in synchronism with its output, which also connects directly to the AD5220. You linearly vary the clock's pulse width by adjusting RBIAS.

Figure 2



In clockwise rotation, signal B leads A (a); in counterclockwise rotation, A leads B (b).

Aside from decoding the quadrature output of the rotary encoder and providing a clock signal, the LS7084 also filters noise, jitter, and other transient effects. This feature is important for this type of application. Unlike optical encoders, the RE11CT-V1Y12-EF2CS is a low-cost electrical encoder, in which each turn can create some bounce or noise issues because of the imperfect nature of the metal contacts within the switch. The LS7084 prevents such erroneous signals from reaching the AD5220. The operation of the circuit in **Figure 1** is simple. When the rotary encoder turns clockwise, the resistance from the wiper to terminal B1 of the digital potentiometer, RWB_1, increments until the device reaches full scale. Any further turning of the knob in the same direction has no effect on the resistance.

Likewise, a counterclockwise turn of the knob reduces RWB_1 until it reaches the zero scale, and any further turning of the knob in the same direction has no effect. One example of the flexibility and performance this circuit offers becomes apparent when you consider systems with front-panel rotary adjustment. You can lay out the compact digital potentiometer and quad-

rature decoder anywhere in the system. All the ICs need are two digital control signals routed to the front panel where the rotary encoder is located. This setup proves impervious to interference, noise, and other transmission-line effects that arise in traditional designs with mechanical potentiometers. These designs force the sensitive analog signal to travel all the way to the front of the panel to be processed and then back to its destination.

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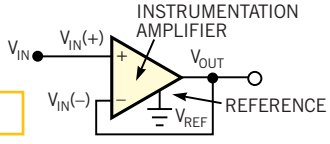
Amplifiers perform precision divide-by-2 circuit

Glen Brisebois and Jon Munson, Linear Technology Corp, Milpitas, CA

THE CLASSIC IMPLEMENTATION of a voltage-halving circuit uses two equal-value resistors. Using 1% resistors provides a divider output with 2% accuracy. For most applications, this performance is cost-effective and more than adequate. However, when you need extreme precision, this approach requires correspondingly accurate resistors and can become expensive. Putting feedback around a finite-gain instrumentation amplifier yields a divide-by-2 circuit with the added benefit of a buffered output (**Figure 1**). The operation of the circuit is straightforward. The instrumentation amplifier has unity gain, so the voltage it sees across its inputs appears between V_{REF} and V_{OUT}: $V_{OUT}-V_{REF}=V_{IN}(+)-V_{IN}(-)$. But, considering the circuit in **Figure 1**, note that $V_{OUT}=V_{IN}(-)$, and $V_{REF}=0$. Substituting in the first equation, you obtain $V_{OUT}=V_{IN}(+)-V_{OUT}$, $2V_{OUT}=V_{IN}(+)$, or $V_{OUT}= 1/2\ V_{IN}(+)$. Thus, you have a divide-by-2 circuit. One of the interesting features of this approach is that the input and the output offsets of the instrumentation amplifier are divided by 2 as well.

Figure 1

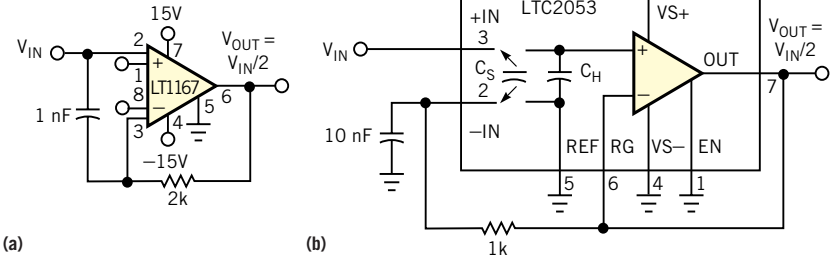


An instrumentation amplifier makes a simple divide-by-2 circuit.

You can implement the circuit on the bench using the LT1167 or the LTC2053 instrumentation amplifiers (**Figure 2**). Although benchtests are unnecessary, you can introduce an RC network into the feedback path for noise shaping and to guarantee dominant-pole behavior. To test for LT1167 offset, set $V_{IN}(+)$ to 0V and alternate $V_{IN}(-)$ between 0V and V_{OUT}. This test confirms that the feedback halves the total offset voltage. Dividing 10V to 5V, the LT1167 shows an error of 100 µV. With the more precise LTC2053, the output error in dividing 2.5V to 1.25V is an almost-immeasurable 2.5 µV. Using cold spray and a heat gun, you can degrade this error to 15 µV. However, perhaps equally important are the calculated worst-case results.

Worst-case calculations for the LT1167 show a maximum 1.12-mV error over 0 to 70°C with 10V input and 5V output. This figure constitutes a total error of 224 ppm over temperature. Resistors that guarantee this accuracy would need a maximum tolerance of 112 ppm each over temperature. The error budget of a resistor-divider solution would require an initial ratio match of approximately 50 ppm with a temperature-coefficient match better than 1 ppm/°C. Worst-case calculations for the LTC2053 with 2.5V input and 1.25V output show a maximum 80-µV error over 0 to 70°C. This figure constitutes a total error of 64 ppm over temperature. Resistors that guarantee this accuracy would need a maximum tolerance of 32 ppm each over temperature. The error budget of a resistor-divider solution would require an initial ratio match of approximately 15 ppm (0.0015%) with a temperature-coefficient match better than 0.25 ppm/°C. In either case, resistors of this caliber would be extraordinarily expensive if available at all. Also, the amplifiers provide the additional benefits of high input impedance and output buffering. Moreover, the error calculations include the effects of input offset voltage, bias current, gain error, and common-mode rejection ratio, which a resistor op amp would still have to add.

Figure 2



Practical implementations of the circuit in Figure 1 use the LT1167 (a) and the LTC2053 (b).

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Edited by Bill Travis

Correct voltage drop and phase shift in transmission lines

Ron Shakery, Texas Instruments, Dallas, TX

Many precision test-and-measurement and high-speed analog applications require an exact targeted voltage to be delivered to the device under test or intended load to accurately analyze the device. Design and test engineers are well-aware that this goal is sometimes unattainable, because the impedance across the traces delivering the signal to the load alters the original signal. Traditionally, engineers use a Kelvin connection to measure the accurate voltage that the load or the device under test sees at its terminals. The Kelvin-connection method enables you to accurately measure the voltage at the load terminal, but it may not correct for the voltage drop or the phase shift that occurs dynamically across the signal lines with various impedances. In high-frequency signals, the RLC (transmission-line effects) of the traces come into play and cause a significant signal phase shift. As a result, designers always look for the least expensive methods to correct the voltage drop and the phase shift across the transmission lines. The circuit in **Figure 1** is a fully differential line driver comprising a fully differential amplifier and two high-frequency, high-impedance feedback paths.

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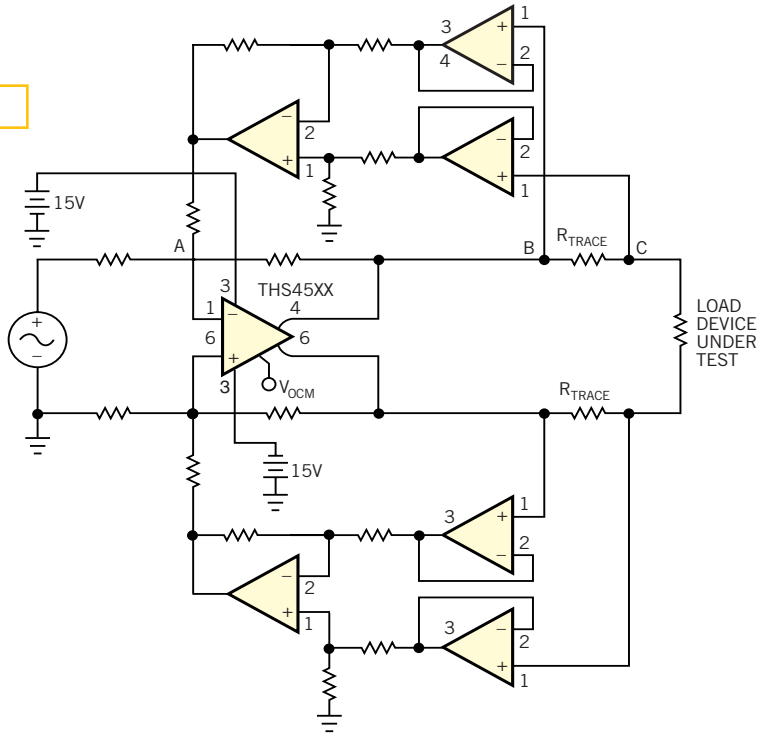
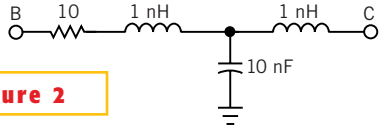
Figure 1



This fully differential circuit compensates for voltage drop and phase shift in transmission lines.

The resistance associated with each trace causes a voltage drop through the path. Thus, the signal amplitude delivered to the load is lower than the signal amplitude at the output of the fully differential line driver. This voltage drop is proportional to the resistance value of the trace, R_{TRACE}, and the current flow through the corresponding trace. For example, if the output current of the line driver is 100 mA and the trace resistance is 10Ω, a 1V drop develops across R_{TRACE}. As a result, if the output amplitude is 10V p-p, the load sees a 9V p-p signal. The feedback paths, which work as subtracters, accurately measure this voltage drop. The feedback paths measure the voltage drop across R_{TRACE}. This voltage then adds to the input of the line driver at the summing Node A. Because the circuit is symmetrical, the same function occurs at the opposite corresponding points. As a result, regardless of the value of the total voltage drop across R_{TRACE}, the sub-

Figure 2



This circuit represents a simulated transmission line inserted between points A and B of the circuit in Figure 1.

tracter measures it and adds it back into the input signal of the line driver. Consequently, the output of the line driver increases by the measure of the voltage drop across R_{TRACE}, and the load sees the exact voltage it was initially intended to see. Because the circuit is a closed-loop system and has negative feedback, the circuit remains in a stable condition.

The buffers in the feedback paths form a high-input-impedance node to prevent any load alteration. For example, without buffers, the series and parallel resistors of the subtracter would cause the value of the load to vary. These buffers, in conjunction with the subtracter, form an instrumentation amplifier. You can adjust this configuration for different gains to create variations of this circuit for different applications. The instrumentation amplifier creates a high-input-impedance path that works similarly to the sense lines of a Kelvin connection. The main difference is that the sense line in this circuit measures the actual voltage drop across R_{TRACE} over various frequencies and adds it back to the original signal. You should pay attention to the ratio of the line driver's gain configuration and the subtracter's gain configuration to ensure stability of the circuit. Additionally, you should verify that the bandwidths of the feedback-path devices are greater than the bandwidth of the line driver to prevent any added errors to the system via feedback paths' bandwidth limitations. You may choose to design the feedback paths with much greater bandwidth than the line driver (two times greater, for example). Doing so enables this circuit to correct the phase shift across the transmission line if the traces manifest RCL characteristics.

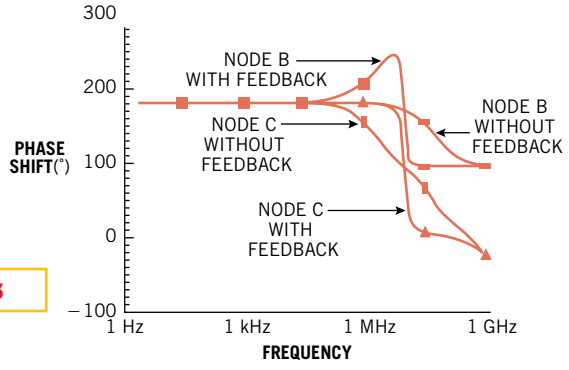


Figure 3

The phase-shift curves at Node B before the transmission line and at Node C after the transmission line show the effect of the feedback path in correcting the phase shift at the end of the transmission line.

For example, assume that you insert a transmission-line model between nodes B and C in the circuit of **Figure 1**, as in **Figure 2**. The bandwidth of the fully differential amplifier is 300 MHz at unity gain, and the input signal is 2V p-p. The bandwidth of the feedback paths is 600 MHz to prevent any added phase shift to the signal from the feedback circuit. Configuring the test circuit as such lets you see the phase shift that the transmission line alone introduces. The transmission line causes a significant phase shift in the signal delivered to the load. **Figure 3** shows the phase-shift curves at Node B before the transmission line and at Node C after the transmission line, right above the load. These curves show the effect of the feedback path in correcting the phase shift at the end of the transmission line where the load is located. This circuit configuration essentially corrects the phase shift of the signal that the RCL of the transmission line causes. The fully differential line driver enables you to deliver twice the voltage swing across the load as opposed to using a single-ended line driver with the same power supplies and similar specifications. However, the nature of fully differential configurations requires that you pay close attention to maintaining the balance of passive and active components to preserve the signal integrity delivered to the load. Therefore, you should set equal resistor values on the top and the bottom feedback paths. This design can correct for voltage drop and phase shifts across the transmission lines in low- and high-frequency cases. Design simplicity and the fact that the design uses few components make it cost-effective for many applications dealing with voltage-correction and phase-shift issues.

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Why limit your power supply's input range?

Michael Day, Texas Instruments, Dallas, TX

Taking only a cursory look at the input-voltage ratings of your power-supply IC can limit the usable input-voltage range. With careful examination of an IC's operating specifications and circuit topology, you may be able to work around that input-voltage limitation. For instance, The data sheet for TI's (www.ti.com) TPS61042 shows that it has all the functions necessary for providing a constant-current drive to a white-LED circuit; however, the input voltage of the IC does not meet the input-voltage requirements of this Design Idea. The dual lithium-ion input voltage varies from 6 to 8.4V, but the TPS61042 input-voltage range is 1.8 to 6V. Closer examination of the circuit shows that the power stage need not connect to the same voltage rail as the control IC. **Figure 1** shows that by separating the input voltage to the TPS61042 from the power stage, you can power the LED driver from an input voltage greater than 6V.

The IC can receive power from any available system voltage of 1.8 to 6V by connecting this voltage to the VIN pin. The input to the power stage can now connect directly to the battery. In general, the power stage can connect to any voltage that is lower than the required output voltage. With a boost topology, the input voltage to the power stage must be less than the output voltage, or the inductor and diode pass the input voltage directly to the output. The maximum allowable voltage on the SW pin, 28V, also limits the maximum input voltage to the power stage.

This technique also improves system ef-

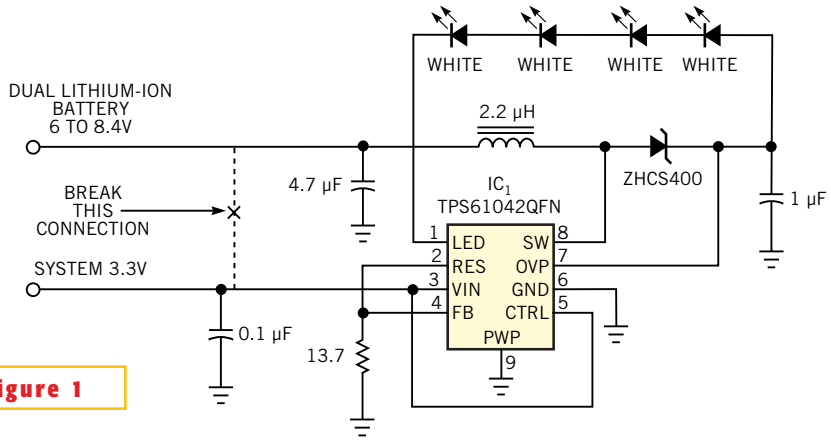

Figure 1

This circuit provides a way to get around a power-supply IC's input-voltage limitations.

ficiency. Efficiency data for this circuit shows that higher input voltages provide higher efficiency. If you have to run the LED driver from a voltage that is lower than 6V, the power to drive the LED is "double-converted." It first converts from the raw lithium-ion input into an intermediate system voltage and then converts from the intermediate-system voltage into the LED-drive current. By carefully examining the operating specs for the IC, you can get around around its input-voltage limitation, save cost and board space, and increase system efficiency.

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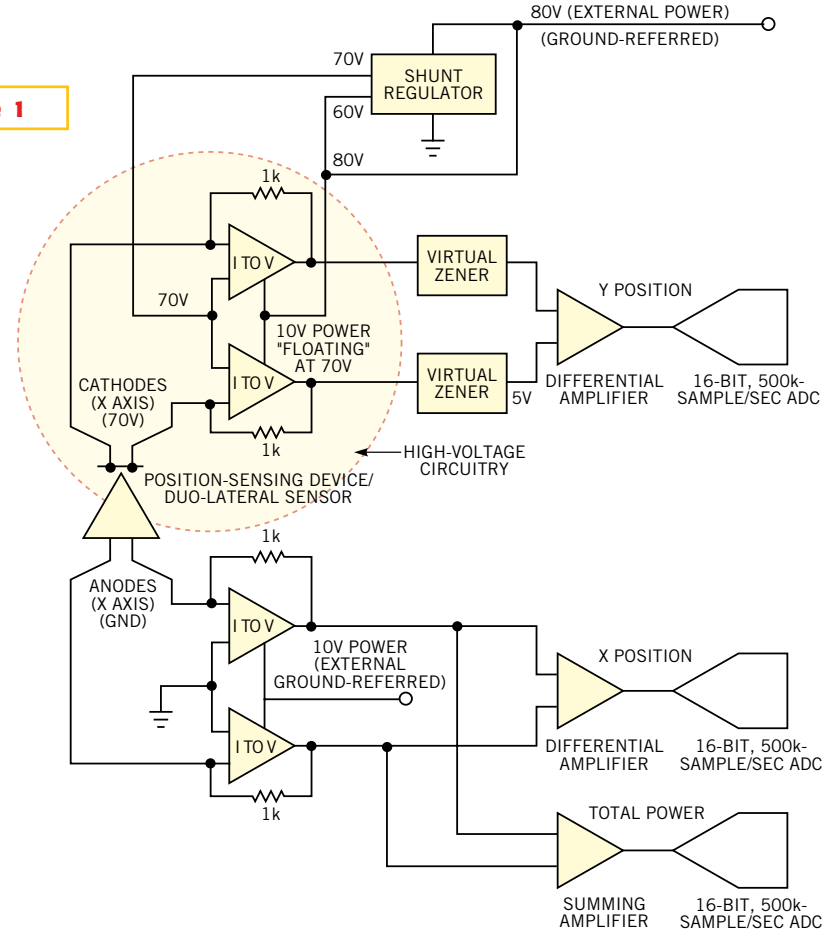
Virtual-zener circuit simplifies high-voltage interface

Philip Lane, Transparent Networks Inc, Bellevue, WA

THIS DESIGN FOR a photonic switch needs more than approximately 70V at the cathode of a duo-lateral optical position-sensing device. This voltage gets speedy response at longer wavelengths, such as 980 nm. The circuit uses fast transimpedance amps, "floated" at 70V. Two "virtual-zener" circuits step down the high-voltage signals for subsequent processing in a ground-referred differential-amplifier stage (**Figure 1**). The circuit drops exactly 65.58V dc with the component values shown, notwithstanding errors arising from op-amp offset voltages and resistor tolerances (**Figure 2**). The function of the virtual-zener circuit is to provide a regulated, floating dc voltage drop between input and output. The size of the drop depends on the ratio of R_1 to R_2 and the magnitude of the reference voltage. The input of the circuit, nominally at 70V dc, draws a constant 3.65 mA. The THS3001 sources or sinks this current plus any additional current as necessary, adjusting the output voltage until the voltages at its two inputs are equal. This equality occurs when $V_Z=(V_{IN}-V_{OUT})=V_{REF}(1+R_1/R_2)$.

The op amp's power-supply rails and output range, along with the voltage drop across R_3, limit the output-voltage compliance. C_1 bypasses R_1. This bypass swamps the bandwidth-reducing effect of

Figure 1



"Virtual-zener" circuits simplify the high-voltage interface in this position-sensing system.

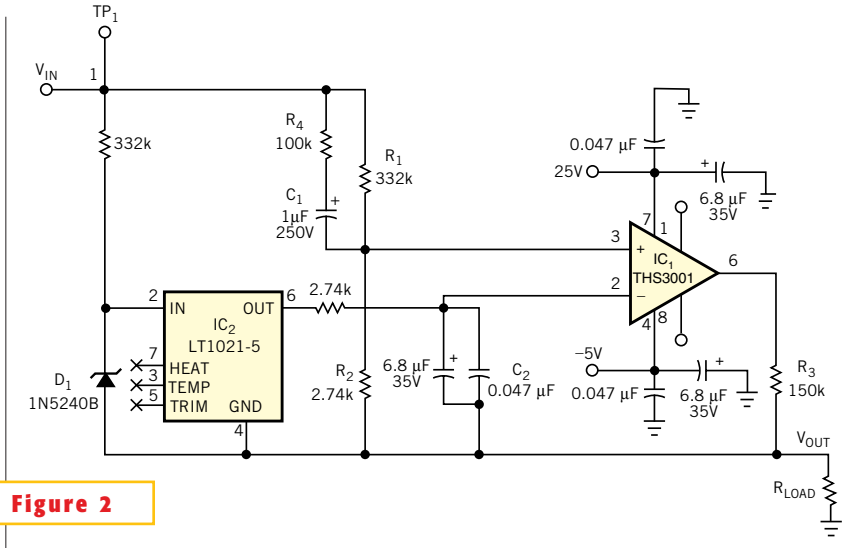


Figure 2

This virtual-zener circuit provides a regulated, "floating" voltage between the input and output.

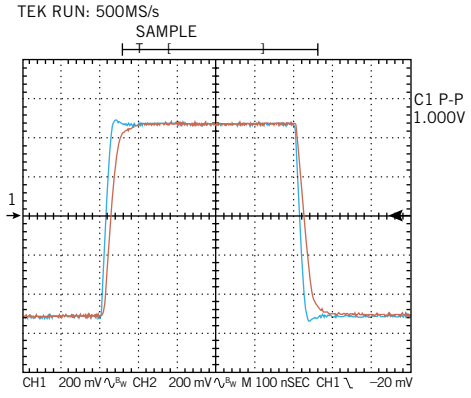


Figure 3

The transient response of the circuit in Figure 2 is exceedingly fast.

capacitance at the noninverting input, and it greatly reduces the noise at the output. Without C_1, the op amp's inherent noise would gain up by a factor of $(1+R_1/R_2)$. R_4 protects IC_1's noninverting input by limiting the transient current supplied by C_1 during power-up and power-down. R_3 and the output, R_{LOAD}, have a similar protective effect on the inverting input, limiting any transient current in C_2. R_3 is necessary to ensure feedback stability of the op amp. The inclusion of this resistor is standard operating procedure for a current-feedback op amp, such as the THS3001. If you use a voltage-feedback type, you could possibly eliminate R_3. Bandwidth is extremely high. **Figure 3** shows the pulse response at 100 nsec per division. (Blue is the input, and red is the output.)

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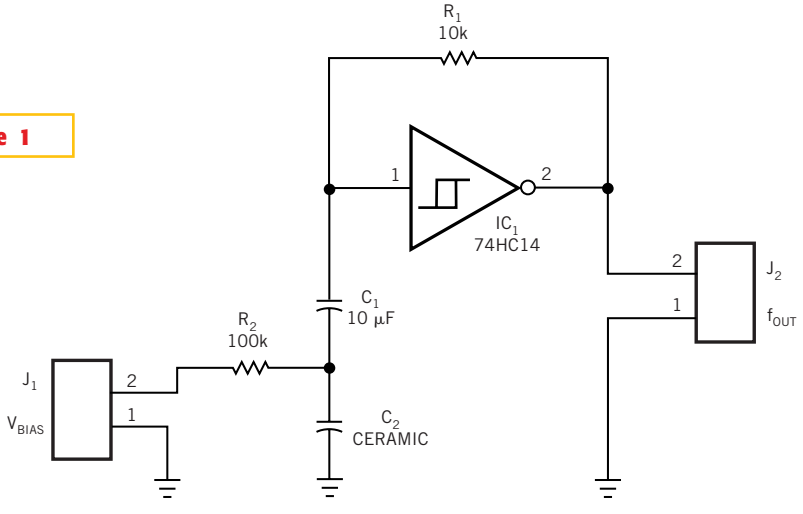
Multilayer capacitor doubles as varactor

Susanne Nell, Breitenfurt, Austria

THE MAIN PURPOSE for building the circuit in **Figure 1** is to study the idiosyncrasies of X5R, Z5U, and Y5V multilayer ceramic capacitors. The circuit is also an inexpensive VCO (voltage-controlled oscillator) with only five components. Many types of ceramic capacitors for surface-mount placement are on the market. The parts become continually smaller because of space problems on the board, and the capacitance values continually increase to compete with more expensive tantalum-electrolytic units. Unfortunately, capacitors with X5R, Z5U, or Y5V dielectrics have some undesirable properties. They exhibit voltage-dependent capacitance values. The idea behind the circuit in **Figure 1** is to check the influence of a dc bias

Figure 1



This simple oscillator shows the effect of a dc bias on a multilayer capacitor, C_2.

voltage on the frequency of a simple oscillator. The net result is a low-frequency VCO with a relatively large voltage-gain figure, which depends largely on the type of capacitor you use.

The circuit is a simple oscillator using a Schmitt-trigger inverter. The frequency is a function of R_1, C_1, and C_2. C_2 is the ceramic capacitor with voltage-dependent capacitance. Using the value of C_1, you can shift the frequency independently of C_2. This design uses a stable-foil-type capacitor for C_1 to avoid bias-voltage-dependent effects in the measured results. If necessary, you can compensate the temperature coefficient of the capacitor with a combination of NTC, PTC, and metal-film resistors for R_1. For measurements, this design uses a simple metal-film resistor. The capacitance change with temperature is normally less than 10% from 10 to 35°C for Z5U and Y5V and much lower for X5R. **Figure 2** shows the measured voltage-versus-frequency graphs with different values and types for C_2. For **Figure 2,** C_1=10 µF; the orange curve represents a 4.7-µF, 10V, Z5U multilayer capacitor, and the purple curve represents a 10-µF, 10V, Z5U multilayer capacitor. **Figure 3** shows similar plots for values of C_1 (orange: 1 µF; purple: 10 µF). The moral of the story is: Be wary when using high-capacitance ceramic capacitors with high or variable dc bias; the varying capacitance can greatly influence circuit performance.

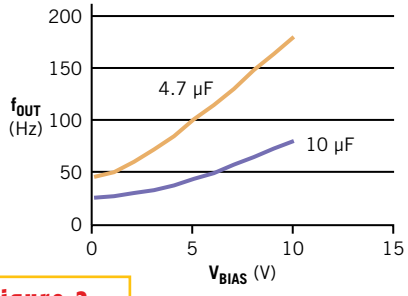


Figure 2

The frequency of the oscillator in Figure 1 exhibits almost a 4-to-1 shift for a 4.7-µF Z5U multilayer capacitor.

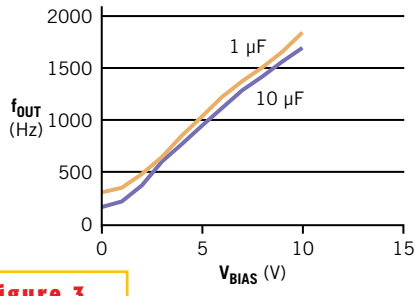


Figure 3

The value of C_1 has little effect on the frequency curves for the circuit in Figure 1.

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Buck regulator and two inductors make dual-polarity converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

A common problem for power-supply designers is to create a compact, dual-polarity step-down converter. If space and cost are not concerns, the obvious solution is a pair of dc/dc converters, one for each output. But space and cost are almost always issues for communications, data-acquisition, and disk-drive applications. **Figure 1** shows a single current-control- regulator approach that supplies 5V at 700 mA and −5V at 500 mA from a 12V system source. The circuit features efficiency similar to that of a two-regulator solution and has no component measuring more than 3 mm high. The low profile and low board real estate that this design requires are almost impossible to match using a flyback design or a similar dual-output SEPIC design using a transformer instead of two inductors. Note, however, one important limitation of this circuit that makes it inappropriate for some applications: For the circuit to maintain regulation, the positive load must always outweigh the negative load. **Figure 2** shows some efficiency curves at various positive-output currents.

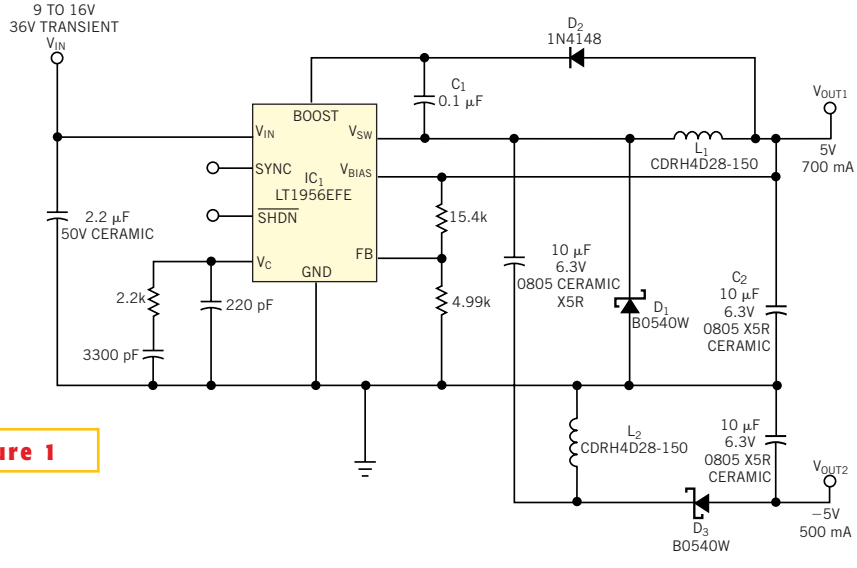


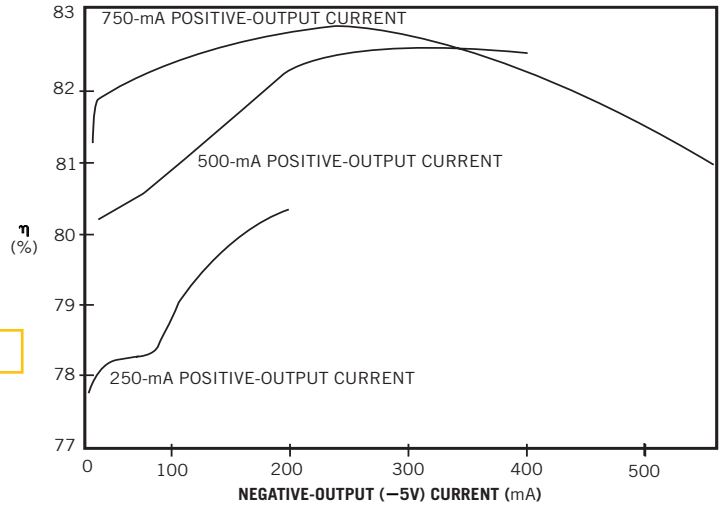
Figure 1

This dual-polarity dc/dc converter uses a single-switch buck regulator.

The dual-polarity output circuit is similar to that of a typical single-output positive buck regulator. The circuit adds a secondary negative output by attaching a coupling capacitor (C_1), a second in-

ductor (L_2), a catch diode (D_3), and an output capacitor (C_2). The negative output voltage maintains regulation based on the voltage of the coupling capacitor's remaining constant and equal to the 5V output voltage. Current ramps up and down in the secondary inductor, L_2, with the same peak-to-peak ripple as that of the primary inductor, L_1. The low-impedance path of the coupling capacitor provides the current to L_2 during the on-time of the switch and induces the same voltage across L_2 as appears across L_1. The Schottky catch diode, D_3, provides a current path for the inductor during the off-time of the switch and a current path from the coupling capacitor when discharging into the positive output. Current must flow from the coupling capacitor into L_1 during the off-time of the switch for the capacitor to discharge all the charge gained during the on-time of the switch. This current flowing into the positive inductor during the off-time takes the place of some of the current that would normally be sourced from the positive catch diode, D_1, reducing the losses in D_1 but increasing the losses in D_3.

Figure 2

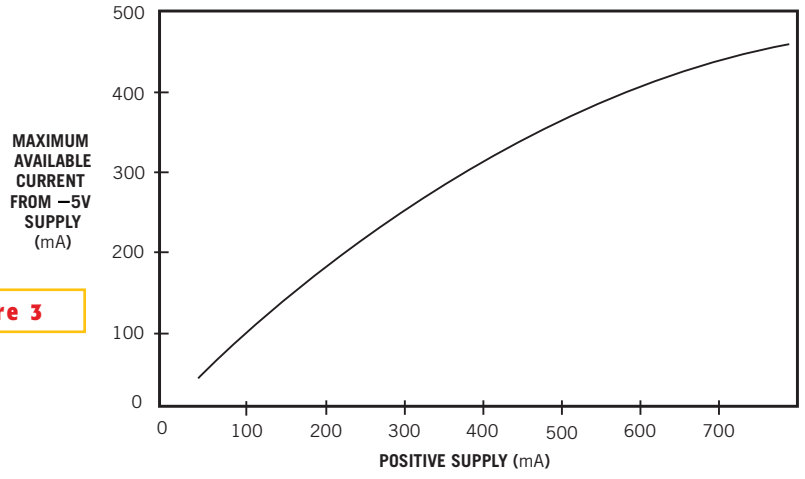


These curves represent efficiency figures for various positive and negative output currents.

The need for the coupling capacitor to charge and discharge equally creates

an important limitation of the circuit: To maintain regulation on both outputs, the negative-supply output current must always be less than the positive-supply output current (**Figure 3**). If the negative-supply output current increases enough to equal the positive-supply output current, regardless of how great the positive current is, the output voltage begins to collapse. Also, if the negative-supply output current is too low (below 5 to 25 mA, depending on input voltage), the negative-supply voltage can balloon. With extremely light negative loads, the coupling-capacitor discharge current during switch off-time and the inductor current (L_2) during switch on-time come only from the negative output capacitor, C_2 (as opposed to both the negative output capacitor and the negative dc load). Thus, the output capacitor charges well past its intended voltage because no negative dc load is available to discharge the capacitor. If you use this circuit in an application in which the negative output will see light loads, use a 25-mA preload to maintain regulation.

Figure 3



This curve gives the maximum available negative-output current as a function of positive-supply current.

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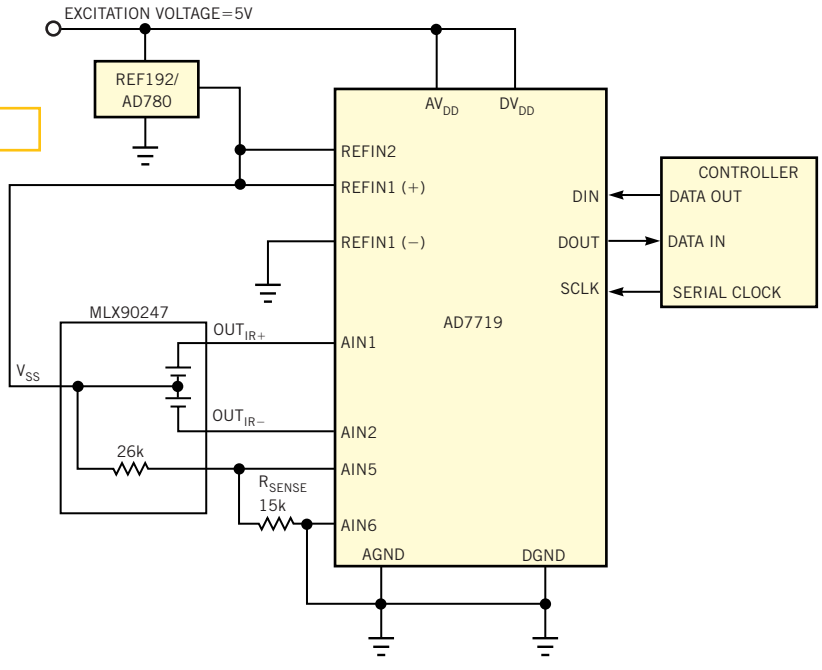
Temperature-measurement scheme uses IR sensor and sigma-delta ADC

Albert O'Grady and Mary McCarthy, Analog Devices, Limerick, Ireland

Many noncontact temperature-measurement systems use infrared sensors, such as thermopiles, which can detect small amounts of heat radiation. Biomedical thermometers that measure the temperature of an ear or a temple use noncontact temperature measurement, as do automotive-HVAC systems that adjust temperature zones based on the body temperature of passengers. Household appliances and industrial processes can also benefit from the use of noncontact temperature measurement. Infrared thermometers can measure objects that move, rotate, or vibrate, measuring temperature levels at which contact probes either would not work or would have a shortened operating life. Infrared measurements do not damage or contaminate the surface of the item being measured. Thermal conductivity of the object being measured presents no problem, as would be the case with a contact temperature-measurement device. The circuit in **Figure 1** provides a design for a high-resolution digital thermometer that uses a thermopile sensor and a sigma-delta ADC. The design provides high resolution and response times of approximately 1 msec, and it eliminates the need for high-performance, low-noise signal conditioning before the ADC.

Figure 1



Using an infrared sensor and a sigma-delta ADC, you can make noncontact temperature measurements.

The high-accuracy, noncontact digital temperature measurement system uses the MLX90247D thermopile from Melexis (www.melexis.com) and the AD7719 high-resolution, sigma-delta ADC from Analog Devices (www.analog.com). The AD7719 provides differential inputs and a programmable-gain amplifier; thus, you can connect it directly to the sensor, allowing the temperature-measurement system to provide high accuracy without the need for precision signal-conditioning components preceding the ADC. The MLX90247D sensor comprises a thin, micromachined membrane embedded with semiconductor thermocouple junctions. The Seebeck-coefficient thermocouples generate a dc voltage in response to the temperature differential generated between the hot and the cold junctions. The low thermal conductivity of the membrane allows absorbed heat to cause a higher temperature increase at the center of the membrane than at the edge, thus creating a temperature difference that is converted to an electric potential by the thermoelectric effect in the thermopile junctions. The MLX90247D also con-

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tains a thermistor, allowing you to configure a temperature-compensated system in relative-measurement mode.

The AD7719, a dual-channel, simultaneously converting ADC with an internal programmable-gain amplifier is an ideal ADC when you use it with the MLX90247D sensor in temperature-measurement applications. The main channel is 24 bits wide, and you can configure it to accept analog inputs of 20 mV to 2.56V at update rates of 5 to 105 Hz. The auxiliary channel contains a 16-bit ADC and accepts full-scale analog inputs of 1.25 or 2.5V with an update rate equal to that of the main channel. The AD7719 accepts signals directly from the sensor; the internal programmable-gain amplifier eliminates the need for high-accuracy, low-noise external-signal conditioning. The AD7719 simultaneously converts both the thermopile and the thermistor sensor outputs. The main channel with its programmable-gain amplifier monitors the thermopile, and the auxiliary channel monitors the thermistor. You can use on-chip chopping and calibration schemes in optimizing the design. The AD7719 features a flexible serial interface for accessing the digital data and allows direct interface to all controllers.

The sensitivity of the thermopile is 42 μV/K; thus, it produces an output voltage of 9.78 to 15 mV over the industrial temperature range of −40 to +85°C, an output that the AD7719 can directly measure. The thermistor's impedance ranges from 15.207 kΩ at −40°C to 38.253 kΩ at +85°C with a nominal impedance of 26 kΩ at 25°C. Again, you can directly measure voltages from the thermistor, as **Figure 1** indicates. Biomedical thermometers generally have a measurement range of 34 to 42°C. In this range, the thermopile's differential output is 336 μV. Operating the AD7719 in its ±20-mV input range with a 5-Hz update rate allows temperature measurement with a resolution of 0.05°C.

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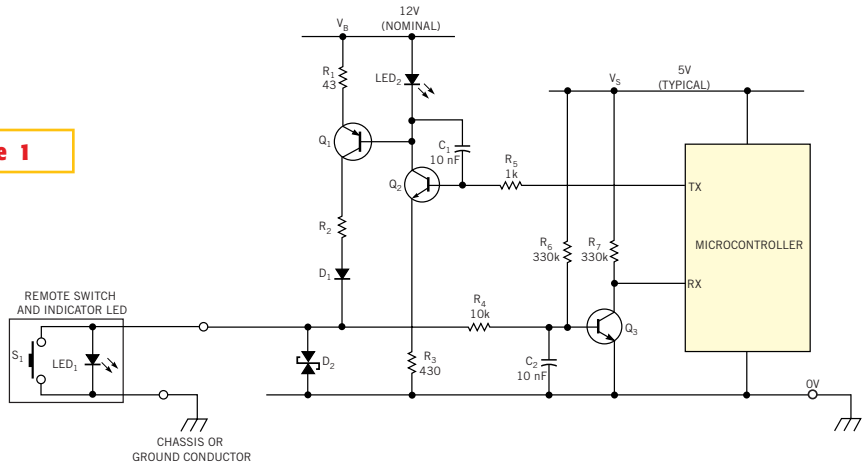
Automotive link uses single wire

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

In the automotive industry, in which the goal is to produce cars with simpler, lighter wiring looms, any interface that uses just one wire instead of two offers a distinct advantage. The circuit in **Figure 1** implements a bidirectional link using a single wire, with the car's chassis or ground conductor providing a negative return path. The microcontroller communicates with the driver of the car by illuminating LED_1. The driver communicates by operating switch S_1. Detecting the switch closure requires no current sensing: The circuit simply exploits the fact that the forward voltage drop of a properly biased LED is usually two or three times the V_{BE} of a bipolar transistor. Q_1, LED_2, and Q_2 form a semiprecision current source. Q_3 in the receiver path detects the switch closure. When the microcontroller's TX pin goes high, Q_2 illuminates LED_2 and biases Q_1 on. Q_1 sources a constant current to LED_1 via R_2 and D_1.

Figure 1



This circuit implements a bidirectional link using a single wire and a ground return.

LED_2 constitutes an inexpensive but effective voltage reference, which imposes a constant voltage across current-setting resistor R_1. Provided that you choose R_3's value to suit Q_2's base drive, you can set the current in LED_2 and the voltage across it to fairly precise and constant values. For example, with R_3=430Ω, the current in LED_2 is approximately 10 mA with 5V at Q_2's base (TX high). If you use a device such as the HLMP-1000 for LED_2, its forward voltage remains constant at approximately 1.6V, putting approximately 0.9V across R_1. The resulting 20 mA or so flowing in Q_1 provides adequate brightness for LED_1 and remains acceptably constant with changes in V_B or temperature.

With S_1 open, R_6 biases Q_3 on, pulling the receiver pin, RX, low. RX remains low, regardless of whether LED_1 is on. When the switch closes, the values for R_4 and R_6 ensure that Q_3's base pulls down to approximately 150 mV (with V_S=5V), thereby turning off Q_3 and allowing RX to go high. As long as the switch remains closed, RX stays high, whatever the state of the TX pin. Powering the current source directly from the car's battery voltage, V_B, rather than from the microcon-

troller's supply, not only relieves the burden on the low-voltage regulator, but also ensures that LED_1 receives proper bias, even with a very low value for V_S. Thus, provided that R_3, R_4, and R_6 have appropriate values, the circuit functions with V_S as low as 3V or even lower. A further advantage is that you can replace LED_1 with several LEDs connected in series. With $V_B = 12V$, the current source has adequate compliance to drive four or five LEDs.

R_2 is a nonessential component, but it reduces the power consumption in Q_1. D_1 provides positive overvoltage protection for the current source, and voltage-suppressor D_2 can protect against the harmful transients that systems often encounter in the harsh automotive environment. C_2 with R_4 provides a degree of noise filtering and has negligible effect on the switching of Q_3. You may need C_1 and R_5 to roll off Q_2's frequency response to avoid the possibility of high-frequency oscillation. The transistor types are not critical; most devices with respectable current gain and adequate power rating are satisfactory. LED_2 provides a triple function. As well as acting as a voltage reference for the current source, it also provides local indication of the external LED status by illuminating in synchronism with LED_1. Additionally, it provides open-circuit (broken-wire) indication by turning off completely (even when TX is high) if the connection between D_1 and the external LED breaks—a feature that may be useful for troubleshooting purposes. In the event of a broken wire, little collector current flows in Q_1, and its base-emitter junction shunts LED_2; provided that R_1 is much smaller than R_3, the shunt steals LED_2's bias current, thereby turning it off. Although the circuit was developed for an automotive product, you could easily adapt it for use in other applications in which a simple user interface must operate on a single line.

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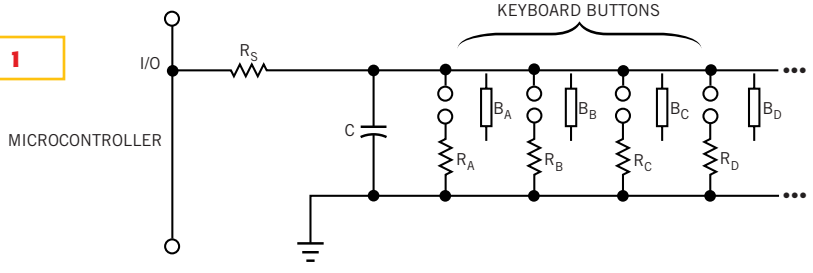
Novel idea implements low-cost keyboard

Jean-Jacques Thevenin, Thomson Plasma, Moirans, France

Many applications that use a microcontroller also use a keyboard. If your application uses a relatively powerful microcontroller, you can use several free I/O pins or an unused input with an ADC to effect an easy keyboard connection. But, if the microcontroller in your system has too few free I/O pins and no on-chip ADC, you can be in trouble. However, if your system doesn't require a high-performance keyboard, you can solve the problem by using the circuit in **Figure 1**. How does it work? At system initialization, the I/O connection is an output, set to logic 0; hence, C is discharged. In reading the keyboard, the following steps take place:

Figure 1



This circuit provides an inexpensive and easy way to read a small keyboard using only one I/O line of a microcontroller.

1. I/O (output) assumes the state logic 1, V_{OUT}.
2. V_C charges to logic 1 (V_{OUT}) or to a voltage that R_S and the other resistors determines. (You can set the output I/O to logic 1 by default. In this case, you can omit steps 1 and 2, and the routine becomes faster. This design uses 0 instead of 1 to have an inactive signal on the line when the keyboard is not checked.)
3. I/O becomes an input.
4. For a duration T_{MAX}, the microcontroller checks the input I/O to see whether it resets to logic 0.
5. If, after T_{MAX}, the input I/O is still at logic 1, no button has been activated.
6. If within T_{MAX}, the input I/O resets to logic 0, the measured time indicates the activated buttons.
7. I/O becomes output again and resets to logic 0 to discharge C.

Several equations describe the operation of the scheme. First, assume some conditions: V_{OUT} is the voltage of the output I/O at logic 1; V_{TH} is the threshold for logic 0 input to the microcontroller; and R_X is the value of the parallel combination of R_A, R_B, and the other resistors.

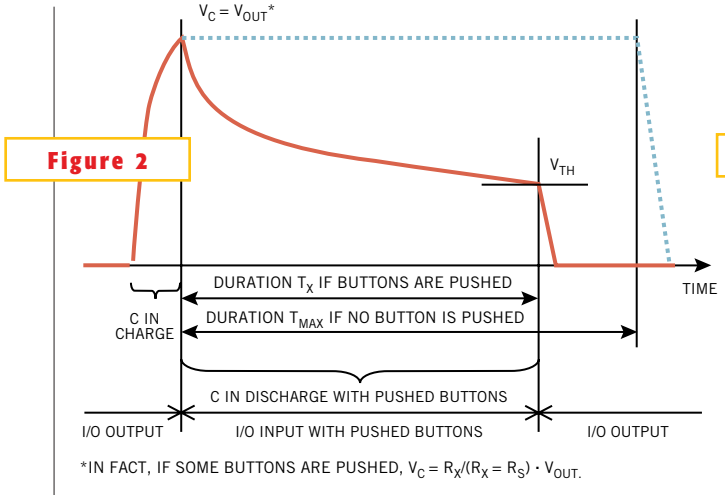
Figure 2 shows the timing diagram for the circuit of **Figure 1**. You can evaluate the duration of T_X with the following expression: $T_X \simeq R_X C \log_e(V_C/V_{TH})$. If R_X is not negligible with respect to R_{XMIN} (but the R_{INPUT} of the microcontroller greatly exceeds R_X), then

$$T_X \approx R_X \bullet C \bullet \log_e\left(\frac{V_{OUT}}{V_{TH}} \bullet \frac{R_X}{(R_X + R_S)}\right),$$

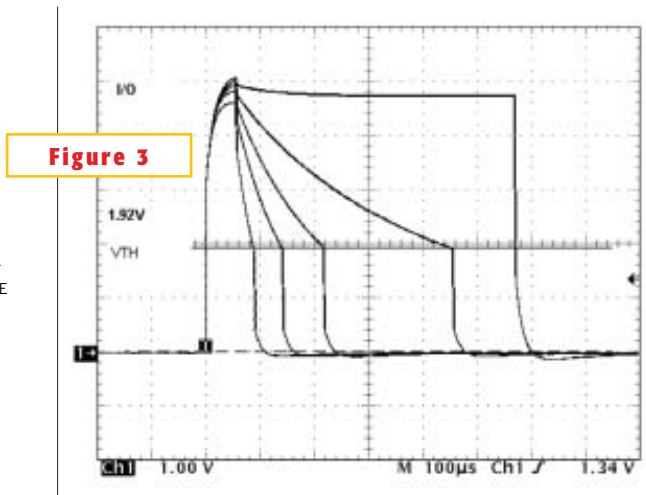
where V_{OUT} is the voltage at logic 1 on the I/O output. From the last equation, a condition for R_X is:

$$R_{XMIN} > R_S \bullet \frac{V_{TH}}{V_{OUT} - V_{TH}}.$$

Note that, if R_A, R_B, and the other re-



The duration, T_X, indicates which buttons or combinations thereof you pushed.



These waveforms at the I/O pin and table show the returned value (duration) with different combinations.

sistors form an R-2R string, R_{XMIN} is approximately equal to $R_A/2$. R_S limits the current from the microcontroller and must have a minimum value of V_{OUTMIN}/V_{OUTMAX}. This resistor creates a delay for charging and discharging C of approximately $5R_SC$. The following is an example of a small keyboard with four buttons: To choose R_S, I_{OUTMAX} of the microcontroller is 25 mA at V_{OUT}=5V, so $R_{SMIN} \geq 200\Omega$. So this design uses $R_S = 220\Omega$. R_A, R_B, R_C, and R_D are 1, 2.2, 3.9, and 8.2 kΩ, respectively. You can select values that greatly exceed R_S. In this case, the effect of R_S is negligible, but you should then consider the effects of the input resistance of the microcontroller.

The duration between two measurements is approximately 2 µsec (**Listing 1**). With one byte, the maximum duration, T_{MAX}, is 512 µsec (when no button is pushed). So, time T_X with R_{XMAX} (in other words, R_D) must be inferior to T_{MAX}. Assuming that V_{TH} is 1.5V (minimum), the equation for T_X becomes

$$8200 \bullet C_{MAX} \bullet \log_e\left(\frac{5}{1.5} \bullet \frac{8200}{(8200+220)}\right) < 512\ \mu SEC \rightarrow C_{MAX} < 53\ nF.$$

So, at the beginning of each measurement, you must append a delay of 5×220Ω×47 nF=52 µsec to charge C. **Figure 3** shows the waveforms at the I/O pin and the returned values with different button combinations. The power consumption of the circuit, with C=47 nF, V_{CC}=5V, and a keyboard reading every 30 msec, is approximately 0.04 mW (practically negligible). You can use this scheme in all applications that don't require great accuracy or high speed. You can download **Listing 1** from the Web version of this Design Idea at www.edn.com.

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LISTING 1–THE DURATION BETWEEN TWO MEASUREMENTS

```
/*
 * Function :     LittleKb_Scan with 1 I/O
 *
 * Description :  scans the Little Keyboard
 *
 * Return value : 0 if not any touch is pushed
 *                else a value between 1 and 255
 *
 * Note :         by default, KB_IO is an output
 *                and its exit is set to 0 (see Note 1)
 */

BYTE LittleKb_Scan (void)
{
BYTE bRet = 0;
                        // beginning …
KB_IO = 1;              // sets I/O (out) to 1 (see Note 1)
Delay_us(55);           // waits for 55us (see Note 1)

KB_IO_Input();          // KB_IO is an input
do
{
      bRet++;           // counter ++
      if(KB_IO == 0)    // checks I/O (input)
            break;
} while (bRet != 0);    // the loop lasts 2us

KB_IO = 0;              // resets I/O to 0 (see Note 1)
KB_IO_Output();         // KB_IO is an Output
                        // and discharges C
return bRet;            // … end
}
```

Get more power with a boosted triode

Dave Cuthbert, Boise, ID

Even though 6L6 beam-power tubes have been around for 66 years, they are still quite popular for use in electric-guitar amplifiers, and its cousin, the 6CA7 (EL34) power pentode, is a favorite among audiophiles. The developers of these tubes designed them for pentode-mode operation, and they deliver maximum audio power in this mode. On the other hand, many audiophiles prefer triode-mode operation and, until now, had to be content with a 50% reduction in output power. This reduction means that they require larger power supplies and twice as many expensive tubes to obtain pentode power from a triode amplifier. **Figures 1a**, **1b**, and **1c** show the 6L6 connected as a pentode, a true triode, and a "boosted triode," respectively. The boosted-triode configuration allows pentodes to produce pentodelike power while operating in a true-triode mode. To understand the operation of the boosted triode, it's useful to review some vacuum-tube theory.

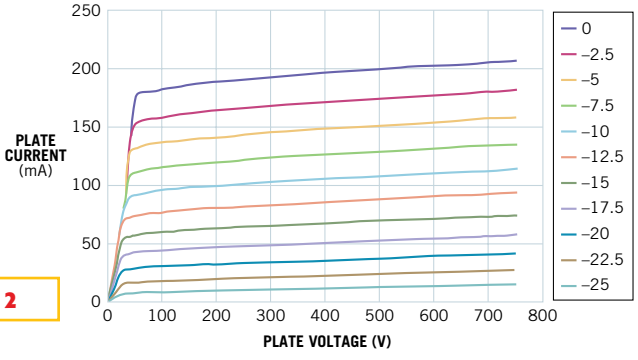

Figure 2

The load lines for a pentode show that the plate can draw 150 mA at a plate voltage of only 50V.

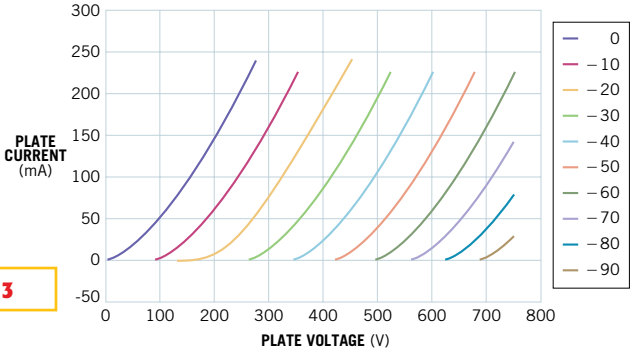

Figure 3

A pure triode needs 200V plate voltage to draw 150 mA.

The 6L6 is a beam-power tube and has cathode, control-grid, screen-grid, suppressor-grid, and plate electrodes. The suppressor grid is actually a virtual suppressor grid provided by two beam-forming plates, but you can treat the 6L6 beam-power tube as a pentode. You can think of a pentode as an n-channel JFET with the following electrode functions:

- Thermionic cathode: source of electrons (corresponds to the JFET source);
- Control grid: controls the cathode current; operated at a negative potential relative to the cathode (corresponds to the JFET gate);
- Screen grid: electrostatically screens the control grid from the plate, thereby reducing the effect that the plate voltage has on the cathode current; operates at a positive potential relative to the cathode;
- Suppressor grid: prevents secondary electrons from leaving the plate and traveling to the screen grid; operates at the cathode potential; and
- Plate: collects the electrons (corresponds to the JFET drain).

Figure 2 shows the pentode's characteristic curves for control-grid voltages of 0 to −25V and a screen-grid voltage of

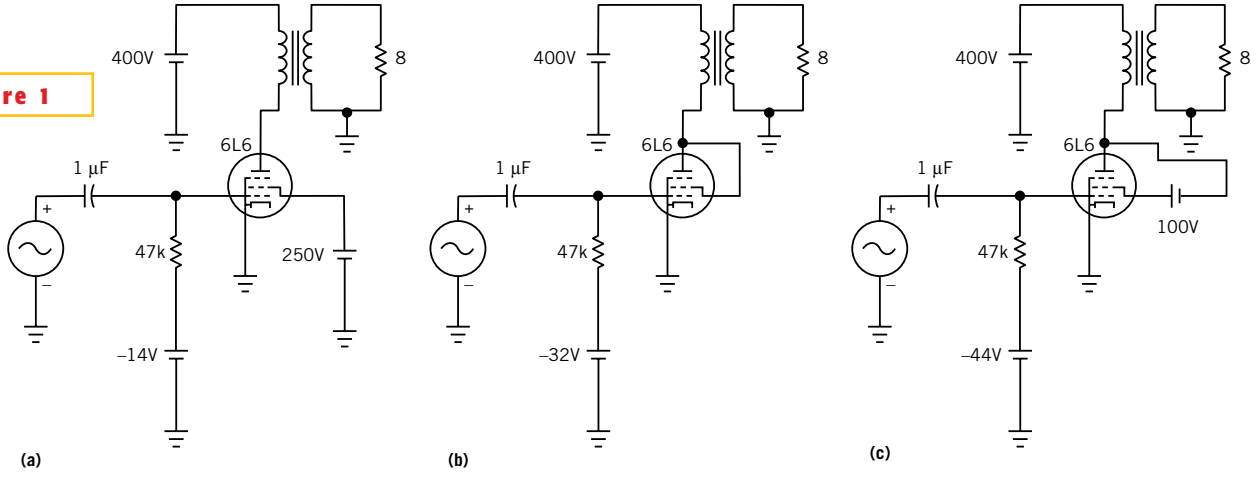

Figure 1

A pentode (a) can deliver much more power than a triode (b), unless you use a boosted-triode configuration (c).

250V. Note the idealized load line and that the tube can draw a plate current of 150 mA at a plate voltage of only 50V. High voltage gain, high plate impedance, and high output power characterize pentode-mode amplification. By connecting the screen grid directly to the plate, you can operate the tube in triode mode. Low voltage gain and low output impedance characterize this mode. **Figure 3** shows how the triode curves differ from the pentode curves. The curves represent control grid voltages of 0 to −90V. Note the load line and that, in triode mode, the plate cannot draw 150 mA at a plate voltage lower than 200V. This fact greatly limits amplifier efficiency and power output. However, in spite of the limited output power, some people still prefer triode mode because they claim it produces a superior-sounding amplifier.

TABLE 1—PENTODE, TRIODE, AND BOOSTED-TRIODE PARAMETERS

Amplifier	DC plate current (mA)	Grid bias (V)	Grid swing (V)	Output power (W)
Pentode	75	−14	22	11
Triode	75	−32	64	6
Boosted triode	75	−44	88	10

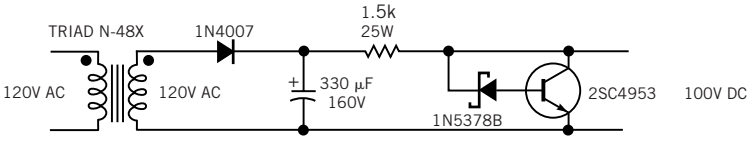

Figure 4

A 100V screen-grid power supply transforms a normal triode into a boosted triode.

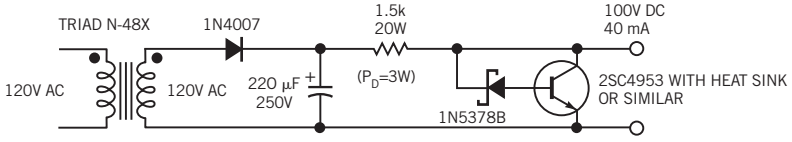

Figure 5

With a boosted triode, the plate can draw 150 mA with a plate voltage of 100V, versus 200V for a pure triode.

For the boosted-triode circuit in **Figure 1c**, you simply add a 100V screen-to-plate power supply (**Figure 4**) to the standard triode-amplifier circuit. This addition shifts the triode characteristic curves 100V to the left (**Figure 5**). Note the load line and that the plate can now draw 150 mA at a plate voltage of only 100V, rather than 200V as with the pure-triode-mode circuit. You can obtain significantly higher power with boosted-triode amplification and still maintain the characteristics of triode amplification. In Spice simulations of three single-ended Class A audio amplifiers using MicroCap-7 evaluation software (www.spectrum-soft.com), the control-grid bias for a quiescent plate current is 75 mA, and the ac grid signal is just short of amplifier clipping. The transformer ratios provide a plate-load impedance of 5 kΩ for the pentode and 3 kΩ for both the triode and the boosted triode. **Table 1** details the parameters.

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Anticipating timer switches before you push the button

Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

(Editor's note: This *Twilight Zone*-worthy circuit will be the subject of an upcoming network sitcom, *My Big Fat Anticipating Timer*.)

IT HAPPENS TO ALMOST EVERYONE that an apparatus or system should have been turned off *a moment ago*. The device in question could be the car heater, the air conditioner, the lights...

This Design Idea offers a solution to the challenge of turning devices on or off in the past. In **Figure 1**, IC_2 is a 555-type timer (preferably CMOS) connected as a monostable one-shot multivibrator. The pushbutton switch, S_1, triggers IC_2. You can replace S_1 with a transistor or an optocoupler, for example. You can connect V_{OUT} to a relay or a transistor, if needed. You might need to adjust the values of R_4 and R_5, depending on the output load and the characteristics of S_1. The interval during which V_{OUT} remains high is $T=1.1RC_2$. In **Figure 1**, you replace the resistor, R, that normally connects to C_2 with the circuit inside the dashed line. This circuit comprises a 741 op amp, IC_1, and three resistors: R_1, R_2, and R_3. You could replace the war-horse 741 with a TL081 if your design needs longer time delays.

Taking into account the usual op-amp assumptions—equal voltage on both inputs and zero input current—you de-

rive the following expressions: $V_O=V(R_2+R_1)/R_1$, and $V_O=V-R_3I_C$, where V_O is the op amp's output voltage, V is the voltage at the noninverting input, and I_C is the current through R_3. I_C is also the current that charges C_2. Combining the cited expressions, you can compute the value of resistor R that the op-amp circuit replaces: $R=V/I_C=-R_3R_1/R_2$. The timing interval of this timer is thus $T=-1.1C_2R_3R_1/R_2$. Using appropriate values, you can obtain long time delays that you can't attain with the basic 555 circuit. But the real innovation inherent in this circuit is that its output turns on at a defined time, T, *before* you press S_1. To adjust interval T, use a potentiometer for R_1. Because the wiper of the potentiometer connects to the power supply, adjusting R_1 contributes minimal EMI and other insidious effects to the op amp's input. C_1 is a power-supply bypass capacitor, and C_3 stabilizes the 555's control voltage. With the values shown in **Figure 1**, the interval T is approximately 18 minutes.

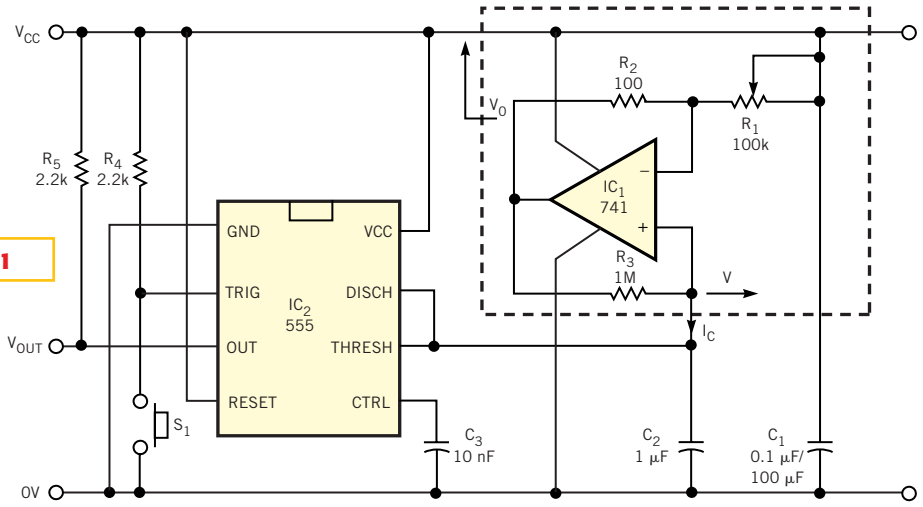

Figure 1 This innovative timer turns on approximately 18 minutes *before* you press switch S_1.

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design ideas

Edited by Bill Travis

Reset supervisor waits for stable supply

Mike Mitchell, Texas Instruments, Dallas, TX

THE POWER-UP CYCLE of the supply voltage in embedded-system applications is sometimes not a clean event. This fact holds especially true in battery-operated systems, because the insertion of a battery often causes significant ringing or glitching on the supply line (**Figure 1**). In products with on-off switches, the contact bounce of the switch can cause an unclean power-up. A power-up cycle such as the one in **Figure 1** can often cause a processor to enter a brownout condition. This condition constitutes an errant condition of the processor, which requires a reset to take place before the processor behaves as expected. The processor is often "lost" or "in the weeds" during a brownout condition. Usually, a reset supervisor controls the reset line to the processor and thus avoids the brownout condition. Traditional supply-voltage-supervisor circuits hold the processor in reset until the supply voltage reaches a predetermined value. They also reset the processor if the voltage dips below the predetermined value. However, the level at which the SVS operates often does not suit the system. For example, the level may be lower than the minimum operating voltage of the processor, or it may be higher than the desired operating voltage of the system. The reset circuit in **Figure 2** provides a reset to the processor based on stabilization of the supply voltage and not on a predetermined value.

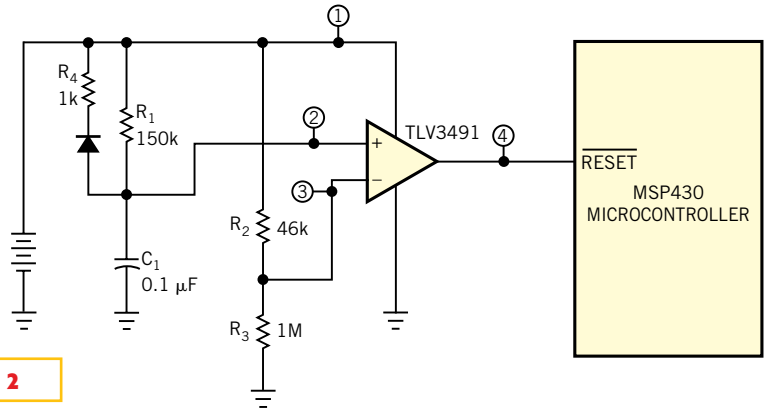

Figure 2

This circuit resets a processor based on the stabilization time of the supply voltage.

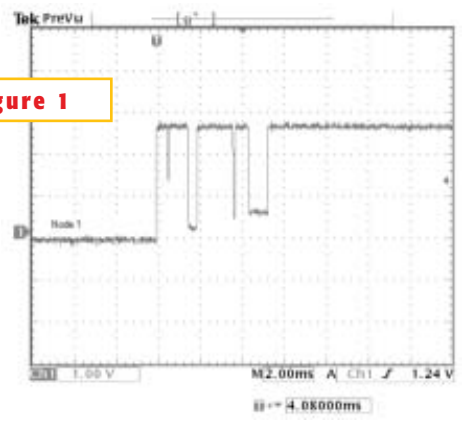

Figure 1

Insertion of a battery supply often results in glitching and ringing.

The circuit uses a TLV3491 from Texas Instruments (www.ti.com). The comparator draws approximately 1 µA and operates from 1.8 to 5.5V, making it well-adapted to battery-operated applications. The input to the minus terminal is a simple resistor divider. The resistor values should be relatively high to reduce the power consumption of the circuit. The input to the plus terminal is basically an RC circuit. The RC time constant provides a tunable power-up delay. When you apply power or insert a battery, the output of the comparator is low, holding the processor in the reset condition. The plus input of the comparator becomes higher than the minus input only after the supply voltage stabilizes, resulting in a high output state and thus releasing the processor for operation. The stabilization time for the supply voltage depends on the RC-network component values. Here, the use of low-value resistors carries no penalty, because no current flows through the RC network after supply stabilization. By selecting R_1, C_1, R_2, and R_3, you can guarantee a reliable reset signal to the processor for a given dV/dt for V_{CC}. The equations for the voltages at the comparator's inputs are:

$$V^+ = V_{CC} - V_{CC}\, e^{\frac{-t}{R_1 C_1}};$$

$$V^- = V_{CC}\,\frac{R_3}{R_2 + R_3}.$$

To hold the processor in reset, you

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need the condition $V^- > V^+$. That condition yields:

$$V_{CC}\frac{R_3}{R_2+R_3} > V_{CC} - V_{CC}e^{\frac{-t}{R_1C_1}}.$$

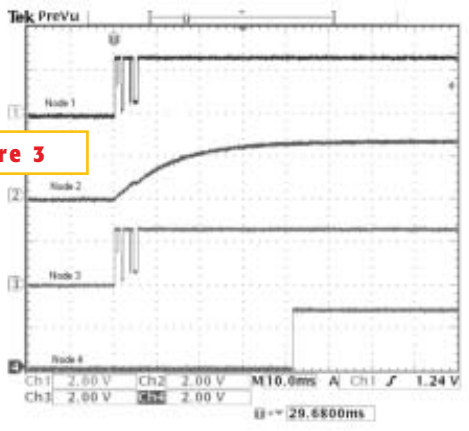
Solving for t, you obtain

$$t < -R_1C_1\ln\left(\frac{R_2}{R_2+R_3}\right).$$

From the last equation, you can calculate the amount of time the processor stays in reset. Therefore, as long as the supply ramps to a steady state in a shorter time, you're guaranteed a reliable reset. The reverse-biased diode and resistor R_4 provide a faster discharge path for the capacitor. This fast discharge allows the circuit to quickly react to negative glitches in the supply voltage during normal operation, in which it may be desirable to reset the processor. R_4 allows you to tune the response time of the circuit for any expected supply-voltage glitches. Removal of the resistor yields the fastest response time to supply-voltage glitches but may result in undesired resets for the processor. The pullup resistor at the output of the comparator is necessary because of the comparator's open-drain output. The capacitor at the comparator's output smoothes any fast switching the comparator may encounter.

The current consumption of the circuit in **Figure 2** is approximately 1 µA (the current consumption of the comparator) plus the current through R_2 and R_3. The circuit costs less than many dedicated supply-voltage supervisors. **Figure 3** illustrates the performance of the circuit. **Figure 3** is a scope capture of the same battery insertion of **Figure 1**. The top trace is the supply voltage; the next trace is the positive input to the comparator. The negative input to the comparator is the next trace, and the bottom trace is the comparator's output (connected to the microcontroller's reset pin). You can clearly see that the circuit holds the processor in reset until the supply stabilizes. Thus, the perfomance depends not on any predefined supply-voltage level, but rather on stabilization time.

Figure 3



The circuit in Figure 2 enables the processor well after the stabilization of the power-supply voltage.

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Small circuit forms programmable 4- to 20-mA transmitter

Alan Li and Jeritt Kent, Analog Devices, Bellevue, WA

One of the key challenges in the design of 4- to 20-mA current transmitters is the voltage-to-current conversion stage. Conventional transmitters use multiple op amps and transistors to perform the conversion function. These approaches have been around for a long time, but they are usually inflexible, have poor power efficiency, and have limited current compliance. An improved Howland current pump, on the other hand, can be cost-effective, because it addresses the cited problems. In addition, it closely models an ideal current source with the potential for nearly infinite output impedance. **Figure 1** shows the improved Howland-current-pump topology, implemented with a high-resolution DAC, a precision reference, and a high-current op amp. Analyzing the circuit in **Figure 1** (neglecting the loading effects at the output of IC_3), the voltage at V_X is $V_X = (V_{REF} \times D)/2^N$, where D is the decimal equivalent of the DAC's digital code and N is the number of bits.

Analyzing nodes V_L and V_N, you obtain

$$I_L = \frac{V_{OUT} - V_L}{R_3'} - \frac{V_L}{R_1' + R_2'}. \quad (1)$$

$$\frac{V_N - V_X}{R_1} = \frac{V_{OUT} - V_N}{R_2 + R_3}. \quad (2)$$

Because V_N and V_P are virtually shorted, you obtain

$$V_N = \frac{R_1'}{R_1' + R_2'}V_L. \quad (3)$$

Substituting V_N and V_{OUT}, I_L becomes

$$I_L = \frac{(R_2+R_3)/R_1}{R_3'}V_X + \frac{(R_1'R_2 - R_1R_2') + (R_1'R_3 - R_1R_3')}{R_1R_3'(R_1' + R_2')}V_L. \quad (4)$$

Making $R_1 = R_1'$, $R_2 = R_2'$, and $R_3 = R_3'$ simplifies **Equation 4** to

$$I_L = \frac{(R_2+R_3)/R_1}{R_3'} \bullet \frac{V_{REF} \bullet D}{2^N}. \quad (5)$$

According to **Equation 5**, you can use R_3' to set the circuit's sensitivity. You can make R_3' as small as necessary to achieve the desired current and improve the load range. As an alternative, you can make the other resistors large to keep the quiescent current low for high power efficiency. The improved Howland current pump is flexible. It offers both current-sink and -source capability. The input voltage at V_X is polarity-insensitive; you can apply it to either R_1 or R_1'. You can connect the load to the supply rail as a high-side load, or you can refer it to a low-side supply or ground (**Figure 1**). Further, one of the primary advantages of this topology is that the current pump provides poten-

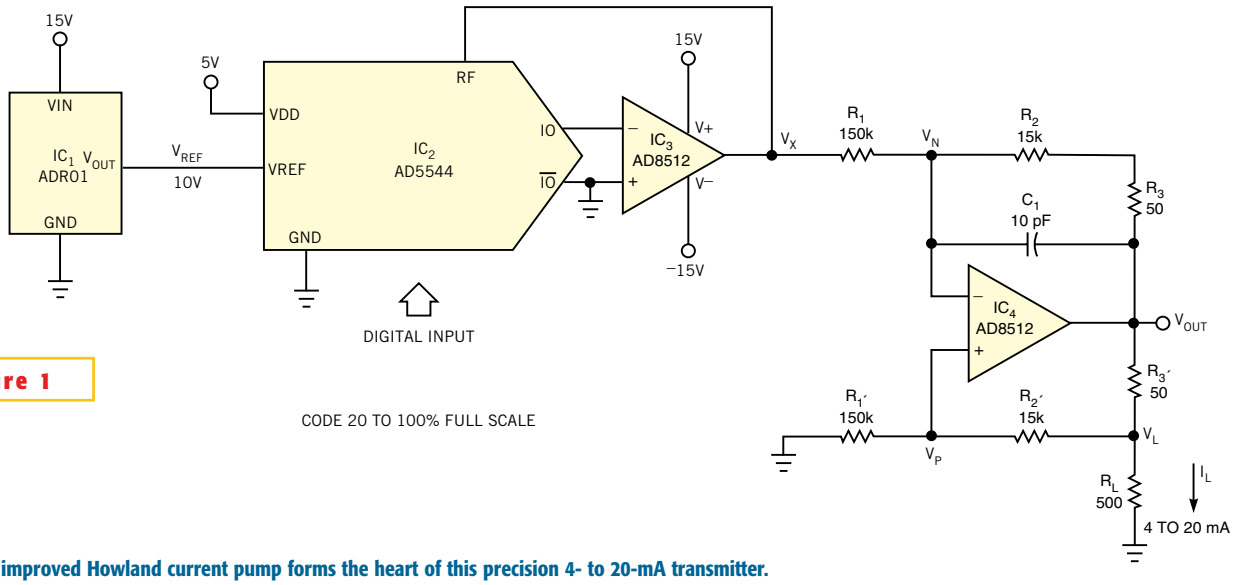

Figure 1

An improved Howland current pump forms the heart of this precision 4- to 20-mA transmitter.

tially *infinite* output impedance, like that of an ideal current source. However, you must pay strict attention to resistor matching. You can see the importance of matching by examining the circuit's output impedance. If you ground all inputs and apply a test voltage at V_L, you can see that

$$Z_{OUT} = \frac{V(t)}{I(t)} = \frac{R_1R_3'(R_1' + R_2')}{R_1'(R_2 + R_3) - R_1(R_2' + R_3')}. \quad (6)$$

Equation 6 shows that, if the resistors are perfectly matched, Z_{OUT} is infinite. Infinite output impedance is a desirable characteristic of a current source because the resistance of the load does not affect the current flowing in the load. On the other hand, if the resistors are not matched, Z_{OUT} can be either positive or negative. Negative Z_{OUT} causes instability because of the existence of a right-half-plane pole in the s-plane domain. Any amount of parasitic capacitance—from poor pc-board layout, op-amp differential capacitance, or both—at the inverting node of IC_4 could cause instability or worse. These parasitics, along with R_1, introduce a zero into the noise-gain transfer function, resulting in a slope of 20 dB per decade. If the noise-gain transfer function of the amplifier intersects with the open-loop response at a slope (rate of closure) equal to or greater than 40 dB per decade and the open-loop gain at the intersection exceeds unity, then the circuit is likely to be unstable. The circuit may ring, show gain peaking, or conditionally oscillate after a step function in the DAC adjustment.

An effective approach to the stability problem is to insert a pole into the noise-gain transfer function by adding a compensation capacitor, C_1. This capacitor creates a pole to keep the rate of closure at 20 dB per decade. Optimum compensation occurs when $R_1C_{PARASITIC} = R_2C_1$. Because $C_{PARASITIC}$ is unknown, you should determine C_1 empirically to obtain optimum results. In general, C_1 in the range of some tenths of a picofarad to a few picofarads satisfies compensation requirements. Note that optimum compensation attempts to balance the fact that a small C_1 cannot compensate for all possible causes of oscillation, whereas large values of C_1 could adversely affect the settling time of any DAC. Consider the following design objectives: 16-bit programmability, four channels, small form factor, a maximum ground-referred load of 500Ω with 10V compliance, 90% minimum efficiency, and 50-mW maximum dissipation from each resistor.

Given the requirements of small form factor and high precision, the design in **Figure 1** uses IC_2, the a 16-bit current-output AD5544 DAC, with an external op amp instead of a voltage-output DAC. You face some important trade-offs in deciding whether to use a current-output or a voltage-output DAC. Current-output devices typically cost less than voltage-output DACs. The design must convert the current to a voltage to run the current pump, and the external op amp determines the accuracy of this conversion. Thus, you have control of the amount of accuracy as your application requires. Voltage-output DACs generally cost more than current-output devices because the current-to-voltage conversion takes place in the package, entailing the inclusion of an op amp. Al-

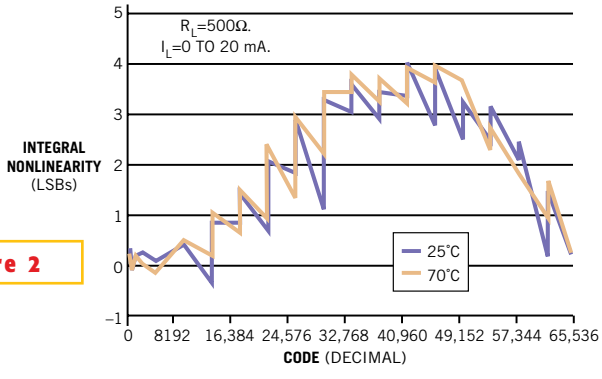

Figure 2

Integral-nonlinearity errors from the circuit in Figure 1 don't exceed 4 LSBs at 16-bit resolution.

though a voltage-output DAC reduces component count in this design, you have to accept a particular accuracy figure based on the specifications of the op-amp buffer inside the DAC. Both approaches typically require an external reference. In the end, a current-output approach yields the highest accuracy at comparable cost and board space.

Although IC_3, which performs the current-to-voltage conversion, can be almost any precision op amp using ±15V supplies, IC_4 requires adequate current-driving capability to handle the maximum 20-mA load. The improved Howland current pump is insensitive to load-resistance perturbations. Only IC_4's supply voltages limit the compliance voltage. A 500Ω load, for example, can place V_L as high as 10V at 20-mA load current. This scenario sets V_{OUT} at 11V, requiring the op amp to swing within 4V of the positive rail. The AD8512 dual op amp can drive 20 mA into a 500Ω load using ±15V supplies. However, IC_4's output-voltage swing is likely to limit resistive loads to 500Ω in this application. This design uses the 10V ADR01 reference because it is precise and compact.

To minimize the power in the resistors, you start with $R_3' = 50\Omega$. R_3' is in the direct load-current path, and it carries just slightly more current than the load, assuming $R_2' + R_1' >> R_L$. At the 20-mA peak current, the power dissipation is just above 20 mW. With the limited headroom between the supply and the compliance voltages, you should scale the ratio between R_2 and R_3 such that the additional gain does not saturate IC_4. As a result, you should choose R_2 to be 10 times smaller than R_1. Using **Equation 5** and the resistance-matching criteria, you obtain the following values: $R_1 = R_1' = 150$ kΩ; $R_2 = R_2' = 15$ kΩ, and $R_3 = R_3' = 50\Omega$. It's desirable to add a 1- to 10-pF capacitor, C_1, to the negative-feedback path to avoid possible oscillation arising from eventual resistor mismatch.

A 16-bit, programmable, 4- to 20-mA current transmitter theoretically has 0.3-μA resolution. The actual measured performance of the circuit in **Figure 1** shows that the worst-case integral-nonlinearity error is approximately 4 LSBs. This error is equivalent to 1.2 μA, or 0.006% total system error, well within most systems' requirements. **Figure 2** shows the measured results at 25 and 70°C.

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High-side current sensor monitors negative rail

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

All dedicated current-sense amplifiers provide high-side sensing on a positive supply, but you can adapt such circuits for monitoring a negative supply (**Figure 1**). The positive-supply pin, V+, connects to the system's positive supply, and the ground pin, GND, connects to the negative supply, V_{EE}. That arrangement monitors the negative supply and provides a positive output voltage for the external interface—typically, an A/D converter. The RS+ pin of the current-sense amplifier, IC_1, connects to the load, and the RS− pin connects to the negative supply. IC_1's current-source output drives a current that is proportional to load current flowing to ground, not to the GND pin. Output resistor R_{OUT} converts the current to a voltage, which an optional ADC then digitizes.

Saturation in the internal transistors, which occurs at approximately ((V+)−1.2V), limits the maximum output voltage. Thus, V+ must exceed the full-scale output by at least 1.2V. If, for instance, the full-scale output is 1V, then V+≥2.2V. To meet the device's maximum and minimum operating voltages, $0 \geq V_{EE} \geq -(32 - V+)$, and $((V+) - V_{EE})) \geq 3V$. **Figure 2** shows the variation of current measurement accuracy with load current.

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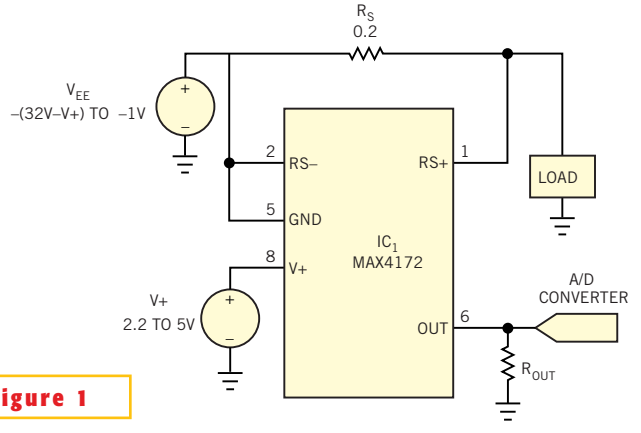

Figure 1

Connecting this positive-supply monitor allows it to monitor a negative current and generate a positive output voltage for the ADC.

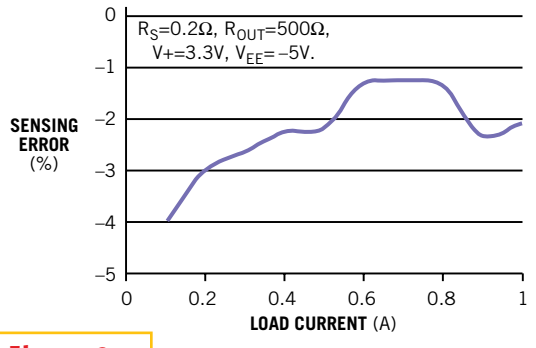

Figure 2

The current-sensing error of the circuit in Figure 1 varies with load current.

Transconductance amp gives oscillator reciprocal response

Mike Irwin, Shawville, PQ, Canada

THE CIRCUIT IN **Figure 1** is a variation on the familiar integrator/comparator triangle-wave oscillator, which you typically implement with two op amps. An integrator and a comparator connect in a positive-feedback loop; the comparator drives the integrator and vice versa. A fixed amount of hysteresis exists in the comparator, producing a triangle wave at the integrator's output. The wave oscillates between the fixed threshold voltages. You can vary the oscillation rate using a potentiometer to set the integrator's gain and thus obtain a constant-amplitude, variable-frequency, triangle-wave output. In the circuit of **Figure 2**, the integrator's gain is fixed, whereas the comparator's hysteresis is variable. An OTA (operational transconductance amplifier), IC_2, sets the hysteresis, producing an oscillator in which the period is a linear function of an externally applied voltage. The oscillation rate is inversely proportional to the control voltage; in other words, the oscillator has a 1/x response. Such an oscillator is useful in A/D-converter applications and for clocking time-delay systems, such as audio-delay lines.

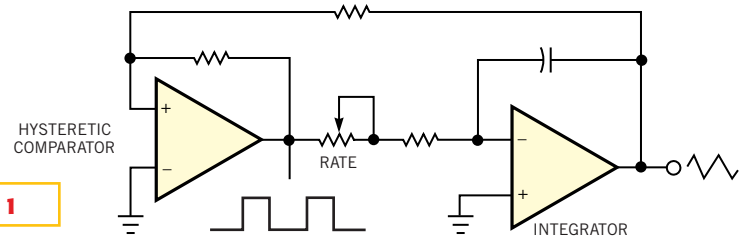

Figure 1

This circuit is a classic triangle-wave generator, using an integrator and a comparator with hysteresis.

In **Figure 2**, R_3 and the ±15V output of comparator IC_{3A} fix the integrator current at ±20 µA. The integrator produces a triangle of fixed ±200V/sec slope, and the peak amplitude is a function of the hysteresis. OTA IC_2 provides voltage control of the hysteresis. With increasing V_{IN}, the hysteresis and triangle-wave peak-to-peak amplitude increase, consequently increasing the oscillator period, T. The triangle wave's amplitude changes from approximately 1 mV p-p to a maximum of 20V p-p as V_{IN} varies from 0 to 10V. With the same V_{IN} span, the period increases from 20 µsec to 200 msec. IC_1 and Q_1 form a linear voltage-controlled current source that supplies bias current, I_{ABC}, to the OTA. The current $I_{ABC}=V_{IN}/R_{IN}$. You can see that I_{ABC} increases from 0 to 0.5 mA as V_{IN} varies from 0 to 10V. The OTA is a switched-current generator, producing a bidirec-

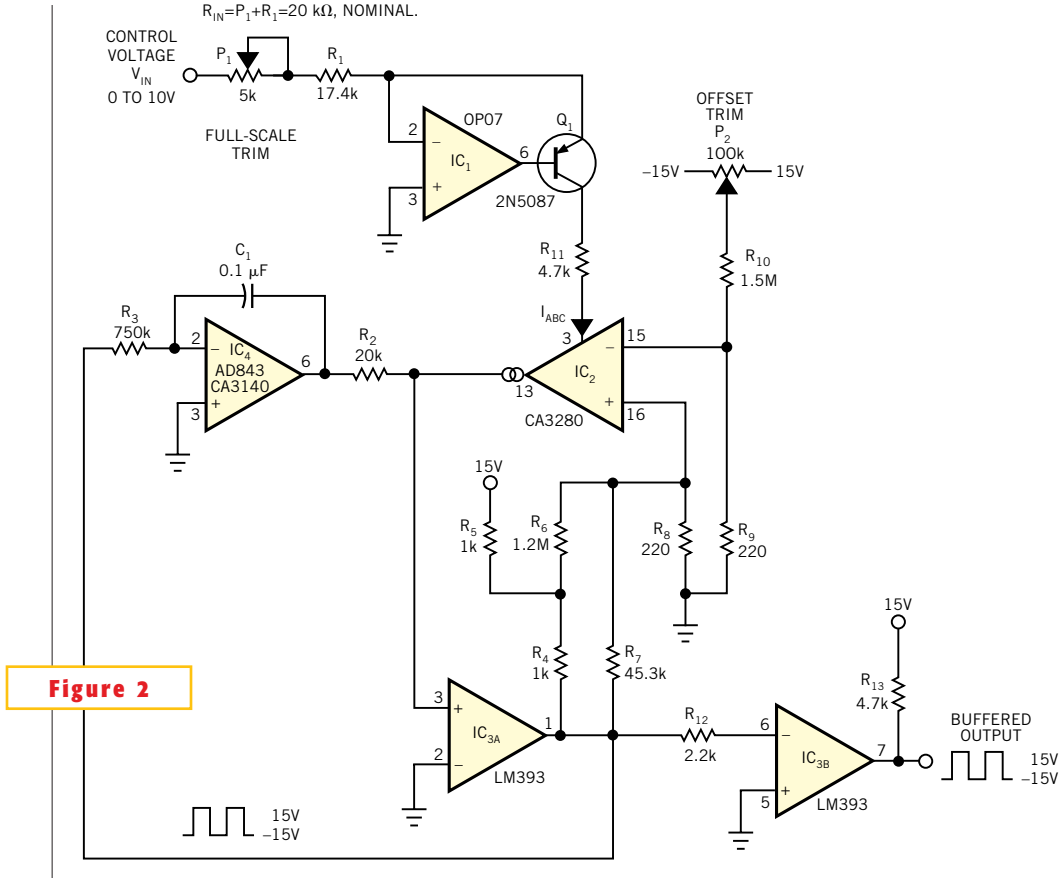

Figure 2

This VCO uses an OTA and a hysteretic comparator to deliver a reciprocal (1/x) response to the control voltage.

tional output current approximately equal in amplitude to I_{ABC}, when it receives drive from the comparator's open-collector output.

The OTA sources current when the comparator's output is 15V and sinks an identical current when the output is −15V. Pullup resistors R_4 and R_5, along with resistors R_6 through R_9, provide a symmetrical ±70-mV drive to the OTA's noninverting input. The high-compliance output of the OTA provides hysteresis by translating the voltage at the comparator's noninverting input up and down by the amount $R_2I_{ABC}=R_2V_{IN}/R_{IN}$. The resulting threshold voltages are symmetrical around the comparator's input offset voltage. This symmetry reduces the effect of offset voltage on the oscillator's period. This design uses an LM393 comparator for its relatively low maximum bias current of 25 nA. The comparator's output changes state when the integrator's output begins to exceed the threshold voltage set by hysteresis, reversing the direction of the OTA's output current and the threshold polarity. This action makes the integrator's slope reverse and initiates the next half-cycle.

You can calculate the oscillator's period as follows:

$$T=\frac{4I_{ABC}R_2C}{I_{INT}}=\frac{4(V_{IN}/R_{IN})R_2C}{V_{SUPPLY}/R_3}.$$

For the given component values,

$$T=\frac{4(V_{IN}/20\ k\Omega)(20\ k\Omega)\,10^{-7}}{15V/750\ k\Omega}=$$

$$0.02V_{IN}(SEC).$$

$$RATE=\frac{50}{V_{IN}}(Hz).$$

Potentiometer P_1 sets the full-scale period for $V_{IN}=10V$, and P_2 nulls the OTA's input offset voltage to optimize the performance at small values of V_{IN}. With the component values shown, the circuit covers a three-decade range from 200 µsec to 200 msec with lower than 1% linearity error. The error increases to 2% for T=100 µsec. With a 10-nF integrator capacitor, the circuit oscillates at frequencies as high as approximately 150 kHz (T=6.7 µsec). The CA3280 OTA provides the best performance in this circuit, thanks to its excellent offset specifications. Using the CA3080 and LM13600 in the circuit reduces performance. The integrator op amp should have low input-bias current and high-speed response to minimize ringing on triangle peaks. The AD843 and CA3140 both work well. You could add temperature compensation by including a thermistor in the OTA's input-attenuator circuit. Finally, note that you should use polystyrene or polypropylene capacitors in the integrator.

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design ideas

Edited by Bill Travis

Buck IC boosts battery voltage for white LED

Robert Kollman, Texas Instruments, Dallas, TX

White-light LEDs are finding their way into many markets that incandescent bulbs once served. Flashlights are among the newer applications in which reliability, ruggedness, and ability to control the power draw of the LEDs make these devices attractive. With incandescent bulbs, the power management for the device is a simple on-off switch. However, the LEDs cannot operate directly from the two cells you typically find in most flashlights, because their required voltage is 2.8 to 4V, compared with a battery voltage of 1.8 to 3V. The power management has a further complication because the light output of the LED relates to current, and the LED's characteristics are extremely nonlinear with voltage. One approach to this problem is to boost the power supply with a current limit. A number of devices for LED applications are available; however, their current ratings are typically too low for the 1 to 5W that flashlight applications need.

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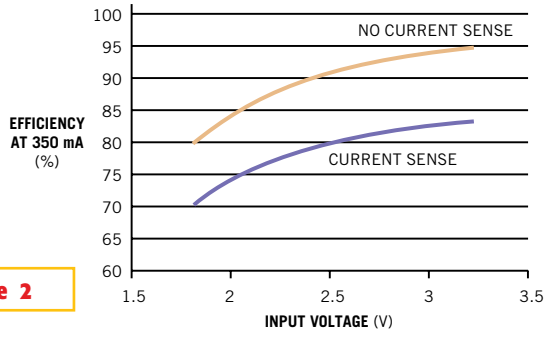

Figure 2

Resistive current sensing has an adverse effect on the efficiency of the circuit in Figure 1.

Figure 1 presents an alternative to the typical boost power regulator. A buck-converter IC, IC_1, generates the higher voltage that the white-light LED needs. An internal buck power stage connects between VIN and PGND, sourcing current to output Pin L. This circuit operates by turning on the high switch, thereby connecting the battery voltage across inductor L_1. Once inductor L_1 stores sufficient energy, the high-side switch turns off. The inductor current drives the switching node negative, and energy transfers through the low side into output capacitor C_1, creating an essentially lossless switching event. Also, because the high- and low-side switches are MOSFETs, voltage drop is lower than that of a diode implementation; therefore, efficiency can be high. The converter IC

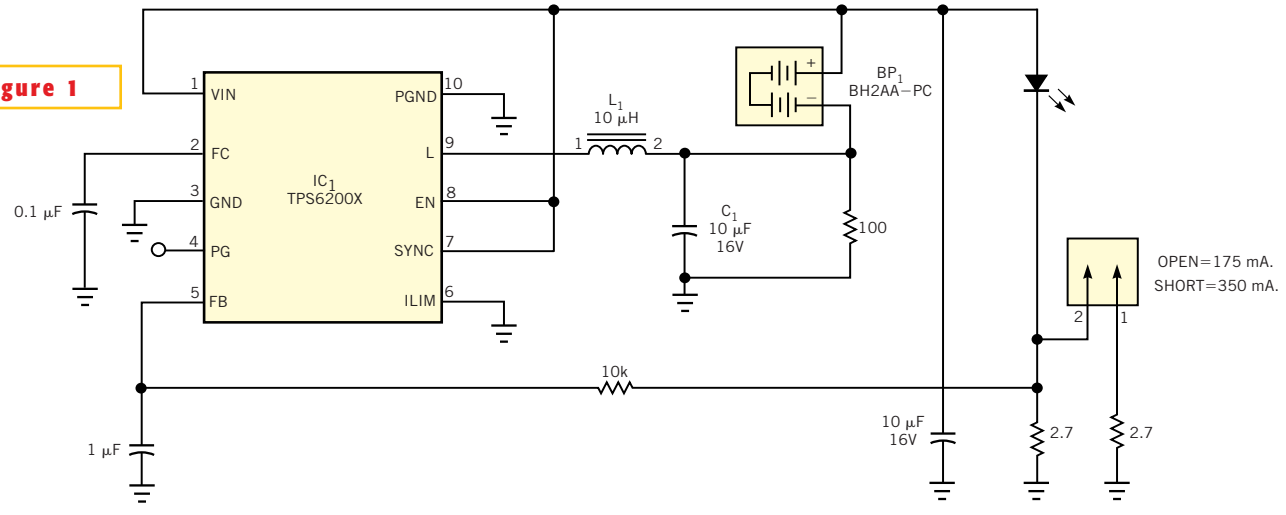

Figure 1

A buck-converter IC is a good choice for boosting voltages for white-LED drive.

monitors the current through the LED via a current-sense resistor and compares the current-sense voltage with an internal 0.45V reference within the converter IC to achieve regulation. Current and, therefore, illumination are functions of the current-sense resistor voltage. Although the internal reference voltage of the IC is lower than that of most other ICs, it does cause an appreciable power loss. With the LED voltage of 2.8 to 4V, it degrades efficiency by 10 to 14%. Reducing the resistor's value and using an amplifier to sense the current at a lower voltage could reduce this loss.

Figure 2 shows load-current regulation and boost voltage at a 350-mA current setpoint. Efficiency is 80% or better over the normal battery-voltage range but falls as battery voltage drops to end-of-life values. Also, the **figure** shows the impact of the resistive-current sensing. At high input voltages, the efficiency approaches 95%, and, at low input voltages, it falls to 80%. The trend for the curves stems from two interrelated effects: At high input voltage, input current and, hence, switch current are low. Therefore, conduction and switching losses are low. Second, much like an autotransformer, the boost power stage does not handle the total output power. The amount of power that the power stage handles relates to the boost voltage, or the difference between the input voltage and the LED voltage. In this design, the LED voltage is approximately 3.7V, so that at high line of 3.2V, the power stage handles only 13% ((3.7−3.2)/3.7) of the power. At low line, in which the currents are much higher, the power stage handles almost four times as much, or 50%, of the power. Although a buck controller is not an obvious choice for this application, it provides low-cost, low-input-voltage operation and good efficiency over a wide input-voltage variation.

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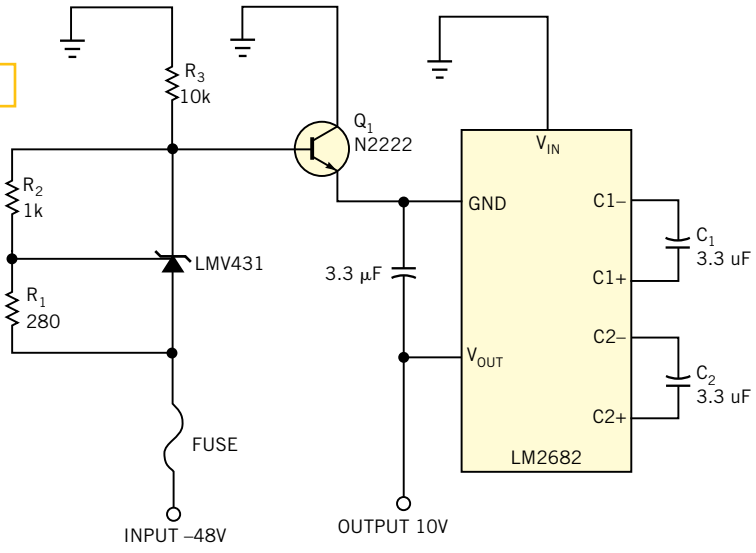
Switched-capacitor IC and reference form elegant −48 to +10V converter

Wallace Ly, National Semiconductor, Santa Clara, CA

A system designer must almost always face a trade-off in choosing the right part for an application. The trade-off usually involves performance, price, and function. An example is the issue of powering circuits from a telecom-voltage source. Telecom systems almost exclusively use high-potential negative rails, such as −48V. Digital circuits typically in use in such applications usually operate from a "brick"-type power supply. However, analog circuits rarely require enough power to justify using a costly brick. At the heart of these bricks is nothing more than a specialized switching converter in tandem with an isolated flyback-transformer coil. But some applications neither require nor can tolerate the use of a coil-based approach. **Figure 1** depicts a way to address the problem. The circuit provides a small amount of power to analog/digital circuits, such as the LMH6672 DSL op amp.

Figure 1



This simple circuit provides a 10V power source from −48V telecom power rails.

The LMV431 voltage reference, along with the voltage-setting resistors sets the output voltage to approximately (1+1 kΩ/280Ω)×1.24V~−5.7V. This output voltage then goes to the base of Q_1, the 2N2222 transistor. The configuration of the transistor causes a V_{BE} drop of approximately 0.7V, resulting in a net voltage of −5V for the next stage. The purpose of the transistor is to provide additional current to the LM2682 switched-capacitor converter. Note that the converter has a −5V reference (GND pin). Small capacitors C_1 and C_2 enable the pumping and inverting action required to convert the −5V to 10V. Furthermore, the MSO-8 package of the LM2682 and the SOT-23-3 package of the LMV431 allow the circuit to consume little board space. In roughly the size of a small transformer, the proposed circuit does an elegant job of powering low-power circuits from a negative high-voltage source.

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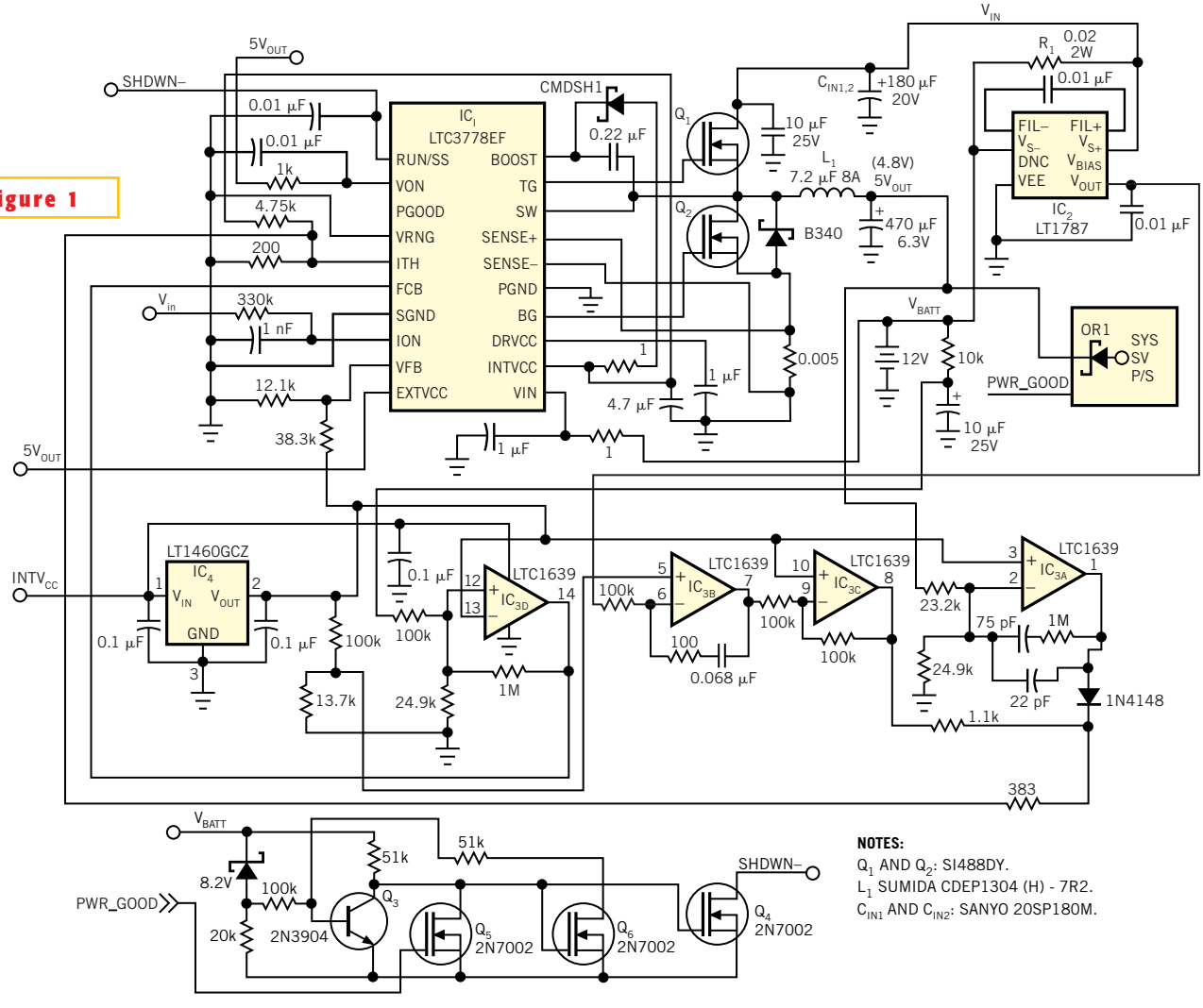
Buck converter handles battery-backup system

Haresh Patel, Linear Technology Corp, Milpitas, CA

Asynchronous buck converter is inherently bidirectional. That is, it transfers energy from input to output as a buck regulator when the output voltage is low, but, when the output voltage is *high*, the converter acts as a boost regulator, transferring power from output to input. This Design Idea shows how to use this bidirectional energy transfer to automatically recharge a battery when the main 5V supply is available in a battery-backed 5V system. The circuit in **Figure 1** provides as much as 7A current at 5V output set at 4.8V and recharges a 12V sealed lead-acid battery with a current as high as 2A. The basic concept is that the ITH-pin voltage of the LTC3778 controls the L_1 inductor current, or the valley level. Above approximately 0.7V at the ITH pin, the net inductor current is positive from input to output. Below that level, the inductor current becomes increasingly negative, resulting in a boost function that transfers energy from output to input. When the FCB pin of the LTC3778 is high, the IC inhibits negative inductor current and the boost function by turning off the bottom MOSFET.

Figure 2 shows a 5V power supply backed up by a battery-powered, LTC-3778-controlled power supply. The synchronous, bidirectional LTC3778 buck circuit acts as a battery-to-5V converter if the main 5V supply is off and as a battery charger when the 5V supply is alive. As **Figure 1** shows, in the charging mode, the circuit regulates the battery current by sensing the charge current through R_1 by means of an LT1787 current-sense

Figure 1



NOTES:
Q_1 AND Q_2: SI488DY.
L_1 SUMIDA CDEP1304 (H) - 7R2.
C_{IN1} AND C_{IN2}: SANYO 20SP180M.

This bidirectional converter automatically recharges a battery when the 5V main supply is active.

amplifier, IC_2. An error amplifier, IC_{3B} and IC_{3C}, compares the current-sense signal with a reference voltage from the LT1460GCZ, IC_4, and drives the ITH pin of IC_1. When the ITH-pin voltage falls lower than approximately 0.7V, the circuit forces the average inductor current to a negative value, causing reverse power flow from the output to the input of the LTC3778, thereby charging the battery. The lower the voltage at the ITH pin, the higher the charge current.

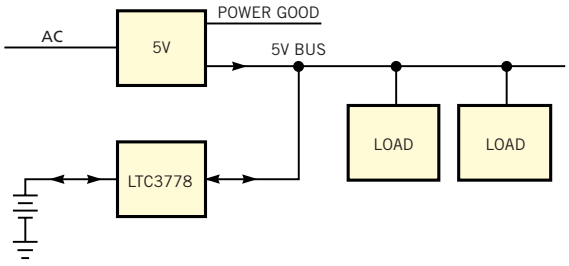


Figure 2

The battery charges when the 5V main supply is alive and provides 5V power when the main supply goes down.

At the beginning of the charge cycle, a constant current charges the battery. When the battery voltage reaches 13.8V, IC_{3D} pulls the FCB pin of IC_1 high, thereby not allowing Q_2 to turn on. So, the circuit inhibits boost mode regardless of the level at the ITH pin. The interruption in charging current causes the battery voltage to drop below 13.2V to restart charging. This action results in pulse charging with the pulse frequency gradually decreasing until the battery fully charges. In the backup mode, IC_{3A} senses the output-voltage drop to 4.8V and drives the ITH pin to maintain the output voltage at 4.8V. The recharging resumes when the system's 5V power returns and the 5V bus goes higher than 4.8V. In this scheme, the main supply voltage must be slightly higher than the backup-supply voltage for proper switchover. Approximately 100 to 200 mV should be adequate to prevent unnecessary mode switching attributable to ripple.

If the lower voltage in the backup mode is objectionable, then you can use a power-good signal from the main supply to change the reference voltage to the desired value when the power-good signal is low. Q_3 through Q_6 prevent low-battery discharge by shutting down IC_1 when the battery voltage is low and the power-good signal from the main supply is inactive. You could implement more sophisticated charging algorithms using a system microcontroller or analog circuitry that sets the charge current as a function of battery voltage. You can implement float charging by reducing the charge current to approximately 100 mA when the battery is nearly fully charged. A gradually tapering charge current can mimic constant-voltage charging as a alternative to pulse charging. The circuit can use a three-cell (in series) lithium-ion battery if you set the maximum voltage to 12.6V.

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Circuit disconnects load from low-voltage supply

Steve Caldwell, Maxim Integrated Products, Chandler, AZ

Power supplies often include a circuit that disconnects the load when the supply voltage drops too low, such as when a battery is nearly discharged. A p-channel MOSFET connected between supply and load is the typical approach. However, a 1.5V single-cell battery or other low-voltage supply is insufficient to fully turn on the MOSFET. For such low-voltage systems, consider the circuit of **Figure 1**. A small inverting charge pump, IC_1, generates a negative voltage approximately equal to the input supply, V_{CC}. That voltage connects to the ground terminal of a microprocessor supervisor, IC_2, which monitors the voltage difference between its own V_{CC} and ground pins. As long as this difference is greater than the supervisor's internal trip-voltage threshold, the reset output voltage assumes the charge-pump output voltage of approximately $-2V_{CC}$, which provides a gate-source voltage adequate to keep the MOSFET on. When the monitored voltage drops below the threshold of the supervisor, its reset output goes up to V_{CC} and turns off the MOSFET. The supervisor has a threshold of 2.6V. Because the voltage it detects is twice the supply voltage, this circuit disconnects the load when the supply voltage drops below 1.3V, making it suitable for use with a typical 1.5V battery. Other internal threshold voltages are available.

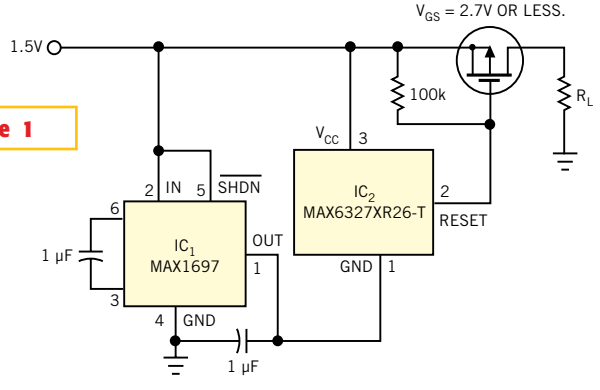

Figure 1

This low-voltage circuit disconnects the load when the supply voltage drops below a predetermined threshold of 1.3V in this case.

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Circuit forms gamma-photon detector

Bruce Denmark, Maxim Integrated Products, Sunnyvale, CA

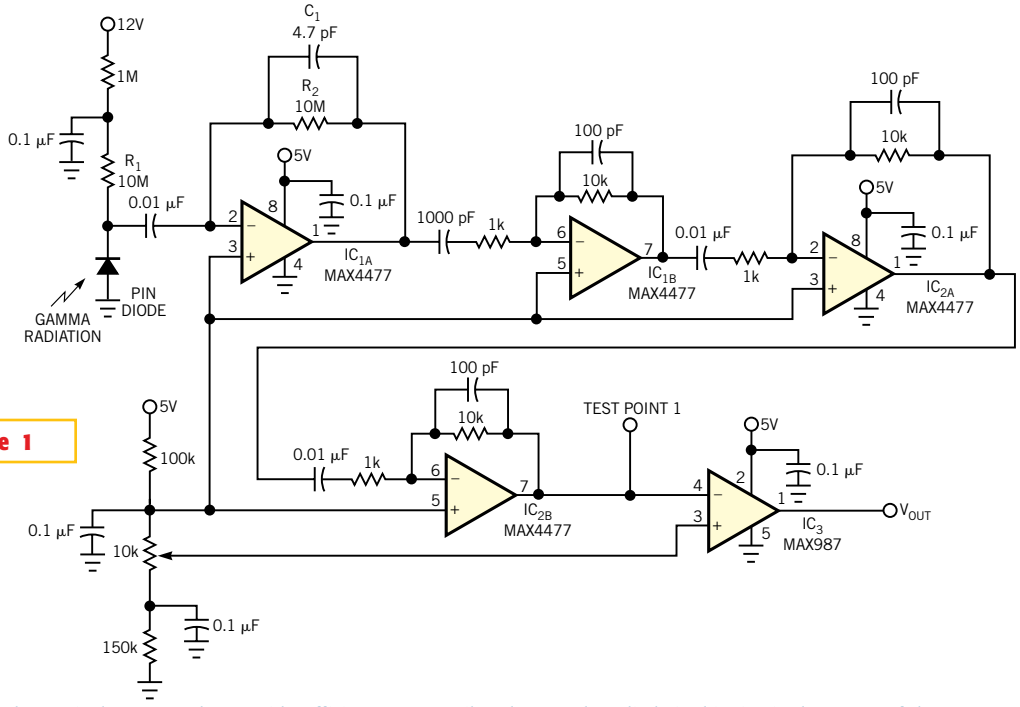


Figure 1

When a single gamma photon with sufficient energy strikes the PIN photodiode in this circuit, the output of the comparator pulses high.

THE CIRCUIT of **Figure 1** includes a PIN photodiode that detects individual photons of gamma radiation. The reverse bias on the photodiode sometimes creates a depletion region. When such a photon strikes this depletion region, a small amount of charge develops. This charge is proportional to the photon's energy. Four amplifiers following the PIN photodiode amplify and filter the resulting signal. A final comparator distinguishes between the signal and the noise. Thus, the comparator's output pulses high each time a gamma photon with sufficient energy strikes the photodiode. Small signal levels make this design an interesting challenge. The design requires very-low-noise circuitry because the individual gamma photons generate a small amount of charge and because lowering the overall noise level allows the circuit to detect lower energy gamma photons. You must pay special attention to the first stage, which is the most noise-critical.

The most critical component is the PIN photodiode, whose selection often involves conflicting considerations. Detector sensitivity (the number of photons detected for a given radiation field), for example, depends on the size of the depletion region, which in turn depends on the area of the diode and the reverse bias applied to the diode. To maximize sensitivity, therefore, you should choose a large-area detector with high reverse bias. Large-area detectors tend to have high capacitance, which increases the noise gain of the circuit. Similarly, a high bias voltage means high leakage current. Leakage current also generates noise. The circuit in **Figure 1** includes the QSE773 PIN photodiode from Fairchild (www.fairchildsemi.com). Though readily available and inexpensive, it is probably not the optimal choice. Certain PIN diodes from Hamamatsu (www.hamamatsu.com) can work nicely in this application. Choosing a detector with 25- to 50-pF capacitance with reverse bias applied provides a fair compromise between sensitivity and noise.

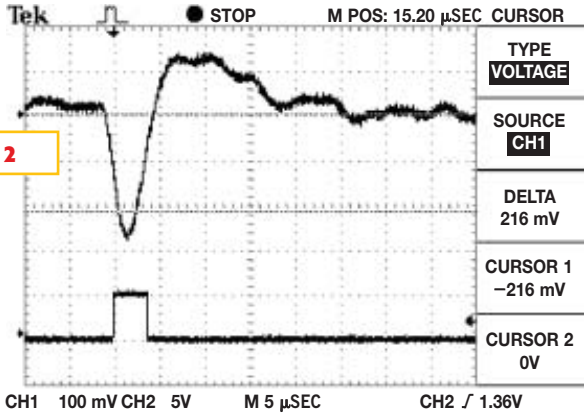
Important considerations for the first-stage op amp include input-voltage noise, input-current noise, and input capacitance. Input-current noise is directly in the signal path, so the op amp should keep that parameter to a minimum. JFET- or CMOS-input op amps are a must. Also, if possible, the op amp's input capacitance should be smaller than that of the PIN photodiode. If you use a high-quality PIN photodiode and an op amp with low current noise and pay careful attention to design, the limiting factor for noise should be the first-stage op amp's input-voltage noise multiplied by the total capacitance at the op amp's inverting node. That capacitance includes the PIN-photodiode capacitance; the op-amp input capacitance; and the feedback capacitance, C_1. Thus, to minimize circuit noise, minimize the op amp's input-voltage noise. The op amp in this circuit, IC_{1A}, a MAX4477, well suits this design. It has negligible input-current noise and low input-voltage noise of 3.5 to 4.5 $nV/\sqrt{Hz}$ at the critical frequencies of 10 to 200 kHz. Its input capacitance is 10 pF.

R_1 and R_2 contribute equally to noise because they are directly in the signal path. Resistor-current noise is inversely proportional to the square root of the resistance, so use as large a resistance value as the circuit can tolerate. Keep in mind, though, that leakage current from the PIN diode and first-stage op amp place a practical limit on how large the resistance can be. The MAX4477's maximum leakage current is only 150 pA, so R_2 could be much larger than the 10 MΩ shown. R_1 can also be substantially larger when the circuit operates with a high-quality

PIN photodiode. C_1 affects the circuit gain, and smaller values benefit both noise and gain. Use a capacitor with low temperature coefficient to avoid gain changes with temperature. This capacitance value also affects the requirement for gain-bandwidth product in the op amp. Smaller capacitance values require a higher gain-bandwidth product.

To ensure that the circuit measures gamma radiation and not light, cover the PIN photodiode with an opaque material. To block radiated emission from power lines, computer monitors, and other extraneous sources, be sure to shield the circuit with a grounded enclosure. You can test the circuit by using an inexpensive smoke detector. The ionizing types of smoke detectors use americium 241, which emits a 60-keV gamma photon. (The more expensive photoelectric smoke detectors do not contain americium.) A 60-keV gamma is close to the circuit's noise floor but should be detectable. A graph shows the result of a typical gamma strike (**Figure 2**). The top waveform is from Test Point 1, and the bottom waveform represents the comparator's output. A possible improvement would be to replace C_1 with a digitally trimmable capacitor, such as the MAX1474, which provides the circuit with digitally programmable gain. Similarly, replacing the mechanical potentiometer with a digital potentiometer, such as the MAX5403 allows digital adjustment of the comparator threshold. Finally, driving the comparator's noninverting input with a reference instead of the 5V supply improves the comparator's threshold stability.

Figure 2



These waveforms from the Figure 1 circuit show the signal at Test Point 1 (top trace) when a gamma photon strikes the PIN photodiode, and the resulting comparator output (bottom trace).

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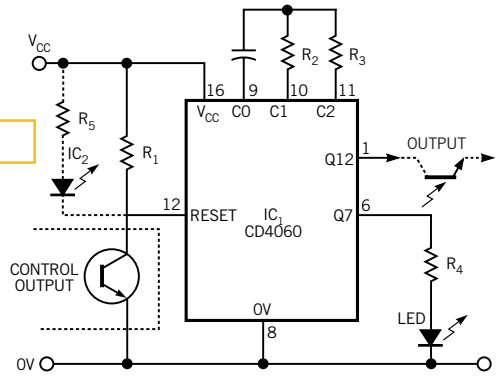
Circuit ensures safety in power-on operation

Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

Computers find universal use in industrial-control systems. During power- and start-up sequences (booting), the outputs of such control systems may yield uncontrolled pulses before the software defines the correct status. If these outputs control the power-on state of a system, these uncontrolled pulses could have dramatic consequences. Safety regulations forbid such erratic behavior. The circuit in **Figure 1** is a cost-effective approach to the spurious-pulse problem. The circuit costs approximately 10 times less than other available timers. The open-collector output of the controlling device connects to the reset input of the CD4060 counter, IC_1. You can easily adapt this circuit to other controller-output configurations, such as an optocoupler. As long as R_1 pulls the reset input high (controller-output off), the counter's clock stays disabled and all outputs are low. C, R_2, and R_3 are the timing components for IC_1. With $R_2=R_3=10\,k\Omega$ and $C=0.1\,\mu F$, the measured clock frequency is approximately 360 Hz.

The output of the circuit is Q12. The reset input must stay low longer than $T=(2^{n-1})/f=(2048)/360=5$ sec for the output to turn on (n is the output number, 12). Any spurious pulse from the controller's output that is shorter than 5 sec has no effect on the output of the circuit. Output Q13 of the counter turns on after 11 sec, Q14 after 23 sec, and so on. The LED, connected to Q7 through R_4, flashes during the timing period. With $V_{CC}=12V$ and an LED current of 10 mA, $R_4=(V_{CC}-2)/10=1\,k\Omega$. For safety reasons, you can add the optocoupler, IC_2. If output Q12 of the counter fails (shorted to V_{CC}), the output turns on only if the controller's output is on. Choose the value of R_1 depending on the controller's output and the noise level; in this design, $R_1=10\,k\Omega$. Note that V_{CC} should have a maximum value of 15V for the CD4060 and 6V for the 74HC4060.

Figure 1



This simple timing circuit ensures that a controller's spurious pulses do not affect a system's start-up operation.

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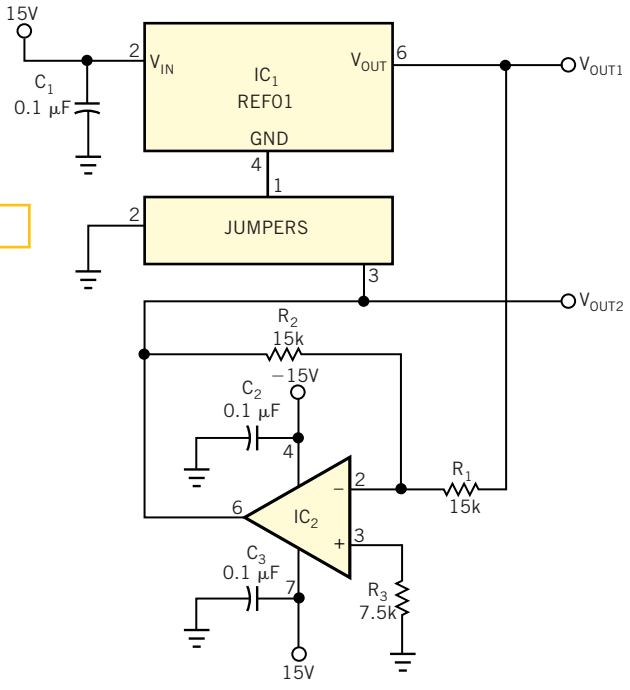
Edited by Bill Travis

Supply delivers pin-programmable multiple references

V Manoharan, Kochi, India

In the circuit of **Figure 1**, the REF01, IC_1, is a buried-zener-diode-based, precision 10V reference that features minimal noise and drift over temperature. The circuit provides not only the 10V output of the REF01, but also a 5V output that a REF02 reference would deliver. In addition, the circuit provides −5V, −10V, and an unbalanced dual reference, the sum of whose voltages is precisely 10V. In addition to the REF01, the circuit uses a highly precise, unity-gain inverting amplifier, IC_2. **Tables 1** and **2** define the output voltages as a function of the jumper connections and as a function of the optional use of a REF02 reference in place of the REF01. In **Figure 1**, assume the use of a REF01 reference, and that Point 1 connects to Point 2. (Pin 4 of IC_1 connects to ground.) IC_2 inverts the 10V output of IC_1 to deliver −10V at V_{OUT2}.

Figure 1



This pin-configurable voltage reference delivers a variety of positive and negative output voltages.

Now assume that Point 1 connects to Point 3. (Pin 4 of IC_1 connects to the output of IC_2). If V_{OUT1} is at X volts, V_{OUT2} assumes a level of −X volts. The REF01 forces exactly 10V between its output and Pin 4. Therefore, X−(−X)=10, 2X=10, and X=5V. In this arrangement, 5V and −5V are simultaneously available at V_{OUT1} and V_{OUT2}, respectively. To obtain precisely −5V at V_{OUT2}, you must ratio-match R_1 and R_2 and also match their temperature coefficients. Now assume $R_2/R_1=A$ and Point 1 connects to Point 3. In this case, the gain of the inverting amplifier is A. Therefore, V_{OUT1} and V_{OUT2} deliver unbalanced outputs, the sum of which is 10V. You can easily derive that $V_{OUT1}=10/(1+A)$ and $V_{OUT2}=-10A/(1+A)$.

The flexibility of this circuit eliminates the need to design and inventory several voltage sources. Moreover, the circuit can serve as a dual reference. The circuit finds application in D/A converters needing external references, portable instruments, digital multimeters, and A/D converters. It is advisable to use the ultralow-offset-voltage OP07 or ultralow-noise OP27 for the inverting amplifier.□

TABLE 1–AVAILABLE OUTPUT VOLTAGES

Device IC_1	Jumper connection	V_{OUT1} (V)	V_{OUT2} (V)
REF01	1 to 2	10	−10
REF01	1 to 3	5	−5
REF02	1 to 2	5	−5
REF02	1 to 3	2.5	−2.5

TABLE 2–UNBALANCED OUTPUT VOLTAGES

Device IC_1	R_2/R_1	V_{OUT1}	V_{OUT2}
REF01	A	10/(1+A)	−10A/(1+A)
REF02	A	5/(1+A)	−5A/(1+A)

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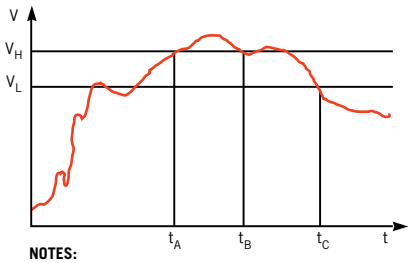
Design an efficient reset circuit

Guillermo Bosque, Asesoría e Integracion de Tecnologías, Urduliz, Spain

When you work with microprocessors, you must ensure that when the power-supply voltage fluctuates to the minimum permissible level, V_L, that the processor's ALU continues to operate normally. Also, when you switch on the power supply, the ALU must operate normally when the supply voltage equals or exceeds a certain high level, V_H. The minimum and high levels constitute a hysteresis band ($V_{HYST}=V_H-V_L$), and fluctuations in supply voltage within this band should not perturb the logic operations of the processor (**Figure 1**). A properly designed reset circuit can ensure proper operation of a microprocessor. One requirement of an efficient reset circuit is that it operates properly over the intended temperature range—for example, −40 to +85°C. Several reset circuits are available that meet the voltage conditions, but the temperature constraints render them unsatisfactory. This Design Idea proposes a small, inexpensive reset-circuit structure.



NOTES:
IF $t < t_A$, THEN RESET.
IF $t_B - t_A > t_{MIN}$, THEN THE RESET DISAPPEARS.
t_C: RESET INSTANT APPEARS.

Figure 1

A proper reset signal plays an important role in microprocessor operation.

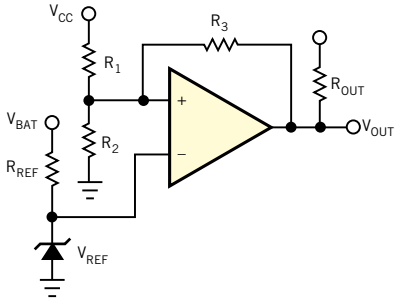


Figure 2

This comparator has built-in hysteresis to provide a reset signal when the supply voltage falls outside the limit band.

To obtain V_{REF} by using a battery voltage, V_{BAT}, but V_{CC} would work as well. The pullup resistor, R_{OUT}, is necessary to obtain a positive voltage at the output, because the comparator's output has an open-collector or open-drain structure. The following approximate and exact equations are based on selection of V_H and V_L. (Remember that $V_{HYST}=V_H-V_L$.)

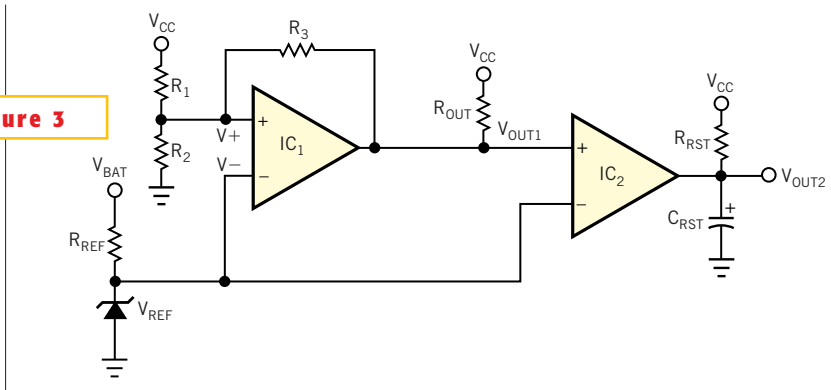


Figure 3

This circuit introduces a time constant in the reset function.

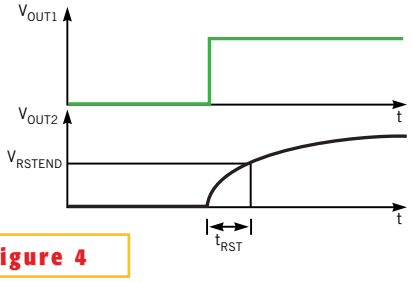


Figure 4

The reset signal ends after one time constant in the circuit of Figure 3.

APPROXIMATE EQUATIONS	EXACT EQUATIONS
$R_1 = R_2\left(\frac{V_L}{V_{REF}} - 1\right)$.	$\frac{R_2 + R_3}{R_2 R_3} = \frac{1}{R_1}\left(\frac{V_H}{V_{REF}} - 1\right)$.
$R_3 = R_2\left(\frac{V_L - V_{REF}}{V_{HYST}}\right)$.	$\frac{R_1(R_3 + R_{OUT})}{R_1 + R_3 + R_{OUT}} = R_2\left(\frac{V_L}{V_{REF}} - 1\right)$.

In the approximate equations, you disregard R_{OUT}, because its value is negligible.

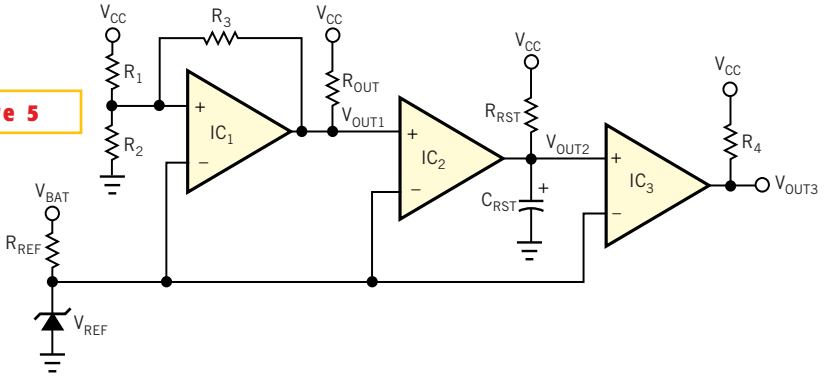


Figure 5

The additional comparator in Figure 5 switches when the exponential signal reaches V_{REF}.

ble compared with that of R_3. But the value of R_{OUT} affects V_L, because R_{OUT} and R_3 are additive when the comparator is in the high-impedance (off) state. Choosing values for V_{HYST} and V_L and knowing V_{REF}, you obtain the following approximations: $R_1=R_2(V_L/V_{REF}-1)$, and $R_3=R_1(V_{REF}/V_{HYST})$. Now, you add a timing circuit to the hysteretic comparator (**Figure 3**). When V_{OUT1} assumes a low level, V_{OUT2} switches to a low level and discharges C_{RST}. When V_{OUT1} switches high, comparator IC_2 switches to its high-impedance state, and C_{RST} begins to charge through R_{RST}. V_{OUT2} follows an exponential curve and arrives at a value, V_{RSTEND}, which signals the end of the reset signal (**Figure 4**). You can modify the t_{RST} by adjusting the values of C_{RST} and R_{RST}. Now, if you add another comparator, IC_3 (**Figure 5**), you obtain the waveforms of **Figure 6**.

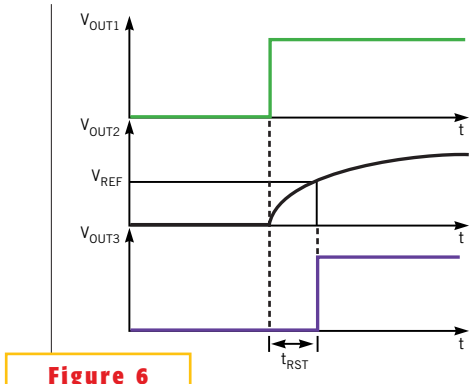
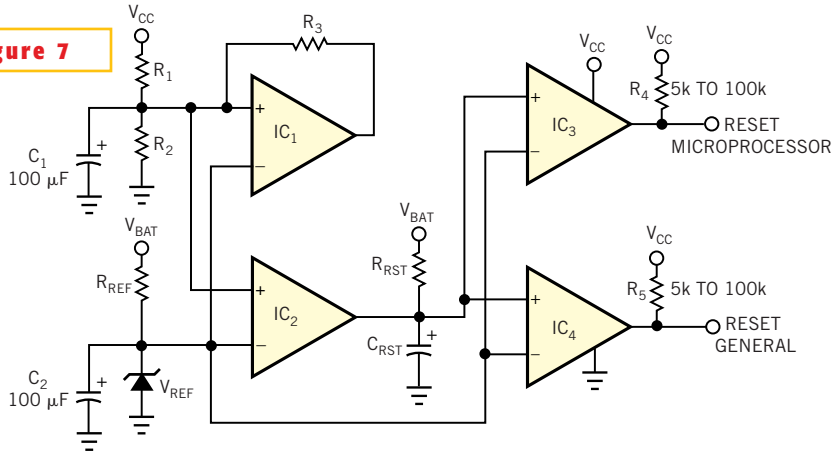


Figure 6

One additional comparator produces a positive signal at the processor's reset port.

Figure 7



The complete reset circuit can handle microprocessors and other circuitry.

The final reset circuit appears in **Figure 7**. The circuit has four comparators, one voltage reference, seven resistors, and three capacitors. To determine the resistor values, you can use the following equations: $R_1=R_2(V_L/V_{REF}-1)$, and $R_3=R_1(V_{REF}/V_{HYST})$. An appropriate comparator IC is the quad LM239 (−25 to +85°C) or the LM139 (−55 to +125°C). The voltage reference is the 1.2V ICL8069CMSQ (−55 to +125°C). C_1 and C_2 stabilize high-frequency fluctuations and have values of 100 nF and 10 µF, respectively. R_{REF} has a value of 50 kΩ, and R_4 and R_5 have values of 5 to 100 kΩ, depending on the circuit you wish to control. If you chose $V_L=4.75V$, $V_{HYST}=0.1V$, and $R_2=10$ kΩ, you obtain $R_1=29.6$ kΩ and $R_3=355$ kΩ. For timing the reset, you use the capacitor-charging equation, $V=V_{CC}(1-e^{-t/RRST/CRST})$.

The final instant of reset occurs when $V=V_{REF}=1.2V$. Choose 5V for V_{CC}. The equation then becomes $t=-R_{RST}C_{RST}\ln(1-V/V_{CC})$. If you choose t=1 sec and $C_{RST}=10$ µF, then

$$R_{RST}=\frac{t}{C_{RST}\left(1-\frac{V}{V_{CC}}\right)}.$$

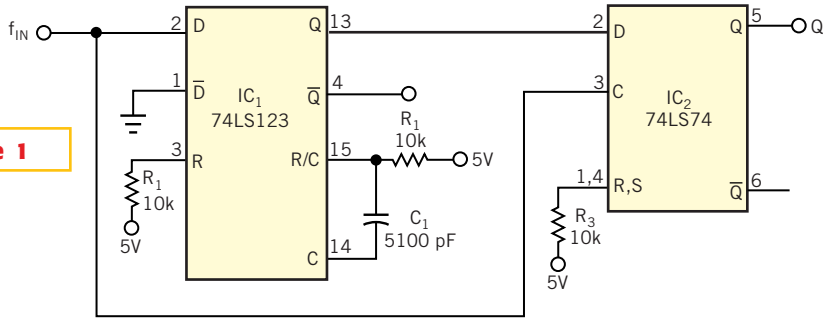
You obtain $R_{RST}=36.4$ kΩ. If $C_{RST}=1$ µF, then $R_{RST}=364$ kΩ. It's preferable to have a low value for C_{RST} because of the low current in the comparator's output transistor. Solving for R_2, you obtain $R_2=10$ kΩ.□

One-shot provides frequency discrimination

Victor Aksenenka, CSRI Elektropribor, St Petersburg, Russia

You use a frequency discriminator to compare one signal frequency with another one. A functional feature, retriggering, of a monostable, one-shot 74xx123 multivibrator can yield frequency discrimination. **Figure 1** shows a frequency discriminator that determines the relation of input-pulse frequency to a reference frequency. The external components, R_1 and C_1, set the reference frequency. These values determine the 74xx123's reference frequen-

Figure 1



This simple circuit can reveal whether an input frequency is above or below a reference frequency.

cy as follows: $f_R=1/t_W$, and $t_W=kR_1C_1$. The multiplication factor k depends on C_1's value and the power-supply voltage. The rising edge of the input pulse starts the one-shot, whose output switches high for the interval t_W. The same pulse edge sets the 74xx174 flip-flop to the same state as the output of the one-shot. If the interval between pulses is longer than t_W, the next pulse arrives after the one-shot returns to its initial state. The one-shot's output is low, and the rising edge of the input pulse sets the flip-flop low. The low flip-flop output indicates that the input-pulse frequency, f_{IN}, is lower than f_R.

If the interval between input pulses is shorter than t_W, the next pulse arrives before the one-shot completes its cycle and returns to its initial state. The one-shot's output is high, and the rising edge of the input pulse sets the flip-flop high. A high flip-flop output indicates that the input-pulse frequency, f_{IN}, is higher than f_R. Doubling the circuit in **Figure 1** implements frequency discrimination with a "window" characteristic (**Figure 2**). Two pairs of R and C values determine the lower and upper reference frequencies. An exclusive-OR circuit takes the outputs of the upper and lower flip-flops. The exclusive OR's output is high when f_{IN} is between f_{RL} and f_{RH}. When f_{IN} is outside the frequency band f_{RL} to f_{RH} the exclusive OR's output is low. **Figure 3** shows the frequency-discrimination characteristic. With R and C values as in **Figure 2**, and the use of a 74LS123 one-shot, f_{RL}=16 kHz, and f_{RH}=46 kHz. Other types of one-shots could produce different results.□

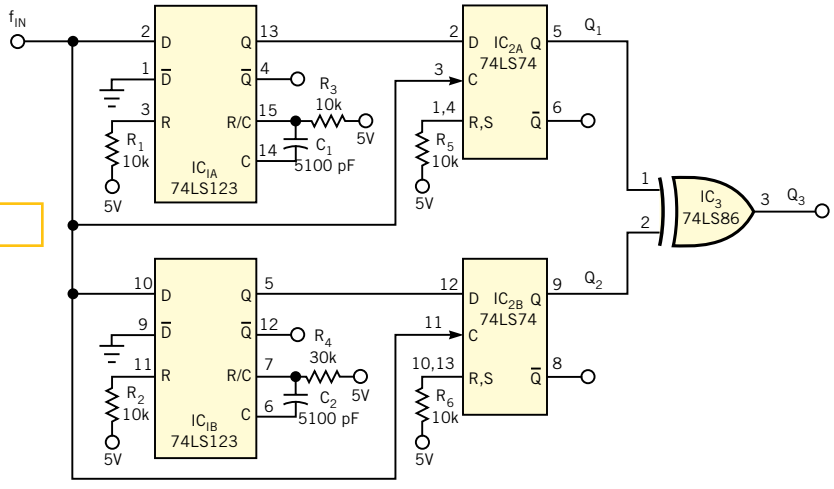


Figure 2

Doubling the circuit in Figure 1 and using an exclusive-OR circuit results in a window discriminator.

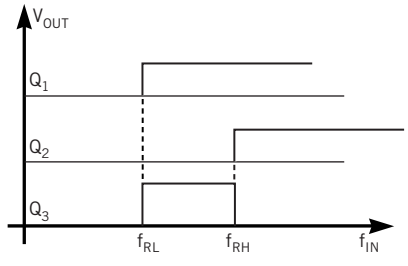


Figure 3

The output of the exclusive-OR circuit in Figure 2 is high only when the input frequency is between defined limits.

Circuit forms novel floating current source

S Casans, AE Navarro, and D Ramirez, University of Valencia, Burjassot, Spain

FIGURE 1 SHOWS A POLARIZATION circuit applicable to ISFET (ion-sensitive field-effect-transistor) sensors. ISFETs are solid-state chemical sensors that measure the pH value of a solution in biomedical and environmental applications, for example. The circuit in **Figure 1** is extremely simple; it sets fixed-bias conditions for ISFET sensors ($V_{DS}=I_0R_X$; $I_{DS}=I_0$). When a sensor needs characterization, you must modify the bias conditions, thus increasing the cost and the complexity of the bias circuit. The low-cost auxiliary module in **Figure 2** implements a novel, voltage-controlled floating current source. The current range covers the interval 0 to 100 µA. You implement this module to control the ISFET sensor's bias voltage, but you can apply it to any sensor that needs bias of 100 µA or lower. The floating current source uses three operational amplifiers, all portions of a Texas Instruments (www.ti.com) TL084. The cur-

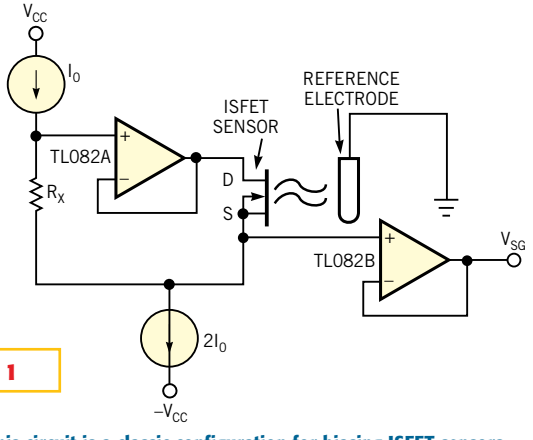
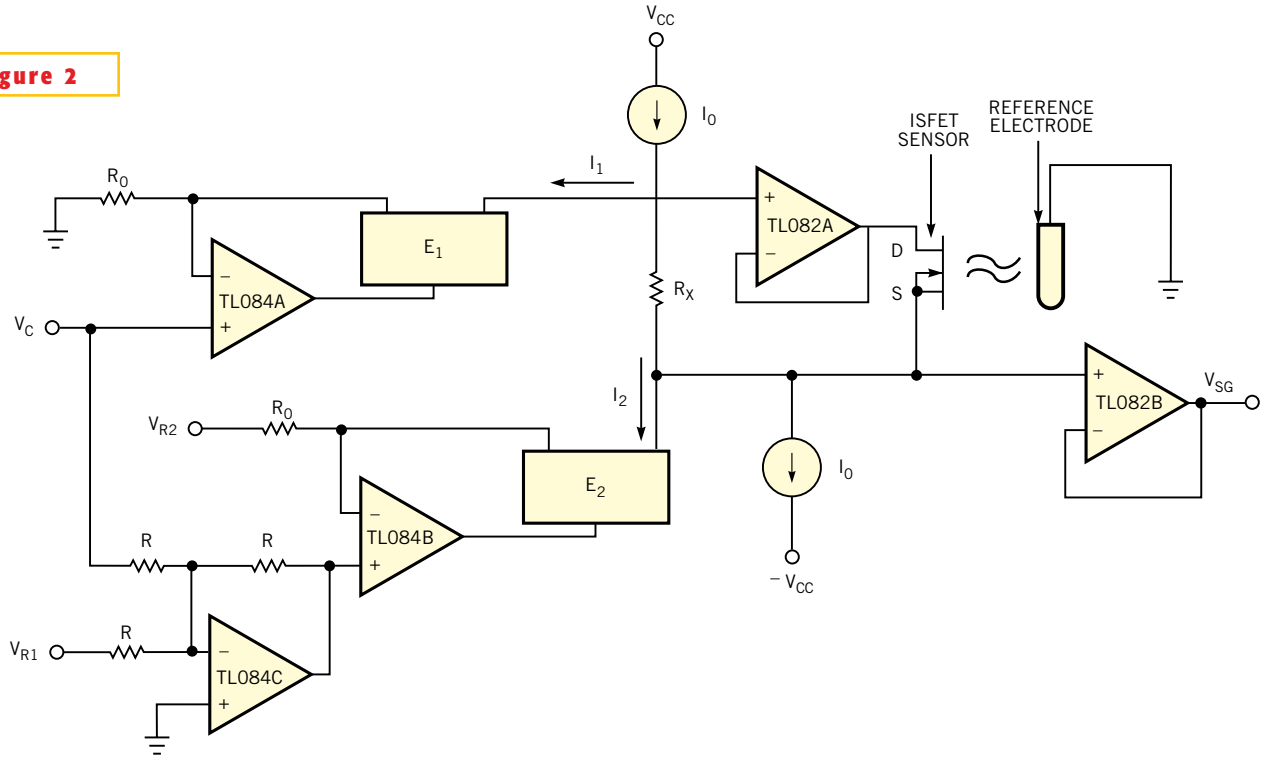


Figure 1

This circuit is a classic configuration for biasing ISFET sensors.

Figure 2



This novel floating current source represents an improved way to bias ISFET sensors.

rent sources (I_0) and the current mirrors (E_1 and E_2)use the Burr-Brown (www.ti.com) REF200. The REF200 has two 100-µA floating current sources (I_0) and one current mirror E_i (i=1, 2). The V_{R1} and V_{R2} voltages compensate the deviations arising from the operational amplifiers' offset voltages and the resistor tolerances. The V_C voltage controls the currents I_1 and I_2; therefore, in the circuit in **Figure 2**, V_C controls the sensor bias voltage V_{DS}.

Figures 3 and **4** show the measured absolute errors occurring in the bias current and voltage, respectively. The main advantages of this current source are that it floats and that you can connect it to any circuit without changing its operating mode, because the currents I_1 and I_2 are complementary. Therefore, if I_1 diminishes, the I_2 current increases in the same proportion, and this action does not affect the other currents in the circuit. In the ISFET-sensor case, changing I_2 via V_C allows you to vary the bias voltage applied to the sensor without changing the bias current, I_{DS}.□

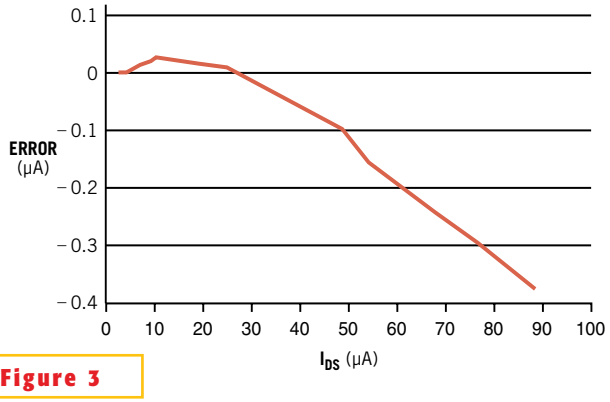


Figure 3

Very small measured errors appear in the ISFET's bias current.

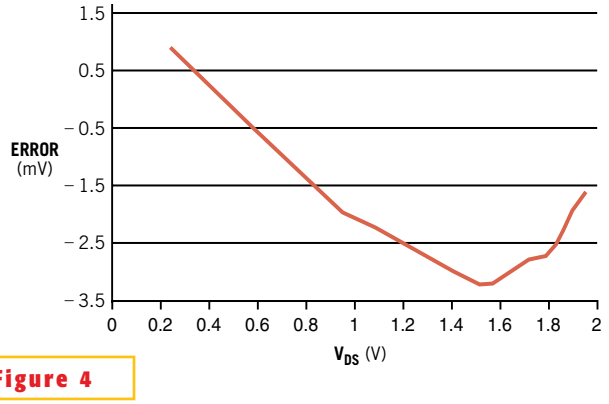


Figure 4

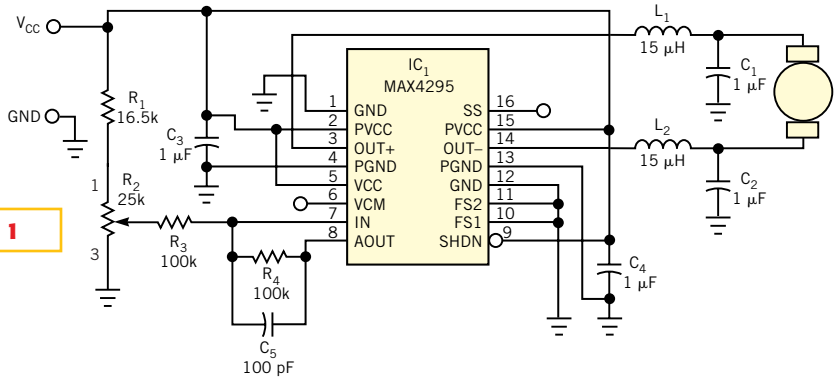
Only a few millivolts of error appear over the full range of V_{DS}.

Circuit provides Class D motor control

John Guy, Maxim Integrated Products, Sunnyvale, CA

Class D audio amplifiers provide a dual benefit for battery-powered portable devices. They enhance battery life, and they produce much less power dissipation than do their linear cousins. Those features make Class D amplifiers ideal candidates for controlling speed and direction in small electric motors. The standard application circuit for a Class D audio amplifier, IC_1, requires only slight modifications. In place of the usual audio-signal input is a variable dc voltage that potentiometer R_2 generates. Resistor R_1 biases the potentiometer to match the input range of IC_1. Full-counterclockwise rotation of the potentiometer corresponds to maximum-speed reverse rotation of the motor. Midscale on the potentiometer corresponds to motor off, and full-clockwise rotation of the potentiometer produces maximum-speed forward rotation in the motor. The characteristics of a given motor may allow you to eliminate the amplifier's output filter, which comprises L_1, L_2, C_1, and C_2. But, unless the control circuitry is near the motor, you should include the filter to reduce EMI.□

Figure 1



A Class D audio amplifier, IC_1, helps implement this simple motor-speed controller.

design ideas

Edited by Bill Travis

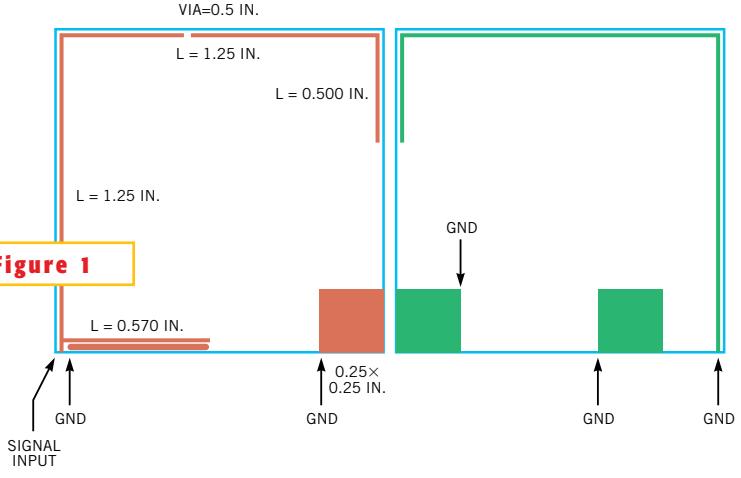
Small, 915-MHz antenna beats monopole

Dave Cuthbert and Bob Casiano, Micron Technology, Boise, ID

A 915-MHz data-acquisition project required a small antenna, but the available antennas lacked the necessary characteristics: efficiency, compactness—that is, smaller than a standard 3-in. monopole—with adequate bandwidth, and with amenability to modeling by inexpensive NEC-2 antenna software. (To learn more about NEC antenna software, go to www.nittany-scientific.com/nec.) The result of this design effort, called the "Tab" antenna for its square shape has the following characteristics:

- a square shape, 1.25 in. per side (0.1 wavelengths);
- the ability to be constructed in FR-4 pc board;
- linear polarization;
- a 2-to-1 VSWR (voltage-standing-wave-ratio) bandwidth of 46 MHz (5% bandwidth);
- the ability to be mounted parallel or perpendicular to a pc board;
- enhanced suppression of second- and third-harmonic radiation; and
- the ability to be mechanically trimmable to resonance.

Figure 1



This 915-MHz antenna measures only 1.25 in. sq yet outperforms a standard 3-in. monopole.

The Tab antenna is a folded monopole that you miniaturize by forming it into an inverted L with a downward bend at the end (**Figure 1**). You can solder it perpendicular to a pc board or build it as part of a pc board and place it at a corner. The folded section transforms the 12.5Ω radiation resistance to 50Ω and provides second-harmonic suppression. Third-harmonic suppression comes from an open stub near the base of the antenna. Detailed NEC-2 modeling explores the sensitivity to changes in the dimensions and optimized harmonic suppression. Because NEC models wire antennas in a vacuum and the Tab antenna is built on FR-4, you must incorporate the dielectric properties of the dielectric between the antenna elements into the model.

To incorporate the dielectric properties, you add periodic RC loads between the transmission-line elements. The loads are the small boxes in **Figure 2,** and each load comprises a 30Ω resistor in series with a 78-fF capacitor. The capacitance of each RC load is equal to the difference between the transmission-line capacitances calculated with FR-4 as the dielectric and with vacuum as the dielectric. You calculate the resistance of each RC load using the published FR-4 loss tangent of 0.02. The following formulas determine the approximate RC values for the transmission-line loads:

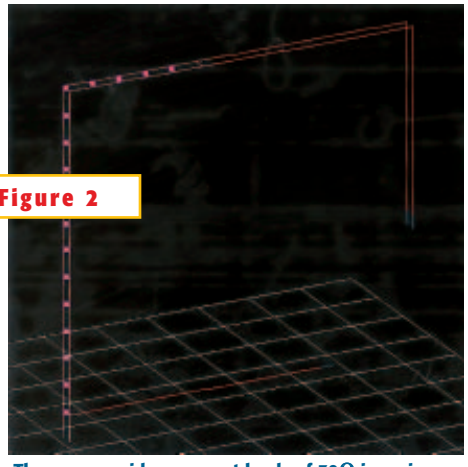
$$Z_0 = \frac{276}{\sqrt{Er}} \log_{10}\left(\frac{2D}{d}\right),$$

where D is the conductor spacing and d is the conductor diameter.

$$C = \frac{t_{PROP\_VACUUM}\sqrt{Er}}{Z_0}.$$

$$R = \frac{LOSS\ TANGENT}{2\pi fC}.$$

Figure 2



The square grids represent loads of 30Ω in series with 78-fF capacitors.

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You calculate the RC load parameters for 915 MHz and place them every 0.1 in. (approximately 5°) along the line. You use the following parameters in the calculations:

- D=62 mils,
- d=20 mils,
- effective Er (dielectric constant) of FR-4=3,
- loss tangent=0.02, and
- t_{PROP_VACUUM}=85 psec/in.

Table 1 shows the effective parameters in air and in the FR-4 medium. You use iterative modeling to determine the antenna dimensions with the following design parameters: The first vertical section and the horizontal section must be of equal lengths, the feedpoint impedance target is 50Ω, and the resonant frequency is 915 MHz. You meet these design criteria with a simulated antenna height of 1.3 in. and a total element length of 3.3 in. The actual element length of 3 in. stems from dielectric loading. You also shorten the actual antenna height to 1.25 in. to compensate for the impedance increase that the dielectric loss causes. Note that the modified NEC model accounts only for the dielectric between the antenna elements.

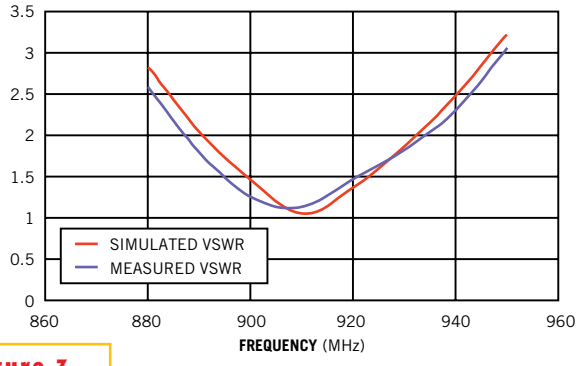


Figure 3

The simulated VSWR figures of the Tab antenna agree closely with the measured results.

The folded section, functioning as a shorted 180° transmission line at 1830 MHz, provides second-harmonic suppression. And, although the optimum point for the short circuit is 1.75 in. from the feedpoint, you can achieve second-harmonic suppression of 25 dB by placing the short within 10% of this point. The location of the short has little effect at 915 MHz. An open transmission line at the feedpoint that is 90° at 2745 MHz provides third-harmonic suppression. This line creates a near-short circuit at 2745 MHz and provides harmonic suppression of 15 dB when you trim it to within 5% of the optimum length. **Table 2** compares the simulated harmonic suppression of the Tab antenna with that of a quarter-wavelength monopole with a 50Ω source driving both antennas.

The Tab antenna has 20-mil-wide traces on opposite sides of 62-mil FR-4 and mounting pads at three locations to allow soldering the antenna securely to a larger board. You tune the antenna by trimming the open transmission line to provide an impedance minimum at 2745 MHz and then trimming the antenna elements to resonance at 915 MHz. **Figure 3** shows that the simulated 2-to-1 VSWR bandwidth is 41 MHz, whereas the measured bandwidth is 46 MHz. Note that the required operating band is only 902 to 928 MHz. The increased measured bandwidth arises from dielectric losses and indicates that the radiation efficiency is approximately 90%. The large bandwidth of the Tab antenna results in low sensitivity to environmental detuning. This design effort yields an antenna only 40% as tall as a standard quarter-wavelength monopole, yet having excellent radiation efficiency, extended bandwidth, and superior harmonic suppression.□

TABLE 1–ANTENNA PARAMETERS IN AIR AND IN FR-4 PC-BOARD MATERIAL

Dielectric	Er	Z_0 (Ω)	C (fF)	R
Air	1	219	39/0.1 in.	Infinite
FR-4	3	126	117/0.1 in.	30Ω
RC load			78	30Ω

TABLE 2–HARMONIC SUPPRESSION OF QUARTER-WAVELENGTH MONOPOLE AND TAB ANTENNA

Frequency (MHz)	Quarter-wavelength monopole (dB)	Tab antenna (dB)
1830	7	25
2745	1	15

Digital signal controls sine generator

Simon Bramble, Maxim Integrated Products, UK

THE CIRCUIT of **Figure 1** produces an accurate, variable-frequency sine wave for use as a general-purpose reference signal. It includes an eighth-order elliptic, switched-capacitor lowpass filter, IC_3, which uses a 100-kHz square-wave clock signal that microcontroller IC_2 generates. (Any other convenient square-wave source is also acceptable.) The microcontroller receives its clock signal from a 10-MHz oscillator module. A voltage supervisor,

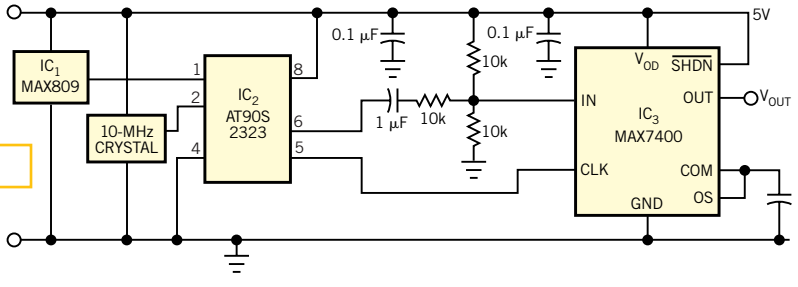


Figure 1

By removing harmonics from a square wave, this circuit generates an accurate and adjustable sine-wave output.

LISTING 1—ASSEMBLY CODE FOR SINE GENERATOR

```
;*****************************************************************************
; PORT DEFINITIONS
;*****************************************************************************

.equ   SREG   =$3f
.equ   SPL    =$3d
.equ   GIMSK  =$3b
.equ   GIFR   =$3a
.equ   TIMSK  =$39
.equ   TIFR   =$38
.equ   MCUCR  =$35
.equ   MCUSR  =$34
.equ   TCCR0  =$33
.equ   TCNT0  =$32
.equ   WDTCR  =$21
.equ   EEAR   =$1e
.equ   EEARL  =$1e
.equ   EEDR   =$1d
.equ   EECR   =$1c
.equ   PORTB  =$18
.equ   DDRB   =$17
.equ   PINB   =$16

.equ    RAMEND  =$DF    ;Last On-Chip SRAM Location
.equ   XRAMEND =$DF
.equ   E2END  =$7F
.equ   FLASHEND=$1FF

;*****************************************************************************
; REGISTER DEFINITIONS
;*****************************************************************************

.def   junk        =r16              ; junk register
.def   junk1       =r17              ; another junk reg (!)
.def   count       =r18

;*****************************************************************************
; MAIN CODE

;*********************************************************************
.cseg
.org   0
       rjmp   reset                  ; executed on RESET
.org   2
       rjmp   Int_T0                       ; executed on Timer 0 overflow
start:
       ldi    junk, 0xD8             ; preload counter with 3664
       out    TCNT0, junk            ; to give overflow after 5us

count_loop:
       cpi    count, 0x64            ; count to 100
       brne   count_loop

       ldi    junk1, 0b00000001
       in     junk, PORTB            ; read in Port B
       eor    junk, junk1
       out    PORTB, junk            ; flip bit 0 (CLK2 output)

       clr    count
       rjmp   start
```

```
;*****************************************************************************
; SUBROUTINES
;*****************************************************************************

;********************** MICRO INITIALISATION ROUTINE *************************
reset:                                ; port definitions and reset
; Initialise Stack:
       ldi    junk, low(RAMEND)
       out    SPL, junk              ; define top of Stack

; Initialise Timer 0
       ldi    junk, 0b00000000       ; stop counter
       out    TCCR0, junk

; Initialise ports:
       ser    junk
       out    DDRB,junk              ; set all ports to outputs
       clr    junk
       out    PORTB, junk            ; clear outputs

; Initialise Interrupts:
       ldi    junk, 0b10000000       ; enable Timer 0
       out    GIMSK, junk            ; set Global Interrupt bit
       ldi    junk, 0b00000010
       out    TIMSK, junk            ; overflow Interrupt

       clr    count

       ldi    junk, 0b00000001       ; Start Counter, Prescaler = 1
       out    TCCR0, junk

       rjmp   start

;*************** TIMER/COUNTER OVERFLOW INTERRUPT ROUTINE *********************



Int_T0:                               ; service here on interrupt

       ldi    junk, 0xD8             ; reset clock
       out    TCNT0, junk            ; to give overflow after 5us

       ldi    junk1, 0b00000010
       in     junk, PORTB            ; read in Port B
       eor    junk, junk1
       out    PORTB, junk            ; flip bit 1 (CLK1 output)

       inc    count
       reti

;*****************************************************************************

end:
       rjmp   end

;*****************************************************************************
; END OF FILE
;*****************************************************************************
```

IC_1, ensures correct operation in the event of a power failure. IC_3 sets the filter's cutoff frequency at one-hundredth the clock frequency.

The eighth-order elliptic filter's sharp roll-off sharply reduces the harmonic amplitudes in a 1-kHz square-wave input, thereby producing a nearly perfect 1-kHz sine wave at its output. Using divider-chain logic or a processor, you can then create a digitally adjustable sine-wave source by adjusting the clock and input frequencies and maintain a ratio of 100-to-1 between them. To prevent clipping at the positive and negative peaks, attenuate the input signal and superimpose it on a dc level of $V_{CC}/2$. The result for a 5V input is a 2.25V peak-to-peak output. **Listing 1** shows the assembly code for the microcontroller this application uses. You can download the code from the Web version of this Design Idea at www.edn.com.□

Transmitter accurately transfers voltage input

Clayton Grantham, National Semiconductor, Tucson, AZ

When you connect remote sensors to a central process controller, a simple, robust, and commonly used interface is the 4- to 20-mA loop. The advantages of this current loop include the simplicity of just two twisted wires that share both power and signal, the loop's high noise immunity in harsh environments, and the de facto loop standard within the process-control industry. Within this interface scheme, a typical 24V battery

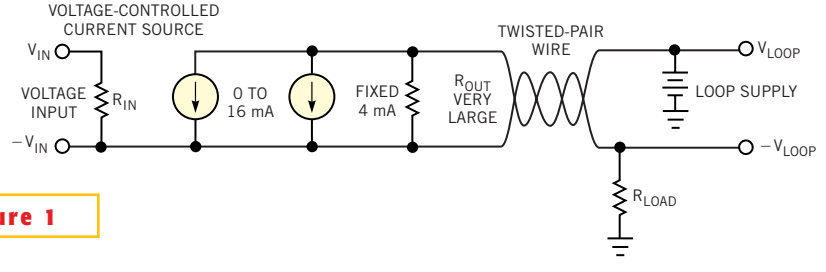
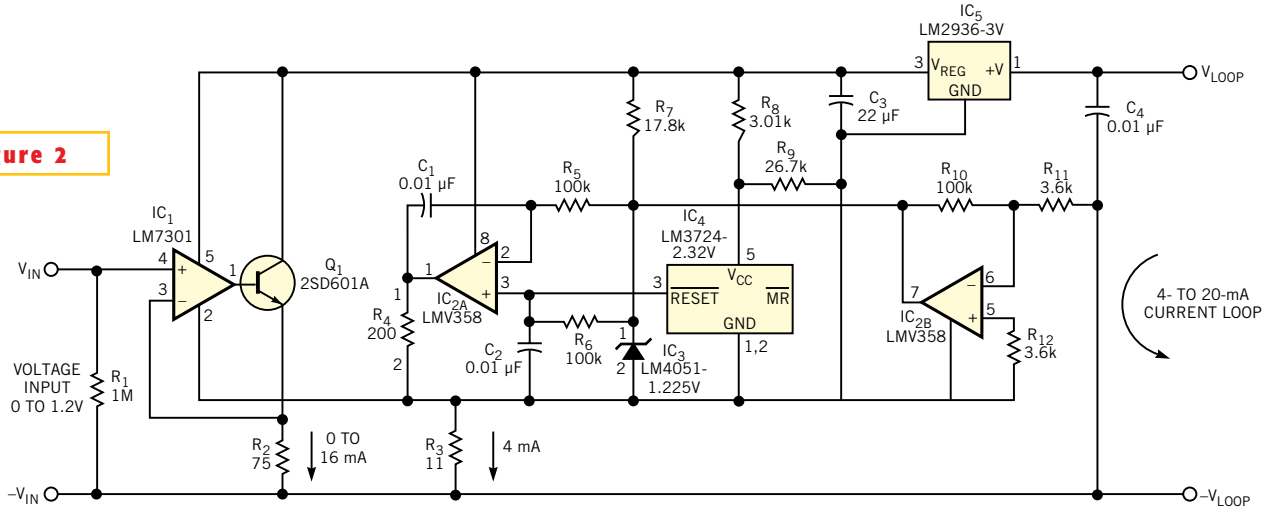


Figure 1

This ideal 4- to 20-mA current transmitter has one voltage-controlled current source and one fixed current source.

Figure 2



This circuit transforms a 0 to 1.2V input voltage to a 4- to 20-mA output range.

(loop power source) connects through a twisted-wire pair to a transconductance amplifier (voltage-to-current converter) that converts a sensor's—for example, a pressure transducer's—output voltage into a current that then gets transmitted back through the twisted-wire pair to a receiver (load resistor) at the process-control computer. An important criterion in this interface is that the current transfer of sensor information must be accurate. **Figure 1** shows the transmitter with one voltage-controlled current source and one fixed-current source.

The fixed-current source is 4 mA, a current that constitutes the power source for the transmitter and the sensor electronics. This fixed current source must have an output impedance greater than 20 MΩ to keep the loop current independent of loop-supply variations. Similarly, current needs to be independent of temperature—that is, greater than 100 ppm/°C—because the transmitter and the sensor can be in harsh environments. The voltage-controlled current source has the same requirements as the fixed-current source and needs to convert the input voltage signal linearly into a 0- to 16-mA current. Thus, it produces an ideal transconductance as the two-port network representation of a voltage-controlled current source. The total loop-current equation is: Loop current=4 mA+(gm)V_{IN} (for V_{IN}=1.2V, gm=13.3 mmho).

The transconductance circuit in **Figure 2** allows you to transmit current (4- to 20-mA loop) with less than 1% total error from −40 to +85°C and over a 3.2 to 40V loop-voltage range. Many IC realizations of a current transmitter have existed for years, but none operates at the loop voltage of 3.2V. Also, these ICs are becoming sensor-specific, whereas you can modify and optimize the circuit in **Figure 2** for any sensor electronics or loop-current variation (for example, a 1 to 5A loop) at low loop voltage. The total loop current is as follows: Loop current=1.225V(R_{11}/R_{10})/R_3+V_{IN} /R_2. The circuit discussion starts with the realization of the fixed current source, I_S. The fixed 4-mA current all flows through R_3. The servo circuitry, including IC_2 and IC_3, senses the 44-mV voltage drop across R_3 and keeps it fixed. Note that the ground current of all ICs also flows through R_3; thus, the 4-mA fixed-current setting includes ground-current errors. The dual op amp, IC_2, is both an inverting gain stage and an integrator stage. R_{10} and R_{11} set the inverting gain to −27.8V/V. The noninverting-integrator components C_1, C_2, R_5, and R_6 provide a comparison of the −44 mV across R_3 (gained up to 1.225V) to the shunt-reference voltage of IC_3. The output of IC_{2A} adjusts the sum of the current though R_4 and any ground current from IC_2, IC_3, and IC_4 to a value of 4 mA. IC_4 acts as an analog power-on-reset circuit that holds off the start-up of servo action until all the ICs have sufficient supply voltage. With the divider ratio of R_8 and R_9 and the 2.32V option of IC_4, the start-up voltage equates to: $V_{START-UP}$=2.32V(R_8+R_9)/R_9=2.7V.

This start-up value is higher than the rated supplies of IC_1 and IC_2 and lower than IC_5's regulated output of 3V. R_4 level-shifts the output of IC_{2A} up from zero. R_7 biases IC_3 into its specification range to guarantee 0.1% tolerance and 50-ppm/°C temperature coefficient over the −40 to +85°C range. The circuit discussion continues with the realization of the voltage-controlled current-source. IC_1, Q_1, and R_2 are configured as a voltage-to-current converter. Thus, for a full-scale range of 20 mA, 16 mA comes from the voltage-to-current converter. With the maximum V_{IN} at 1.2V, R_2 must be 75Ω to produce 16 mA. IC_1 must have a common- mode input range that goes beyond its negative supply (less than −44 mV). R_1 is optional and prevents an open circuit on IC_1's input. You can remove R_1, depending on the output impedance of any input-sensor electronics. Note that R_1 directly introduces an error in the full-scale loop-current.

At the heart of the circuit discussion is the realization of an output impedance, R_{OUT}, greater than 20 MΩ in **Figure 1**. The low-dropout regulator, IC_5, accomplishes this task by subregulating the supply to IC_1 and IC_2. The good line regulation of IC_5 keeps the 3V output within 30 mV over the input range of 3.2 to 40V. Additionally, IC_5 requires as little as 200 mV of overhead to properly regulate, and it

can withstand more than 40V. This current-transmitter circuit is useful for both low-loop-voltage designs, and it's backward-compatible with higher loop-voltage implementations. Furthermore, IC_5 has reverse-supply and surge protection. Therefore, this circuit does not require an additional diode within the loop, a common need with other ICs to prevent accidental reverse-wiring damage. The TO-252-package option simplifies the thermal-design considerations. With a 1-in.-sq-area pad for heat sinking, the worst-case power dissipation calculation would keep the junction temperature within its rated 150°C: $T_J = 85°C + (20\ mA)(40V) \times 50°C/W = 125°C$.

You could increase the V_{IN} range of the current-transmitter by scaling R_2, as long as you don't violate the common-mode input range of IC_1. IC_1's V_{CM} includes its positive rail. So, to obtain a higher V_{CM}, you can increase the voltage option of IC_5. For example, use the LM2936-5V and R_2 equal to 312.5Ω for a 0 to 5V input range. This configuration would also require that the loop supply be at least 5.2V. Note that any sensor and other electronics can and should use the 3V subrails that IC_5 creates as long as the current they demand does not exceed 3 mA. The 4-mA fixed-current circuitry adjusts for the current demand. **Figure 3** shows the total error on prototype units over temperature.

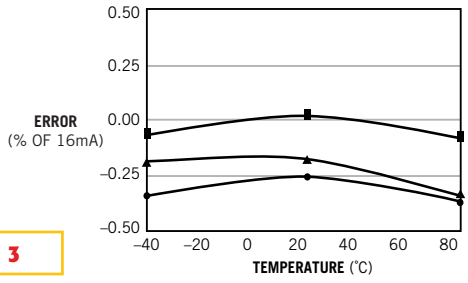


Figure 3

On three prototype circuits of Figure 2, the total error is well below 1% over temperature at 3.2V loop voltage.

The total error includes the offset (4-mA) and full-scale (20-mA) effects on the ideal loop current. The tolerances of R_2, R_3, R_7, and R_8 should be within 0.1% with 50-ppm/°C temperature coefficients. With IC_5 subregulating the rails of IC_1, IC_2, and IC_3, the power-supply-rejection-ratio error of these ICs does not generate a significant error. In like manner, IC_2's CMRR (common-mode-rejection-ratio) error does not generate a significant error. IC_3's CMRR error and Q_1's base-current error both influence the best nonlinearity attainable: less than 0.01%. IC_2's offset error is in series with the 44-mV voltage across R_3, producing an offset error of 4 mA. Adjust R_3 if you need to null this error. Adjust R_2 to fine-tune the full-scale range of 20 mA. The op amp's offset-temperature-coefficient error is small compared with the Δ1% temperature-range budget.□

Absolute-value circuit delivers high bandwidth

Ron Mancini, Texas Instruments, Bushnell, FL

Most absolute-value circuits have limited bandwidth and high component count, and they require several matched resistors. The circuit in **Figure 1** uses three fewer components than most absolute-value circuits require, and only two of the resistors must have 1% tolerance to obtain 1% accuracy. This circuit's output voltage is an accurate representation of the absolute value of the input signal, and it is accurate for input signals containing frequencies as high as 10 MHz. Another advantage of this circuit is that it has a positive-voltage output, thus saving an analog inverter in most applications. When the input voltage is positive, the negative output voltage of IC_1 cuts off the diode, thereby preventing signal propagation through IC_1. Virtually no signal propagates through R_2, because the resistor connects to ac ground through the output of IC_2. The only signal path is through R_3 to buffer IC_2, and the output of the buffer is a positive voltage. When the input voltage is negative, the positive output voltage of IC_1 forward-biases the diode, thus providing an ac short circuit for R_3 to ground. IC_2 is within IC_1's feedback loop, so the output voltage is positive because of IC_1's configuration as an inverting op amp.

This design uses a dual op amp to minimize parts count. Two op amps in a feedback loop tend to be unstable. Select an op amp that has sufficient phase margin to prevent oscillation when the input voltage is negative. The circuit's dynamic range is from the op amp's input offset voltage to the maximum output voltage. This dynamic range is from 1 mV to 4.1V for the TLC072 with ±5V power supplies. The excellent bandwidth performance results from combining the high-frequency TLC072 op amp with a fast Schottky-barrier diode. You can use higher frequency op amps to obtain better bandwidth results, but you must take care in the op-amp selection to avoid oscillation or reduced dynamic range.□

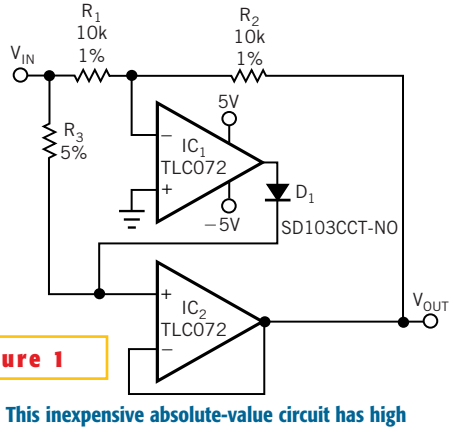


Figure 1

This inexpensive absolute-value circuit has high bandwidth.

Edited by Bill Travis

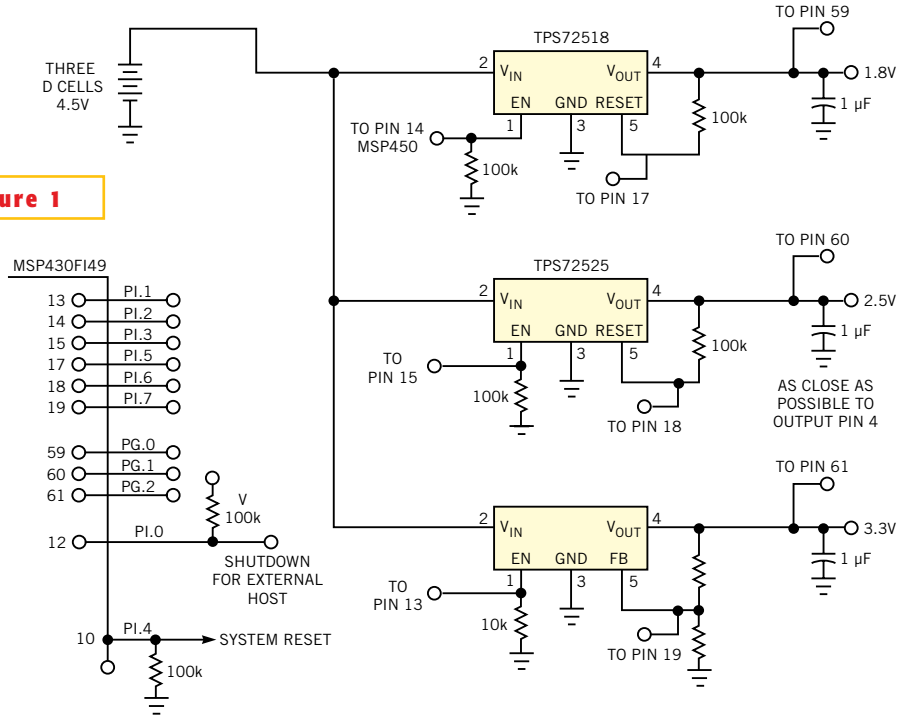
Microcontroller directs supply sequencing and control

Joe DiBartolomeo, Texas Instruments, Dallas, TX

With the proliferation of dual-voltage architectures and multiprocessor boards, even simple applications can require several processor voltage rails. With each processor having its own power-up and -down requirements, power-rail sequencing and control can become a complex task. The challenge for power-supply designers is to consider each processor's timing and voltage requirements and assimilate these into a total system, ensuring that the final design meets the requirements of all processors.

Failure to properly power processors can lead to problems that range from the fairly benign, such as a reduction in MTBF, to the catastrophic, such as latch-up. Given the variety of available processors and the application challenges you expect when developing a power-sequencing and -control scheme, use of a microcontroller is desirable because of its programmability. The MSP430 is a good fit for such an application (**Figure 1**). The high-performance, low-cost 16-bit RISC processor has several high-quality analog peripherals and a JTAG interface.

Figure 1



An ultra-low-power microcontroller controls a system's power-supply sequencing.

Controlling power supplies that have enable pins, such as those on most "brick" dc/dc converters and low-dropout regulators, is simply a matter of using a GPIO (general-purpose I/O) line. If the power supply has no enable function, an inline switch, normally a MOSFET, can control the power supply, either with a GPIO or PWM signal. The circuit in **Figure 1** uses the TPS725xx family of low-dropout regulators to provide 3.3, 2.5, and 1.8V from an input dc source. These regulators have an enable pin and a reset function. You can easily expand this circuit to any number of voltage rails. The MSP430 monitors a control variable to determine when to activate each rail. For power-sequencing applications, the two most commonly controlled variables are time and voltage. When time is the control variable, the controller enables the first rail. At a specific time thereafter, it enables the next rail. Some time after that, it enables the next rail, and so on until it has enabled all rails.

The MSP430 provides the timing-sequence and the -control signals to turn on the power supplies. If voltage is the control variable, then the controller activates the first voltage rail and monitors its rise via an ADC. When the first voltage rail reaches a specific voltage level, the controller enables the next voltage rail and monitors its rise until it reaches

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a specified voltage level. At this point, the controller enables the next voltage rail and monitors it. This process continues until the controller has enabled all voltage rails. When using voltage as the control variable, the controller can use either a GPIO or a PWM signal as the enable signal, depending on whether the design requires rail tracking. You can also use a combination of voltage and timing control.

In **Figure 1**, each low-dropout regulator connects to two MSP430 lines—one for enabling and the other for monitoring. When time is the control variable, the monitoring takes place via Port 1 (GPIO); when voltage is the control variable the monitoring occurs via Port 6 (ADC). The MSP430 also provides a system reset and has an input for power-down. The code is fairly simple and does not require much programming experience. When time is the control variable, the first thing to do is initialize the MSP430 and setup the port and timer; this operation takes five lines of code (see **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com). The next operation is to load the capture-and-compare register zero (CCR0) with the first timing interval and start the timer. When CCR0's value is equal to the timer's value, the first voltage rail becomes enabled. CCR0 is then loaded with the next time interval, and the timer resets and restarts. When CCR0 is equal to the timer value, the second voltage rail becomes enabled. This operation repeats until all rails become enabled.

Once all rails are enabled, a delay loop enters the picture to ensure that the reset pins on the low-dropout regulators have time to come up. The TPS725xx family has an open-drain, 100-msec reset function. Once the delay is complete, the MSP430 checks each regulator's reset line to ensure that all rails are up. If all rails are up, the MSP430 issues a system reset. When voltage is the control variable, only five lines of code are necessary to initialize the MSP430 (**Listing 2**, which is available with the Web version of this Design Idea at www.edn.com). The next operation is to load registers R9, R10, and R11 with values that represent 3.3, 2.5, and 1.8V, based on a 3V ADC reference. The first rail becomes enabled, and its output voltage undergoes monitoring until it is within specification, at which point the next rail is enabled and monitored. This operation repeats until all three rails become enabled. Once all the rails are enabled, the delay loop for regulator reset activates, and the system reset occurs.

Once the MSP430 turns on all the voltage rails and applies the system reset, it enters the monitor mode. It continually checks the low-dropout regulator's output voltage, via the reset or output pins, depending on whether time or voltage is the control variable. If a fault occurs, the MSP430 enters an error routine. The most obvious fault would be the loss of a voltage rail, but other faults, such as overvoltage and undervoltage, are also amenable to monitoring. The actions that the error routine takes depend on the application. The simplest actions would be to power down all rails, but programmability gives you complete control. One final function is the powering down of the voltage rails. An external signal, likely from the main processor, signals the MSP430 to power down the processor rails. In this example the power-down sequencing is just the opposite of the power-up sequence, but you can define any sequence. One addition to the power-down sequence could be to turn on dummy loads to discharge the output filter capacitors. This design uses the TPS-725xx low-dropout regulators because they offer fast transient response and stability with any output capacitor. However, some applications may require large output capacitors to maintain stability and transient response. In these cases, the ability to discharge these filter capacitors improves MTBF. □

Circuit provides leading-edge blanking

Michael O'Loughlin, Texas Instruments, Dallas, TX

In isolated switch-mode power supplies using peak-current-mode control, generally the current-sense resistor senses the current on the primary side of the power converter. **Figure 1** shows a typical circuit, in which R_2 is the current-sense resistor that monitors the current. The current-sense signal goes to the input of the PWM comparator—in this case, the PWM comparator's input (I_{SENSE}) of the controller IC. R_3 and C_1 provide an RC delay in an attempt to remove some of the leading-edge spikes on the current-sense signal. Sometimes, the RC delay circuit is insufficient for removing the false noise signals at the input of the PWM comparator. This Design Idea shows how to suppress the false triggering signals caused by parasitic LC (inductance and capacitance), causing LC tanking and false-peak current triggering to the peak-current-limit comparator.

The RC delay circuit in **Figure 1** works for most applications in suppressing voltage spikes that may falsely trip the peak-limit-current comparator. However, some applications require a leading-edge blanking circuit to suppress false triggering. **Figure 2** shows the typical current-sense signal that appears across R_2. The leading-edge spike at time T_1 occurs

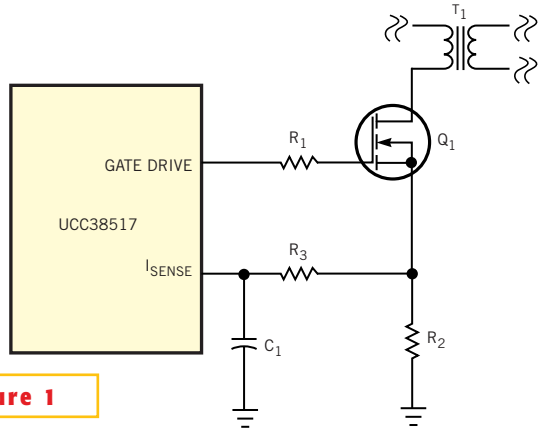


Figure 1

In this classic PWM-controller configuration, R_2 is the sending resistor for the output current.

when the gate drive switches from low to high and the parasitic capacitance from the gate to the source of Q_1 is charging. Depending on the values of R_1 and R_2, a large-enough leading-edge voltage spike could falsely trigger the PWM comparator at the I_{SENSE} pin. This problem is common in isolated dc/dc power converters. To remove false triggering from the PWM comparator, it is desirable to blank out the leading-edge spikes that appear on the current-sense signal. You can suppress these leading-edge spikes by adding four additional components to the circuit in **Figure 1**. **Figure 3** shows the extra circuitry necessary to provide leading-edge blanking. The gate drive from the PWM circuit activates the leading-edge blanking circuit. Transistor Q_2 suppresses the leading-edge current-signal spike. Components R_4, C_2, and R_5 set up the amount of time the leading edge of the current-sense signal is suppressed from the PWM comparator.

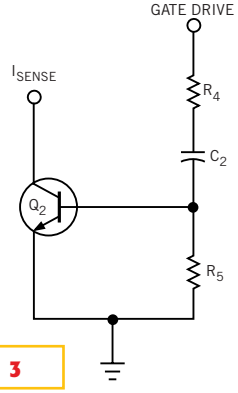


Figure 3

Transistor Q_2 suppresses (blanks) leading-edge spikes that could falsely trigger a PWM comparator.

Selecting the components for the leading-edge blanking circuit is simple. You select Q_2 with sufficiently low saturation voltage, V_{SAT}, to suppress the leading edge of the current-sense signal. You select R_4 and R_5 to drive transistor Q_2 into saturation. You then select C_2 to set up the timing for the circuit. To select transistor Q_2, the maximum collector-to-emitter voltage, V_{CE}, must be less than the gate-drive voltage. The transistor saturation voltage, V_{SAT}, must be low enough to suppress the voltage spike at the PWM comparator's input. For most applications, you can get away with using a 2N2222 transistor. You must select R_3 to provide some current-limiting protection for transistor Q_2. R_4 must supply sufficient base drive, I_B, current to Q_2. You select R_5 such that its current is 10% of the base-drive current. You choose the value of C_2 to keep transistor Q_2 saturated for two RC time constants. You can use the following equations to calculate the resistor and capacitor sizes:

$$R_4 = \frac{V_{GATE} - V_{BE}}{I_B},$$

$$R_5 = \frac{V_{GATE} - V_{BE}}{I_B/10}$$

and

$$C_2 = \frac{T_{BLANK}}{2(R_4 + R_5)},$$

where V_{GATE} is the maximum gate-drive voltage of the PWM comparator, and T_{BLANK} is the amount of leading-edge blanking time required.

Another power-supply design has current-sense spikes so large that the module will not regulate. This design requires the implementation of the leading-edge blanking circuit in **Figure 2**. The design, a 200-kHz flyback converter, requires a leading-edge blanking time, T_{BLANK}, time of 200 nsec. The leading-edge blanking circuit requires a maximum base current, I_B, of 42 mA. The I_B specifications require R_4 to be 275Ω and R_5 to be 200Ω. To attain the 200-nsec delay, C_2 needs to be approximately 390 pF. Q_2, a 2N2222 current-suppression transistor, requires a current-limiting resistor, R_3, of roughly 1 kΩ. The PWM comparator's input, I_{SENSE}, has a peak threshold of 1.5V. **Figure 4** shows the current-sense signal of the flyback converter before the addition of the suppression circuit. The waveform shows that leading-edge spikes turn off switch Q_1.

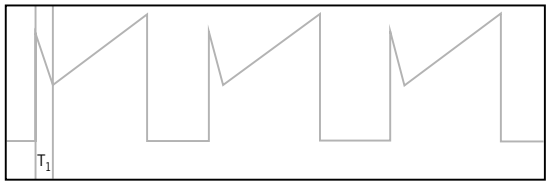


Figure 2

The leading-edge spike in this waveform could falsely trigger the PWM comparator in Figure 1.

After you add the leading-edge blanking circuit to the power module, it clamps the leading-edge voltage spikes and allows the converter to operate correctly. **Figure 5** shows the current-sense waveform. Leading-edge noise spikes on the current-sense signal can cause instabilities in peak-current-mode-control power-supply designs. Usually, you can resolve these issues with an RC filter at the input of the peak-current-limit comparator. In some instances, the noise disturbance caused by parasitic capacitance and gate-drive current can cause the PWM comparator to trip falsely. In these instances, the supply requires a leading-edge blanking circuit similar to this one.□

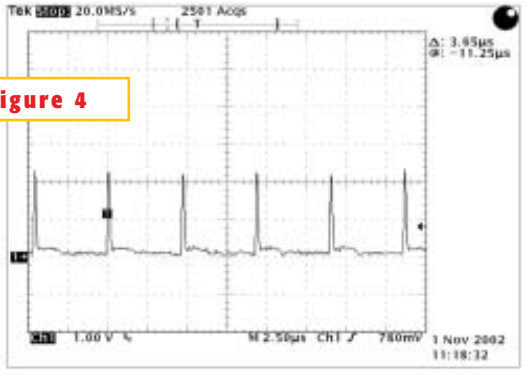


Figure 4

Without leading-edge suppression, the spikes turn off Q_1 in Figure 1.

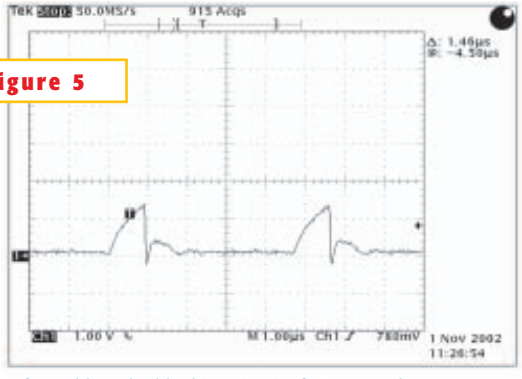


Figure 5

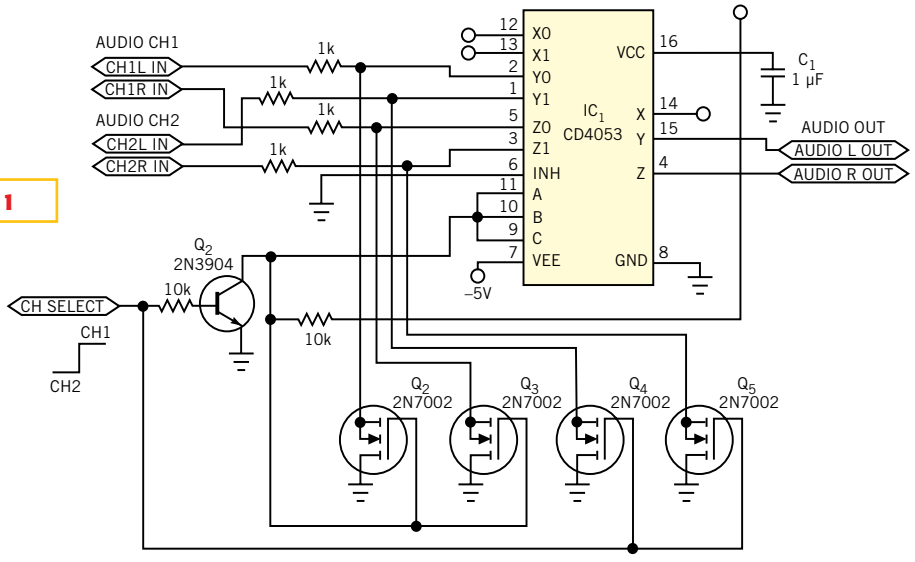
After adding the blanking circuit of Figure 3, the converter works normally.

MOSFETs reduce crosstalk effects on analog switches

Stanley Chen, Global Mixed-Mode Technology, Taipei, Taiwan

Some cost-effective analog multiplexer/demultiplexer ICs, such as the CD4053 and CD4066, find frequent use as signal distributors. These digitally controlled analog switches have low on-resistance. However, with all channels in the same package, crosstalk can be annoying and unavoidable.

Figure 1



By using a few low-cost MOSFETs, you can drastically reduce crosstalk effects in an analog multiplexer.

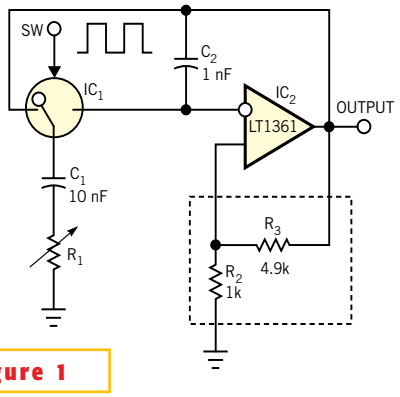
Figure 1 provides a cost-effective and viable method of solving this problem. By simply adding some n-channel MOSFETs, such as the 2N7002 or 2N7000, the crosstalk effect becomes negligible. When the Channel Select signal is high, the CD4053's input pins A, B, and C assume a level of nearly 0V. This operation selects Channel 1. Therefore, the Y output connects to Y0 and Z to Z0. Meanwhile, the Channel Select signal turns on Q_4 and Q_5, thereby drastically attenuating the Channel 2 signal at Y1 and Z1. The crosstalk effect simultaneously decreases. When the Channel Select signal is set low, Y=Y1 and Z=Z1, and Q_2 and Q_3 turn on to attenuate the crosstalk effect. For the 2N7002, the $R_{DS(ON)}$ resistance is several ohms; therefore, the crosstalk decreases by more than 40 dB. Add to that the analog switch's internal rejection ratio, and the total crosstalk rejection could be as high as 80 dB.□

Grounded resistor tunes oscillator

Vladimir Tepin, Taganrog, Russia

To vary the frequency of any sine-wave oscillator, you should use a pair of ganged variable resistors, and you should thoroughly match their characteristics over the entire variation range to satisfy the oscillator's balancing conditions. This restriction leads to problems in the tuning range and high cost, thereby limiting the range of applications. The sine-wave oscillator in **Figure 1** is free of the cited disadvantage. You can tune it over a wide frequency range using only variable resistor R_1. The oscillator requires no balancing, so no matching problems arise. The variable resistor connects to ground, an advantageous fact in many applications. Like most classic sine-wave RC oscillators, the implementation comprises an operational amplifier, IC_2, with two feedback loops. One loop is a frequency-independent, positive-feedback loop using two fixed resistors, R_2 and R_3, in this example. The other loop is frequency-dependent. This loop uses capacitors C_1 and C_2; variable resistor R_1; and a single-pole, double-throw analog switch, IC_1, driven by a periodic sequence of square-wave pulses applied to the SW input.

Figure 1



In this sine-wave oscillator, the output frequency is dependent only on the value of the grounded resistor R_1.

Assuming a switching frequency, $F_S=1/T$, much higher than the oscillation frequency and assuming that the pulse width, τ, is half the switching period ($\tau=0.5T$), the approximate voltage trans-

fer function of the frequency-dependent feedback loop is:

$$H(s)=\frac{s^2+s\omega_0 d_1+\omega_0^2}{s^2+s\omega_0 d_0+\omega_0^2},$$

where $\omega_0=1/2R\sqrt{C_1C_2}$ is the oscillation frequency, $d_0=\sqrt{C_1/C_2}+2\sqrt{C_2/C_1}$, and $d_1=2\sqrt{C_2/C_1}$. Using this function and assuming the transfer coefficient of the positive-feedback circuit to be $\gamma=R_2/(R_2+R_3)$, you obtain the oscillation condition in the form $\gamma>d_1/d_2=2\sqrt{C_2/C_1}/(2\sqrt{C_2/C_1}+\sqrt{C_1/C_2})$. The oscillation condition does not depend on R_1. It thus becomes obvious that controlling grounded resistor R_1 results only in the variation of the oscillation frequency and does not affect the condition for oscillation. This situation means that you can tune this oscillator over a wide range of frequencies, preserving the output waveform.

PSpice simulations prove the possibility of tuning the oscillation frequency over three decades (20 Hz to 20 kHz) by varying R_1 from 1.2 MΩ to 1.2 kΩ. This design uses an LT1361 (www.linear.com) for IC$_2$, $R_2=1$ kΩ, $R_3=4.9$ kΩ, $C_1=10$ nF, $C_2=1$ nF, and $F_S=500$ kHz. The output-voltage amplitude is 3.2 to 3.3V. The total harmonic distortion in the 0- to 100-kHz band does not exceed 3%. It's useful to note that, because the oscillation frequency is proportional to the conductance of the variable resistor ($G_1=1/R_1$), you can use the oscillator as a linear, wideband conductance-to-frequency or resistance-to-period converter.□

Obtain higher voltage from a buck regulator

Ajmal Godil, Micrel Semiconductor, San Diego, CA

Several semiconductor vendors' current-mode buck controllers have input-voltage ranges of 30 to 36V but have output-voltage ranges from the reference voltage to approximately 6V. This output-voltage constraint arises from the common-mode-voltage limitation of the current-sense amplifier. In real-world applications, the power-supply designer must be able to generate high output voltage for printers, servers, routers, networking, and test equipment. Using a conventional buck regulator to generate higher voltages is a challenge. The circuit in **Figure 1** meets

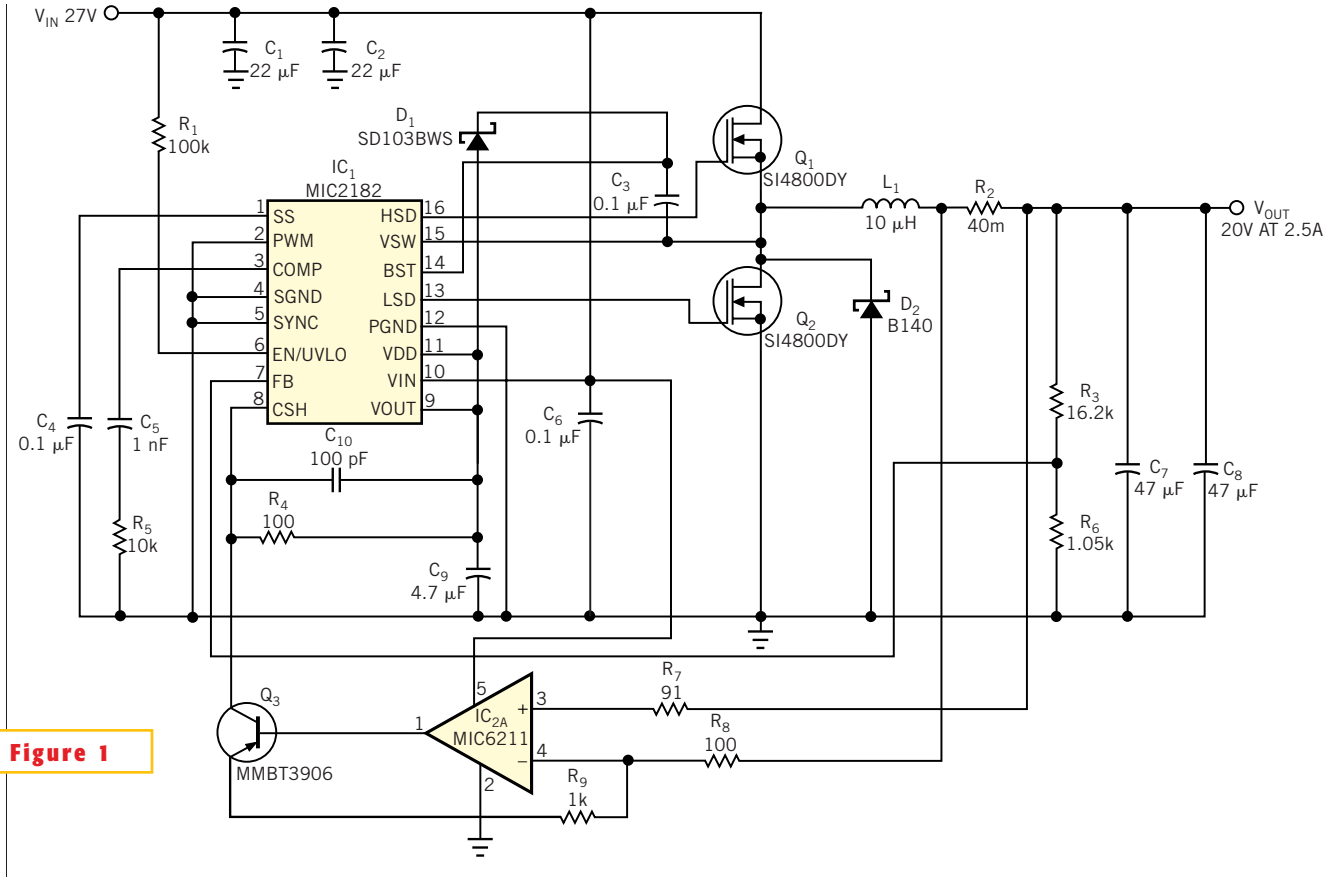


Figure 1

You can generate 20V output using a standard, current-mode buck regulator.

the challenge by using an external op amp, a small-signal pnp transistor, and a low-output-voltage buck regulator to deliver 20V output voltage from a 27V input supply for load currents as high as 2.5A. You can easily program the circuit to provide higher load currents by merely lowering the sense resistor, R_2. IC_1, the controller in **Figure 1** is the MIC2182, and IC_2, the operational amplifier, is the MIC6211. Resistors R_3 and R_6 program the output voltage as follows: $V_{OUT}=20V=V_{FB}(1+R_3/R_6)$.

CSH (Pin 8) and VOUT (Pin 9) of the buck controller normally connect across the sense resistor, R_2, for output voltages as high as 6V. The controller asserts current limit when it senses approximately 100 mV across these two pins. In the case of $V_{OUT}=20V$, the operational amplifier and Q_3 level-shift the voltage drop across R_2 from 20V down to 5V, which is within the input common-mode range of the internal current-sense amplifier of the buck regulator. You can readily understand the circuit operation by assuming a voltage drop of 40 mV across R_2 for a load current of 1A. The current through R_8 is 400 µA ((20.04−20)/100), which is also the current through R_9 and R_4 (via Q_3). This current generates a voltage drop of 40 mV across R_4 (400 µA×100Ω). The controller's VOUT pin connects to the internal 5V regulator (VDD) and R_4; the other side of R_4 connects to the CSH pin. The voltage on the VOUT pin is 5V, and the voltage on the CSH pin is 5.04V. The voltage difference between these two pins is exactly the voltage drop across R_2. The simple circuit in **Figure 1** allows you to achieve greater than 95% efficiency for load currents as high as 2.5A with $V_{OUT}=20V$, using a conventional low-output-voltage, current-mode buck regulator. **Figure 2** shows the efficiency of the regulator.□

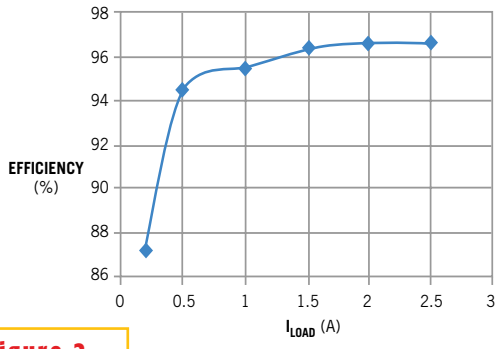


Figure 2

This curve shows the efficiency of the regulator in Figure 1.

design ideas

Edited by Bill Travis

Light a white LED from half a cell

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

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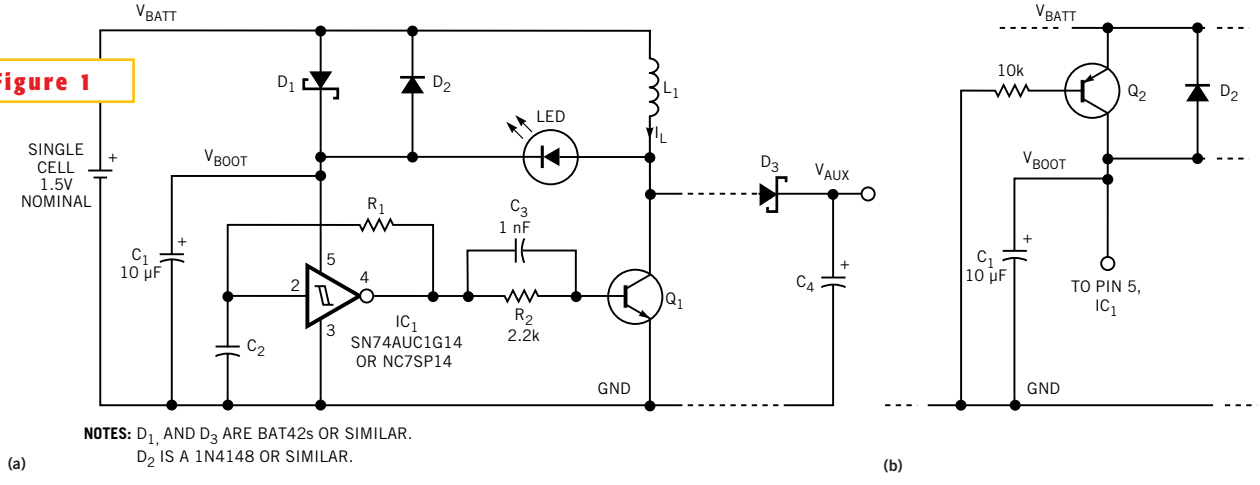
Whether you use them as indicators or to provide illumination, LEDs are hard to beat in efficiency, reliability, and cost. White LEDs are rapidly gaining popularity as sources of illumination, as in LCD backlights, but with forward voltages typically ranging from 3 to 5V, operating them from a single cell presents obvious difficulties. This design exploits the ultralow operating voltage of a single-gate Schmitt inverter, such as the Texas Instruments (www.ti.com) SN74AUC1G14 or the Fairchild (www.fairchildsemi.com) NC7SP14 (**Figure 1**). When you first apply battery power, Schottky diode D_1 conducts, and the familiar Schmitt-trigger astable multivibrator starts to oscillate at a frequency determined by timing components C_2 and R_1. When IC_1's output goes high, transistor Q_1 turns on, and current begins to ramp up in inductor L_1. The maximum, or peak, level of inductor current is $I_{L(PEAK)}=(V_{BATT}-V_{CE(SAT)})\times t_{ON}/L_1$, where V_{BATT} is the applied battery voltage, $V_{CE(SAT)}$ is Q_1's saturation voltage, and t_{ON} is the duration of the high-level pulse at the Schmitt trigger's output. If Q_1's saturation voltage is, for example, less than 50 mV, you can ignore $V_{CE(SAT)}$ and simplify the expression to $I_{L(PEAK)}=V_{BATT}\times t_{ON}/L_1$.

At the end of t_{ON}, when the inverter output goes low, Q_1 turns off, and the voltage across L_1 reverses polarity. The resulting "flyback" voltage immediately raises Q_1's collector voltage above V_{BATT} and forward-biases the LED and D_2, which appear in series. This action illuminates the LED with a maximum forward current equal to $I_{L(PEAK)}$ and raises IC_1's supply voltage, V_{BOOT}, to a diode drop above V_{BATT}. D_1 is now reverse-biased and remains so for as long as the circuit continues to oscillate. The resulting "bootstrapped" supply voltage for IC_1 ensures that the astable multivibrator continues to operate even when V_{BATT} falls to very low levels. You should choose values for C_2 and R_1 to produce a time constant of microseconds, thereby allowing a small inductance value for L_1. For example, a test circuit using values of C_2=68 pF, R_1=39 kΩ, and L_1=47 µH produces an operating frequency of approximately 150 kHz at V_{BATT}=1V. The resulting value of t_{ON}=3 µsec leads to a peak inductor current of approximately 65 mA and produces excellent brightness in the white LED. Even with V_{BATT} as low as 500 mV, the corresponding peak current of 33 mA produces reasonable LED intensity.

The inductance value should be as low as possible to maintain a high peak current and, hence, adequate LED brightness at the lowest supply voltage. However, L_1 should not be too small, or the peak current could exceed the LED's maximum current rating when V_{BATT} is at a maximum. Remember that the inductor should be adequately rated to en-

Figure 1



NOTES: D_1, AND D_3 ARE BAT42s OR SIMILAR.
D_2 IS A 1N4148 OR SIMILAR.

(a) (b)

This circuit produces dazzling intensity in a white LED from very low battery voltages (a). A modification allows even lower battery voltages (b).

sure it does not saturate at the highest value of peak current. Switching transistor Q_1 should have very low saturation voltage to minimize losses and produce the highest possible peak current. The addition of D_3 and C_4 enables the circuit to generate an auxiliary supply voltage, V_{AUX}, which you can use to drive low-power circuitry without adversely affecting the LED's intensity. With a battery voltage of 1V, the test circuit produces good light intensity in the white LED and delivers almost 1.5 mA at 4.7V to the auxiliary load. Even at V_{BATT}=500 mV, the circuit delivers 340 µA into a 10-kΩ load and maintains reasonable LED brightness. Note that IC_1 cannot take power from the auxiliary rail, because V_{AUX} can easily exceed the maximum voltage rating of the two suggested device types.

The minimum start-up voltage depends largely on the device you use for D_1. Tests using a high-quality Schottky diode produce a minimum power-up voltage of just 800 mV. You can further reduce this level by replacing D_1 with pnp transistor Q_2 (**Figure 1b**). This modification allows the test circuit to start up at just 650 mV at room temperature. Note, however, that Q_2's collector-base junction becomes forward-biased under quiescent conditions, which results in wasted power in its base-bias resistor. Despite its simplicity, the circuit can produce spectacular results with high-brightness LEDs. The Luxeon range of LEDs from Lumileds (www.lumileds.com) allows the circuit to demonstrate its prowess. With L_1 reduced to 10 µH and V_{BATT}=1V, the circuit generates a peak current of 220 mA in a Luxeon LXHL-PW01 white LED, resulting in dazzling light intensity.□

LED driver delivers constant luminosity

Israel Schleicher, Bakersfield, CA

THE CIRCUIT IN **Figure 1** is similar in principle to that of a previous Design Idea (**Reference 1**) but offers improved, more reproducible performance. The output current is almost constant over an input-voltage range of 1.2 to 1.5V and is insensitive to variations of transistor gain. Transistors Q_1 and Q_2 form an astable flip-flop. R_1 and C define the on-time of Q_2. During that time, Q_1 is off, and the voltage at the base of Q_1 and the current in inductor L ramp up. When the voltage at the base of Q_1 reaches approximately 0.6V, Q_1 turns on, and Q_2 turns off. This switching causes "flyback" action in inductor L. The voltage across the inductor reverses, and the energy stored in the inductor transfers to the LED in the form of a down-ramping pulse of current. During flyback time, voltage across the LED is approximately constant.

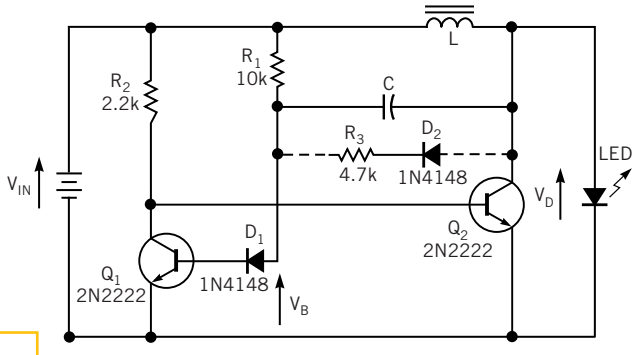


Figure 1

NOTE:
WHITE LED REQUIRES R_3 AND D_2.

This circuit delivers virtually constant luminosity for a white or a yellow LED.

The voltage for yellow and white LEDs is approximately 1.9 and 3.5V, respectively. When the current through the LED falls to zero, the voltage at the collector of Q_2 falls sharply, and this circuit condition triggers the next cycle. Assuming the justifiable approximation that the saturation voltage of Q_2 is close to 0V and that the LED's forward voltage, V_D, is constant, you can easily derive the expression for the average dc current through the LED:

$$I_{AVE} = \frac{V_{IN}^2 R_1 C}{2 V_D L} \log_e \left(\frac{V_{IN} + V_D - V_B}{V_{IN} - V_B} \right).$$

At first glance, I_{AVE} depends strongly on V_{IN}. But close examination of the logarithmic term reveals that, with a proper selection of V_B, the logarithmic term can become a sharply declining function of V_{IN}. The logarithmic term thus fully compensates for the term V_{IN}^2 in the expression. That compensation is precisely the purpose of the diode, D_1, in series with the base of Q_1. The circuit drives a high-brightness yellow or white LED. **Table 1** shows the proper component selection for both colors. **Table 1** also shows some measured results at V_{IN}=1.35V. Because the voltage across the white LED falls from 3.9 to 3.1V during flyback, capacitor C subtracts current from the amount available to the base of Q_1. This subtraction might retrigger the circuit before the current in L falls to zero. The addition of R_3 and D_2 solves this problem. During flyback, the current that flows through R_3 compensates for the current withdrawn through C.□

TABLE 1–COMPONENT SELECTION FOR YELLOW OR WHITE LED

LED	L (mH)	C (pF)	D_1	Current drain (mA)	LED current (mA)	Frequency (kHz)	Power-conversion efficiency (%)
Yellow	1	470	1N4003	5.6	3.3±0.1	40	83
White	2	1800	1N752	12.4	3.7±0.2	15	78

REFERENCE

1.Nell, Susanne, "Voltage-to-current converter drives white LEDs," *EDN*, June 27, 2002, pg 84.

Get more power with a boosted triode

Dave Cuthbert, Boise, ID

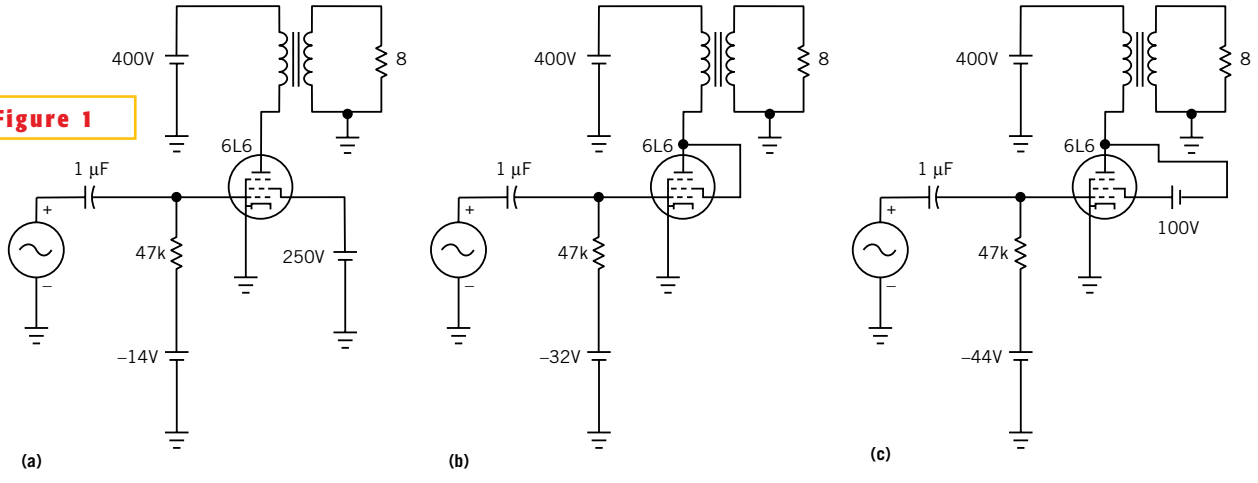
This Design Idea is a reprint of an earlier one that contained errors in graphics (**Reference 1**). Even though 6L6 beam-power tubes have been around for 66 years, they are still quite popular for use in electric-guitar amplifiers, and its cousin, the 6CA7 (EL34) power pentode, is a favorite among audiophiles. The developers of these tubes designed them for pentode-mode operation, and they deliver maximum audio power in this mode. On the other hand, many audiophiles prefer triode-mode operation and, until now, had to be content with a 50% reduction in output power. This reduction means that they require larger power supplies and twice as many expensive tubes to obtain pentode power from a triode amplifier. **Figures 1a**, **1b**, and **1c** show the 6L6 connected as a pentode, a true triode, and a "boosted triode," respectively. The boosted-triode configuration allows pentodes to produce pentodelike power while operating in a true-triode mode. To understand the operation of the boosted triode, it's useful to review some vacuum-tube theory. The 6L6 is a beam-power tube and has cathode, control-grid, screen-grid, suppressor-grid, and plate electrodes. The suppressor grid is actually a virtual suppressor grid provided by two beam-forming plates, but you can treat the 6L6 beam-power tube as a pentode. You can think of a pentode as an n-channel JFET with the following electrode functions:

- Thermionic cathode: source of electrons (corresponds to the JFET source);
- Control grid: controls the cathode current; operated at a negative potential relative to the cathode (corresponds to the JFET gate);
- Screen grid: electrostatically screens the control grid from the plate, thereby reducing the effect that the plate voltage has on the cathode current; operates at a

TABLE 1–PENTODE, TRIODE, AND BOOSTED-TRIODE PARAMETERS

Amplifier	DC plate current (mA)	Grid bias (V)	Grid swing (V)	Output power (W)
Pentode	75	−14	22	11
Triode	75	−32	64	6
Boosted triode	75	−44	88	10

Figure 1



A pentode (a) can deliver much more power than a triode (b), unless you use a boosted-triode configuration (c).

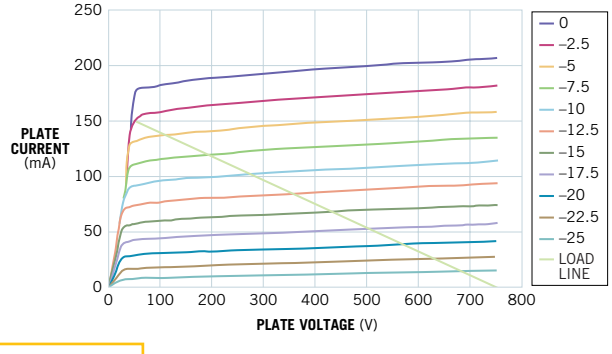


Figure 2 The load lines for a pentode show that the plate can draw 150 mA at a plate voltage of only 50V.

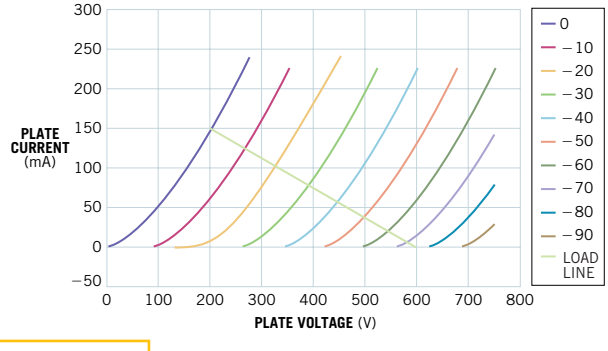


Figure 3 A pure triode needs 200V plate voltage to draw 150 mA.

positive potential relative to the cathode;

- Suppressor grid: prevents secondary electrons from leaving the plate and traveling to the screen grid; operates at the cathode potential; and
- Plate: collects the electrons (corresponds to the JFET drain).

Figure 2 shows the pentode's characteristic curves for control-grid voltages of 0 to −25V and a screen-grid voltage of 250V. Note the idealized load line and that the tube can draw a plate current of 150 mA at a plate voltage of only 50V. High voltage gain, high plate impedance, and high output power characterize pentode-mode amplification. By connecting the screen grid directly to the plate, you can operate the tube in triode mode. Low voltage gain and low output impedance characterize this mode. **Figure 3** shows how the triode curves differ from the pentode curves. The curves represent control-grid voltages of 0 to −90V. Note the load line and that, in triode mode, the plate cannot draw 150 mA at a plate voltage lower than 200V. This fact greatly limits amplifier efficiency and power output. However, in spite of the limited output power, some people still prefer triode mode because they claim that it produces a superior-sounding amplifier.

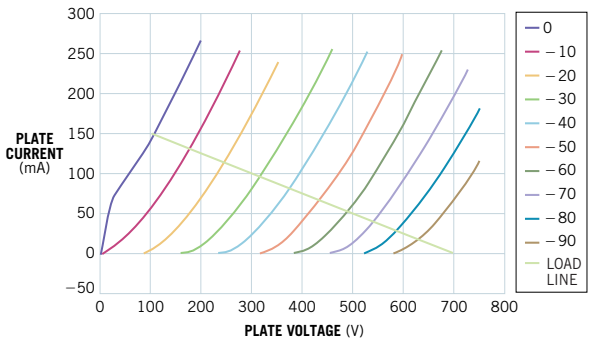


Figure 5 With a boosted triode, the plate can draw 150 mA with a plate voltage of 100V versus 200V for a pure triode.

For the boosted-triode circuit in **Figure 1c**, you simply add a 100V screen-to-plate power supply (**Figure 4**) to the standard triode-amplifier circuit. This addition shifts the triode characteristic curves 100V to the left (**Figure 5**). Note the load line and that the plate can now draw 150 mA at a plate voltage of only 100V, rather than 200V as with the pure-triode-mode circuit. You can obtain significantly higher power with boosted-triode amplification and still maintain the characteristics of triode amplification. In Spice simulations of three single-ended Class A audio amplifiers using MicroCap-7 evaluation software (www.spectrum-soft.com), the control-grid bias for a quiescent plate current is 75 mA, and the ac grid signal is just short of amplifier clipping. The transformer ratios provide a plate-load impedance of 5 kΩ for the pentode and 3 kΩ for both the triode and the boosted triode. **Table 1** details the parameters.□

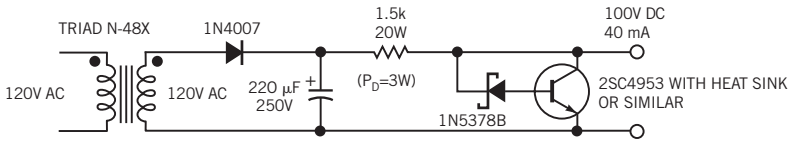


Figure 4 A 100V screen-grid power supply transforms a normal triode into a boosted triode.

Reference

1. Cuthbert, Dave, "Get more power with a boosted triode," *EDN*, April 3, 2003, pg 72.

White-LED driver touts high efficiency

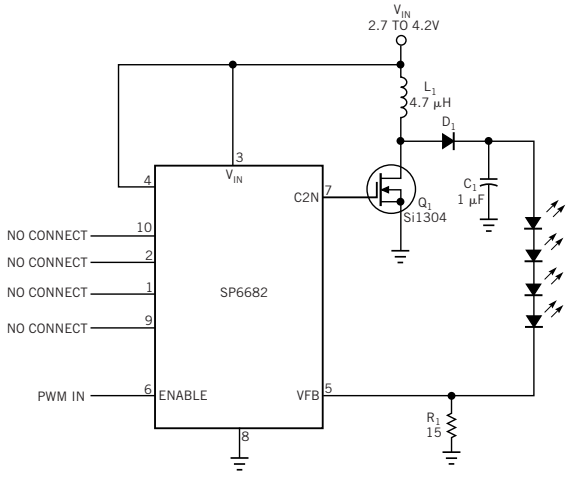
Dimitry Goder, Sipex Corp, San Jose, CA

White LEDs, the most recent addition to the LCD backlight, find common use in providing backlight for color LCDs. Thanks to their size and white-light output, they appear in small, portable devices with color displays, such as PDAs and cellular phones. Like other LEDs, a white LED needs a constant-current source—typically, on the order of 15 to 20 mA. The forward voltage of a white LED is approximately 3.5V. Most products use multiple LEDs to provide adequate backlight for a display. Because the LED's brightness depends on its forward current, these multiple diodes commonly connect in series to ensure that the same current flows through each of them. You need approximately 14V to forward-bias four series-connected LEDs, starting from the nominal operating voltage, 2.7 to 4.2V, of a single-cell lithium-ion battery. Boost regulators usually provide this operating voltage. A current-sense resistor, which you insert in series with the LEDs, closes the feedback loop. However, it is important to minimize the voltage drop across this resistor to increase efficiency. Currently available integrated boost regulators commonly use a 1.24V bandgap voltage as the feedback reference, which results in 1.24V loss across the current-sense resistor, a loss that represents approximately 7% loss in efficiency. **Figure 1** shows an interesting LED-drive circuit.

You use the SP6682, a standard, regulated charge-pump circuit, in an unusual manner to control the external switch, Q_1. This IC incorporates an internal 500-kHz oscillator, which would normally drive charge-pump capacitors to double the input voltage. The circuit in **Figure 1** uses no charge-pump capacitors. Instead, the oscillator output appears on Pin 7 and drives Q_1 on and off. Q_1, L_1, D_1, and C_1 function as a conventional boost reg-

ulator, which builds up voltage across C_1. When this voltage exceeds the sum of the diodes' forward drop, current starts to flow. The circuit senses current across R_1 and compares it with a 0.3V reference voltage inside the chip. This circuit provides efficiencies as high as 87%, a figure that exceeds that of any integrated boost regulator. Several factors are responsible for the increased efficiency. First, the chip integrates the 0.3V reference voltage, which is significantly lower than the typical 1.24V. This reference voltage appears in series with the LEDs and therefore constitutes an efficiency loss proportional to the value of the reference. Second, a discrete MOSFET provides low on-resistance and high switching speed, parameters superior to those of any integrated switch.

Figure 1



This circuit uses a charge-pump IC to provide power to a series string of LEDs.

Q_1 is a low-cost device that comes in a tiny SOT-23 package. Also, the excellent drive capability of the charge-pump IC ensures low switching losses. By changing the type of the MOSFET you use, you can make a trade-off between desired efficiency and cost. The breakdown voltage of the MOSFET limits the maximum output voltage; you can adjust the voltage to drive a system with as many LEDs as you need. (Larger displays use eight to 12 LEDs.) For dimming purposes, applying a PWM signal to the Enable pin causes the regulator to shut down and restart. This function allows you to precisely control LED brightness.□

design ideas

Edited by Bill Travis

Gate-drive method extends supply's input range

John Betten and Robert Kollman, Texas Instruments, Dallas, TX

Industrial and telecom applications often require a nonisolated, low-voltage supply from a high-voltage input. IC manufacturers have responded to that need with the application of high-voltage processes and offer control ICs that work to 50V and higher. That voltage is sometimes insufficient, and you need further design techniques to extend the input voltage. The buck converter in **Figure 1** represents one such technique. In addition to allowing circuit operation over a wide input-voltage range, the technique reduces power dissipation, because the control circuit does not operate directly from V_{IN}. The circuit uses a linear regulator and a source-switched driver to buffer a control IC from a line whose voltage is as high as 110V. When you apply the input voltage, current flows through resistor R_2 and zener diode D_2, clamping the gate voltage of FET Q_1 to 9.1V. C_2 reaches a voltage of approximately 6V, which is equal to Q_1's gate voltage minus its typical turn-on threshold of 3V. FET Q_1 now acts as a crude linear regulator and allows the control circuit to become active.

The source-switched driver of Q_2, Q_4, and Q_5 then comes into play to allow the supply to come into regulation. The TL5001's open-collector output switches to a low state to turn on the main power switch, Q_3. With the gate of FET Q_5 also held at 9.1V and the output pin of the TL5001 low, current flows through Q_5's

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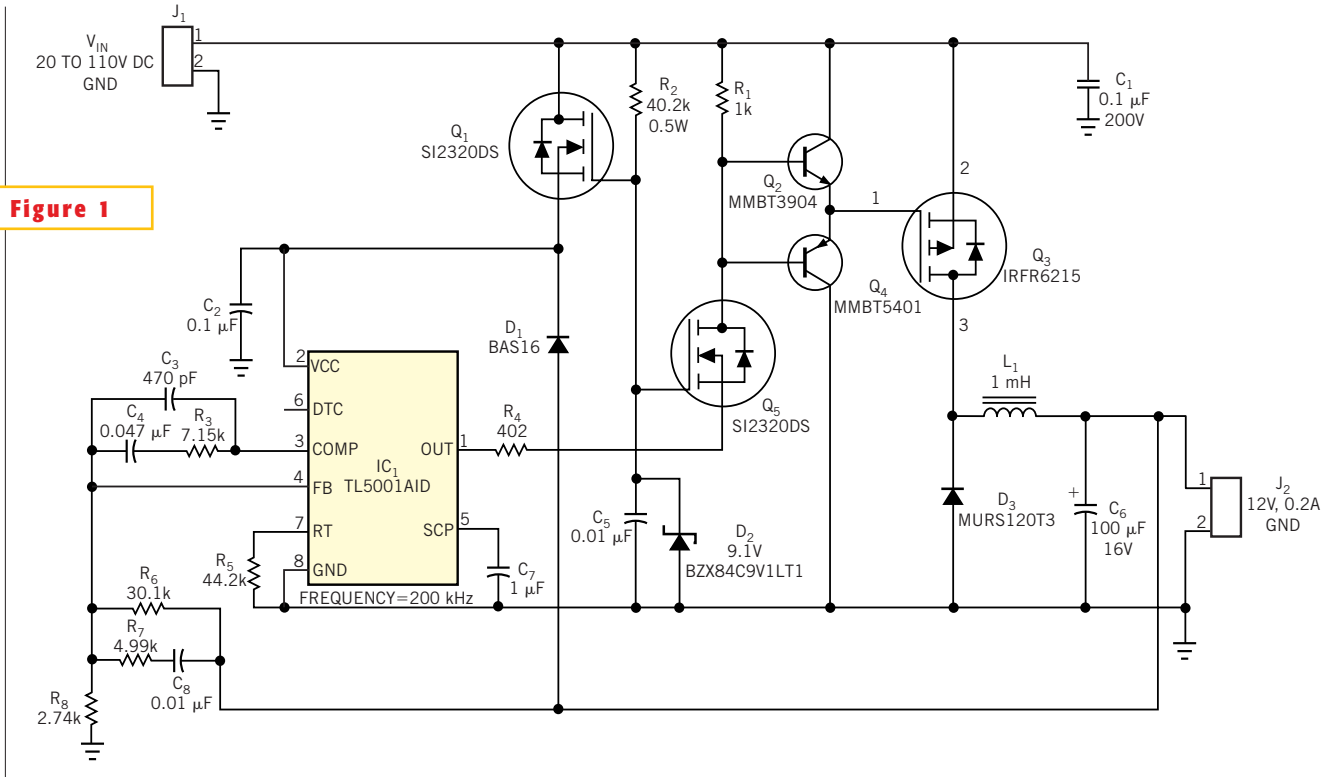
Figure 1



A buck converter uses switched-source gate drive to generate high output voltages.

drain-to-source pins. The amount of drain current that flows is equal to: (9.1V−Q_5's turn-on threshold−IC_1's Pin 1 saturation voltage)/R_4. In this example, this current is nominally approximately 12 mA. Because most of this current flows through R_1, the value of R_1 sets the voltage amplitude used for the gate drive of Q_3. With a value of 1 kΩ for R_1, the voltage across it is 12V. Transistors Q_2 and Q_4 form an npn/pnp pair to quickly switch gate-drive current into and out of Q_3. The base-emitter junction of Q_4 conducts when a voltage drop exists across R_1. This conduction quickly pulls down the gate of Q_3 from V_{IN} to approximately 11.2V (12V−V_{BE}). Because Q_3 is a p-channel FET, pulling the gate to 11.2V lower than the source turns it on. When current is not flowing in R_1, the base of Q_2 pulls up to V_{IN}, a voltage that forward-biases its base-emitter junction.

The gate of Q_3 quickly charges to near-V_{IN} potential, thereby turning off Q_3. This drive circuit is fast, because none of the transistors operates in a saturated mode; therefore, Q_3 can attain 0.5-µsec turn-on time. This speed means that the circuit can achieve reasonably high operating frequencies with the low duty cycles you encounter in a high-voltage input. You can scale this gate-drive circuit for higher or lower input voltages by the proper selection of the drain-source (or collector-emitter) ratings of Q_1, Q_3, Q_4, and Q_5. All must have voltage ratings greater than the input voltage, and all, except for Q_1, should also be able to switch at high speeds. The addition of diode D_1 offers two advantages. It allows the control circuit to operate after start-up from the output voltage, rather than the input voltage. This method is more efficient, inasmuch as the input voltage is relatively high. A bias-power savings of approximately sevenfold is the result. Also, adding D_1 pulls the source pin of Q_1 to approximately 11.2V, thus Q_1 turns off. All bias power to the controller now comes from the output voltage, and Q_1 no longer dissipates power.□

Active-clamp/reset-PWM IC becomes more versatile

Gowripathi and M Sindhu, ITI Ltd, Bangalore, India

The UCC3580 (www.ti.com), IC_1 in **Figure 1**, is an active-clamp/reset-PWM IC that has all the requisites of a power-supply IC except for current limit. You can use the shutdown pin (16) for this purpose (see the UCC3580 data sheet). But when the shutdown pin activates, the soft-start capacitor normally connected to Pin 15 discharges, and the converter starts again, resulting in hiccup mode. Poor dynamic response ensues because of this circuit behavior. The problem becomes especially serious when you hot-plug a load card, with typically 100-µF decoupling across the converter's output, into the motherboard. You can avoid this problem by not using the shutdown pin for current limiting. Instead, use the

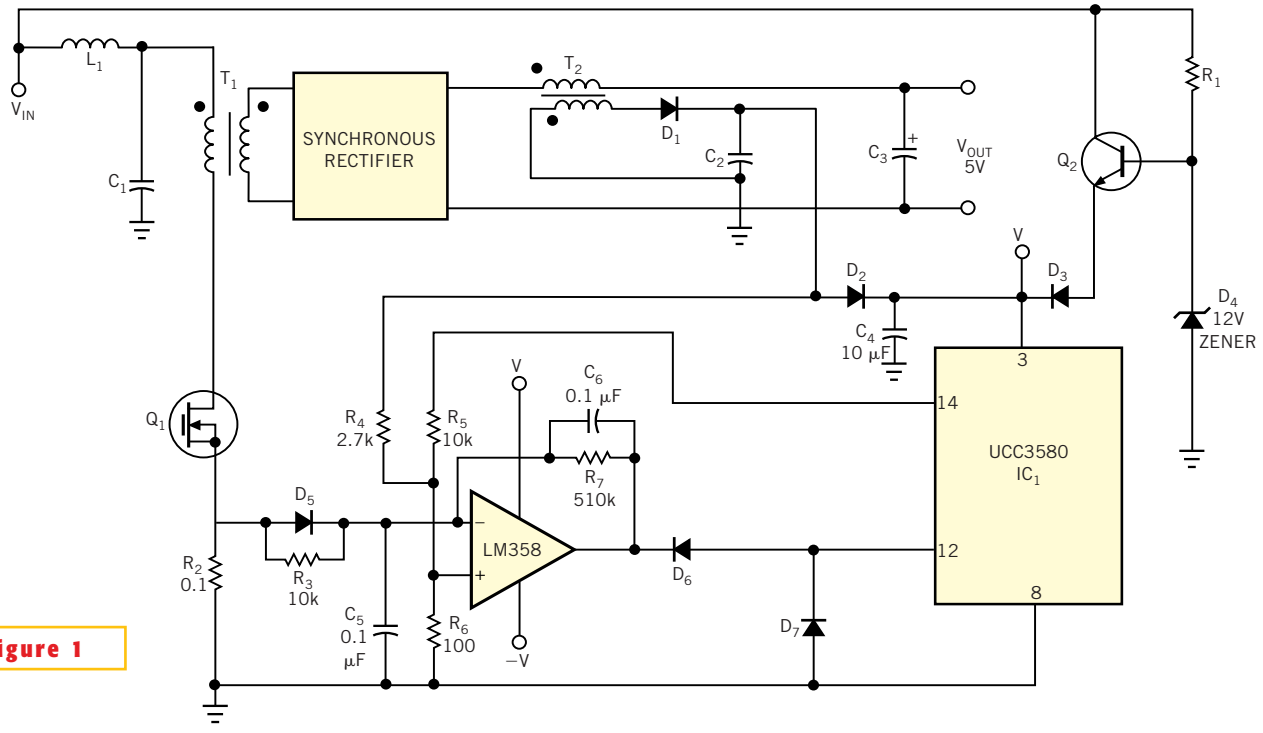


Figure 1

This circuit does not use the shutdown pin of the PWM IC; instead, it relies on the error amplifier's output to provide current limit.

error amplifier's output pin, Pin 12. Q_1 is the main switch, T_1 is the main transformer, and C_1 is the bulk capacitor. Q_2, D_3, and D_4 provide power (+V) for IC_1 during start-up and current limit. D_1 and C_2 rectify and filter the voltage from the auxiliary winding of T_2 to power the control circuit during normal operation. R_2 senses the current in the main switch, Q_1.

The LM358 op amp provides current limit. Diode D_6 isolates the op amp and Pin 12 of IC_1 during normal operation. According to the data sheet of UCC3580, the error amplifier's output should pull down to 0.3V or lower for 0% duty cycle. This condition forces you to use a negative supply (−V) for the op amp to obtain rated performance. As **Figure 1** shows, the same supply voltage (+V) serves for the PWM IC and the op amp. You can obtain the negative supply voltage (−V) for the op amp from another winding on T_2. Even though the voltages that T_2 generates decrease in foldback condition, the op amp continues to obtain +V from Q_2. A negative voltage (−V) from T_2 is adequate for proper operation of the op amp. The Schottky diode, D_7, from Pin 12 to ground protects the error amplifier's output from large negative voltages.

The inverting input of the op amp senses the peak pulse voltage across R_2. Diode D_5 helps C_5 to charge to peak voltage (peak detection), and R_3 helps to discharge C_5 when the peak voltage across R_2 decreases. Use a slow diode for D_5. The reference voltage at the noninverting input has two components—first, from the fixed 5V reference (Pin 14) of IC_1; second, from the voltage generated by the T_2 winding. This voltage decreases with output voltage, and voltage foldback occurs at the noninverting input. The 50-mV component from the fixed 5V reference is necessary for start-up. As the current limit starts, the output voltage starts to decrease, and the noninverting-input voltage also decreases, causing foldback. With this circuit, if the current limit starts at an output current of 10A, the output short-circuit current is 2A. The output recovers even with minimal current hysteresis. The positive voltage that the T_2 winding generates decreases from 13V just before current limit to 3V at short circuit. This circuit does not influence the transient response of the converter.□

Circuit provides hiccup-current limiting

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Current-limit protection is an essential feature for power-supply systems. The three major types of current-limit-protection mechanisms are constant, foldback, and hiccup. Hiccup current limit performs the best of the three types; however, the implementation is rather complex. In this scheme, upon detection of an overcurrent event, the whole power supply shuts down for an interval before it tries to power itself up again. The cycle repeats until the overcurrent fault disappears. With such operation, the dissipation in the power supply itself is minimal. You can incorporate the circuit in **Figure 1a** into the PWM circuit of a switch-mode power supply to implement the hiccup feature. **Figure 1b** represents a typical shunt-voltage regulator to regulate the V_{CC} that powers the PWM controller.

Most PWM controllers have an undervoltage-protection feature, in which the internal circuitry shuts down whenever its V_{CC} drops below a certain threshold. For example, assume that the circuit in **Figure 1a** works with a UCC3570 PWM controller. In this chip, an excessive current that causes the Count pin to exceed 4V or the ILIM pin to exceed 0.6V sets the shutdown latch. This action then forces the PWM controller's output to go low and discharge the soft-start capaci-

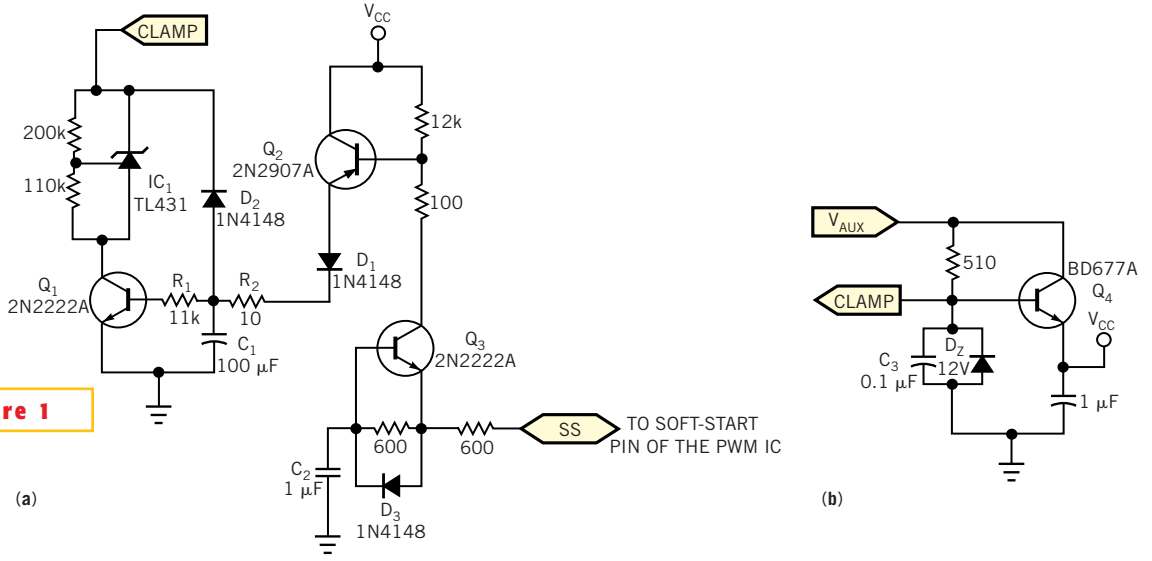

Figure 1

You can incorporate hiccup circuitry (a) into your PWM-control scheme, using a typical shunt regulator (b) to regulate the supply voltage to the PWM chip.

tor, C_2. The discharge current of C_2 causes Q_3 and, hence, Q_2 to turn on for a short interval to charge the timing capacitor, C_1. The moment the voltage across C_1 builds up, Q_1 turns on and activates IC_1 to overwrite the V_{CC} voltage, which D_Z initially set to a voltage—in this case, 7.02V—low enough to turn off the PWM controller (**Figure 1b**). With this action, the controller becomes temporary disabled, and the shutdown latch resets.

After C_2 completely discharges, Q_3 and Q_2 switch off, and the charge stored in C_1 continuously supplies the base drive needed to hold Q_1 on through R_1. The PWM controller then stays in sleep mode for the fixed interval, t_{SLEEP}, until the discharge current of C_1 can no longer keep Q_1 on. You can estimate this sleep-time interval (**Figure 2**) by using the following equation:

$$\frac{I_{IC1}}{h_{FEQ1}} \times R_1 = \left(V_{C1}(0) - V_{BEQ1}\right) \times e^{\frac{-t_{SLEEP}}{\tau}},$$

where I_{IC1} is the forward current of IC_1 ($\simeq$10.7 mA with V_{AUX}=12.5V), $V_{C1}(0)$ is the initial voltage stored in C_1 ($\simeq$5.05V), $\tau=R_1C_1$ ($\simeq$1.1 sec), h_{FEQ1} is the dc current gain of Q_1 ($\simeq$170 from test results), and t_{SLEEP} is the sleep time for the PWM IC ($\simeq$2 sec).

Note that, according to the 2N2222A data sheet, dc current gain can be 75 to 300. Therefore, to obtain a better prediction from the above equation, it is advisable to determine the dc gain through simple testing. To solve the equation, you must first determine $V_{C1}(0)$. This quantity depends on several factors. First, it depends on the PWM IC. The IC can discharge the soft-start capacitor either linearly (constant-current sink) or exponentially (RC discharge). Knowing this fact, you can work out the turn-on time, t_{ON}, of Q_3 and Q_2 by plugging t_{ON} and V_{CC} into the standard RC-charging equation with the time constant of $\tau_1=R_2C_1$. In **Figure 1a**, because $2.3\tau_1<t_{ON}<5\tau_1$, you can approximate $V_{C1}(0)$ by using $V_{C1}(0)=V_{IC1}-V_{BEQ4}-V_{CEQ2}-V_{D1}$.

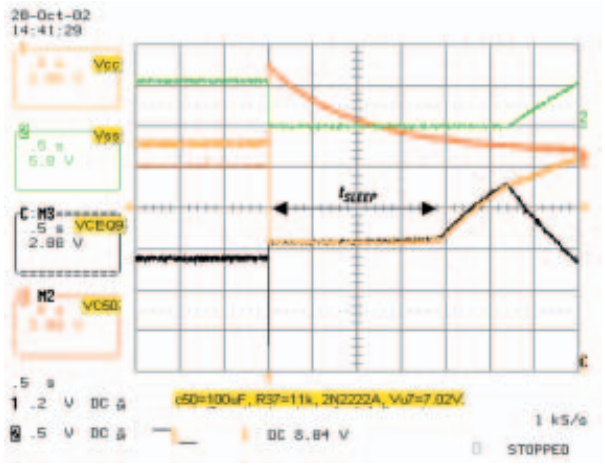

Figure 2 A scope display shows the relevant waveforms during hiccup operation. Trace 1 is the V_{CC} output voltage of the shunt regulator, Trace 2 is the soft-start voltage of the PWM controller, Trace C is the collector-emitter voltage of Q_3, and Trace B is the voltage across timing capacitor C_1.

After time period t_{SLEEP} elapses, C_1 should have discharged to a low enough voltage to turn off Q_1, thereby allowing V_{CC} to climb back to its normal value, thus enabling the PWM controller. The soft-start capacitor then charges up again. The output pulse gradually starts to generate after the soft-start voltage reaches the internal threshold. This "sleep-reboot-detect" cycle repeats until the fault disappears.□

Microcontroller provides SRAM battery backup

Dave Bordui, Cypress Semiconductor, Orlando, FL

To maintain content in the event of power loss, many designs that include SRAM require a dedicated device that can automatically switch from a standard power supply to battery operation. Microcontrollers seldom find use in power-switching applications. Because microcontrollers typically operate from the primary power supply, they stop execution if that supply drops, thereby making it impossible to perform the switching operation. However, by using a characteristic of many microcontrollers, you can perform this switching function without interruption to the SRAM (**Figure 1**). Many microcontrollers have internal protection diodes on their I/O pins. Therefore, if the V_{CC} pin is left floating, the CPU in many instances powers up and runs if you apply power only to an I/O pin. With this fact in mind, you can create an "automatic voltage switch" by connecting the main power-supply rail and a secondary battery backup to two separate I/O pins of the microcontroller. The microcontroller can then have firmware that drives a third I/O to a logic-high (source) mode or otherwise source current to an output pin. This output then provides the uninterrupted power to the external low- power SRAM device.

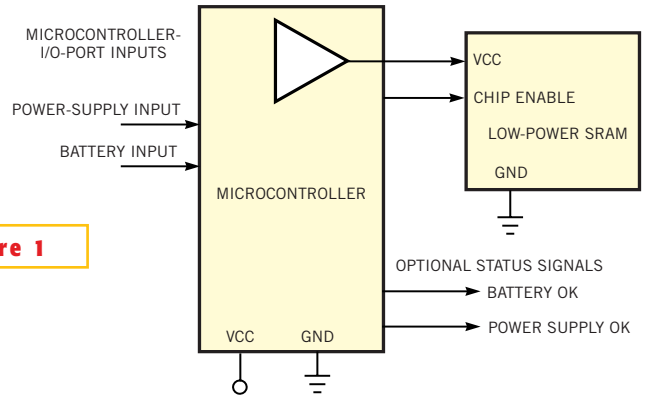

Figure 1 A microcontroller can power up and run even if its V_{CC} pin is floating.

When the V_{CC} rail is present, the mi-

crocontroller draws current from the V_{CC} pin and operates normally. If the V_{CC} rail drops below the battery-input voltage, the microcontroller automatically draws current from the battery instead. Although this scenario requires no firmware whatsoever, many microcontrollers can run firmware and continue execution throughout this power-supply transition. Continuing the microcontroller's firmware execution allows other firmware-based functions, such as deassertion of SRAM chip enable, battery- and rail-health indication, and analog-to-digital conversion. When you use this technique, you must take care to ensure that the entire design draws less current than the forward-bias-current rating of the protection diode. Also, the external SRAM circuit must draw no more current than the microcontroller's output can source. This stipulation remains true whether the V_{CC} rail or the battery provides power. It is also important to realize that, because the protection diodes are sourcing the power, a slight voltage drop exists on the microcontroller's uninterrupted-power-supply output. This voltage drop is equivalent to the one that the microcontroller's manufacturer specifies. You should consider this drop when you select the battery, V_{CC} rail, and external-SRAM voltage requirements.□

Positive regulator makes dual negative-output converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Some systems, such as optical networks, require more than one negative voltage. A common procedure is to boost the main negative supply of −5V to −10V and then reduce it with a linear regulator to −9V. The −5V itself comes from a positive supply, typically 5 or 12V. Independently creating each of the two negative voltages requires the use of two switching-regulator ICs. However, a simpler approach uses only one step-down switching regulator and creates both a negative output with low ripple current and a second output with twice the voltage. The circuit in **Figure 1** is a positive-to-dual-negative dc/dc converter that converts 5V to both −5V and −10V, using a positive buck regulator. This configuration is not a usual application circuit of a positive buck-regulator IC, which you would typically find in single-output step-down applications. However, by rearranging the connections to ground and V_{OUT}, the dc/dc converter becomes a common positive-to-negative converter.

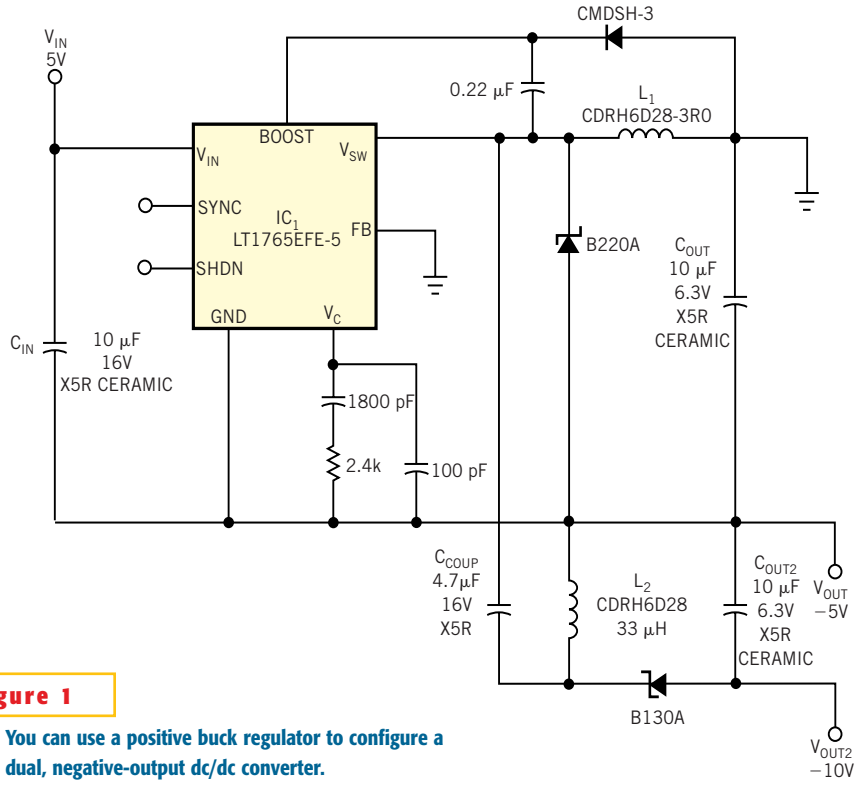

Figure 1

You can use a positive buck regulator to configure a dual, negative-output dc/dc converter.

The circuit features an additional negative-output stage with twice the voltage of the first output by using a second inductor, a catch diode, and an output capacitor. The circuit includes a coupling capacitor, C_{COUP}, for energy transfer to the second winding and offers regulation of the secondary output without feedback. The use of two inductors, as opposed to one transformer, can provide a flexible circuit layout. This circuit measures less than 3 mm high and delivers high load current (**Figure 2**). You can replace the two inductors with a single 1-to-1 transformer, but even at the high 1.25-MHz switching frequencies, it may be difficult to find a less-than-5-mm-high transformer that can do the job. The LT1765 buck regulator provides high current capabilities even with small inductors and all-ceramic coupling, input, and output capacitors, thanks to both its 1.25-MHz switching frequency and its 3A on-board power switch.

Figure 2 shows the output capability for the circuit in **Figure 1**. The load current on one output determines the maximum available load current on the other. At maximum output current, the peak

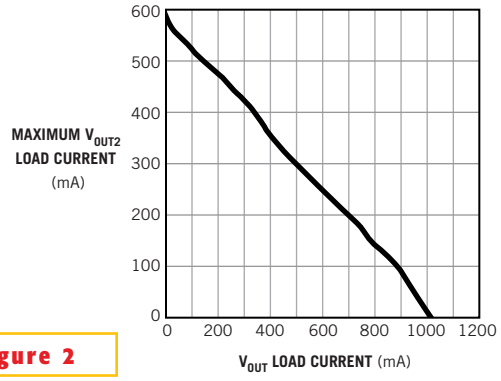

Figure 2

The circuit delivers high maximum currents available from the two outputs in the circuit of Figure 1.

switch current (the sum of the peak inductor currents) is equal to 3A. Forcing the output current higher than the maximum value can cause the output voltage on both lines to collapse and lose regulation. The single feedback signal directly monitors V_{OUT}, but the low-impedance ceramic coupling capacitor with an extremely high rms current rating keeps V_{OUT2} well-regulated. As load conditions change on both V_{OUT} and V_{OUT2}, V_{OUT2}'s regulation becomes slightly compromised over different load conditions. V_{OUT2} can become unregulated if the load current on V_{OUT2} becomes extremely small. A preload of 5 mA on V_{OUT2} is necessary to maintain regulation if the load current falls below 5 mA. Zero load current on V_{OUT} does not cause the converter to lose regulation. Cross-regulation typically stays within 1% of the typical output voltage, an excellent rating for a single-feedback, dual-output converter. **Figure 3** shows typical efficiency curves for various values of the load current on V_{OUT2}.□

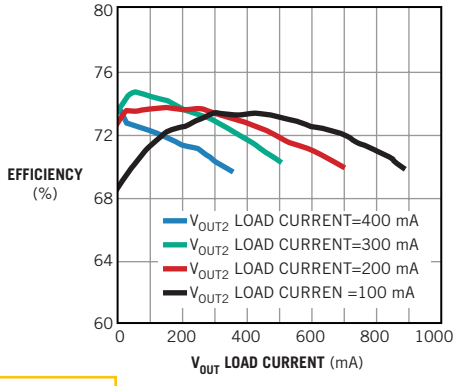

Figure 3

The circuit in Figure 1 has high conversion efficiency for various values of load current.

Analog switch frees stuck I²C bus

Bob Marshall, Philips Semiconductor, Morgan Hill, CA

THE DUAL-CHANNEL PCA9540 I²C multiplexer often breaks up an I²C or SM bus or allows you to use devices with the same addresses on the same bus. When the PCA9540 initially powers up, it comes up in a state in which both channels are deselected. The I²C- or SM-bus master can then address the control register in the PCA9540 to select either Channel 0 or Channel 1, connecting the master to the appropriate channel. The I²C bus can then address downstream devices on the selected channel. If a failure occurs in one of the downstream channels, such that the I²C bus is stuck at high or low, the I²C-bus master could become disabled. Because the PCA9540 has a power-on-reset function that initializes the multiplexer with all channels disconnected, this feature can free the bus. In some applications, however, powering down the entire system may be impractical. One way to avoid powering down the entire system is to install a low-on-resistance analog switch in series with the power-supply line of the multiplexer (**Figure 1**).

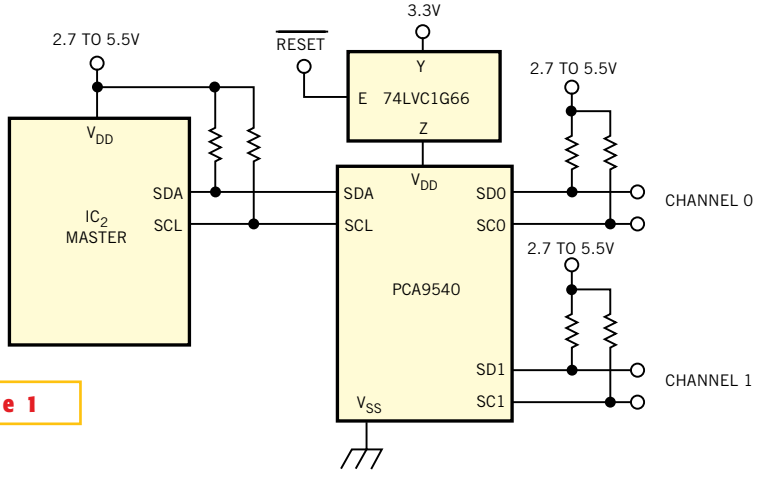

Figure 1

To free up a stuck I²C bus, this circuit controls the supply voltage to force a hardware reset.

When the enable pin of the 74LVC1G66 goes low, the supply voltage disconnects from the multiplexer, thereby freeing up the I²C bus. The I²C master or any other system controller can generate this hardware reset. The 74LVC1G66 is available in a 2-mm² package, so the circuit takes up little additional board space. This example uses the PCA9540, but you can use the 74LVC1G66, with a typical on-resistance of approximately 6Ω, to selectively control the power for any device that has a power-on-reset function. Its size and wide operating-voltage range also make it practical to selectively power down sections of any circuit in power-sensitive applications.□

design ideas

Edited by Bill Travis

DDS device produces sawtooth waveform

Niamh Collins, Analog Devices, Limerick, Ireland

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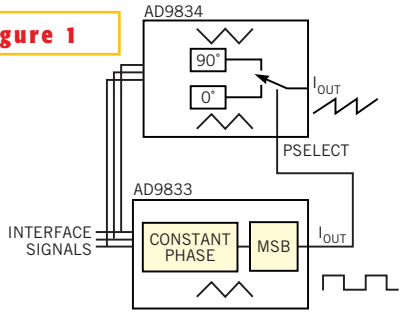
Ramp or sawtooth waveforms are useful for a broad range of applications, including automatic-test equipment, benchtest equipment, and actuator control. Discrete components typically set the waveform frequency. Unfortunately, drift in these component values over time and temperature limits the accuracy of the output frequency. Also, changing the frequency requires that you use a different set of components. This Design Idea describes a flexible implementation of a sawtooth waveform generator (**Figure 1**) using two DDS (direct-digital-synthesis) devices. The frequency of the sawtooth is digitally programmable, so the design requires no external components to set the frequency. A DDS device, a programmable waveform generator, can deliver sine, square, and triangular (up/down ramp) waveforms. You can digitally implement changes in phase or frequency by loading onboard registers. Using the phase registers, the DDS chip can generate two linear up/down ramps of the same frequency but with a 90° offset. The up ramp of one occurs at the same time as the down ramp of the other. Selecting a phase register causes the signal from that register to go to the output. A sawtooth waveform occurs when the only the "up ramp" of each signal is directed to the output. The AD9833 delivers the MSB of the phase register, thus producing a digital signal at the frequency of the up/down ramp. This signal connects to the PSELECT pin on the AD9834, which controls switching between the phase registers.

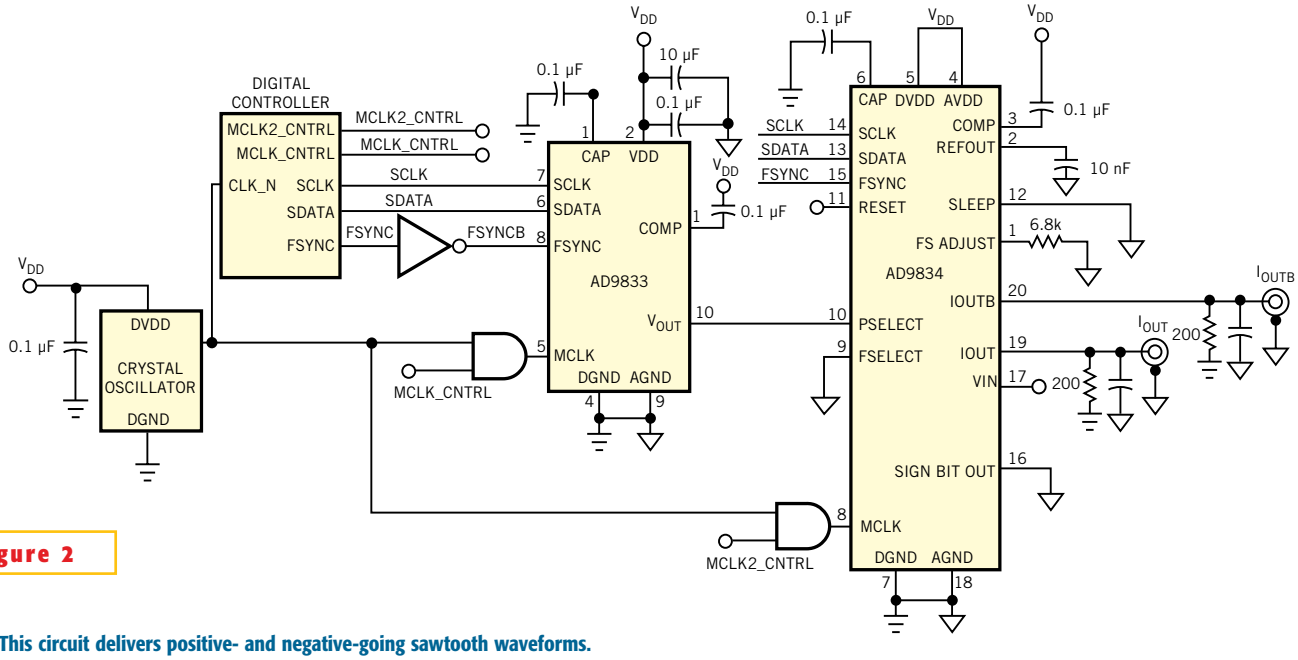
Latency in the devices means that you see the effect of switching between the phase registers on the output only after

Figure 1



Two DDS chips provide a convenient way to generate sawtooth waveforms.

Figure 2



This circuit delivers positive- and negative-going sawtooth waveforms.

seven MCLK (master clock) cycles. Controlling the MCLK signals of both devices so that one MCLK is inactive for a number of clock cycles can overcome this inherent latency. **Figure 2** illustrates how the two devices connect. The connections to the interfaces of the two devices combine so that they can accept programs from the same digital controller. The AD9833 is connected such that FSYNC is active high; the AD9834 is connected such that FSYNC is active low. In this way, the controller has to control only three signals instead of six. The AD9834 is configured so that the frequency and phase are controlled via the pins. This configuration allows the digital output from the AD9833 to control phase-register selection by simply connecting it to the PSELECT line. Two analog outputs from the AD9834, IOUT and IOUTB, deliver complementary sawtooth waveforms (**Figure 3**).

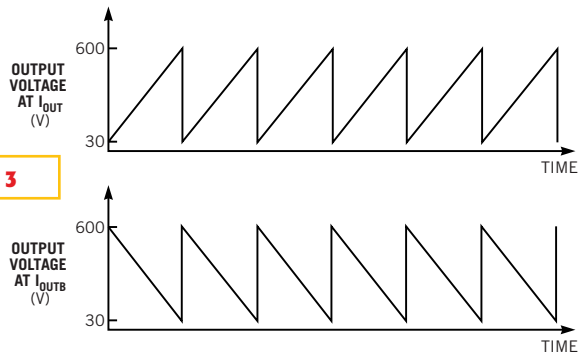


Figure 3

The up ramp of the upper waveforms occurs at the same time as the down ramp of the bottom waveform.

A RESET (Pin 11) signal initializes the devices. This initialization can occur in the same way for both devices, using the control register. This operation requires a control word with the RESET bit set to 1. The frequency and phase registers of both devices are then ready to load with data. Because of the switching involved in creating the sawtooth waveform, its frequency is twice that of an equivalent triangular waveform:

$$f_{SAWTOOTH} = \frac{F_{WORD}}{2^{27}} \times f_{MCLK},$$

where F_{WORD} is the frequency word loaded in both devices.

The AD9834 phase switches between 0 and $\pi/2$. Following instructions in the IC's data sheet, you should therefore load Phase Register 0 with 0 and Phase Register 1 with 0x800 (which corresponds to a 90° phase shift). The AD9833's phase is always set to $\pi/2$, so you should therefore load Phase Register 0 with 0x800. Once the MCLK of the AD9833 begins to run and after seven MCLKs of latency, the output of the AD9833 changes because of the $\pi/2$ phase shift in Phase Register 0. You can deactivate RESET through the control register once the registers are loaded with data. In the same control word to the AD9834, you should set the MODE bit to 1, which results in the selection of the triangular waveform as the output waveform, and you should set PIN-SW to 1, so that the pin controls phase-register-select function. And, for the AD9833, you should set the OPBITEN bit to 1 to enable the digital output. You should set the DIV2 bit to 1 so that the digital output is not divided by 2, and set the SLEEP12 bit to 1 because the DAC is not being used. For the system to implement the sawtooth, there must be an offset between the times when the MCLKs of both devices begin to run. You calculate the offset as follows:

$$\text{OFFSET} = \left[\text{ROUND}\left[\left[\frac{2^{28}}{F_{WORD}}\right] \div 4\right] - 7\right].$$

If, for example, Offset=10, then the MCLK of the AD9834 should run for 10 cycles before the MCLK of the AD9833 starts running. From then on, the ICs should be synchronous. A negative value of Offset indicates that the MCLK of the AD9833 should start running first.

This Design Idea provides a flexible method for generating a sawtooth waveform. The frequency is digitally programmable, and the design requires no external components to change the frequency. The frequency does not change with component drift over time or temperature.□

Circuit makes universal VCSEL driver

Andrzej Wolczko, Institute of Electronics AGH, Krakow, Poland

VCSELs (vertical-cavity surface-emitting lasers) are commercially available infrared semiconductor lasers with $\lambda \simeq 850$ nm. Short-cavity-length, high-quality Bragg mirrors impart properties to VCSELs that differ from those that earlier Fabrey-Perot lasers impart. The emission characteristics—optical power, P_λ, versus diode current—shows threshold and operating currents of approximately 3 and 13 mA, respectively, for the Lasermate TSC-M85A416 VCSEL. Such values are typical for this type of laser (**Figure 1**). The current characteristics are nearly independent of temperature. Thanks to their low operating current, effective coupling to multimode fibers, high-speed switching, and low price—about one-third that of a Fabrey-Perot laser—VCSELs may replace LED light sources in short fiber-optic links. The MC10EP89 ECL coaxial VCSEL driver allows the circuit to switch current with less-than-1-nsec rise and fall times (**Figure 2**). The IC delivers a voltage swing of

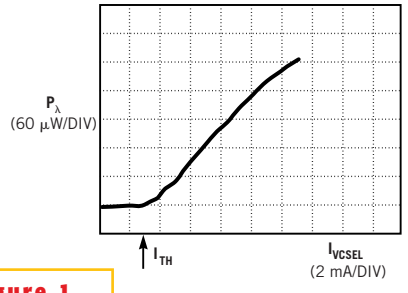


Figure 1

A VCSEL has threshold and operating currents of approximately 3 and 13 mA, respectively.

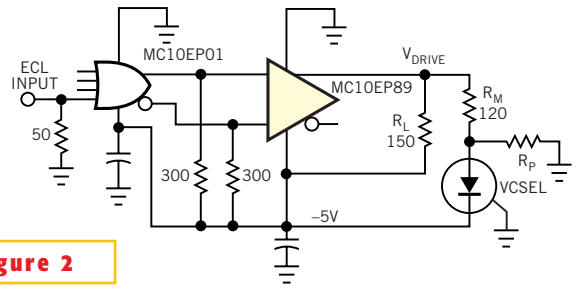


Figure 2

This universal VCSEL driver allows you optimize the circuit for any type of laser diode.

1.6V minimum to a 75Ω load (**Figure 3**).

The 120Ω resistor, R_M, limits the amplitude of the pulse current, and R_P determines the initial polarization current of the laser. For $R_P=\infty$, the laser practically switches off during the low state of the driver. You must load the MC10EP89 with resistor R_L for proper operation of the IC. You can optimize the values of R_M and R_P for each type and characteristic (individual emission parameters) of the VCSEL you select. Because of the dynamic resistance of the laser, the voltage drop across the junction varies from approximately 1.9 to 2.2V within the full current range. Therefore, you should consider this variation when you calculate R_M and R_P. In turning off the optical power of the VCSEL, you observe some residual emission (tail) in the optical-pulse response (**Figure 4**). If the current falls to zero ($R_P=\infty$), the tail is shorter and smaller, but the optical-power amplitude also decreases.

The oscillogram represents the response of a 155-Mbps laser (**Figure 4**). VCSELs for 622 and 1250 Mbps are also available from Lasermate. The MC10EP89 needs symmetrical drive; the input OR/NOR gate works as an asymmetrical/symmetrical ECL converter. The laser's good thermal properties eliminate the need to provide a complicated stabilization loop for the optical power. The entire circuit is dc-coupled and operates with constant optical power amplitude for each binary code, and the circuit is insensitive to bit patterns. A slow-start circuit is unnecessary. Because of the operating speed, you must carefully design the pc board according to high-frequency rules: Keep connections as short as possible, use surface-mount components, and carefully perform decoupling, for example. You must ground the metal case of the laser and isolate it from the chip.□

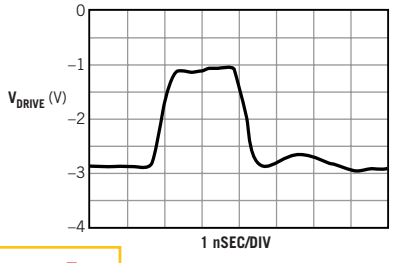


Figure 3

The driver in Figure 1 switches 1.6V into 75Ω with less-than-1-nsec rise and fall times.

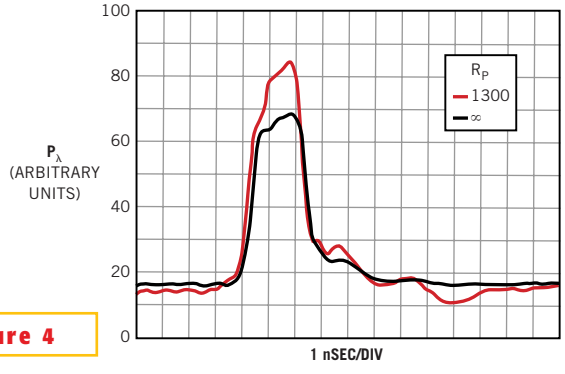


Figure 4

These curves show the VCSEL's response with R_P open and R_P=1300Ω.

Circuit level-shifts ac signals

Ron Mancini, Texas Instruments, Bushnell, FL

AC SIGNALS CAN EMANATE from many sources, and many of these sources are incompatible with the most popular interface voltages, such as TTL. A temptation always exists to capacitively couple the ac signals because capacitive coupling strips off the dc level. Capacitive coupling sometimes doesn't work, because the coupled signal's voltage swings around ground, so you have to add dc offset to make the coupled signal compatible with the interface voltage. Also, the coupled signal contains a dc content, V_{DC}, which varies with pulse width, and the dc variation interferes with the interface voltage when the signal swing is large. This circuit completes the signal interface by measuring the dc offset, adding appropriate compensation to the capacitively coupled signal and adding an adjustable-dc- level feature (**Figure 1**). R_1 and C_2 form a lowpass filter (f_{3dB}=0.312 Hz) that measures the dc content of the input signal. The transfer equation is the following:

$$V_A=\left[\frac{V_{IN}R_3+V_{REF}(R_1+R_2)}{(R_2+R_3)(R_1C_2s+1)+R_1}\right]\bullet\left[\frac{R_F+R_G}{R_G}\right].$$

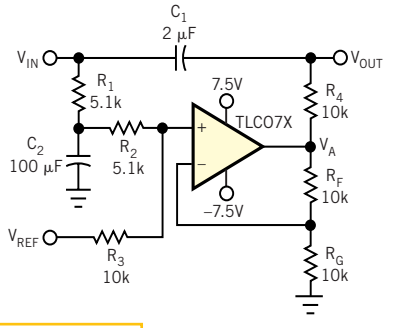


Figure 1

This circuit is a universal level shifter for ac signals; it accommodates any interface standard.

When $R_1+R_2=R_3$ and $R_F=R_G$, V_{DC} transfers to the output signal, V_A, because it is multiplied by 1/2(2)=1 or a gain of one. The output voltage for the same resistor values contains V_{REF}; thus, the output signal is level-shifted by the voltage, V_{REF}, not V_{REF} plus the V_{DC}. When the input signal's duty cycle changes, rather than the output voltage's changing with duty cycle, the op amp keeps the output-voltage level constant. The gain for the V_{DC} must be one, so that it cancels the voltage shift after ac-coupling. The gain for the reference voltage can be greater than one; for example if $R_1+R_2=3R_3$ and $R_F=3R_G$, the dc content is 1/4(4)=1, and the reference-voltage gain is 3/4(4)=3. V_{REF} can be positive or negative, so you can obtain TTL, CMOS, or ECL logic levels with this circuit. The time constant formed by C_1 and R_4 must be large enough to pass the lowest frequency signal without distortion. The value of R_4 is not critical, as long as the op amp can drive R_4 without losing too much signal swing. In some cases, you can size R_4 to present the driving-point impedance you need to eliminate near-end reflections. The circuit easily couples 400-MHz data as configured, but the data rate depends on the time constant formed by R_4 and the input impedance of the driven circuit.□

Interface a serial 12-bit ADC to a PC

DS Oberoi and Harinder Dhingra, GCET, Jammu, India

Over the years, IC manufacturers have devised various ways of effecting interfaces and paying special attention to reducing the number of ICs' interface-I/O pins. The MAX187 is one such device, a 12-bit A/D converter. You can create an interface to this ADC using serial data-communications techniques. Analog-to-digital conversion and data transfer from MAX-187 require only three digital-I/O lines. You can create a simple interface between the MAX187 and a PC using the computer's Centronics printer port (**Figure 1**). You enable or disable the MAX187 by setting the $\overline{SHDN}$ pin (Pin 3) to high or low level, respectively. If you leave this pin open, then the internal reference (4.096V) becomes disabled, and you must apply an external voltage reference to REF (Pin 4). Otherwise, this pin connects to a 4.7-µF bypass capacitor, C_1. The digital data from the MAX187 transfers to the processing unit one bit at a time by using an external clock at SCLK (Pin 8).

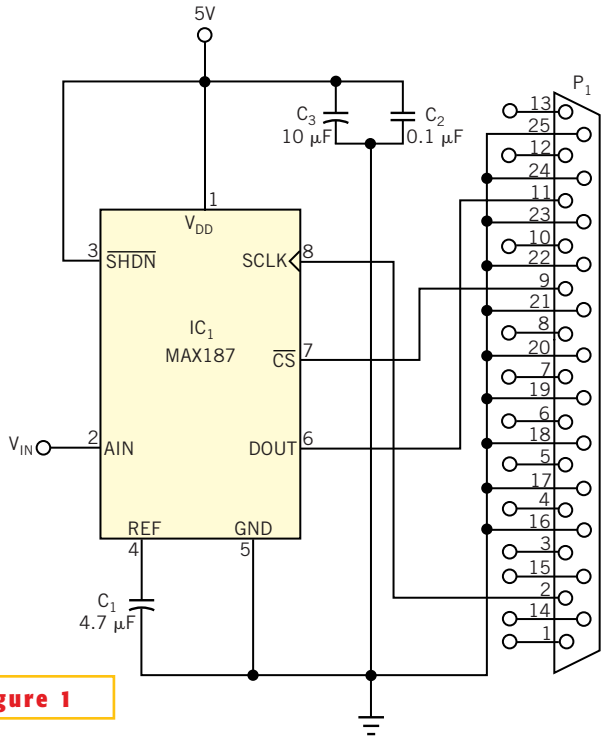


Figure 1 It's easy to effect an interface of a 12-bit serial ADC to a PC.

A complete data transfer requires 13 external clock pulses. The first clock pulse's falling edge latches the first data bit (the MSB) at the DOUT pin (Pin 6). The output data bit changes at the falling edge of the next external clock, and you can read the serial data bits until the appearance of the falling edge of the next clock cycles. The analog-to-digital conversion starts when the ADC's $\overline{CS}$ pin (Pin 7) goes low. This pin must remain in the low state until the complete cycle of conversion and subsequent serial-data transfer has taken place. A change of state in the DOUT pin from low to high level indicates the EOC (end-of-conversion) status. Then, serial 12-bit data is available for transfer. Software controls the MAX187's operation. The software should be able to generate all the control signals for successful conversion and also should be able to detect the EOC status. It should also be able to generate 13 external clock pulses to read serial 12-bit data and convert it into parallel data.

The software for the MAX-187's operation is in Turbo C++, Version 3.0 (which you can download from the Web version of this Design Idea at www.edn.com). In the code, Port defines the Centronics port of the PC to which the MAX187 interfaces. Write Port defines the port for initiating the analog-to-digital conversion and generating the external clock pulses. Read Port defines the port for reading the EOC and serial data from the ADC. After pulling CS and SCLK low, the EOC loop checks for the EOC status. If a valid EOC does not appear, this loop remains operational. As soon as a valid EOC appears, the first of the 13 clock cycles appears, which latches the first data bit (MSB). After this action, the routine calls a subroutine (get_adc()). The subroutine generates the rest of the external clock cycles to read the 12 bits of serial data. The function also converts the received serial data into parallel data (adc_val). It converts by multiplying the previous data by two by shifting adc val to the left by one bit and adding one to the parallel data if the serial bit's value is one. Once the parallel data is available, the function returns the value and displays it on the screen.□

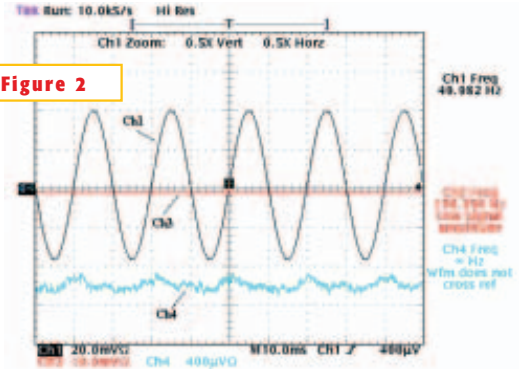
Safety device uses GMR sensor

J Pelegri-Sebastia and D Ramirez-Munoz, University of Valencia, Spain

THIS DESIGN IDEA presents a differential safety device to prevent risks arising from current leakages in household applications. The proposed circuit uses a new method for differential current sensing (**Figure 1**). The method entails the use of Helmholtz coils and a magnetic sensor based on the GMR (giant-magnetoresistive) effect. The AC004-01 magnetic sensor from NVE (www.nve.com) uses GMR technology (**Reference 1**). Two Helmholtz coils carry the household's input current. If no differential current between phase and ground exists at the center of the coils, then the magnetic field is uniform and null. But, in the presence of an unbalanced magnetic field, corresponding to a leakage current to ground, a differential magnetic field appears at the center of the Helmholtz coils (**Reference 2**). Thus, the sensor's output is a nonzero voltage that the circuit in **Figure 1** amplifies and compares with a preset reference voltage. The reference voltage corresponds to the highest allowable leakage current—generally, approximately 30 mA.

The sensor's output, a differential voltage, connects via a highpass filter to an INA118 instrumentation amplifier, a device with high common-mode rejection (**Reference 3**). This stage converts the sensor's differential signal from a Wheatstone-bridge arrangement to a unipolar output with an appropriate gain figure. This output goes through a half-wave rectifier and a lowpass filter and becomes a dc signal. If this signal is greater than V_{REF1}, then the MOC3041 optotriac turns off, thereby interrupting the power to the household appliance.

Figure 2



The sensor's output (Channel 4) is zero because the differential line current is zero.

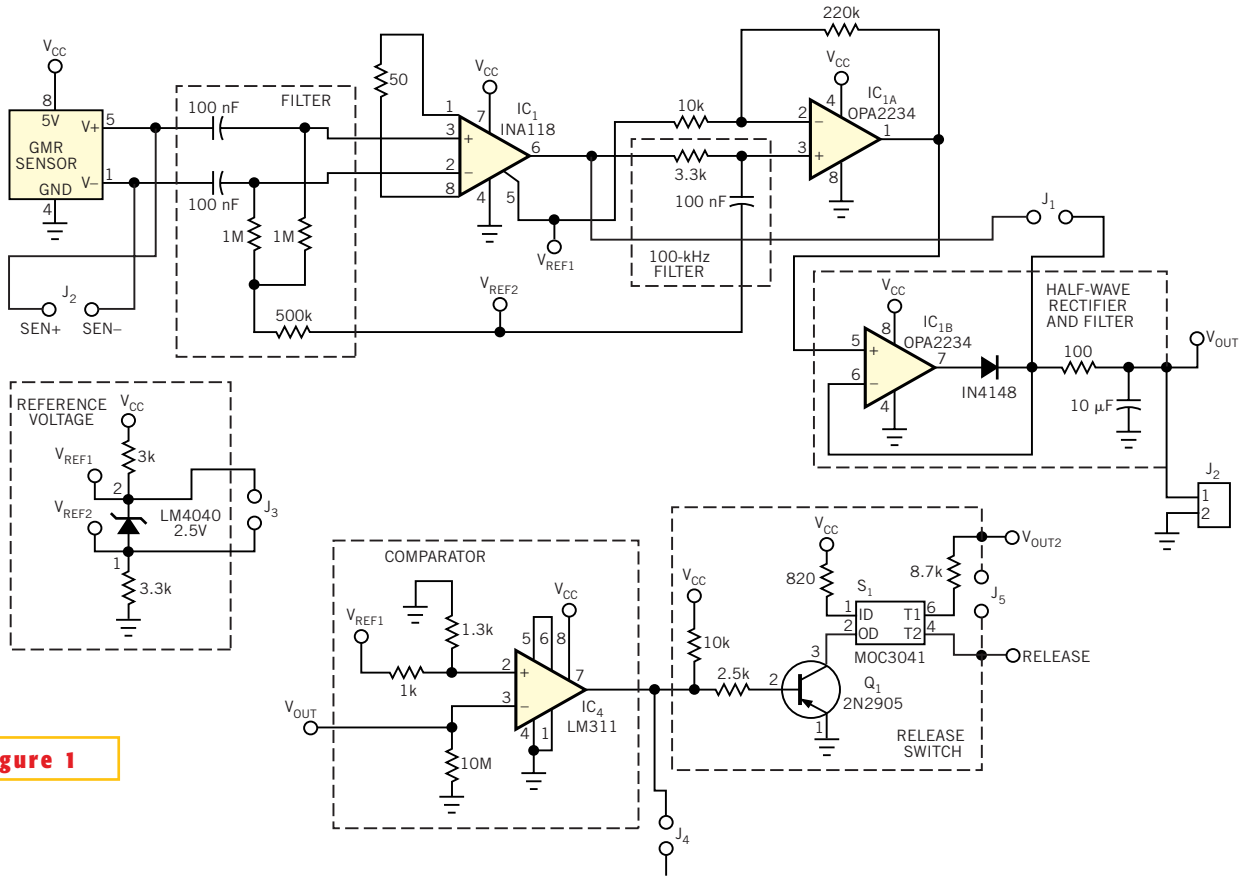
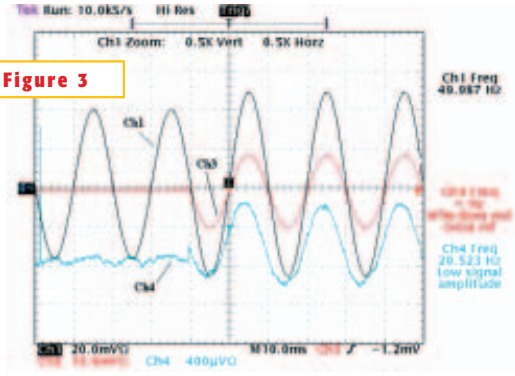


Figure 1

This circuit uses a GMR sensor to detect and disable dangerous differential line currents.

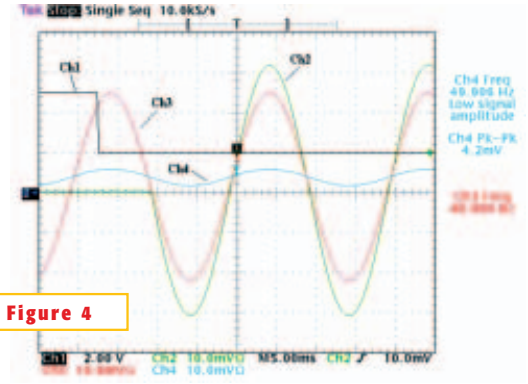
Figures 2 and **3** depict two scenarios. The Channel 1 trace represents the line current; Channel 2 shows the current circulating through the line; and Channel 4 represents the sensor's output, which is proportional to the difference between line and ground currents. In **Figure 2**, the sensor's output is zero because the current difference is null. **Figure 3** shows a ground current that generates a nonzero magnetic field in the sensor. In **Figure 4**, the ground current is greater than 30 mA. The comparator changes state, activating the optotriac (Channel 1) and turning on the relay (Channel 2, 20 mA/division). Channel 3 shows the live current, and Channel 4 shows the sensor's output (1 mV/division).□

Figure 3



A ground current generates a nonzero magnetic field in the sensor (Channel 4).

Figure 4



The ground current exceeds 30 mA. An optotriac and a relay disconnect power to the household appliance.

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3. Casas, O, and R Pallas, "Basics of analog differential filters," *IEEE Transactions on Instrumentation and Measurement*, 1996.

Edited by Bill Travis

Clip extracts signal from phone line

Maxwell Strange, Fulton, MD

Using a capacitive-coupled clip, you can pick up the signal from a twisted-pair or -wire telephone line or from other unshielded analog lines without piercing the insulation. No line test can detect the clip's presence, and it leaves no evidence of having been attached. It needs no ground return. You can fasten the small, insulated pickup plates to the opposing jaws of an alligator clip for quick and easy attachment. Balanced lines from the plates connect to the inputs of a high-impedance differential amplifier (**Figure 1**). For this scheme to have satisfactory signal-to-noise and frequency-response parameters, the clip, connecting cable, and amplifier must m be attached parallel to the signal wire and must be as long as is conveniently possible—an inch or more—and preferably slightly curved to maximize the coupling capacitance. (For a twisted-conductor line, the plates should not be longer than the twist "wavelength" to avoid signal cancellation.) You should orient the clip for the cleanest signal output.

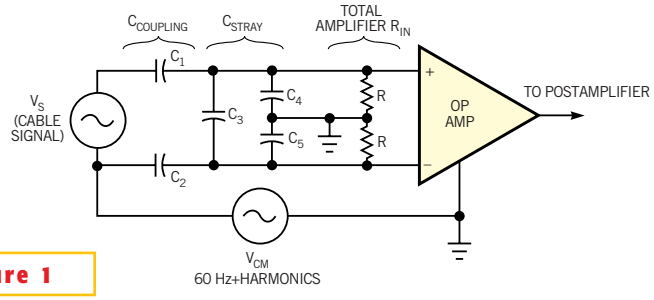

Figure 1

In this equivalent circuit, you should maximize the coupling capacitances, C_1 and C_2, and minimize the stray capacitances, C_3, C_4, and C_5.

The clip, its connecting cable, and the amplifier must be shielded to minimize interference, typically comprising 60-Hz signals and their harmonics from power-line fields. The cable should have good electrical symmetry and low total capacitance between conductors and to the shield. Thus, the amplifier must be near the clip. The amplifier should have high input resistance, low current noise, and adequate common-mode rejection.

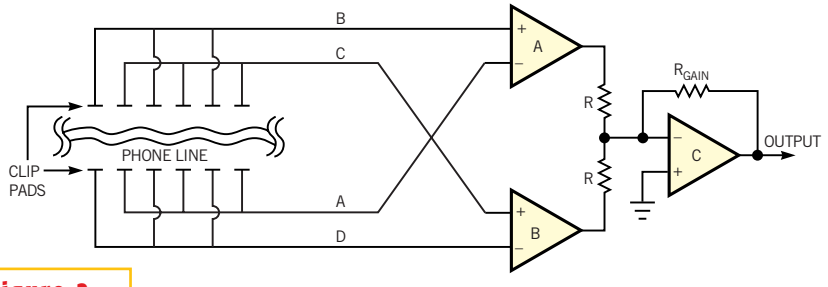

Figure 2

A multiple-pad approach produces cancellation of equal noise that the opposed pad pairs pick up.

The clip's coupling capacitance and stray capacitance and the amplifier's input resistance determine the low-frequency cutoff of the detected signal. Stray capacitances in the clip and in its connecting cable to the shield are generally much larger than the coupling capacitance. Thus, voltage-divider action reduces the signal, but the stray component adds to the capacitance the amplifier's input sees and reduces the circuit's noise by the square root of the signal attenuation. The noise reduction accrues from reducing the needed input resistance. Therefore, you generally don't need the complication of an insulated "bootstrapped" shield. You can follow the amplifier with a nearby or remotely located postamplifier for more gain and bandpass filtering to optimize the signal-to-noise performance. A telephone signal has a bandwidth of approximately 300 Hz to 3 or 4 kHz. A sharp highpass cutoff at 300 Hz effectively rejects power-line noise pickup. A simple, two-pole, Sallen-Key Butterworth filter works well. You can trim it to provide some high-frequency peaking to obtain the most intelligible signal.

A multiple-pad pickup scheme improves noise rejection (**Figure 2**). The circuit's arrangement is such that even-numbered pads on one side and odd-numbered pads on the other side pick up equal noise that produces opposite-phase outputs from op amps A and B. Op amp C then sums the signals and rejects the noise. The desired difference signal, however, appears in-phase at the outputs of A and B, so both op amps con-

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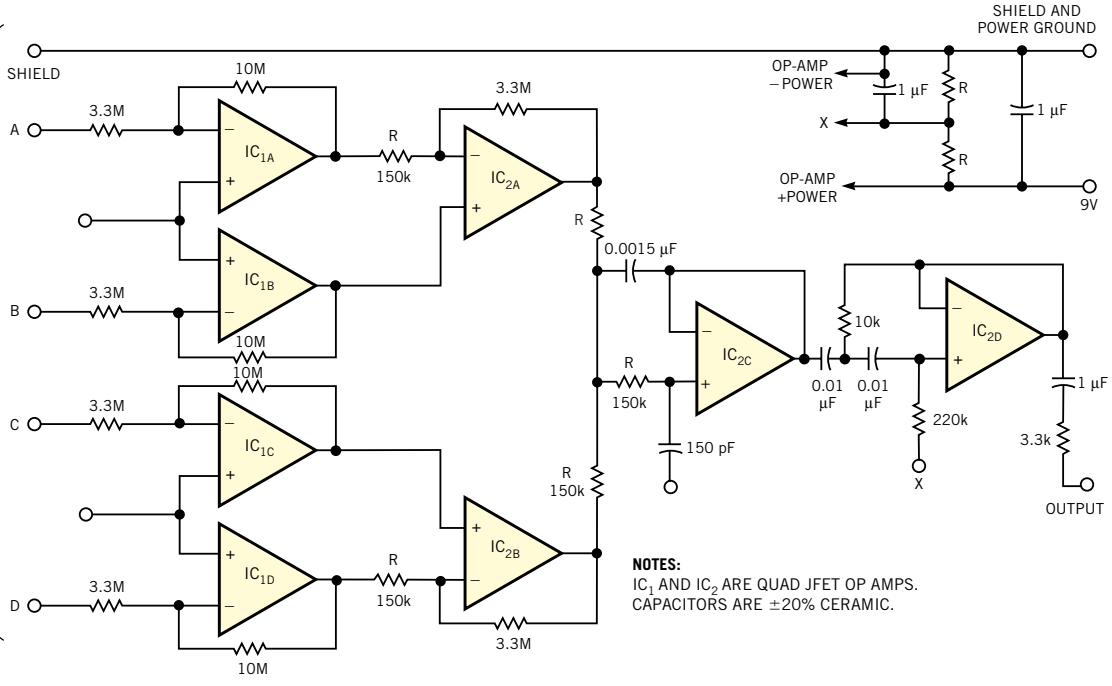


Figure 3

This amplifier, using the multiple-pad approach effectively reduces power-line-related noise pickup.

tribute equally to the output. You can make a segmented pickup from pieces of two-sided pc board with the solid-copper side serving as a shield. You can solder the shield side of the pieces to a suitable alligator clip. Alternatively, for longer term use, you can simply tape them onto the cable. You can use any even number of pads. the more you use, the better, but eight on each side are sufficient.

The amplifier of **Figure 3** uses two quad J-FET or BiFET op amps. Thanks to stray capacitance on the input lines of the test model, a relatively low input resistance of 3.3 MΩ is sufficient. Input noise is mostly the Johnson noise of the 10-MΩ feedback resistors. Power-line noise pickup is usually the bigger problem. The output stages incorporate some highpass filtering to reject noise below 300 Hz. The output level depends on many factors but is approximately 50 mV. A postamplifier (not shown) can provide more equalization, filtering, and gain if necessary, as well as manual or automatic level control. Tests of models of both design approaches use readily available components and show perfectly clear telephone speech through a small speaker in the postamplifier box. The multiple-pad pickup system produces noticeably lower noise, and clip orientation is less critical.□

Circuit produces variable frequency, duty cycle

Mark Reed, Texas Instruments, Dallas, TX

This Design Idea shows a simple, low-cost circuit that produces a highly accurate variable-frequency and variable-duty-cycle output (**Figure 1**). Further, the duty cycle and frequency are independent of each other (excluding 0 and 100% duty cycle). The method derives its accuracy and stability from the fact that the output is based on a crystal oscillator and divisions of the oscillator's frequency. The design uses only six devices. IC_1, a 74HC393 binary ripple counter, has as its input is the oscillator's output frequency. The outputs are the oscillator frequency divided by two, four, eight, 16, 32, 64, 128, and 256. IC_{5B} is cascaded with IC_1 to divide the oscillator frequency further by 512, 1024, 2048, and 4096. In this circuit, the divide-by-128 is the largest division it uses. You could, with a simple wiring change, substitute an unused divider to obtain a different output-frequency range. The eight inputs of IC_2, a 74HC151 eight-line-to-one-line multiplexer, connect to the oscillator's frequency divided by one, two, four, eight, 16, 32, 64, and 128. Note that the oscillator's output connects directly to an input of IC_2. This connection allows selecting the oscillator's frequency divided by one. IC_2 connects one of the eight frequencies to the input of IC_3.

IC_3, a 74HC4017 decade counter, di-

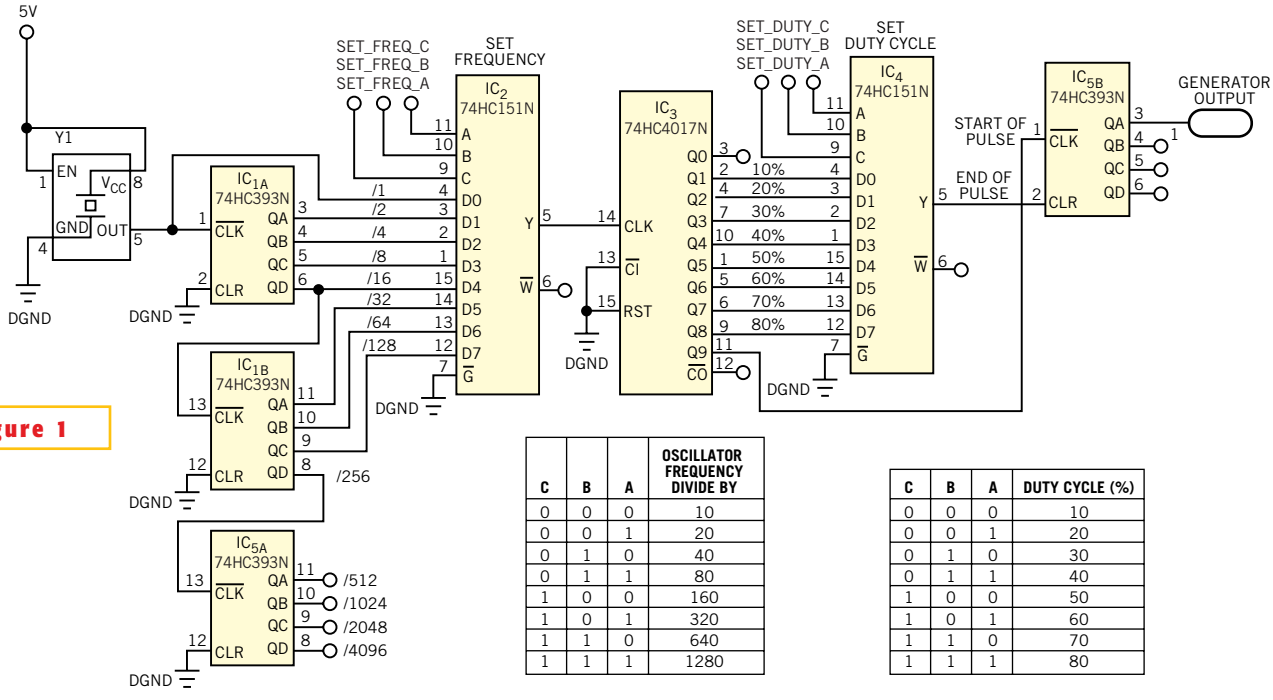


Figure 1

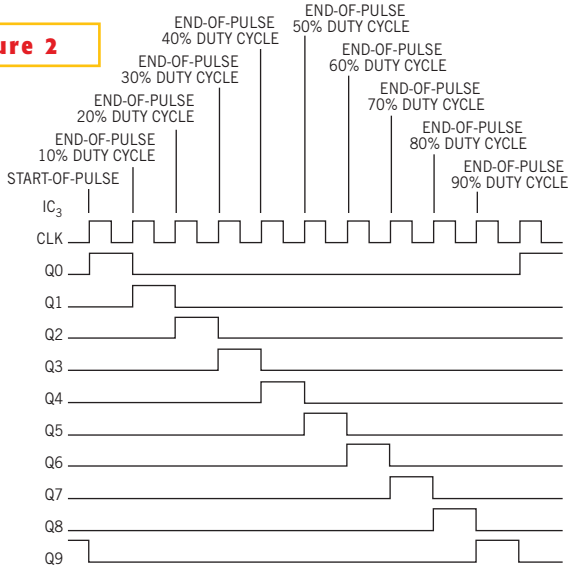
C	B	A	OSCILLATOR FREQUENCY DIVIDE BY
0	0	0	10
0	0	1	20
0	1	0	40
0	1	1	80
1	0	0	160
1	0	1	320
1	1	0	640
1	1	1	1280

C	B	A	DUTY CYCLE (%)
0	0	0	10
0	0	1	20
0	1	0	30
0	1	1	40
1	0	0	50
1	0	1	60
1	1	0	70
1	1	1	80

This circuit produces waveforms of variable frequency and duty cycle. Further, the frequency and duty cycle are independent of each other.

vides the frequency from IC_2's output by 10. Therefore, the maximum output frequency for this design is the oscillator frequency divided by 10. Each of the decoded decade counter's 10 outputs goes high for one clock cycle only (**Figure 2**). Using the 10 outputs, a frequency's period divides into 10 equal intervals. You can use these 10 equal intervals to generate duty cycles of 10, 20, 30, 40, 50, 60, 70, 80, and 90%. For this circuit, the outputs of IC_3, Q1 through Q8, yield the end-of-pulse signals for duty cycles of 10 through 80%, respectively. The start-of-pulse signal is Q9's negative edge, which occurs at the same time as Q0's positive edge. Therefore, you can use Q9 as start-of-pulse low true, and the end-of-pulse signals are high true. The eight inputs of IC_4, an eight-line-to-one-line multiplexer, connect to eight of the nine end-of-pulse outputs from IC_3. This circuit omits the 90% duty cycle. You can include the 90% duty cycle with a simple wiring change. If you want to select 0% duty cycle, connect an input to IC_4. If you select 0% duty cycle, the generator's output is low. IC_4 connects one of eight end-of-pulse signals to IC_5.

Figure 2



The end-of-pulse signals from IC_4 determine the duty cycle of the output waveform.

IC_{5A} is a binary ripple counter that serves as a set-reset latch. The start-of-pulse signal sets the latch. The end-of-pulse signal resets the latch. The output of IC_5 is the variable-frequency and variable-duty-cycle output of the signal generator. For example, if the oscillator's frequency is 4 MHz and IC_2's C B A inputs are 0 1 0, then the generator delivers 100 kHz. If IC_4's C B A inputs are 0 0 1, then the generator's output exhibits 20% duty cycle. If you need to select from more than eight frequencies, use a larger multiplexer than IC_2. Cascade more or different types of dividers to achieve your frequency needs. You can use a 74HC390 to obtain division by five, 10, 50, 100, and so on. If you need other duty cycles, cascade 74HC4017s to divide the period by the desired number of intervals. Finally, if you need to select from more than eight duty cycles, use a larger multiplexer than IC_4.□

Active-feedback IC serves as current-sensing instrumentation amplifier

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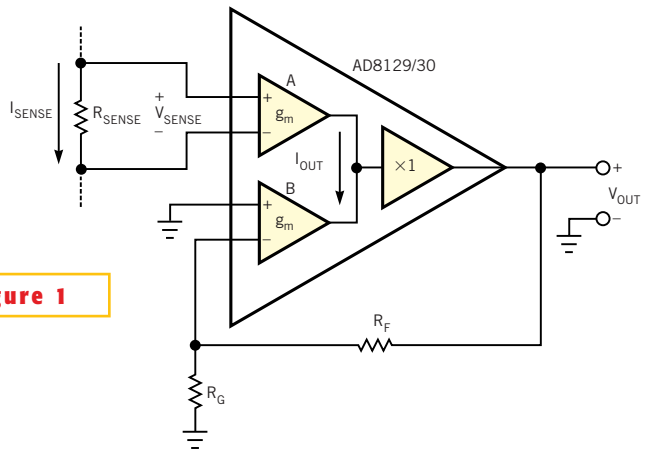
High-speed current sensing presents a designer with some significant challenges. Most techniques for sensing current involve measuring the differential voltage the current produces as it flows through a sense element, such as a resistor or a Hall-effect device. The differential voltage across the sense element is generally small and is often riding on a common-mode voltage that is considerably larger than the differential voltage itself. Accurate amplification of the differential voltage requires a differential amplifier with high input impedance, high CMR (common-mode rejection); wide input-common-mode voltage range; and high, well-defined gain. Traditional instrumentation amplifiers have these features and often serve for low-frequency current sensing, but they perform poorly at high speeds. High-speed current sensing requires the kind of performance that instrumentation amps provide, but their abilities must extend to high frequencies. **Figure 1** shows how high-speed active feedback amplifiers, such as the AD8129 and AD8130 differential receivers, are ideal for these high-speed instrumentation-amp applications. The AD8129 requires a minimum closed-loop voltage gain of 10 for stability, whereas the AD8130 is unity-gain-stable.

Figure 1

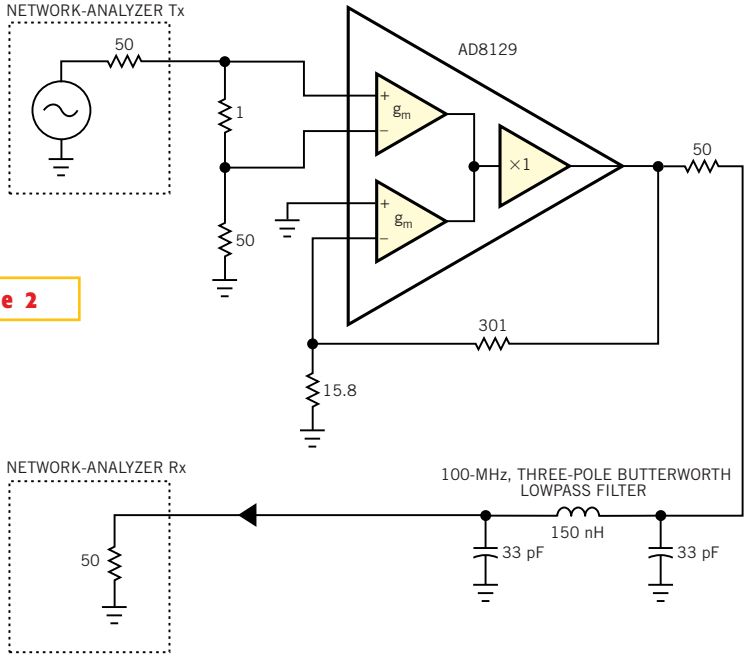


An active-feedback amplifier is ideal for current-sensing applications.

Active-feedback amplifier operation differs from that of traditional op amps; it provides a beneficial separation between the signal input and the feedback network. **Figure 1** shows a high-level block diagram of an active-feedback amplifier in a typical closed-loop configuration. High-speed current sensing uses a resistor as the sense element. The input stages are high-impedance, high-CMR, wideband, high-gain transconductance amplifiers with closely matched transconductance parameters. The output currents of the transconductance amplifiers undergo summing, and the voltage at the summing node is buffered to provide a low-impedance output. Applying negative feedback around amplifier B drives V_{OUT} to a level that forces the input voltage of amplifier B to equal the negative value of the input voltage at amplifier A, because the current from amplifier A equals the negative value of the current from amplifier B, and the gm values are closely matched. From the foregoing discussion, you can express the closed-loop voltage gain for the ideal case as: $V_{OUT}/V_{IN}=1+R_F/R_G\equiv A_V$.

Measurement sensitivity in volts per amp is expressed as: $V_{OUT}/I_{SENSE}=A_VR_{SENSE}$. Minimizing the values of R_F and R_G also minimizes resistor and output-voltage noise arising from input-referred current

Figure 2



This test circuit produces flat frequency response to 10 MHz.

noise. Because of the small sense resistance and high measurement frequencies, you must minimize parasitic effects in the input circuitry to avoid measurement errors. Parasitic trace inductance in series with the sense element is of particular concern, because it causes the impedance across the amplifier's input to increase with increasing frequency, producing a spurious increase in output voltage at high frequencies. **Figure 2** illustrates a test circuit with $R_{SENSE}=1\Omega$ and $A_V=20$, which equates to a measurement sensitivity of 20V/A. The three-pole lowpass filter produces a defined bandwidth and attenuates spurious responses at the amplifier's output arising from input signals at frequencies outside the desired measurement bandwidth. The test circuit's frequency response in **Figure 3** shows that the expected differential-to-single-ended gain of 20/101, or −14 dB, is flat to approximately 10 MHz and is down by 3 dB at 62 MHz. **Figure 3** demonstrates the effectiveness of the high CMR of active-feedback amplifiers. The common-mode signal at the amplifier's input is approximately 50 times greater than the differential signal across the sense resistor.□

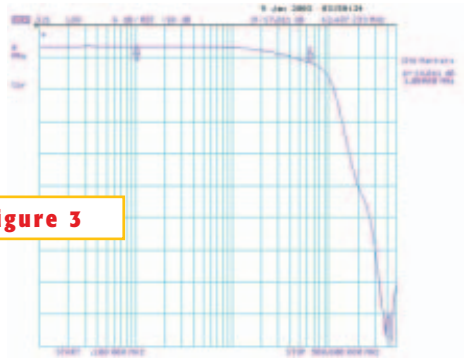


Figure 3

The test circuit in Figure 2 exhibits accurate differential gain in the presence of large common-mode signals.

Create secondary colors from multicolored LEDs

Claude Haridge, Stittsville, ON, Canada

It is well-known that simultaneously mixing two primary-color light sources, such as red and green, creates a secondary color, such as yellow. This mixing process commonly occurs in tricolor LEDs. One disadvantage of this method of generating a yellow color is that the LED must use twice the current because both the red and the green LEDs must be on. In battery-powered circuits, the LED indicator's operating current may be a significant fraction of the supply current, so using the same current to generate both primary and secondary colors is advantageous. The operating-current savings may be significant in telecom-line-card applications involving thousands of line cards or large-panel RGB LED displays. This Design Idea proposes a sequencing method to generate balanced secondary colors from bicolor, tricolor, and RGB LEDs, using only one LED's operating current. Advantages include lower power dissipation and more uniform intensities between primary and secondary colors. Using the sequencing method also allows a bicolor LED to now produce three colors and keep a simpler pc-board layout using two rather than three pins. In addition, you can also produce white light with RGB LEDs using the sequencing method.

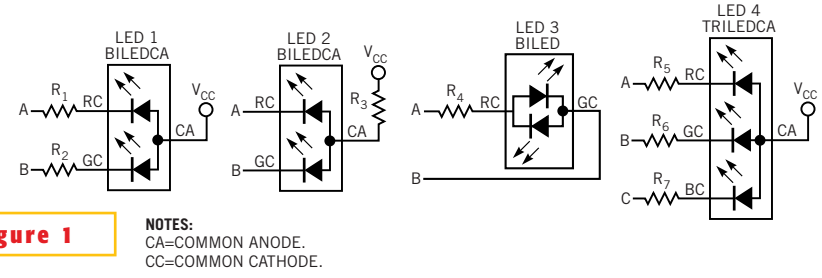


Figure 1

NOTES:
CA=COMMON ANODE.
CC=COMMON CATHODE.

All these LED configurations can produce secondary colors, either by current control or duty-cycle control.

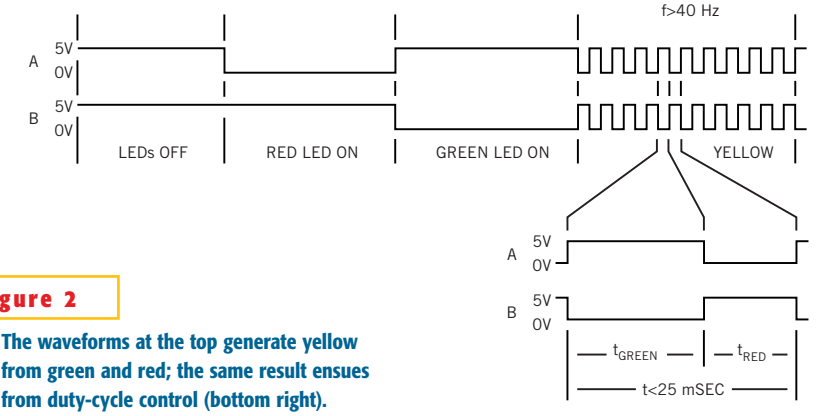


Figure 2

The waveforms at the top generate yellow from green and red; the same result ensues from duty-cycle control (bottom right).

The method uses the property of images to persist in the human eye for several tens of milliseconds. If different primary colors flash sequentially and quickly enough from one point, humans see them as overlapping in time, and the brain interprets them to appear as secondary colors or even white, depending on the color components. Experimentation with two or three primary-color LEDs shows that the flash sequence must complete within approximately 25 msec or less to produce a solid secondary color or white light. In testing for an upper limit, you can use flash rates to 1 MHz to produce this effect without degrading secondary colors. Thus, you can use any convenient clock source higher than 40 Hz to create secondary colors. Note that

the primary-color LEDs must be physically close together, such as on a semiconductor chip, for the eye to properly mix the light. Diffused lenses also allow a wider viewing angle. These combinations are commercially available as bicolor, tricolor, and RGB LEDs.

Figure 1 shows the various LED-circuit configurations, and **Figure 2** shows the timing to generate all three colors from bicolor and tricolor LEDs, although using only one LED's operating current. Note that the driver for the bicolor LED must be able to sink and source current. You may have to provide color balance between the primary-color LEDs to ensure that the secondary colors appear properly. The LEDs have different efficiencies and intensities as the human eye sees them, and these parameters need correcting. For tricolor LEDs in a common-anode or -cathode configuration and 50% duty cycle, the correction is easy to effect by adjusting the current-limiting resistors. Alternatively, you can use one current-limiting resistor and then vary the duty cycle to provide the necessary color balance. For two-leaded, bicolor LEDs, it is easier to adjust the duty cycle to produce the correct secondary color than to use additional circuitry. The waveforms at the bottom of **Figure 2** illustrate duty-cycle control to achieve secondary-color balance for both bicolor and tricolor LEDs.

TABLE 1–SECONDARY COLORS FROM RGB LEDs

Red	Green	Blue	Emitted color	Notes
0	0	0	None	
1	0	0	Red	
0	1	0	Green	
0	0	1	Blue	
1	1	0	Yellow	Red/green sequenced
0	1	1	Cyan	Green/blue sequenced
1	0	1	Magenta	Blue/red sequenced
1	1	1	White	Red/green/blue sequenced

Using a sequenced bicolor LED to generate three colors has packaging advantages, particularly when you vertically stack several LEDs. Previously, stacked, tricolor LEDs needed to use a through-hole assembly, because the middle lead would be inaccessible if the devices were surface-mounted. Because the bicolor LED has only two pins, you can vertically stack several of them and bend out the leads for surface mounting. The generation of secondary colors can also extend to RGB LEDs (**Table 1**). You can achieve color balancing by adjusting the current-limiting resistors or the duty cycle. You can program three pins from a microcontroller's port to sequence through the various primary-color combinations.□

Edited by Bill Travis

Make noise with a PIC

Peter Guettler, APS Software Engineering GmbH, Cologne, Germany

Building a stable noise generator for audio-frequency purposes requires only a few components. The circuit in **Figure 1** relies on linear-feedback shift registers and some simple software. An eight-pin Microchip (www.microchip.com) PIC12C508 controller (IC_2) with a short program generates pseudorandom noise at its output pin, GP0. A single controller is sufficient for simple applications. To obtain Gaussian-distributed noise, you can use a number of identical PIC controllers in parallel in a true realization of the central-limit theorem. (The central-limit theorem states that the sum of an infinite number of noise sources has Gaussian distribution, regardless of the individual noise distribution of each generator.) Using an infinite number of noise generators is impractical, but 10 to 16 are sufficient in most cases. And, because the smallest member of the PIC family is an inexpensive chip with low current consumption, the circuit is easy to realize.

All noise generators run the same program (**Listing 1** on the Web version of this Design Idea at www.edn.com). Perfectionists might program each PIC with an individual initial value for the shift register, but, because all controllers run uncorrelated with their own internal oscillators and start out of reset at different times, this measure is unnecessary. Op amp IC_{1A} sums and level-shifts the noise signals. Summing resistors R_1 and R_2 must have a value of 10 kΩ times the number of noise generators you use. The output signal of IC_{1A} feeds a −3-dB/octave filter to obtain pink noise. Buffer IC_{1B} decouples the filter and provides low output impedance. The signal amplitude is approximately 400 mV p-p with a flat spectral distribution of 20 Hz to 20 kHz. Closing S_1 or applying a low level at pin GP4 immediately stops all noise generators and freezes the prevailing signal amplitude. You can download the PIC software from the Web version of this Design Idea at www.edn.com.□

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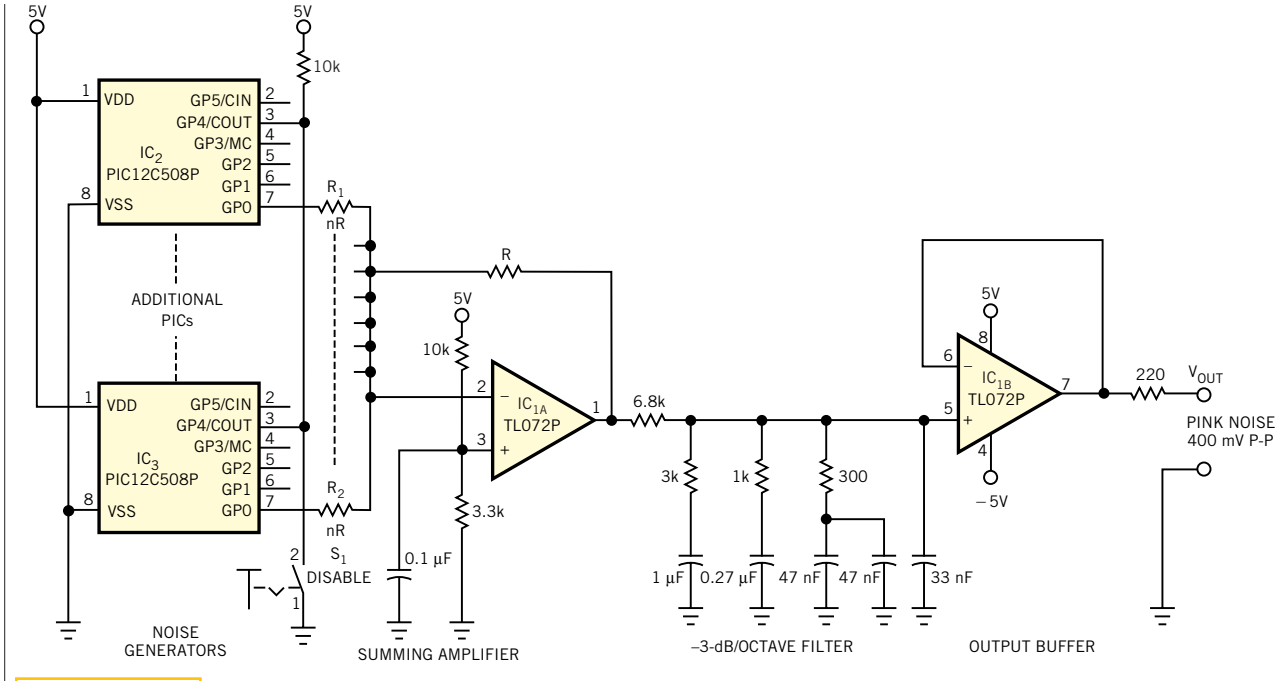


Figure 1 This simple circuit generates Gaussian-distributed noise for audio applications.

Circuit provides linear resistance-to-time conversion

S Kaliyugavaradan and D Arul Raj, Anna University, Chennai, India

RESISTANCE-BASED transducers, such as strain gauges and piezoresistive devices, find common use in the measurement of several physical parameters. For applications in which digital processors or microcontrollers serve for data acquisition and signal processing, the transducer's response must assume a form suitable for conversion to digital format. It is desirable to convert the resistance change of such sensors into a proportional frequency or a time interval so that you can easily obtain an output in digital form, using a counter/timer. The circuit of **Figure1** linearly converts the sensor resistance, R_S, into a proportional time period. The circuit is essentially a relaxation oscillator, comprising a current source, a bridge amplifier, a comparator, and a flip-flop. The current, I_S, divides in the paths of R_1 and R_2 as if the two resistors were connected in parallel. Assuming ideal op amps, the circuit functions as an oscillator when R_X (R_4+R_S) is greater than R_1R_3/R_2.

The circuit produces waveforms at the input and output of the comparator, IC_2 (**Figure 2**). T_1 and T_2 are the time intervals for which the comparator's output assumes levels V_{S1} and $-V_{S2}$, respectively. The output voltage from IC_2, with its levels changed via a zener-diode circuit, serves as clock input to a D flip-flop. From the 7474 flip-flop, you obtain a square-wave output that is high and low alternately for a time period $T=4C(R_2R_X-R_1R_3)/R_1$. This equation indicates that the circuit converts a change in sensor resistance into a proportional time period ΔT with sensitivity $\Delta T/\Delta R_S=4C(R_2/R_1)$. The following salient features of **Figure 1** merit mention:

- The sensor is grounded; you can easily vary the conversion sensitivity by varying either R_1 or R_2.
- You can adjust the offset value, T_0 (about which changes in T occur because of a change in the sensor's resistance), by changing either R_3 or R_4 without affecting the conversion sensitivity.
- The offset voltages of the op amps alter T_1 and T_2 in opposite ways, such that their overall effect on $T(T_1+T_2)$ is not appreciable.
- Thanks to the current source, the output is largely insensitive to noise voltages in the line of the current source and to changes that occur in V_{S1} and V_{S2}.

Consider the example of converting a

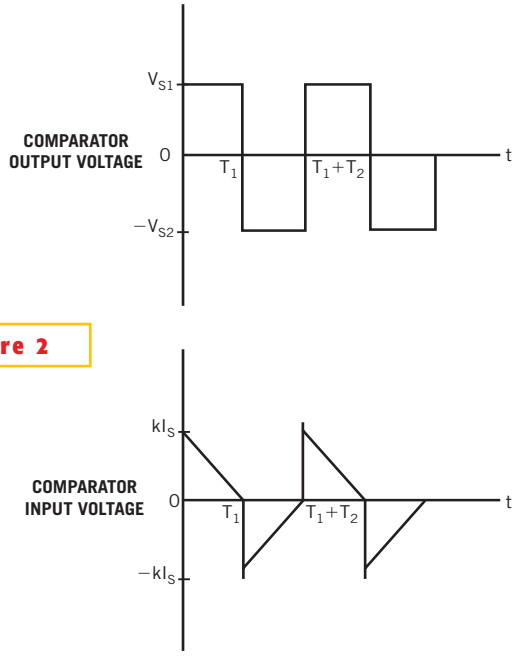


Figure 2 These waveforms represent the input and output of comparator IC_2.

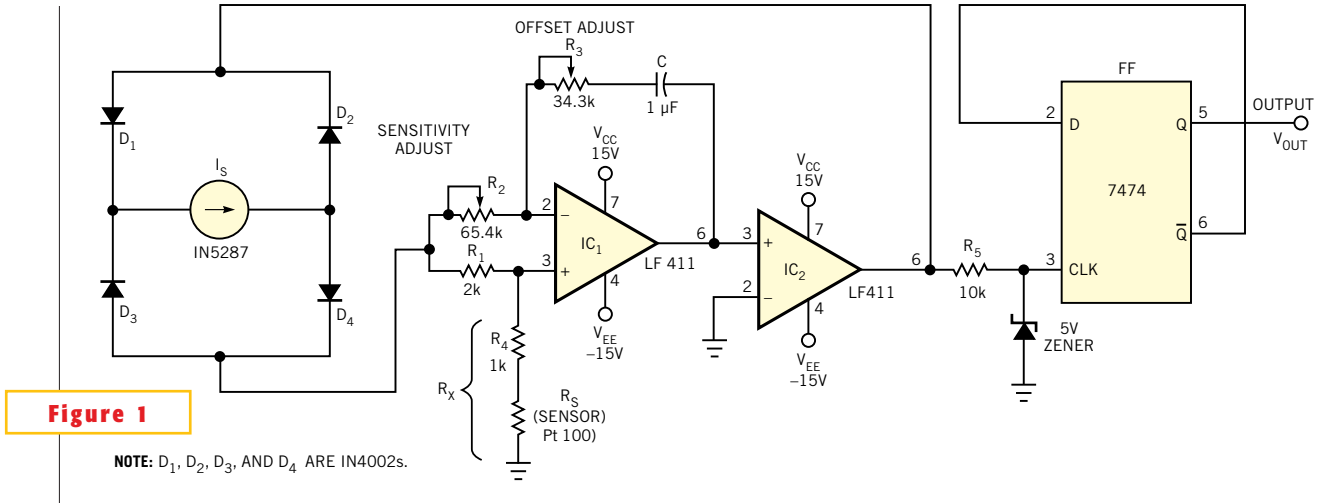


Figure 1 NOTE: D_1, D_2, D_3, AND D_4 ARE IN4002s.

This simple circuit converts a resistance reading to a time period.

Pt-100 (platinum RTD) sensor in the range of 119.4 to 138.51Ω, which corresponds to a temperature range of 50 to 100°C, into time periods of 10 to 12.5 msec. The design is simple. Because the current through the sensor is a fraction of I_S, I_S should be low enough to keep the self-heating error to an acceptably low level. This design uses an IN5287 current regulator; it provides an I_S of approximately 0.33 mA and has a dynamic impedance better than 1.35 MΩ. For a better current source, you could use a circuit based on a voltage-regulator IC. In the next step, with suitable and practical fixed values for R_1 and C, you adjust R_2 until you obtain the needed sensitivity: 130.82 μsec/Ω. Following this step, with a fixed R_4, you adjust R_3 to obtain the offset required in the output (T). **Figure 1** shows the values of components for this example. The resistors all have 1% tolerance and 0.25W rating, and C is a polycarbonate capacitor.□

PC-configurable RLC resonator yields single-output filter

Saurav Gupta, New Delhi, India

This Design Idea presents a versatile filter circuit for low-power-consumption instrumentation that you can program from your PC using the parallel port. The circuit uses analog switches and latches instead of digital potentiometers for the digital control (**figures 1** and **2**). By running simple software code on the PC, you can configure a single robust design to work as a lowpass, highpass, or bandpass filter, and you can also select the desired center frequency, ω_0 (**Listing 1**). Unlike a similarly controllable design (**Reference 1**), this design is a single-output-at-a-time filter. Many power-sensitive systems do not require simultaneous-filter functions.

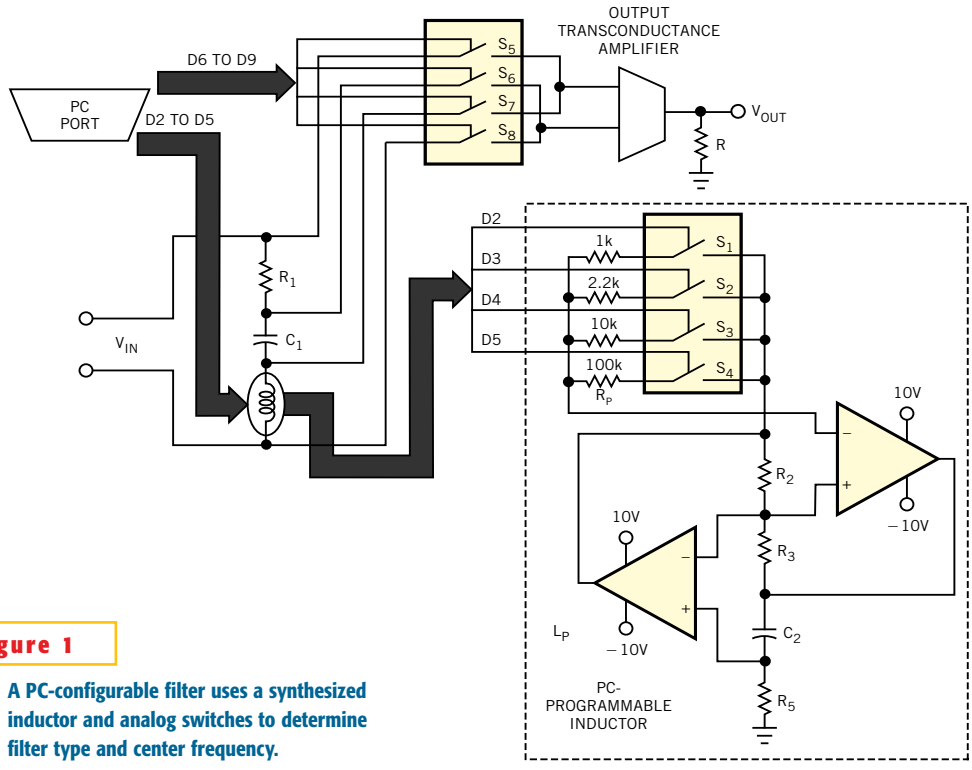


Figure 1

A PC-configurable filter uses a synthesized inductor and analog switches to determine filter type and center frequency.

The design exploits the fact that a series RLC resonator can provide various filter functions with its elements. Because the design is based on an RLC section, it is trivial to convert the design into a PC-controlled resonator. In **Figure 1**, the inductor, L_P, is implemented as a PC-controlled synthesized inductor. The value of the inductor is $L_P = C_2R_PR_3R_5/R_2$. Here, R_P can assume any of 15 possible values, depending upon the state of switches S_1 through S_4 (determined by PC-port data bits D2 through D5). The expression for the frequency is $\omega_0 = (R_2/C_1R_PR_3R_5)^{1/2}$. You can thus effectively select 15 frequency values. (This design uses 12 values of practical interest.) Data bits D6 through D9 from the PC's parallel port set the state of analog switches S_5 through S_8. The state of the switches determines the type of filter.

Figure 3 shows the software-generated display for the circuit. This design uses a

TABLE 1–REPRESENTATIVE PORT SETTINGS AND FILTER PARAMETERS

Filter type/center frequency	Port setting								Hex output from PC
	D9	D8	D7	D6	D5	D4	D3	D2	
Lowpass/9.93 kHz	0	0	1	1	0	1	0	0	X34
Highpass/22.9 kHz	1	0	1	0	0	1	1	0	XA6
Bandpass/3.16 kHz	0	1	0	1	1	0	0	0	X58
Bandpass/37.3 kHz	0	1	0	1	0	1	1	1	X57

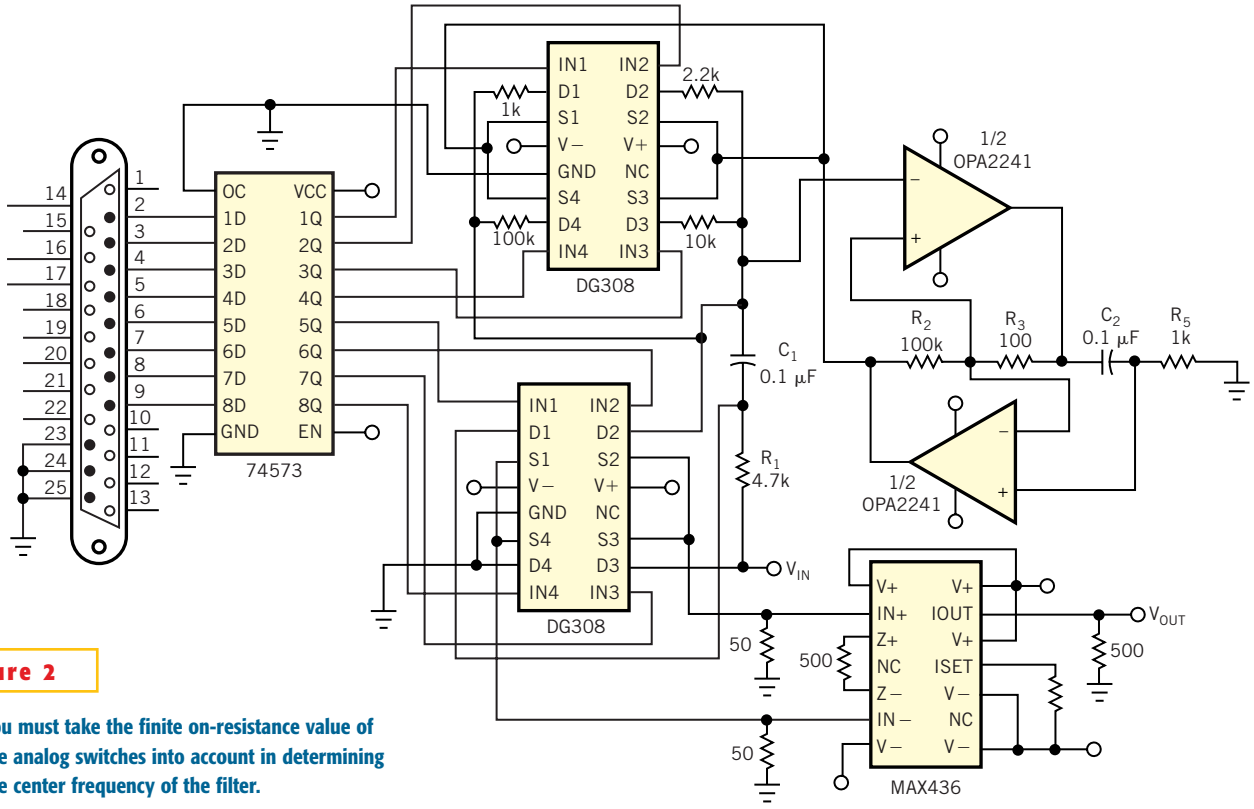


Figure 2

You must take the finite on-resistance value of the analog switches into account in determining the center frequency of the filter.

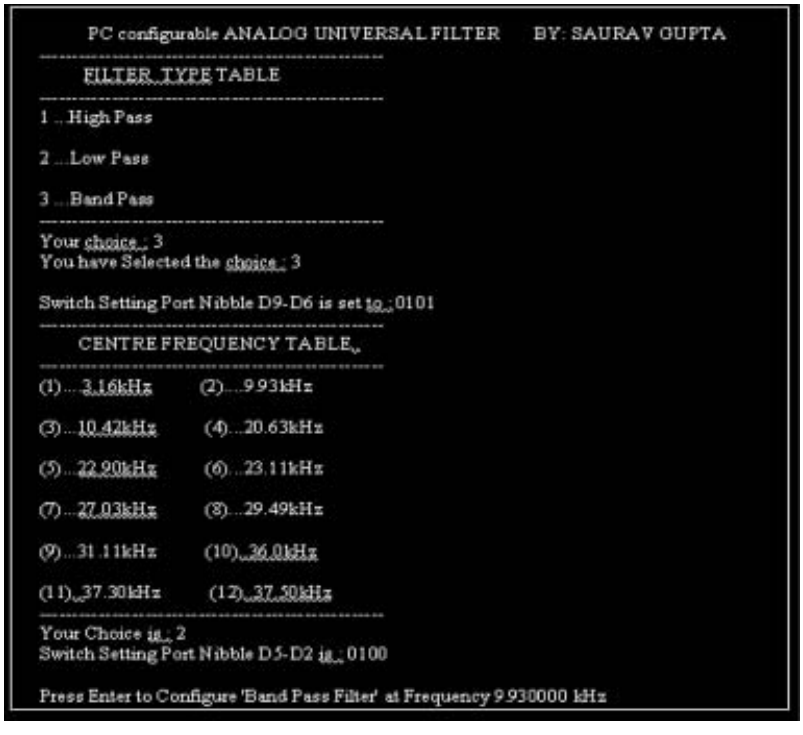


Figure 3

This user-friendly configuration screen allows you to determine filter type and frequency.

9.93-kHz bandpass filter for demonstration and testing. Increasing the number of analog switches can provide a wider range. Moreover, you could use additional switches for gain programmability. The 74573 latch provides the interface to the PC. **Table 1** shows the port/switch settings for a few frequency and filter-type selections. Note that the analog switches (DG308) have a finite operating on-resistance of approximately about 110Ω; you must take this resistance into account when you calculate the center frequency. For precision instrumentation, other switches are available with operating on-resistances as low as 30 to 50Ω. You can download **Listing 1** from the Web version of this Design Idea at www.edn.com.□

Reference

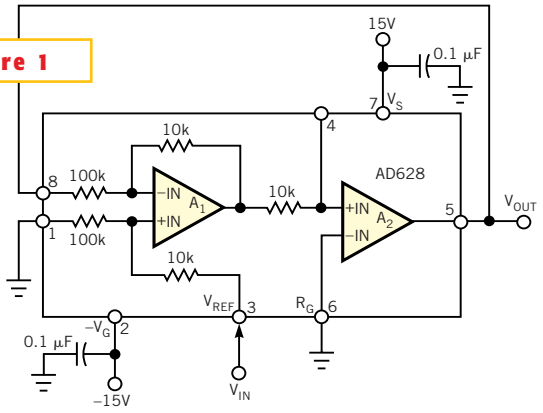
1. Gupta, Saurav, and Tejinder Singh, "PC-based configurable filter uses no digital potentiometers," *EDN*, Jan 23, 2003, pg 76.

Single IC provides gains of 10 and −10

Moshe Gerstenhaber and Charles Kitchin, Analog Devices, Wilmington, MA

Real-world data-acquisition systems require amplifying weak signals to match the full-scale input range of an A/D converter. Unfortunately, when you configure them as gain blocks, most common amplifiers have both gain errors and offset drift. The typical two-resistor gain-setting arrangement found in many op-amp circuits has serious accuracy and drift limitations. With standard 1% resistors, the circuit gain can be off by as much as 2%. Also, the gain can vary with temperature, because each resistor drifts differently. You can use monolithic resistor networks for precise gain setting, but these components are expensive and consume valuable pc-board space. The circuits of **figures 1** and **2** offer improved performance and lower cost; they are also smaller. The single-µSOIC approach is the smallest available for this function, and the circuits require no external components. **Figure 1** shows an AD628 precision gain block connected to provide a voltage gain of 10. The gain block itself comprises two internal amplifiers: a gain-of-0.1 difference amplifier, A_1, followed by an uncommitted buffer amplifier, A_2. You can configure it to provide different gains by strapping or grounding the appropriate pins.

Figure 1



This circuit has a precise gain of 10 and uses no external components.

For a gain of 10, the input signal connects between the V_{REF} pin (Pin 3) and ground, instead of to the op amp's inputs. With the input tied to the V_{REF} pin, the

voltage at the noninverting input of A_1 equals V_{IN}(100 kΩ/110 kΩ), or V_{IN}(10/11). The inverting input of A_2 (Pin 6) is grounded; therefore, feedback from the output of A_2 forces the noninverting input of A_2 to be 0V. The output of A_1 must then also be at 0V. The voltage on the inverting input of A_1 must be equal to the voltage on the noninverting input of A_1, so both equal V_{IN}(10/11). Thus, the output voltage of A_2, V_{OUT}, equals

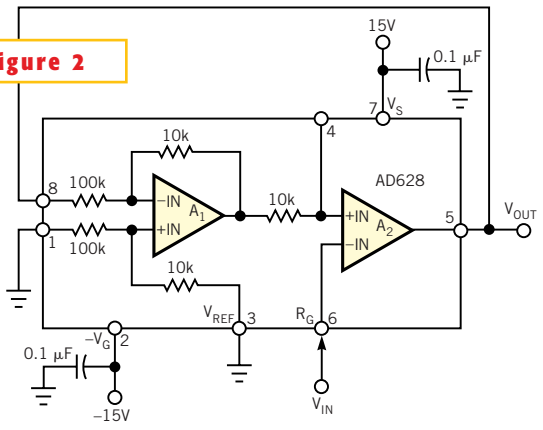
$$V_{OUT} = V_{IN} \times \frac{10}{11} \times \left(1 + \frac{100k}{10k}\right)$$

$$= V_{IN} \times \frac{10}{11} \times 11 = 10V_{IN},$$

providing a precise gain of 10 with no external components.

The companion circuit of **Figure 2** provides a gain of −10. This time, the input connects between the inverting input of A_2 (Pin 6) and ground. Operation is similar to that of **Figure 1**, but A_2 now inverts the input signal by 180°. With the V_{REF} pin grounded, the noninverting input of A_1 is at 0V, so feedback forces the inverting input of A_1 to 0V as well. Because A_1 operates at a gain of 0.1, the output of A_2 necessary to force the inverting input of A1 to 0V is $-10V_{IN}$. The two connections exhibit different input impedances. When you drive the V_{REF} input (Pin 3) for a gain of 10, the input impedance to ground is 110 kΩ; it is approximately 50 GΩ when you drive the noninverting input of A_2 (Pin 6) for a gain of −10. All resistors are internal to the gain block, so both accuracy and drift are excellent. These circuits have gain accuracy better than 0.1%, with a gain temperature coefficient lower than 5 ppm/°C. The −3-dB bandwidth is approximately 110 kHz with a 10-mV input and 95 kHz with a 100-mV input. Although ±15V supplies are appropriate, you may operate these circuits with dual supplies from ±2.25V to ±18V.□

Figure 2



This companion circuit to the one in Figure 1 delivers an accurate gain of −10.

Edited by Bill Travis

Video multiplexer uses high-speed op amps

Bruce Carter, Texas Instruments, Dallas, TX

Video multiplexers route video from several sources to a single channel. Low-end consumer products use CMOS analog switches and multiplexers, such as the 4066 and 4051. Unfortunately, these devices have a series on-resistance that ranges from approximately 100Ω to 1 kΩ, a resistance that is not constant with video level and that appears in series with the signal. The traditional way of solving this problem is by buffering the analog-switch outputs with transistor stages. With this approach, the characteristics of the CMOS switch and the buffer stage degrade video performance. However, if you forget the multiplexing action for a moment and consider just the buffer-amplifier function, you will see that a better approach exists. It must present high enough input impedance to the switch that a 1-kΩ switch resistance is inconsequential and that variation in resistance of the switch with IRE (Institute of Radio Engineers) level produces no luminance shifts. **Figure 1** shows a configuration using high-speed op amps in a video-multiplexing application.

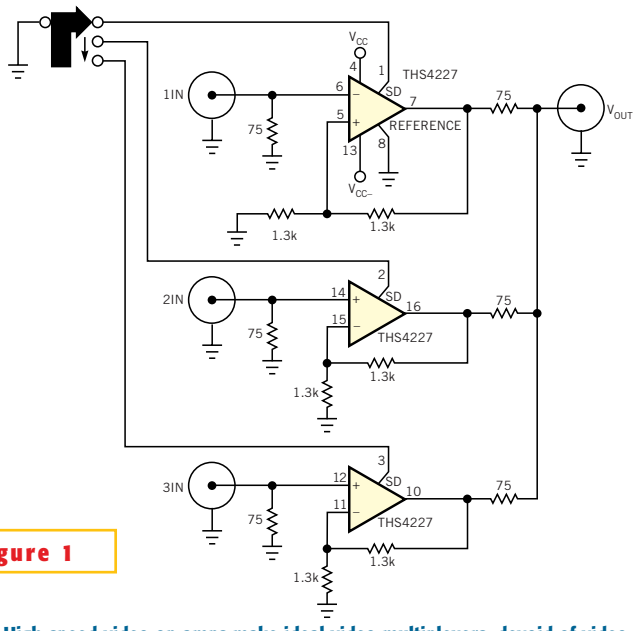


Figure 1

High-speed video op amps make ideal video multiplexers, devoid of video distortion or other artifacts.

High-speed op amps have plenty of bandwidth for video applications. By using an op amp that has 20 or more times the video bandwidth, roll-off and phase shift at 6 MHz are negligible. An op amp has high input impedance in the noninverting mode. You can terminate it for 75Ω input impedance by connecting a simple resistor. Two equal resistors create a gain of two in the noninverting configuration. The gain compensates for a 75Ω back-termination resistor on the op amp's output. The overall stage gain is therefore one. Now, consider the multiplexing function. Some video op amps have a "power-down" feature. This feature allows disabling the output of the op amp, producing a 0V (0 IRE) black level on its output. Its output can therefore connect in parallel with the outputs of other op amps, because it contributes no luminance or sync pulses. This feature enables the op amp to operate as a video multiplexer. The multiplexer in **Figure 1** shows a three-position, single-pole rotary switch. This switch could be a "break-before-make" or an electronic switching system, perhaps with an intelligent infrared interface.

To test the quality of signals passed through the video multiplexer, this design uses the Lucasfilm THX (www.thx.com) test patterns on one video input and a high-quality NTSC program source on another input. When the contrast/picture test goes through the video multiplexer as the active source, the presence of the op amp as a buffer has no effect on black and white levels. No bleeding or blooming occurs. Any crosstalk results in a visible brightening of the center of the picture in the video-program source, but none occurs. You set the brightness level with the video multiplexer, not in the circuit. Then, you insert the video buffer into the signal path. You'll find that brightness level does not change. The brightness setup test is also an ideal way to test for crosstalk between two video channels. Crosstalk would show up on the black background as a "ghost" image of the program material on the inactive channel; however, none occurs. No color shifts appear in the SMPTE (Society of Motion Picture and Television Engineers) bars with or without the video multiplexer in the signal chain. The color-bar patterns would also produce color shifts in the other channel if crosstalk were a factor. Human skin is the toughest color to get "right," and any change in skin tone arising from color crosstalk is apparent. No flesh-tone color shifts occur in the test.□

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Single resistor tunes lowpass filter

Vladimir Tepin, State Radioengineering University, Taganrog, Russia

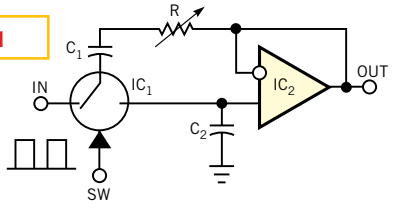
Any tunable, second-order, active RC-filter section requires at least two thoroughly matched variable resistors. But the lowpass implementation in **Figure 1** provides for wide-range cutoff-frequency control using only a single variable resistor, R. In addition to the resistor, this filter comprises an operational amplifier, IC_2, which serves as a unity-gain buffer; two capacitors, C_1 and C_2; and a single-pole, double-throw analog switch, IC_1, driven by a periodic sequence of square-wave switching pulses applied to the SW input. Thanks to the high-frequency periodic switching, you can simultaneously control the time constants of both C_1 and C_2 in their recharging processes using only R. The approximate voltage-transfer function of the filter, assuming that the switching frequency is much higher than the filter's cutoff frequency, is:

$$H(s)=\frac{1}{\left(\frac{s}{\omega_P}\right)^2+\left(\frac{s}{\omega_P Q}\right)+1},$$

where $\omega_P=1/(R\sqrt{C_1C_2\Theta(1-\Theta)}$ is the pole frequency; $Q=\sqrt{\Theta(1-\Theta)C_1/C_2}$ is the quality factor; $\Theta=\tau/T$ is the online time ratio (duty cycle); τ is the pulse width; and T is the switching period.

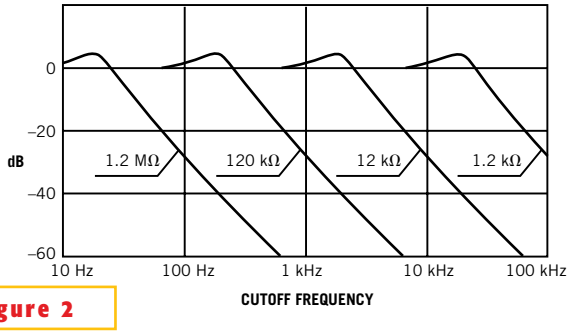
Obviously, controlling R results only in variations of pole frequency and does not affect the quality factor. So, you can tune this filter over a wide frequency range, preserving its passband gain and ripple. You can achieve a stable value of Θ by using a binary counter. A high-resolution, digitally programmable potentiometer is probably the most appropriate choice for R in this filter. **Figure 2** shows the filter's frequency response, simulated in PSpice. This design tunes the cutoff frequency over 20 Hz to 20 kHz by varying the resistor value from 1.2 MΩ to 1.2 kΩ, with C_1=10 nF, C_2=1 nF, Θ=0.5, and a switching frequency of 500 kHz. Using this method, you can also implement a high-order lowpass filter by cascading second-order sections or by joining them to multiple-feedback structures.□

Figure 1



This second-order lowpass filter uses a single resistor to control cutoff frequency.

Figure 2



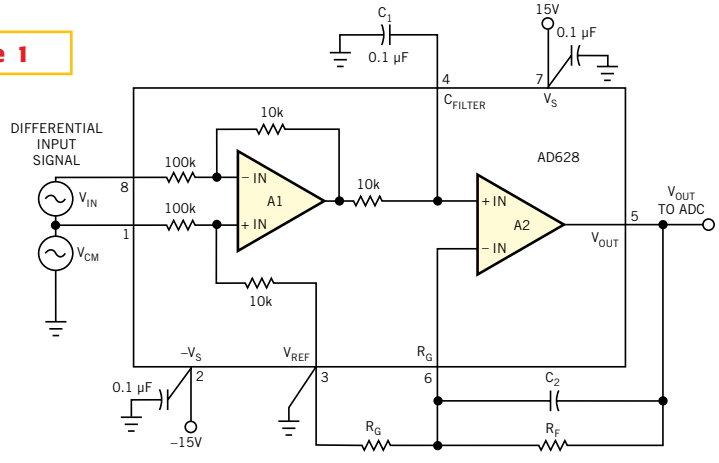
By varying one resistor, you can adjust the cutoff frequency over 20 Hz to 20 kHz.

Simple circuit provides precision ADC interface

Moshe Gerstenhaber and Charles Kitchin, Analog Devices, Wilmington, MA

Real-world measurement requires the extraction of weak signals from noisy sources. High common-mode voltages are often present even in differential measurements. The usual approach to this problem is to use an op amp or an instrumentation amplifier and then perform some type of lowpass-filtering to reduce the background noise level. The problems with this traditional approach are that a discrete op-amp circuit has poor common-mode rejection, and its input voltage range is always lower than the power-supply voltage. When you use a differential signal source with an instrumentation-amplifier circuit, using a monolithic IC can

Figure 1



An instrumentation-amplifier IC provides precision drive and lowpass filtering for an ADC input.

greatly improve common-mode rejection. However, a standard instrumentation amplifier cannot handle sources greater than the power-supply voltage or signals riding on high common-mode voltages. Instrumentation amplifiers using a single external gain resistor also suffer from gain drift. In addition, lowpass filtering requires the use of a separate op amp along with several external components. This approach uses up valuable board space. The circuit of **Figure 1** overcomes all of these performance limitations on one μSOIC.

TABLE 1—COMPONENT VALUES FOR 10V P-P FULL-SCALE INPUT FOR A TWO-POLE LOWPASS FILTER

	−3-dB corner frequency			
	200 Hz	1 kHz	5 kHz	10 kHz
Capacitor C_2	0.01 μF	0.002 μF	390 pF	220 pF
Capacitor C_1	0.047 μF	0.01 μF	0.002 μF	0.001 μF

Note: Output is 5V p-p; R_F=49.9 kΩ, and R_G=12.4 kΩ.

TABLE 2—COMPONENT VALUES FOR 20V P-P FULL-SCALE INPUT FOR A TWO-POLE LOWPASS FILTER

	−3-dB corner frequency			
	200 Hz	1 kHz	5 kHz	10 kHz
Capacitor C_2	0.02 μF	0.0039 μF	820 pF	390 pF
Capacitor C_1	0.047 μF	0.01 μF	0.002 μF	0.001 μF

Note: Output is 5V p-p, R_F=24.3 kΩ, and R_G=16.2 kΩ.

An AD628 precision-gain-block IC is configured as a differential-input amplifier and a two-pole lowpass filter. This circuit can extract weak signals riding on common-mode voltages as high as ±120V. The precision-gain block directly drives an ADC. A separate V_{REF} pin is available for offsetting the AD628 output signal so that it is centered in the middle of the ADC's input range. Although **Figure 1** indicates ±15V, the circuit can operate with ±2.25 to ±18V dual supplies. The V_{REF} pin can also allow single-supply operation; for this purpose, you simply bias V_{REF} at V_S/2. The gain block has two internal amplifiers: A1 and A2. Pin 3 connects to ground, thus operating amplifier A1 at a gain of 0.1. The output of A1 directly drives the positive input of amplifier A2.

The first pole of the lowpass filter is a function of the internal 10-kΩ resistor at the output of A1, and an external capacitor, C_1. The gain of A2 is a function of external resistors R_F and R_G. An external RC time constant in the feedback of A2 creates the second pole. This time constant comprises capacitor C_2 across resistor R_F. Note that this second pole provides a more rapid roll-off of frequencies above its RC "corner" frequency (1/(2πRC)) than does a single-pole lowpass filter. However, as the input frequency increases, the gain of amplifier A2 eventually drops to unity and does not decrease. So, the ratio of R_F/R_G sets the voltage gain of amplifier A2 at frequencies below its −3-dB corner and unity gain at higher frequencies.

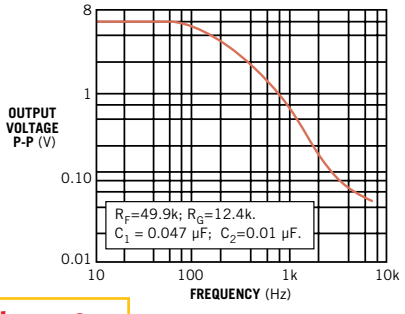


Figure 2

The frequency response of the two-pole filter in the circuit of Figure 1 shows a sharp roll-off between the corner frequency and approximately 10 times the corner frequency.

Figure 2 is a graph of the filter's output versus frequency using components to provide a 200-Hz, −3-dB corner frequency. Note the sharp roll-off between the corner frequency and approximately 10 times the corner frequency. Above this point, the second pole starts to become less effective, and the rate of attenuation is close to that of a single-pole response. **Tables 1** and **2** provide typical component values for various −3-dB corner frequencies and two full-scale input ranges. The values are rounded off to match standard resistor and capacitor values. Capacitors C_1 and C_2 must be high-Q, low-drift units; avoid low-grade disc ceramics. High-quality NP0 ceramic, Mylar, or polyester-film capacitors offer the best drift characteristics and settling time.□

Buck regulator operates without a dedicated clock

Robert Bell, National Semiconductor, Phoenix, AZ

Most switching regulators rely on a dedicated clock oscillator to determine the switching frequency of operation. A dedicated oscillator circuit within the power controller usually generates the clock signal. A class of hysteretic switching regulators can actually operate at a relatively fixed frequency without a clock, even with changing input-line and output-loading conditions. **Figure 1** shows a simplified buck regulator operating in continuous-conduction mode. (The inductor current always remains positive.) The output voltage, V_{OUT}, is equal to DV_{IN}, where D is the duty-cycle ratio of buck switch Q_1 and V_{IN} is the input voltage. The duty cycle, D, at fixed-frequency operation is T_{ON}/T_S, where T_{ON} is the on-time of Q_1 and T_S is the switching-frequency period, $1/F_S$. Some rearranging and substitution leads to the expression $D=V_{OUT}/V_{IN}=T_{ON}/(1/F_S)=T_{ON}F_S$.

Now, look at a regulator circuit, which, rather than using a fixed clock and a PWM, uses a circuit that turns on Q_1 for a time, T_{ON}, that's inversely proportional

to the input voltage, V_{IN}. **Figure 2** shows a regulator based on this principle. This regulator does not contain a clock oscillator, yet it remains at a fixed operating frequency even while the input voltage varies from 14 to 75V. The two main regulation blocks within this regulator are the on-timer and the regulation comparator. The comparator monitors the output voltage. If the output voltage is lower than the target value, the comparator enables the output switch, Q_1, for a period of time that the on-timer determines. The time period of the on-timer is $T_{ON}=KR_{ON}/V_{IN}$, where K is a constant (1.3×10^{-10}), R is a configuration resistor, and V_{IN} is the input voltage. If you now substitute T_{ON} in the previous buck-regulator equations, an interesting result occurs: $V_{OUT}/V_{IN}=F_SKR_{ON}/V_{IN}$. If you solve for F_S, you obtain $F_S=V_{OUT}/KR_{ON}$. Because V_{OUT} remains regulated and the K and R_{ON} terms are constants, the switching frequency also remains constant.

The constant-frequency relationship holds true provided that the inductor current remains continuous. At lighter loading, the current in the inductor becomes discontinuous. (The inductor current is zero for some portion of the switching cycle.) At the onset of discontinuous operation, the switching frequency begins to decrease. This reduction is a desirable feature to maintain high efficiency as the load decreases, because switching losses greatly decrease at lower switching frequencies. You derive the switching frequency in discontinuous mode as follows: The peak inductor current $I_P=V_{IN}T_{ON}/L=V_{IN}KR_{ON}/LV_{IN}=KR_{ON}/L$, where L is the output-inductor value. The output power is $P_{OUT}=V_{OUT}^2/R_{OUT}=LI_P^2F/2=FK^2R_{ON}^2/L$. Solving for F: $F=(V_{OUT}^2L)/(R_{OUT}K^2R_{ON}^2)$. As you can see, the switching frequency varies inversely with the output resistance, R_{OUT}.

Fixed-frequency operation without an oscillator offers a low-cost, easy-to-implement step-down regulator. You needn't worry about any loop-compensation or stability issues. The transient response is fast because the circuit has no bandwidth-limiting feedback components. Depending on the inductor value and loading, the operating frequency remains constant for most of the output-power range. A desirable reduction in operating frequency occurs at low loading levels.□

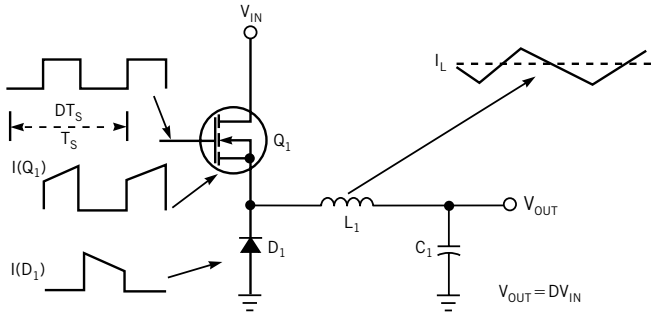


Figure 1 In a typical buck regulator, the output is the switching duty cycle times the input.

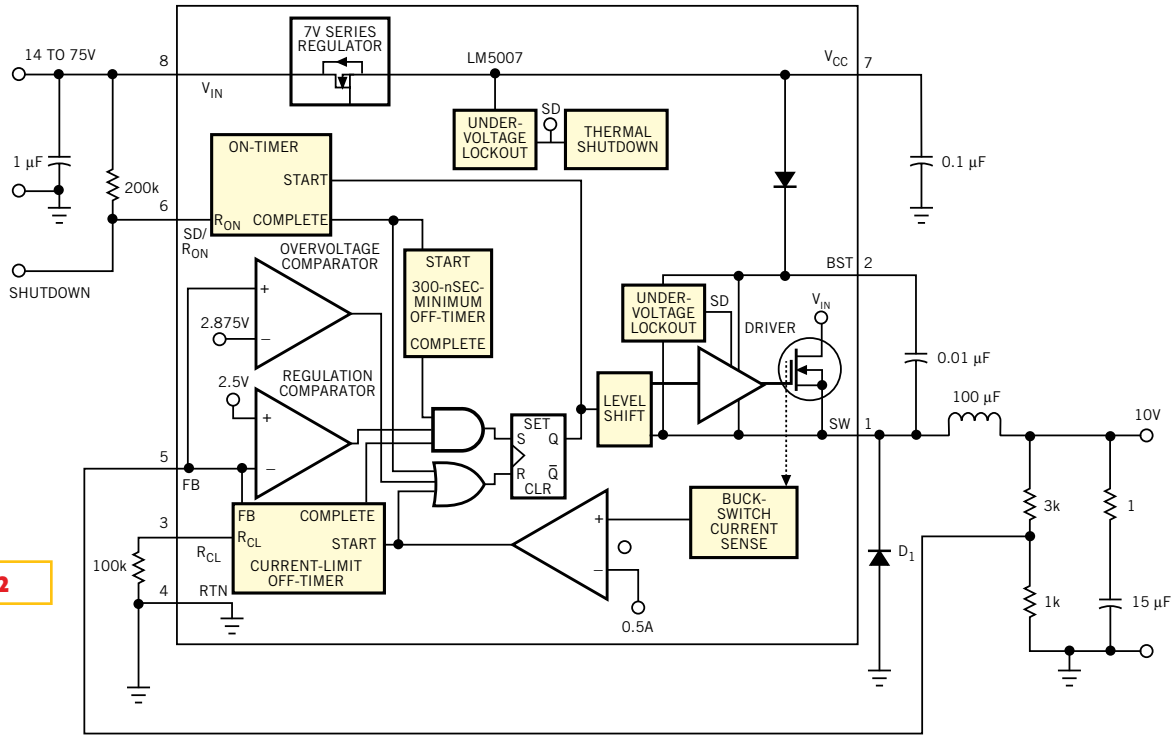


Figure 2 In this buck regulator, the switching frequency remains constant over a wide range of input voltages.

LED driver combines high speed, precision

Richard Cappels, Mesa, AZ

Applications such as turbidity measurement and densitometry require cleanly pulsed light sources with stable amplitudes. The LED driver in **Figure 1** illuminates retinal neurons in a biological experiment that has similar requirements. For a given LED at a given current, the intensity is stable, so switching a stable current is a simple and effective way to obtain the needed function. The circuit provides current pulses to the LED with rise and fall times lower than 500 nsec and overshoot lower than 7%. You can make the current computer-programmable by replacing the potentiometer with a DAC. The circuit comprises an adjustable, regulated current source (IC_1 and Q_2), an overdriven differential amplifier (Q_3 and Q_4) acting as a switch, and a level shifter (Q_1) to shift the TTL input signal to levels needed to drive the differential pair.

Voltage at the wiper of R_6 results in an equal voltage across R_9 because of feedback to the op amp. Because transistor Q_2 has a high alpha, most of the emitter current that produces the voltage across R_9 comes from the collector of Q_2. Because alpha varies little with temperature, this current remains stable. Transistors Q_3 and Q_4 constitute a differential pair. Depending on which transistor is conducting, the emitter of one or the other sources current to the collector of Q_1. When the base of Q_3 becomes several hundred millivolts more positive than the base of Q_4, current from Q_2 shunts to the 5V power supply. No current flows through Q_4, so the LED is off. When the base of Q_3 is less positive than that of Q_4, current from Q_2 passes through the LED. The all-or-nothing switching action results from the large differential voltage across the bases. Similar to the case of Q_2, the collector current in Q_4, when it is conducting, is a high and stable percentage of the emitter current. The constant load the emitters of Q_3 and Q_4 present to the current source enables the current source to operate continuously, allowing the use of a low-bandwidth op amp.

Q_1 is a common-base amplifier connected in a manner essentially the same as a TTL-input stage with the exception of C_3, the 1000-pF capacitor across base resistor R_4. When the input signal is greater than 2V, the base of Q_1 remains at 2.5V, and the collector of Q_1 rises enough to ensure that Q_4 and the LED conduct no current. When the input is below 0.4V, Q_1's emitter voltage is low enough and the base current through R_4 is high enough to saturate Q_1. This action holds the base of Q_3 low enough to ensure that all the collector current from Q_2 passes through Q_4 and the LED. When the input signal swings positive again, the energy stored in C_3 develops a reverse bias across Q_1's emitter-base junction to quickly deplete the stored charge, resulting in a rapid turn-off. Make sure that you don't exceed the power rating of Q_4. Take the current and collector-to-emitter voltage into account. Using transistors in TO-92 packages and an LED that drops 2V at 50 mA, the circuit in **Figure 1** operates at temperatures greater than 55°C with a jumper in place of R_{12}. If you need higher currents or use smaller transistor packages, you may find it necessary to use a finite resistor for R_{12} to lower the dissipation in Q_4 to a safe level.□

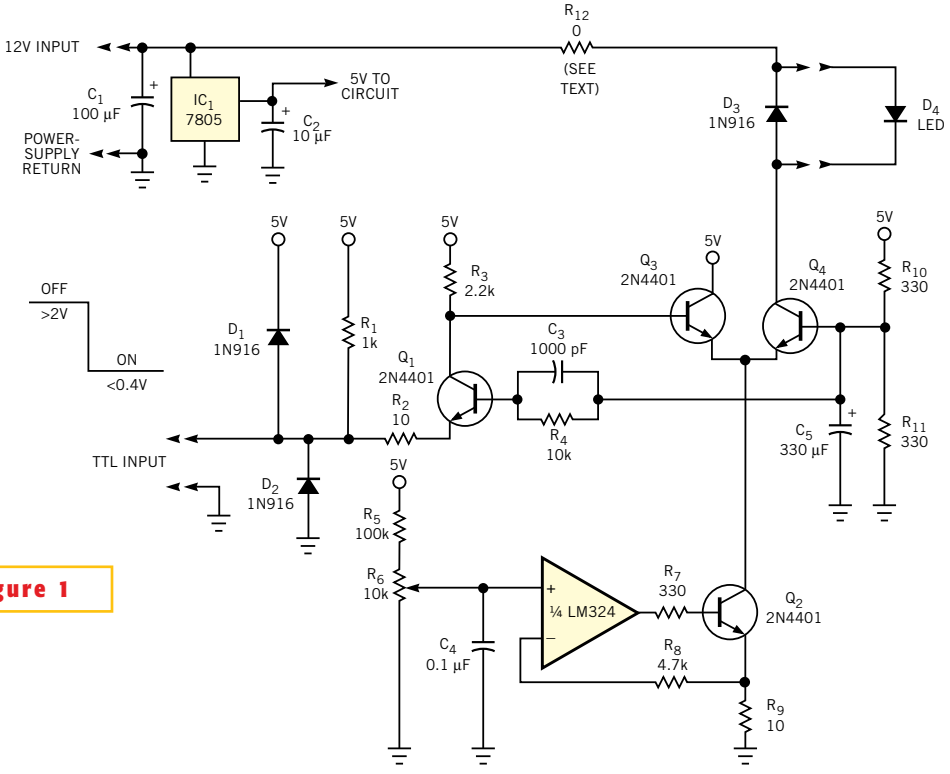


Figure 1

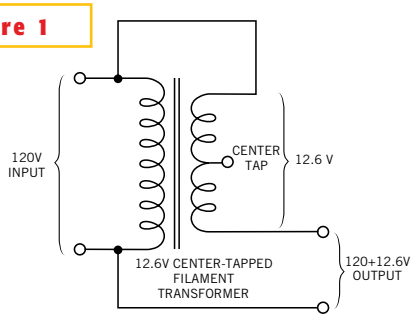
This circuit delivers a stable, precision dose of current to an LED.

Filament transformer adjusts line voltage

EE Barnes, Cochranville, PA

THE PROBLEM: I couldn't use my Heathkit oscilloscope in a house I lived in during the 1960s because my lab was too far from the power-line input to the house, and the line drop through the house was substantial. Depending on the time of day, the screen would shrink to perhaps half the normal display size. I checked the line voltage, and it was down to just approximately 100V. I lacked the funds to buy a high-wattage Variac to deal with the problem.

Figure 1



You can use a small, inexpensive filament transformer to buck or boost the ac-line voltage.

The solution: I had a couple of 12.6V filament transformers, rated at 3 or 4A. I simply connected one of these in my lab, with the primary winding across the ac line (**Figure 1**). Then, I connected the secondary winding such that one side connected to the ac line, and the other side provided the new, boosted ac line. Because the transformer had a center tap, I could adjust the line voltage in 6.3V steps. The beauty of this approach is that the transformer handles only the incremental power from the slight boost in voltage. And the technique uses less space and is less expensive than using a Variac.

Note that, by changing the polarity of the filament transformer's output, you can decrease rather than increase the ac output. This fact could come in handy in situations in which the line voltage is too high, causing incandescent-lamp burnout. Reduction in lamp life is a function of approximately the 13th power of the overvoltage (**Reference 1**). For the long, skinny, and expensive European incandescent lamps that some bathrooms use as a vertical light source, the lamp-life reduction can be significant. You can buck, or subtract, the line voltage to increase the lamps' life. Even at nominal line voltage, you can use the method to drop the voltage to an expensive or particularly inaccessible incandescent lamp.□

REFERENCE

1. Fink, Donald and Christiansen, Donald, *Electronic Engineers' Handbook*, 1975, McGraw-Hill, pg 11-6.

design ideas

Edited by Bill Travis

Seven-segment LCD uses two-wire interface

Hans Krobath, EEC, Nesconset, NY

You can connect seven-segment LCDs using only a two-wire interface (**Figure 1**). The two-wire interface may be at the field-effect, direct-drive LCD or at a serial interface (such as I²C) that uses an eight-pin microcontroller. The design in **Figure 1** uses an Atmel (www.atmel.com) ATtiny12 microcontroller, IC_1. V_{CC} can range from 2.7 to 5.5V. Each digit receives drive from an 8-bit 74HC164 shift register, which provides seven outputs for each of the segments and one output for a decimal point or a colon. The data input to the shift register drives the LCD's common terminal. Software for the eight-pin microcontroller generates the required symmetrical ac square wave between the segments and the common terminal (**Listing 1**, which you can find at the Web version of this Design Idea at www.edn.com). This generation entails shifting the seven-segment data and decimal points to the appropriate outputs and setting the shift-register-input/LCD-common-terminal to low at a less-than 1-msec rate. A delay of 16 msec followed by shifting the same data complemented, as well as the complement of the LCD common terminal with another 16-msec delay, provides the second half of the required ac waveform. Because field-effect LCDs takes tens of milliseconds to respond, the rapid data-shifting and display-common changing does not affect the displayed image. You can use the two 16-msec delays per cycle for application processing.

Directly driving the segments allows the display of not only the numbers zero to nine, but also any combination of segments and decimal points. You can use the eight-pin ATtiny12 with a built-in, 1-MHz clock oscillator to produce the described two-wire signal and to provide a two-wire I²C application interface. The dedicated use of the microcontroller for display control and its I²C interface frees the application hardware and software from timing and resource restrictions. The implemented I²C interface operates at 0 to 40 kbps and is bit-synchronous. One data protocol allows for the input of a two-byte binary integer, which converts to decimal for display. A third byte in the protocol indicates any decimal points or colons. This data format allows the easiest interface from binary measurement or calculation. A second protocol accepts four bytes that directly control the segments and decimal points, allowing the display of a variety of characters and symbols possible on a seven-segment display. You can download the source code and hex object file for the ATtiny12 from the Web version of this Design Idea at www.edn.com. The code provides a two-wire I²C interface for a four-digit Lumex (www.lumex.com) LCD-S401C-52TR display.□

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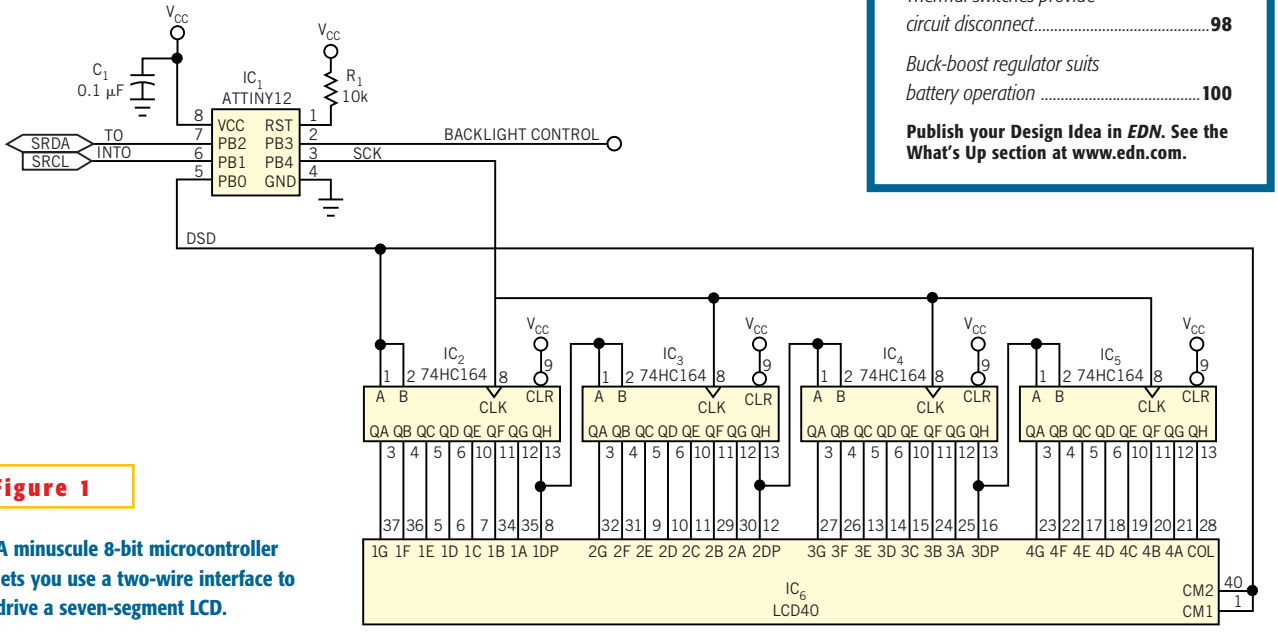

Figure 1

A minuscule 8-bit microcontroller lets you use a two-wire interface to drive a seven-segment LCD.

Open-collector output provides fail-safe operation

Susanne Nell, Breitenfurt, Austria

IT IS COMMON PRACTICE to use digital open-collector outputs for control units in industrial applications. Using these outputs, you can switch loads, such as relays, lamps, solenoids, and heaters. One possible problem inherent to this type of output stage is a short circuit from the output to the supply voltage (often, 24V). This condition can destroy the output transistor if it lacks protection. The simplest approach to solving this problem is to use a fuse. This method has a disadvantage, however: You have to replace the fuse after it blows. A PTC (resettable) fuse is often too slow to protect the transistor under the short-circuit condition. Another possibility is to use a current source as the switching element. This approach is safe and simple, but it produces heat during the error condition. If the power rating and the cooling of the transistor are inadequate, the transistor fails because of thermal overload. The circuit in **Figure 1** shows another simple approach to the fail-safe protection of such switching devices.

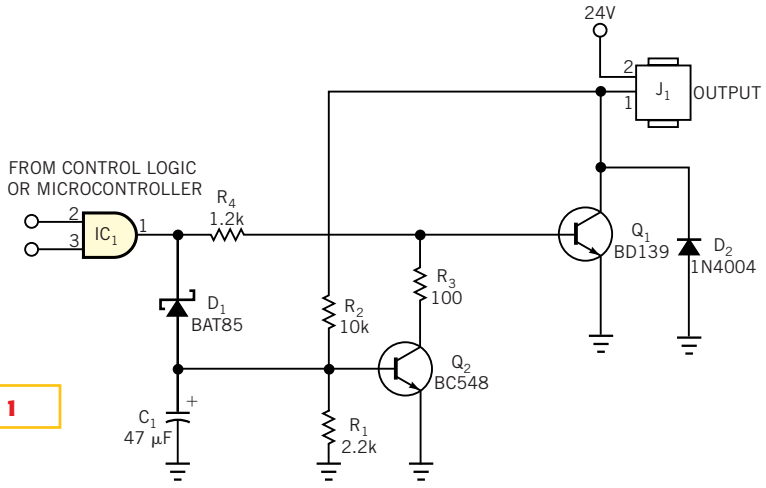

Figure 1

This circuit provides fail-safe protection of an open-collector output stage.

The principal function of the circuit is to switch off the transistor if the voltage on the collector is higher than a predetermined value. Under normal switching conditions, transistor Q_1 should saturate when it turns on with a voltage lower than 0.2V between the collector of Q_1 and ground. If a short circuit exists on the output J_1 or if the impedance of the load is lower than specified, the voltage on the collector of Q_1 rises because too little base-current feed comes from the control logic (via R_4) to saturate Q_1. If the collector voltage of Q_1 reaches the switching voltage on the base of Q_2, Q_2 turns on, and Q_1 switches off. You can adjust this switching point with the R_1-R_2 voltage divider. Now, the voltage on the collector of Q_1 rises to 24V, and the output stays in the switched-off condition. To reset the circuit, you must switch the steering output from the control logic to low. Now, the Schottky diode, D_1, is forward-biased and thus discharges C_1 and switches off Q_2. If the steering output from the control logic again switches to the high state, Q_2 stays in the switched-off condition during the charging of C_1. If the output of Q_1 is not overloaded, Q_1 saturates again and stays switched on. If the output has a short circuit to the supply or it is overloaded, then Q_1 switches on only during the charging of C_1; after this time, Q_2 switches off Q_1. The maximum load current depends on the value of R_4, the output voltage from the control logic, and the current gain of Q_1.□

Low-battery indicator uses fleapower

Yongping Xia, Navcom Technology, Redondo Beach, CA

IT IS ALWAYS DESIRABLE to use a low-battery indicator that consumes as little power as possible. For a 9V, 450-mAhr alkaline battery, a 50-µA low-battery indicator can by itself run the battery down in a little more than a year. Battery-powered devices that need to run continuously for a long time require battery indicators that consume minimal power. The circuit in **Figure 1**, designed for a 9V battery, uses extra-low power. When the battery is at full charge (9V), the circuit draws 1.4-µA current. At the indication-threshold voltage, 6.5V, the circuit draws 1 µA. Assume that the average operating current is 1.2 µA. The circuit uses 42 mAhr in a four-year period, less than 10% of the battery's rated energy. A red LED, D_2, flashes periodically when the battery voltage drops below 6.5V. IC_1, an LTC1540, is a nanopower comparator with a built-in 1.18V reference. A battery-voltage divider comprising $R_1$and R_2, and a positive-feedback network, R_3, feed the positive input of the comparator. The positive feedback generates hysteresis in the comparator. The negative input of the comparator receives bias from the reference voltage, through the R_4-C_1 delay circuit.

During normal operation, the voltage at the positive input is approximately 1.62V when the battery is at 9V. The output of the comparator is at a high state, such that no current flows through D_1 and D_2. When the battery voltage drops

below 6.5V, the voltage at the positive input drops below the reference voltage at the negative input. The output of IC_1 switches from high to low, thereby lighting the LED, D_2. The switching changes the voltage at the positive input to 0.58V and causes C_1 to discharge through D_1 and R_6. Because the value of R_6 is much smaller than that of R_4, the voltage at the negative input drops quickly, according to the time constant that C_1 and R_6 set. Once the voltage at the negative input falls below 0.58V, the comparator switches back to a high state. This change sets the voltage at the positive input to 1.18V, turns off the LED, and reverse-biases D_1, so the reference charges C_1 through R_4. When the voltage at the negative input again reaches 1.18V, the cycle repeats. The LED's on-time is a function of C_1 and R_6, and the off-time is a function of C_1 and R_4. With the values in **Figure 1**, the on- and off-times are 20 msec and 10 sec, respectively, at 6.5V threshold voltage. At this point, the LED's on-state current is (6.5V−1.8V)/2.2 kΩ=2.1 mA. The average LED current is (20 msec×2.1 mA)/10 sec=4.2 µA.□

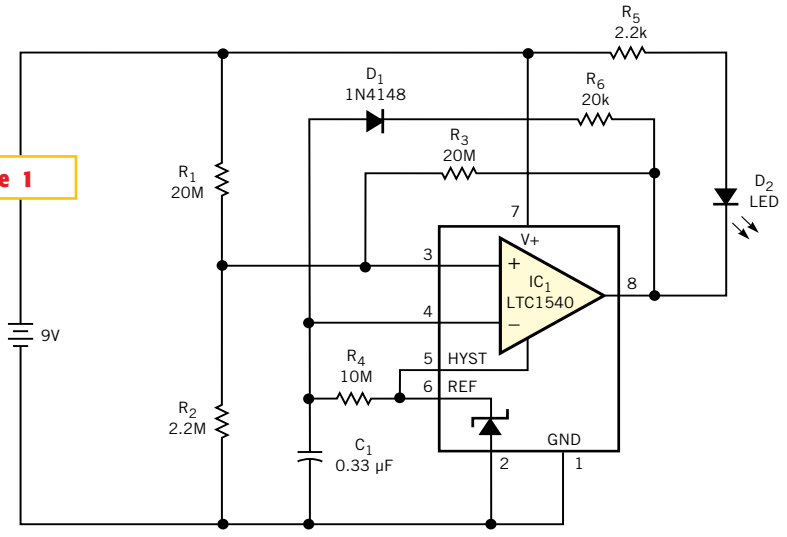

Figure 1

This fleapower low-battery indicator draws just 1.2-µA operating current.

Indicator has "electronic lens"

Abel Raynus, Armatron International Inc, Melrose, MA

THE METHOD for implementing an extended-scale meter described in an earlier Design Idea had a conceptual error: The meter impedance must change continuously, not discretely as expressed (**Reference 1**). You could achieve the desired result by using a digital potentiometer controlled by an input voltage via an appropriate interface. But this approach is probably too sophisticated. **Figure 1** shows an alternative approach that needs only a small and inexpensive microcontroller. The method exploits the fact that a dc meter measures the average value of a PWM signal: $I_{AVG}=I_{PEAK}(T_{PULSEWIDTH})/(T_{PERIOD})$.

Therefore, you can control the current through the meter by changing the pulse width of the PWM signal. The PWM-generating software determines the law that governs the change in current in the meter. In the process of creating this software, you can choose expansion of any part of the scale (**Figure 2**).

The transfer function, a, represents a linear meter response; b denotes expansion of the beginning of the scale; c indicates expansion of the middle of the scale; and d denotes the expansion of the upper end of the scale. The curves with high slopes in the graph of **Figure 2** correspond to expanded scales. You can create the scale patterns by choosing the threshold voltages (breakpoints) and slopes. The circuit resembles an "electronic lens" attached to the meter, which magnifies any chosen part of the scale. The ADC in the microcontroller of **Figure 1** transforms the measured input voltage into its 8-bit hex equivalent. The microcontroller program (**Listing 1** at the Web version of this Design Idea at www.edn.com) reads the hex value and finds a corresponding pulse width from a table in its memory. Finally, the routine generates the PWM signal with the given pulse width. **Figure 3** shows the software flow chart for the process.

As an example of the method, calculate the scale expansion of a 100-µA dc me-

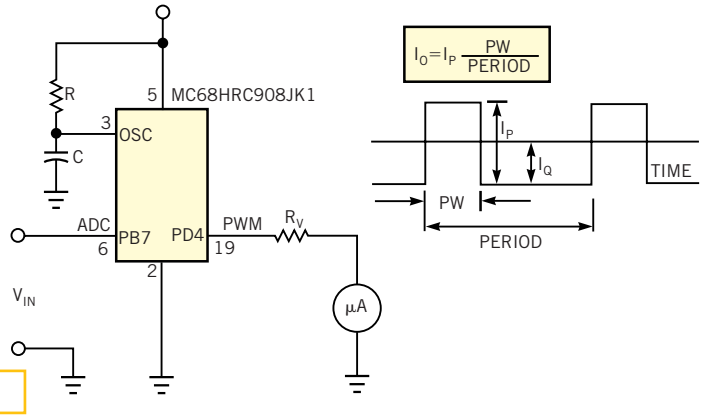

Figure 1

An inexpensive microcontroller allows you to expand any portion of the scale of a linear meter.

ter with a measured-voltage range of 0 to 5V. You need to magnify the portion of the input from 2 to 3V, from 20 to 70%, leaving 10% at the beginning and 20% at the end of the scale (**Figure 2**, characteristic c). **Table 1** shows the steps of the calculations, which you execute as follows:

1. Choose a number (N) and the values of the measured input voltages, V_{IN}. These parameters depend on the desired accuracy of the meter scale. As an example, assume voltages with increments of 0.5V for the low slope (**Figure 2**) and 0.1V for the high slope (**Table 1**, column 2). Therefore, N=19.

2. Calculate the 8-bit ADC's digital output, N_{IN}, for the selected input voltages (column 3): $N_{IN}=(256/5)V_{IN}=51.2V_{IN}$.

3. Transform N_{IN} from decimal to hexadecimal format (column 4). The errors arising from the 8-bit quantization are insignificant for an analog indicator.

4. Choose the PWM period, T. This value depends on the rapidity of the input-voltage change and should be relatively short to prevent needle chatter. Assume T=10 msec for easy **Table 1** calculations.

5. Calculate the number of timer cycles for the PWM period. The accuracy of any microcontroller's time intervals is a function of the accuracy of its oscillator frequency, which for the MC68HRC908K1 depends on the external RC circuit. The data sheet for the IC recommends a tolerance of 1% or less for these components to obtain a clock tolerance of 10% or better. But it is difficult to find a 10-pF±1% capacitor, so this design uses a less expensive 5% capacitor and measures the oscillation frequency. According to the microcontroller manual, the timing components R=20 kΩ and C=10 pF should yield a frequency of approximately 4.5 MHz. The measured frequency is 5.75 MHz. With the timer/counter prescaler set at 64, the timer-clock period is 44.5 µsec. Hence, you can calculate the number of timer cycles for any time interval as $N_t=(t \text{ in milliseconds})/(44.5\times10^{-3})=22.5\times(t \text{ in milliseconds})$. Thus, for T=10 msec, $N_{10}=225$ or $N_{HEX}=\$E1$.

6. Determine the duty cycle (α) of the PWM signal for each chosen input voltage, V_{IN}, as well as the scale-expansion pattern (column 5); $\alpha=(I_V/I_{MAX})\times100\%$. You could either read the current value directly from the diagram in **Figure 2** (characteristic c) or calculate it for three linear parts of the scale with the following equation: $I_V=I_{Ti}+S_i(V_{IN}-V_{Ti})$, where I_V is the current for the given input voltage V_{IN}, I_{Ti} is the current for the threshold voltage V_{Ti} (i={1,2,3}), and S_i is the slope of each linear portion of the scale in **Figure 2** (characteristic c). The expressions for the three piecewise-linear segments are as follows:

$$V_{T1}=0;\ I_{T1}=0;\ S_1=\frac{10}{2}=5\ \mu A/V.$$

$$V_{T2}=2V;\ I_{T2}=10\ \mu A;$$
$$S_2=\frac{80-10}{3-2}=70\ \mu A/V.$$

$$V_{T3}=3V;\ I_{T3}=80\ \mu A;$$
$$S_3=\frac{100-80}{5-3}=10\ \mu A/V.$$

7. Determine the pulse width of the PWM signal: PW=αT (column 6).

8. Calculate the number of timer cycles, N_{OUT}, for this pulse width by using

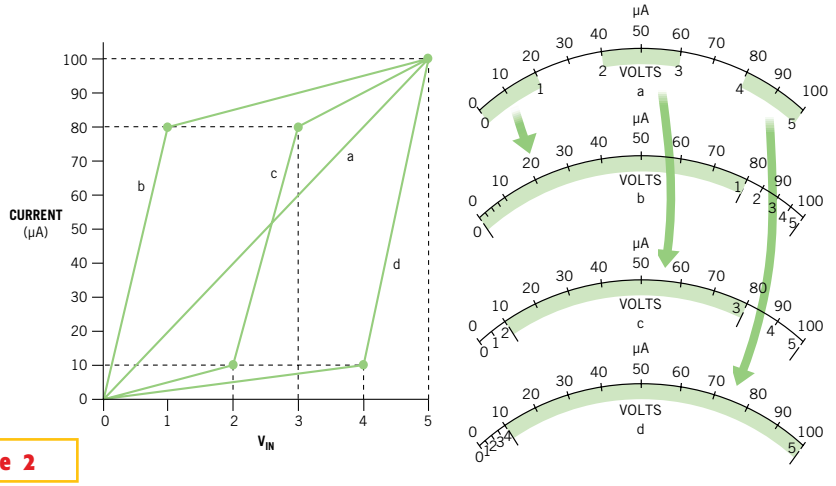

Figure 2

By selecting slopes and breakpoints, you can expand the bottom (b), the middle (c), or the top (d) portions of a linear meter's response.

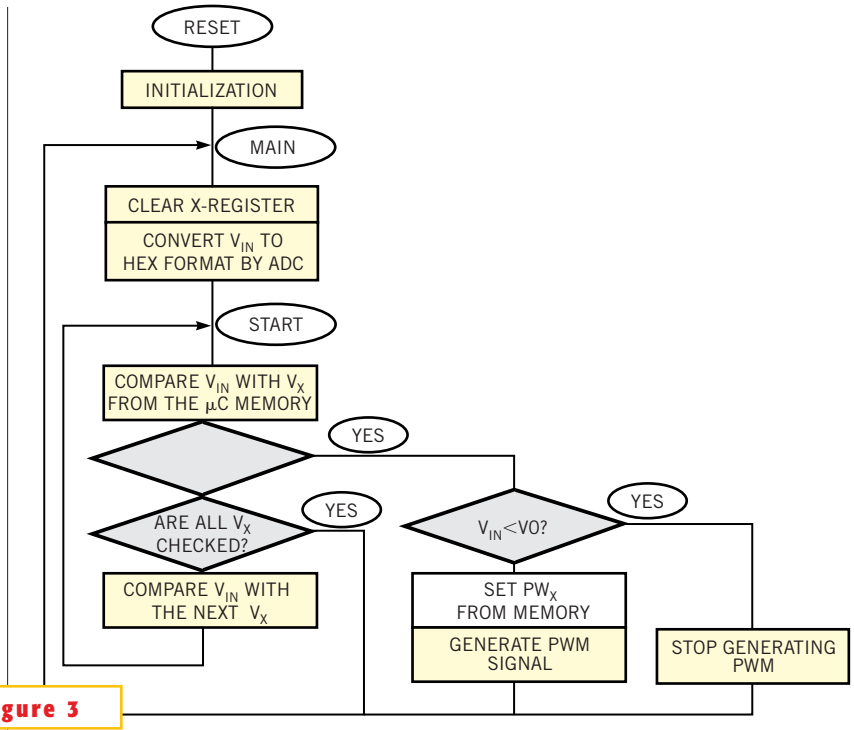

Figure 3

This flow chart shows the steps in the scale-expansion process.

the equation for N_t and transform the number into hexadecimal format (columns 7 and 8).

9. Enter N_{IN} and N_{OUT} **Listing 1.**

You can use any microcontroller with a PWM function and built-in ADC. The one in **Figure 1** has a 12-channel, 8-bit ADC and the capability to generate a PWM signal. This microcontroller has 15 I/O pins, which are necessary for executing other functions. If your application needs only to effect the meter-scale expansion, then the eight-pin 68HC908-QT2 is probably a better choice. This microcontroller has a built-in oscillator and costs less than $1. You can download **Listing 1** from the Web version of this Design Idea at www.edn.com.□

TABLE 1–EXAMPLE OF MIDSCALE EXPANSION

1 x	2 V_{IN} (V)	3 N_{IN}	4 N_{IN} (hexadecimal)	5 α (%)	6 Pulse width (msec)	7 N_{OUT}	8 N_{OUT} (hexadecimal)
0	0.04	2	$2	0	0	0	$0
1	0.5	25.6	$1A	2.5	0.25	5.6	$6
2	1	51.2	$33	5	0.5	11.2	$0b
3	1.5	76.8	$4D	7.5	0.75	16.87	$11
4	2	102.4	$66	10	1	22.5	$16
5	2.1	107.5	$6C	17	1.7	38.25	$26
6	2.2	112.6	$71	24	2.4	54	$36
7	2.3	117.8	$76	31	3.1	69.75	$46
8	2.4	122.9	$7B	38	3.8	85.5	$55
9	2.5	128	$80	45	4.5	101.25	$65
10	2.6	133.1	$85	52	5.2	117	$75
11	2.7	138.2	$8A	59	5.9	132.75	$85
12	2.8	143.3	$8F	66	6.6	148.5	$95
13	2.9	148.5	$94	73	7.3	164.25	$A4
14	3	153.6	$9A	80	8	180	$B4
15	3.5	179.2	$B3	85	8.5	191.25	$BF
16	4	204.8	$CD	90	9	202.5	$CB
17	4.5	230.4	$E6	95	9.5	213.75	$D6
18	5	250.9	$FB	99	9.9	222.75	$DF

REFERENCE

1. Raynus, Abel, "Expanded-scale indicator revisited," *EDN*, Aug 8, 2002, pg 112.

Thermal switches provide circuit disconnect

Mark Cherry, Maxim Integrated Products, Sunnyvale, CA

A SINGLE TEMPERATURE sensor can provide an interrupt to a microcontroller when the measured temperature goes out of range. You need multiple temperature sensors when you have to monitor more than one hot spot. A microcontroller implements the proper protective action when one of the temperature monitors detects an overtemperature condition. It is sometimes easier and more cost-effective to simply disconnect the offending circuit from the power supply without involving a microcontroller. A simple thermal-protection circuit (**Figure 1**) includes two temperature switches, IC_1 and IC_2, with active-high outputs. Temperature thresholds for these switches depend on resistors R_1 and R_2, and the switch outputs connect to the inputs of a dual-input OR gate, IC_3. OR gates with more than two inputs are available if you need more than two temperature switches. When excessive temperature drives either input high, the OR gate's output switches high, causing an SCR (silicon-controlled rectifier) to crowbar the power supply and blow the fuse. You must take precautions to ensure that the SCR does not trigger on a false gate pulse. Power-supply transients can cause a false high signal at the output of the OR gate and cause the SCR to turn on. Once triggered, the SCR cannot turn off, and the fuse blows. A small RC filter, R_3 and C_3, suppresses any gate transients that would otherwise turn on the SCR.□

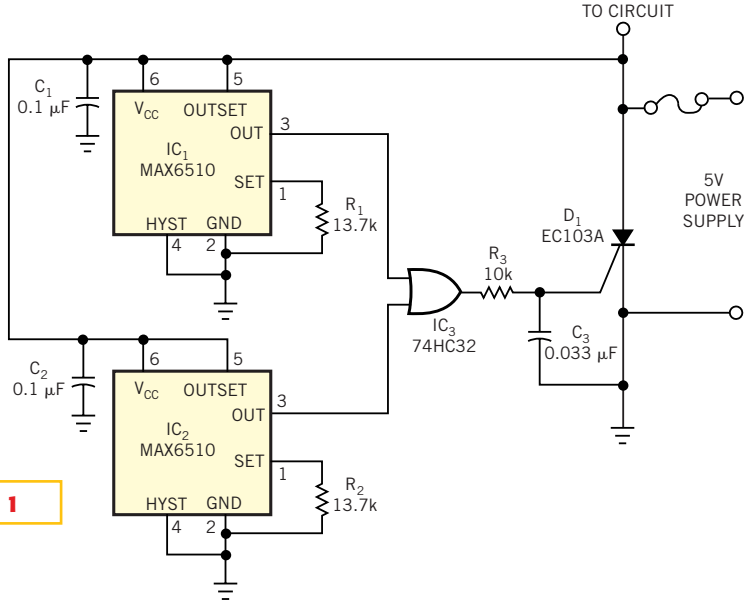

Figure 1

This thermal-protection circuit includes a crowbar device, D_1, driven by thermal switches IC_1 and IC_2.

Buck-boost regulator suits battery operation

Kahou Wong, On Semiconductor, Phoenix, AZ

A BUCK/BOOST CONVERTER can step a voltage up or down. Such a converter is appropriate for battery-powered applications. One application derives a regulated 14.1V at 1A from 12V solar panels with 9 to 18V variation. In this type of battery application, efficiency is an important factor; hence, this design uses an inexpensive synchronous-rectifier-based MC33166/7 circuit. It is difficult to find a buck-boost controller in the market. It is even more difficult to find an inexpensive one with an integrated high-current switch. One way to build a buck-boost converter is to use a buck regulator with an internal switch, such as the MC33166/7 (**Figure 1**). The negative-polarity output voltage connects to the IC's ground pin, and a resistor pair divides the 14.1V output voltage to 5V for connection to the FB pin of the IC. So, the IC effectively regulates an input of $V_{IN}+V_{OUT}=18+14.1=32.1$V to an output of 14.1V.

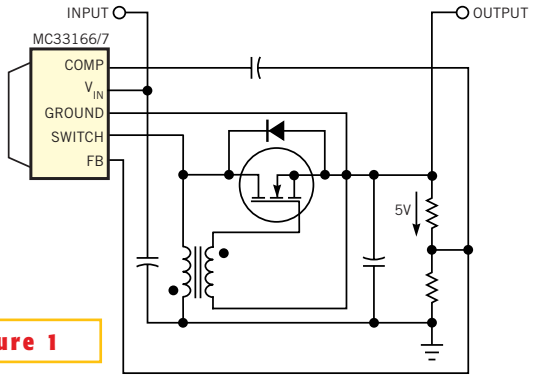

Figure 1

This inexpensive buck-boost controller uses synchronous rectification for high efficiency.

The MC33166/7 has a 40V maximum switch rating, and it can accommodate 95% duty cycle, so it's adequate for the application. To implement synchronous rectification for better efficiency, the design uses an additional transformer winding and a MOSFET. The auxiliary winding provides bias voltage to turn on the MOSFET when the switching-node polarity turns negative. Note that the synchronous rectifier is an important factor in the efficiency of this circuit, because the input-to-output ratio is approximately 1-to-1. So, the duty cycle is approximately 50%, which means that the MOSFET conducts for half the switching-frequency period.□

design ideas

Edited by Bill Travis

Dual comparator thermally protects lithium-ion battery

Mike Hess, Maxim Integrated Products, Sunnyvale, CA

Most manufacturers recommend that you don't change lithium-ion batteries at temperatures lower than 0°C or higher than 50°C. You can monitor both thresholds by adding a thermistor and dual (window) comparator to a lithium-ion battery charger (**Figure 1**). Set the low-temperature trip point at 2.5°C and the high-temperature trip point at 47.5°C. A precision voltage reference is unnecessary, because the comparator's resistor network is ratiometric, so variations on the supply voltage, V_{BUS}, do not affect the trip thresholds. By driving the charger's enable input, EN, the comparators' open-drain outputs ensure that charging is inhibited when the battery temperature is out of range. As an alternative, you can substitute a dual comparator with push-pull CMOS outputs, such as the MAX9032, if you also add a tiny, SOT-323 dual diode (the dashed lines in **Figure 1**). The dual comparator and the MAX9032 are available in SOT-23 packages, and both offer built-in hysteresis of 2 or 4 mV, respectively.

IC_2 is a single-cell lithium-ion battery charger that can derive its power directly from a USB port or from an external supply as high as 6.5V. The 0.5% accuracy of its battery-regulation voltage allows maximum usage of the battery's capacity. The charger's internal FET delivers as much as 500 mA of charging current, and you can configure its SELV input for charging a 4.1 or 4.2V battery. The SELI input sets the charge current to either 100 or 500 mA, and an open-drain output, CHG, indicates the charge status. For near-dead batteries, a preconditioning capability soft-starts the cell before charging. Other safety features include continuous monitoring of voltage and current and initial checking for fault conditions before charging.□

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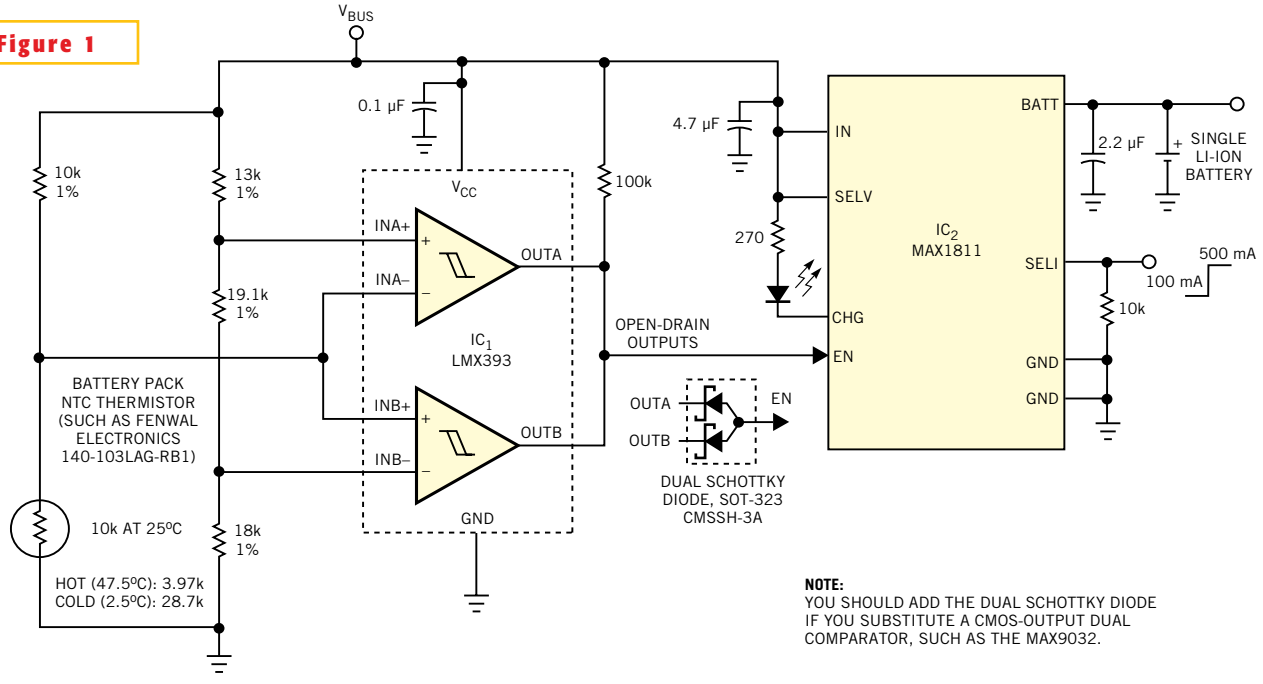
Figure 1



NOTE:
YOU SHOULD ADD THE DUAL SCHOTTKY DIODE IF YOU SUBSTITUTE A CMOS-OUTPUT DUAL COMPARATOR, SUCH AS THE MAX9032.

While charging a lithium battery from a USB port, this circuit provides thermal protection for the battery.

Lowpass filter discriminates step input from noise

Eric Desrochers, Aircuity Inc, Newton, MA

Numerous applications exist in industry, particularly with control systems, in which it is desirable to remove all but the lowest frequency components from a signal to effectively yield a dc voltage. This voltage may, for example, serve as a setpoint to a PID controller in a process-control or an HVAC application, in which the cable that is carrying the analog signal is exposed to a wide spectrum of noise, including low-frequency noise components from various sources. These sources could include variable-speed drives, ballasts, transients from switching gear, and motors. In many cases, noise reduction using a conventional lowpass filter can create adverse effects in the response time of the system, even if you use a multipole filter. As an alternative, the circuit of **Figure 1** is ideally suited to provide extensive noise reduction for applications such as these without impairing a system's ability to track rapid changes in signal level. The concept involves a lowpass filter with a slewing mechanism that has significant performance advantages over other nonlinear-lowpass-circuit topologies, given its ability to discriminate step changes in signals from noise.

The basic operation of the circuit is to momentarily increase the corner frequency of the lowpass filter formed by R_6 and C_3, using an analog switch, IC_1, upon detection of a step change in signal, allowing V_{OUT} to track V_{IN} with little delay. IC_1 has an on-resistance of about 100Ω, so when it closes across R_6, the corner frequency of the circuit changes from 0.016 Hz to approximately 160 Hz, which is ample bandwidth for the target applications for this circuit. IC_{2B}, along with R_4, R_5, and C_2, operates as an error amplifier with a corner frequency of $f_{CERR}=1/2\pi R_5C_2=1.59$ Hz. The amplifier generates an error signal, V_{ERR}, that IC_{2A} measures in reference to V_{OUT}. IC_{2A} acts as a floating window comparator that places the lowpass filter into slew mode when V_{ERR} exceeds the predetermined threshold that zener diode D_3 establishes. For values of V_{ERR} that are greater than V_{OUT}, diode D_2 conducts, causing the noninverting input of IC_{2A} to track this signal. IC_{2A} compares the signal to a threshold voltage of approximately $V_{OUT}+5.2$V at its inverting input. When a negative-step change ($V_{IN}<V_{OUT}$) to the input, V_{IN}, is of sufficient amplitude such that V_{ERR} becomes approximately 5.7V (accounting for the barrier potential of D_2), IC_{2A}'s output switches high. This action activates IC_1, causing a short circuit across R_6, thus allowing V_{OUT} to track V_{IN}.

For values of V_{ERR} below V_{OUT}, the action is similar, except that the inverting input of IC_{2A} tracks V_{ERR} through D_3 and D_4, and the comparator's output toggles high at the point at which V_{ERR} is approximately 5.2V below V_{OUT}. Although the asymmetry in the window comparator's performance is not of great significance, you could realize improved symmetry by replacing D_2 with a Schottky diode, which has a lower barrier potential. The comparator's trip points, along with the dc gain of the error-amplifier stage (IC_{2B})—determined by the ratio R_5/R_4—establish the upper and lower deadband of **Figure 1**. With the values shown in **Figure 1** the circuit triggers to slew in response to negative-step changes in V_{IN} as small as 0.260V and positive-step changes that are as small as 0.285V. You can realize better sensitivity by reducing the zener voltage of D_3 or by increasing the ratio R_5/R_4 and ensuring that the error-amplifier stage provides adequate roll-off. The roll-off must ensure that noise levels that may ex-

(continued on pg 96)

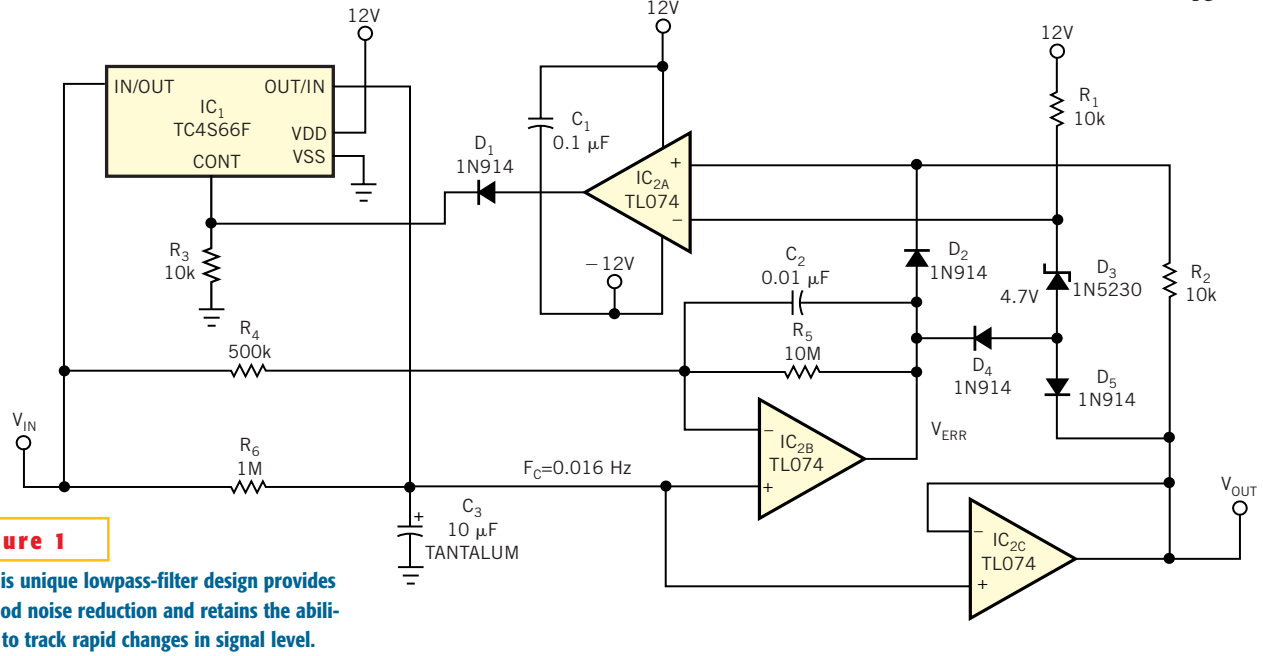


Figure 1

This unique lowpass-filter design provides good noise reduction and retains the ability to track rapid changes in signal level.

ist in a given application cannot trigger the circuit into slew mode.

Another important parameter to consider when choosing component values for the error- amplifier stage is the step response of that circuit, because it directly impacts the overall settling time of the lowpass filter when it encounters step changes in signal. To be conservative, choose values for R_5 and C_2 such that three times the RC time constant they form is well within the settling time desired for the lowpass filter. For example, with $R_5=10\ M\Omega$ and $C_2=0.01\ \mu F$, $3\tau=0.3$ sec. This case represents the approximate worst-case delay to the response to a step change in V_{IN} that is outside the deadband of the circuit. In practice, however, the delay is much smaller for step changes in V_{IN} that are larger in magnitude, given the first-order nature of this circuit. **Figure 2** illustrates the response of the lowpass-filter design to a 600-mV step change in V_{IN}. The graphic also illustrates the circuit's significant filtering capabilities on a severe, 30-Hz, 640-mV p-p noise component superimposed on the signal. An ac-coupled view of the filter's performance at steady state illustrates more than 65 dB of attenuation at 30 Hz (**Figure 3**).□

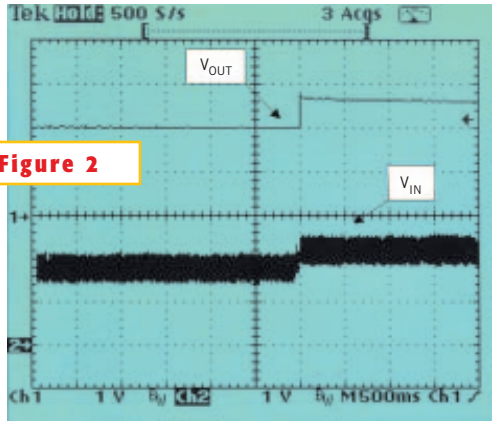


Figure 2 The circuit in Figure 1 has good step response, even with a nasty 640-mV p-p, 30-Hz noise term superimposed on the input.

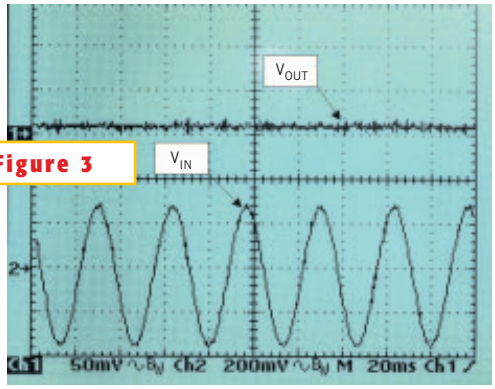


Figure 3 This ac-coupled view illustrates more than 65 dB of attenuation at 30 Hz.

Voltage-to-current converter makes a flexible current reference

Art Kay, Texas Instruments, Tucson, AZ

The voltage-to-current converter in **Figure 1** can both source and sink current. The circuit is more flexible than some traditional current references that require different topologies for current sourcing and sinking. Also, you can easily adjust the value of the current reference by simply adjusting the circuit's input voltage. Performing a simple nodal analysis generates the following equation:

$$I_{OUT}=\frac{-R_2V_{IN}}{R_1R_3A_{IC2}}.$$

You typically set R_1 equal to R_2. The output current is a function of R_3 and the gain of the instrumentation amplifier. Note that capacitor C_1 stabilizes the circuit. In this example, $R_3=10\ M\Omega$, and the instrumentation amplifier's gain is unity. Varying the input, V_{IN}, by ±10V yields a current-output range of ±1 μA. Performing a more detailed nodal analysis on the circuit in **Figure 1** yields the following equation:

$$I_{OUT}=\left[\frac{-R_2V_{IN}}{R_1R_3A_{IC2}}\right]+$$
CURRENT TERM
$$\left[\frac{R_2V_{OS1}}{R_1R_3A_{IC2}}+\frac{R_1V_{OS2}}{R_1R_3}+\frac{R_1V_{OS1}}{R_1R_3A_{IC2}}+I_{B2}\right],$$
ERROR TERM

where V_{OS1} and V_{OS2} are the offset voltages of IC_1 and IC_2, respectively, I_{B2} is the input-bias current of IC_2, and A_{IC2} is the gain of IC_2.

This second equation is useful in understanding error sources and, consequently, can aid in selecting the components that are best suited to an application. For example, for a nanoampere current reference, you should consider the error that the instrumentation amplifier's bias current generates. The example in **Figure 1** uses the INA121P FET-input instrumentation amplifier to minimize the input-bias current. A milliampere reference, on the other hand, would focus more on the input offset voltage of the instrumentation amplifier. In general, you can neglect the error that the offset voltage of the op amp generates if you use a precision, low-offset amplifier. However, resistor-mismatch and instrumentation-amplifier gain errors are inevitable, regardless of the application.□

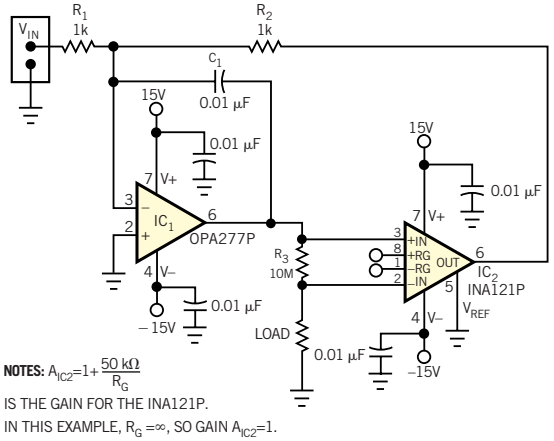


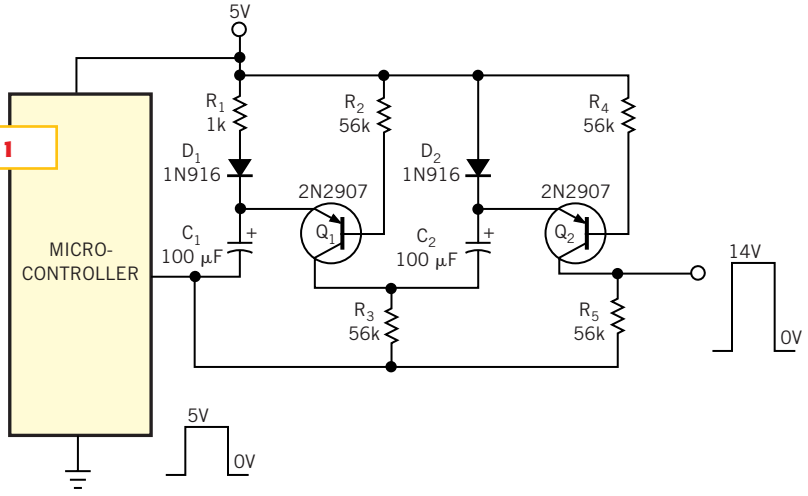
Figure 1 This current reference delivers an output that's a linear function of the input voltage.

Circuit forms single-pulse voltage multiplier

Richard Cappels, Mesa, AZ

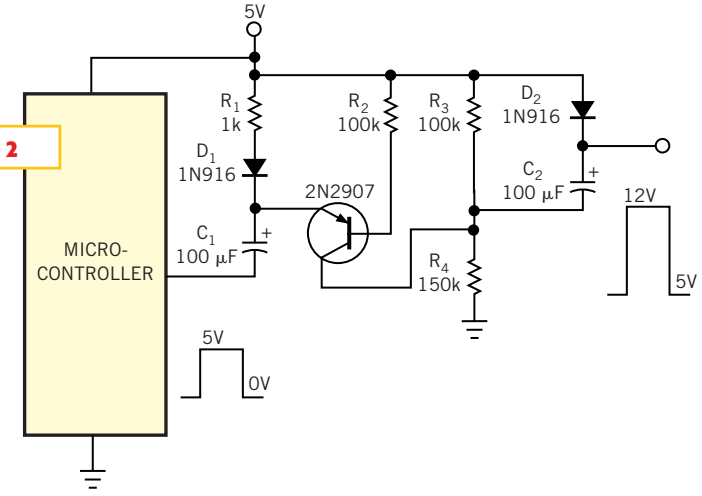
It is sometimes necessary for a microcontroller to generate a pulse whose voltage is higher than the power-supply voltage of the microcontroller. The circuit in **Figure 1** allows you to generate 14V pulses from a 5V power supply. An adaptation of the circuit provides a 5 to 12V programming pulse for programming the fuse bits in Atmel (www.atmel.com) microcontrollers (**Figure 2**). The approach is economical, in that it combines the voltage-multiplier and pulse-amplifier functions. Moreover, the technique benefits from the absence of noise that would arise from a continuously running switching power supply. In **Figure 1**, when the microcontroller's output is low, C_1 and C_2 charge in parallel to nearly 5V. When the microcontroller switches to 5V, it effectively makes the capacitors appear in series with the 5V pulse, resulting in a pulse approaching three times the power-supply voltage at the output. C_1 charges through D_1, and R_1 limits the charging current from the microcontroller's output to a few milliamperes. C_2 charges through D_2 and R_3.

Figure 1



This simple circuit provides single pulses of 14V from a 5V power supply.

Figure 2



This variation on the circuit of Figure 1 supplies fuse-programming pulses for Atmel ATV microcontrollers.

During the output pulse, C_1 must supply the base current for Q_1 and Q_2, as well as the load current. Because the voltage drop across the diodes decreases as current through them diminishes, after a charging time of several time constants, the diode drop is only a couple of hundred millivolts. Therefore, pulses of nearly three times the power-supply voltage are possible. When the pulses are continuous or when they occur within a couple of time constants of power application, diode drops of approximately 1.5V subtract from the output. Additional losses can arise from voltage drops across the resistance of the microcontroller and saturation losses in the transistors. You can reduce the saturation losses by reducing the values of R_2 and R_4, but be aware that reducing these values increases the droop rate of the output pulse. For some applications, you could omit D_1 and replace D_2 with a resistor, but the result would be longer charging and faster discharging for the capacitors. These trade-offs are acceptable for some applications.

The circuit in **Figure 2** provides a 5 to 12V programming pulse for Atmel ATV microcontrollers for the couple of hundred milliseconds the ICs require. Because the output during the time the microcontroller's output is low needs to be 5V, you omit the second transistor and take the output directly from the cathode of D_2. Because the output voltage needs to go to only 12V, C_2 charges from a voltage divider. C_2 charges to only 2V, which then appears in series with the 10V from the series combination of C_1 and the output of the microcontroller. You get no "free lunch" with this circuit. If the pulse initiation occurs before R_3 and R_4 sufficiently charge C_2 (60 kΩ×100 µF=6 sec), the voltage is lower than intended. You can reduce the charge time of the circuit by reducing the values of the capacitors. C_2 has the most effect because of the high-resistance charging path. However, reducing the capacitor values makes the output pulse droop more quickly.□

Feedback circuit eliminates CCD-driver delay mismatch

Mike Wong, Intersil-Elantec, Milpitas, CA

In a CCD (charge-coupled device), packets of charges shift across the array. The transistor array, also called a bucket-brigade shift register, receives drive from a dual-phase clock signal. Dual-phase clock signals comprise two synchronized clock signals that are 180° out of phase. High peak-output-current CCD drivers can buffer the logic-level clock signals and turn them into high-voltage and high-peak-current signals to drive the heavily capacitive gates of the many CCD transistors. Because of the speed mismatch of CCD-drivers' n- and p-channel FETs, the turn-on and -off delay times are poorly matched. **Figure 1** shows the outputs of one such current CCD driver, Intersil's EL7212 (www.elantec.com), with a dual-phase input clock. The overlap in the output stems from the turn-on and -off delay mismatches of the EL7212.

In a low-resolution system with a lower clock frequency, the delay mismatch is an insignificant part of the clock period. As CCD scan rate increases, the mismatch becomes a large part of the clock period. You need a new approach to correct the CCD-driver delay mismatch. **Figure 2** shows a circuit that uses amplifiers to sense the delay mismatch and correct it. Because $\overline{V_{OUT}}$ and V_{OUT} are 180° out of phase, if their turn-on and -off times coincide perfectly, the voltage between R_4, R_7, and C_2 is $1/2V_{CC}$. Amplifiers IC_{2A} and IC_{2B} compare voltage on C_2 with the $1/2V_{CC}$ reference voltage and adjust the voltage between R_3 and R_6. IC_{2A} provides the phase inversion, and IC_{2B} is the high-dc-gain error-correction amplifier. The output of the error amplifier drives R_3 and R_6, which shift the voltage offset of the incoming clock signal. When the offset-voltage level of the input clock signal shifts, the time at which the CCD driver is triggered also shifts. IC_{2A} and IC_{2B} guarantee that the proper offset voltage goes to the input clock signals so that the delay mismatch cancels. D_1 and D_2 rectify the input clock signals and create the supply voltage to the IC_{2A} and IC_{2B} amplifiers. When the input signals are removed, the power to the amplifiers shuts off, and the error-correction loop deactivates to prevent output oscillation with no inputs.□

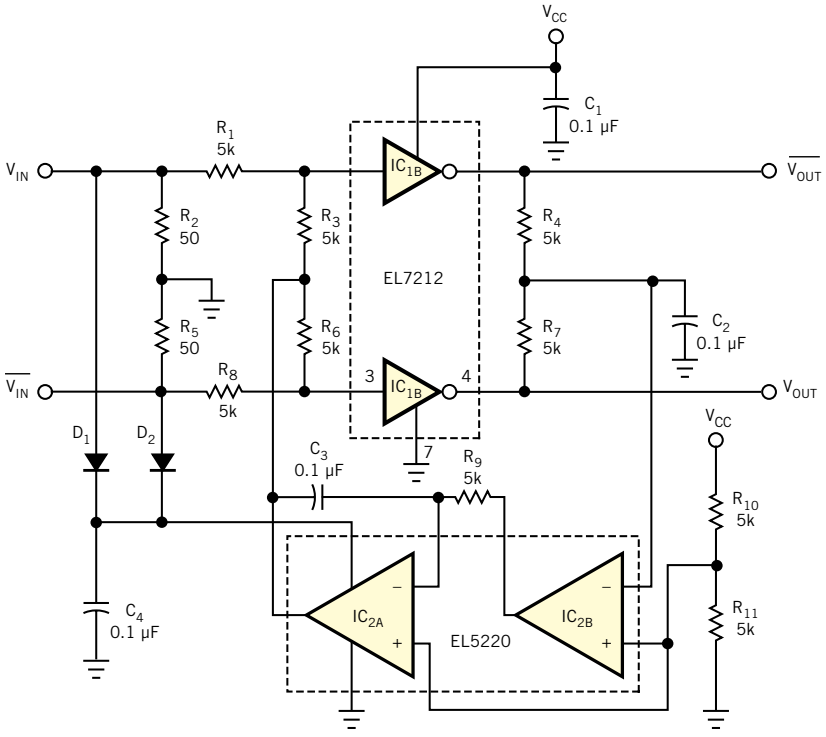


Figure 2 This circuit can correct the mismatch in turn-on and -off delays in a CCD-driver IC.

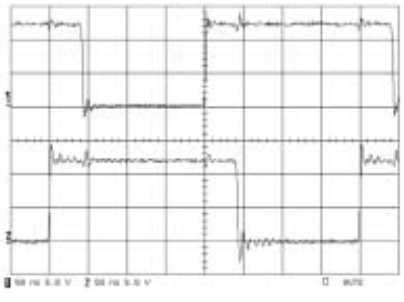


Figure 1 In a CCD driver, a mismatch may occur in the turn-on and -off delay times.

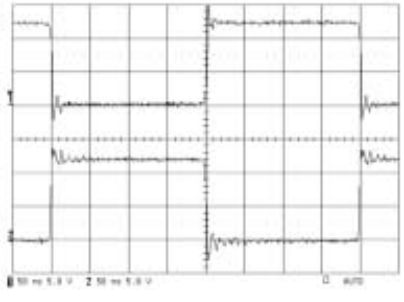


Figure 3 After the circuit in Figure 2 does its job, the turn-on and -off waveforms line up nicely.

design ideas

Edited by Bill Travis

Simple emulator speeds testing

Navdhish Gupta, Chicago, IL

Designing and testing embedded hardware can be frustrating if you have to rely on somebody else's perhaps-unready firmware to test your hardware. Often, hardware is ready for testing before debugging and system firmware are available from software developers. Microprocessor emulators are solutions but are often expensive, hard to use, and sometimes inappropriate for use by hardware developers, who often just need to read and configure registers on devices on their boards. If you are not primarily concerned with your processor's bus performance and need simple read and write access to registers on chips on your board to configure and test hardware, then building a simple processor-bus emulator, such as the one in **Figure 1,** may be an attractive option. The simple emulator shown uses an easy-to-use Basic Stamp microcontroller (www.parallax.com) on a carrier board and a small CPLD to emulate a 16-bit "ISA-like" I/O bus. **Figure 2** shows the timing parameters for the bus (**Figure 2a** shows write-cycle timing; **Figure 2b** shows read-cycle timing). Note that the bus emulator runs much slower than a "normal" processor bus but is useful to read and configure registers that you need to test hardware. This design uses the 16-bit ISA-like bus mainly for illustrative purposes; you could emulate almost any processor bus with a similar setup.

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The simple emulator consists of two parts, the hardware (**Figure 1**) and the Basic Stamp firmware (**Listing 1**, which you can download from the Web version of this Design Idea at www.edn.com). You must connect the emulator itself to a 5V power supply and a PC with a keyboard, monitor, and serial port, and you load any simple terminal-emulator software, such as Hyper Term. The serial programming cable you use to program the Basic Stamp also communicates with the terminal-emulator software by inserting a switch, S_1, that lets you disconnect or connect the DTR/ATN connection. When the switch is closed, you can program the Basic Stamp, and, when it is open, you can use the terminal-emulator software to communicate with the Basic Stamp. You enter commands on the keyboard, and the results appear on the monitor. The emulator connects to the board and devices to test and configure, such as a custom FPGA, through the board's normal processor bus. (You need to either socket the original processor or provide a test port on the board.) You tristate the original processor or remove it from the board to use the emulator.

The Basic Stamp firmware emulates processor-bus cycles by changing the appropriate control signals on its pins. The

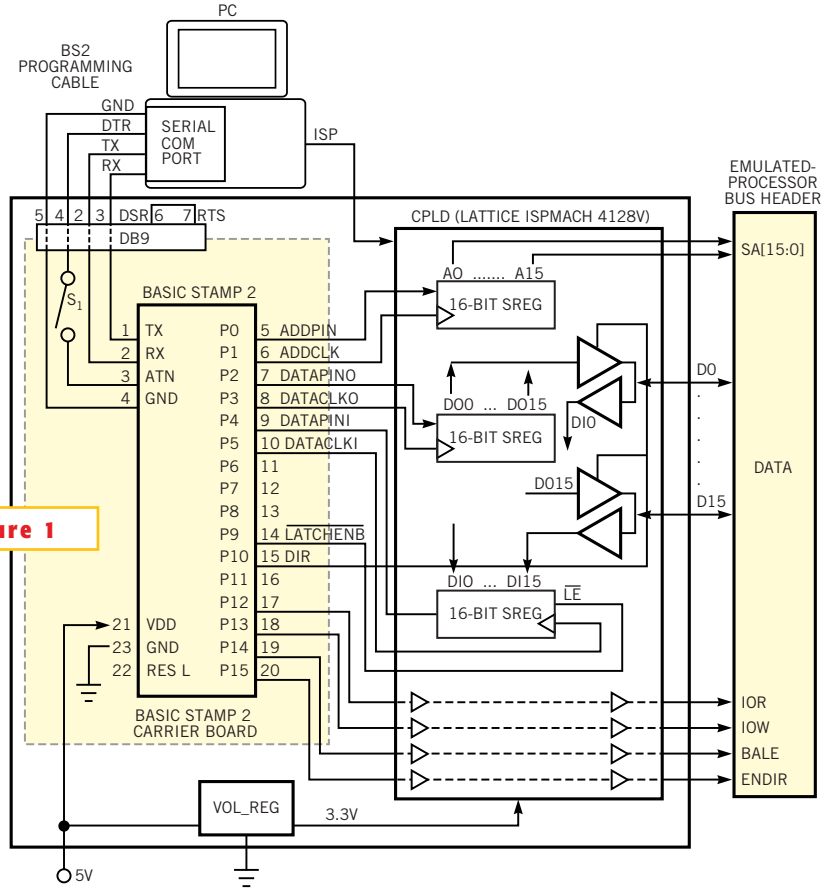


Figure 1

A simple emulator uses a Basic Stamp microcontroller and a small CPLD.

CPLD uses shift registers to interface the serial address and data into and out of the Basic Stamp to the emulated 16-bit parallel address- and data-bus signals. The CPLD also "conditions" the control signals from the Basic Stamp to the emulator header by performing logic-threshold conversion through CPLD I/O buffers. **Listing 2**, also available from the Web version of this Design Idea at www.edn.com, shows the Verilog code for the CPLD. Note that, although the control signals IOW, IOR, BALE, and ENDIR come from the basic code firmware and the Basic Stamp pins and are conditioned through the CPLD; they could come directly from a simple finite-state machine in the CPLD if your design requires more realistic bus timing. The Lattice (www.latticesemi.com) ispMACH 4128V CPLD is a 5V-tolerant device whose inputs you can safely drive with voltages as high as 5.5V. It also supports as many as 64 I/O lines and is in-system-programmable through the IEEE-standard 1532 interface. These features make the CPLD a good choice for use in the hardware implementation of the logic needed in the emulator.□

Figure 2

The simple emulator uses Basic Stamp signals for write-cycle timing (a) and read-cycle timing (b).

Software snippet provides improved subset-sum algorithm

Ivan Basov, Brandeis University, Waltham, MA

The subset-sum problem is one of the most frequently occurring NP (nondeterministic, polynomial-time)-complete) problems. It asks whether a subset of numbers in a set of positive integers adds up exactly to a given value. A relaxed version of the problem tries to identify a subset of numbers that adds up to a maximum value no greater than a given value. This problem arises in transportation, network design, scheduling, logistics systems, robotics, and many other areas. The problem permits you to develop and illustrate the power of different algorithmic tools. The problem is as follows:

Given a set of positive integer values W[1], W[2], ...W[m] and an integer n.0, does a subset of the values add up to exactly n?

A well-known pseudo-polynomial algorithm (**Reference 1**) defines a table: T[ij], $1 \le i \le m$ and $1 \le j \le n$, to be T[ij]=true if and only if a subset of W[1],...W[i] sums to exactly j. The algorithm uses O(mn) time to fill in a table that uses O(mn) space. **Table 1** with n=13 shows the true entries and leaves the false ones blank. This Design Idea proposes an improved algorithm that uses O(mn) time to fill in an array that uses only O(n) space:

SubsetSum(W, m, n)
1. Define a bit array A[j], $1 \le j \le n$.
2. Initialize the array to zeros.
3. A[0]:=1.
4. for i:=1 to m do.
5. for j:=n to 0 do.
6. if A[j]=1 then A[j1W[i]]:=1.
7. return A[n].

You can easily prove that the returned value is 1 if and only if a subset of the weights adds up to exactly n. The proof is analogous to the one of the original O(mn)-space algorithm. The following routine implements the above algorithm in C++. It just shifts a bit map m times by W[j] bits and applies a bitwise OR operation with the bit map from the previous step.

```
int SubsetSum(int W[], int m, int n)
{
bit_vector x=1;
for(i=1; i<=m; i++) x |=x<<W[i];
```

```
return (x>>n) &1;
}
```

The bit_vector class overloads bitwise operators and behaves as an (n+1) bits integer (with bits ranging from 0 to n). Now, consider a low-density subset-sum problem, the case in which the above algorithms produce a bunch of zeros and only a few ones in the bit array. You use a dynamically growing linked list and waste no space for "empty" elements:

SubsetSumLD(W, m, n)

1. Define, a linked list with only one element with value 0 and with the Head being equal to the Tail.
2. for i:=1 to m do.
3. for Element :=Head to Tail do.
4. if Element.value+W[i]≤ n.
5. Insert(Element.value+W[i]).
6. if Head.value=n.
7. return 1.
8. else.
9. return 0.

The function Insert(value) inserts the value into the list in descending sorted order. The function does nothing if an element with the same value already exists. The disadvantage of the subset-sum algorithm is that it solves only a decision—a yes-or-no problem—and doesn't allow restoring the partition itself. To overcome this disadvantage, you can use an array of integers instead of an array of bits and store the number of ones in the corresponding element. This solution requires O(n log(m)) space, and the array represents the sum of the rows of the table T[ij] of the original O(mn)-space algorithm.□

TABLE 1–SUBSET-SUM ARRAY

i/j	0	1	2	3	4	5	6	7	8	9	10	11	12	13
W[1]=1	T	T												
W[2]=9	T	T								T	T			
W[3]=5	T	T				T	T			T	T			
W[4]=3	T	T		T	T	T	T		T	T	T		T	T
W[5]=8	T	T		T	T	T	T		T	T	T	T	T	T

Reference

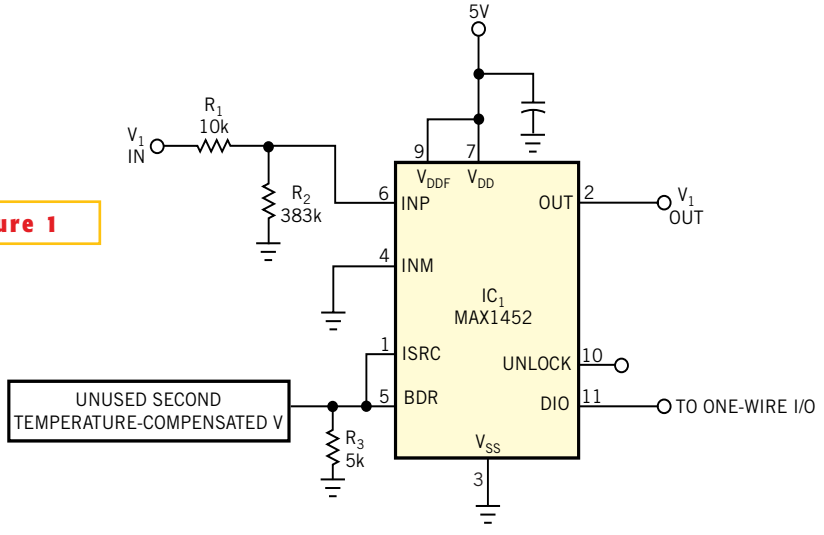
1. Garey, Michael R and Johnson, David S, *A Guide to the Theory of NP Completeness*, Freeman, San Francisco, CA, 1979.

IC removes nonlinear temperature effects

Kevin Schemansky, Maxim Integrated Products, Howell, MI

A common technique for removing nonlinear temperature-related effects from a dc voltage is to incorporate a temperature sensor that a microprocessor samples via an A/D converter. The processor determines—by mathematical calculation or a temperature-indexed look-up table—the amount of adjustment is necessary at a given temperature and delivers the resulting value via a D/A converter. Though effective, that approach incurs design effort, cost, and multiple ICs. An alternative technique uses a single IC in an unorthodox fashion (**Figure 1**). The chip, intended as a low-cost interface to a Wheatstone bridge, normally provides precision analog-signal processing along with digitally programmable compensation of gain, offset, and temperature effects. Much of its capability remains unused in this application, but its size and pre-engineered internal circuitry can readily add nonlinear temperature compensation to a design.

Figure 1



IC$_1$ introduces nonlinear temperature compensation to the analog voltage, V$_1$.

IC$_1$ contains a bandgap temperature sensor whose output is digitized by an 8-bit A/D converter, producing a digital representation of die temperature with 1.45°/bit resolution. An internal 768-byte EEPROM, read/write accessible via the one-wire asynchronous DIO pin, provides the user with two independent temperature-indexed look-up tables. (This design uses only one.) For the table in use, an 8-bit temperature register indexes which of 176 16-bit stored values is applied to an internal 16-bit D/A converter. Because the temperature-indexing boundaries of −69 to +184°C are outside the IC's operating range of −40 to +125°C, the IC can compensate for brief temperature excursions outside its normal operating range.

The **Figure 1** circuit removes temperature-variable nonlinear offsets from the analog voltage, V$_1$IN. First, you program IC$_1$ for its minimum gain, 39V/V, so the

R_1/R_2 attenuation provides an overall gain of unity. (The internal PGA provides a gain range of 39 to 264V/V.) Next, program the internal coarse-offset DAC with 0000 binary and the offset-TC DAC with 0000hex, to ensure that they have no effect on the V_1 input voltage. To generate a compensated output (Pin 2), the output stage adds in the temperature-indexed value of a third DAC (the offset DAC), whose 16-bit resolution achieves adjustments as fine as 74 µV. After calculating coefficients for the offset DAC, you program them into the IC via the DIO pin. The equation for output voltage is $V_1OUT=39(V_1IN/39)+V_{DD}$(offset-DAC value/65,536)(offset-DAC sign).□

Motor controller uses fleapower

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

A simple, permanent-magnet dc motor is an essential element in a variety of products, such as toys, servo mechanisms, valve actuators, robots, and automotive electronics. In many of these applications, the motor must rotate in a given direction until the mechanism reaches the end of travel, at which point the motor must automatically stop. Although you can use microswitches to stop the motor at the end of travel, their size, weight, and cost can be prohibitive, particularly in low-cost, portable items. The circuit in **Figure 1** implements a low-cost, micropower, latching motor controller that uses current sensing rather than switches to stop the motor. The design is optimized for a supply voltage of 3 to 9V, making it well-suited to battery-powered applications. To understand how the circuit works, assume that cross-coupled flip-flops IC_{1A} and IC_{1B} are both in a reset state, such that the D input of each one is high. Because both Q outputs are low, the H-bridge transistors, Q_1 to Q_4, are all off, and the motor is idle.

A momentary closure of the Forward switch latches the Q output of IC_{1A} high and turns on MOSFET Q_2. This action, in turn, provides bias for Q_3, causing the motor to run in the forward direction. The circuit is now latched, and, because IC_{1B}'s D input is now low, any closure of the Reverse pushbutton has no effect on the H-bridge, and the motor continues running in the clockwise direction. IC_2 contains a comparator and a bandgap reference-voltage (nominally 1.182V) output at the Reference terminal (Pin 6). The motor's armature current generates a sense voltage, V_{SENSE}, across current-sense resistor R_{SENSE}. The comparator compares V_{SENSE} at the IN+ input to a reference voltage, which R_5 and R_6 set, at the IN− pin. Under normal running conditions, V_{SENSE} is lower than the voltage at the IN− input, and the comparator's output at Pin 8 is low. However, when the mechanism hits an end stop at the limit of travel, the motor's armature current increases rapidly, causing a corresponding rise in V_{SENSE}. The comparator detects this increase, and the comparator's output goes high, thus resetting

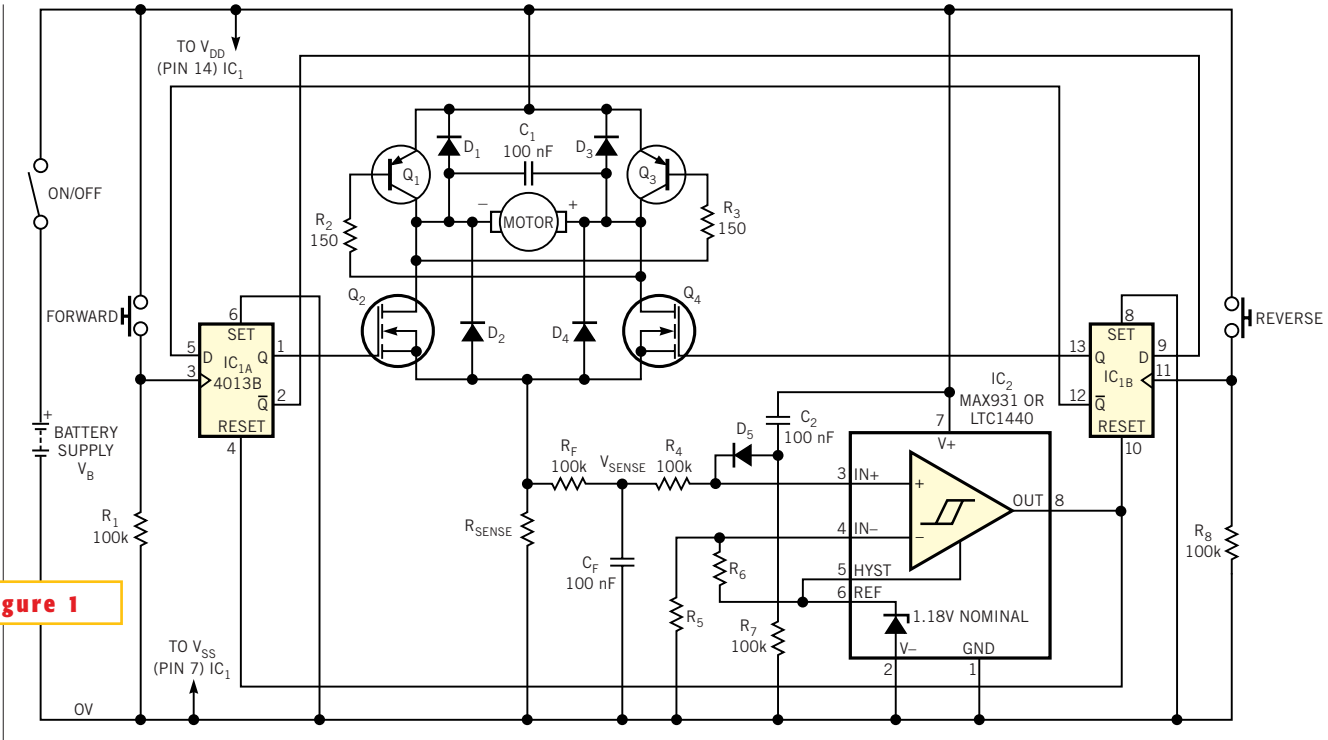
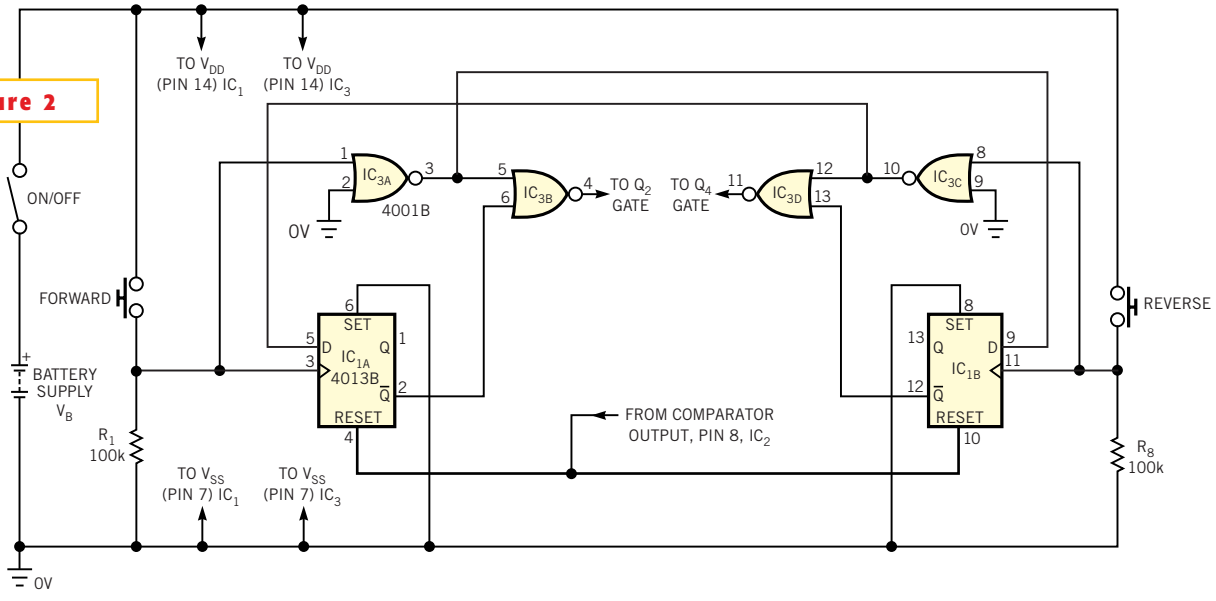


Figure 1

This latching motor controller uses current sensing, rather than switches, to stop the motor.

Figure 2



This addition to the circuit in Figure 1 yields a nonlatching controller, in which the motor runs only when the associated switch is closed.

flip-flop IC_{1A}. Transistors Q_2 and Q_3 now turn off, and the motor stops running.

Because IC_{1B}'s D input is now high, closing the Reverse switch latches IC_{1B}'s Q output high. This action turns on Q_4 and Q_1 in the opposite arm of the H-bridge, such that the motor now runs in the counterclockwise, reverse direction. IC_{1A}'s D input is now low, thereby disabling the Forward pushbutton, and the motor continues to run in the reverse direction until the mechanism hits the opposite end stop. Once again, the comparator detects the increase in armature current, and the comparator resets IC_{1B} and turns off the motor. The motor's cutoff threshold is a function of R_{SENSE}, R_5, and R_6, and the bandgap voltage at the REF pin. R_{SENSE} should be in the region of a few ohms to ensure that V_{SENSE} is also small when the motor is running under normal loading conditions. Keeping V_{SENSE} low makes practically all of the supply voltage available to the motor and ensures that the gate-source voltage of Q_2 and Q_4 is as large as possible. You should choose values greater than 300 kΩ for R_5 and R_6 to minimize the loading on the REF pin. In noisy environments, it may be necessary to decouple the IN− pin.

Filter components R_F and C_F serve a dual purpose. They are necessary to smooth the relatively "lumpy" voltage appearing across R_{SENSE} and are also essential to prevent the motor's in-rush current at turn-on from tripping the comparator. Values of 100 kΩ and 100 nF should be adequate, but some experimentation may be necessary to determine the best time constant for your application. Reset components C_2, D_5, and R_7 ensure that the comparator's output is high at power-up. You should select all transistors in the H-bridge to produce minimal saturation voltage when the devices conduct the maximum motor current. Choose low-$V_{CE(SAT)}$ devices for Q_1 and Q_3, and make sure that MOSFETs Q_2 and Q_4 can receive full enhancement at the minimum operating voltage. Depending on the type of MOSFETs you use, you may need to add a resistor in series with each gate to prevent spurious oscillation.

You should select resistors R_2 and R_3 to provide adequate base drive for Q_1 and Q_3 at the lowest supply voltage. Depending on the application, it may be possible to replace Q_1 and Q_3 with p-channel MOSFETs, in which case R_2 and R_3 can be fairly large. Freewheeling diodes D_1 to D_4 are necessary to commutate the currents generated by the motor's back-EMF at turn-off. You may require capacitor C_1 to suppress any noise that the motor's brushes produce. The circuit's quiescent, motor-idle current drain is extremely low, making it ideally suited to battery-powered applications. Measurements on a breadboard circuit operating from a 9V supply voltage reveal a quiescent current of just 9.5 µA. You can adapt the circuit to produce a nonlatching version in which the motor runs in the forward or the reverse direction only while the associated switch is closed. However, this approach is not simply a matter of gating the comparator's output with each switch; that action merely causes the motor to hiccup at the cutoff point. Instead, you must again latch the comparator's output and add some extra logic in the form of a quad NOR gate. **Figure 2** shows the arrangement, in which NOR gates IC_{3B} and IC_{3D} control the H-bridge, and the comparator controls the flip-flop's reset pins as in **Figure 1**.

The motor runs in the forward direction only while you depress the Forward button; releasing the pushbutton stops the motor. While the switch is closed, IC_{3A} holds IC_{1B}'s D input low, thereby ensuring that the Reverse switch can have no effect on the motor while the Forward switch is closed. Once you release the Forward switch, you can use the Reverse switch to reverse the motor's rotation. Again, the motor runs only while you depress the pushbutton. You can see from the symmetry of the circuit that closing the Reverse switch locks out any operation of the Forward switch. When the mechanism hits an end stop in either direction, the comparator resets the relevant flip-flop and shuts off the motor.□

design ideas

Edited by Bill Travis

DDS circuit generates precise PWM waveforms

Colm Slattery, Analog Devices, Limerick, Ireland

Pulse-width modulation is a simple way to modulate, or change, a square wave. In its basic form, the duty cycle of the square wave changes according to some input. The duty cycle is the ratio of high and low times in the square wave. A waveform with a 50% duty cycle would be high for 50% of the time and low for 50% of the time, and a waveform with a 10% duty cycle would be high for 10% and low for 90%. Many applications exist for PWM, including motor control, servo control, light dimming, switching power supplies, and even some audio amplifiers. In applications such as MEMS (micro-electromechanical-system) mirror-actuator control, a feedback system needs to regulate the PWM. A circuit monitors and controls the PWM output and varies the duty cycle according to the requirements of the application. The output frequency tunes the actuator, and the duty cycle sets the actuator's speed. The feedback loop controls the threshold level. This Design Idea describes a high-frequency, high-resolution PWM with feedback control. First, it might be useful to discuss some PWM theory.

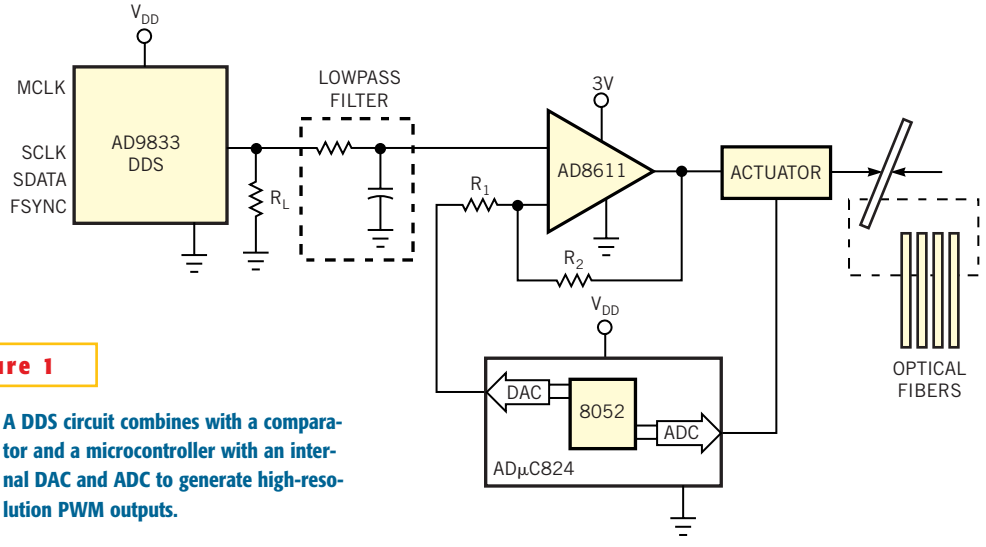


Figure 1

A DDS circuit combines with a comparator and a microcontroller with an internal DAC and ADC to generate high-resolution PWM outputs.

ALTERNATIVE ARCHITECTURES

Traditional PWMs use two op amps to generate a sawtooth waveform, a potentiometer to generate a dc reference, and a comparator to generate the PWM output. The advantage of this type of design is that the circuit is practical and inexpensive. Unfortunately, you cannot easily program the frequency without changing component values, and fine-frequency tuning is difficult. Another problem with this method is that accurate control of the duty cycle is difficult. You could use a digital potentiometer in place of the mechanical one, but this replacement results in a more costly design. A second method for generating PWM waveforms uses an ADμC824 MicroConverter. In addition to providing two PWM outputs, it also integrates ADCs, DACs, an 8052-compatible microcontroller, and flash memory. You can configure the PWM with resolution as high as 16 bits. However, the programmed frequency affects the resolution of the PWM. The frequency and resolution of the PWM are as follows: $F_{PWM} = 16.777$ MHz/N, where N is the resolution in bits.

An internal PLL derives the 16.77-MHz reference clock from a 32-kHz crystal. This reference clock samples the output of the PWM. As stated, N, the number of bits, is the resolution of the PWM. For 16-bit resolution the maximum frequency is 266 Hz. The resolution at 200 kHz drops to approximately 6 bits. Thus, the ADμC832 is the ideal low-cost approach for low-frequency, high-resolution applications but not for a high-frequency, high-resolution application.

DDS IMPLEMENTATION

Applications requiring high-resolution frequency tuning and pulse-width-modulation tuning in real time can use a DDS (direct digital synthesizer) to provide a high-accuracy sawtooth waveform with fine-frequency resolution across a large bandwidth. You can then use this signal as the input to a comparator in either

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open- or closed-loop applications. **Figure 1** shows an easy method of generating programmable square waves with programmable duty cycles. The AD9833 DDS drives a programmable triangular wave into one input of the AD8611 comparator and controls the frequency of the output waveform. The feedback loop from the actuator controls the threshold level of the comparator. The AD8611 is a single 4-nsec comparator with a latch function and complementary output. The input signal from the DDS connects directly to the inverting input of the comparator. The output feeds back to the noninverting input through R_1 and R_2. The ratio of R_1 to R_1+R_2 establishes the width of the hysteresis window with V_{DAC} setting the center of the window or the average switching voltage. The output switches low when the input voltage is greater than V_{HI} and does not switch high again until the input voltage is lower than V_{LO}, as the following expressions show: $V_{HI}=(V^+-1.5\ V-V_{DAC})(R_1/(R_1+R_2))+V_{DAC}$, and $V_{LO}=V_{DAC}(R_2/(R_1+R_2))$, where V^+ is the positive supply voltage to the comparator and V_{DAC} is the level that the DAC sets. The AD8611 can accept a 100-MHz signal with 400-mV p-p levels and can also accept input signals in the tens of millivolts. The AD9833 can provide sinusoidal- and triangular-wave outputs using the DDS architecture. It includes a numerical-controlled oscillator employing a 28-bit phase accumulator, a sine ROM, and a 10-bit D/A converter on a single chip (**Figure 2**).

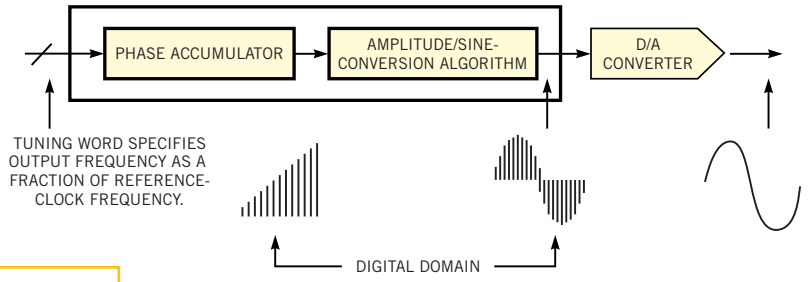


Figure 2

A DDS circuit includes a numerical-controlled oscillator employing a 28-bit phase accumulator, a sine ROM, and a 10-bit D/A converter on a single chip.

You typically think of sine waves in terms of their magnitude expression: $a(t)=\sin(vt)$. However, these waveforms are nonlinear and are difficult to generate. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit in time. Knowing that the phase of a sine wave is linear and given a reference interval (clock period), you can determine the phase rotation for that period:

$\text{Phases}=\omega dt;$

$\omega=\Delta\text{Phase}/dt;$

$f=(\Delta\text{Phase}\times f_{MCLK})/2\pi,$

where dt is the reciprocal of f_{MCLK}, the master clock. You can generate output frequencies using this formula, knowing the phase and master-clock frequency. The phase accumulator provides the 28-bit linear phase. The sine ROM stores the amplitude coefficients of the output sine wave in digital format. The DAC converts the sine wave to its analog domain. If you bypass the sine ROM, the part delivers triangular waveforms instead of sinusoidal waveforms. You program the device by writing to the frequency registers. The analog output from the part is then $f_{OUT}=(f_{MCLK}/228)\times(\text{frequency-register word})$.

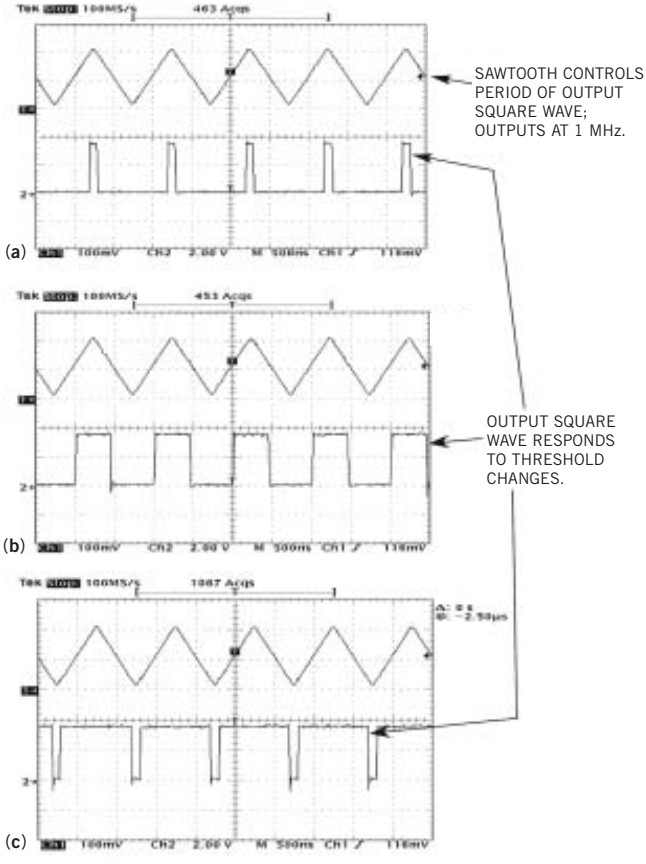


Figure 3

Applying different thresholds to the comparator in the circuit of Figure 1 has these effects.

The DDS outputs have 28-bit resolution, so effective frequency steps on the order of 0.1 Hz are possible to a maximum of approximately 10 MHz. Two phase registers provide 12-bit phase resolution. These registers phase-shift the signal by $P_{SHIFT}=(2\pi/4096)\times(\text{phase-register word})$. A 25-MHz crystal oscillator provides the master reference clock for the DDS. The output stage of the DDS is a voltage-output DAC with a typical swing of 0.7V p-p into an internal 200Ω resistor. Adding load resistor R_L reduces the peak-to-peak output voltage, thus allowing you to tune the peak-to-peak output of the DDS to the input range of the comparator. A filter stage generally appears on the output

of the DDS. The purpose of this stage is to filter feedthrough from the reference clock, images, and higher frequencies and to bandlimit the signals under consideration.

Figure 3 shows typical output plots from the AD8611 comparator in **Figure 1**. The input signal from the DDS is a triangle wave set to 1 MHz. Each plot shows the PWM output for various threshold voltages. In the closed-loop circuit of **Figure 1**, you can tune the output of the PWM to 12-bit accuracy. You have access to many possible ways of providing pulse-width modulation; the approach depends on the application. For low-resolution applications, traditional methods using op amps and potentiometers are acceptable and inexpensive. For low-frequency, high-resolution applications, the ADμC832 provides a one-chip approach with added features for free. For high-resolution, high-frequency applications requiring fine-frequency tuning, you can combine a DDS and a comparator to generate precise, high-frequency PWM waveforms.□

High-CMRR instrumentation amp works with low supply voltages

Dobromir Dobrev, Jet Electronics, Sofia, Bulgaria

Modern battery-cell voltages of 3 to 3.6V require circuits that offer efficient low-voltage operation. This Design Idea proposes an ac-coupled instrumentation-amplifier design that features high CMRR (common-mode-rejection ratio), wide dc input-voltage tolerance, and a first-order highpass characteristic. Most of these features stem from a high-gain first-stage design. The circuit uses popular-value and -tolerance components. **Figure 1a** shows the simplified amplifier circuit. The general principle is that the capacitor, C, and the R_3 resistors buffer and ac-couple the input signal. The second stage comprises two differential amplifiers, A_D. Each of them amplifies half the differential input signal. A summing operation yields the following expression for V_{OUT}:

$$V_{OUT} = A_D(V_A - V_B + V_C - V_D) = A_D\left(\frac{2sR_3C}{1+2sR_3C}\right).$$

In **Figure 1a**, V_A, V_B, V_C, and V_D are the two differential amplifiers' inputs, and A_D is the gain. The time constant $2R_3C$ defines the highpass cutoff frequency. **Figure 1b** shows the detailed circuit. The input stage comprises op amps A_1, A_2, A_3, and A_4. A_1 and A_2 are the main gain stages. Because their inverting and noninverting inputs are at the same potential, the input voltages supply the R_3 resistors. The buffers A_3 and A_4, along with the R_2 resistors, produce an amplification factor, $1+R_3/R_2$, for the current in R_3, because R_2 and R_3 connect to equal potentials. This circuit structure is the heart of the design. The voltage on capacitor C has no ac component, and A_1 and A_2 each amplifies one-half of the differential-input ac signal. C filters the input dc component, which appears at the A_3 and A_4 outputs. The second stage is a unity-gain, four-input adder-subtracter stage. It implements the above equation, where A_D is $1+R_1/(R_2||R_1)$. Assuming $R_3>>R_2$, $A_D=1+R_1/R_2$.

Another possible implementation for the second stage could use two differential-channel ADCs, producing a

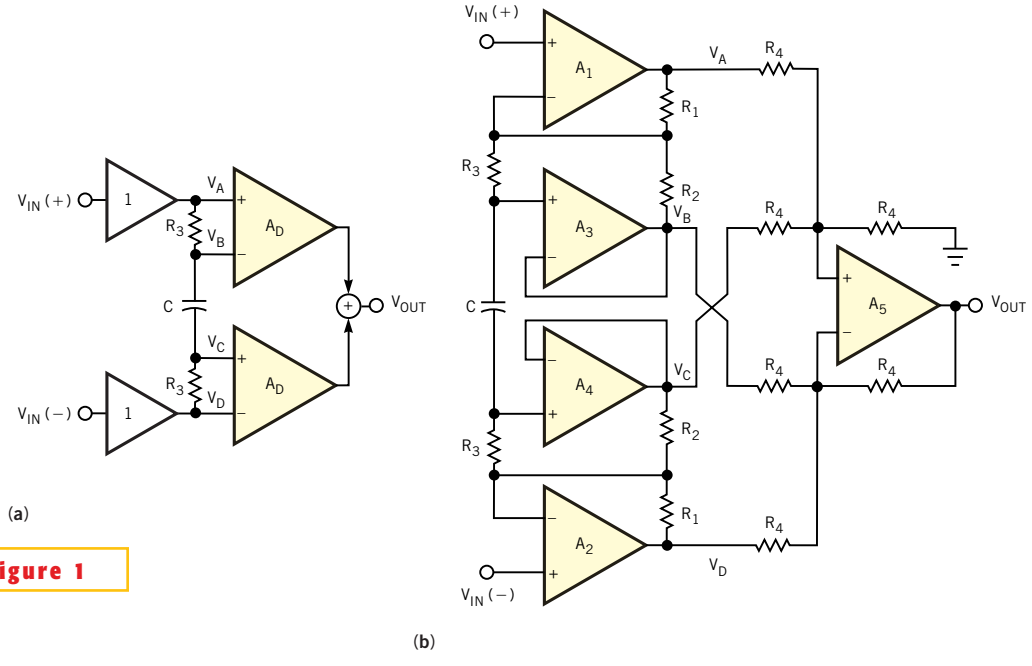


Figure 1

Capacitor C ac-decouples the simplified amplifier circuit (a); the detailed circuit (b) uses gain stages and an adder-subtracter stage.

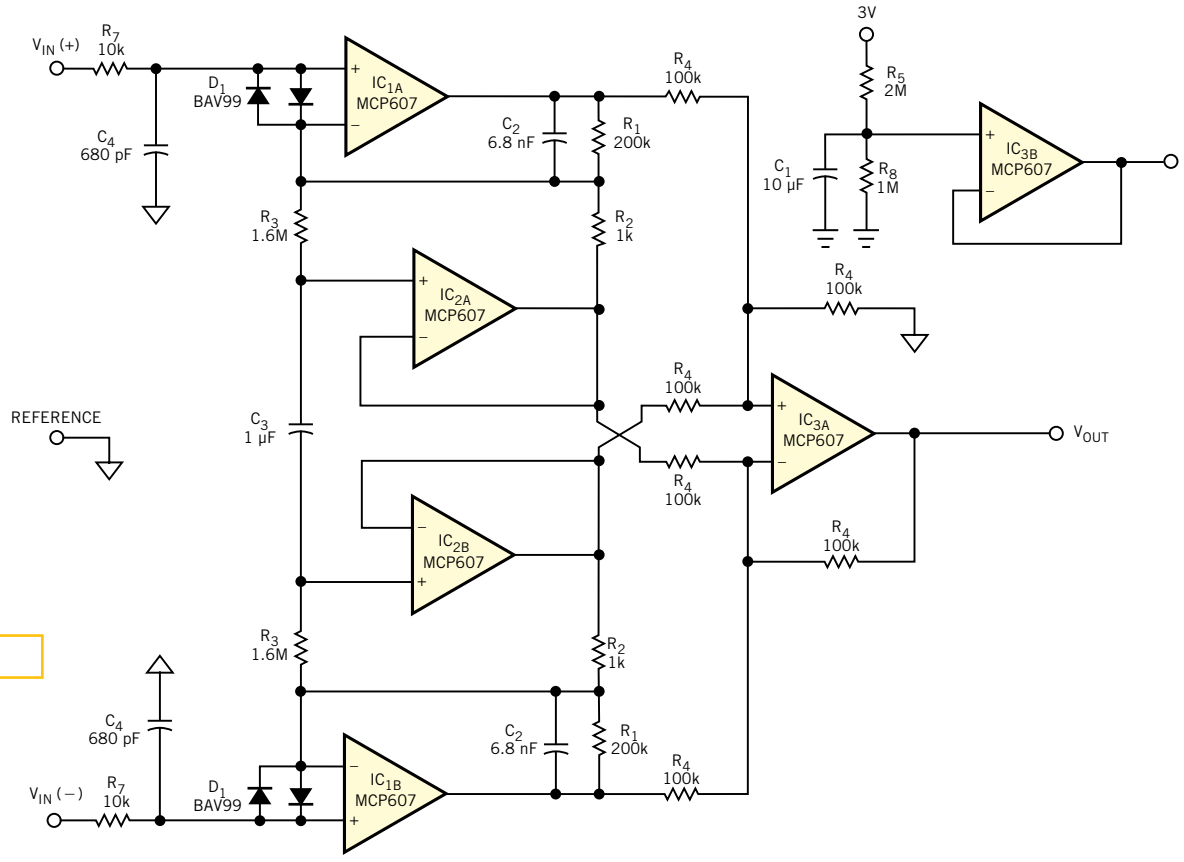


Figure 2

This high-CMRR instrumentation amplifier operates from extremely low supply voltages.

digitized V_{OUT}, ready for microcomputer processing. If a ±5V supply is available, it is possible to obtain V_{OUT} by using two difference amplifiers on one chip, such as the INA2134. You can calculate the minimum CMRR as:

$$\text{CMRR} = \frac{A_{D(1-4)}}{A_{CM(1-4)}} \times \frac{A_{D5}}{A_{CM5}} = \frac{A_D}{4\Delta/(1+R_4/2R_4)} = \frac{1.5A_D}{4\Delta},$$

where $A_{D(1-4)}$ is the differential gain of amplifiers A_1 through A_4, $A_{CM(1-4)}$ is the common-mode gain of these amplifiers, A_{D5} is the differential gain of amplifier A_5, and A_{CM5} is the common-mode gain of A_5. Δ is the tolerance of the R_4 resistors in the circuit. A very important parameter is the op amps' input offset voltage, especially for A_3 and A_4. The A_1 and A_2 offsets do not contribute to error, because they add to the input signal's dc component, which capacitor C cancels. The maximum output-voltage error attributable to op-amp offset voltage is:

$$V_{MAX} = \left(V_{IOA3MAX} + V_{IOA4MAX}\right)\left(1+\frac{R_1}{R_2}\right) + 3V_{IOA5MAX} \approx 2A_D V_{IOA34MAX},$$

where V_{IOMAX} are the maximum offset voltages of the corresponding op amps. In selecting op amps, you should note the following: A_3, A_4, and A_5 should be low-offset and high-CMRR types, and A_1 and A_2 should have high open-loop gain, CMRR, and gain-bandwidth products. **Figure 2** shows a practical amplifier circuit. The power supply is one 3V lithium battery. You can use several op-amp types, such as MCP607s or OPA2336s. Because of the input common-mode voltage range, you set the signal ground to one-third of the supply voltage. The D_1 diodes prevent the circuit from latching up. The R_7-C_4 networks provide RF-noise filtering at the inputs. You derive the network's values from the following consideration: With $R_7C_4 = (R_1||R_2||R_3)C_2 \sim R_2C_2$, the high-frequency zero in the amplifier's transfer function cancels:

$$A_D(s) = \frac{V_{OUT}}{V_{IN}(+) - V_{IN}-} = \frac{2sC_3R_3}{(1+sC_4R_4)(1+2sC_3R_3} \times \left(1+\frac{R_1}{R_2 \,||\, R_3}\right) \times \left(\frac{1+sC_2(R_1 \,||\, R_2 \,||\, R}{1+sC_2R_1}\right).$$

The circuit has the following advantages:

- The first stage ensures the overall gain, thus providing high CMRR without the use of high-precision resistors in the second stage.
- By connecting the low-frequency-determining RC network to the inverting inputs of the op-amp pair that amplifies the input signal, the circuit needs no additional input buffers.
- The circuit delivers a standard, first-order highpass characteristic, using passive components with popular values and tolerances.
- The differential-input range is as high as 2V, using a 3V supply.
- The circuit consumes low supply current and power: approximately 120 µA, 0.4 mW.□

Use a DAC to vary LVDT excitation

Anthony Di Tommaso and Ljubisa Milojevic, ABB Inc, Natrona Heights, PA

LVDTs (linear variable differential transformers) are electromechanical measuring devices that convert the position of a magnetic core into electrical signals. You generate these signals via excitation on the primary side. The results on the secondary side—typically, two secondary windings—depend on the position of the core (**Figure 1**). The excitation typically ranges in amplitude from 1 to 10V and in frequency from 1 to 10 kHz, depending on the type of LVDT you employ. Traditionally, for one circuit to provide such variability in frequency and amplitude, you can use either an LC tank with adjustable components or a sine-wave generator under microcontroller control. It can be difficult to achieve precision over time and temperature with the LC-tank circuit because of variations in passive components. You also must manually perform calibration. You can more easily obtain precision over time and temperature through the use of a microcontroller-controlled sine-wave-generator chip, and calibration can be automatic, but the method incurs a greater expense than the LC-tank circuit. The circuit in **Figure 2** presents an alternative.

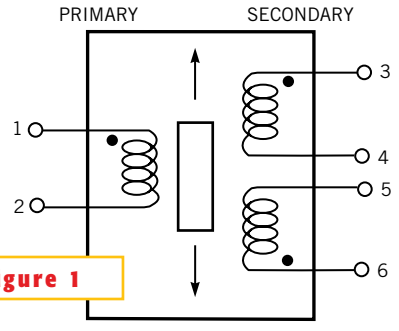


Figure 1

An LVDT is an electromechanical measuring device that converts the position of a magnetic core into electrical signals.

Rather than using a sinusoidal signal to excite the LVDT, a triangular wave comes from the integration of a square-wave output provided by a microcontroller timer. With the use of a current-output DAC, such as the AD7564 from Analog Devices (www.analog.com), you can create a circuit that provides an alternative at a lower cost than that of a sine-wave-generator chip and with greater ease of modification than with an LC-tank circuit. Beginning with the microcontroller, the frequency of the excitation wave depends on the configuration of the microcontroller's timer. You can configure a free-running timer, for example, to toggle the output based on the comparison match of a preset count. You base the count on the desired frequency output and the timer's internal clock rate. You then adjust the output of the microcontroller's timer to remove offset. You need to eliminate as much offset in the signal as possible because such offset adversely affects the transformation process. You can use an op amp to remove the offset because the offset is constant—in this case, half the voltage that powers the microcontroller. In general, you should choose an op amp with low offset and low bias, not only for the difference stage, but also later.

Once you center it about common, the signal becomes a triangular wave. The integrator you use is basically a single-pole, lowpass filter with a configurable (via the DAC) corner frequency. The corner frequency you choose guarantees that integration of the excitation signal occurs. To accommodate variability in frequency and amplitude, the DAC provides an easy interface. With two channels of the AD7564, the circuit can emulate variable resistors for the feed-forward and the feedback of the integrating op amp. (The other two channels could serve for the demodulation gain of each LVDT secondary.) You can use these "resistors" to form the corner frequency for the "lossy" integrator and to establish the gain through the circuit, ensuring that the signal is integrated and that the amplitude of the excitation signal is appropriate for the LVDT.

You need to make several calculations in advance to determine the configura-

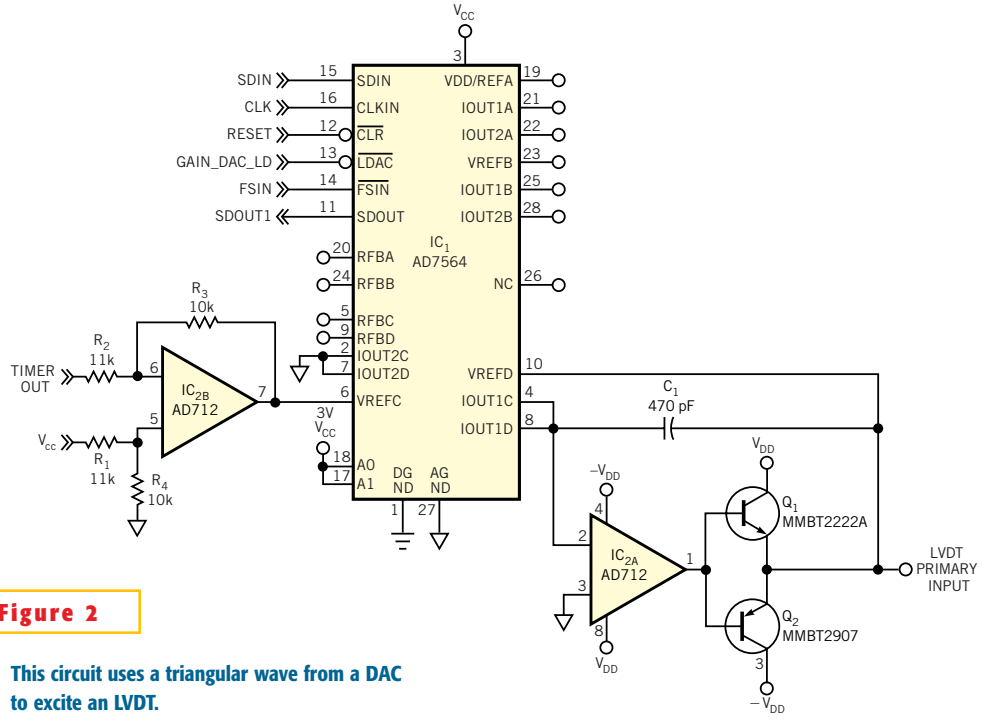


Figure 2

This circuit uses a triangular wave from a DAC to excite an LVDT.

tion of the DAC and the establishment of the resistances. According to the data sheet, the resistance of the R-2R ladder in the Analog Devices AD7564 DAC is typically 9.5 kΩ. You can calculate the feedback resistance using the following formula: $R_{FB}=1/(2\pi f_D C)$, where f_D is the desired corner frequency of the integrator and C is the value of the capacitor you use. You can then assemble the data word for that effective resistance accordingly: $N_{FB}=(4096\times 9500)/R_{FB}$, where N_{FB} is the digital word loaded into the DAC. The feed-forward resistance of the integrator circuit is then $R_I=R_{FB}/(\text{gain factor})$, where the gain factor depends on the desired output amplitude. The data word for that effective resistance becomes $N_I=(R_{FB}/R_I)N_{FB}$ or $N_I=(\text{gain factor})\times N_{FB}$. In most cases, you may need to use additional drive current from the output of the "lossy" integrator to drive the primary coil of the LVDT. This approach may entail the addition of transistors and other components.

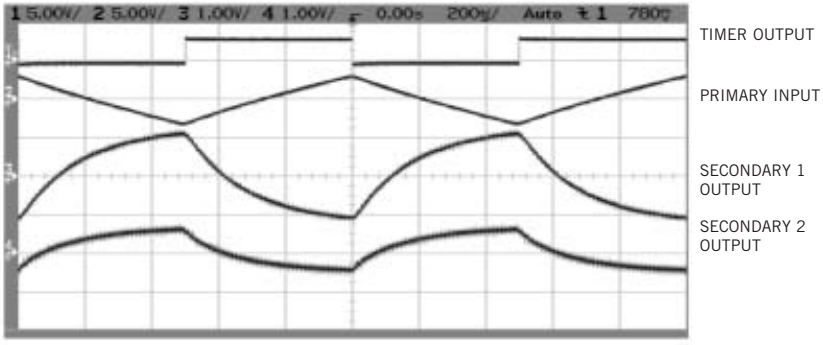


Figure 3 Although what appears on the secondary side differs from the excitation signal, it is sufficient because of the inherent filtering properties of the LVDT.

You have some flexibility in the type of excitation signal the circuit uses because it is common practice to calibrate an LVDT. **Figure 3** illustrates the output of the excitation circuit and the results on the secondary side of the LVDT. Although what appears on the secondary side differs from the excitation signal, it is sufficient because of the inherent filtering properties of the LVDT. The output of each secondary side generally transforms into a constant root-mean-square or mean-absolute-deviation value. In the situation of two secondary coils, a comparison between those values occurs. As long as you excite both coils in the same manner—which is guaranteed because only one primary coil exists—and the output signal is of sufficient resolution, then a triangular wave can excite such an LVDT.□

design ideas

Edited by Bill Travis

High-fidelity triangle-wave generator consumes only 6 µA

Glen Brisebois, Linear Technology Corp, Milpitas, CA

IDEAL TRIANGLE WAVES involve infinite d^2V/dt^2, so high-fidelity triangle waves entail very high bandwidths. Micropower circuits have fairly low bandwidth, so generating good triangle waves with such circuitry becomes problematic. The circuits of **Figure 1** show two methods of generating triangle waves. The solitary-comparator circuit uses a relaxation-oscillator approach with the triangle approximation assuming an RC (exponential) nature (**Figure 1a**). When you need better linearity, adding an integrator improves the triangle approximation (**Figure 1b**). Both circuits include a hysteretic-feedback path, as well as an RC or integrator feedback path comprising R_3 and C_1. The hysteretic-feedback path keeps changing the direction of the RC integrator and setting the new target voltage, and the RC integrator sets the rate of change toward the new target. These circuits are robust and find wide usage.

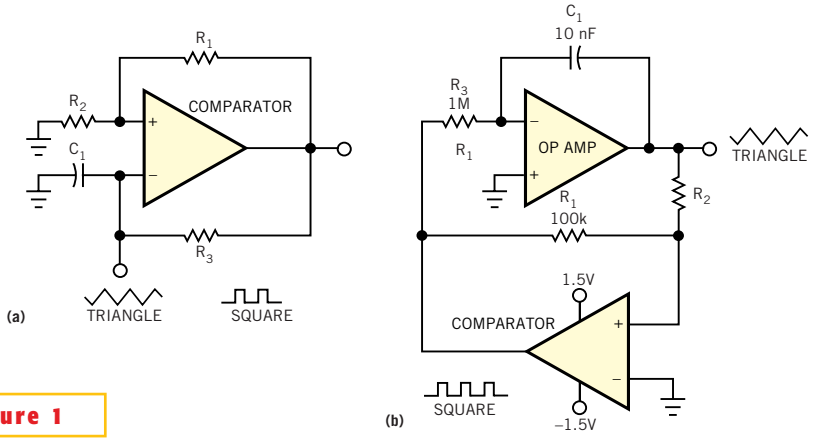
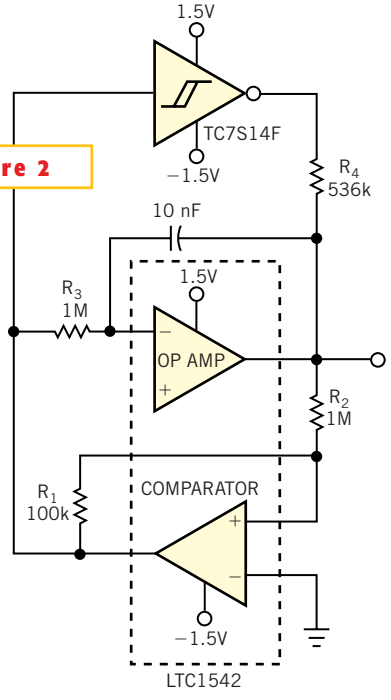


Figure 1

These popular methods of generating triangle waves have drawbacks, especially when your design requires low-power operation.

The problem arises when you simultaneously require ultralow power consumption and relatively high-frequency operation. This scenario makes phenomenal demands on the micropower op amp. Consider that, every time the comparator reverses direction, it slams an instantaneous current into or out of the op amp's output through the two feedback paths. This situation would be acceptable, except that the amount of current it slams is greater than the op amp's total supply current. The result is a disastrous-looking waveform with enormous glitches stemming from the fact that the op amp cannot provide the instantaneous output-switch current demands. You can gain some improvement by increasing the resistor values and reducing the capacitor values. However, the improvements are only incremental, and the circuit becomes noisier and more susceptible to interference.

Figure 2



A simple CMOS inverter provides high-bandwidth current assist, improving the waveform drastically with minimal impact on supply current.

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But take heart; a simple and inexpensive solution is at hand. Why not let a CMOS inverter provide the instantaneous current and let the op amp simply provide the precision linearizing current? **Figure 2** shows the method. The circuit is identical to that of **Figure 1b**, except that the op amp need not provide the instantaneous switch current. Instead of the drastic change in output-current polarity at the triangle peaks, the op amp's output current slowly crosses zero at midsupply. In the improved waveform, the total supply current at 280-Hz operating frequency is 6.2 µA.□

High-current driver serves home-power-line modems

Ryan Metivier, Analog Devices, Wilmington, MA

HOME-BASED power-line networking signals are similar to xDSL (digital-subscriber-line) signals in that they both typically employ a form of OFDM (orthogonal frequency-division multiplexing). Both applications require high output current, wide bandwidth, and good linearity. This Design Idea describes a simple line-driver circuit, designed with an xDSL driver, to drive high-speed data over a home power line. **Figure 1** shows the AD8391 current-feedback amplifier connected in a negative-feedback circuit to drive wideband, discrete multitone-based signals through home power lines. The advantage of current feedback is that it allows you the flexibility of increasing the gain beyond unity without being limited by the gain-bandwidth product. The AD8391 has 60-MHz bandwidth, 600V/µsec slew rate and 250-mA output-drive-current capability, making it ideal for driving home power lines.

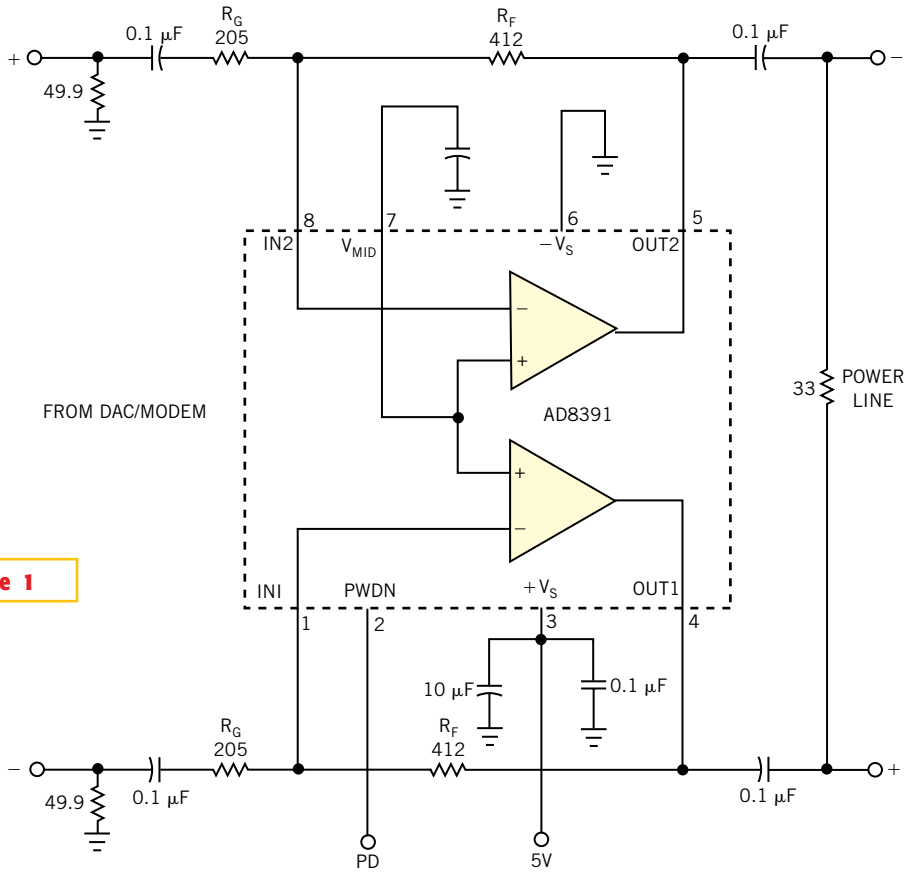


Figure 1

An xDSL driver uses current-feedback technology to make an efficient home-power-line driver.

The circuit in **Figure 1** operates with a 5V supply, has a voltage gain of $-2(-R_F/R_G)$, and drives a 33Ω load. The 33Ω load emulates the worst-case impedance of a home power-line network, which can vary greatly from home to home. The driver is transformer-coupled to the power line. The amplitude of the output signal is 2.8V p-p into the differential power line (hot and neutral) with a peak-to-average ratio of 4V/V. The feedback resistor, R_F, and the gain resistor, R_G, maximize circuit bandwidth and stability. For this circuit, an acceptable bandwidth is approximately 30 MHz. The following **equation** shows the relationship between closed-loop bandwidth (f_{CL}), R_G, and R_F for current-feedback amplifiers.

$$f_{CL} = \frac{1}{2\pi C_P R_F\left(1+\frac{R_{IN-}}{R_F}+\frac{R_{IN-}}{R_G}\right)}.$$

C_P, the internal capacitance, sets the corner frequency of the open-loop transimpedance function, and R_{IN} is the input impedance of the inverting terminal of each amplifier. (**Figure 1** does not

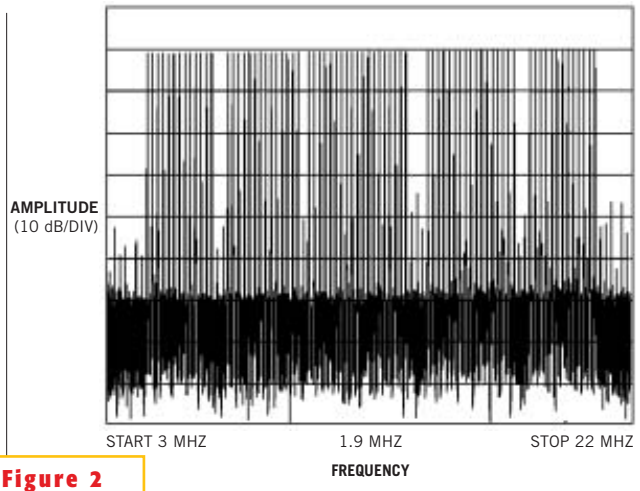


Figure 2

The output spectrum of the power-line driver in Figure 1 shows that the worst-case empty-tone distortion is −35 dBc.

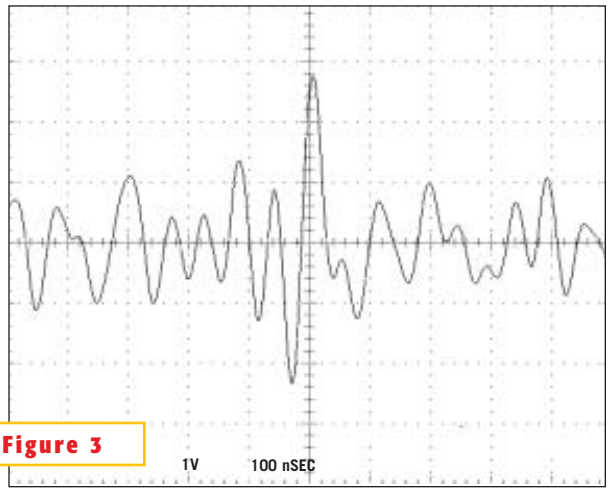


Figure 3

This plot represents the time-domain characteristic of the power-line driver.

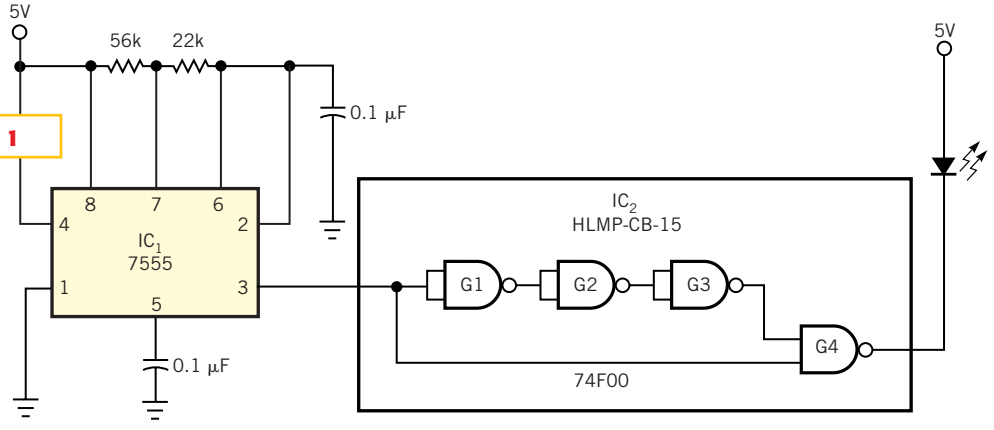
show C_P and R_{IN}.) It is important to note that R_F dominates the expression, thus controlling the closed-loop bandwidth. The 49.9Ω resistors on the inputs of the circuit terminate the signal source. You should adjust these values based on each application. The four 0.1-µF capacitors provide ac coupling on the input and output lines. The test signal is a composite waveform constructed from the sum of 75 sinusoids of pseudorandom phase. Each tone in the test waveform may have one of four phases to emulate QPSK (quadrature phase-shift keying). The sinusoids are orthogonally spaced from 4 to 21 MHz, leaving the amateur-radio bands empty. **Figure 2** shows that the worst-case empty-tone distortion is −35 dBc. This figure is adequate for most practical power-line applications. **Figure 3** shows the output in the time domain.□

Circuit forms fast, portable light pulser

SK Kaul and IK Kaul, Bhabha Atomic Research Centre, Trombay, Mumbai, India

THE ABSENCE of a fast one-shot multivibrator in the entire TTL family, as well as the low-voltage swing and unwieldy supply requirements of ECL, drove us to exploit the fast transition times and low propagation delays of F-series gates. The application called for the implementation of a compact, portable, fast light pulser for field testing fast photomultipliers in gamma-ray astronomy work. The use of only two ICs helped to minimize the size and power consumption (**Figure 1**). The normally high pulses at the output gate, G4, in IC_2 have rise and fall times of approximately 2.5 nsec and a duration of less than 10 nsec, corresponding to three gate delays. These pulses are ideally suited to pull low the cathode of a fast, blue HLMP-CB-15-type LED with the anode clamped at 5V. The gate forces almost the entire 5V supply voltage across the LED. This high swing ensures optimum brightness of the LED, which is soldered to the edge of a small pc-board strip. Rechargeable batteries are clamped onto the other side of the pc board. Using a CMOS version of the timer, IC_1, the circuit has a current drain of less than 4 mA.□

Figure 1



This circuit provides fast light pulses in a blue LED.

3V supply delivers 12V p-p to piezo speaker

Royce Higashi and Tony Doy, Maxim Integrated Products, Sunnyvale, CA

Low-profile piezoelectric speakers can provide quality sound for portable electronic devices, but they require voltage swings greater than 8V p-p across the speaker element. Yet, most portable devices include only a low-voltage power source, and conventional amplifiers operating from batteries cannot provide enough voltage swing to drive a piezoelectric speaker. One approach to this problem is to use IC_1 in **Figure 1**, which you can configure to drive a piezoelectric speaker with as much as 12V p-p and operate from a single 3V supply. IC_1, a MAX4410, combines a stereo-headphone driver with an inverting charge pump that derives a negative −3V supply from the positive 3V supply. Thus, providing the drive amplifiers with an internal ±3V supply allows each output of IC_1 to swing 6V p-p. Configuring IC_1 as a BTL (bridge-tied load) driver again doubles the maximum swing at the load to 12V p-p. In the BTL configuration, IC_1's right channel serves as the master amplifier. It sets the gain of the device, drives one side of the speaker, and provides a signal to the left channel. If you configure IC_1 as a unity-gain follower, the left channel inverts the output of the right channel and drives the other leg of the speaker. To ensure low distortion and good matching, you should set the left-channel gain using precision resistors.

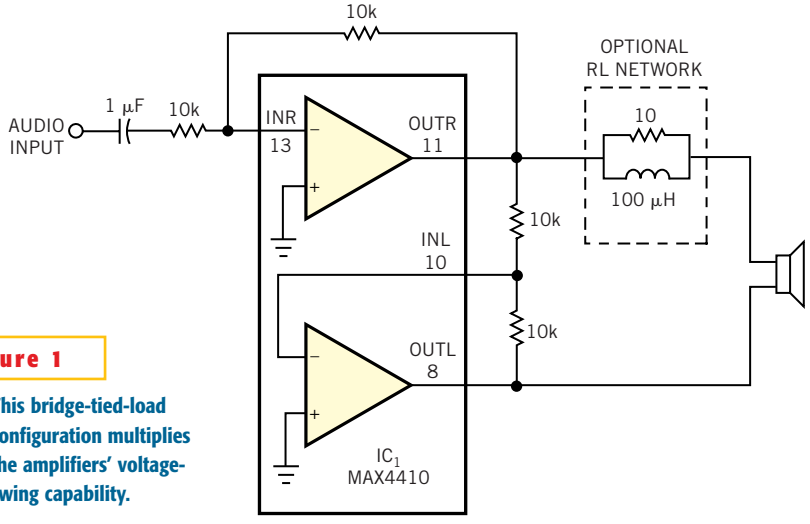


Figure 1 This bridge-tied-load configuration multiplies the amplifiers' voltage-swing capability.

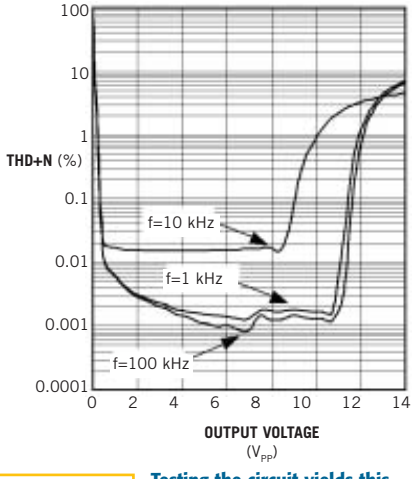


Figure 2 Testing the circuit yields this THD+N versus output voltage for the Figure 1 circuit.

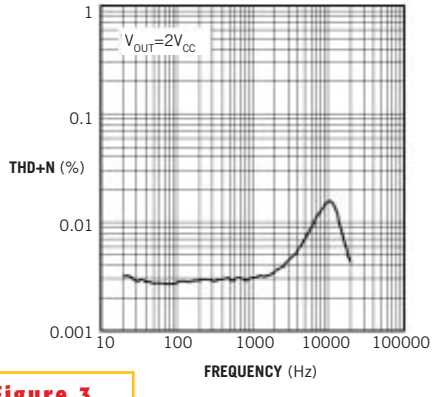


Figure 3 Testing the circuit yields this THD+N versus frequency for the Figure 1 circuit.

We tested the circuit with a Panasonic (www.panasonic.com) WM-R57A piezoelectric speaker, yielding the THD+N (total-harmonic-distortion-plus noise) curves (**figures 2** and **3**). Note that THD+N increases as frequency increases in both graphs. Because the speaker appears to the amplifier as a capacitor, the speaker's impedance decreases as frequency increases, resulting in a larger current draw from the amplifier. IC_1 remains stable with the speaker, but a speaker with different characteristics might cause instability (**Figure 4**),. In that case, you can isolate the speaker's capacitance from the amplifier by adding a simple inductor/resistor network in series with the speaker (within the dotted lines on **Figure 1**). The network maintains stability by maintaining a minimum high-frequency load of approximately 10Ω at the IC's output.□

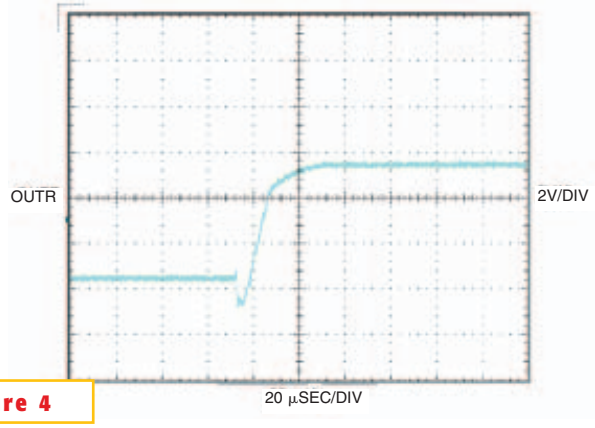


Figure 4 Step response at the OUTR output of IC_1 in Figure 1, which drives a WM-R57A piezoelectric speaker, shows that IC_1 remains stable with the speaker.

Code provides adjustable differential drive for robots

Alton Harkcom, EGO North America, Newnan, GA

Intelligently modifying the motor-drive commands to a robot can give you control finesse during competitions. Moving a joystick hard right, for example, might have different effects, depending on the robot's speed and direction. Software running on an inexpensive microcontroller (in this case, an NEC (www.nec.com) PD78F9814) manages this control by calculating separate drive and adjust vectors and then combining the vectors and calculating the appropriate power ratio for two tread motors (**Figure 1**). This demonstration system uses a simple treaded toy vehicle to show how the ratio-drive concept works and requires no sensors in the vehicle. The microcontroller controls the tread motors with simple forward/reverse signals based on the calculated motor speeds and directions.

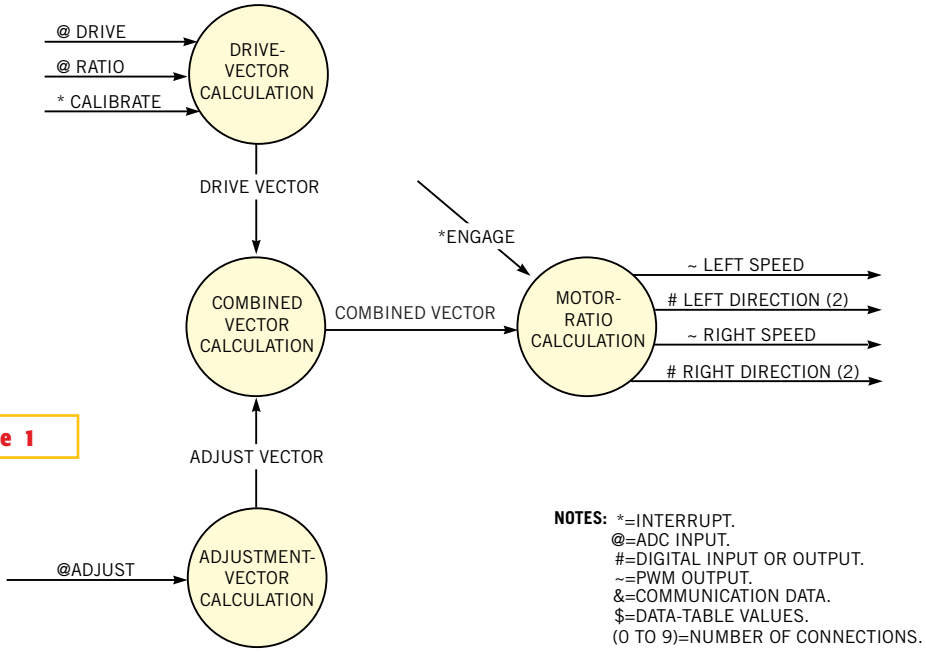


Figure 1

An NEC microcontroller calculates the appropriate power ratios for two tread motors in a robot.

Listing 1, which you can download from the Web version of this Design Idea at www.edn.com, shows the main routine for this application. It begins by initializing all the signals and then calibrating them with the joystick at the idle position (MID) and each extreme (LO and HI). The code uses several sets of variables. Drive variables (DriveRaw, DriveHI, DriveMID, DriveLO, and Drive) specify the combined drive speed for the motors. Ratio variables (RatioRaw, RatioHI, RatioMID, RatioLO, and Ratio) specify the ratio of right-to-left motor balance. Adjust variables (AdjustRaw, AdjustHI, AdjustLO, and Adjust) specify the adjustment value to the ratio value. The adjustment reduces the ratio value to better control left/right balance at particular speeds. Range-conversion variables (RangedUpper, RangedLower, and Ranged) rerange the ADC inputs to the desired 0 to 100% values for the motor speed and direction. After the code calculates the Left and Right motor vectors, another routine uses these vectors to drive the motors. If Right is greater than 1, for example, the drive routine enables a RightForward PWM signal and disables the reverse signal. For experimentation purposes, you can use a 1A quad half-H bridge to route the speed and direction signals to the motors. In actual competitions, you need a heavier duty motor controller because the motor-stall currents can exceed 1A.□

Microcontroller produces analog output

Abel Raynus, Armatron International, Melrose, MA

A brushless dc motor needs several voltage levels to control its speed: 0V to stop the motor, 5V to run it at maximum speed, and some voltages between these extremes to run it slower. When you use such a motor in a system under microcontroller supervision, the microcontroller should generate all these voltages. But a microcontroller is a digital device, and it usually has no analog output. Several methods are available to overcome this deficiency. For example, you could use a DAC, a digitally programmable potentiometer, or some analog switches connected to resistor dividers. However, when you need only a few intermediate voltage levels, it would be more attractive to find a method that uses microcontroller software. This Design Idea exploits the fact that you can program a microcontroller's I/O pins as either input or output. When you program a pin as output, you set its voltage level to high (5V) or low (0V). When you program a pin as input, it has

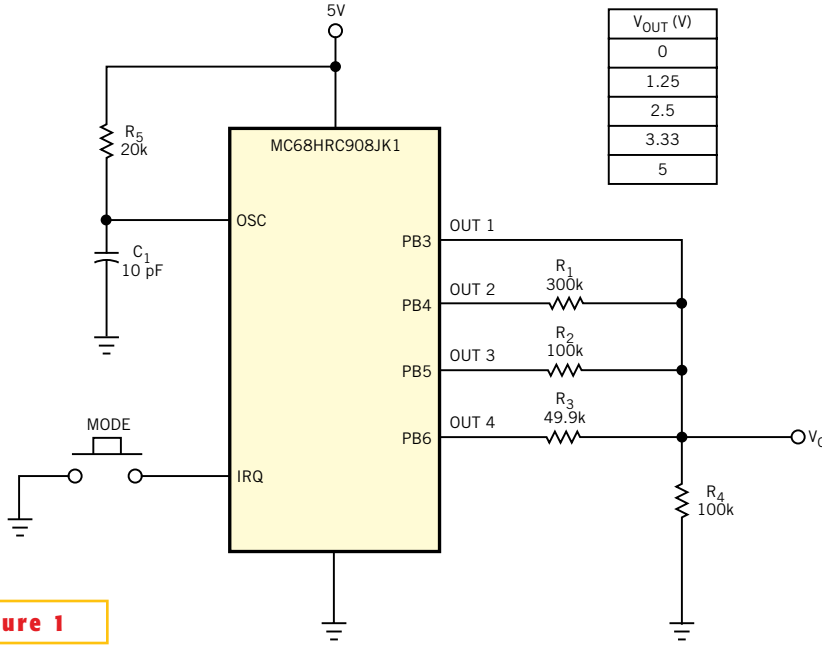


Figure 1

A microcontroller can generate analog outputs for motor-control purposes.

no effect on output voltage. **Figure 1** shows a circuit example.

The circuit needs no external components, except for a few resistors. You can set the output-voltage levels during the main program execution or by an external interrupt. For testing purposes, using an external interrupt is preferable (see **Listing 1** at www.edn.com). A pushbutton-mode switch triggers the external interrupt, the service routine of which consequently sets all the predetermined voltages. This design uses 0, 1.25, 2.5, 3.33, and 5V levels. Resistors R_1 to R_4 determine the intermediate levels. The circuit uses the inexpensive, 8-bit MC68HRC908JK1 flash microcontroller from Motorola (www.motorola.com), but this method applies to almost any kind of microcontroller. You can download the microcontroller software from the Web version of this Design Idea at www.ednmag.com.□

Single transistor provides short-circuit protection

Keith Szolusha, Linear Technology Corp, Milpitas, CA

In certain dc/dc-converter applications, on-chip, cycle-by-cycle current limit may be insufficient protection to prevent a failure during a short circuit. A nonsynchronous boost converter provides a direct path from the input to the short circuit through the inductor and the catch diode. Regardless of current-limit protection in the IC, when a short circuit exists in the load, extremely high currents that flow through the load path can damage the catch diode, the inductor, and the IC. In a SEPIC (single-ended, primary-inductance-converter) circuit, the coupling capacitor breaks this path. Thus, when a short circuit exists in the load, no direct path exists for current to flow from input to output. However, if the required minimum on-time is less than the application-specific duty cycle, the inductor and, thus, the switch current can rapidly increase, causing IC fail-

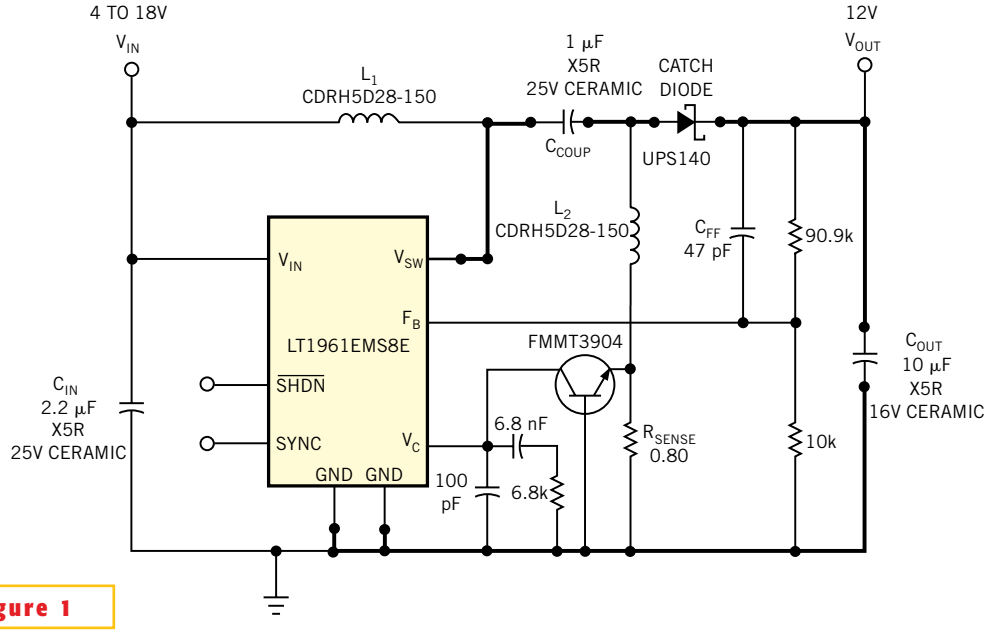


Figure 1

This 4 to 18V-input, 12V-output SEPIC has short-circuit protection.

ure, input-supply overload, or both. Even in certain buck-regulator applications, duty-cycle limitations sometimes keep the switch on too long to maintain control during an output short-circuit condition, especially at very high input voltage with extremely high-frequency ICs. A single-transistor approach protects the SEPIC circuit from short-circuit fault conditions by pulling down the V_C pin (the output of the error amplifier) when the inductor current starts to run away during an overload or short circuit in the load (**Figure 1**).

Pulling the V_C pin low forces the IC to stop switching, skipping minimum on-time switch cycles, and allowing the current in each inductor to ramp down. During a short circuit, the peak current in L_1, which decreases because of the limited number of switch cycles, and the peak current in L_2 sum up to equal the peak current in the switch, which is less than the 1.5A limit of the LT1961EMS8E. **Figure 2** shows the short-circuit input and output currents at different input voltages. **Figure 3** shows the maximum load current versus input voltage. The average current in L_2 is equal to the load current and is a maximum of 600 mA under all load conditions. If the sense resistor sees 800 mA, it knows that an overload condition has occurred and tells the transistor to protect the circuit.□

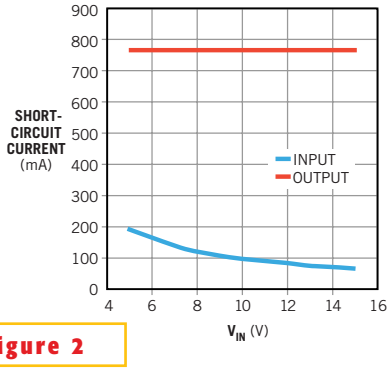


Figure 2

The short-circuit input and output current for the circuit of Figure 1 differ at different voltages.

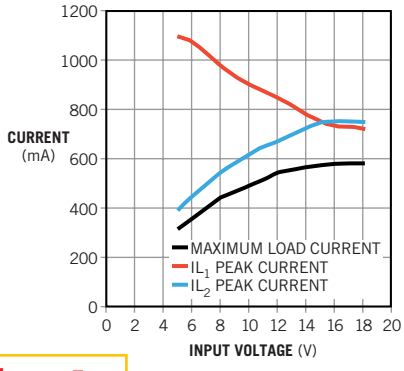


Figure 3

These curves show the maximum load current under normal load conditions.

design ideas

Edited by Bill Travis

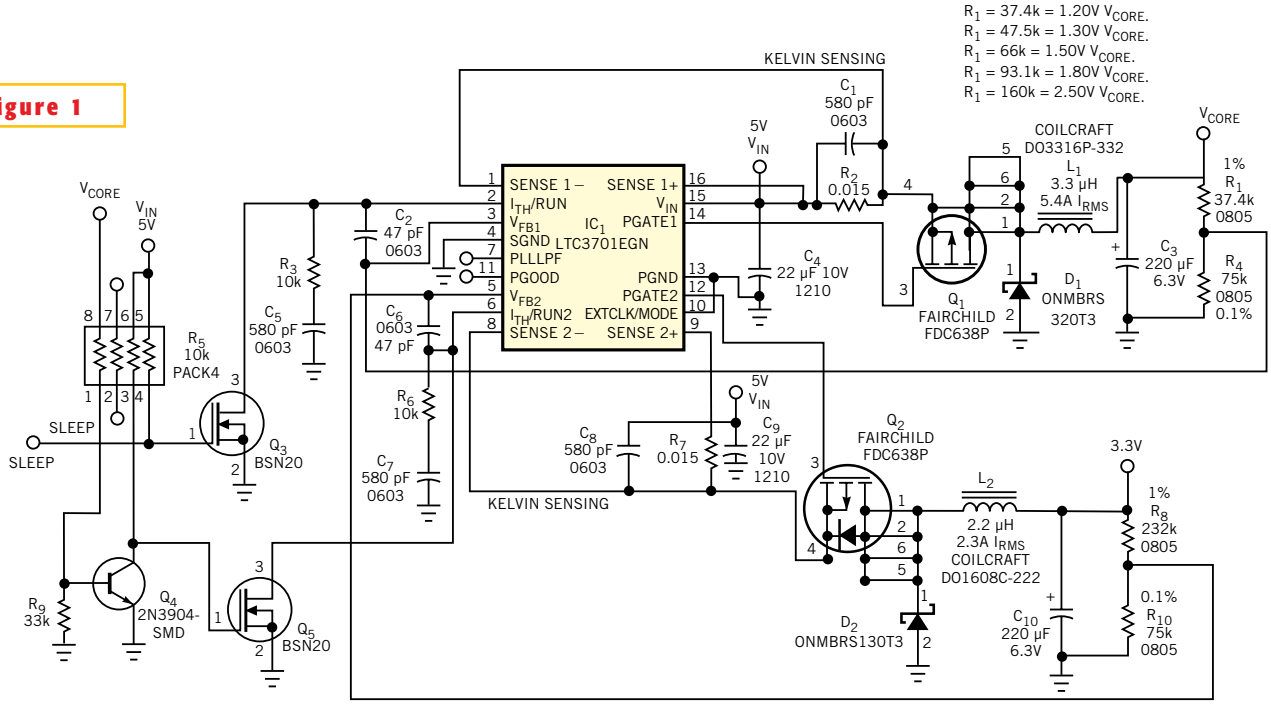
Scheme adds sequencing and shutdown control to regulator

Said Jackson, Equator Technologies Inc, Campbell, CA

Modern microprocessor- or FPGA-based circuits require separate and independent power-supply voltages for the core and the I/O circuits. Some devices require stringent control of the turn-on characteristics and sequencing of these multiple power supplies to avoid internal parasitic current flows and consequent latch-ups. Although regulators exist with specific soft-start and shutdown inputs, it may be more cost-effective to use regulators that do not inherently provide these features and to add these features with external discrete devices. This Design Idea shows how to use an inexpensive Linear Technology (www.linear.com) LTC3701 dual switching regulator to provide a sequenced, and standby-controlled, power supply for an Equator Technologies (www.equator.com) broadband-signal processor. You can also adjust the circuit for FPGA or generic microprocessor applications. The features of the circuit in **Figure 1** increase the regulator's stability beyond what you can achieve with the standard Linear Technology application-note circuit.

The LTC3701 switching regulator, IC_1, provides two independently adjustable output voltages with very high voltage accuracy at a cost compatible with consumer-type applications. Because of cost constraints, it does not provide the soft-start or shutdown features present in other switching regulators. This design adds three discrete transistors to the conventional regulator circuitry to provide both arbitrary power-on-sequencing control and a simultaneous-shutdown feature. Q_3, Q_4, and Q_5 are inexpensive discrete

Figure 1



Adding a few transistors to a switching regulator adds power-sequencing and shutdown control to a power supply.

devices that control the voltage on the regulator's I_{TH}/Run pins. The I_{TH}/Run pins of IC_1 provide an external compensation to the internal feedback loops; they can also serve to shut down the device when you pull them to ground. A microprocessor's TTL/CMOS-compatible input signal (Sleep) controls the power state of the circuit. You can put the circuit into shutdown mode by either letting the Sleep pin float high or pulling it higher than approximately 1.5V. Q_3 then connects the I_{TH}/Run1 pin to ground, which causes the V_{CORE} core-voltage supply to shut off. The V_{CORE} voltage then drops toward ground, and Q_4 stops conducting when V_{CORE} falls below approximately 0.8V. The gate of Q_5 pulls to the 5V unregulated input voltage, and Q_5 shorts the I_{TH}/Run2 pin to ground, which turns off the 3.3V regulator. The circuit is now in standby mode, and both power supplies are off.

Pulling the Sleep pin lower than approximately 0.8V turns on the power supply and sequences the voltages in the following manner: Q_3 stops conducting, and the voltage on the I_{TH}/Run1 pin can rise, thanks to internal current sources in IC_1. The V_{CORE} voltage regulator then starts to operate, and V_{CORE} rises to its set voltage, 1.2V by default. Q_4 starts conducting as soon as V_{CORE} rises above approximately 0.8V. This action turns off Q_5 and allows the I_{TH}/Run2 pin voltage to start rising. The 3.3V power supply thus turns on. The combined effect of driving Q_4 and Q_5 from the V_{CORE} voltage is that the 3.3V I/O voltage always turns on only after the V_{CORE} voltage attains an established level. The end result is to sequence the power supplies over a period of 4 msec (**Figure 2**).

The circuit is symmetric, and changing the base drive of Q_4 and interchanging the drain signals of Q_3 and Q_5 reverses the sequencing order of the power supplies for chips that require the I/O voltage to rise before the core voltage. You can adjust the value of R_1 to generate any core voltage above approximately 1V. You may need to adjust the value of R_9 if your design requires core voltages below approximately 1V. You can replace Q_3 and Q_5 by potentially cheaper industry-standard 2N2007 devices at the expense of slightly higher capacitive loading on the I_{TH}/Run pins of IC_1. C_2 and C_6 are compensation capacitors that the Linear Technology literature does not mention but that are highly effective in preventing subharmonic oscillation arising from dynamic current loading on the outputs. (See the Linear Technology Web site for information on subharmonic oscillation.)

The gate-drain-source capacitance of Q_3 and Q_5 also add to the stability of the loop filter. Note that sequencing the turn-on ramps of the power supplies also has the benefit of reducing the inrush current into the power supply by staggering this current and preventing simultaneous current loading of the primary bypass capacitors by both power supplies. The selected component values allow for more than 2A of current on the 3.3V line and more than 3.5A of current on the V_{CORE} line.□

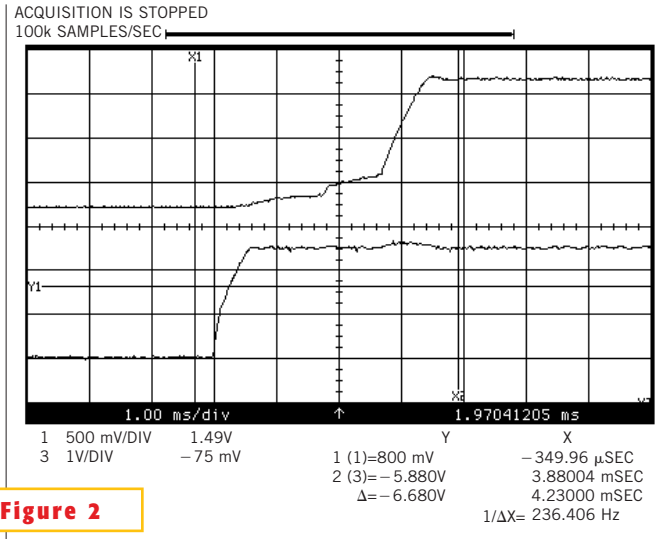


Figure 2 The 3.3V supply turns on several milliseconds after V_{CORE} attains an established level.

MathCAD functions perform log interpolation

James Bach, Delphi Delco Electronics Systems, Kokomo, IN

MathCAD provides a number of interpolation and curve-fitting functions, so that, given a set of X-Y data points, you can estimate the Y value for any given X coordinate. Unfortunately, these functions work poorly with data that is to be displayed in a nonlinear (logarithmic) manner. Examples of these functions are:

- Log-Lin: phase/magnitude-versus-frequency (Bode plots);
- Log-Log: impedance-versus-frequency (reactance plots); and
- Lin-Log: impedance-versus-tem-

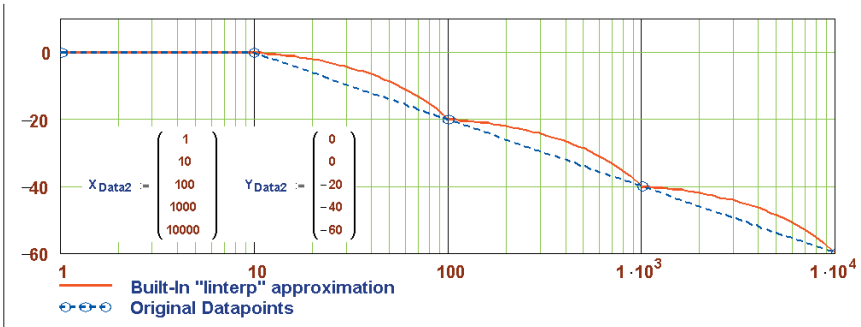


Figure 1 At X coordinates between data points, MathCAD's linterp function creates a bulging effect.

(continued on pg 94)

perature (thermistor data).

Using the built-in "linterp" function, MathCAD estimates and plots the data (**Figure 1**). As you can see, at X coordinates between the original data points, the "linterp" function creates a "bulging" effect. The following trio of simple interpolation functions allows the correct interpolation of nonlinear data on its appropriate scale. These routines function by prewarping the incoming-data matrices before feeding them into the existing "linterp" function; for logarithmic Y-axis functions, you raise 10 to the result of the "linterp" function to restore the values to the proper decade:

$$LogLogInterp(Vx, Vy, X) \equiv 10^{linterp(\overrightarrow{\log(Vx)}, \overrightarrow{\log(Vy)}, \log(X))} \quad Log\ X / Log\ Y$$

$$LogLinInterp(Vx, Vy, X) \equiv linterp(\overrightarrow{\log(Vx)}, Vy, \log(X)) \quad Log\ X / Lin\ Y$$

$$LinLogInterp(Vx, Vy, X) \equiv 10^{linterp(Vx, \overrightarrow{\log(Vy)}, X)} \quad Lin\ X / Log\ Y$$

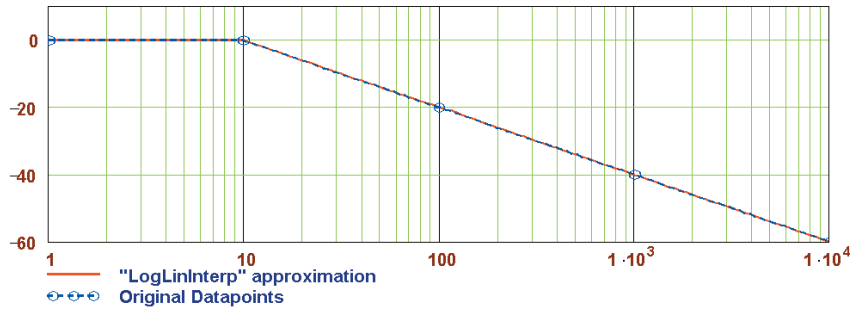


Figure 2 Using the LogLogInterp function, the bulges in Figure 1 disappear.

Using the newly created LogLogInterp function, the straight-line data is displayed (**Figure 2**).□

Scheme improves on low-cost keyboard

Martin O'Hara, Telematica Systems Ltd, Cranfield, Bedfordshire, UK

You can easily improve on a previous Design Idea to produce a slightly simpler resistor arrangement with better timing balance between switches, using a single resistor value (**Reference 1**, **Figure 1**). The use of a single resistor value, R_S, in a series chain for the switch resistors gives the timing parameters a simpler format and should reduce bill-of-materials cost. The timing balance between switches should now also be more even. The improved balance eases extending the keyboard for adding key inputs. The additional benefit of this arrangement is to make the circuit easier to adapt for faster or slower microprocessors, because you can easily adapt the circuit by changing the single switch resistor or capacitor values to alter the charge-discharge characteristics (**Figure 2**). It can also make building the circuit into a keypad housing easier, especially if you use membrane keys. The entire circuit is an SMD assembly with just two component types: switch and resistor. In the original idea, in cases of multiple keys being pressed, the timing is some odd multiple of parallel resistors and could accidentally represent a key that was not selected. With the arrangement of **Figure 1**, the lowest order key dominates; hence, the keypad has hard-wired priority setting and always results in a selected key timing, and no intermediate timing period should occur.□

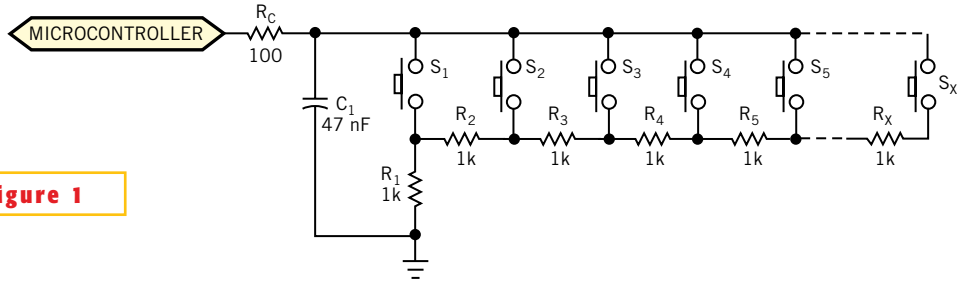


Figure 1 This simple keypad arrangement uses a single resistor value to select the switches.

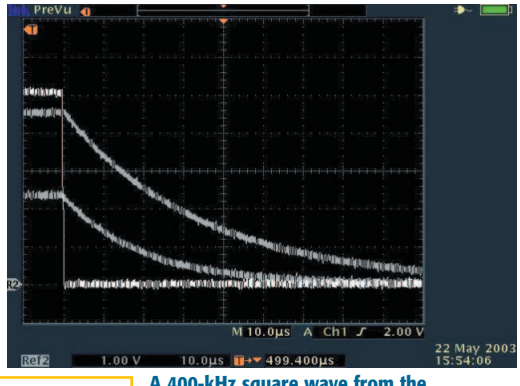


Figure 2 A 400-kHz square wave from the microprocessor shows no key, key 1, and key 5 pressed.

Reference

1. Thevenin, Jean-Jacques, "Novel idea implements low-cost keyboard," *EDN*, April 3, 2003, pg 69.

ADC interface conditions high-level signals

Moshe Gerstenhaber and Stephen Lee, Analog Devices, Wilmington, MA

DESIGNERS who build equipment for the industrial market share a widespread problem. At one extreme, they must build equipment that supports ±10V bipolar voltages, often riding on a high common-mode level, a requirement enforced by 30 years of legacy industrial equipment. At the other extreme, the analog signal needs conditioning to match the full-scale range of a low-voltage, single-supply ADC. Designers need to scale and level-shift signal levels throughout their system to accommodate the high voltage levels that sensor manufacturers dictate and the low voltage levels that the ADC dictates. Operating from a single 5V supply, the circuit in this Design Idea provides an interface of large bipolar inputs to a single-supply, low-voltage, differential-input ADC. The circuit in **Figure 1** comprises two difference amplifiers, connected in antiphase. The differential output, V_1-V_2, is an attenuated version of the input signal: $V_1-V_2=(V_A-V_B)/5$.

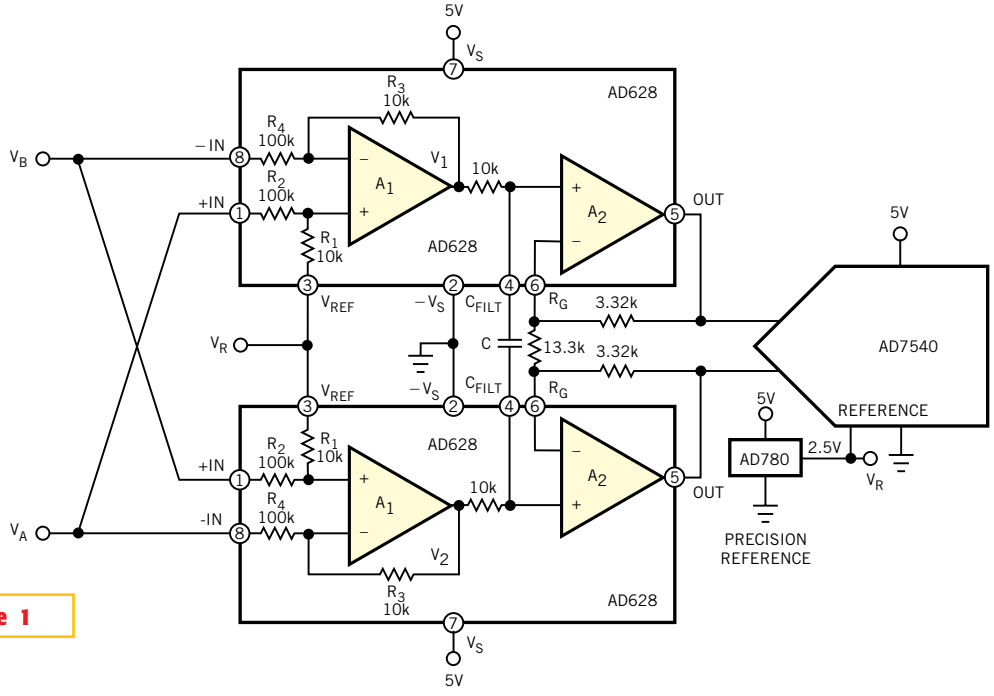


Figure 1 This circuit attenuates and level-shifts a ±10V differential signal while operating from a single 5V supply.

The difference amplifiers reject the common-mode voltage on inputs V_A and V_B. The reference voltage, V_R, which the AD780 develops and the ADC and the amplifier share, sets the output common-mode voltage. A single capacitor, C, placed arcros the C_{FILT} pins, lowpass-filters the difference signal, V_1-V_2. The −3-dB pole frequency is: $f_P=1/(40{,}000\times\pi\times C)$. A_2 amplifies the difference signal by 1.5. Thus, the total gain of this circuit is $^3/_{10}$. **Figure 2** shows a 10V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom). The benefits of this configuration go beyond simply interfacing with the ADC. The circuit improves specifications such as common-mode-rejection ratio, offset voltage, drift, and noise by a factor of $\sqrt{2}$ because the errors of each AD628 are not correlated.

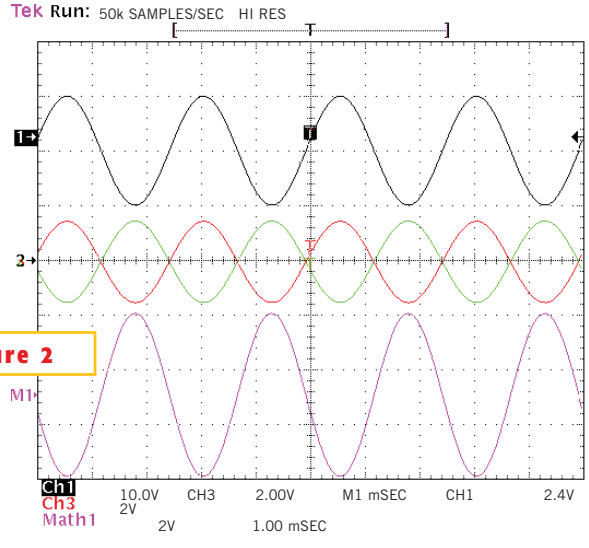


Figure 2 The waveforms show a 10V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom).

The output demonstrates 85-dB SNR (**Figure 3**). The two AD628s interface with an AD7450 12-bit, differential-input ADC. The AD7450 easily rejects residual common-mode signals at the output of the difference amplifiers. **Figure 4** shows the common-mode error at the output of the AD628.

The topmost waveform is a 10V, common-mode input signal. The middle waveform, measuring 150 µV, is the common-mode error measured, differentially, from the output of the two AD628s. The bottom waveform, measuring 80 µV, is the resultant common-mode error.□

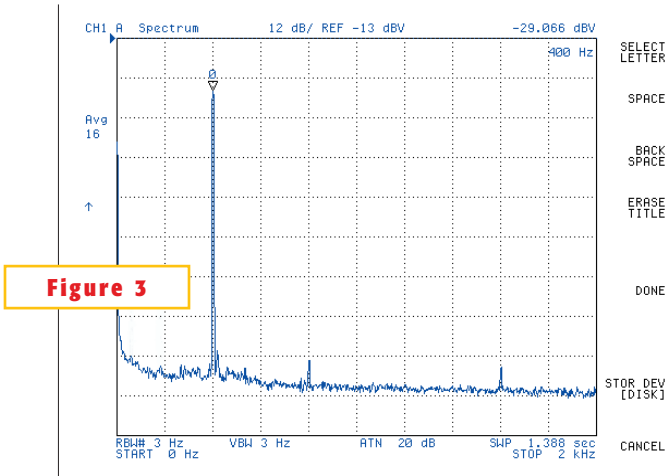


Figure 3

The circuit in Figure 1 has an 85-dBV SNR.

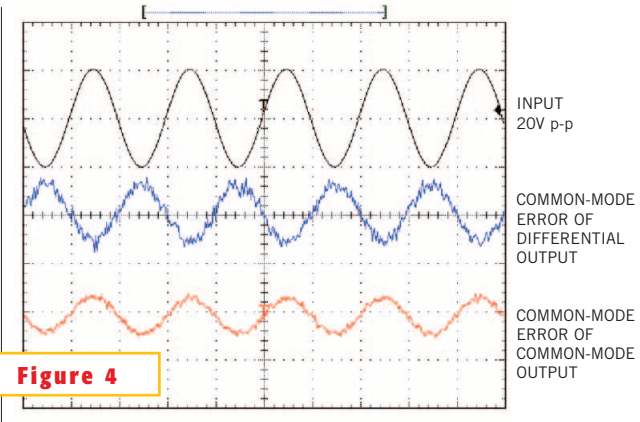


Figure 4

The common mode input (top) measures 20V p-p. The common-mode error of the differential output (middle) is 200 µV p-p. The error of the common-mode output (bottom) is 80 µV p-p.

Two op amps provide averaged absolute value

Dobromir Dobrev, Jet Electronics, Sofia, Bulgaria

THE CIRCUIT in **Figure 1** is useful when you need amplitude demodulation or an averaged absolute-value conversion. The circuit comprises two stages, the first of which, IC_{1A}, is a differential-output absolute-value converter. The second stage, IC_{1B}, is a traditional differential amplifier. The combination of the two stages performs single-ended absolute-value conversion but only if $R_3 >> R_2$. The C_1 capacitors integrate the current flow and yield averaged voltages V_A and V_B. In addition, the capacitors ensure low ac-impedance points at nodes V_A and V_B when the output diodes are reverse-biased. The additional C_2 capacitors in parallel with R_4 resistors impart a second-order-lowpass-filter characteristic to the circuit and remove the remaining ac signal. From a practical point of view, you can choose R_3 to be five to 10 times higher than R_2. The gain of the circuit is $(R_2||R_3/R_1)(R_4/R_3)$. In most applications, you would choose the filter time constants $\tau_1 = R_2||R_3C_1$ and $\tau_2 = R_4C_2$ to be equal. The circuit in **Figure 1** is simple, symmetrical, and cost-effective. It also makes it easy to calculate and adjust the gain using one resistor, R_1. Other advantages are that the circuit has equal delay for positive- and negative-going signals and that it doesn't need matched diodes.□

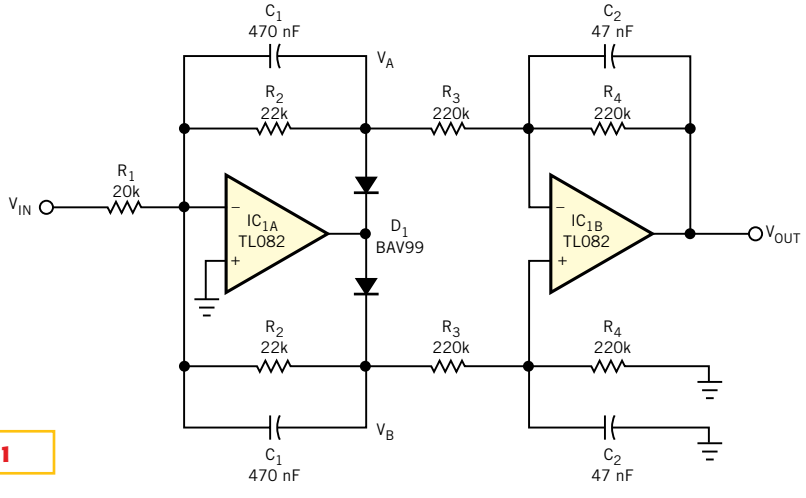


Figure 1

This single-ended, averaged absolute-value converter is useful for amplitude demodulation.

Edited by Bill Travis

Input filter prevents instrumentation-amp RF-rectification errors

Charles Kitchin, Lew Counts, and Moshe Gerstenhaber, Analog Devices, Wilmington, MA

Instrumentation amplifiers serve in a variety of applications that need to extract a weak differential signal from large common-mode noise or interference. However, designers often overlook the potential problem of RF rectification inside the instrumentation amplifier. The amplifier's common-mode rejection normally greatly reduces common-mode signals at an instrumentation amplifier's input. Unfortunately, RF rectification still occurs, because even the best instrumentation amplifiers have virtually no common-mode rejection at frequencies higher than 20 kHz. The amplifier's input stage may rectify a strong RF signal and then appear as a dc-offset error. Once the input stage rectifies the signal, no amount of low-pass-filtering at the instrumentation amplifier's output can remove the error. Finally, if the RF interference is intermittent, measurement errors may go undetected. The best practical solution to this problem is to provide RF attenuation ahead of the instrumentation amplifier by using a differential lowpass filter. The filter needs to remove as much RF energy as possible from the input lines, preserve the ac signal's "balance" between each line and ground (common), and maintain a high enough input impedance over the measurement bandwidth to avoid loading the signal source. **Figure 1** provides a basic building block for a wide range of differential RFI filters.

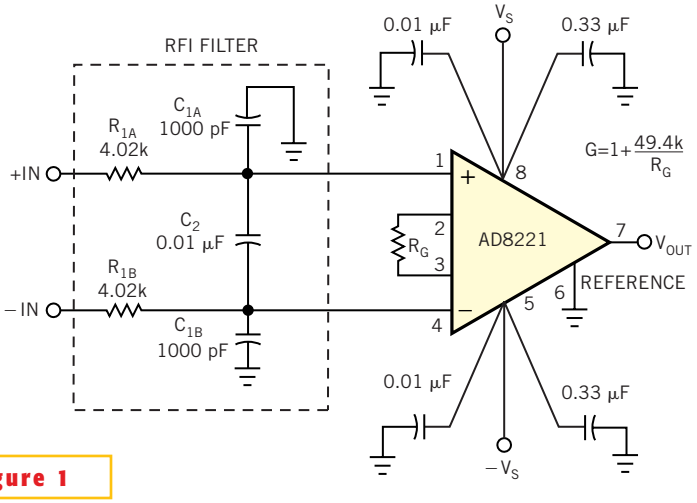


Figure 1

This lowpass-filter circuit prevents RF-rectification errors in instrumentation amplifiers.

The component values are typical of those for the latest generation of instrumentation amplifiers, such as the AD-8221, which has a typical −3-dB bandwidth of 1 MHz and a typical voltage noise level of 7 nV/$\sqrt{\text{Hz}}$. In addition to RFI suppression, the filter also provides additional input-overload protection; resistors R_{1A} and R_{1B} help isolate the instrumentation amplifier's input circuitry from the external signal source. **Figure 2** shows a simplified version of the RFI circuit. It reveals that the filter forms a bridge circuit whose output appears across the instrumentation amplifier's input pins. Because of this connection, any mismatch between the time constants of C_{1A}/R_{1A} and C_{1B}/R_{1B} unbalance the bridge and reduce high-frequency common-mode rejection. Therefore, resistors R_{1A} and R_{1B} and capacitors C_{1A} and C_{1B} should always be equal. C_2 connects across the "bridge output" so that C_2 is effectively in parallel with the series combination of C_{1A} and C_{1B}. Thus connected, C_2 effectively reduces any ac common-mode-rejection errors from mismatching. For example, making C_2 10 times larger than C_1 provides a 20-times reduction in common-mode-rejection errors arising from C_{1A}/C_{1B} mismatch. Note that the filter does not affect dc common-mode rejection.

The RFI filter has differential and common-mode bandwidths. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the circuit's two inputs, +IN and −IN. The sum of the two equal-value input resistors, R_{1A} and R_{1B}, and the differential capacitance,

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which is C_2 in parallel with the series combination of C_{1A} and C_{1B}, establish this RC time constant. The −3-dB differential bandwidth of this filter is equal to $BW_{DIFF}=[1/(2\pi R(2C_2+C_1))]$. The common-mode bandwidth defines what a common-mode RF signal "sees" between the two inputs tied together and ground. C_2 does not affect the bandwidth of the common-mode RF signal, because this capacitor connects *between* the two inputs, helping to keep them at the same RF-signal level. Therefore, the parallel impedance of the two RC networks (R_{1A}/C_{1A} and R_{1B}/C_{1B}) to ground sets common-mode bandwidth. The −3-dB common-mode bandwidth is equal to $BW_{CM}=1/(2\pi R_1 C_1)$.

Using the circuit of **Figure 1**, with a C_2 value of 0.01 µF, the −3-dB differential-signal bandwidth is approximately 1900 Hz. When operating at a gain of 5, the circuit has measured dc-offset shift over a frequency range of 10 Hz to 20 MHz of less than 6 µV referred to the input. At unity gain, there is no measurable dc-offset shift. Some instrumentation amplifiers are more prone to RF rectification than others and may need a more robust filter. A micropower instrumentation amplifier, such as the AD627, with its low-input-stage operating current, is a good example. The simple expedient of increasing the value of the two input resistors, R_{1A}/R_{1B}, that of capacitor C_2, or both can provide further RF attenuation at the expense of reduced signal bandwidth. Some steps for selecting RFI-filter component values follow:

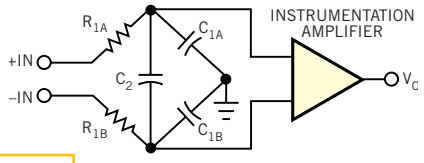


Figure 2

Capacitor C_2 shunts C_{1A}/C_{1B} and reduces ac common-mode-rejection errors arising from component mismatch.

1. Decide on the value of the two series resistors and ensure that the previous circuitry can adequately drive this impedance. With typical values of 2 to 10 kΩ, these resistors should not contribute more noise than that of the instrumentation amplifier itself. Using a pair of 2-kΩ resistors adds Johnson noise of 8 $nV/\sqrt{Hz}$. This figure increases to 11 $nV/\sqrt{Hz}$ with 4-kΩ resistors and 18 $nV/\sqrt{Hz}$ with 10-kΩ resistors.

2. Select an appropriate value for capacitor C_2, which sets the filter's differential (signal) bandwidth. Set this value as low as possible without attenuating the input signal. A differential bandwidth of 10 times the highest signal frequency is usually adequate.

3. Select values for capacitors C_{1A} and C_{1B}, which set the common-mode bandwidth. For decent ac common-mode rejection, these capacitors should have values 10% or lower of the value of C_2. The common-mode bandwidth should always be less than 10% of the instrumentation amplifier's bandwidth at unity gain.

You should build the RFI filter using a pc board with a ground plane on both sides. All component leads should be as short as possible. Resistors R_1 and R_2 can be common 1% metal-film units. However, all three capacitors need to be reasonably high-Q, low-loss components. Capacitors C_{1A} and C_{1B} need to be ±5%-tolerance devices to avoid degrading the circuit's common-mode rejection. Good choices are the traditional 5% silver micas, miniature micas, or the new Panasonic ±2% PPS film capacitors (Digi-key part number PS1H102G-ND).□

White-LED driver backlights LCD and keypad

Fabien Franc, Catalyst Semiconductor, Sunnyvale, CA

Designers widely use white LEDs to backlight color LCDs and keypads in handheld devices, such as cell phones, MP3 players, GPS navigators, and PDAs. Their spectrum and brightness represent near-ideal light sources. One possible configuration for a phone or a phone/PDA combination is to have a group of three LEDs to light the display and six LEDs for the keypad. **Figure 1** shows a method for driving all the LEDs with a single driver IC from Catalyst Semiconductor (www.catsemi.com), the CAT32. Power comes from a single lithium-ion battery cell. A FET switch can independently turn off the group of six LEDs. The shutdown input, $\overline{SHDN}$, on the CAT32 turns off all the LEDs. LED brightness is a direct function of the current running through

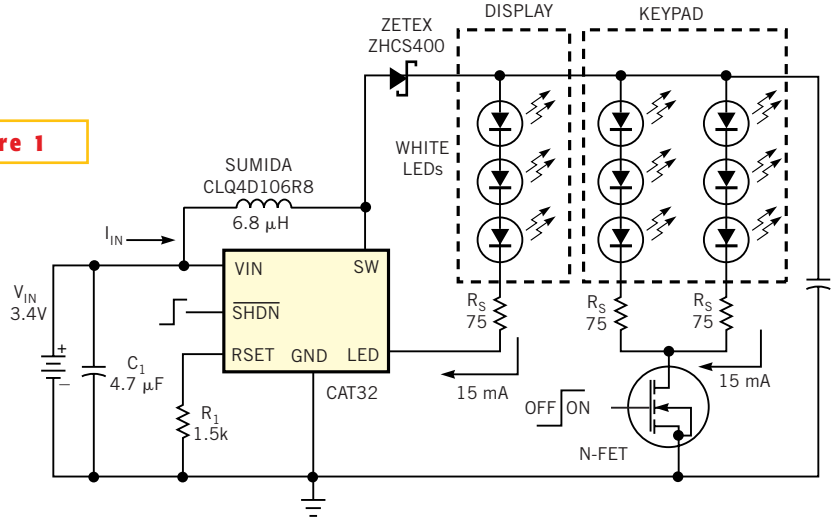
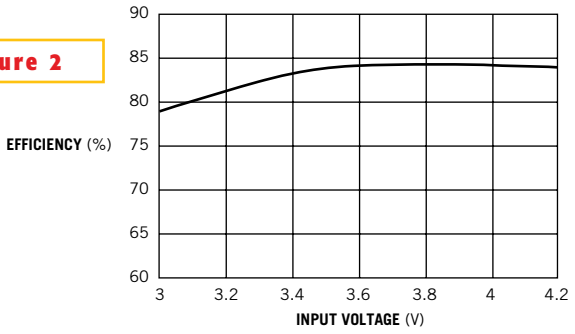


Figure 1

A single IC boosts the battery voltage to drive a total of nine LEDs.

the LED, and typical values are 10 to 20 mA for white LEDs. The CAT32 regulates a constant current through the LED pin. Resistor R_1 connected to the RSET pin adjusts the LED current.

The driver is a step-up converter using an inductor to boost the voltage, such as that from a lithium-ion battery, and bias multiple LEDs in series. The R_S resistors in series with the LEDs balance out the current between the groups of LEDs. The LED forward voltage, typically around 3.5V, experiences some variation from one LED to the other for a given bias current, and the series resistors also compensate for that situation. By using series resistors with values of 75Ω, a current of approximately 15 mA flows in all LEDs. The display uses Nichia (www.nichia.com) NSCW335 side-view LEDs, and top-view Nichia NSCW100 LEDs backlight the keypad. You define efficiency as the ratio of the power dissipated in the LEDs, including the power in the series resistors but not including the loss in the Schottky diode, to the total input power. **Figure 2** shows the efficiency of the circuit for a load of 15-mA current in the LEDs and for supply voltage ranging from 3 and 4.2V, corresponding to the charge-discharge cycle of lithium-ion batteries. The expression for efficiency is as follows:



This curve shows the efficiency of the circuit in Figure 1 for 15-mA LED current and 3 to 4.2V battery voltage.

$$\text{EFFICIENCY} = \frac{P_{OUT}}{P_{IN}} = \frac{\sum_{i=1}^{9} V_{LEDi} \times I_{LEDi} + \sum_{j=1}^{3} R_{Sj} \times I_i^2}{V_{IN} \times I_{IN}},$$

where V_{LED} is the voltage across the LED, I_{LED} is the LED current, R_S is the series resistor, and I_{IN} is the current from the input supply. The efficiency is approximately 84% for a 3.6V supply. If you now consider only the power the LEDs dissipate, excluding all the other losses, the following formula gives the net efficiency (approximately 75% with a 3.6V supply):

$$\text{NET EFFICIENCY} = \frac{P_{OUT}}{P_{IN}} = \frac{\sum_{i=1}^{9} V_{LEDi} \times I_{LED_i}}{V_{IN} \times I_{IN}}.$$

Microcontroller or DSP circuit controls on/off function

Dirk Gehrke, Texas Instruments, Freising, Germany, and Frans Ravn, ChemoMetec A/S, Alleroed, Denmark

In many applications, a single on/off button switches the power supply on or off. Usually, the system switches off regardless of the processing function or workload the microcontroller or DSP circuit is currently handling. The small circuit in **Figure 1** is intended to make the microcontroller or DSP circuit the master over this on/off function. The circuit allows the microcontroller or DSP circuit to take ownership over the on/off function. Thus, the system can do whatever has to be done, such as processing data, storing data, and so forth, before it issues the command to shut down the supply. **Figure 2** shows the timing diagram. The switch connects directly to the dc supply or battery, though the end application is disconnected from the supply. Thus, all the capacitors discharge. The most difficult task is to get the two D flip-flops in **Figure 1** into the desired "off" configuration.

The inverter, IC_{1B}, in **Figure 1** resets the D flip-flop, IC_{2B}, via the diode, D_4. The RC network comprising R_{10}, R_{11}, and C_4, connected to the input of the inverter, IC_{1B}, generates a delay time of approximately 4.7 msec. This interval ensures that this D flip-flop is released from reset after a delay time of approximately 4.7 msec. When the delay time has passed, reset-input pin R of IC_{2B} changes from high to low potential because R_7 connects to ground. At the same time, output Q of IC_{2B} switches to low level, and $\overline{Q}$ switches to high level. The D input node of IC_{2B} changes as well from high to low potential because it connects to the output pin, $\overline{Q}$. The RC network comprising R_1 and C_3, in conjunction with the inverter, IC_{1A}, generates a delay of approximately 47 msec. This delayed output connects to the set pin of the D flip-flop, IC_{2A}. The set pin holds high for 47 msec before it goes low. The RC network, comprising $R_1$and C_3, along with the inverter, IC_{1A}, generate a 47-msec delay. The delayed output connects to the set pin of the D flip-flop, IC_{2A}. The set pin holds high for 47 msec before it goes low.

After the set pin falls to a low level, the D flip-flop, $IC_{2A,}$ changes its output levels at Q to high and $\overline{Q}$ to low, and feedback from $\overline{Q}$ connects to the D input. The high level at Q ($\overline{SHTDN}$), connected to the enable pin of the dc/dc converter or low-dropout regulator, keeps the system off. The D flip-flop, IC_{2A}, is now in an off condition. From this point on, both D flip-flops are in a known state. The DSP I/O pin is low during this initialization, because the DSP circuit receives no power. R_{15} ensures a low level during the power-up sequence at the DSP I/O pin. The $\overline{SHTDN}$, after its initialization phase, assumes an active-high level. If you connect it to the enable pin of the system dc/dc converter or low-dropout regulator, it keeps the system in an off condition. IC_{1B}'s input changes its level from high to low when you press the pushbutton, because the switch shorts the pullup resistor at the pushbutton node to ground. IC_{1B}'s output changes its level according-

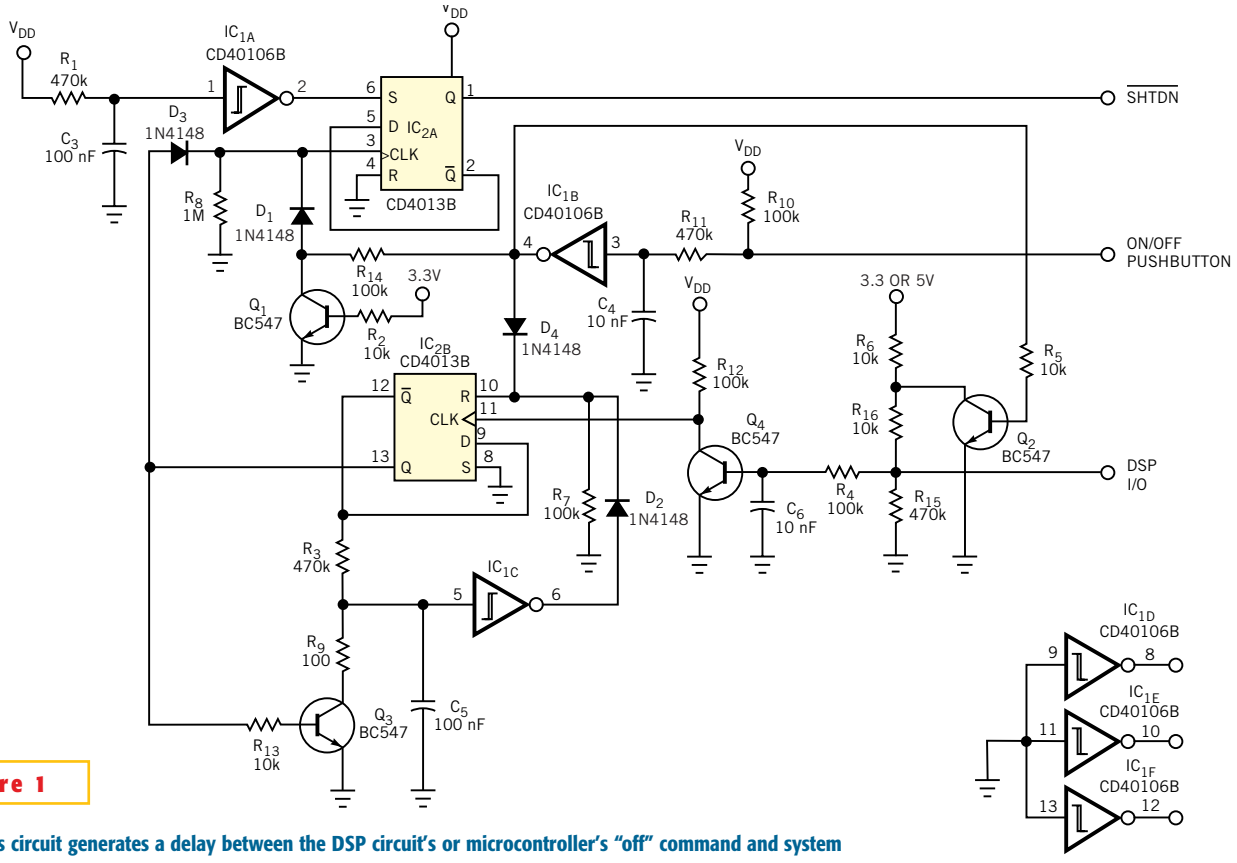


Figure 1

This circuit generates a delay between the DSP circuit's or microcontroller's "off" command and system shutdown.

ly from low to high for that period.

The CLK input of D flip-flop IC_{2A} triggers via R_{14} and D_1, and output Q changes its status from low to high. This state enables the low-dropout regulator or dc/dc converter to start operation. The 3.3 or 5V connected to R_2 supplies transistor Q_1 to change the logic level at the CLK input of D flip-flop IC_{2A}. This action ensures that the system disregards glitches when you press the on/off pushbutton. The DSP I/O pin of the circuit connects to one of the DSP circuit's or microcontroller's I/O pins. You should configure the I/O pin of the DSP circuit or microcontroller as an input pin after power-up and reset release. As long as you press the on/off pushbutton, transistor Q_2 remains on, driving the DSP circuit's I/O pin low. You should program the DSP circuit or microcontroller such that the DSP circuit stops executing code before you release the button, and the DSP I/O pin changes its level from low to high. D flip-flop IC_{2B} again resets via D_4, but this reset does not alter the output because the application is running.

When you again press the on/off pushbutton, the DSP I/O pin assumes a low level. The DSP circuit or microcontroller should now detect this input change and generate an interrupt. This interrupt should initiate a shutdown procedure. D flip-flop IC_{2B} changes, via D_4, to reset mode, so that the toggle signal valid at CLK has no impact on the output status. You now release the on/off pushbutton. D flip-flop IC_{2B} releases from reset after

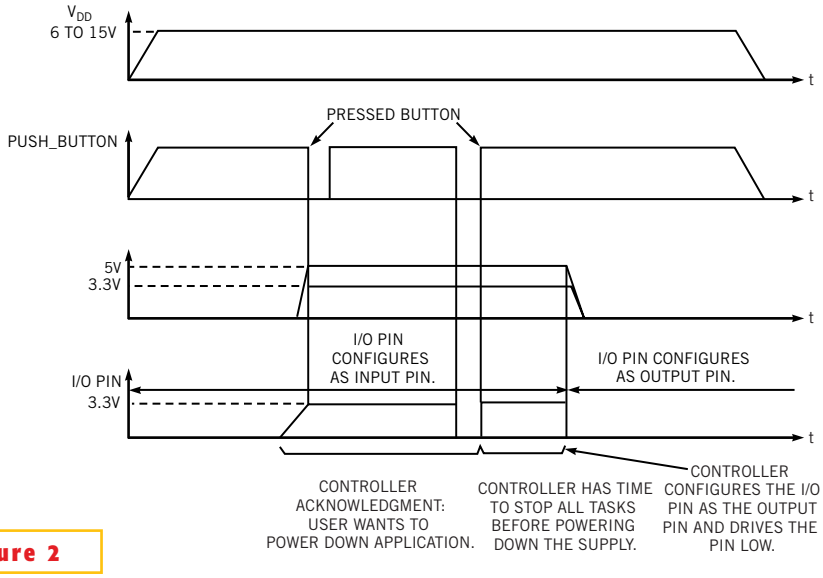


Figure 2

This timing diagram shows that the DSP circuit or microcontroller takes ownership over the system's on/off function to allow time for performing crucial tasks.

approximately 4.7 msec, and Q_2 and Q_4 change levels and maintain a low signal at the CLK pin before the reset delay time passes. The microcontroller or DSP circuit sees a high signal at the I/O pin after this time-out and can start the shutdown procedure.

The DSP circuit or microcontroller now has the time to store any critical data. You must program the microcontroller's or DSP circuit's I/O pin as an output pin set low. Q_4 loses its drive voltage, and the CLK pin of D flip-flop IC_{2B} changes its status from low to high. D flip-flop IC_{2A} changes its output status via the output, Q, and D_3. Q and $\overline{Q}$ change the status of the $\overline{SHTDN}$ pin to low level, and the system shuts down. At the same time, D flip-flop IC_{2B} resets via Q_3 and the comparator IC_{1C}. This reset brings D flip-flop IC_{2B} to the initial state described above before you first pressed the on/off pushbutton.□

Simple power supply fits into small spaces

Raymond Zheng, Linear Technology, Milpitas, CA

THE DEMAND FOR negative-voltage power supplies is increasing with the popularity of applications for portable devices. It can be expensive and relatively complicated to generate a negative supply from a positive input source, especially when the design requires both positive and negative outputs. **Figure 1** shows a simple and cost-effective solution that combines a voltage inverter and a voltage doubler in a single charge-pump circuit. It produces a regulated −5V output and an unregulated 10V output from a 5 to 6V input. The circuit requires only five small, ceramic, surface-mount capacitors and two diodes in addition to the charge-pump IC in an SOT-23 package.

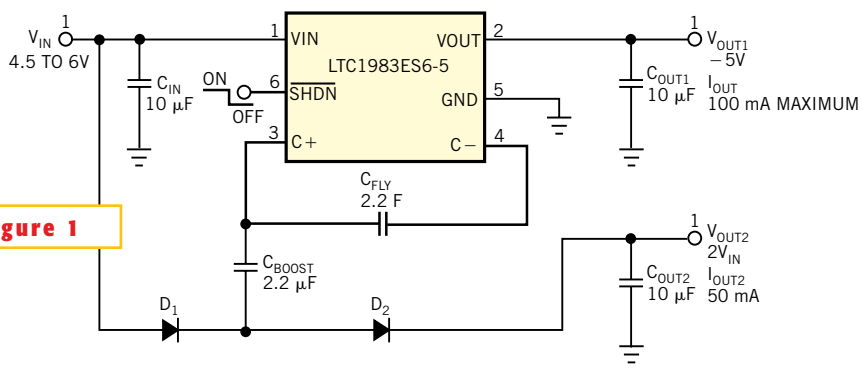


Figure 1

NOTES: C_{IN}, C_{OUT1}, C_{OUT2}: TAIYO YUDEN JMK316BJ106ML.
C_{FLY}: TAIYO YUDEN LMK212BJ225MG.
C_{BOOST}: TAIYO YUDEN EMK316BJ225ML.

This circuit combines a regulated inverter and a voltage doubler.

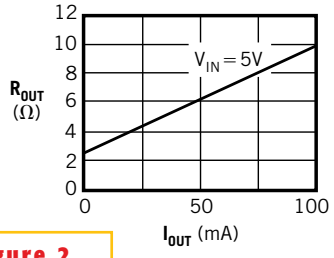


Figure 2

This graphic shows R_{OUT} versus I_{OUT} for the circuit in Figure 1.

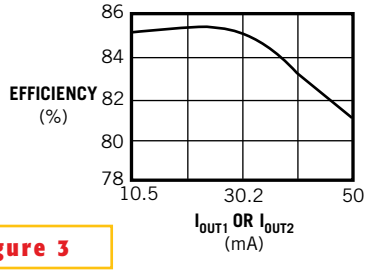


Figure 3

This curve shows efficiency versus either output current.

From a 6V input, the inductorless dc/dc inverter can deliver 100 mA at a regulated −5V (±5%), and the voltage doubler can provide 50 mA at 10.5V with ±7% variation. The inverter's output-voltage regulation follows the relationship $(V_{IN}-5)>(I_{OUT}\times R_{OUT})$; you can determine the values of R_{OUT} and I_{OUT} for V_{IN}=5V from the graph in **Figure 2**. (The R_{OUT} and I_{OUT} values for other V_{IN} values are available in the LTC-1983's data sheet.) If the variables don't meet this inequality condition, the part runs in open-loop mode and acts as a low-output-impedance inverter in which the output voltage is $V_{OUT1}=-[V_{IN}-(I_{OUT}\times R_{OUT})]$. You can define the output voltage of the voltage doubler as $V_{OUT2}=2V_{IN}-2V_D$, where V_D is the forward voltage drop across the diodes. **Figure 3** shows the efficiency of the circuit, which exceeds 81% and peaks at approximately 85%. **Figure 4** shows the inverter's output-voltage regulation versus inverter output current. The IC includes short-circuit and thermal protection.□

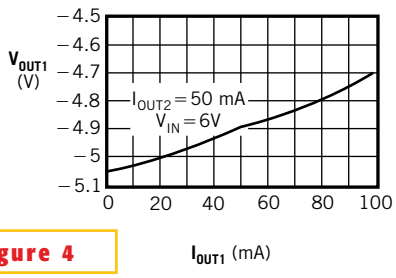


Figure 4

This curve shows output-voltage regulation versus output current.

Amplifier and current source emulate instrumentation amplifier

Dobromir Dobrev, Jet Electronics, Sofia, Bulgaria

THE CLASSIC three- or two-op-amp instrumentation-amplifier circuits are standard ways to amplify a small-amplitude differential signal contaminated with high common-mode noise. In some applications, the signal source is floating with high-series-output impedance and thus requires an appropriate high-input-impedance amplifier. This Design Idea proposes an alternative approach using a simplified amplifier circuit (**Figure 1**). The basic principle is to sense the current in the amplifier input B (I_B) and inject a current of the same value in the amplifier input A (I_A), by combining a virtual-ground transimpedance amplifier (A_1) with a voltage-controlled current source (G_1). Thus, G_1 balances the common- mode interference currents. In addition, the voltage at input B is at virtual-ground potential.

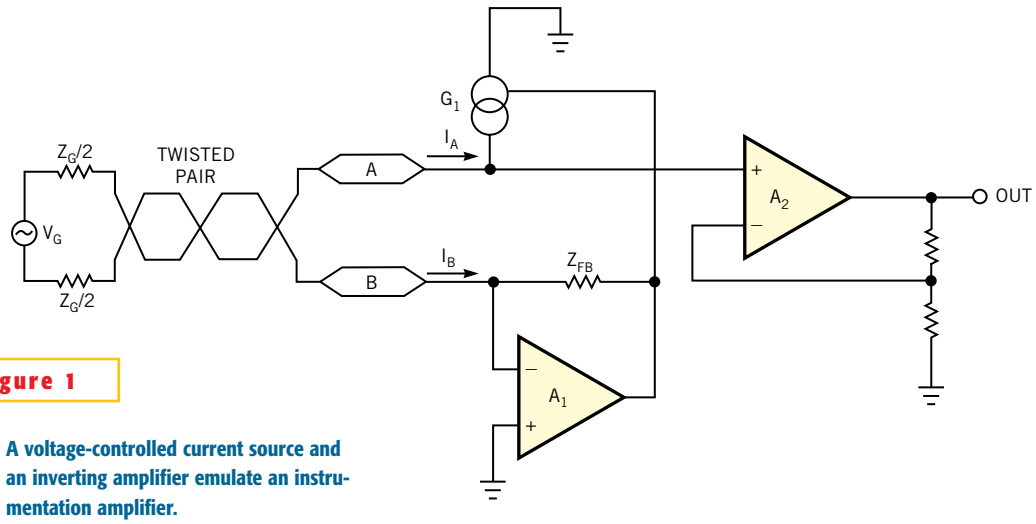


Figure 1

A voltage-controlled current source and an inverting amplifier emulate an instrumentation amplifier.

A practical circuit is a two-electrode biosignal amplifier for electrocardiogram signals (**Figure 2**). IC_{2B} is the transimpedance amplifier. The feedback capacitor, C_{FB}, ensures circuit stability. The INA134 difference amplifier, IC_1, and the op amp, IC_{2A}, make up a high-quality, bidirectional voltage-controlled current source. You could use many similar ICs, such as INA132, 133, 152, 154, 105, or AMP03, for IC_1. The remaining part of the circuit comprises two conventional noninverting stages. The proposed circuit can be useful in many two-wire or two-electrode applications, in which you need to maintain high amplifier input-impedance values.□

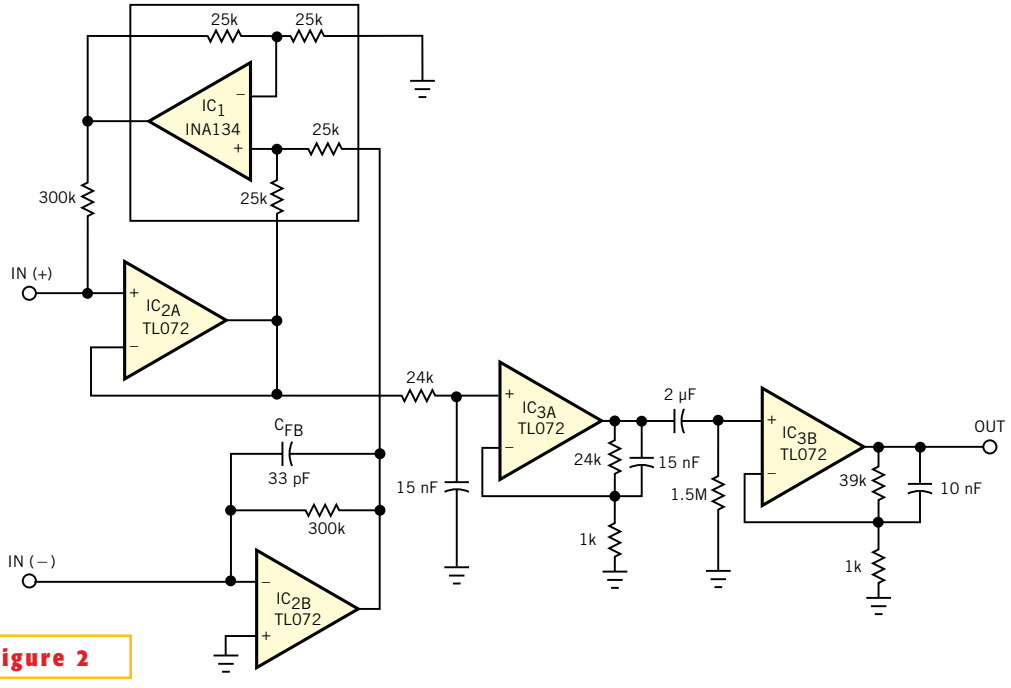


Figure 2

This biosignal amplifier has the high input impedance that medical applications require.

Hardware histogram speeds ADC test

Tony Zizzo Jr, Texas Instruments, Tucson, AZ

Accumulating enough samples to effectively and accurately measure linearity errors in pipeline converters at production test and minimizing test time are difficult enough. Add to that multiple sites, multiple channels, and the expense of multiple custom-instrument resources during periods of low capital expenditure, and engineers must think creatively to increase throughput without sacrificing yield. Many test approaches are beginning to rely more on FPGAs. These ICs' high speeds and flexible usage lend them well to ATE (automated-test-equipment) shortfall workarounds and pare down final test time, which could add up to thousands of dollars in savings, depending on time saved and volume. But development of FPGA designs can be time-consuming and expensive; outsourced designs can cost more than $100,000, depending on complexity. Also, the hardware-histogram capability of many ATE systems is expensive, and you must multiplex it to multiple sites, which reduces its time-saving effectiveness. This Design Idea presents a simple, discrete hardware-histogram circuit module (**Figure 1**), which uses off-the-shelf components, requires no software, is easy to debug, and is easy to multiply to many sites and channels.

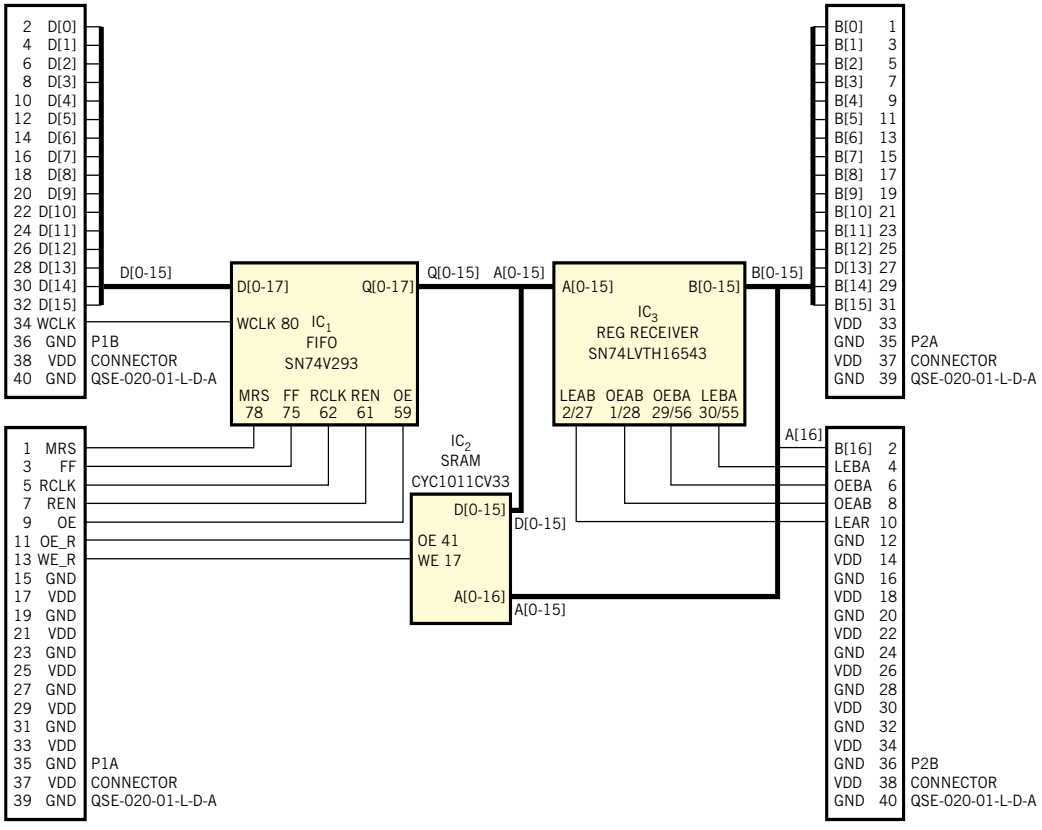


Figure 1

A hardware-based histogram system for testing ADCs uses off-the-shelf components.

The circuit of **Figure 1** shows how you can configure a FIFO memory, a static SRAM, and a bus register to generate fast hardware histograms for linearity tests and still allow straight data acquisition for other tests. The main purpose of the FIFO memory is to collect data at the speed of the DUT (device under test), because, with all the data-swapping that occurs during the histogram routine, the cycle is slower than the DUT. But it also reduces switching noise in the test circuit by keeping the outputs and the other devices "quiet" during the initial acquisition. And, because many high-speed converters require low-jitter sources, the use of the FIFO memory eliminates the need to synchronize the test head with external sources by using the system clock to run the rest of the circuit.

The SRAM stores each bin count in the address whose value is equal to the code being accumulated. The memory is generally underused, because part of the memory holds a look-up table of all practical bin counts. Rather than use an adder or a counter to implement the bin-count function, which would require an extra IC, this circuit implements data+1 by storing each look-up entry in the address whose value is one less than the value stored at that location, not including bit 16. Address-bit 16 keeps the bin counts and look-up table in different columns. When each sample routes from the FIFO memory to the address bits, the FIFO memory's output becomes disabled as the bin count for that code appears on the bus. The bus register's "bus-hold" function conveniently holds the current bin count on the address lines while the

SRAM's address-bit 16 is toggled to access the count look-up table, and the bin count+1 appears on the bus. The bus register latches in the new bin count while the FIFO memory reasserts the sample data.

The SRAM then accesses the bin count (address-bit 16 reset) in write mode when the bus register reasserts the new bin count with the FIFO memory disabled. This cycle plays out until the histogram is complete and the data is read through the bus register to the test head. **Figure 2** shows the timing scheme. Although the FIFO memory has a depth of only 64 kbytes, note that the FIFO memory can be filled multiple times and the histogram can be updated multiple times until the SRAM is cleared. You encounter no overflow, regardless of bus width, as long as no bin count exceeds 16,383. The look-up table can be written before any device is tested, and the bin counts can be reset between tests when the handler is binning. This circuit is particularly useful when your application requires multiple sites or multiple channels, because you can simply plug the inexpensive module into other sites or channels and operate it in parallel.□

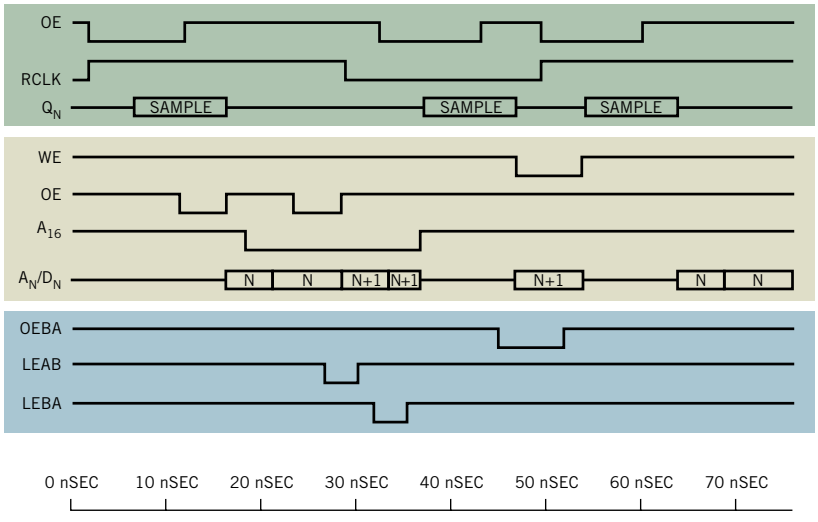


Figure 2 This graphic shows the histogram cycle timing for the circuit in Figure 1.

Edited by Bill Travis

Circuit controls microneedle etching

Stephen Woodward, Marine Sciences, Chapel Hill, NC

At its invention roughly two decades ago, STM (scanning tunneling microscopy) created a sensation because it was the first technology to make atomic-scale-resolution imaging a routine procedure. An essential requirement for the practical application of STM is some means for the reproducible fabrication of supersharp, atomic-scale needle tips. One way to make the tips is to etch them from short pieces of platinum wire in a calcium-chloride electrolyte bath. Applying an ac voltage between the electrolyte and the wire generates a chemical reaction accompanied by vigorous fizzing at the surface of the liquid. This reaction etches the platinum, causing the wire to neck down and eventually break into two pieces. If the etching current turns off within milliseconds of the wire's breaking, then the point of separation remains supersharp. This sharp point is suitable for use as a high-quality STM tip. Swift interruption of the current, however, is essential to tip sharpness, because only a few milliseconds of overetch suffice to dull and ruin the tip. The circuit in **Figure 1** achieves precision etch-termination by using relay-actuated etch turnoff based on the sudden drop in etch current that occurs when the wire parts. Precision sensing and full-wave rectification of the etch current is critical to circuit operation; the circuit achieves this precision by using an unusual differential-input rectifier.

Precision, full-wave rectification of low-level ac signals to a dc format is a common signal-processing function; many classic rectifier topologies accom-

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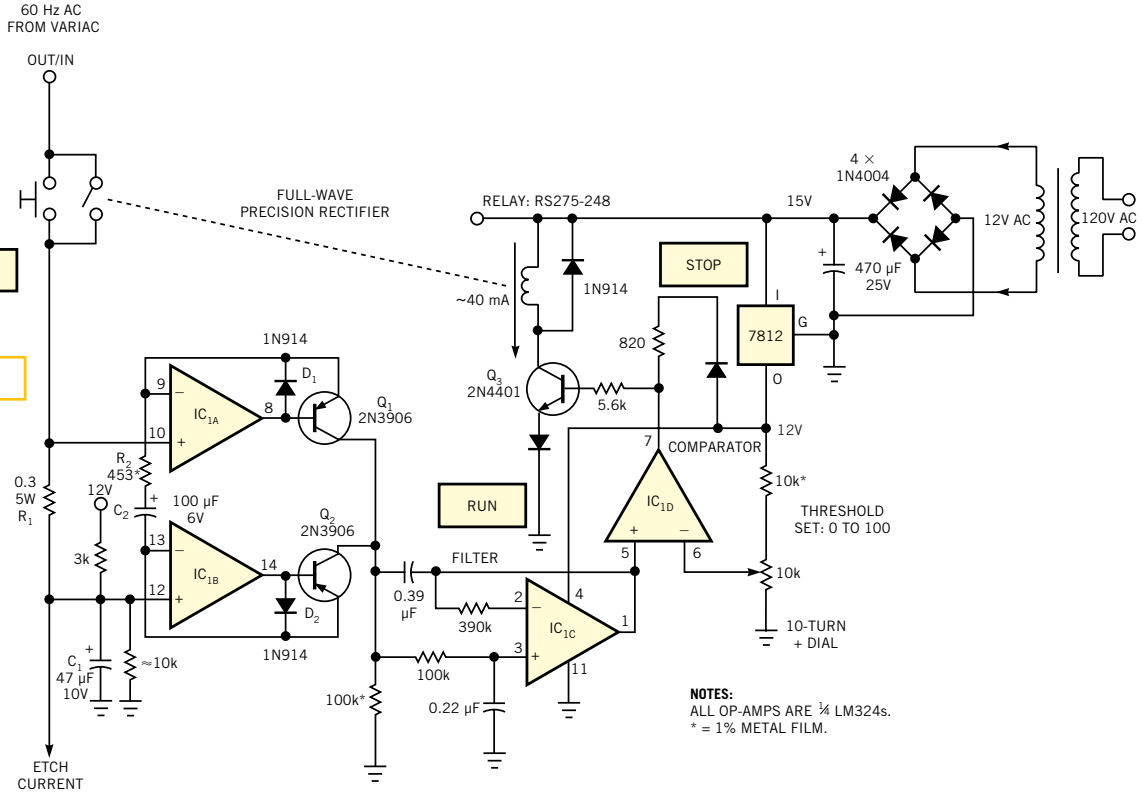
Figure 1



This etch-control circuit produces supersharp microneedles by terminating the etching process at precisely the right time.

plish this function. But the accuracy of typical precision rectifiers depends on the precise matching of resistor ratios. Moreover, op-amp input-offset voltages limit the accuracy of these standard circuits. The offset error generally limits sensitivity to input spans no smaller than some hundreds of millivolts. The converter in this design avoids these faults and adds a number of new and useful features. The differential ac signal to be rectified goes to the noninverting inputs of op amps IC_{1A} and IC_{1B} (**Figure 1**). Rectification proceeds as follows: Consider a signal excursion, V_{IN}, that drives IC_{1A}'s input more positive than IC_{1B}'s. Amplifier IC_{1A} responds by driving diode D_1 into conduction, thereby forcing R_2 to track the input. Amplifier IC_{1B} responds with a negative output excursion, forcing transistor Q_2 to conduct sufficiently to cause the inverting input of IC_{1A} and the bottom end of R_1 to track. Q_2's emitter current, and, therefore, collector current is then $I=V_{IN}/R_2=V_{R1}/R_2$; Q_2 is a high-alpha transistor.

The respective roles of the amplifiers reverse for input excursions of the opposite polarity, with D_2 and Q_2 conducting. The match of Q_1 and Q_2 alpha values, which is typically 0.3% or better, is the only limit on rectification symmetry. This precision rectifier is therefore unique in that neither rectification symmetry nor common-mode rejection, which exceeds 60 dB, depends on resistor matching. Meanwhile, C_2 affords ac coupling, which eliminates offset-voltage-related errors. Operation of the rest of the etch controller is straightforward. IC_{1C} implements a unity-gain, two-pole Butterworth lowpass filter for good ripple attenuation without excessive time delay. Etching begins when you push the Start pushbutton. The etch-current comparator, IC_{1D}, then drives Q_3 to keep the relay energized until the etch current drops below the level set by the Threshold Set potentiometer. IC_{1D}'s output then drops low, turning Q_3 off, opening the relay, and terminating the etch. The result is a serviceable, atomically sharp scan tip almost every time.□

Circuit removes relay-contact bounce

John Guy, Maxim Integrated Products, Sunnyvale, CA

Advances in semiconductor technology have allowed ICs to replace many mechanical relays, but relays still dominate in high-current circuits that must stand off high voltages of arbitrary polarity. Contact bounce in those relays, however, can prove troublesome to downstream circuitry. One approach to contact bounce combines a relay with a hot-swap controller. Such controllers are increasingly popular as the means for switching system components without shutting down the system power. In **Figure 1**, a relay contact replaces the pin of a mechanical connector. The drive circuit drives the relay closed, and that relay closure connects the input of the hot-swap circuitry to the power supply: 28V, in this case. The hot-swap controller, IC_1, keeps the p-channel MOSFET, Q_1, off for a minimum of 150 msec after the input supply reaches a valid level. That delay allows ample time for contact bounce in the relay to subside. After the 150-msec delay, IC_1 drives the MOSFET gate such that the output voltage slews at 9V/msec. This controlled ramp rate minimizes the inrush current, thereby reducing stress on the power supply, the relay, and capacitors downstream from the hot-swap controller.

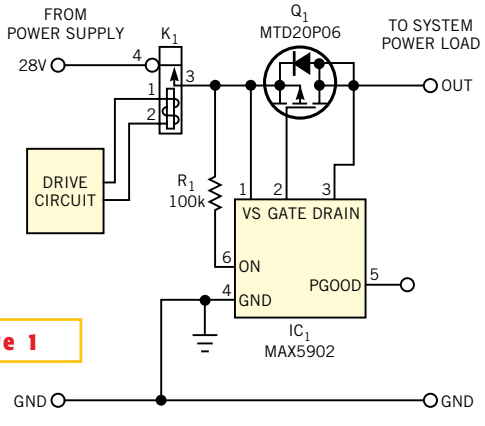


Figure 1 A hot-swap controller IC and external MOSFET removes contact bounce from relay K_1.

An example of relay contact bounce shows three bounces with an inrush-current peak of almost 30A (**Figure 2**). The top trace is output voltage at 10V/division, the lower trace is input current at 5A/division, and the output load is 54Ω in parallel with 100 µF. Use of the **Figure 1** circuit under these conditions yields a better picture (**Figure 3**). The delayed rise in output voltage is clearly visible, with no hiccups arising from contact bounce. The input current shows much less variation, peaking under 1.5A before settling to a steady-state value of 500 mA.□

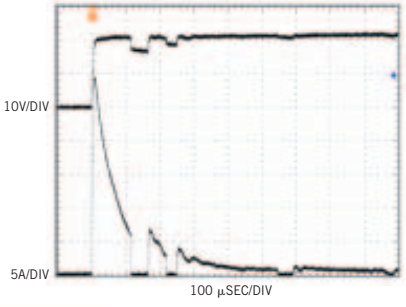


Figure 2 The mechanical relay, K_1, by itself exhibits contact bounce on closure as shown.

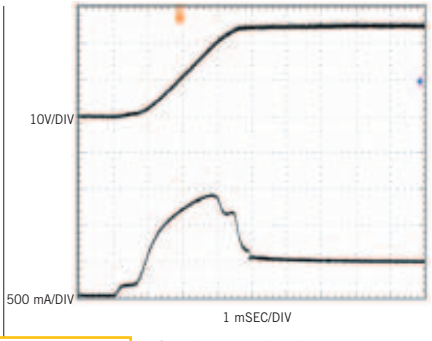


Figure 3 The Figure 1 circuit removes relay-contact bounce and reduces inrush current.

Log-ratio amplifier has six-decade dynamic range

Reza Moghimi, Analog Devices, San Jose, CA

You need optical-power monitoring to guarantee overall system performance in fiber-optic communication systems. Logarithmic-signal processing can maintain precise measurements over a wide dynamic range. The wide-dynamic-range signal undergoes compression, and the use of a lower resolution measurement system then saves cost. As an example of this technique, consider a photodiode with responsivity of 0.5A/W that converts light energy to a current of 100 nA to 1 mA. With a four-decade dynamic range and 1% error, the required measurement resolution is 0.01×10^{-4}, or 1 ppm. This measurement requires a 20-bit ADC. Instead, you can compress this input to a 0 to 4V range using a log-ratio amplifier and then use a 10-bit ADC, substantially reducing the system cost. Programming the reference current allows shifting the output voltage to the desired level. You can customize and use the circuit in **Figure 1** in applications involving unusual combinations of dynamic range; input signal, such as voltage or current; polarity; and scaling; or operations such as log products and ratios. Log-ratio amplifiers find applications in wide-dynamic-range ratiometric measurements, which measure an unknown signal against a variable-current reference. The transfer function of the circuit in **Figure 1** is:

$$V_{OUT} = K \times \log_{10}\left(\frac{I_{IN}}{I_{REF}}\right);$$

$$K = -2.303\frac{(R_T + R_2)\times V_T}{R_{(T)}},$$

where K is the output scale factor, I_{IN} is the current that the photodiode generates, V_T is a temperature-dependent term (typically, 26 mV at 25°C and proportional to absolute temperature), and I_{REF} is the reference current. $V_{OUT}=0$ when $I_{IN}=I_{REF}$. For proper operation, I_{IN}/I_{REF} should always be greater than 0. The output of the log-ratio circuit can be positive, negative, or bipolar, depending on the ratio of I_{IN}/I_{REF}. The 4V full-scale input range of the ADC sets the 4-mA full-scale input-current range. Programming I_{REF} to a value of 40 to 600 µA places the output in the middle of the measurement range.

The components give an output-scale factor of −1. This circuit has an output defined over a range of 4.5 decades of signal current, I_{IN}, and 1.5 decades of reference current, I_{REF} (limited by the load-driving capability of the reference for a total six-decade range. For most applications, you would use only a portion of the entire six-decade range. By determining the range of the expected input signals and computing their ratios, you can use the equations to predict the expected output-voltage range. You can assign I_{REF} and I_{IN} to match device performance to the current range, but you should observe polarity.

A log amplifier generally depends on the nonlinear transfer function of a transistor. The general transfer function of a log amplifier is related to I_S and V_T, which both depend on temperature. I_S is the

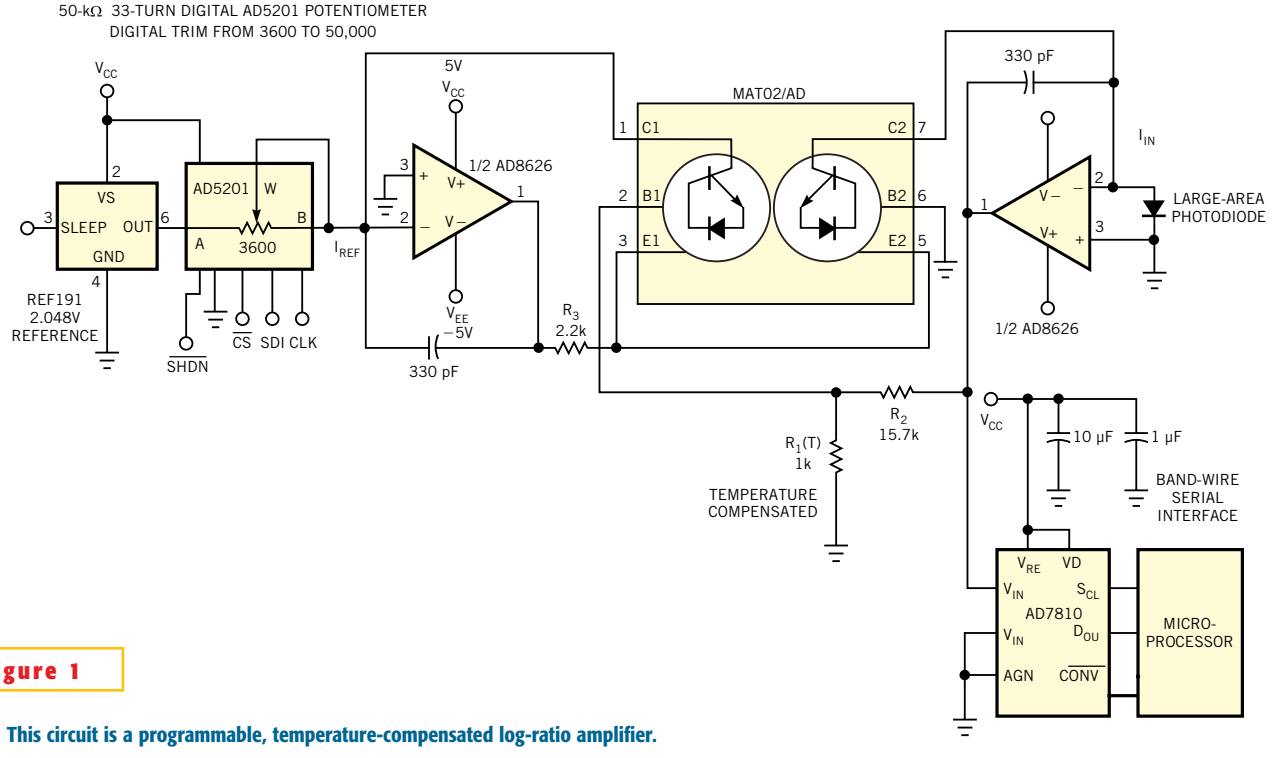
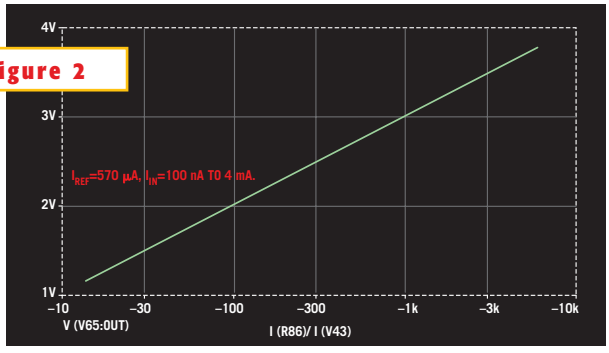


Figure 1

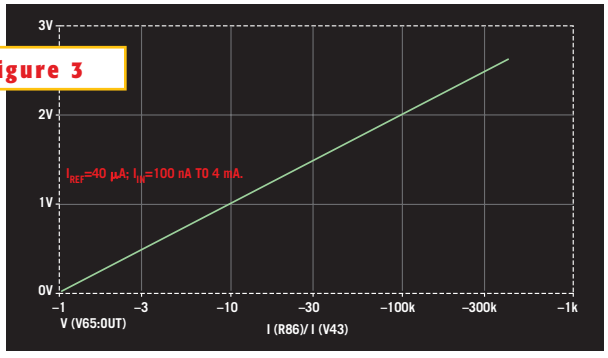
This circuit is a programmable, temperature-compensated log-ratio amplifier.

Figure 2



V_{OUT} has I_{REF} programmed to full scale of 570 µA.

Figure 3



V_{OUT} has I_{REF} programmed to zero scale of 40 µA.

transistor's collector saturation current, and V_T is the transistor's "thermal voltage." To overcome this temperature dependency, this design uses a matched pair of MAT02 transistors to cancel the I_S temperature drift and a temperature-sensitive resistive voltage divider to compensate for the temperature coefficient of V_T. The heart of the I_{REF} generator is a REF191. You adjust its output with an AD5201 digital potentiometer. This modification allows you to program the reference current in 33 steps, from 40 to 600 µA.

The combination of the REF191 and the AD5201 provides a current source that is stable with respect to time and temperature. For higher resolution, you can use the 1024-position AD5231. The AD8626 is a dual precision-JFET-input amplifier with true single-supply operation to 26V, low power consumption, and rail-to-rail output swing, allowing a wide dynamic range. Its output is stable with capacitive loads in excess of 500 pF. **Figures 2** and **3** show the transfer function of the log-ratio amplifier at the input of the ADC. The output is limited to 0 to 4V to match the unipolar input-voltage range of the AD7810 ADC.□

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VCXO makes inexpensive dual-clock reference

Said Jackson, Equator Technologies Inc, Campbell, CA

THIS DESIGN IDEA describes an inexpensive circuit to generate two extremely high-quality, crystal-clock-reference-signals, one of which is a PWM-controlled VCXO (voltage-controlled crystal oscillator) clock signal (**Figure 1**). The design also includes circuitry to statically switch and hold the VCXO at its nominal fixed frequency of operation (equivalent to 50% PWM) without requiring any external PWM stimulus. Most digital audio/video microprocessor-based systems today require several independent clocks with low jitter and the potential adjustability a VCXO provides. The described circuit replaces two expensive monolithic VCXO and crystal oscillators at a fraction of their cost and provides much higher quality output signals than the monolithic solutions can generate, especially at the control limits of the VCXO (±100% deviation). The circuit generates signals with higher stability, much lower jitter, lower operating voltage (3.3 versus 5V) and a wider VCXO pull range than comparable monolithic approaches at less than one-third of their cost.

You can use the circuit in a wide variety of applications; the indicated component values make it a perfect fit for a digital audio/video system, such as a digital video recorder, digital camera, or set-top box. The circuit is well-suited to single-chip, media-processing applications that require adjustability, low cost, and low-jitter performance, such as systems based on Equator's (www.equator.com) broadband-signal processors. These types of systems generally require a fixed frequency, such as 25 or 33 MHz, for the processor subsystem (Ethernet, PCI bus, for example) and an adjustable 27-MHz reference clock for the audio/video reference subsystem. A PLL system generally controls the 27-MHz reference clock. (This PLL is usually implemented in software with PWM outputs from the microprocessor controlling the 27-MHz clock's deviation.) This approach guarantees a correct synchronization of the audio and the video data streams to each other and the broadcast source. The clock requires ±50-ppm adjustability, and the circuit in **Figure 1** provides more than ±70 ppm. The circuit suits high-volume manufacturing, the highest quality signal (lowest jitter), and the lowest production cost.

The design incorporates several novel circuit features, such as both overtone- and harmonic-crystal operation, use of inexpensive voltage-controlled capacitors (varactor diodes), a single 3.3V power-supply operating voltage, and a selectable 50%-duty-cycle, 27-MHz-operation, fixed-frequency mode. The fixed-frequency mode allows operation at 27 MHz without the PLL-PWM circuit's having to provide a 50% duty cycle, potentially freeing up hardware and software resources in the microprocessor that usually generates the PWM signal. This mode is usually invoked when the audio/video signals are generated internal-

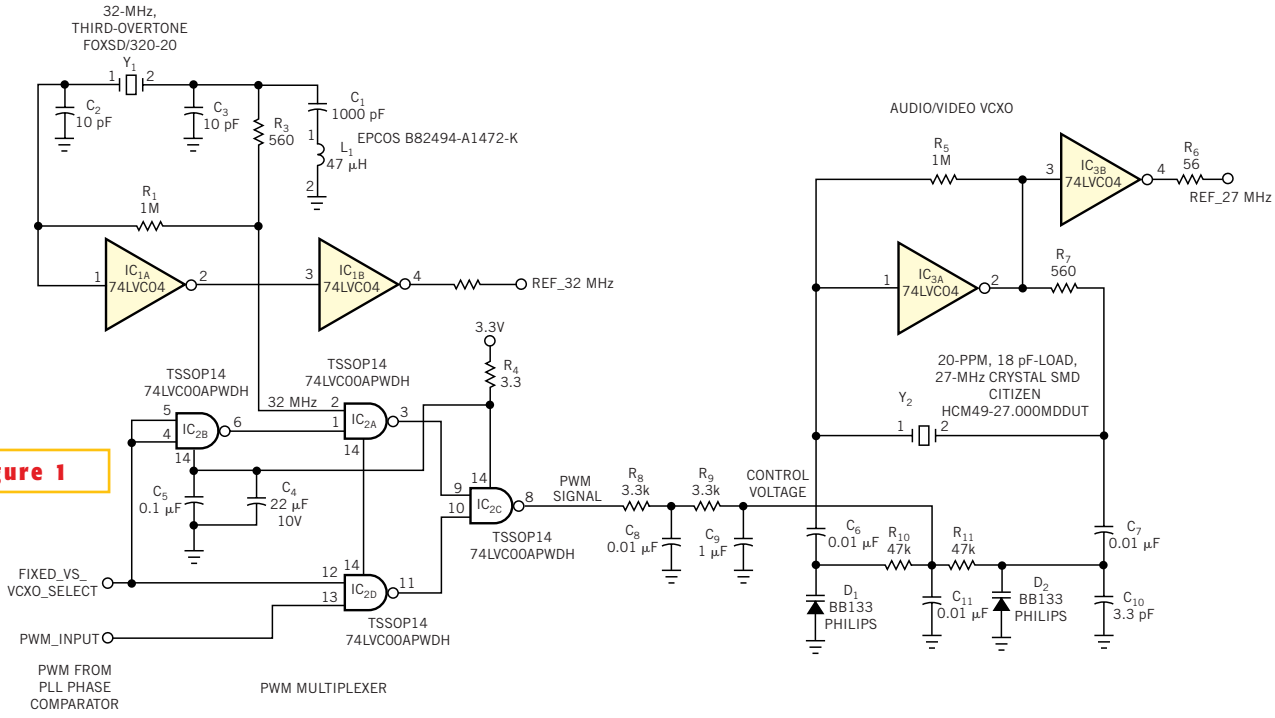


Figure 1

This circuit, ideal for A/V applications, generates two high-quality clock-reference signals.

ly to the system, such as when playing back from a hard drive, and audio/video synchronization to an external source is unnecessary.

The circuit includes IC_1, a 32-MHz, PCI-based fixed-frequency reference clock; IC_2, a PWM multiplexer; and IC_3, a 27-MHz VCXO clock. A Fox (www.foxonline.com) 32-MHz, third-overtone crystal serves to generate both the PCI reference clock and the 50%-duty-cycle reference for the fixed-frequency mode. A third-overtone, 32-MHz part is less expensive and more mechanically robust than a 33-MHz, fundamental-mode crystal at the expense of running the PCI clock slightly slower. The tank circuit around inductor L_1 and capacitors C_1 and C_3 prevent the crystal from oscillating at its fundamental mode of approximately 11 MHz. This tank circuit works by creating an LC series-resonant circuit between L_1 and C_3 that has natural resonance at approximately 24 MHz, which is approximately 75% of the desired 32-MHz frequency. Note that C_1 is large enough to have no effect on this tank circuit's resonance frequency; it merely acts as a dc blocker for inductor L_1. One thing to avoid is to connect this tank circuit to the input side of inverter IC_{1A}. Connecting it to the input side of IC_{1A} could potentially create a resonant RC circuit with resistor R_1 and capacitor C_1 acting as the RC components. This circuit could oscillate at less than 1 kHz, a frequency at which L_1 would effectively be a short circuit, and crystal Y_1 would be an open circuit. Placing C_1 and L_1 on the output side of IC_{1A} prevents this spurious-oscillation mode.

By tuning L_1 and C_3, you can adjust the circuit to oscillate at a frequency higher than the third overtone. Oscillation at the fifth, seventh, or even ninth overtone is possible and is limited only by the performance of IC_{1A} and the parasitic capacitance. The 32-MHz PCI reference-clock output also serves as a 50%-duty-cycle reference for the VCXO when the VCXO is operating in its fixed-frequency, 27-MHz mode. Multiplexer IC_2 selects either this 32-MHz, 50% PWM clock signal or the PWM clock signal from a PLL phase comparator (usually implemented in the microprocessor and not shown in the schematic) to set the VCXO to its fixed-frequency mode. The advantage of using the PCI clock for this feature is that traditional circuits would have to generate an analog one-half-V_{DD} voltage and use an analog multiplexer to set the VCXO at its nominal frequency. Thus, this design avoids the necessity of using accurate and expensive analog circuitry and also generates a reference signal with much higher immunity to temperature, for example, than analog approaches could provide.

Digital multiplexer IC_2 forwards one of two PWM signals to the VCXO based on the state of the fixed-versus-VCXO selected input signal. The PWM-input signal serves as the PWM reference input to the VCXO if the select pin is high, and the design uses the 50%-duty-cycle PWM signal from the PCI clock circuit if the select pin is low. The design uses a 74LVC00 chip as a multiplexer because of its ready availability and low cost. IC_{2C} buffers the PWM signal, and the cascaded RC filter comprising R_8, R_9, C_8, and C_9 then low-pass-filters the signal. The analog-voltage stability of the VCXO control voltage at the output of this RC filter depends on the quality of the V_{DD} supply to IC_{2C}. IC_2 receives its 3.3V power through an RC filter: R_4 with C_4 and C_5. IC_2 with R_8, R_9, C_8, and C_9 thus form a highly accurate D/A converter.

The VCXO's lowpass filter uses a cascaded design, because stray 32-MHz noise could pass across the small parasitic capacitance inherent in R_8 into the analog VCXO-control voltage. Cascading also has the advantage of filtering noise with 12 dB of attenuation per octave for frequencies greater than 5 kHz, thus creating a noise-free VCXO control voltage. The 27-MHz audio/video VCXO circuit uses a fundamental-mode crystal that varactor diodes D_1 and D_2 load with adjustable capacitance. These backbiased diodes' junction capacitance depends highly on the bias voltage. Larger bias voltages lower their capacitance, thus lowering the load across the crystal and increasing its oscillation frequency. Diodes D_1 and D_2 find use in many tuners and are widely available. Capacitors C_6 and C_7 again function as dc blockers.

The adjustment range of the VCXO is approximately 27 MHz±2 kHz, which calculates to approximately ±74 ppm. The circuit is stable with very low jitter throughout its entire 0 to 100% VCXO-adjustment range. You can use the VCXO subcircuit by itself to generate a spread-spectrum clock for EMI compliance. You drive the VCXO voltage or PWM duty cycle from 0V (0%) to 3.3V (100%) with a triangular-shaped drive signal. The frequency of the triangular wave must be below the PWM RC filter's cutoff frequency of 24 Hz to be effective. The oscillator circuit's jitter depends on the power-supply quality of IC_1, IC_2, and IC_3 and on the noise inside these chips. To avoid crosstalk between 32 MHz and 27 MHz, the design uses two chips. Implementing buffers IC_{1B} and IC_{3B} with separate chips, thus separating the power-supply loading from the sensitive buffers, IC_{1A} and IC_{3A}, could further reduce jitter. With independent clock buffers and a low-noise power supply, this circuit has exhibited a maximum cycle-to-cycle jitter of less than the 60-psec limitation of the HP54720D oscilloscope that measures it. This figure betters the jitter characteristics of popular crystal oscillators and VCXO chips available for consumer applications. It also does not suffer from unstable operation at its adjustment margins (operating at ±100% deviation), as designers commonly encounter with monolithic components. Another added benefit is that it achieves its ±74-ppm adjustment range with only a single 3.3V power supply, whereas monolithic approaches usually require a 5V power supply and control voltage. Finally, it offers all this performance at a total price of less than $1.40 in large quantities by using only commonly available, off-the-shelf components. This figure compares to $3 to $6 parts cost with monolithic approaches.□

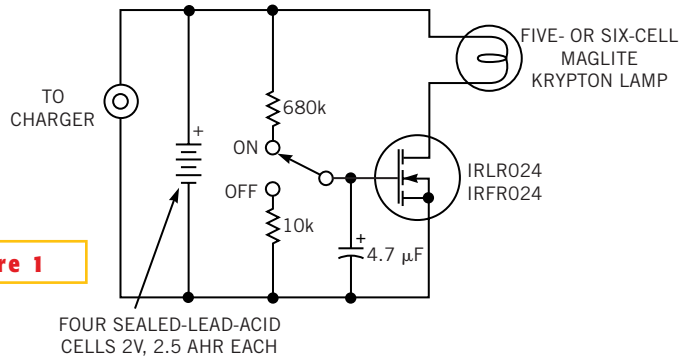
Edited by Bill Travis

Rechargeable flashlight obsoletes lantern battery

Fran Huffart, Linear Technology, Milpitas, CA

This Design Idea describes a high-intensity, rechargeable flashlight system that you can build from a 6V lantern-type flashlight. The rechargeable battery comprises four 2V, 2.5-Ahr (ampere-hour) SLA (sealed lead-acid) cells, similar in size to a standard D-sized battery. SLA cells are especially well-suited to powering flashlights because of their low self-discharge rate. NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) cells can lose as much as 1% of their charge per day, compared with less than 0.2% per day for SLA cells. SLA cells are also easy to charge and can withstand abuse. The flashlight in this design uses a krypton high-intensity lamp. Maglite (www.maglite.com) makes this lamp as a replacement lamp for its line of flashlights. The lamps are extremely bright; have a standard miniature-flange-base, built-in lens; and are available in five- or six-cell versions. (Manufacturers typically rate flashlight lamps by the number of alkaline cells the flashlight uses.) The lamp's operating voltage is approximately 1.25V per cell, which makes the lamp voltage of a six-cell lamp equal to 7.5V. This design uses a six-cell lamp for this flashlight, although you could also use a five-cell, 6.25V lamp. A five-cell lamp provides approximately 30% more light output but has a shorter lamp life. To increase lamp life, this flashlight includes the soft-start circuit in **Figure 1**.

Figure 1

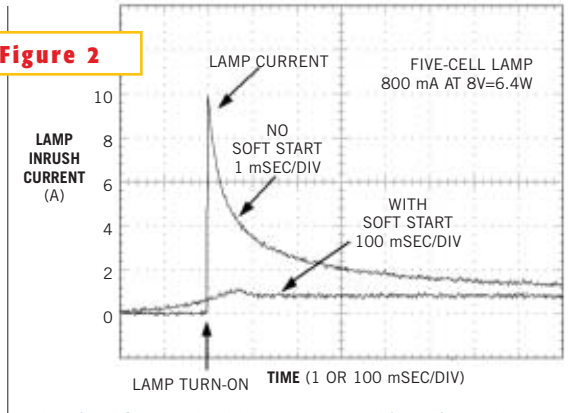


This soft-start circuit reduces inrush current, thereby prolonging lamp life.

Incandescent lamps inherently draw large start-up currents because of the filament's relatively low resistance when it is cold. A tungsten filament's resistance is typically 10 times lower when cold than it is when at normal operating temperature. When the full battery voltage suddenly hits a cold filament, the inrush current is typically 10 times the normal operating current, and this instant is when a lamp is likely to fail. Adding a soft-start circuit nearly eliminates this large inrush current, allowing for a higher power lamp and reducing the probability of the lamp's failure at turn-on. The soft-start circuit consists of an n-channel MOSFET in series with the lamp, which ramps the lamp voltage up at a controlled rate to reduce the inrush current. A gate-to-source capacitor controls the ramp speed. The lamp turns on in approximately 2 sec. **Figure 2** shows the dramatic reduction in lamp inrush current when you use the soft-start circuit.

The charger is a 200-kHz step-down switching regulator using current-limited constant voltage to charge the battery (**Figure 3**). When a discharged battery connects to the charger, the charge cycle starts in a 1A constant-current mode. As the battery accepts charge, the battery voltage increases until it reaches the programmed charge voltage of 2.5V/cell (10V total). At this point, the charge cycle enters constant-voltage mode. During constant-voltage mode, the charge current drops exponentially. When the charge current reaches approximately 10% (100 mA) of the programmed current, the charge voltage drops to a float voltage of 2.35V/cell

Figure 2



Using the soft-start circuit in Figure 1 provides a dramatic decrease in inrush current.

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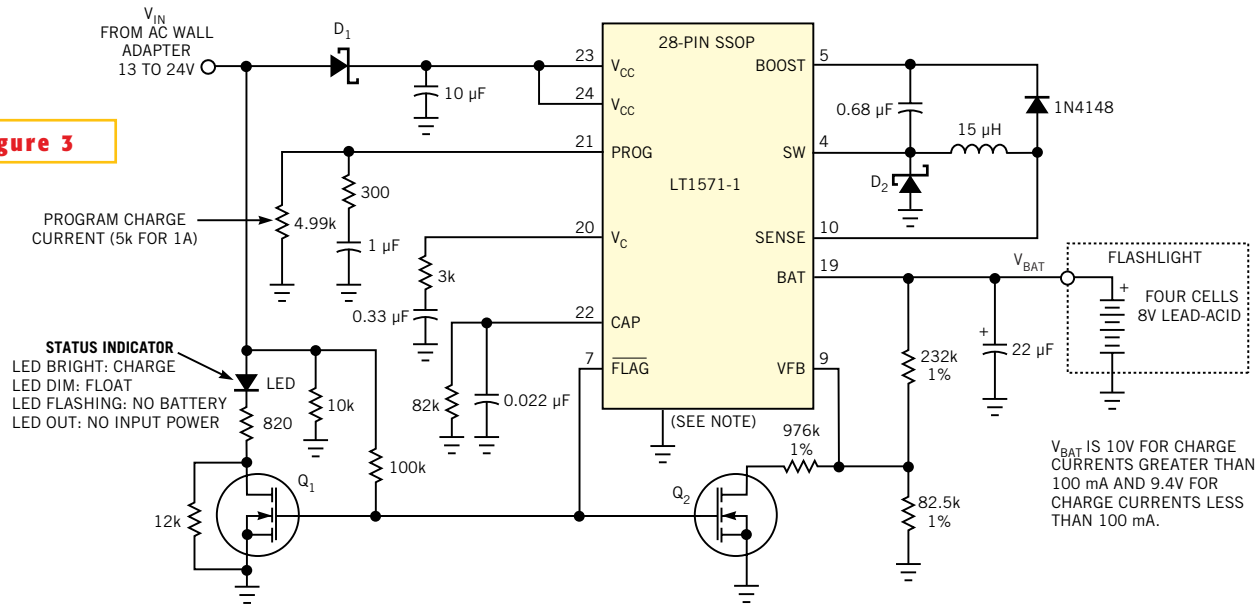
Figure 3



NOTES:
GROUND PINS 1, 2, 3, 11, 12, 13, 14, 15, 16, 17, 18, 25, 26, 27, AND 28 TO GENEROUS AMOUNTS OF PC-BOARD COPPER FOR BEST THERMAL AND ELECTRICAL PERFORMANCE.
Q_1 AND Q_2 ARE VN2222s, OR 2N7002s.

D_1 AND D_2 ARE 1A ,30V SCHOTTKY DIODES.

This battery charger uses current-limited constant voltage to charge the lead-acid cells in the flashlight.

(9.4V total). This dual-voltage approach provides a faster charge and also provides an LED indication when the battery is nearly fully charged. The charger keeps the battery at this float voltage, thus keeping the battery in a fully charged condition. You can leave the charger indefinitely connected to the battery without damage to the battery, although battery damage can result if it is fully discharged—when the battery voltage is less than 1.8V/cell—either through use or self-discharge. The $\overline{\text{FLAG}}$ pin is an open-collector output that indicates when the charge current has dropped to approximately 10% of the full programmed charge current.

A wall adapter with an output from 13V, 1A to 26V, 0.5A provides power to the charger. This design uses all surface-mount components to reduce the overall size of the charger. The pc-board layout should include wide ground traces that expand to larger copper areas to minimize the possibility of overheating the IC. The flashlight housing features a 3- to 4-in. reflector and has a handle on top; it is readily available from Radio Shack (www.radioshack.com) and other electronics outlets. The light is designed for a 6V lantern battery, but this design replaces the lantern battery with four D-sized, SLA cells. The cells leave enough room for the soft-start circuitry. Other modifications include replacing the switch with a high-quality SPDT switch and soldering all the connections for increased reliability. A dc power jack connects the flashlight to the charger.□

Single cell flashes white LED

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

Many portable appliances and other products that must operate from a single cell are restricted to working at very low voltages. It is thus difficult to drive white LEDs that typically have a forward voltage of 3 to 5V. The ability to flash the LED with a supply voltage as low as 1V presents additional complications. The circuit in the **Figure 1** provides a discrete approach to these problems and allows a white LED to flash at a rate set by an RC time constant. Components Q_1, Q_2, R_3, R_4, and R_5 form a simple Schmitt trigger that, together with R_1, R_2, and C_1, controls the flashing of the LED. Q_4, Q_5, L_1, and associated components form a voltage booster that steps up the single-cell voltage, V_S, to a level high enough to drive the LED. Transistor Q_3 functions as a switch that gates the booster on and off at a rate determined by the Schmitt-trigger section.

To understand how the booster section works, assume that Q_3 is fully on, such that Q_4's emitter is roughly at the battery-supply voltage, V_S. Q_4 and R_8 provide bias for Q_5, which turns on and sinks current,

I_L, through inductor L_1. The inductor current ramps up at a rate determined mainly by V_S and the value of L_1; during this time, LED_1 and series diode D_1 are reverse-biased. The current continues to ramp up until it reaches a peak value, I_{LPEAK}. Q_5 can sustain no further increase, and the voltage across the inductor at this point reverses polarity. The resulting "flyback" voltage raises LED_1's anode to a positive voltage higher than V_S, sufficient to forward-bias LED_1 and signal diode D_1. The flyback voltage is also coupled through C_3 and R_{10} to Q_4's base, thus causing Q_4 and, hence, Q_5 to turn off rapidly.

The inductor current now circulates around L_1, LED_1, and D_1, and, as the energy stored in L_1 decays, the current ramps down to zero. At this point, the inductor voltage again reverses polarity and the negative-going change is coupled through C_3, rapidly turning on Q_4 and, in turn, Q_5. Current again begins to ramp up in L_1, and the process repeats. The booster section oscillates at a rate determined by several factors. The important factors determining the rate of oscillation include the values of V_S, L_1, and R_8; the forward-current gain of Q_5; and the forward voltage of LED_1. With the component values in the **figure**, the oscillation frequency is typically 50 to 200 kHz. On each cycle, a pulse of current with a peak value equal to I_{LPEAK} flows through LED_1 and, because this scenario occurs thousands of times every second, LED_1 appears to be continuously on.

The low-frequency oscillator formed around the Schmitt trigger turns the booster section on and off at a low rate. To understand how this works, assume that Q_1 is off and Q_2 is on. Provided that Q_2 has reasonably large forward-current gain, you can ignore the effects of its base current and say that V_S and the R_3-R_5 voltage divider set Q_2's base voltage, V_{B2}. With the values of R_3 and R_5 in **Figure 1**, V_{B2} is approximately 800 to 900 mV when $V_S = 1V$. This voltage produces approximately 300 to 400 mV across R_4, resulting in a collector current of at least 15 µA in Q_2 with $R_4 = 20\ k\Omega$. Q_2's collector current provides base drive for Q_3, which saturates, turning on the booster section and illuminating LED_1. When LED_1 is forward-biased, C_4 charges to a positive voltage, V_P, roughly one diode drop above V_S.

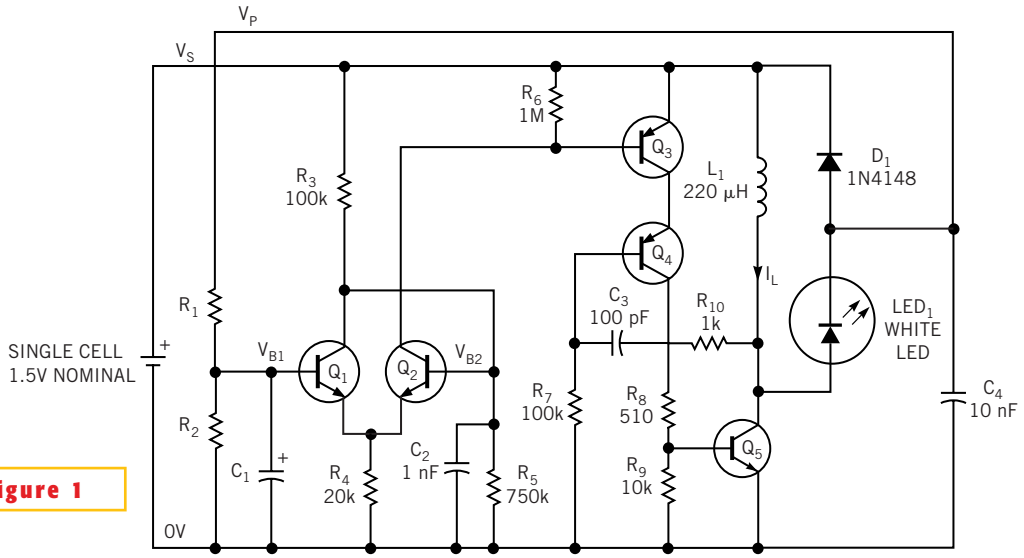


Figure 1

This circuit provides boosted voltage and flashes a white LED from a single cell.

Timing capacitor C_1 now charges via R_1 at a rate determined mainly by the values of V_P, R_1, R_2, and C_1. Provided that you carefully choose the ratio of R_1 to R_2, Q_1's base voltage, V_{B1}, eventually exceeds the quiescent level of V_{B2} (roughly equal to the Schmitt trigger's upper threshold voltage, V_{TU}), causing Q_1 to turn on and Q_2 to turn off. At this point, Q_3 also turns off, thereby disabling the booster section and turning off LED_1.

With LED_1 off, V_P rapidly decays, and C_1 begins to discharge at a rate determined mainly by the values of R_2 and C_1 and by Q_1's base current. The LED remains off until V_{B2} has fallen below the Schmitt trigger's lower threshold voltage, V_{TL}, at which point Q_1 turns off, Q_2 turns on, and the booster section again activates, illuminating LED_1. Provided that R_1, R_2, and C_1 are large enough, LED_1 can flash at a low rate. For example, if R_1 and R_2 have values of approximately 1 MΩ each and C_1 has a value of 1 µF or greater, a rate of less than one flash per second is possible. Remember, however, that R_1 and R_2 form a voltage divider that sets Q_1's base voltage, V_{B1}; therefore, R_2 must be sufficiently larger than R_1 to ensure that V_{B1} can cross the Schmitt trigger's upper threshold voltage as C_1 charges. With this fact in mind, you can with some trial and error fairly easily find the optimum values of R_1, R_2, and C_1 necessary for a given flash rate.

The value of V_P significantly influences the charging and discharging of C_1, and V_P's value hence varies according to the prevailing battery supply voltage, V_S. However, changes in V_{B2}, which also varies with V_S, somewhat balances this dependence. Nevertheless, the flash rate and duty cycle do vary somewhat as the battery voltage falls. For example, with $R_1 = 2.2\ M\Omega$, $R_2 = 10\ M\Omega$, and $C_1 = 1\ \mu F$, the test circuit's flash rate at $V_S = 1.5V$ is approximately 0.52 Hz with a duty cycle of 66%. With a V_S of 1V, the flash rate increases to approximately 0.75 Hz but with a lower duty cycle of 44%. The Schmitt-trigger thresholds, V_{LT} and V_{TU}, are typically approximately 0.7V and 1.2V at $V_S = 1.5V$, falling to approximately 0.6V and 0.8V when V_S is 1V.

The LED's intensity is proportional to

its average forward current and is thus determined by the peak inductor current, $I_{L\text{-}PEAK}$, and by the duration of the current pulse through the LED. Provided that L_1 is properly rated such that it does not saturate, the peak current depends largely on the maximum collector current that Q_5 can sustain. For a given supply voltage, this figure depends primarily on Q_5's forward-current gain, and on the value of R_8 that you can select to give optimum LED brightness at the lowest supply voltage. Experiment with different values of R_8 to get the best intensity for a given LED type. Take care, however, that the peak current does not exceed the LED's maximum current rating when V_S is at a maximum. The actual value of L_1 is not critical, but values in the range 100 to 330 µH should provide good performance and reasonable efficiency. The transistor types in the circuit are not critical; the test circuit works well with general-purpose, small-signal devices having medium to high current gain. If possible, select low-saturation types for Q_3, Q_4, and Q_5. C_2 is not essential to circuit operation but helps to decouple any switching noise at Q_2's base.

C_4 acts as a charge reservoir and ensures that R_1 can charge C_1 from a stable voltage source (V_P) when LED_1 is on. Because the charging current is likely to be low, C_4 can be fairly small; a value of 10 nF should be adequate. Note that C_4 must connect to the junction of D_1 and LED_1 as shown, rather than being charged, via a rectifying diode, from the flyback voltage at Q_5's collector. The reasons for this caveat are, first, that this approach ensures that V_P is only a diode drop above V_S, thereby minimizing the value of R_1 necessary for a given C_1 charging current. Also, and more important, this approach places the forward voltage of the LED in the path from V_S through L_1 and R_1 to Q_1's base. Because the forward voltage of a white LED is usually at least 3V, this connection prevents Q_1 from being turned on via this route, which could otherwise cause the circuit to lock in the "off" state.

At first sight, it might appear that you can turn the booster section on and off by gating current to Q_4's base, thus obviating the need for Q_3. However, under certain conditions, once you activate the booster section, the feedback to Q_4's base via C_3 and R_{10} is sufficient to maintain oscillation without feeding any dc bias to Q_4's base. Therefore, the only reliable way to gate the booster on and off is via Q_3, as shown. The test circuit starts up and operates with V_S as low as 0.9V, although the LED is dim at this voltage. The LED's intensity is good at V_S=1.5V (equivalent to a fully charged alkaline cell) and remains acceptable with V_S as low as 1V. The circuit should find applications in toys, security devices, miniature beacons, and any other products that must provide a flashing visual indication while operating from a single cell.□

Hot-swap controller handles dual polarity

Dan Meeks, Texas Instruments, Manchester, NH

Some applications require a hot-swap controller, a circuit-breaker function, or both for dual-polarity, dc-input power-supply rails. In some hot-swap cases, the requirement is based only on inrush-current considerations. Control of the inrush current is necessary to eliminate connector stress and glitching of the power-supply rails. Other applications may have issues when one of the supplies fails for some reason. A good example is a bias supply for a gallium-arsenide FET amplifier. If you remove the negative gate bias, then you must also remove the positive drain supply; otherwise, the device may destroy itself because of the resulting high drain current. You can meet both these requirements by using a single-channel, hot-swap controller.

The circuit in **Figure 1** uses a TPS2331, IC_1, in a floating arrangement. The circuit references the IC's ground to the negative input voltage. If the voltage on the positive rail is too low or the voltage

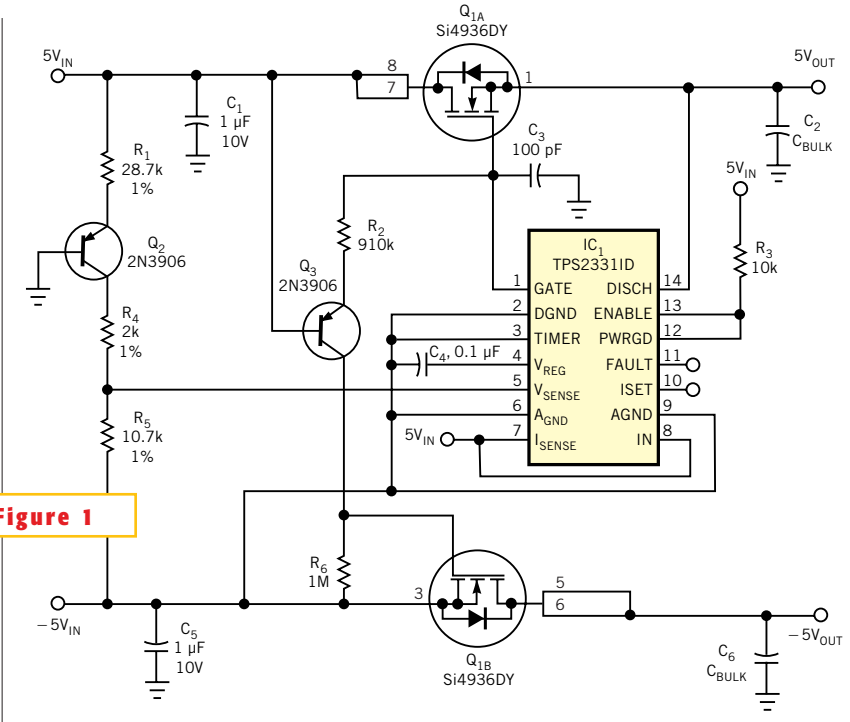
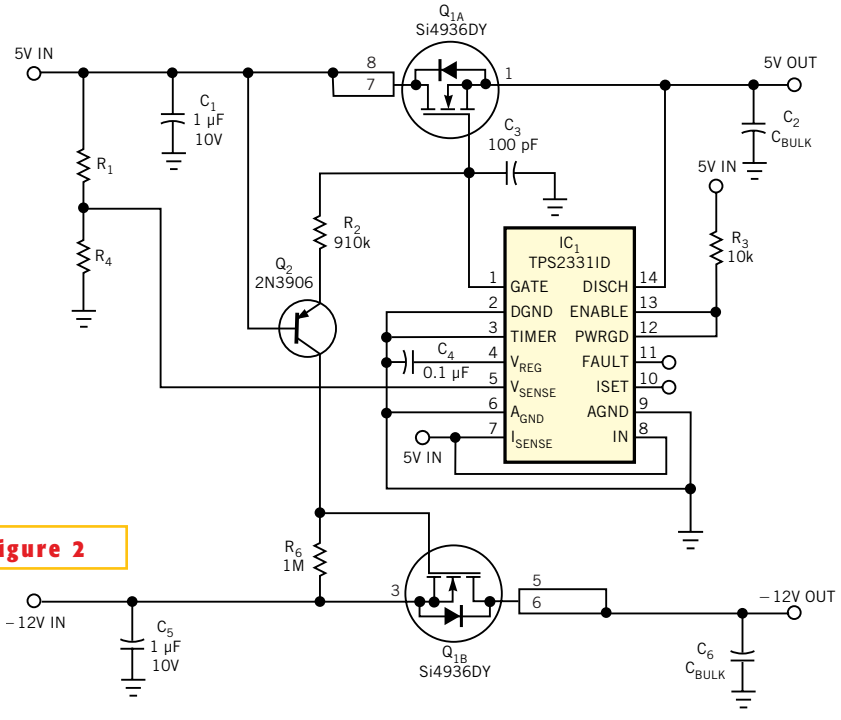


Figure 1

This circuit is a dual-polarity voltage sequencer for low-voltage applications.

on the negative rail is too high, the circuit cannot attain the 1.225V threshold at the V_{SENSE} pin, and the IC turns off. The V_{SENSE} pin incorporates approximately 30 mV of hysteresis to ensure a clean turn-on with no chatter.

When both supplies are beyond their respective thresholds, IC_1 turns on, providing a controlled-slew-rate ramp-up of the two FETs. Note that the circuit uses only n-channel FETs, which have lower on-resistance for a given size and cost than p-channel devices. To turn on Q_{1A} on, the TPS2331 has a built-in charge pump that generates a voltage above the positive rail, thus enhancing the FET. As the gate voltage builds, Q_3 acts as a linear level translator, so that Q_{1B} also ramps on. The turn-on speed is a function of the TPS2331's 14-µA output current and the value of C_3. The design uses the FETs based on the maximum resistance allowed in the dc path and the FETs' power-dissipation figures. You can use virtually any size FET, depending on the current you want to control. Take care that the total voltage span across the TPS2331 does not exceed the maximum rating of 15V. If IC_1 does not float between the input rails, the negative input may be larger.



NOTE: SELECT R_1 AND R_4 TO SET THRESHOLD.

Figure 2 This variation on Figure 1's circuit can handle higher voltages.

Figure 2 shows such an application, in which 5V and −12V are the input supplies. The main requirement is that the level-shifting transistor, Q_3, be able to handle the higher voltage. This circuit also allows you to use a positive input voltage as high as IC_1's maximum rating of 15V.□

Temperature monitor measures three thermal zones

Susan Pratt, Analog Devices, Limerick, Ireland

You can use an ADT7461 single-channel temperature monitor; an ADG708 low-voltage, low-leakage CMOS 8-to-1 multiplexer; and three standard 2N3906 pnp transistors to measure the temperature of three separate remote thermal zones (**Figure 1**). Multiplexers have resistance, R_{ON}, associated with them; the channel matching and flatness of this resistance normally result in a varying temperature offset. This system uses the ADT7461 temperature monitor, which can automatically cancel resistances in series with the external temperature sensors, allowing its use as a multichannel temperature monitor. The resistance automatically cancels out, so R_{ON} flatness and channel-to-channel variations have no effect. Resistance associated with the pc-board tracks and connectors also cancels out, allowing you to place the remote-temperature sensors some distance from the ADT7461. The design requires no user calibration, so the ADT7461 can connect directly to the multiplexer. The ADT7461 digital temperature monitor

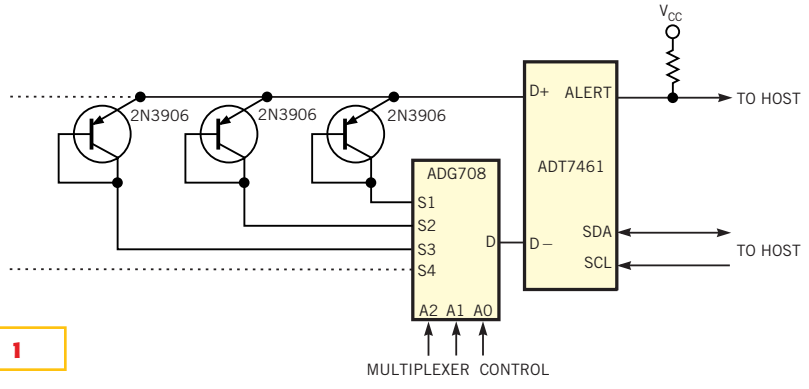


Figure 1 This system measures the temperature of three remote thermal zones.

can measure the temperature of an external sensor with ±1°C accuracy. The remote sensor can be a monolithic or a discrete transistor and normally connects to the D+ and D− pins on the ADT7461. In addition to the remote-sensor-measurement channel, the ADT7561 has an on-chip sensor.

The diode-connected transistors have emitters that connect and then connect to the D+ input of the ADT7461, and each of the base-collector junctions connects to a separate multiplexer input (S1 to S3). You connect the selected remote transistor to the D− input on the ADT7461 by addressing the multiplexer, which address bits A2, A1, and A0 digitally control. The ADT7461 then measures the temperature of whichever transistor is connected through the multiplexer. The ADT7461 measures the temperature of the selected sensor without interference from the other transistors. **Figure 2** shows the results of measuring the temperature of three remote temperature sensors. The sensor at address 000 is at room temperature, the sensor at address 001 is at a low temperature, and the sensor at address 010 is at a high temperature. When you select no external sensor, the "open-circuit" flag in the ADT7461 register activates, and the Alert interrupt output asserts. You can expand the system to include as many external temperature sensors as your design requires. The limiting factor on the number of external sensors is the time available to measure all temperature sensors. If your design requires two-wire serial control of the multiplexer, you can use an ADG728 in place of the ADG708.□

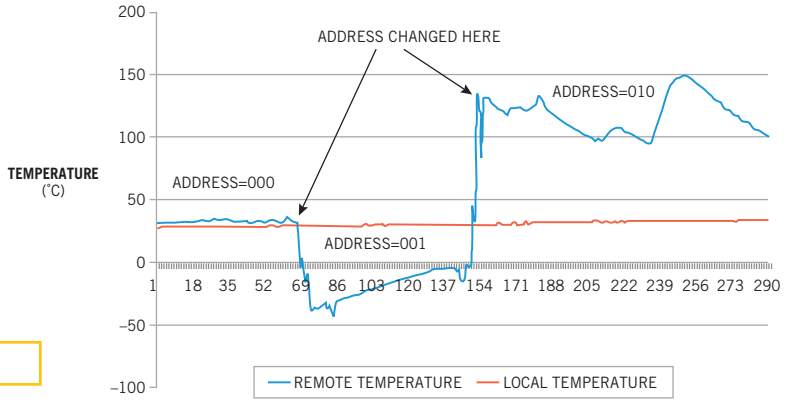


Figure 2

The system in Figure 1 measures ambient (address 000), cold (address 001), and hot (address 010) temperatures.

design ideas

Edited by Bill Travis

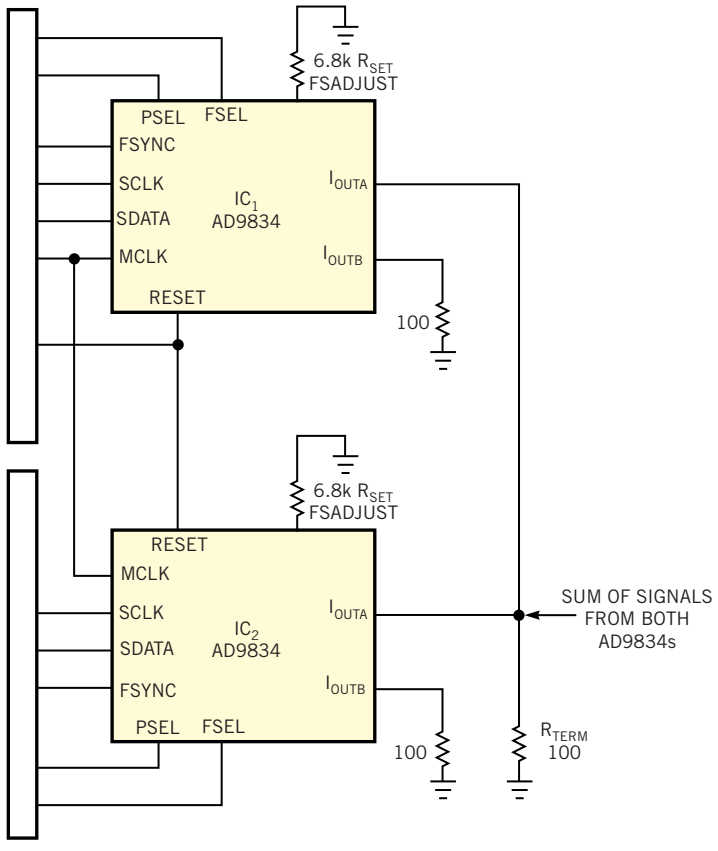
Two DDS ICs implement amplitude-shift keying

Noel McNamara, Analog Devices, Limerick, Ireland

Many communications systems, including RFID systems and cable modems, use AM (amplitude modulation). This Design Idea shows how two DDS (direct-digital-synthesis) devices can implement AM and ASK (amplitude-shift keying) over a range of frequencies. The AD9834 complete 50-MHz DDS IC (**Figure 1**) has a current output, so you can easily sum the outputs of two or more of them by connecting them to a common termination resistor. Each AD9834 has two internal phase registers, P_0 and P_1, and two internal frequency registers, F_0 and F_1 (not shown). With each AD9834 generating a sine wave at the same frequency, the amplitude of the summed signal depends on the phase of each signal. You can achieve four preset amplitude levels—or any on-the-fly level—by summing the outputs of two AD9834s.

Table 1 shows two AD9834s, IC_1 and IC_2, configured to give four output levels. P_{0A} is phase register 0 for IC_1, P_{1A} is phase register 1 for IC_1, and so on. You can select the desired output level with either the PSEL pins or with the PSEL bits in the control register. **Figure 2** shows the waveforms at the R_{TERM} summing junction for the phases used in **Table 1**. You can achieve any signal level from 0V to a full-scale voltage of approximately 600 mV by programming the phase registers with the appropriate values. Both devices use the same MCLK (master clock), and you need to synchronize them to get the correct signal levels at the R_{TERM} output. You achieve synchronization by simultaneously applying a Reset signal to both parts after programming both parts with the correct phase and frequency. You can accomplish the synchronization by applying a positive pulse to the Reset pins, or you can implement a software synchronization by setting the reset bit in the control register to one, stopping MCLK, setting the reset bit in the control register to zero, and then starting MCLK. Either method ensures that both parts simultaneously exit the reset state.

Figure 1



You can use two DDS chips to implement amplitude modulation and amplitude-shift keying.

You can easily implement 100% AM with a single AD9834 by toggling the Reset pin or the reset bit in the control register. When the part is in reset, the DAC's output is at midscale. The predetermined sine wave is available at I_{OUT} when the DDS exits reset. To calculate the magnitude of the sum of the two signals from the AD9834s, represent each signal as a rotating vector (**Figure 3**). You can easily calculate the magnitude and phase of the resulting summed vector as follows: If the length of each vector is 1, then:

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TABLE 1—THE PHASE-REGISTER CONTENTS YIELD FOUR OUTPUT LEVELS FROM THE CIRCUIT IN FIGURE 1

	Device number	Phase-register values (°)		Normalized level of summed signal	Output level with R_{TERM} = 100Ω and R_{SET}=6.8 kΩ (mV)
P_0	A	45	$P_{0A}+P_{0B}(45+180)°$	0.765	223
P_1	A	95	$P_{0A}+P_{1B}(45+210)°$	0.426	128
P_0	B	180	$P_{1A}+P_{0B}(95+180)°$	1.47	435
P_1	B	210	$P_{1A}+P_{1B}(95+210)°$	1.191	350

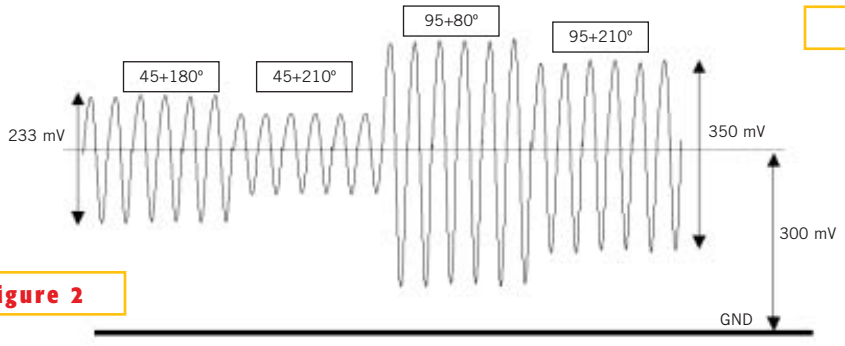
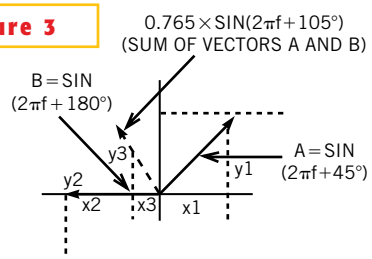


Figure 2

The waveforms at the R_{TERM} summing junction use the phases in Table 1.

Figure 3



You can calculate the magnitude of the summed signals from the DDS chips by representing each signal as a rotating vector.

- x1 = Cos(45°)=0.707: y1=Sin(45°)=0.707;
- x2=Cos(180°)=−1.00: y2=Sin(180°)=0;
- x3=x1+x2=−0.293: y3=y1+y2=0.707;
- Magnitude of resulting vector: $\sqrt{(x3)^2+(y3)^2}$=0.765;
- Phase of summed vector: 112.5° (180°−Tan^{-1}(y3/x3)).

The maximum output-voltage level that any one AD9834 can develop across the 100Ω termination resistor with R_{SET}=6.8 kΩ is 320 mV p-p. Therefore, the voltage level this example achieves is 320 mV×0.765=244.8 mV. This example shows that the phase of the resulting summed vector depends on the phase of two input vectors and may result in a phase discontinuity as the phases of the input vector change. To avoid phase discontinuity at the transition, you can set the resultant phase, P3, to a fixed angle, say 180°≥p2=360°−p1.

Sin(2πf+p1)+Sin(2πf+p2)=2Cos(0.5(p1−p2))×Sin(2πf+(p1+p2)/2).

Desired amplitude: A=2Cos [0.5(p1−p2)]; p1−p2 = 2Cos^{-1}(A/2).

Resultant phase: P3=(p2+p2)/2.

Therefore, p1=180°+Cos^{-1}(A/2), and p2=180°−Cos^{-1}(A/2) gives amplitude A with no phase shift at the transition.□

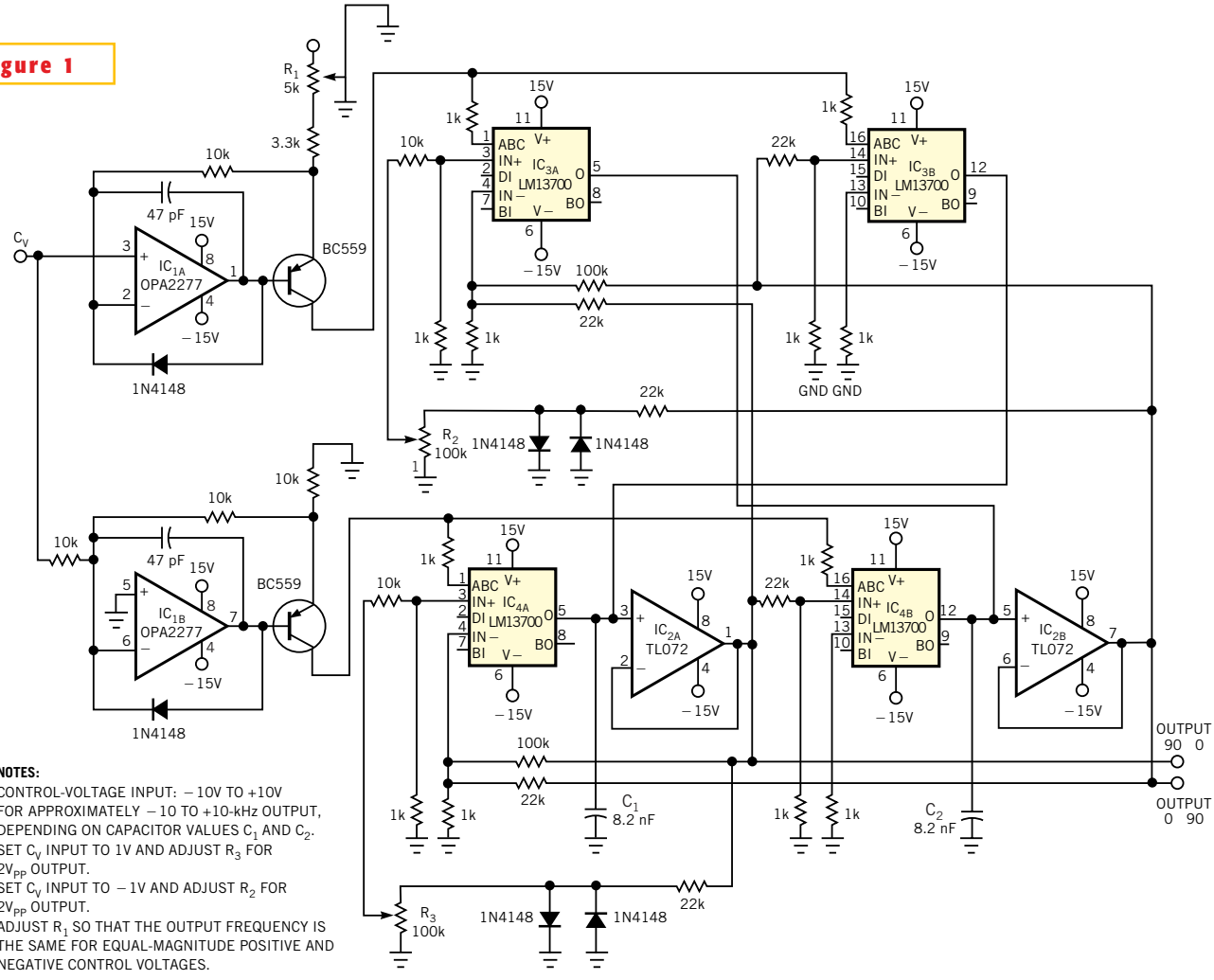
VCO produces positive and negative output frequencies

Henry Walmsley, Farnborough, UK

THE CIRCUIT IN **Figure 1** is a quadrature-output VCO that provides both positive and negative output frequencies, depending on the polarity of the control-voltage input. The circuit provides a function that designers traditionally implement in analog music-effects units, such as Bode/Moog frequency shifters. Bode/Moog shifters use fixed-beat-frequency oscillators at 20 kHz and variable sine oscillators that go higher and lower than 20 kHz. Both oscillators feed into mixers. The circuit in this design reduces the number of oscillators to one and uses no mixers (**Figure 1**). As a result, the output has fewer spurious harmonics and unharmonically related frequency products, resulting in a cleaner output overall.

The two lower transconductance amplifiers, IC_{4A} and IC_{4B}, form a standard, double-integrator bandpass/lowpass filter. The lower amplifiers are active for positive control voltages, and the upper amplifiers, IC_{3A} and IC_{3B}, are effectively turned off for lack of bias current. The upper amplifiers thus play no part in the circuit when the control voltage is positive. The TL072 op amps, IC_{2A} and IC_{2B}, are merely buffers to enable an easier choice of resistor values for IC_{4B}'s input and to avoid excessive loading of the integrator capacitors. The resistor values set the Q (quality factor) to exceed unity. Positive feedback from the bandpass output to the noninverting input makes the filter oscillate. Adjusting the R_3 trimmer allows you to adjust the output amplitude and lets you set the drive to the diodes at a level that ensures oscillation but minimizes distortion. This fairly standard configuration yields quadrature outputs

Figure 1



NOTES:
CONTROL-VOLTAGE INPUT: −10V TO +10V
FOR APPROXIMATELY −10 TO +10-kHz OUTPUT, DEPENDING ON CAPACITOR VALUES C_1 AND C_2.
SET C_V INPUT TO 1V AND ADJUST R_3 FOR $2V_{PP}$ OUTPUT.
SET C_V INPUT TO −1V AND ADJUST R_2 FOR $2V_{PP}$ OUTPUT.
ADJUST R_1 SO THAT THE OUTPUT FREQUENCY IS THE SAME FOR EQUAL-MAGNITUDE POSITIVE AND NEGATIVE CONTROL VOLTAGES.

This quadrature-output VCO produces both positive and negative output frequencies.

from the two buffers with the highest distortion product approximately 40 dB down from the fundamental.

For negative control voltages, the upper transconductance amplifiers, IC_{3A} and IC_{3B}, receive bias current, and the lower amplifiers shut off. The upper amplifiers work in exactly the same way as the lower ones, but they cross-connect to the inputs and integrator capacitors. In this way, the in-phase and quadrature outputs are reversed for negative control voltages, thus creating a smooth transition to what you can consider a "negative frequency." In operation, when viewing the outputs on an X-Y trace, the circular rotation of the dot becomes slower as you adjust the control voltage near zero and then perfectly reverses direction as the control voltage goes negative. This transition occurs without any unwanted crossing of the circle or drifting off beyond the circle.

The two current sources, IC_{1A} and IC_{1B}, are fairly self-explanatory; the upper source operates for negative control voltages and vice versa. The R_1 gain trimmer on the upper source allows you to adjust the oscillator such that a given negative control voltage yields the same frequency as does the equal-magnitude positive control voltage. This trim compensates for differences in transconductance of the two separate dual-amplifier packages. The diodes across the current-source op amps avoid heavy saturation when the respective source turns off. You trim the R_2 potentiometer to obtain equal amplitudes from the upper and the lower sections. The circuit in **Figure 1** uses standard, inexpensive, multiple-sourced components. It requires only minimal (and easy) trimming, with no interacting trims. A 0V control input results in a guaranteed 0-Hz output, dependent only on well-controlled op-amp offsets. With the Bode/Moog system, you must make a front-panel adjustment to zero-beat two oscillators running at 20 kHz.□

16-bit adjustable reference uses 8-bit digital potentiometers

Bonnie Baker, Tucson, AZ

IT MAY BE EASY to find a precision voltage reference for your application; however, a programmable precision reference is another matter. The circuit in **Figure 1** yields a precision reference with an LSB of 62.5 µV. The circuit is a 16-bit DAC using three 8-bit digital potentiometers and three CMOS op amps. Each digital potentiometer operates as an 8-bit multiplying DAC. On the left side of **Figure 1**, two digital potentiometers, IC_{3A} and IC_{3B}, span across V_{REF} to ground, and the wiper outputs are connected to the noninverting inputs of two amplifiers, IC_{4A} and IC_{4B}. In this configuration, the inputs to the amplifiers have high impedance levels, thus isolating the digital potentiometers from the rest of the circuit. The microcontroller, IC_1, programs digital potentiometers IC_{3A} and IC_{3B} through its SPI port. If V_{REF} is equal to 4.096V, the LSB at the outputs of IC_{4A} and IC_{4B} is 16 mV.

To make this circuit perform as a 16-bit DAC, a third digital potentiometer, IC_{2A}, spans across the outputs of the two amplifiers, IC_{4A} and IC_{4B}. The programmed setting of IC_{3A} and IC_{3B} sets the voltage across this third digital potentiometer. If V_{REF} is 4.096V, you can program IC_{3A} and IC_{3B} such that the output difference of op amps IC_{4A} and IC_{4B} is 16 mV. You can achieve high accuracy with this circuit by using a dual digital potentiometer for IC_{3A} and IC_{3B}. With the dual structure, the resistances of these two devices match typically within 0.2%. Given the size of the voltage across the third digital potentiometer, the LSB of the complete circuit from left to right is 62.5 µV ($V_{REF}/2^{16}$). **Table 1** shows the critical device specifications to obtain optimum performance with this circuit.□

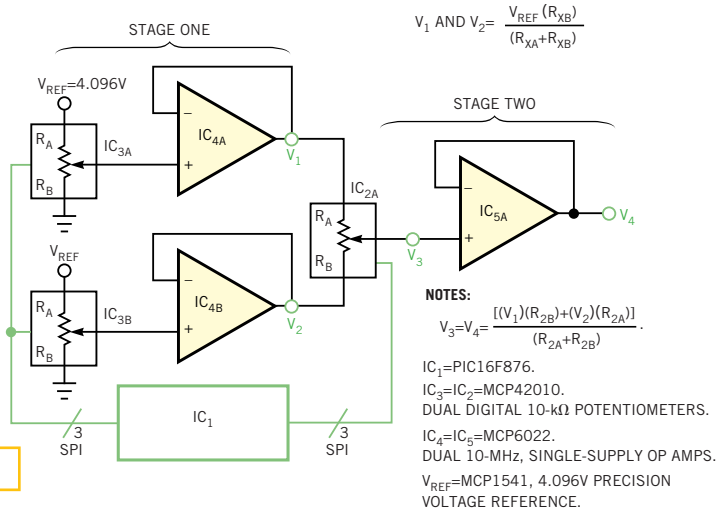


Figure 1

You can design a precision 16-bit DAC by using three digital potentiometers and three op amps.

TABLE 1–DEVICE SPECIFICATIONS FOR OPTIMUM PERFORMANCE

Device	Specification		Purpose
Digital potentiometers (IC_2, IC_3) (MCP42010)	Number of bits	8 bits	Determines the overall LSB and resolution of the circuit.
	Nominal resistance (potentiometer element)	10 kΩ (typical)	Achieve better noise performance by using lower resistance potentiometers. The trade-off for low-noise potentiometers is higher current consumption.
	Differential nonlinearity	±1 LSB (maximum)	Good differential linearity ensures that the circuit exhibits no missing codes.
	Voltage-noise density (for half the resistive element)	9 nV/√Hz at 1 kHz (typical)	If the noise contribution of these devices is too high, it reduces the possibility of achieving 16-bit, noise-free performance. Selecting lower resistance elements can reduce the potentiometer noise.
Operational amplifiers (IC_4, IC_5) (MCP6022)	Input bias current (IB)	1 pA at 25°C (maximum)	Higher input bias current causes a dc error across the potentiometer. CMOS amplifiers are, therefore, good choices.
	Input offset voltage	500 µV (maximum)	A difference in amplifier offset error between IC_{4A} and IC_{4B} could compromise the differential linearity to the overall system; 50 µV is considerably lower than 1 LSB in Stage 1 of the circuit.
	Voltage-noise density	8.7 nV/√Hz at 10 kHz (typical)	If the noise contribution of these devices is too high, it reduces the possibility of achieving 16-bit, noise-free performance. Selecting lower noise amplifiers can reduce overall system noise.