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Edited by Bill Travis

5V power supply teams low-dropout regulator, charge pump

Jim Christensen, Maxim Integrated Products, Sunnyvale, CA

AUXILIARY POWER of 3.3V is replacing the 5V auxiliary power that "silver boxes" supply in most computer systems, but some circuits still require a 5V supply. Such systems impose the messy task of creating a central 5V auxiliary supply from the 3.3V auxiliary supply and then routing 5V power throughout the motherboard. An alternative exists, however, for systems in which only a few ICs need 5V: Employ inexpensive charge pumps as low-power 3.3V-to-5V converters and place them directly at the 5V loads. Regulated charge pumps do this job, but they are uncommon, and they often command a premium price. You can build a regulated charge pump by combining an unregulated charge pump with a low-dropout regulator that reduces the voltage to 5V. Unfortunately, that method requires a low-dropout regulator rated for at least 7V, because an unregulated charge pump can deliver 7V when its 3.3V input goes to the upper limit of tolerance. That fact eliminates the possibility of using the latest low-cost, low-dropout regulators, whose small geometry limits their maximum input to 6.5V.

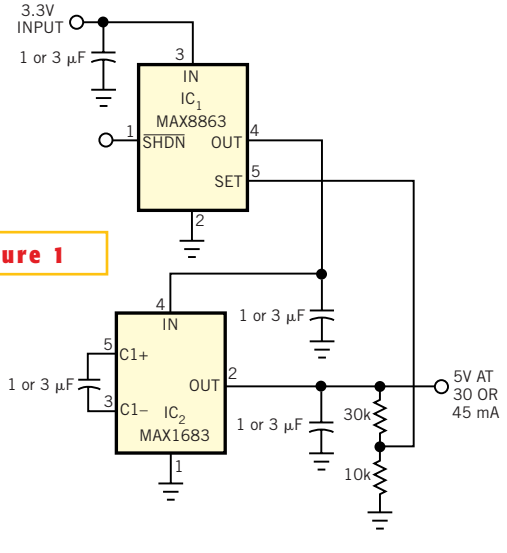
TABLE 1–POWER-SUPPLY PARAMETERS WITH ALL 1-µF CAPACITORS

V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (mW)	I_{IN} at V_{IN}=3.3V (mA)	P_{IN} (mW)	Efficiency (%)	V_{OUT} low-dropout regulator (V)	V_{RIPPLE} (mV p-p)
5.06	10	50.6	20.9	68.8	73.5	2.71	358
5.01	20	100.2	41.1	135.6	73.9	2.86	312
4.9	30	147	62.2	205.3	71.6	3.02	420

TABLE 2–POWER-SUPPLY PARAMETERS WITH ALL 3-µF CAPACITORS

V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (mW)	I_{IN} at V_{IN}=3.3V (mA)	P_{IN} (mW)	Efficiency (%)	V_{OUT} low-dropout regulator (V)	V_{RIPPLE} (mV p-p)
4.99	10	49.9	20.37	68.8	74.2	2.63	154
4.99	20	99.8	40.4	133.3	74.9	2.76	104
4.98	30	149.4	60.6	200	74.7	2.89	154
4.93	40	197.2	80.5	265.7	74.2	3.02	192
4.9	45	220.5	90.5	298.7	73.8	3.09	214

Figure 1



This 5V supply, which you obtain by reducing the 3.3V input with a low-dropout regulator and doubling that output with a charge pump, minimizes the charge-pump output impedance by feeding 5V back to the regulator.

You can reverse the order by placing the low-dropout regulator in front of the charge pump, thereby reducing the 3.3V to 2.5V before doubling it. That approach allows the use of a low-cost, low-voltage, low-dropout regulator, but the charge-pump output impedance then becomes an issue. A low-cost charge pump, such as the MAX1683, operating with 1-µF capacitors exhibits a typical output impedance of 35Ω, making it unusable at currents above a few milliamps. The circuit of **Figure 1** shows a better way to cascade the charge pump with a voltage regulator. The low-dropout regulator, IC_1, reduces the 3.3V input to a lower value, and the unregulated charge pump, IC_2, doubles that value to 5V. To cancel the voltage drop that charge-pump output impedance causes, the circuit feeds the 5V output back to the low-dropout regulator, which alters its output to maintain output regulation. The available headroom of at least 1V allows output currents to approximately 30 mA or even higher with larger capacitors. Although it requires two ICs instead of a single regulated charge pump, this approach can be cheaper because high-vol-

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ume applications use unregulated charge pumps and low-current, low-voltage, low-dropout regulators. Furthermore, because the low-dropout regulator and charge pump are available in SOT-23 packages, the overall footprint of the circuit in **Figure 1** is comparable to that of a regulated-charge-pump circuit.

Table 1 demonstrates the circuit's ability to maintain output-voltage regulation and deliver currents as high as 30 mA; the input, output, and flying capacitors are all 1 µF. Similarly, **Table 2** shows the regulation for output currents to 45 mA; all capacitors are 3 µF. As you can see, load current does not affect efficiency, which is approximately equal to the output voltage divided by twice the input voltage. Capacitor values affect the ripple voltage and available output current but have little effect on efficiency.□

Four-quadrant power supply provides any-polarity voltage and current

Jon Munson, Linear Technology, Milpitas, CA

A conventional power supply operates only in the first quadrant; positive-voltage output and current are sourced to a load or, with a deliberately miswired output, statically in the third quadrant as a "minus" supply. The conventional supply cannot, however, operate in either the second quadrant as an adjustable load for a minus supply, for example, or the fourth quadrant as a discharge-testing a battery with a specific constant current, for example. It also cannot transition seamlessly between the various modes as a function of load condition or control input. The circuit in **Figure 1** achieves full four-quadrant capability with an output topology similar to that of an ordinary audio power amplifier by using a "complementary" pass-transistor configuration. The complementary section may be the basic op-amp output in lower current designs or use external power MOSFETs in cases involving higher power. Controlling the output in the various modes is a simple matter when you use the LT1970 power op amp to manage the operation, thanks to its built-in, closed-loop, current-limiting features.

The four-quadrant supply provides at least ±16V adjustability with as much as ±2A output capability. **Figure 1** shows the basic LT1970-based regulator section. **Figure 2** shows the user-control analog section, using an LT1790-5 reference and an LT1882 quad-precision op amp. The entire circuit operates from a preregulated ±17V bulk power source (not shown). You configure the user-control potentiometers, V_{SET} and I_{LIMIT}, to provide buffered command signals: $V_{CONTROL}$ and $I_{CONTROL}$, respectively (**Figure 2**). You can adjust $V_{CONTROL}$ from −5 to +5V, and the LT1970 regulator circuit amplifies it to form the nominal ±16.5V output range. You can adjust $I_{CONTROL}$ from 0 to 5V; 5V represents the maximum user current-limit command. The V_{CSNK} and V_{CSRC}

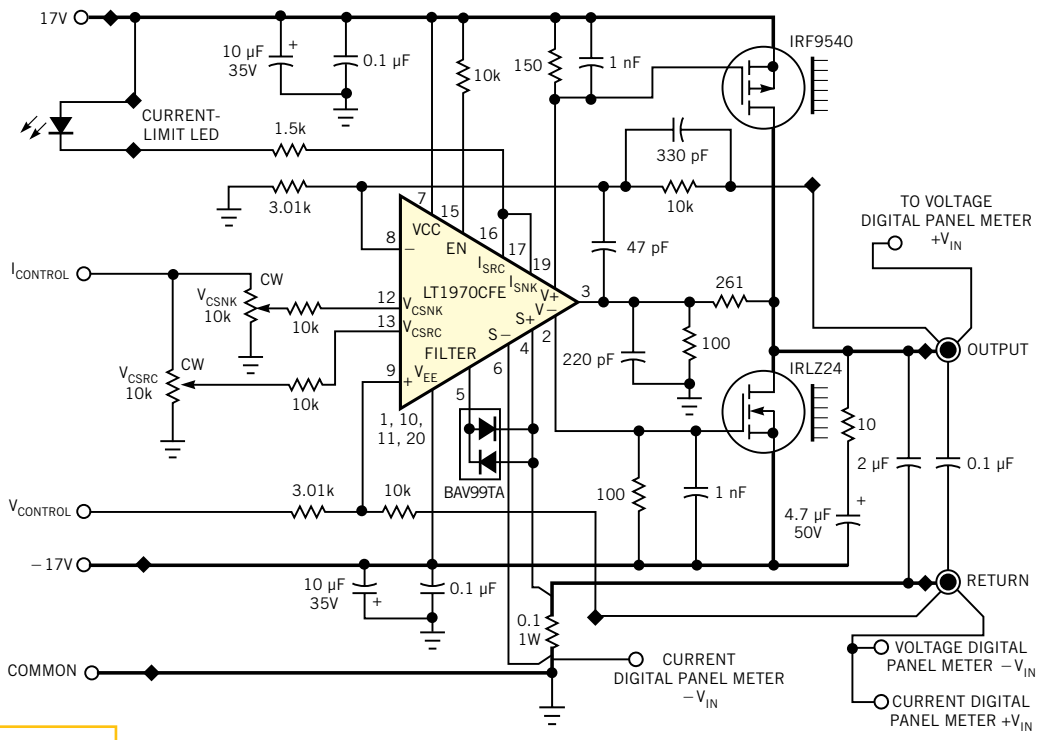

Figure 1

You can obtain four-quadrant power-supply operation by using a power op amp in the output section.

trimmers attenuate the $I_{CONTROL}$ signal to set the precise full-scale currents for sink and source modes, respectively (**Figure 1**).

A 0.1Ω resistor in the load return senses the output current and provides the LT1970 with feedback during current-limiting operation. With this sense resistance, setting the current-limit trimmers to 100% would allow the LT1970 to limit at approximately ±5A, but, because this application requires a 2A maximum current, you set the trimmers to approximately 40% rotation when calibrated. To prevent internal control contention at low output current, the LT1970 sets a minimum-current-limit threshold that corresponds to approximately 40 mA for the sense resistance. Another nice feature of the LT1970 is the availability of status flags, which, in this case, provide a simple means of driving a front-panel LED to indicate when current-limiting is active. The LT1970 features split power connections that allow you to power the internal output section independently from the analog-control portion. The flexibility of this configuration allows direct sensing of the op amp's output current via resistance in the V+ (Pin 19) and V− (Pin 2) connections. This feature gives a convenient means of establishing Class B operation of the MOSFET-output devices using a current-feedback method, in which the op-amp output current is converted to a gate-drive potential, thereby having the MOSFETs turn on only to the extent needed to help the op amp provide the output demand.

Because power supplies inherently must drive heavy capacitive loads—namely, circuits with high-value bypass capacitors—and any overvoltage could damage the circuit, pay careful attention to compensating the op amp for minimal overshoot under all loading conditions. As with most op amps, the LT1970's inner- and outer-loop feedback accomplish capacitive-load tolerance. In this situation, the op amp itself is resistively decoupled from the load. The dc feedback for the LT1970 uses differential voltage sensing to eliminate the regulation error that would otherwise occur with the current-sense and lead resistances in series with the load. You can connect a pair of inexpensive digital panel meters to the output to monitor the output conditions in real time (**Figure 1**). (The two digital panel meters do not share "common" connections, which may complicate their powering.) Note that the selected current-sense resistance optimizes a digital-panel-meter display with the usual ±200-mV full-scale sensitivity to present as much as ±1.999A, for example. One word of caution: When you use this supply in place of a conventional single-quadrant supply to power sensitive electronics, it's good practice to connect a reverse-biased Schottky diode, such as a 1N5821 cathode, to the more positive connection, to the output binding posts. Alternatively, you could use a disconnect relay and power sequencer in the design to protect the load from any energetic reverse transients during turn-on and turn-off of the main bulk supply.

An adjustable power supply is an indispensable tool in any electronics lab. It can be even more useful in many circumstances if it provides the ability to adjust continually through 0V to the polarity, adjustably limit current, or both in either the source or the sink directions. These additional capabilities provide convenient methods of driving or loading circuits that are under development or test that might otherwise require very special or custom equipment, such as active-load units or dc-offset generators. You can readily obtain these features if you base the linear-regulator design on the versatile LT1970 power op amp, which includes built-in adjustable- closed-loop current-limiting functions.□

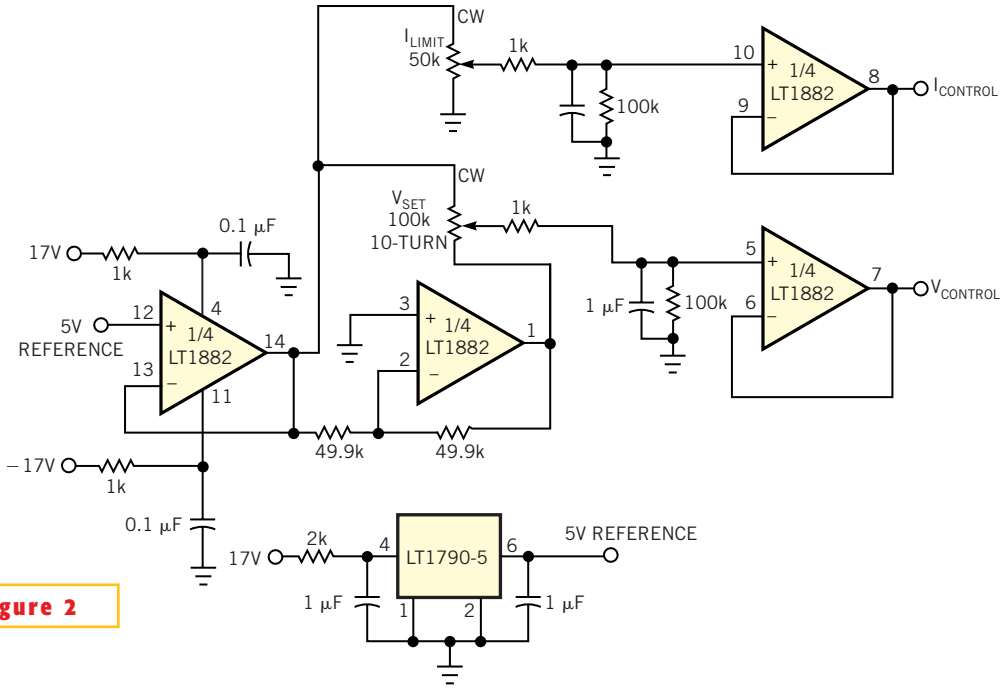

Figure 2

The user-control section allows you to set the voltage range and current-limit parameters for the output section in Figure 1.

Simple circuit controls stepper motors

Noel McNamara, Analog Devices, Limerick, Ireland

STEPPER MOTORS are useful in many consumer, industrial, and military applications. Some, such as personal-transportation systems, require precise speed control. Stepper-motor controllers can be simple (**Figure 1**), but they require a variable-frequency square wave for the clock input. The AD9833 low-power DDS (direct-digital-synthesis) IC with an on-chip, 10-bit DAC is ideal for this task, because you need no external components for setting the clock frequency (**Figure 2**). The device contains a 28-bit accumulator, which allows it to generate signals with 0.1-Hz resolution when you operate it with a 25-MHz MCLK (master clock). In addition, the circuit can easily stop the motor if you program a 0-Hz output frequency.

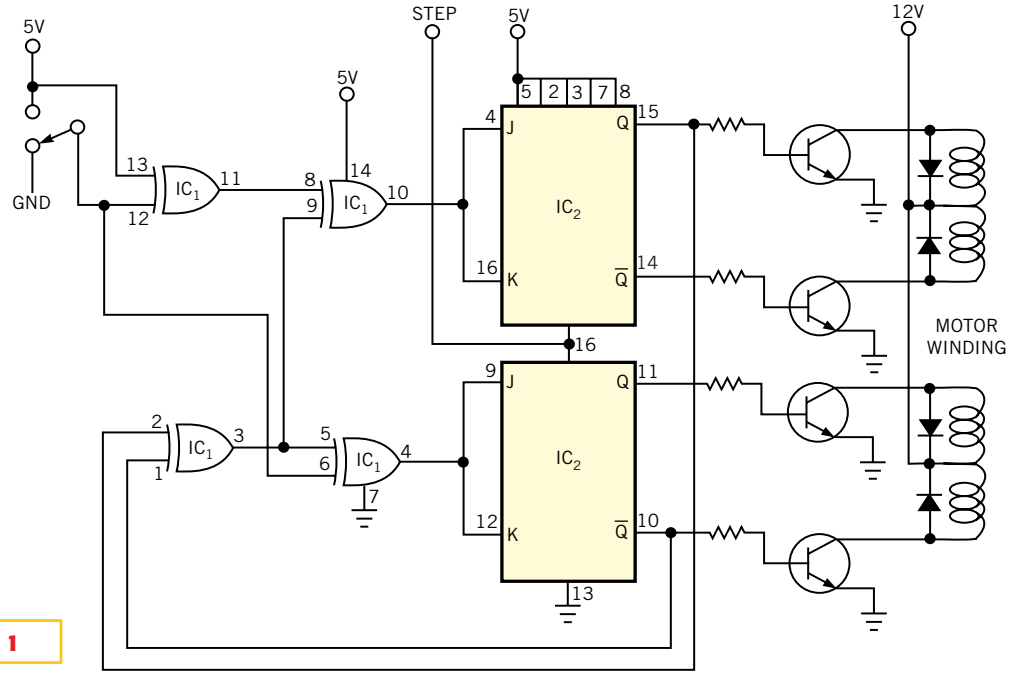

Figure 1

A stepper-motor controller requires only a few logic circuits.

NOTES: IC_1: SN74HC86. IC_2: SN74LS76A.

Figure 3 shows the complete system. The most significant bit of the on-chip DAC switches to the V_{OUT} pin of the AD9833, thus generating the 0-to-V_{DD} square wave that serves as the clock input to the stepper-motor controller. Writing to the frequency-control registers via a simple, three-wire interface sets the clock

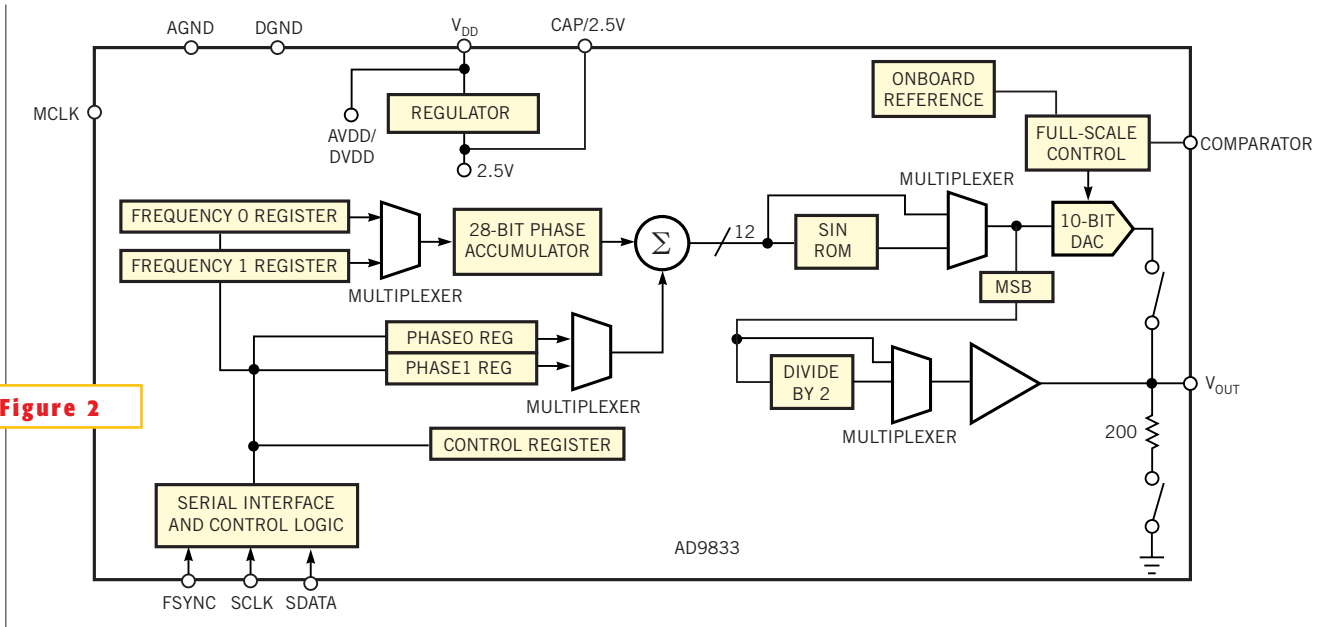

Figure 2

The AD9833 DDS IC generates frequencies with 0.1-Hz resolution.

frequency. Writing a 0 to the frequency register stops the clock, thereby stopping the stepper motor. When you are not using the DAC, you can power it down by writing to a control register. This power-down action results in the AD9833's drawing only 2 mA from the supply. Reducing the MCLK frequency can further reduce the supply current. The AD9833 is available in a tiny, 10-lead package, so you can assemble the complete control system on a very small pc board.□

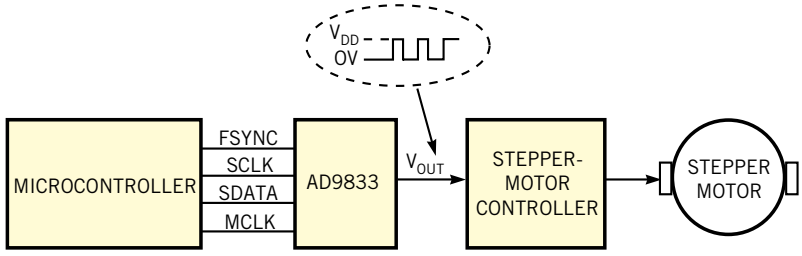

Figure 3

The complete stepper-motor controller uses a DDS IC to generate the variable frequencies for the circuit in Figure 1.

Simple dc/dc converter increases available power in dual-voltage system

David Kim, Linear Technology, Milpitas, CA

THE SCHEMATIC in **Figure 1** shows a way to increase the power available from a current-limited 5V supply by adding power from a −5V supply. The dc/dc converter generates a single 12V, 150-mA (1.8W) output from two regulated and current-limited input sources at 5V, 300 mA (1.5W) and −5V, 300 mA (1.5W). Because the input uses different-polarity voltage sources, the design uses a flyback dc/dc converter to avoid a system-grounding problem. Level-shifted feedback sensing using a pnp transistor, Q_1, references the feedback signal to the negative input voltage. You calculate the feedback-resistor divider by using the formula $R_1=R_4(V_{OUT}-V_{BE})/V_{REF}$, where R_1 connects to the emitter of Q_1, R_4 connects to the collector of Q_1, V_{BE} is the base-emitter voltage of Q_1, and V_{REF} is the feedback reference voltage of the switching regulator.

To simplify the circuit, the flyback converter in **Figure 1** uses an LT1946 monolithic switching regulator. The voltage rating of the monolithic regulator has to be greater than the maximum switching voltage of the flyback converter, calculated by $[(V_{IN1}+|-V_{IN2}|)_{MAX}+V_{OUT(MAX)}/(T_1$ turns ratio)$]+V_{SPIKE}$. The maximum switching voltage is approximately 25V for the circuit in **Figure 1**. Note also that the input capacitor and dc/dc regulator input must be able to handle a maximum input voltage of 10V, resulting from the calculation $+V_{IN1(MAX)}+|-V_{IN2(MAX)}|$. In an event of fault-current conditions, such as shorted input or output, a zener diode, D_2, creates the undervoltage-lockout threshold to turn off the LT1946 whenever either input source is in current limit or the input voltage $(+V_{IN1}+|-V_{IN2}|)$ drops below 6V to help the input supply recover when the fault condition is removed. In a system with two available current-limited power supplies, you can convert the two supplies into a single supply that has more power-handling capability than either of the two inputs. A flyback topology based on an LT1946 monolithic converter offers a simple approach to the grounding problem and the feedback-sensing problem inherent in a dual-input power supply. Sharing the power between two input sources not only adds output-power capability, but also increases the overall flexibility of the system.□

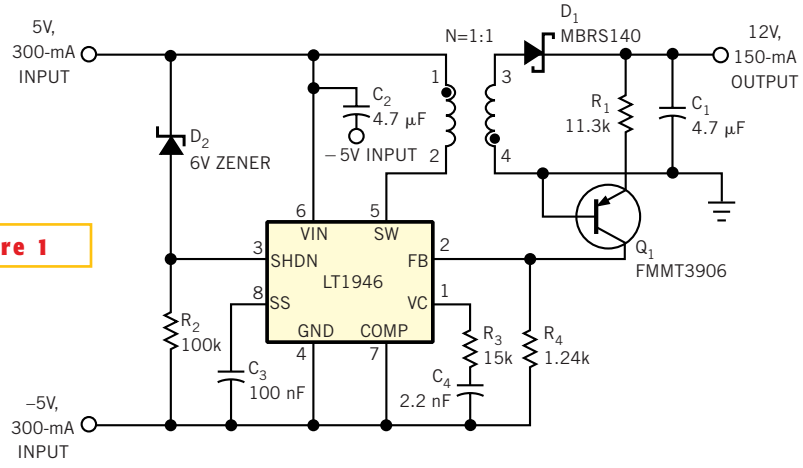

Figure 1

Combining two opposite-polarity power supplies can increase the available power from a flyback regulator.

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Edited by Bill Travis

Force/sense connection eliminates multiplexer on-resistance error

Stephen Woodward, Marine Sciences, Chapel Hill, NC

DIGITALLY CONTROLLED GAIN is an everyday analog-design element. You frequently find this element in an op-amp-based, transimpedance current-to-voltage converter. When you design digital gain control into such a converter, the usual scheme is to arrange things such that a digital multiplexer selects the appropriate feedback resistor for each gain figure. In **Figure 1**, op amp IC_1 is connected in a typical topology but with a twist. The normal way to arrange the gain-setting multiplexer would be to take the converter's output directly from the op amp's output pin (IC_1, Pin 6). The trouble with this method is that the on-resistance of the multiplexer would then be effectively in series with the selected feedback resistance. In cases such as this one, in which the feedback resistance ranges as low as a few hundred ohms or less, the resulting gain error can be large. For example, the on-resistance of the HC4052 in **Figure 1** can exceed 100Ω.

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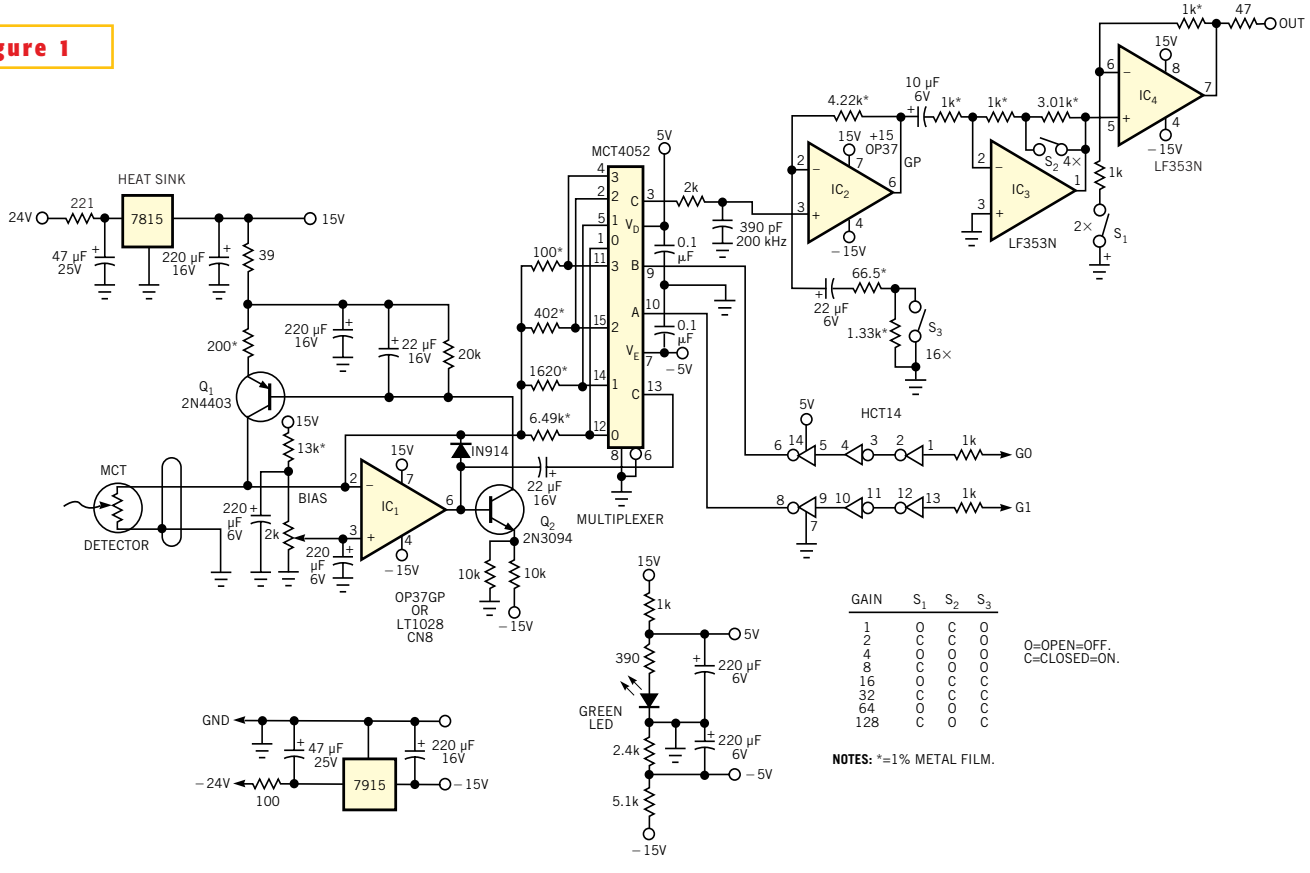
Figure 1



In this programmable-gain circuit, the on-resistance of the gain-setting multiplexer plays no role in the determination of gain.

That figure is equal to that of the lowest gain-setting resistor and, therefore, the source of 100% error. The obvious approach, using larger resistors, works poorly when you need high-frequency performance. The resulting RC delay products can cause frequency peaking, ringing, and, sometimes, outright oscillation.

This Design Idea offers an approach that makes the current-to-voltage converter gain independent of multiplexer resistance. The idea is to use two multiplexers in a force/sense topology such that the output comes from the "force" end of the selected gain resistance, rather than directly from the op amp's output. Assuming that that the load presented to the "sense" output is reasonably high, the result is a gain product that is insensitive to on-resistance. The remainder of the circuit surrounding IC_1 comprises a high-performance bias and preamplifier circuit for a cryogenic (liquid-nitrogen-cooled), mercury-cadmium-telluride infrared detector. These broadband, photoconductive optical sensors are popular in IR spectrometers. They are particularly popular in Fourier-transform-type spectrometers. Their popularity stems from their low noise, wide optical-wavelength responsivity, and electrical response of faster than 1 MHz.

Notable features of the circuit in **Figure 1**, besides the force/sense gain-setting topology, include dynamic biasing (via Q_1 and Q_2) of the MCT detector, 64-to-1 (36-dB) digitally programmable gain, 128-to-1 (42-dB) manual-switch-settable gain, approximately 200-kHz bandpass response, and approximately 700-nV rms input-referred noise of less than 1 nV/$\sqrt{\text{Hz}}$). One trick that helps achieve this noise performance, other than the use of the superquiet LT1028 op amp for IC_1, is the cascaded-inverter HCT14 structure. The HCT14s serve no purpose other than to block entry of noise, which might be present on the digital gain-setting lines, into the gain-setting-multiplexer circuitry. Without these inverters, any such digital noise, a common cause of gremlins in high-gain, computer-controlled analog circuitry, could easily become capacitively coupled to the ac signal path.□

Analog multiplexer uses flying capacitors

Dick Cappels, Mesa, AZ

This Design Idea describes a way to increase the number of analog inputs to your microcontroller for cases in which adding an analog-multiplexer chip or upgrading to a microcontroller with more inputs might be impractical. If the microcontroller you're using has some spare I/O pins and at least one of them is bidirectional or is amenable to tristating, you can configure a simple analog multiplexer using switched capacitors. **Figure 1** shows a two-input multiplexer. A typical switched-capacitor multiplexer completely disconnects the capacitor from the sensed voltage before sampling the voltage across the capacitor.

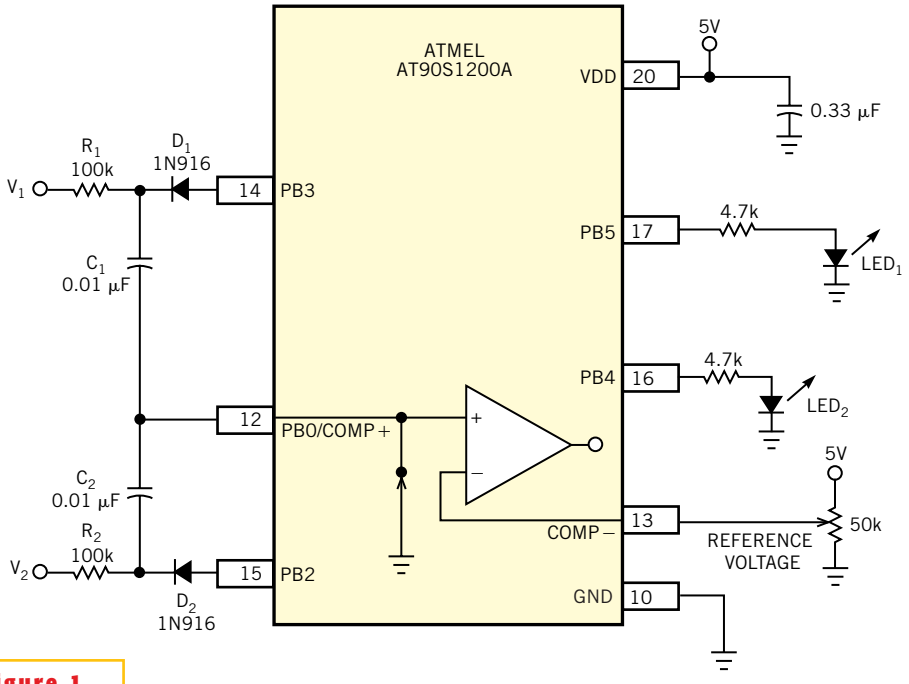


Figure 1

The LEDs in this circuit indicate when the sampled input voltages are above the reference voltage on Pin 13.

To use a typical microcontroller's I/O ports, one terminal of the capacitor remains connected to the input source through a resistor. During most of the operating time, pins 12, 14, and 15 are configured as output pins and are held at logic 0. Diodes D_1 and D_2 do not conduct, so capacitors C_1 and C_2 charge to the values of the input voltages V_1 and V_2, respectively. To sample the voltage stored in the capacitors, pin 12 becomes an input, and the pin associated with each channel switches high while the microcontroller's comparator compares the voltage on Pin 12 with the reference voltage. **Listing 1**, which is available on the Web version of

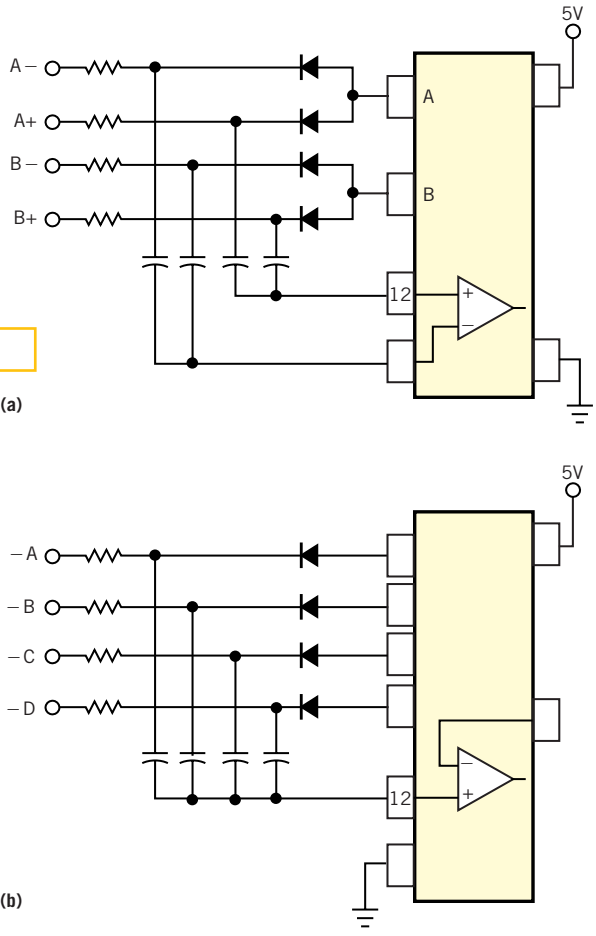
this Design Idea at www.edn.com, gives the code fragment that samples the inputs.

The voltage on Pin 12 is $V_{PIN12}=V_{DD}-V_{DIODE}-V_{IN}$, where V_{PIN12} is the voltage applied to the analog input of the comparator; V_{DD} is the power-supply voltage (5V in this example); V_{DIODE} is the voltage across the diode, and V_{IN} is the voltage applied to input of the RC filter. During the sampling of one input, the voltage on the positive terminals of the capacitors exceeds V_{DD}; thus, D_1 and D_2 are in series with microcontroller pins 14 and 15 to block voltages above V_{DD} and prevent C_1 and C_2 from discharging into the power supply. Also during sampling, C_1 and C_2 are in series with the filter resistor of the input undergoing sampling, causing the capacitors to discharge through the resistor. For this reason, it is important to keep the RC time constant with respect to the sampling period. The worst-case voltage error occurs in the second channel to be sampled, when both V_1 and V_2 are at 0V:

$$V_{ERROR}=(V_{DD}-V_{DIODE})\left(1-e^{-\left(\frac{T_{SAMPLE}}{R_2C_2}\right)}\right),$$

where T_{SAMPLE} is the time one of the diodes' anodes switches to V_{DD} (3 µsec in this example). This sampling time uses the assumptions $R_1=R_2$, $C_1=C_2$, and the fact that the sampling periods for each channel are the same.

Figure 1



The technique lends itself to variations, such as switching sets of inputs (a) and expanding to more than two inputs (b).

With the 1-MHz controller in **Figure 1**, sampling time is a total of 6 µsec for the two channels; using a 16-MHz controller, the total sampling time would be only 375 nsec. When you expand the circuit for more inputs (for example, using the four-input multiplexer in **Figure 2a**), you must take the extra sampling time into account. To maintain a low duty cycle and thus allow the RC filters to charge to the full input voltage, the software should infrequently call the sampling routine. An interrupt every 2048 clock cycles calls the sampling routine in this example. The voltage at Pin 12 in **Figure 2a** is inverted, and, because of the isolation diodes, the maximum input voltage is a diode drop below V_{DD} (approximately 4.4V). If you multiplex both inputs, the circuit compensates for both the polarity and the diode drop (**Figure 2b**). **Listing 2** in the Web version of this Design Idea (www.edn.com) gives the microcontroller assembly code for the multiplexer scheme. You can download the software from the Web version of this Design Idea at www.edn.com.□

FPGA-configuration scheme is flexible

Zhe Lou, Ghent University, Ghent, Belgium

FPGAs are popular in circuit design because of their flexibility and efficiency. You need to program an FPGA by loading configuration data into designated configuration memory. Because most FPGAs have no internal nonvolatile memory, you must store the configuration files in external devices. When you use many FPGAs in a design, it is inadvisable to put a large amount of external memories near the FPGAs. The memory consumes a lot of area and increases the difficulty of the pc-board layout. Consider Xilinx (www.xilinx.com) FPGAs. Xilinx offers daisy-chaining techniques to program multiple FPGAs from a single source. However, when you want to change only one FPGA's functions and keep others unchanged, it is unwise to reprogram all FPGAs, because it takes a lot of time and can cause unexpected problems in the related circuits. This Design Idea describes how to individually program multiple FPGAs with limited resources. It uses a serial port of the Analog Devices (www.analog.com) ADSP21065L to arbitrarily

program four FPGAs (**Figure 1**).

A DSP processor, the ADSP21065L, serves as a microcontroller to program the FPGAs. The configuration bus consists of the Clk, Data, Program, Init, and Done signals. The output data from the ADSP21065L is synchronous with the Clk signal, and the Program (output), Init (input), Done (input), and two control signals (output) are the ADSP21065L's I/O flags. The rest of the circuit comprises four FPGAs from Xilinx. The arrows to the FPGAs represent the configuration bus. The trick is in the so-called switchboard, which traces the configuration bus to an FPGA according to the ADSP-21065L's control signals. At first thought, some bidirectional buffers, for example, 74LVT16245s, would seem suitable for this requirement by linking the control signals to OE and T/R pins of the buffers.

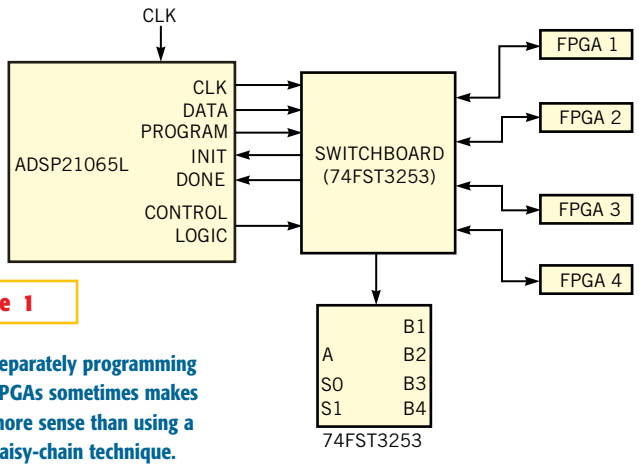


Figure 1 Separately programming FPGAs sometimes makes more sense than using a daisy-chain technique.

But after taking a closer look at the situation, this approach would be difficult because the Init and Done are output signals from the FPGAs, which you cannot merge together. Therefore, the "buffer" you are looking for should have multiplexing or demultiplexing capabilities. This design uses the 74FST3253 dual 4-to-1 multiplexer/demultiplexer bus switch from On Semiconductor (www.onsemi.com) to implement this function. By connecting two control signals to the two select inputs, S0 and S1, you can cause I/O Signal A to connect to I/O lines B1, B2, B3, or B4, respectively, if the value of the two control signals are 00, 01, 10, or 11.□

Add fault protection to a 4- to 20-mA loop supply

Mark Pearson, Maxim Integrated Products, Sunnyvale, CA

A 4- TO 20-mA CURRENT LOOP consists of a power source and a current-measuring device at the control end and a field transmitter that senses process-variable information, such as temperature or pressure, and converts it to a current (**Figure 1**). Most such industrial current loops are powered by 24V dc, but that voltage can range from 12 to 36V. The loop voltage in older systems can be even higher. Many such applications require current limiting, fault protection, or both. For example, a short circuit or another high-current fault in one of several loops powered by a single source can produce a power-supply failure that disables all transmitters powered by that source. Intrinsically safe loops, on the other hand, include a barrier module that limits current and voltage to the transmitter. Fault-protected sources can add another level of system safety. Setting a current limit on each loop lets you accurately size the power supply without overspecifying it. **Figure 2** shows one form of flexible fault protection for the 24V power supply of a 4- to 20-mA loop. It also includes circuitry for recovering a digital signal superimposed on that loop. IC_1, a high-side current-sense amplifier with comparator and reference, senses the loop current in R_1 as an 8- to 40-mV voltage and amplifies it by 100, producing an output-voltage range of 0.8 to 4V. That output, V_{OUT}, can directly drive external meters, strip-chart recorders, and A/D-converter inputs.

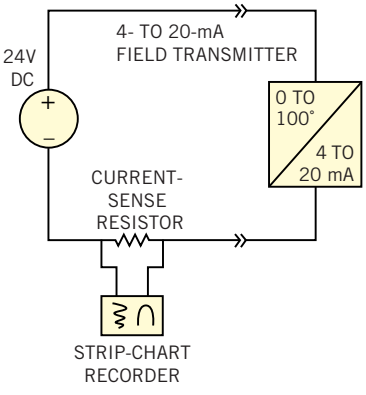


Figure 1 Industrial applications widely use the basic structure of a 4- to 20-mA current loop.

The R_2-R_3 voltage divider sets the selected fault-current trip point for IC_1's first internal comparator at 0.6V. Setting the trip point for a 50-mA fault, for instance, establishes the following relationship between R_1 and R_2: $R_2/(R_1+R_2)=0.6V/(R_1\times100\times I_{FAULT})$, so $R_1=15.67\times R_2$. When faults occur, the C_{OUT1} output assumes a high-impedance state and is pulled high by R_3. The noninverting cascaded-transistor pair Q_2-Q_3 provides an interface to the high loop voltage and preserves a proper logic polarity for controlling the gate of Q_1. Q_1 is held in the off state until pushbutton PB_1 or another reset signal resets IC_1's first comparator. (To disable this comparator's latched output, tie the Reset# pin to ground.) Zener diode ZD_1 protects Q_1's gate-source junction from overvoltage.

IC_2 and its associated circuitry can recover any digital information imposed on the 4- to 20-mA loop current by modu-

lation. The Highway-Addressable Remote Transducer Protocol, for instance, typically uses FSK (frequency-shift keying) of 1200 to 2400 Hz to modulate the loop current between the ±0.5mA levels. (For this circuit, the modulated signal at V_{OUT} (Pin 2 of IC_1) is ±0.1V.) V_{OUT} from IC_1 is capacitively coupled to IC_2 and amplified by that device to recover such digital signals. IC_1 includes a second comparator with inverting input, which you can use to cancel the inversion in IC_2's digital-signal output. Though not essential, this comparator output (C_{OUT2}) can also present the recovered digital signal as a clean rectangular waveform for driving external circuitry.□

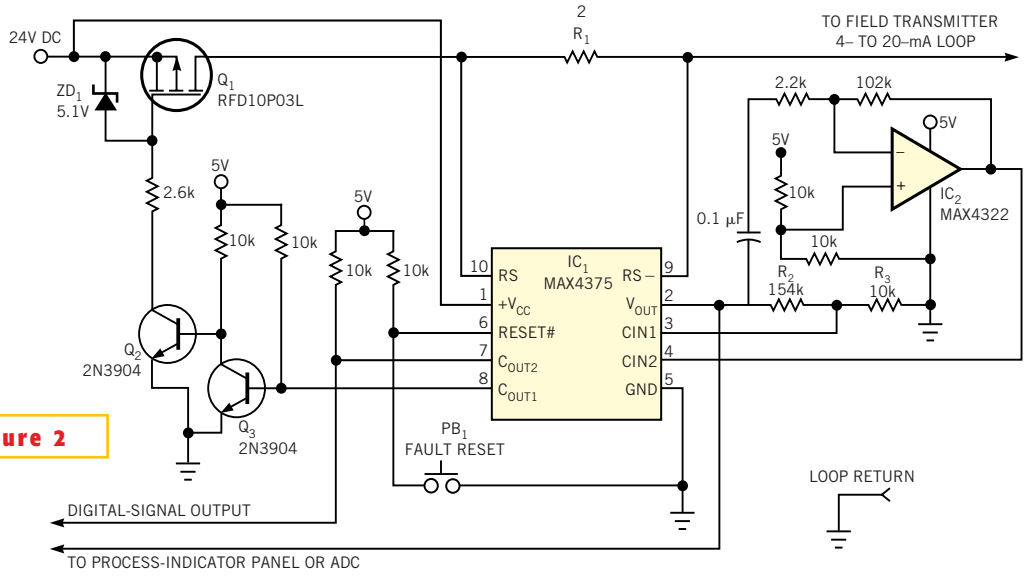


Figure 2

This circuit provides fault protection and digital-signal recovery for a 4- to 20-mA current loop.

Edited by Bill Travis

Double DAC rate by using mixers as switches

Randall Carver, Analog Devices, Greensboro, NC

You can effectively double the sample rate of a DAC by interleaving two DACs into a single unit. Updating each DAC on an alternating basis and switching to the appropriate output double the effective throughput of the overall system. It is essential to overall performance that you use a high-quality, high-speed switch in the multiplexing of the DACs' outputs. The current-mode DACs in this Design Idea allow for current-steering implementation of the output switch. Current steering uses two differential-transistor pairs cross-coupled in the form of a four-quadrant multiplier (**Figure 1**). In this topology, the saturation voltages of the transistors are minimal, voltage swings are small, and switching speeds are high.

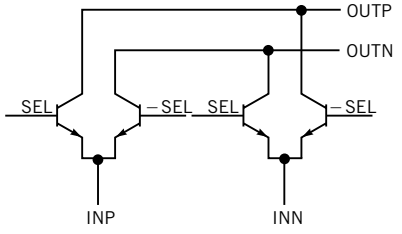


Figure 1 You can use cross-coupled differential transistor pairs as current-mode switches.

The 2.5-GHz AD8343 mixer contains a complete four-quadrant-multiplier structure that you can use as a high-speed, current-mode switch. The bias circuitry internal to the AD8343 sets the dc voltage at the emitters to approximately 1.2V, which in turn sets the compliance voltage necessary at the DAC

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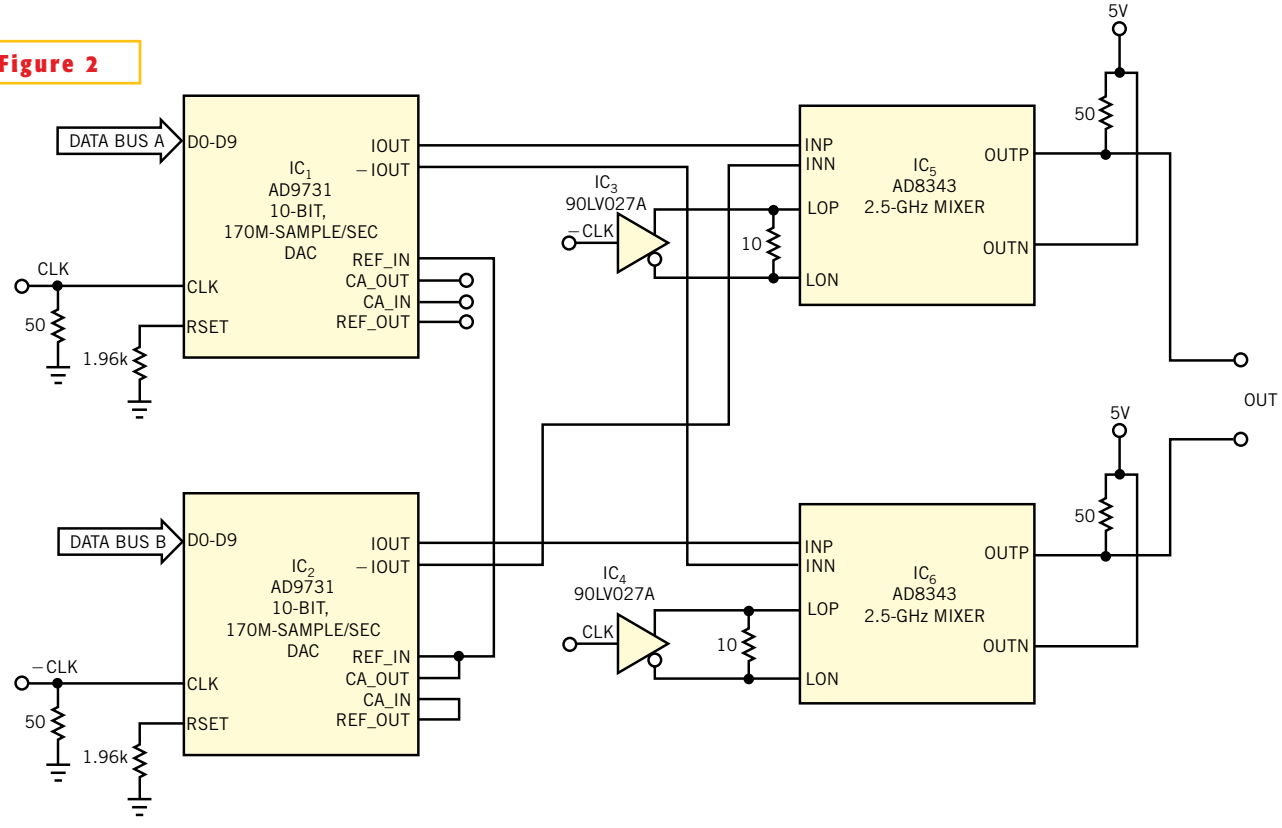
Figure 2



"Ping-ponging" the outputs of two DACs effectively doubles the throughput rate.

outputs. With only a minimal drive signal at the base connections, the emitters appear as a virtual ac ground. The reduced voltage swing at these nodes minimizes the effect of any parasitic capacitances. This Design Idea uses two AD8343 mixers as high-speed switches to multiplex the differential output currents derived from two AD9731 DACs (**Figure 2**). On the output side of the mixers, the termination resistors allow for a dc path to the supply, provide for the current-to-voltage conversion, and present a single-ended back-termination impedance of 50Ω. This configuration allows the circuit to drive a remotely located, 100Ω, differential load via two 50Ω coaxial cables. The low-level clock signals at the LO inputs come from high-speed LVDS buffers terminated in resistances of 10Ω. The approximate ±3.5-mA p-p drivers produce roughly 70-mV p-p drive at the LO inputs. **Figure 3** shows that the circuit provides output rise and fall times faster than 200 psec.□

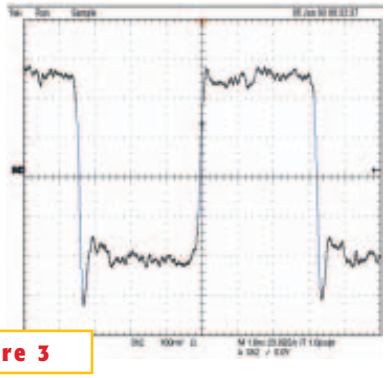


Figure 3

The circuit in Figure 2 produces outputs with less-than-200-psec rise and fall times.

DDS IC plus frequency-to-voltage converter make low-cost DAC

Noel McNamara, Analog Devices, Limerick, Ireland

Precision DACs are essential in many consumer, industrial, and military applications, but high-resolution DACs can be costly. Frequency-to-voltage converters have good nonlinearity specifications—typically, 0.002% for the AD650—and are inherently monotonic. This Design Idea shows how you can use a frequency-to-voltage converter and a DDS (direct-digital-synthesizer) chip for precise digital-to-analog conversion. The DDS chip generates a precision frequency proportional to its digital input. This frequency serves as the input to a voltage-to-frequency converter, thereby generating an 18-bit analog voltage proportional to the original digital input. **Figure 1** shows how the AD650 is configured for frequency-to-voltage conversion. With $R_1+R_3=20$ kΩ and $C_{OS}=620$ pF, a full-scale input frequency of 100 kHz produces a full-scale output voltage of 10V. (See Analog Devices (www.analog.com) application note AN-279 for more details on using the AD650 as a frequency-to-voltage converter.)

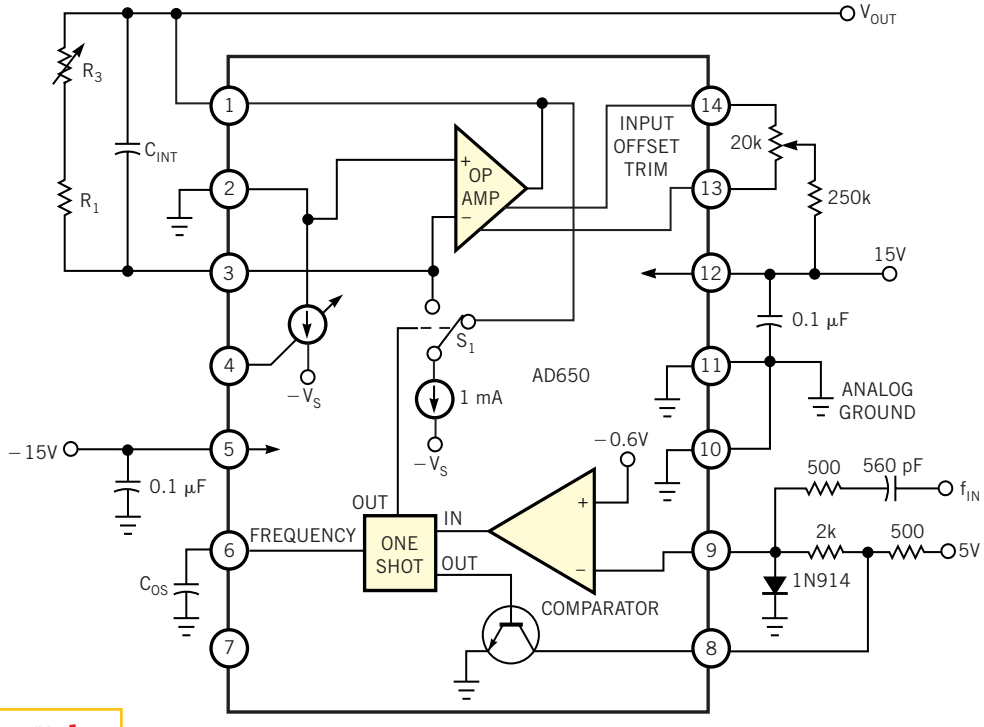


Figure 1

This circuit shows the AD650 in a frequency-to-voltage configuration.

Resolution of 18 bits requires a programmable clock source with a frequency resolution of 0.38 Hz (100 kHz/262,144). The AD9833 low-power DDS IC with on-chip 10-bit DAC is ideal for this task, because setting the clock frequency requires no external components. The device contains a 28-bit accumulator, which allows it to generate signals with 0.1-Hz resolution when you operate it with a 25-MHz master clock. **Figure 2** shows a block diagram of the AD9833 DDS chip. **Figure 3** shows the complete system. The most significant bit of the on-chip DAC switches to the V_{OUT} pin of the AD9833, thus generating the 0V-to-

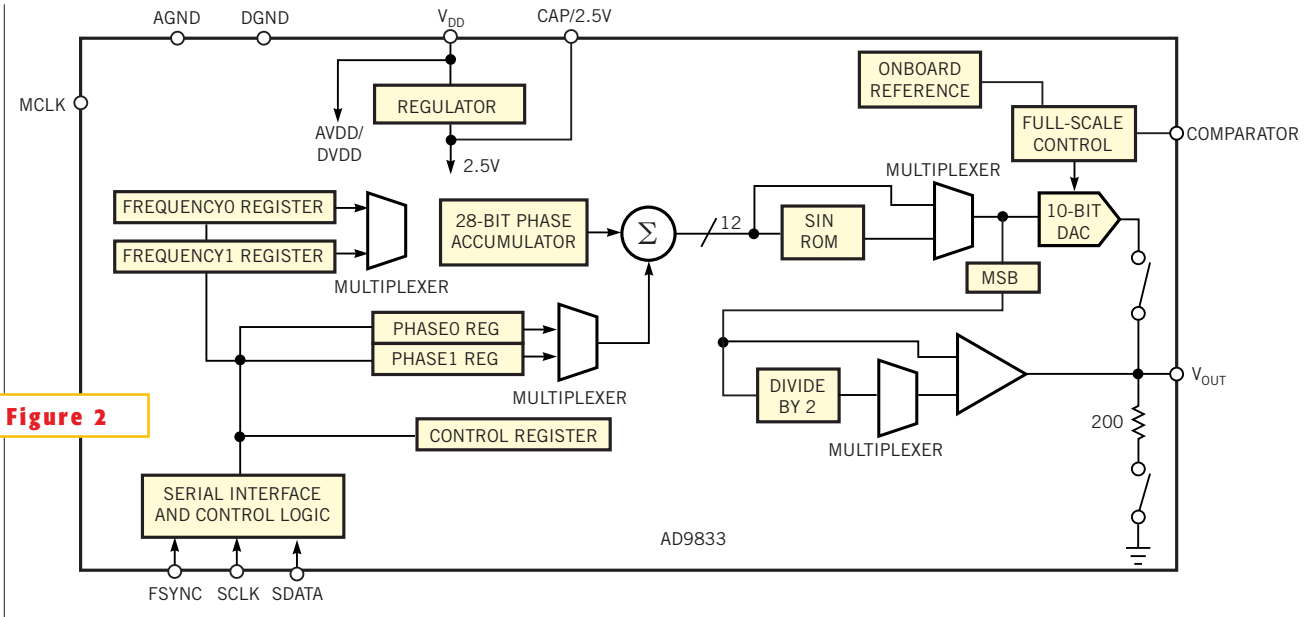


Figure 2

This DDS chip generates signals with 0.1-Hz resolution from a 25-MHz clock.

V_{DD} square wave that serves as the clock input to the AD650 voltage-to-frequency converter. Writing to frequency-control registers via a simple three-wire interface sets the clock frequency, thus programming the voltage output.□

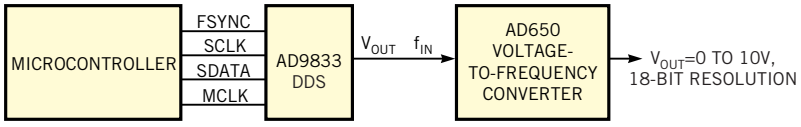


Figure 3

This DAC system delivers 0 to 10V output with 18-bit resolution.

Low-noise ac amplifier has digital control of gain and bandwidth

Philip Karantzalis, Linear Technology, Milpitas, CA

In low-noise analog circuits, a high-gain amplifier serves at the input to increase the SNR. The input signal level determines the input-stage gain; low-level signals require the highest gain. It is also standard practice in low-noise analog-signal processing to make the circuit's bandwidth as narrow as possible to pass only the useful input-signal spectrum. The optimum combination of an amplifier's gain and bandwidth is the goal of a low-noise design. In a data-acquisition system, digital control of gain and bandwidth provides dynamic adjustment to variations in input-signal level and spectrum. **Figure 1** shows a simplified circuit for an ac

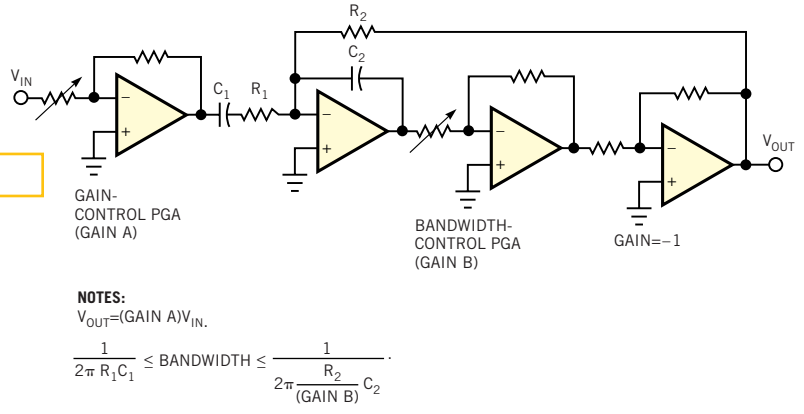
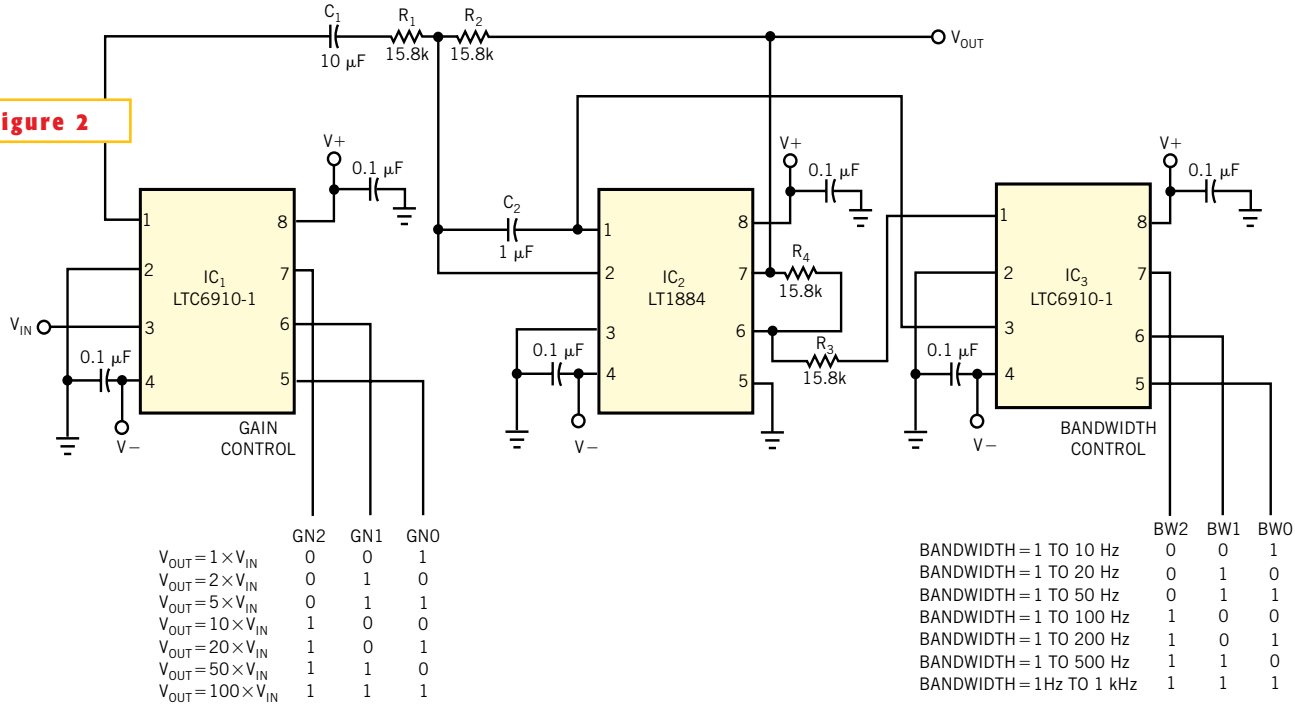


Figure 1

This ac-amplifier configuration offers both gain and bandwidth control.

Figure 2



	GN2	GN1	GN0
$V_{OUT}=1\times V_{IN}$	0	0	1
$V_{OUT}=2\times V_{IN}$	0	1	0
$V_{OUT}=5\times V_{IN}$	0	1	1
$V_{OUT}=10\times V_{IN}$	1	0	0
$V_{OUT}=20\times V_{IN}$	1	0	1
$V_{OUT}=50\times V_{IN}$	1	1	0
$V_{OUT}=100\times V_{IN}$	1	1	1

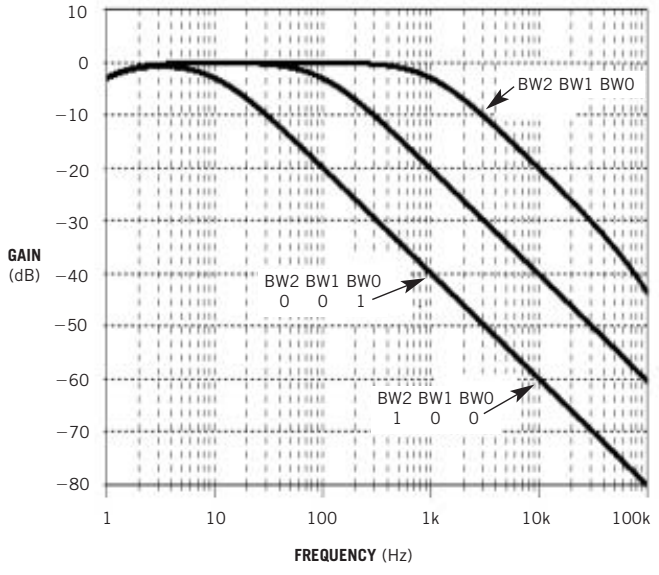
	BW2	BW1	BW0
BANDWIDTH = 1 TO 10 Hz	0	0	1
BANDWIDTH = 1 TO 20 Hz	0	1	0
BANDWIDTH = 1 TO 50 Hz	0	1	1
BANDWIDTH = 1 TO 100 Hz	1	0	0
BANDWIDTH = 1 TO 200 Hz	1	0	1
BANDWIDTH = 1 TO 500 Hz	1	1	0
BANDWIDTH = 1Hz TO 1 kHz	1	1	1

This detailed implementation of the circuit in Figure 1 operates with dual power supplies.

amplifier with control of both gain and bandwidth. The amplifier's input is a PGA (programmable-gain amplifier) providing gain control (Gain A). Following the input PGA is a first-order highpass filter formed with capacitor C_1 and input resistor R_1 of an integrator circuit. Inside the integrator's feedback path, the gain of a second PGA (Gain B) multiplies the integrator's −3-dB frequency, thus providing bandwidth control.

Figure 2 shows a complete circuit implementation using two LTC6910-1 digitally controlled PGAs and an LT1884 dual op amp. The input LTC6910-1, IC_1, provides digital gain control from 1 to 100 using a 3-bit digital input to select gains of 1, 2, 5, 10, 20, 50, and 100. The circuit's lower −3-dB frequency is fixed and set to 1 Hz. A second LTC6910-1, IC_3, is inside an LT1884-based (IC_2) integrator loop.

Figure 3



The frequency response of Figure 2's circuit shows unity gain and three digital bandwidth-control inputs.

The integrator's digital gain control becomes digital bandwidth control, which provides an upper −3-dB frequency control of 10 Hz to 1 kHz. The circuit's low-noise LT1884 op amp and LTC6910-1 (9 nV/$\sqrt{\text{Hz}}$ for each device) combine to provide high SNR. For example, the SNR is 76 dB for a 10-mV peak-to-peak signal with a gain of 100 and 100-Hz bandwidth or 64 dB for a 100-mV peak-to-peak signal with a gain of 10 and 1-kHz bandwidth. With an LT1884 dual op amp (gain-bandwidth product of 1 MHz), the circuit's upper frequency response can increase to 10 kHz by reducing the value of C_2. (The lower −3-dB frequency increases by reducing the value of C_1.) The circuit in **Figure 2** operates with ±5.5V dual power supplies. You can convert it to a single-supply 2.7 to 10V circuit by grounding Pin 4 of IC_1, IC_2, and IC_3; connecting a 1-µF capacitor from Pin 2 of IC_1 to ground; and connecting Pin 2 of IC_1 to pins 3 and 5 of IC_2 and Pin 2 of IC_3. **Figure 3** shows the frequency response of the circuit in **Figure 2** with unity gain and three digital bandwidth-control inputs.□

1-kV power supply produces a continuous arc

Robert Sheehan, Linear Technology, Milpitas, CA

Designing a high-voltage switching power supply that can produce a sustained arc can be challenging. This compact and efficient design delivers 1 kV at 20W and can withstand a continuous arcing, or short-circuit, condition (**Figure 1**). It uses standard, commercially available components. R_1 sets the LTC1871 switching-regulator controller for a nominal operating frequency of 120 kHz. The circuit operates as a discontinuous flyback structure, producing 333V across C_1. The diode/capacitor charge-pump multiplier triples this voltage to create 1000V at the output. **Figure 2** shows the switching waveforms. When the primary switch, Q_1, is on, the output rectifiers are reverse-biased, and energy is stored in the transformer, T_1. When Q_1 turns off, energy transfers to the secondary winding, and C_2 and C_3 pump up the output voltage through the rectifiers. The primary voltage goes high and is clamped through the transformer and rectifier, D_1, by the voltage across C_1. The transformer is well-coupled, so the leakage inductance creates little voltage spike. A small RC snubber across the primary winding damps the ringing and reduces EMI (electromagnetic interference).

For current-limit protection, the circuit in **Figure 1** contains two active circuits and one passive element. The voltage across the current-sense resistor, R_2, limits peak primary current to 7.5A. Q_2 provides secondary-side current limit. Notice the bump on the leading edge of the current ramp of Trace 2 in **Figure 2**. This bump coincides with the positive excursion of the voltage across R_3 in Trace 4, which is the refresh

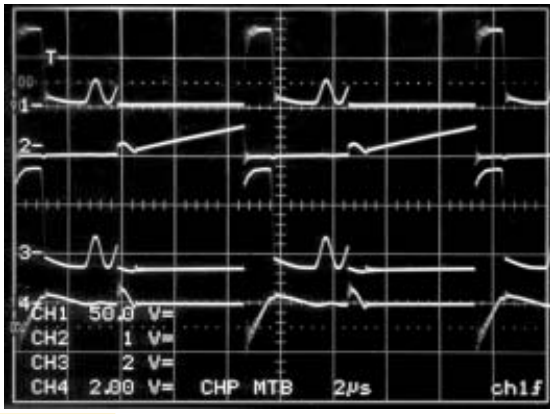
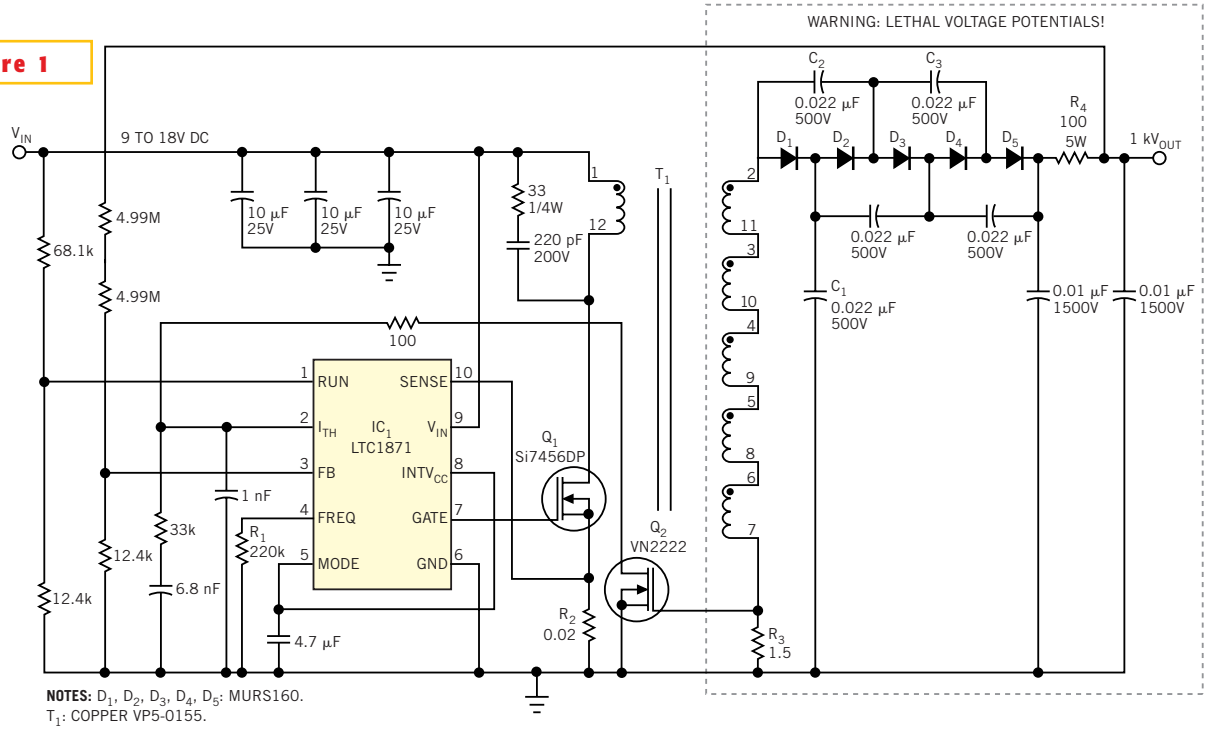


Figure 2 These are the switching waveforms for the circuit in Figure 1. Channel 1is the primary-switch voltage at T_1, Pin 12; Channel 2 is the primary-switch current into Q_1 drain (10A/division); Channel 3 is the secondary-switch voltage at T_1, Pin 2 (200V/division); Channel 4 is the voltage across R_3. (Secondary-switch current=2V/1.5Ω=1.33A/division.)

Figure 1



This circuit delivers 1 kV from a low-voltage input and can produce continuous arcing.

current for C_2 and C_3. When the circuit is overloaded, this slug of current becomes high enough to enhance Q_2, folding back the load current (**Figure 3**). A hard short circuit results in relatively low power dissipation. Omitting Q_2 for the secondary-side current limit results in substantially increased short-circuit current and internal power dissipation, resulting in failure of the primary switch Q_1. R_4 provides a load impedance for the power supply.

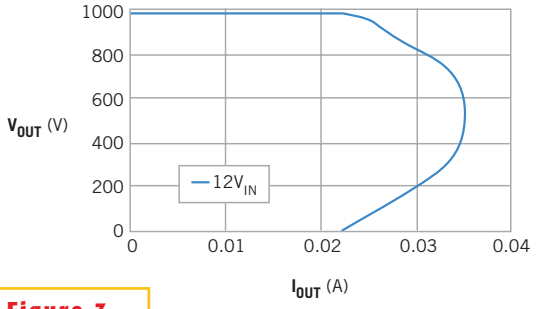


Figure 3 The circuit in Figure 1 has a foldback current-limiting characteristic.

This load helps to limit the peak-current stress in the multiplier capacitors and diodes. Don't skimp on the power rating for R_4, because dissipation during a continuous arc can be substantial. Should R_4 fail open, the feedback circuit forces a full duty cycle with catastrophic results. Too low a value for R_4 can result in charred circuits and hours of debugging. (Yes, a hearty explosion elicits a round of applause from the lab crew.) Arcing is the most stressful condition, and the output capacitor constantly charges and discharges (**Figure 4**). As a final figure of merit, the circuit is efficient (**Figure 5**). The efficiency reaches 87.3% at 12V input and a full load of 20W and increases to 87.7% with an overload of 24W.

So what is this circuit good for? A battery-operated bug zapper, perhaps. And, like raking a live wire across a grounded file, this is a great tool for befuddling the AM-radio listeners on the production floor. The circuit probably doesn't deliver enough energy for use as an ion generator for a plasma cutter, though one engineer I knew was willing to give it a try. A previous version of the circuit used a monolithic switcher, and with the right materials for banana jack and plug, created a bright orange glow and enough heat to raise thoughts about the fire extinguisher (plenty of ozone, too). I'd stay away from using this circuit as a cat trainer or an electric fence. The circuit does generate a lethal voltage potential, and lawsuits can be quite costly. Prototype this circuit at your own risk.□

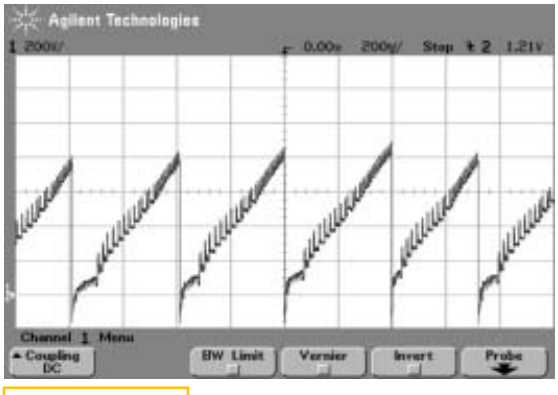


Figure 4 These waveforms represent the output voltage of the circuit in Figure 1 when arcing occurs.

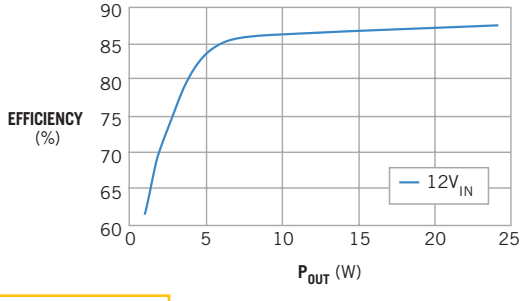


Figure 5 The conversion efficiency of the circuit in Figure 1 is well over 85%.

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Edited by Bill Travis

Solid-state relays simplify monitoring electric-car battery voltage

Robert Krause, Fairchild Semiconductor, San Jose, CA

FIGURE 1 SHOWS the propulsion system of an electric vehicle. It includes an electric motor, drive electronics, a mechanical transmission, vehicle control/power management, a charging system, and a battery. The long-term performance of the electric vehicle depends on ensuring the electrical health of the battery and its charging system. The battery system in an electric or a hybrid-electric car comprises a series connection of 75 to150 individual 2V cells. This series connection generates a potential voltage of 150 to 300V. The measurement of an individual cell's terminal voltage creates a testing dilemma. The high electrical potential precludes the use of standard differential op amps connected across each cell. The measurement of each cell's voltage entails using a switching network that interconnects an isolated or floating A/D converter between the two terminals of each cell in the string. A measurement method also needs a switching system to sequence this "voltmeter" across each of the 150 cells.

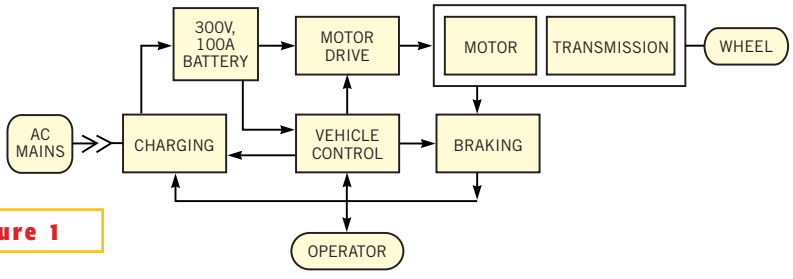

Figure 1

The components of a typical electric vehicle include an electric motor, drive electronics, a mechanical transmission, vehicle control/power management, a charging system, and a battery.

The functional block diagram is an example of an electric car's battery system (**Figure 2**). The battery comprises a series connection of 150 2V cells. This configuration provides a combined potential of 300V. This high dc potential requires the use of an isolated voltage-measurement system. A microcontroller-based isolated voltmeter and isolated switch controller do not provide this function. The cell-measurement system comprises a switching array of 151 of Fairchild Semiconductor's (www.fairchildsemi.com) HSR-412 SSRs (solid-state relays), which provide an off-state blocking voltage of 400V. Each relay is an SPST (single-pole, single-throw), NO (normally open), optically activated switch. As little as 3 mA, or 5 mW, of LED-drive current energize these relays. This low turn-on power consumption eliminates the need for relay-driver ICs.

The first step in measuring the cell's potential is to connect the isolated voltmeter across each cell. A closer look at **Figure 2** reveals how to effect this connection. The input to the isolated voltmeter connects to a two-wire measurement bus. The terminals of this bus are designated A and B. The test points across the various battery cells are designated SSR(N) and SSR(N+1), where (N) is the cell number you are currently measuring. You make Cell 1's voltage measurement by closing SSR_1 and SSR_2 and leaving all the remaining 149 relays off, or open. Closure of the two SSRs connects Cell 1's positive potential to Node A of the absolute converter through the output of SSR_1, and the cell's negative potential to Node B through SSR_2. You measure the second cell in the stack by opening SSR_1 and closing SSR_3 while SSR_2 remains on (closed). This sequence connects Cell 2's positive potential to Node B through the output of SSR_2 and the cell's negative potential to Node A through the output of SSR_3. The process then repeats until all cells have been measured. At this time, the

TABLE 1–THE ALTERNATING POLARITY OF THE A AND B NODES AS THE INDIVIDUAL CELLS ARE MEASURED

Cell number	SSR on (positive cell terminal	SSR on (negative cell terminal)	Voltage at Point A	Voltage at Point B
1	1	2	1	2
2	2	3	2	1
3	3	4	1	2
4	4	5	2	1
5	5	6	1	2
*	*	*	*	*
*	*	*	*	*
148	148	149	1	2
149	149	150	2	1
150	150	151	1	2

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voltmeter returns to Cell 1 and restarts the process.

Table 1 shows the alternating polarity of A and B wires as the cells are measured. To measure the voltage of an individual cell (N), SSR(N) and SSR(N+1) are energized and all other SSRs are off, or open. The alternating polarity of the measurement lines requires the addition of an absolute-value converter between the bus lines and the microcontroller's analog-to-digital input. The microcontroller controls the sequence of measurement events. To measure a cell, the microcontroller sends out a discrete 8-bit digital address corresponding to the cell being measured. This address goes to a decoding block composed of 11 74HC154 multiplexers. The data is transmitted through an array of eight channels of high-speed HCPL2631 optocouplers. The optocouplers provide the common-mode voltage isolation between the 300V battery voltage and the chassis ground. The dual-channel density of the HCPL-2631 optoisolator reduces component count in the block to four. The system addresses the individual cells every 3 msec. This time is how long it takes to turn on and turn off the HSR412 SSR. A cell-voltage measurement takes place 600 µsec after the cell has been addressed. The SSR's turn-on time is less than 500 µsec, thus permitting a 100-µsec acquisition time for the microcontroller's 10-bit A/D converter. The sum of the turn-on and -off times of an SSR times the number of cells measured determines the cycle time. When you use the HSR412, the measurement time for 150 cells is less than 450 msec.

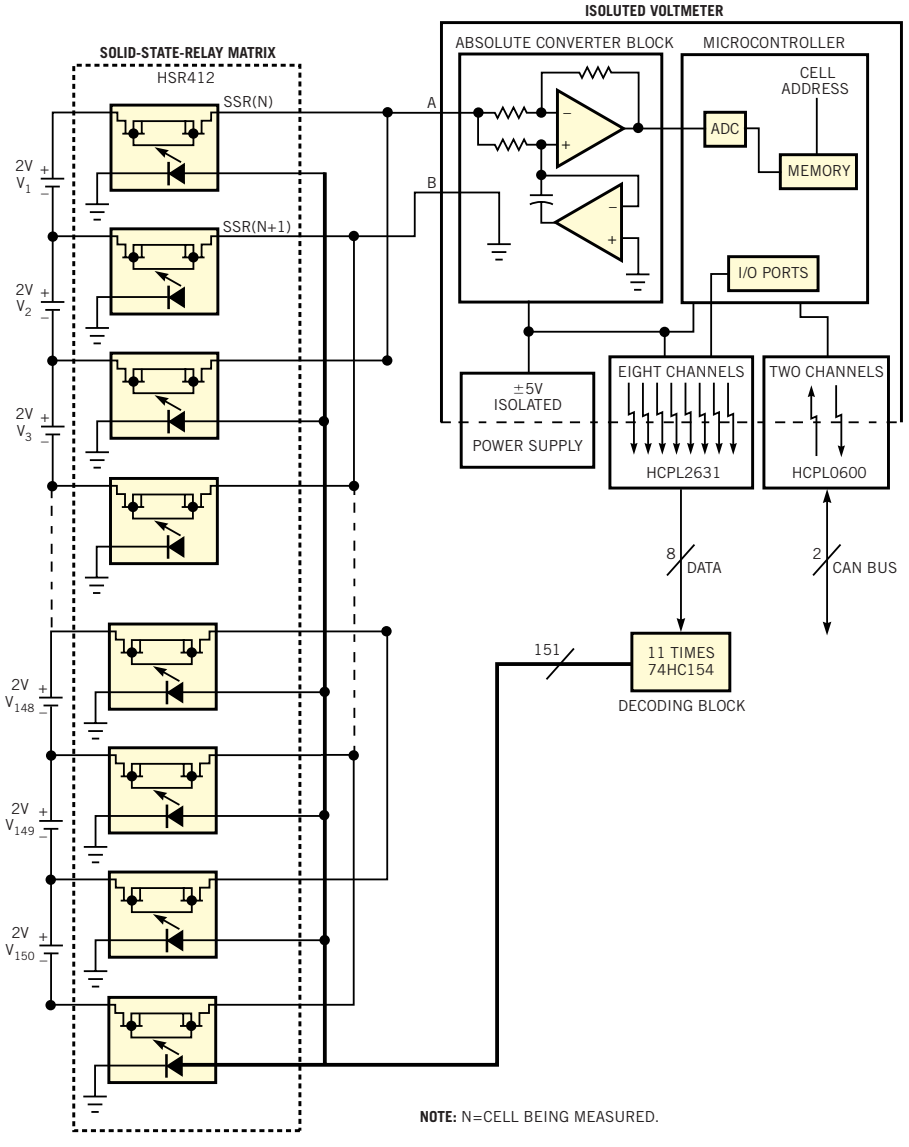


Figure 2 An SSR-based switch matrix allows you to measure individual cells in an electric car's battery.

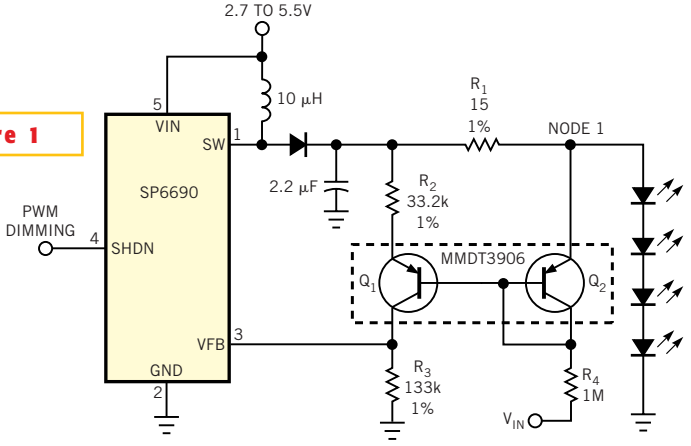
When you measure an individual cell, the V(N)-to-V(N+1) bus potential is approximately 2V. This figure is the differential-mode voltage. The V(N)-to-V(N+1) potential to chassis ground ranges from 2 to 300V, depending on the cell under measurement. This 300V common-mode voltage is well within the 400V off-state blocking voltage of the HSR412. The switch-matrix-control circuits must also be able to accommodate this 300V common-mode voltage. The SSR easily solves this problem. The LED-to-SSR switch isolation voltage is 4 kV rms, which is more than adequate for a 300V system. The 300V common-mode voltage requires that an isolated dc/dc converter powers the microcontroller. The microcontroller records the absolute value of the cell voltage and stores this value and cell number in its onboard memory. At the conclusion of an entire measurement cycle, the microcontroller formats the data to comply with a standard automotive serial-bus format. An example is CAN Bus. Once formatted, the data routes to the vehicle-control computer via a bidirectional, optically isolated link. This link uses two high-speed HCPL-0600 logic-compatible optocouplers. Once that data is received and acknowledged, the measurement cycle can repeat.□

Scheme provides high-side current sensing for white-LED drivers

Dimitry Goder, Sipex Corp, San Jose, CA

White LEDs find wide use in backlighting color-LCD screens in most portable devices, such as cellular phones, PDAs, and MP3 players. Multiple LEDs often connect in series to ensure that the same current flows through every LED. To forward-bias these LEDs, a voltage of 10 to 16V comes from an inductor-based boost regulator, such as an SP6690. However, white LEDs are behind the display, whereas boost regulators are on the main pc board, and it is important to minimize the number of interconnects. You can obtain the best results if you implement high-side and differential-current sensing. In this case, the boost regulator's output looks like a high-voltage true current source. Of course, LEDs need to connect to ground at some point, but it is unimportant where they connect. For example, the display itself can locally pick up ground. This approach allows you to effect a "single"-wire connection. The simple circuit in **Figure 1** shows the implementation of the idea.

Figure 1



This circuit provides high-side current sensing for driving a string of white LEDs.

R_1 acts as a current-sense resistor. The diode-connected Q_2 level-shifts the voltage at Node 1 and applies it to the base of Q_1. These transistors come in one package and provide closely matched V_{BE} voltage when they operate at the same current. Because the V_{BE} values match, the emitter of Q_1 is at the same voltage as Node 1. As a result, the voltage across resistor R_2 matches the drop across R_1 and produces Q_1 emitter current that equals V_{R1}/R_2. This current flows to Q_1's collector and creates a voltage drop across R_3. The boost-regulator SP6690 regulates the voltage across R_3 at 1.22V, the IC's internal reference voltage. R_4 provides current bias for Q_2. The value of R_4 allows the Q_1 and Q_2 collector currents to match. You calculate the value of R_1 as follows: $R_1=R_3\times(V_{OUT}-V_{IN}-V_{BE})/1.22$, where V_{OUT} is the combined LED forward voltage. The output current is $I_{OUT}=0.3A/R_1$. The circuit in **Figure 1** sets I_{OUT} at 20 mA, but you can adjust it by using a different R_1 value. Note that you could return R_4 to ground, but it instead connects to V_{IN}. This connection removes quiescent current through the resistor and Q_1/Q_2 when the SP6690 is in shutdown mode.□

Simple technique makes low-cost pc-board shields

Steve Hageman, Windsor, CA

Many pc-board assemblies require shields to reduce susceptibility to interference from electromagnetic fields. A classic example is a radio receiver, in which the front end usually needs high isolation from the tuning synthesizer. Historically, shields for low-volume or low-cost applications involve trade-offs. You can't justify the cost of a custom-cast shield, and shields machined from aluminum burn through money as fast as the end mills go dull. You can make a simple shield for just a few dollars by using commonly available die-cast aluminum "project boxes," such as those from Hammond Manufacturing (www.hammondmfg.com). These boxes come in sizes from 2×2 in. to more than 7×4 in. You turn the project box into a shield by sandwiching the pc board between the top and the bottom of the box, thus completely enclosing the sensitive circuitry.

The basic idea is to choose a box that is big enough to fit the sensitive circuitry that you want to shield. Then, lay out the circuit in such a way that you can sandwich the board between the cover and the body of the project box. To have a continuous ground around the lip of

Figure 1

You should place a ground track on the top and the bottom of the pc board where the project-box shield sits.

the box, place a 1/8- to 1/4-in.-wide ground track all the way around the area where the box will sit on the top and the bottom sides of the board. Then, add mounting holes in the corner so that you can assemble the box around the pc board and screw it together (**Figure 1**). To get signals into and out of the shield on a multilayer board is easy: Just use the inner layers and go under the ground track. On a double-sided board, you can break the track for traces, or—better yet—you can use a 0.25W resistor to bridge the track. The 0.25W-resistor method serves two purposes. First, it allows a signal to get over the ground track without cutting it. Second, it is a perfect place to add impedance to the signal line and hence obtain high-frequency filtering. This method can help to prevent stray signals from getting into the sensitive circuitry you are trying to protect.

For both the methods mentioned, you need to notch the box's body with a mill or file (**Figure 2**) to provide clearance to the resistor or traces. Note, however, that this notch acts as a waveguide for RF signals, so keep the following in mind: The longest dimension of any gap should be much less than one-quarter of a wavelength at the highest frequency of interest. In high-performance shielding work, strive to keep the gaps below one-twentieth of a wavelength. If you want to "fill up" the gap, you can buy conductive foam or metal gaskets from 3M and WL Gore (www.3m.com and www.gore.com); you can use these gaskets to fill in any gap to make it electrically smaller. Likewise, any gaps in the box-to-pc-board contact as it sits on the ground track also act as waveguides. Depending on the required frequency of operation, these gaps may or may not cause a loss of shielding effectiveness (**Reference 1**). As a side benefit, you can also use the shield as a heat sink. By placing TO-220 regulators outside the box, you can attach the regulators' heat sink to the enclosure. Thus, you have not only a shield, but also a heat sink (**Figure 2**).□

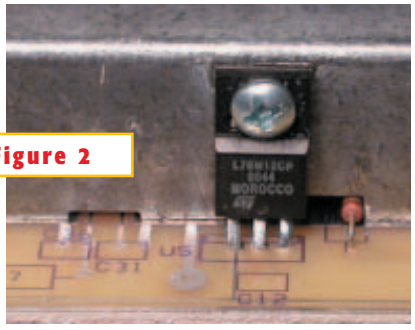


Figure 2

You can mill small notches in the shield to provide signal access. As a side benefit, you can use the shield as a heat sink for TO-220 regulators.

REFERENCE

1. Ott, Henry, *Noise-reduction techniques in electronic systems*, Wiley-Interscience, 1988, ISBN 0-471-85068-3.

Lowpass filter has improved step response

John Guy and Robert Nicoletti, Maxim Integrated Products, Sunnyvale, CA

A COMMON PROBLEM that arises when you design lowpass filters for signal conditioning is the filters' effect on the system's time-domain response. Because pushing the cutoff frequency lower slows the step response, the system may fail to recognize significant changes within a reasonable amount of time. The circuit in **Figure 1** accommodates lower cutoff frequencies without sacrificing the step-response time. A window comparator monitors the delta (difference) between the filter's input and output. When the delta exceeds ±50 mV, the filter increases its slew rate by increasing the cutoff frequency by an order of magnitude. The switched-capacitor filter, IC_1, normally operates as a self-clocked device. Capacitors C_1 and C_2 set the cutoff frequency at 0.1 Hz, and other circuitry forms a dynamic window comparator. Transistor pairs Q_1-Q_2 and Q_3-Q_4 form a complementary current mirror whose output flows through R_2 and R_3, creating a delta of ±50 mV. Connecting the output voltage to the center tap of the two resistors centers the delta on the output voltage. You therefore set the window comparator's upper threshold at V_{OUT}+50 mV and the lower threshold at V_{OUT}−50 mV.

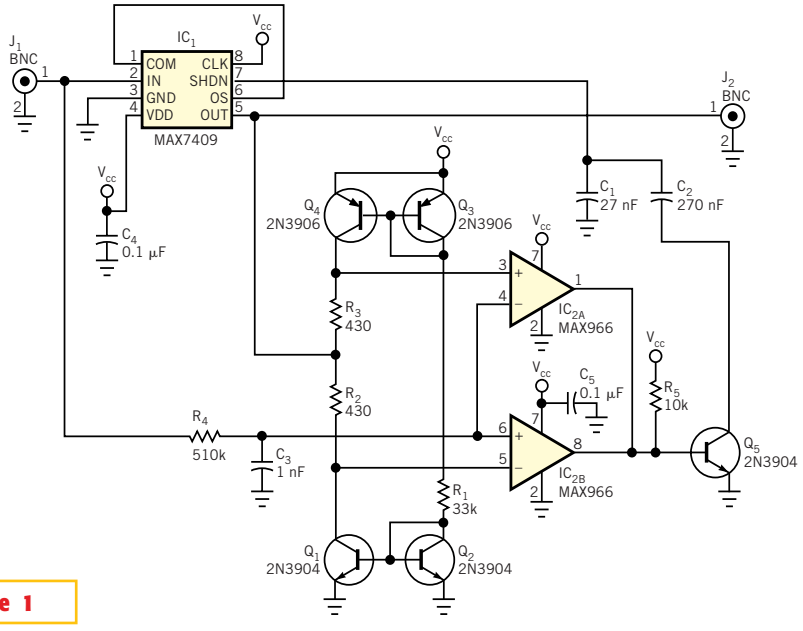


Figure 1

This lowpass filter maintains a fast step response by dynamically adjusting its cutoff frequency.

R_4 and C_3 provide lowpass-filtering to the original input signal, producing a 312-Hz cutoff frequency that reduces sensitivity to momentary glitches. The filtered input drives the window comparator's input. If that input is outside the

±50-mV window, comparator IC_{2A} or IC_{2B} asserts its output low. The low output drives Q_5 into cutoff, causing its collector to assume a high impedance. Because Q_5's collector no longer grounds capacitor C_2, the filter's cutoff frequency increases by a factor of 10. When the system's output changes to within 50 mV of the input, the cutoff frequency throttles back to its quiescent state. **Figure 2**'s oscilloscope photo shows the effect. The top trace is a step from 1.5 to 2.5V, the middle trace is the output with optimization circuitry enabled, and the bottom trace shows the filter's unmodified response. The optimized response includes a slight perturbation during the cutoff-frequency transition, but is five times faster than that of the unmodified circuit. The circuit in **Figure 1** is configured for low cutoff frequencies, but you can rescale it for higher frequencies by changing C_1 and C_2. You can also modify R_2 and R_3 for different window values, for which the delta equals the resistance multiplied by 115 µA. The comparator must be an open-drain type.□

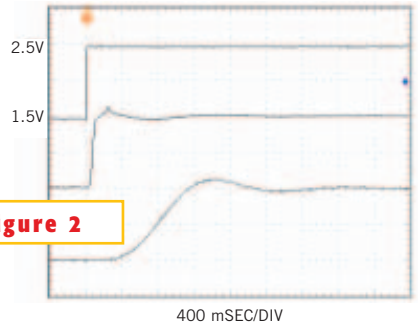


Figure 2

These traces show the time-domain response for the circuit in Figure 1 with optimization circuitry (middle trace) and without it (bottom trace).

Fault-latch circuit protects switchers

Craig Varga, National Semiconductor, Phoenix, AZ

Many power-supply designers like to have a regulator latch off in the event of an overcurrent situation or other fault condition. Yet, many PWM controllers do not internally support this latch-off function. Most do, however, have a power-good output and an enable function. The circuit in **Figure 1** adds that latch-off capability at low cost in little additional space. The design is based on the LMS33460, which is a power-supply monitor in a tiny, five-lead SC-70 package. You just need to combine it with a few small passive parts, and the circuit is complete. When the Enable Input signal goes high, the voltage at the top of C_1 rises quickly to 5V. Because the output voltage is not yet alive, P_{GOOD} stays low, charging C_1 through R_1. Because the voltage on C_1 is zero at the instant of turn-on, Pin 5 of IC_1 pulls up to 5V and begins to drop at a time constant that C_1, R_1, and R_2 determine. If the output does not reach its normal operating voltage before the Pin 5 voltage drops to less than 3V, IC_1 pulls its output low and latches the regulator off.

If, however, the output comes into regulation before the latch times out, P_{GOOD} goes high and C_1 begins to discharge, raising the voltage on Pin 5 and keeping the supply enabled. R_2 provides a couple of volts to IC_1 to keep the IC alive in the event of a latch condition, and D_1 pulls down on the PWM's Enable when the system-enable command switches low. C_1 can be a small tantalum or ceramic capacitor. If you use a ceramic unit, choose a good dielectric, such as X5R. Also, the 5V supply's rising in less than 1 msec or so may eliminate the Enable, and the whole circuit simply runs from the 5V supply. **Figure 2** shows a normal start, and **Figure 3** shows start-up with the second output of a two-output regulator shorted. In both cases, the top trace is the system-enable signal, the second trace is IC_1's Pin 5, the third trace is the PWM Enable at IC_1's Pin 4, and the bottom trace is the regulator's output voltage. You can see in **Figure 3** that IC_1's Pin 5 decays to 3V, at which point it pulls the PWM Enable low, latching off the regulator.□

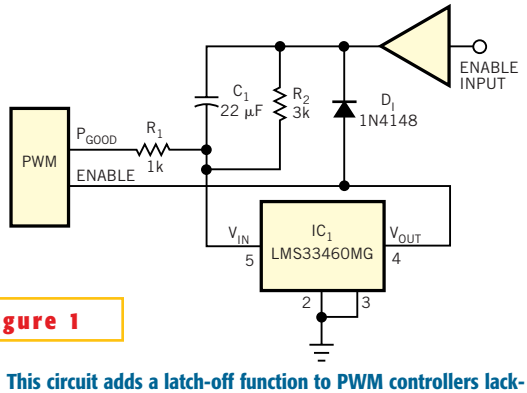


Figure 1

This circuit adds a latch-off function to PWM controllers lacking this feature.

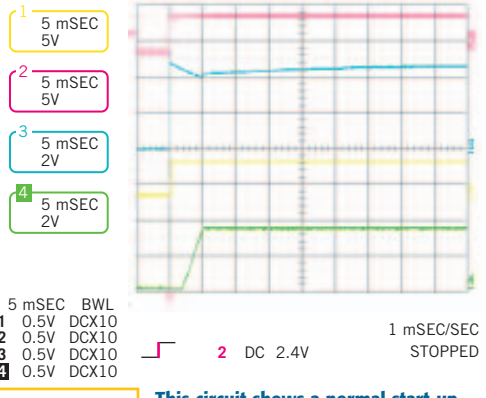


Figure 2

This circuit shows a normal start-up sequence for the circuit in Figure 1.

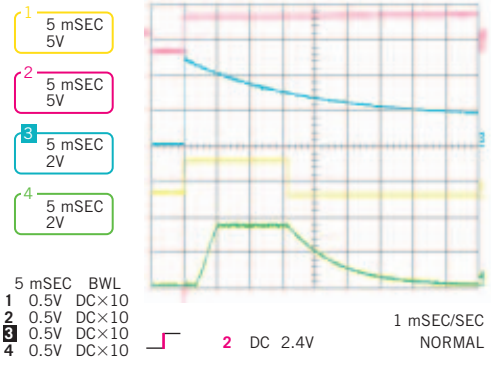


Figure 3

These traces represent start-up with the second output of a two-output regulator shorted.

Edited by Bill Travis

Circuit provides efficient fan-speed control

John Guy, Maxim Integrated Products, Sunnyvale, CA

As Moore's Law plunges us into the realm of multigigahertz processors and PCs with gigabytes of RAM, engineers face the task of removing the heat that these state-of-the-art components produce. Cooling such systems poses a dilemma. If you optimize the fan size and speed for nominal operating conditions, the system is susceptible to failure when conditions deteriorate. If, on the other hand, you select the fan to maintain acceptable operating temperatures under worst-case conditions, the fan may produce an annoying level of sound. Controlling fan speed is the obvious solution. If the system includes a system-management bus, you can add one of the many available sophisticated ICs for controlling fan speed. But if such a bus is unavailable, you need a stand-alone fan-speed controller (**Figure 1**).

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Power comes from the 12V supply, and a dc/dc converter, IC_1, steps down the input voltage to an intermediate voltage for powering the fan. The transfer function of this voltage is a function of resistors R_1 and R_2 and thermistor RT_1. The thermistor is an NTC (negative-temperature-coefficient) type, so the output voltage increases with increasing temperature. The output voltage is approximately 5.5V at room temperature and increases to 12V at approximately 47°C (**Figure 2**). You can easily select the ratio of resistors R_1, R_2, and RT_1 by using a spreadsheet. Note that thermistor manufacturers' tables of resistance ratio versus temperature are easier to use than are the cumbersome equations for thermistor resistance.

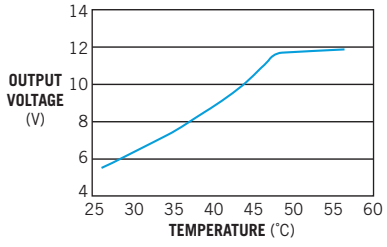


Figure 2 **Output voltage for the circuit in Figure 1 varies with temperature.**

Because the circuit in **Figure 1** does not monitor fan speed or current, it includes R_3, C_1, and D_1 to ensure that the fan starts turning during start-up. The time con-

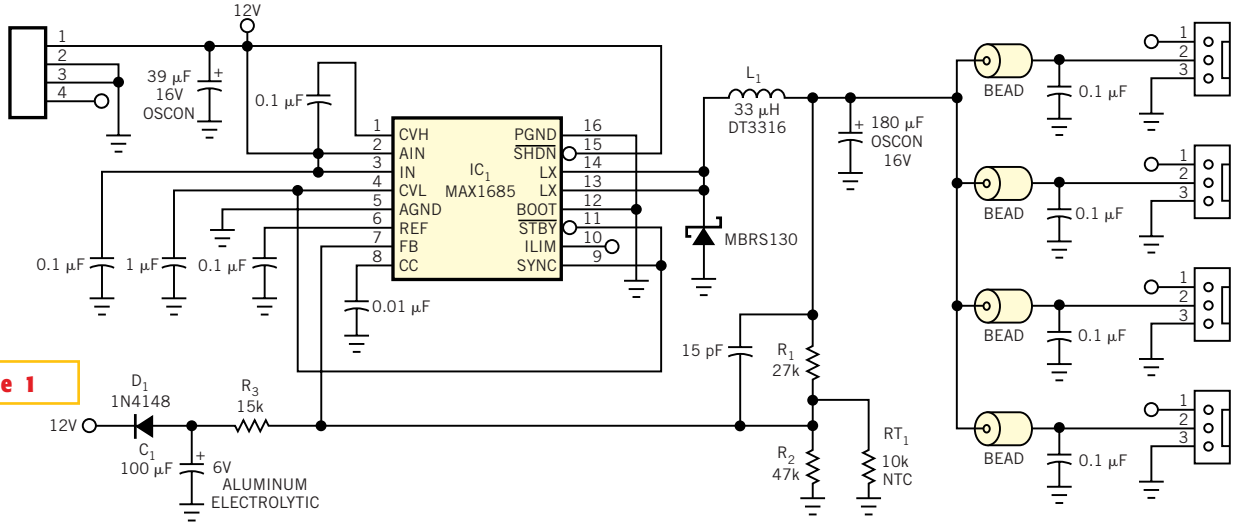


Figure 1 **To control fan speed, thermistor RT_1 adjusts the output voltage of this dc/dc converter.**

stant of R_3 and C_1 serves that purpose by causing IC_1's output to overshoot during the first few seconds of operation. After the fan starts, it easily sustains rotation at the lower operating voltages. An important criterion in selecting a dc/dc converter is the ability to operate at 100% duty cycle. IC_1 satisfies that requirement and offers the convenience of an internal power MOSFET. IC_1 supplies as much as 1A output current, which is enough to drive one to four standard fans. As an added benefit, its high efficiency helps to minimize the heat that the circuit removes.□

Simple circuit forms multichannel temperature monitor

Susan Pratt, Analog Devices, Limerick, Ireland

You can use an ADT7461 single-channel temperature monitor, an ADG708 low-voltage, low-leakage CMOS 8-to-1 multiplexer, and three standard 2N3906 pnp transistors to measure the temperatures of three separate remote thermal zones (**Figure 1**). Multiplexers have an inherent-resistance on-resistance; the channel matching and flatness of this resistance normally results in a varying temperature offset. The ADT7461 temperature monitor in this system can automatically cancel resistances in series with the external temperature sensors. The resulting system is a multichannel temperature monitor. The resistance is automatically cancelled, so on-resistance flatness and channel-to-channel variations have no effect. Resistance associated with the pc-board tracks and connectors is also cancelled, thus allowing you to place the remote temperature sensors some distance from the ADT7461. The system requires no user calibration; therefore, you can connect the ADT7461 directly to the multiplexer.

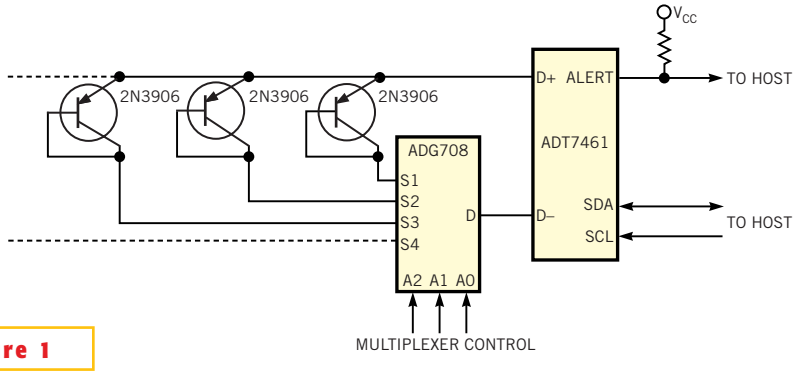


Figure 1 This system measures the temperatures of three remote thermal zones.

The ADT7461 digital temperature monitor can measure the temperature of an external sensor with ±1°C accuracy. The remote sensor can be a substrate-based or discrete transistor and normally connects to the D+ and D− pins on the ADT-7461. In addition to the remote-sensor-measurement channel, the ADT7561 has an on-chip sensor. The diode-connected transistors with their emitters connected together connect to the D+ input of the ADT7461, and each of the base-collector junctions connects to a separate multiplexer input (S1 to S3). You effect the connection of the selected remote transistor to the D− input by addressing the multiplexer, which is digitally controlled by address bits, A2, A1, and A0. The ADT7461 then measures the temperature of whichever transistor connects through the multiplexer.

The ADT7461 measures the temperature of the selected sensor without interference from the other transistors. **Figure 2** shows the results of measuring the temperature of three remote temperature sensors. The sensor at address 000 is at room temperature, the sensor at address 001 is at a low temperature, and the sensor at address 010 is at a high temperature. When you select no external sensor, the "open-circuit" flag in the ADT7461 register activates, and the Alert interrupt output asserts. You can expand the system to include as many external temperature sensors as you require. The limiting factor on the number of external sensors is the time available to measure all temperature sensors. If you require two-wire serial control of the multiplexer, you can use an ADG728 in place of the ADG708.□

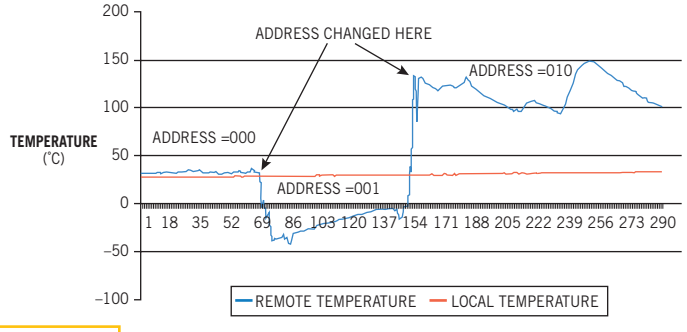


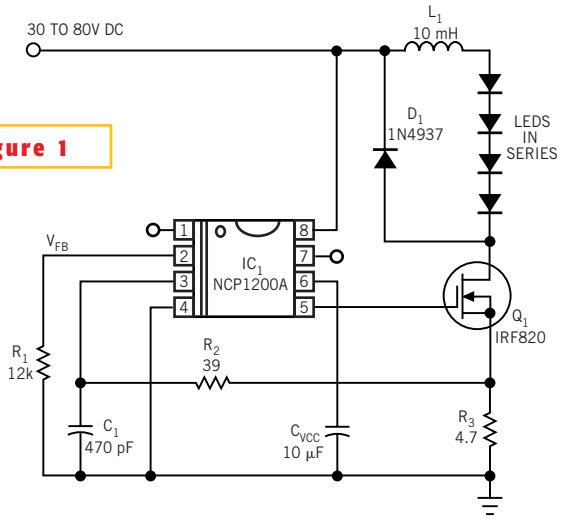
Figure 2 The ADT7461 measures the temperature of the selected sensor without interference from the other transistors with these results for ambient-, hot-, and cold-temperature measurements.

PWM controller drives LEDs from high-voltage lines

Christophe Basso, On Semiconductor, Toulouse, France

Powering LEDs from a wide dc range—say, 30 to 380V—without wasting a lot of power in the regulating block, is a difficult task when the LED current needs to be constant. Dedicated LED drivers are available, but they usually implement boost structures and are thus inadequate for high-voltage inputs. The NCP1200A, a high-voltage controller from On Semiconductor (www.onsemi.com), can serve as a constant-current generator if you add a simple coil in series with a power MOSFET. If you insert diodes between the coil and the MOSFET, the circuit becomes an economical light generator. Furthermore, there is no need for a transformer or any kind of external supply, because the controller directly connects to the rectified high voltage and thus supplies itself (**Figure 1**).

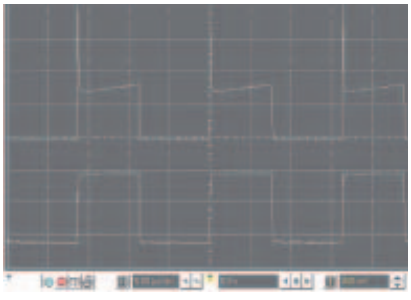
Figure 1



A high-voltage controller makes an ideal off-line LED driver.

The circuit forces a current to build up in the L_1 coil and the LEDs until the voltage developed across R_3 reaches $V_{FB}/3.3V$. At this point, power switch Q_1 turns off, and the magnetizing current keeps circulating in the coil and LEDs, thanks to freewheeling diode D_1. To maintain a "clean" current in the LEDs, L_1 must be large enough to keep the ripple to an acceptable value and to avoid pushing the controller to the minimum on-time (400 nsec) in high-line conditions. Because of the poor T_{RR} (reverse-recovery time) of the LEDs, you must add an external filter, comprising R_2 and C_1 to the IC's internal leading-edge-blanking circuitry. R_1 sets the voltage-feedback level; keeping it lower than 3.3V prevents the NCP1200A's internal short-circuit protection from tripping. In the example, the feedback voltage of 2.5V thus imposes a peak current of 2.5/3.3/4.7=161 mA.

Figure 2



The prototype with low line voltage provides these typical signals.

In this application, the line goes as high as 380V dc. At steady state, L_1 and V_{IN} dictate the on-time, whereas the reset voltage applied to L_1 fixes the current decrease during off-time. This reset voltage, V_{FTOTAL}, equals the total LED forward voltage plus the forward drop of the freewheeling diode. The total reaches approximately 12V in this example. It can obviously vary, depending on the type of LED you want to drive, especially with white LEDs that incur significant forward drops of approximately 3V. To help derive the inductance value corresponding to your needs, a few lines of algebra suffice: $t_{OFF}=L_1(\Delta I/V_{FTOTAL})$ and $t_{ON}=L_1(\Delta I/V_{IN})$, where ΔI is the ripple current in L_1, V_{FTOTAL} is the previously described reset voltage, and V_{IN} is the dc input voltage. Because the circuit runs in continuous-current mode, the sum of on-time and off-time gives the switching period of the 1200AP60: $L_1(\Delta I/V_{FTOTAL})+L_1(\Delta I/V_{IN})=1/f_S$, where f_S is the switching frequency. Extracting L_1 yields $L_1=(1/f_S)[(V_{FTOTAL}\times V_{IN})/(V_{FTOTAL}+V_{IN})](1/\Delta I)$.

If you select a ripple current of 20 mA peak-to-peak at 380V dc, then $L_1=16.66\times11.6\times50=9.6$ mH. From this value, you can check the minimum on-time using the equation: $t_{ON}=9.6mH\times0.02/380=508$ nsec, above the minimum limit. **Figure 2** portrays typical signals captured on the prototype supplied with low line voltage.□

Circuit forms satellite-dish command decoder

Mark Giebler, Oakdale, MN

By decoding the commands sent by a direct-broadcast satellite receiver that uses the DISEQC (digital-satellite-equipment-control) protocol, you can troubleshoot the commands or simply listen in. Eutelsat Corp (www.eutelsat.com) offers the DISEQC protocol. The technique uses only the coaxial cable between the receiver and the dish to send commands for actions such as changing the low-noise-block frequency range or switching between dishes for multisatellite reception. The DISEQC protocol specifies a bit time of 1.5 msec and bit values as shown in **Figure 1**, the timing diagram of bit modulation on the coaxial cable. The signal's ac portion is a 22-Hz burst whose amplitude ranges from 300 to 600 mV. A voltage-doubler circuit detects the 22-Hz portion, producing a pulse stream in

which constant-voltage pulses having amplitudes of 0.6 to 1.2V replace the 22-Hz bursts.

Decoding this bit stream into ASCII hex values is an ideal job for a low-cost 8-bit microcontroller. Using a microcontroller with onboard flash memory, such as the NEC Electronics μPD78F9418A (www.necelam.com), eliminates the need for external memory. The only external components are a few discrete devices for the signal detector and the coaxial-cable loop-through (**Figure 2**). You can add an RS-232 driver if you want to display the ASCII codes on a laptop computer via HyperTerminal. You can also use the μPD78F9418A's onboard LCD controller to display the codes on a dedicated display.

One of the μPD78F9418A microcontroller's 10-bit A/D converters performs pulse detection and acts as a simple timing device. Using a reference voltage of 5V, the converter provides approximately 4.88 mV per step. An A/D-converter conversion value greater than 120 counts (585 mV) represents a valid pulse. Set the A/D converter's conversion time to 28.8 μsec and wait to detect a pulse edge by reading the A/D converter until its value exceeds 120 and then perform a loop while doing analog-to-digital conversions. If the loop count reaches 24 with ADC values greater than 120, the bit is a zero. If the pulse has gone away, the bit is a one. Any extra delay from executing instructions in the loop has little effect, because the bit windows leave plenty of margin.□

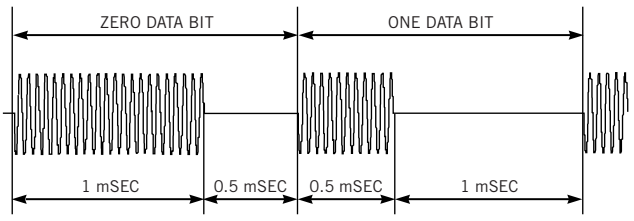


Figure 1 The DISEQC protocol specifies a bit time of 1.5 msec and these bit values.

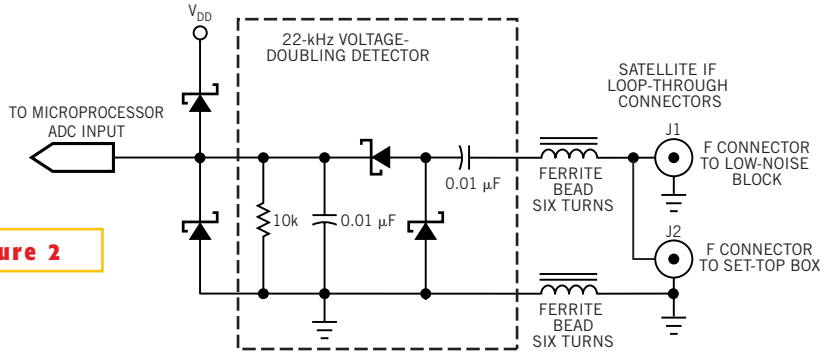


Figure 2 This circuit enables the microcontroller to decode the DISEQC-protocol bit stream.

Use a microcontroller to design a boost converter

Ross Fosler, Microchip Technology, Chandler, AZ

Boost converters, like other switchers, have traditionally received their control signals from a dedicated circuit. However, a recent trend is to integrate simple switching-power-supply building blocks into generic devices, such as microcontrollers. An excellent example of this concept is a microcontroller that combines digital and analog circuitry and makes it easier to build simple power supplies. The programming capability of a microcontroller is an added benefit in power-supply designs, especially when you want to experiment with the supplies. **Figure 1** illustrates a simple boost-converter design using a microcontroller; the basic boost topology in **Figure 1** is a type of flyback circuit. The basic concept is easy to understand. When the MOSFET, Q, turns on, the current flowing through the inductor, L, begins to ramp up linearly (**Figure 2**), resulting in energy storage in the inductor. The MOSFET turns off before the inductor saturates. At this time, the inductor releases its energy to the storage capacitor, C, and the load.

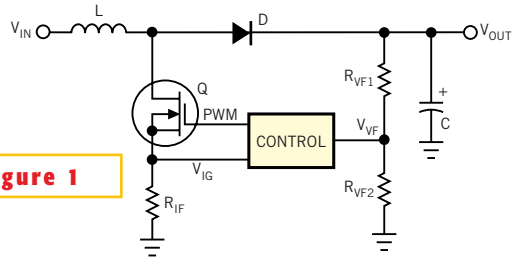


Figure 1 This circuit block represents the basic topology of a boost converter.

You can design a simple boost converter with the following conditions: V_{IN}=9V, V_{OUT}=18V, R_{LOAD}=72Ω, F=1/T=62.5 kHz, η=70%, and ΔV_{DROP}=50 mV, where F is the switching frequency, η is the efficiency, and ΔV_{DROP} is the output ripple voltage. You can calculate the on-time, current, ramp-down time, and the total period in terms of inductance:

$$\frac{2L\,V_{OUT}^2}{R_L\,\eta\,V_{IN}^2} = t_{ON} = 0.1587L.$$

$$\frac{V_{IN}}{V_{OUT}-V_{IN}}\,t_{ON} = t_R = 0.1587L.$$

$$\frac{t_{ON}+t_R}{\eta} = T = 0.4535L.$$

Then, you calculate the peak current through the inductor and the inductance value:

$$\frac{V_{IN}}{L} t_{ON} = I_{PEAK} = 1.428A.$$

$$L = 35.28\ \mu H \approx 33\ \mu H.$$

Finally, you calculate the capacitance based on the ripple voltage:

$$\frac{I(T-t_R)}{\Delta V_{DROP}} = C = 208\ \mu F \approx 220\ \mu F.$$

Note that the design is slightly altered to use readily available components, by using a 33-µH inductor and a 220-µF capacitor. The difference in the inductor value is absorbed in the dead time, as is the power loss.

The control circuit can take many forms, especially if you choose a device such as the PIC16C782 microcontroller. This device integrates a built-in analog peripheral set, diverse analog visibility, and a mixed-signal PWM block. The control circuit in **Figure 3** demonstrates how the analog and pulse-width modulation is contained within the PIC16C782, with the exception of the FET driver. This control circuit combines analog current control and firmware voltage control. The interesting part is the firmware, which is directly in the voltage-feedback path of the control loop. Through firmware, you can alter the dynamics of the control loop by changing the functions within the program. You may be able to design an adaptive power-control system by adjusting the phase and gain to meet the desired needs of a system.

Firmware placement within the control loop is not the only possibility; you could use a combination of firmware and hardware to monitor the system. Because the analog information is visible and the analog functions are controllable within the PIC16C782 device, you can monitor an active system for performance and function. In essence, the system can have self-diagnostic capabilities to check stability, load, input and output conditions, or anything else a system may require. You can also obtain Information about the system, through a serial port or some other means, by routing the data to a terminal or computer display. Even better, the firmware allows the design to change the functions without changing hardware. This approach eases experimentation; you simply changing firmware rather than spending hours in the lab adding or changing parts.

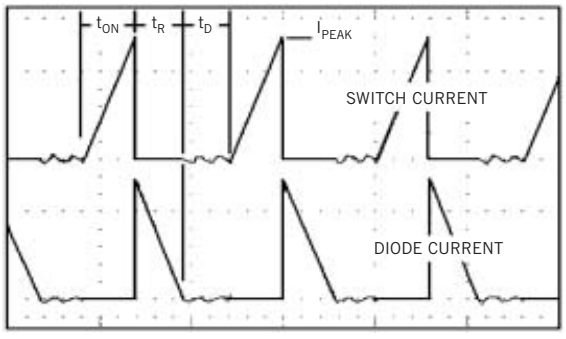


Figure 2 These curves show the switch and diode currents in the circuit of Figure 1.

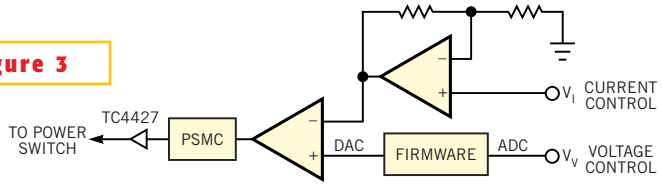


Figure 3 A microcontroller contains all the elements necessary for boost-converter control.

Figures 4 and **5** are oscilloscope photos from a working example of the boost converter implementing the basic topology in **Figure 1** and the control block in **Figure 3**. The peak current in the inductor is 0.3 mV×0.2Ω= 1.5A (**Figure 4**). The on-time is approximately 5.9 µsec. The output voltage is 18V into a 72Ω load (**Figure 5**). The efficiency is approximately 90%. These boost-converter design and control ideas are just a few of the many possible ones using a PIC16C782 device.□

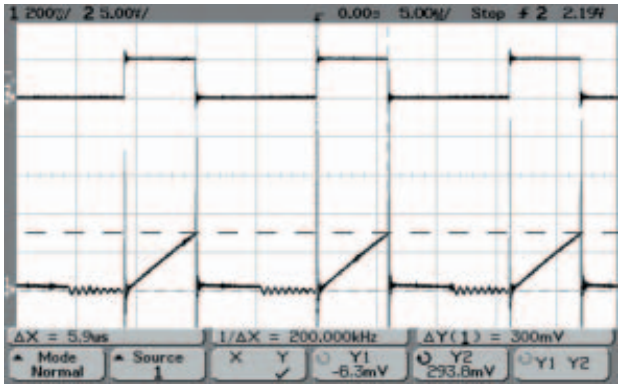


Figure 4 A working example of the boost converter implementing the basic topology of Figure 1 shows the duty cycle (top) and the current-ramp-down waveform (bottom) for the circuit in Figure 1.

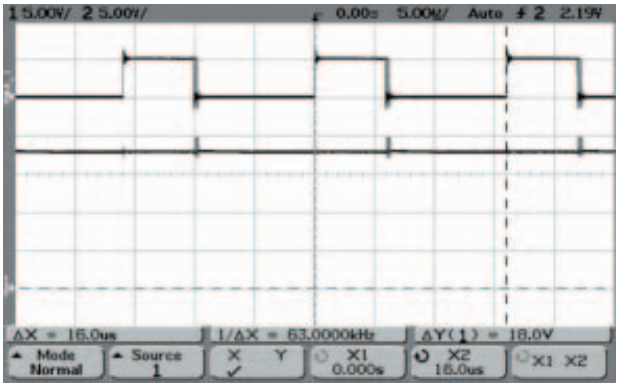


Figure 5 The example shows the duty cycle (top) and the output voltage (bottom) of the circuit in Figure 1.

Edited by Bill Travis

Motor uses simple reverse-battery protection

Dongjie Cheng, Allegro Microsystems, Warminster, PA

THIS DESIGN IDEA presents a low-side, reverse-battery-protection technique for a dc-motor system. The system in **Figure 1** incorporates two protection options. The common practice of using a diode for reverse-battery protection does not work with dc motors' inductive loads. In **Figure 1**, an Allegro (www.allegromicro.com) A3940, a low-cost power MOSFET controller, drives a dc motor. An H-bridge for driving the motor comprises the n-channel MOSFETs Q_0 to Q_3. To change the motor's direction from forward (current flowing from Phase A to Phase B) to reverse, the direction of current in the motor winding must reverse. This reversal means that Q_0 and Q_3 switch from on to off, and Q_1 and Q_2 switch from off to on. For an inductive load, the induced voltage, E, produced by a change in current is E=L(di/dt), where L is the inductance, and di/dt is the rate of change of the current. The induced voltage opposes any change in current. Therefore, after the switches attempt a current reversal, current continues to flow forward (forced by the induced voltage) from ground back to the power supply through Q_2 and Q_1. The current gradually decays to zero and then reverses direction. If a reverse-battery-protection diode is present in the current path, the decaying current is blocked and a large voltage can develop across the protection diode. Thus, the normal current recirculation meets interference. Further, the protection diode may break down, and potentially destructive voltages can appear on the FETs and the IC.

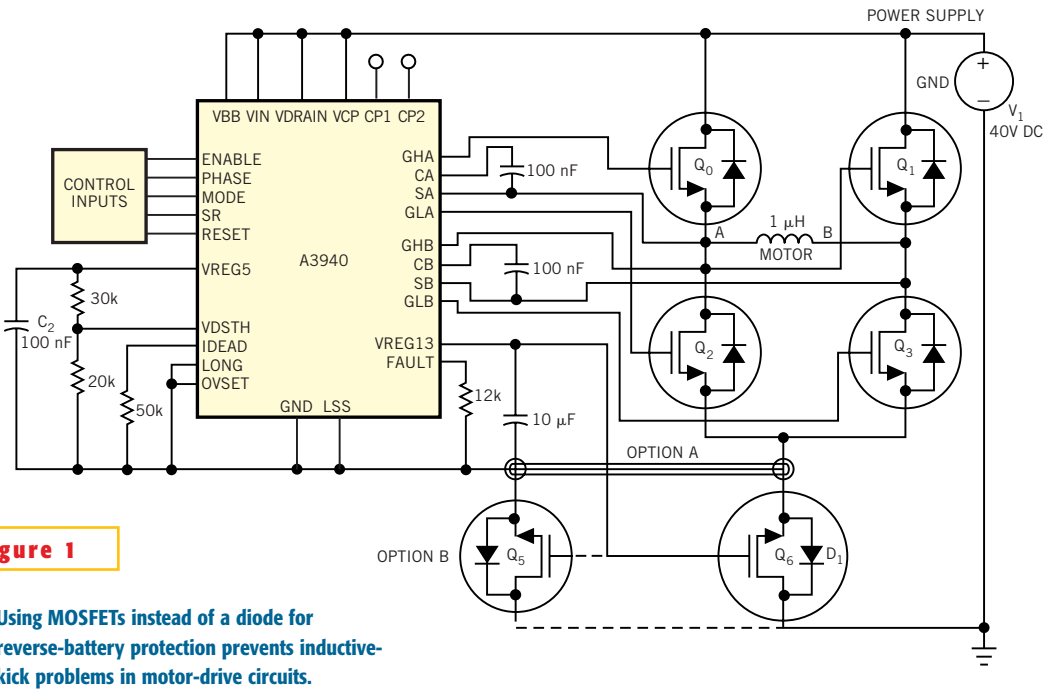


Figure 1

Using MOSFETs instead of a diode for reverse-battery protection prevents inductive-kick problems in motor-drive circuits.

Figure 1 shows how to implement reverse-battery protection using the n-channel MOSFET, Q_6, at the ground (low side) of a power supply. You can use either Option A (solid line) or Option B (broken line) to complete the circuit protection. If you use Option A, remove Q_5. If you use Option B, you should cut open the bold trace marked "Option A." In both options, Q_6 is connected such that its source connects to the H bridge, its drain to the power-supply ground, and its gate to the VREG13 output (a regulated 13.5V). At power-up, the body diode of Q_6, D_1, is forward-biased and provides the dc current path that allows the IC to power up. As the VREG13 regulator powers up, it turns on Q_6, which provides a lower resistance path to ground than does the body diode, D_1. Thus, Q_6 connects the IC's ground and the power supply's ground. In normal operation, the motor current in the H bridge can flow from the power supply to ground or from ground back to the power supply through Q_6. In the case of a reverse-battery condition, Q_6 stays off, because the VREG13 voltage is

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not available and the Q_6 body diode, D_1, is reverse-biased, preventing any reverse-current flow.

We devised Option B because of a concern that switching noise may appear at the IC's ground if Q_6's on-resistance is not low enough. By opening the connection labeled Option A, you isolate the IC ground from the potentially noisier connection at the source of Q_6. Q_5 is configured and operates in the same fashion as Q_6. Q_5 can have higher on-resistance than Q_6, and, in this configuration, you may relax the on-resistance requirements for Q_6. Experiments have demonstrated that both options work equally well if you carefully choose Q_6's on-resistance.□

Simple setup tests bit-error rate

Israel Schneiderman, Rosslare Israel Ltd, Rosh Ha'ayin, Israel

Traditionally, the reception quality of a digital receiver is expressed in terms of BER (bit-error rate). This figure is the proportion of received bit errors in a given period. Typically, you measure the BER in the lab by applying an RF signal, modulated by a pseudorandom code, to the receiver under test. This Design Idea suggests an alternative method based on the use of a simple square wave. This method may not be superior to the usual technique, but it is simple to implement and gives a reliable result. The simplicity of the method is based on the fact that it requires no complex synchronization. Admittedly, a square wave is not truly representative of the data a receiver encounters in normal use (**Figure 1**). The square wave to modulate the RF carrier is phase-shifted to allow for the delay in the receiver. An exclusive-OR gate produces a sampling pulse at each bit transition—typically, 10% of the data-bit width. This sample pulse samples the raw data the receiver generates, producing clean data.

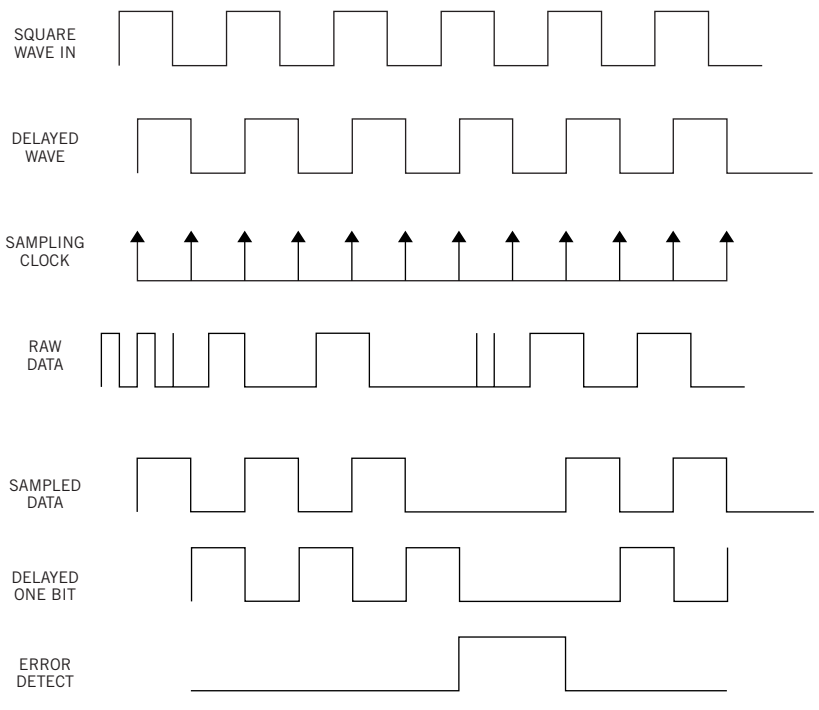

Figure 1 This timing diagram illustrates the operating principles of a simple BER tester.

The key to understanding this technique is to keep in mind that a string of two successive ones or zeros indicates an error. A D flip-flop implementing a 1-bit delay detects the error.

You can display error pulses on an oscilloscope or count them by using a frequency counter. **Figure 2** shows a typical test setup. You modulate the RF generator at the prescribed data rate. Note that a 500-Hz square wave is equivalent to a baud rate of 1 kbps. Both the modulating signal and the received data feed into the BER-test board. You adjust the sampling signal to be near the end of the received-data pulse. In many digital receivers, this arrangement yields a fair approximation to a correlation receiver. Error pulses appear on the oscilloscope. If you wish, for example, to set the RF level for a BER of 1-to-100, you reduce the RF level to the receiver such that, in a 100-msec sweep you see, on average, one error pulse per sweep.

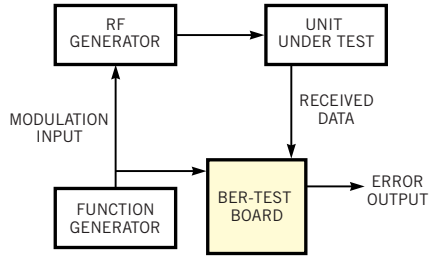

Figure 2 The BER tester uses a signal generator with OOK (on/off-key) modulation.

In **Figure 3**, IC_1 and potentiometer P_1 form the basis of an adjustable phase shifter. R_2 provides hysteresis, and R_1, C_1, and IC_2 form a differentiator that provides a sampling pulse train. The first flip-flop clocked by the sampling pulse makes a hard decision concerning each bit. The next D flip-flop, together with exclusive-OR gate IC_{2B} detects the occurrence of two successive identical bits.

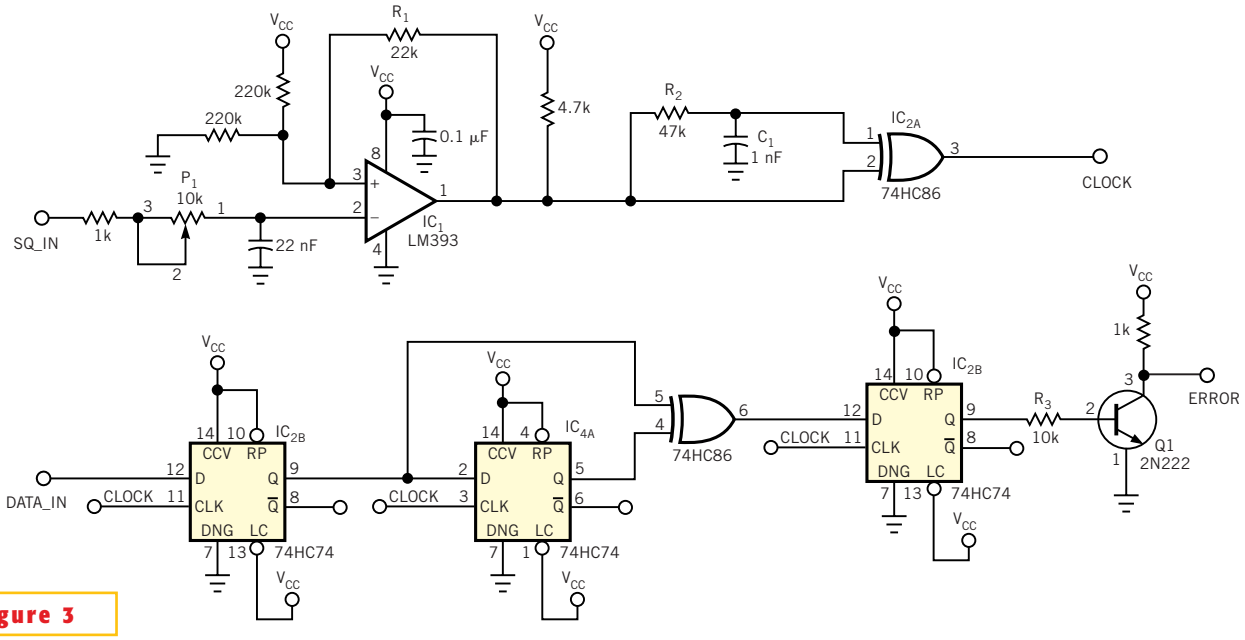

Figure 3

The simple BER tester uses an adjustable phase shifter and a differentiator.

This situation constitutes an error. A final D flip-flop and a transistor ensure that the Error output is clean. The construction of the system follows the circuit diagram in **Figure 3**. It sets an HP8647 RF signal generator at 868.35 MHz, and a function generator provides OOK (on/off-key) modulation. The receiver under test was a Melexis (www.melexis.com) TH7122 at 868.35 MHz in the OOK-modulation mode. Adjust the RF level to vary the error rate. This design obtains an RF level of −107 dBm for a 1-to-1000 BER and −108 dBm for a BER of 1-to-100, levels consistent with the data sheet. You should take care when you're implementing OOK. Most RF generators provide AM. Thus, you must remove 3 dB from the displayed RF value. You can use this technique for other types of binary modulation, such as FSK (frequency-shift keying), for example.□

Solar-powered motor runs on 10 nA

Stepan Novotill, Victoria, BC, Canada

Designs for solar-powered applications with low-duty-cycle requirements can often rely on capacitors for energy storage in place of less reliable batteries. Typical applications include solar positioning, telemetry transmitters, chemical pumps, data loggers, and solar-powered toys. The circuit in **Figure 1** can run a small pager motor from the output of a small calculator-type solar cell in near darkness. The circuit works by repeatedly charging a 4700-µF capacitor, C_1, to 1.75V and then dumping the charge into the motor. Only the self-leakage current of the solar cell limits low-light operation. The circuit itself has such low leak-

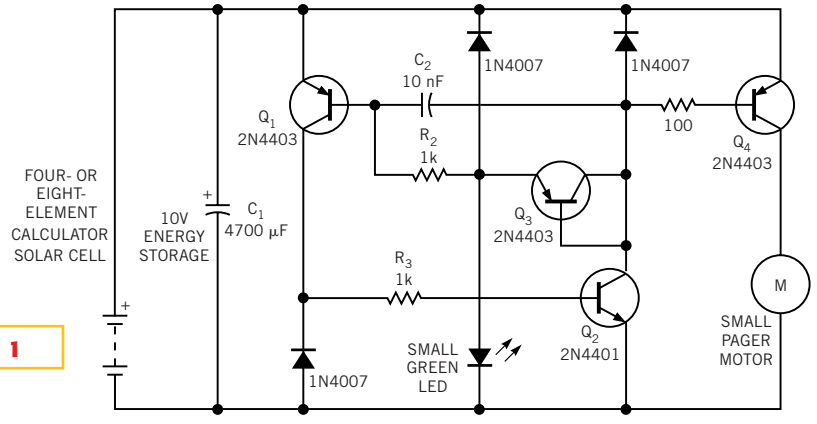

Figure 1

By repeatedly charging a storage capacitor and then dumping its charge into a small motor, this circuit can run the motor on only 10 nA of current.

age currents and trigger-current requirements that it can run the motor on 10 nA of current if you use a low-leakage energy-storage capacitor. Transistors Q_1 and Q_2 form a regenerative pair similar to a thyristor. The 1N4007 diodes take the place of pullup and pulldown resistors, and the diodes bypass the leakage current of the transistors and LED.

As the C_1's charge approaches 1.75V, the green LED starts to conduct, causing Q_1 to turn on and feed current to the base of Q_2. The amplified base current appears as a disturbance at the collector of Q_2. The emitter-base drop of output transistor Q_4 isolates the collector of Q_2 from the output transistor, and the emitter-base-drop of Q_3 and the 10-nF capacitor, C_2, isolate Q_2 from the dc bias at the base of Q_2. However, the nanoamp-magnitude ac disturbance at the collector of Q_2 couples into the base of Q_1 via C_2, causing fierce regenerative action. You achieve nanoamp triggering and charging of C_1 through the use of leakage diodes in place of pullup resistors, through isolation of the load at the start of regeneration, and through the dc isolation of Q_1's bias voltage from the collector of Q_2 at start of regeneration. As regenerative action continues, a dc latching path appears between the base of Q_1 and the collector of Q_2 through transistor Q_3. At this point, output transistor Q_4 also enters saturation, and the motor runs.

The high motor load quickly discharges C_1 toward 1.1V, at which point Q_1 can no longer sustain regenerative action because of the voltage loss in the emitter-collector junctions of Q_1 and Q_3. The 100Ω resistor and the reverse charge on C_2 drive Q_1 into cutoff and another energy-storage-capacitor charging cycle begins. Substitute a blue LED for the green one or add diodes in series with the LED to increase circuit-firing voltage beyond 1.75V. You can use 10-MΩ resistors in place of 1N4007 diodes to improve noise immunity if you don't need less-than-1-μA operation. Capacitors become leaky if you leave them in storage. You may need to condition such capacitors by applying a 9V battery to the capacitor for a few days. Use two solar panels in series to provide enough voltage for very-low-light operation.□

Photovoltaic switch disables unused LEDs

Lance McBride, Monterey Bay Aquarium Research Institute, Moss Landing, CA

In many applications, it's desirable to disable LEDs used for system verification. Many options are available for the disabling function, including manual SPST (single-pole single-throw) switches, enhancement- and depletion-mode MOSFETs, bipolar-junction transistors, and JFETs. The circuit in **Figure 1** automatically disables the LEDs when a mechanical housing encloses the circuit card, thereby preventing you from accidentally leaving the LEDs on to waste power. The main switch portion of the circuit comprises an amplified photovoltaic cell (photodiode) and a small, n-channel MOSFET. The amplified photodiode signal provides drive to the MOSFET's gate when enough light is available. Because the photodiode generates its own power from the available light, the amplified photodiode IC consumes only microwatts in a unity-gain configuration.

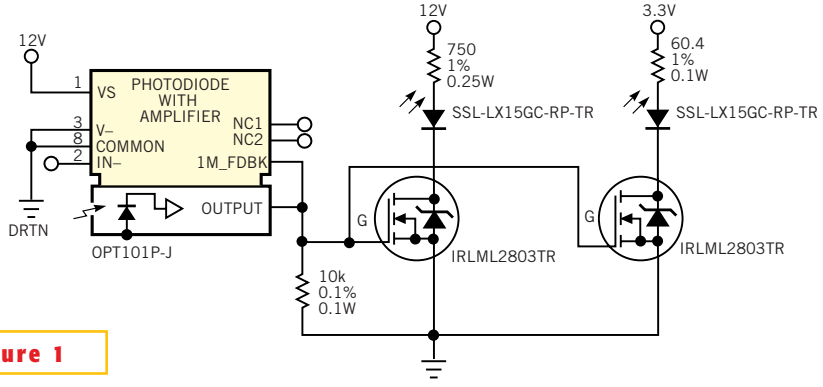

Figure 1

This circuit configuration turns off unneeded LEDs when it's dark.

Originally, I considered using a series string of photodiodes to directly drive the MOSFET's gate. However, the integrated OPT101 design provides reliable operation under a number of light conditions. If you adjust the gain of the amplifier, the circuit can function in both bright and dim applications. I use multiple MOSFETs for unique voltage ranges in which the LED would suffer damage from excessive reverse-bias voltages. This precaution is important in a design with multiple power-supply voltages. For instance, if you used only one MOSFET to control the LEDs in a design using 3.3 and 12V supplies, the reverse voltage across the 3.3V LED would be 8.7V when the switch is off. This reverse voltage exceeds the absolute maximum rating for many LEDs. If you need to control status LEDs using a microcontroller or some other logic-level device, add another MOSFET between the LED and the light-switch circuit. This configuration allows the light switch to act as a master on/off switch and the logic device to act as a secondary on/off control.□

Boost converter works with wide-range negative-input supply

Mike Wong, Intersil Corp, Milpitas, CA

Assume that a design requires positive voltage, but only a negative-voltage power source is available. Using a standard boost-converter IC in the circuit of **Figure 1**, you can efficiently generate a positive voltage from a negative source. The boost converter generates an output voltage that's higher than the input voltage. Because the output voltage—5V in this example—is higher than the negative-input-voltage ground level, the circuit does not violate the boost-converter principle. The circuit in **Figure 1** uses the EL7515, a standard boost converter. The ground pins of the converter IC connect to a negative-voltage input source. Ground becomes the "positive" input source. V_{OUT} is as follows: $V_{OUT} = -V_{FB}(R_2/R_1) = -1.33V\ (37.5k\Omega/10k\Omega) = -5V$. The Q_1 and Q_2 pnp transistors form a translator that scales the 5V output voltage (referred to ground) to a feedback voltage referred to the negative input. The transistor pair also eliminates temperature-change and voltage-drop effects. As the negative input voltage decreases, Q_2 runs at an increasingly higher current than Q_1, causing additional transistor-offset mismatch.

For optimal line regulation, you should set Q_1 and Q_2 to operate at the same currents with the nominal input-voltage applied. **Figure 2** shows the line-regulation results. The maximum output-to-input voltage difference must be within the boost converter's internal power FET drain-to-source breakdown voltage (V_{DS}). For the EL7515, the maximum V_{DS} is 18V. For the 5V output, the minimum (most negative) input voltage is −12V. A 1V safety margin compensates for the D_1 diode drop and any voltage spikes on the drain of the power FET. **Figure 3** shows the load-regulation test results. The maximum output current is a function of the input-to-output voltage ratio and current-limit setting of the boost converter. As **Figure 4** shows, the circuit yields greater than 80% efficiency at 200-mA output.□

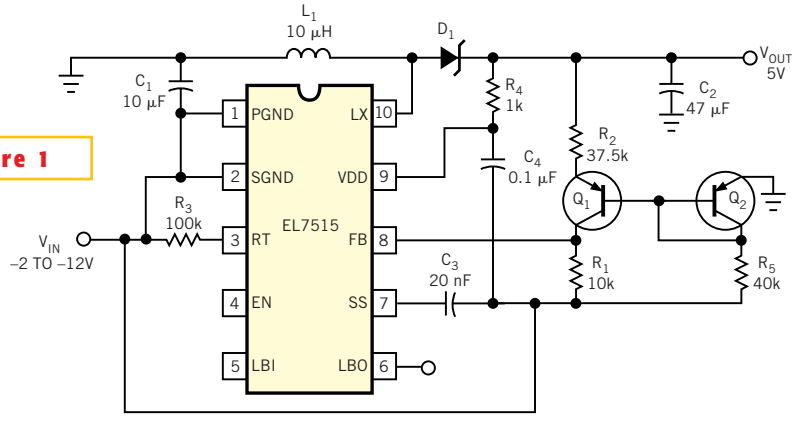

Figure 1

By using its ground terminals as the negative-voltage input, a boost converter can efficiently generate a positive output voltage.

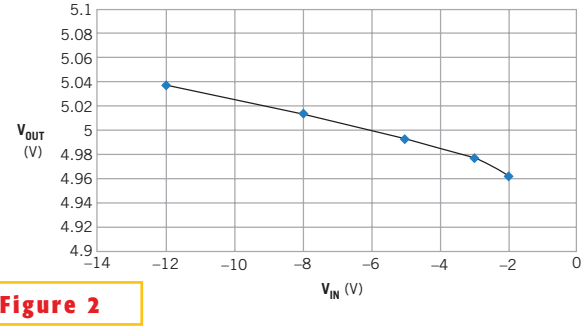

Figure 2

The line regulation is within ±40 mV over the full range of negative inputs.

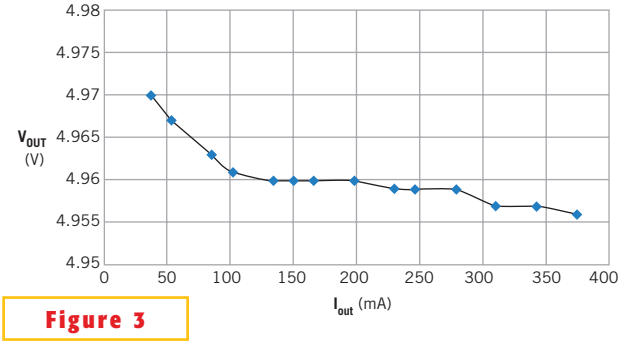

Figure 3

The output voltage varies by less than 14 mV over the full range of output currents.

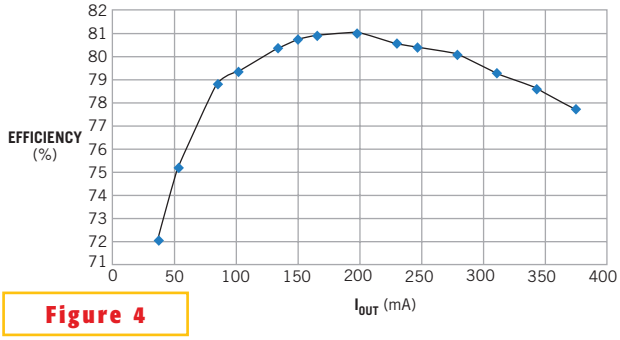

Figure 4

The efficiency of the circuit peaks at 81% for medium output current (200 mA).

Edited by Bill Travis

Positive feedback yields fast amplifier with precision dc offset

Steve Woodward, Chapel Hill, NC

Some signal-processing applications require a high-speed, low-noise, dc-coupled amplifier that incorporates a precision dc-offset adjustment. Examples include oscilloscopes, in which the offset adjustment typically acts as a "position" control), ADC-input gain blocks, and scanning-ion-beam-microscopy deflection circuitry. **Figure 1** illustrates the circuit concepts. Op amp IC_{2A} is a 70-MHz, high-slew-rate device configured with a fixed gain of 3 (9.5 dB) and a ±10V precision offset adjustment. Op amp IC_{1A} buffers and thereby linearizes the offset potentiometer. IC_{1A} is a low-cost, low-frequency device that befits the dc circuit it occupies. But the mismatch between the frequency responses of IC_2 and IC_{1A} creates the need for the novel topology of **Figure 1**. An obvious way to couple IC_{1A} and IC_{2A}, which might seem to allow the addition of dc offset, would be to omit R_1, R_2, R_5, and C_1 and simply connect IC_{1A} as a unity-gain buffer providing the termination for the gain-set resistor, R_3. Unfortunately, this scheme wouldn't work, because the output impedance of the pokey IC_{1A} starts rising at frequencies far below the capabilities of the speedy IC_2.

This drawback would ruin the high-frequency performance of the composite

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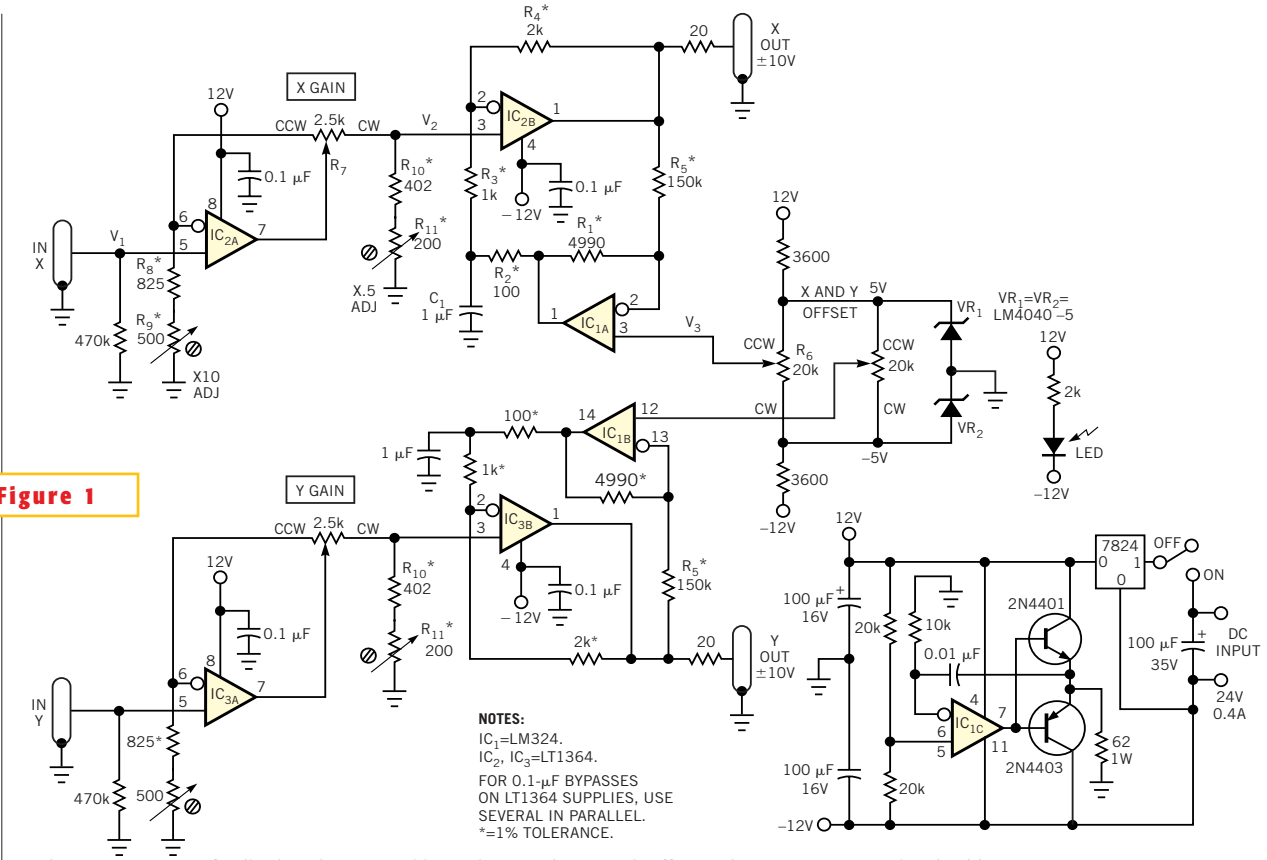


Figure 1

In this circuit, positive feedback makes it possible to obtain wide-range dc offset without compromising bandwidth.

amplifier. You could (partially) avoid this problem by using another LM1364 in place of the LM324, but the result would be a significantly noisier circuit because of the summation of IC_{1A}'s output noise with the signal at point V_2. This Design Idea offers a different approach, in which C_1 provides a robust, low-impedance termination for R_3, and the R_2C_2 time constant isolates the signal path from noise originating in either IC_{1A} or the VR_1 and VR_2 voltage references. Unfortunately, this approach creates a problem arising from R_2's dc resistance. C_1 holds down the bottom end of R_3 for ac-signal frequencies higher than 1 kHz or so. But near dc, R_2 and R_3 tend to sum, and the summing action would make the closed-loop gain of IC_2 approximately 10% less for dc-signal components than for ac. The circuit avoids this effect by using positive feedback that R_1 and R_5 provide.

The dc gain that R_1 and R_5 provide generates a compensation-voltage component that nulls the voltage drop across R_2. This action cancels the tendency of the R_3C_1 node to track IC_{2A}'s input and makes IC_2's output accurately equal to $V_{OUT}=V_2(1+R_4/R_3)-V_3(R_4/R_3)=3V_2+2V_3$. The rest of the schematic illustrates the use of the offset circuit in a dual-channel amplifier. In this amplifier, the variable-gain front ends incorporate a pseudologarithmic gain adjustment spanning gains of 0.5 to 10 (−6 to +20 dB). To achieve this wide gain-control range with a single-turn potentiometer and maintain reasonable adjustment resolution without compromising the LT1364s' 20-MHz capability, the control potentiometer, R_7, is connected such that its resistance element serves two circuit functions. The left half forms a variable-gain (1 to 3.33=0 to 10.5 dB) feedback network around IC_{2A}. The right half forms a variable-loss (1 to 0.167=0 to −15.5 dB) circuit. The net result, when you combine it with the fixed 9.5-dB gain of IC_{2A}, is an overall gain variable from (0−15.5+9.5)=−6 dB when you adjust R_7 to one extreme to (10.5−0+9.5)=20 dB when you adjust R_7 to the other extreme. IC_{1C} finishes the gain-block subsystem by generating tracking ±12V rails, by splitting the ground of the 7824 24V regulator. This regulator uses as its source an inexpensive, unregulated wall-socket power supply.□

Buck regulator forms high-power, inverting −5V supply

Bruce Denmark, Maxim Integrated Products, Sunnyvale, CA

Configuring a step-down switching-converter IC as an inverter yields an efficient, high-power, −5V supply that can of deliver currents as high as 4.5A at the 12V input or 3.2A at the 5V input (**Figure 1**). Conventional inverting power supplies do their switching using a p-channel MOSFET (**Figure 2**). That configuration works well at lower currents, but has limited use above approximately 2A, depending on the input and output voltage levels and the MOSFET you use. If you compare a standard buck circuit with the circuit in **Figure 1**, you can see that the converter's "output" in **Figure 1** connects to ground, and what used to be ground becomes the −5V output (**Figure 3**). Because the on-resistance of an n-channel MOSFET is lower than that of a comparably sized p-channel device, a power supply with n-channel MOSFETs usually provides more current at higher efficiency. To turn on, however, an n-channel device requires a gate voltage approximately 4V higher than the source voltage, which is usually the supply voltage.

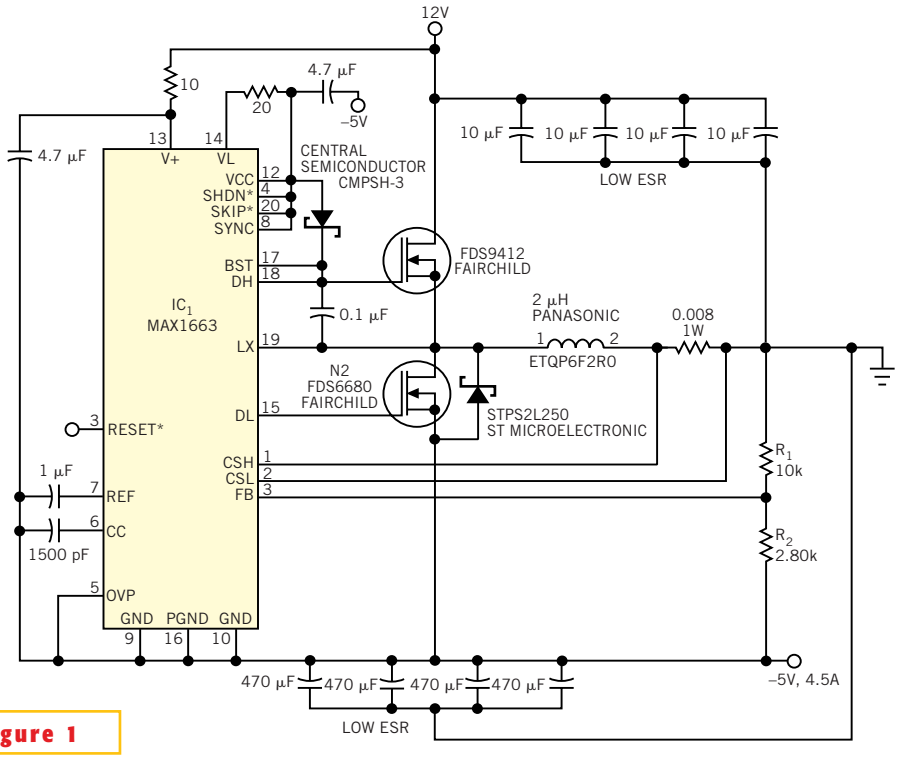
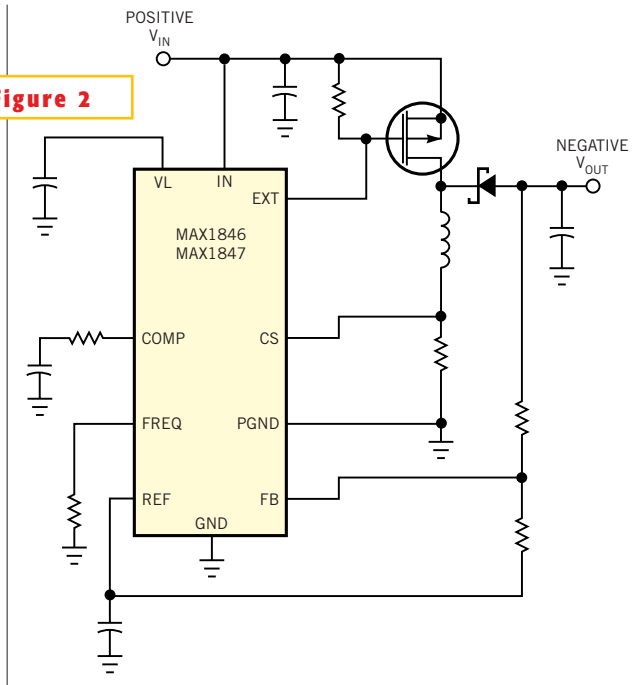


Figure 1

By configuring this high-power dc/dc step-down converter as an inverter, you can obtain 4.5A at −5V from a 12V input or 3.2A at −5V from a 5V input.

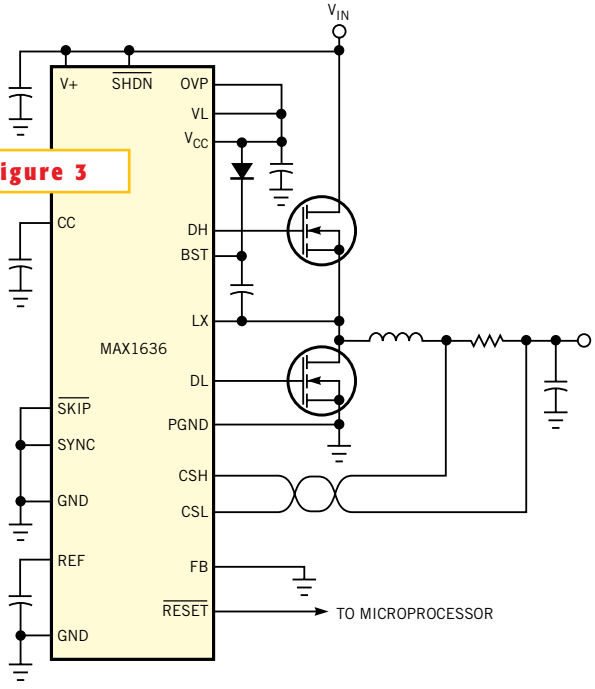
The circuit in **Figure 1** achieves high output current and high efficiency by re-

Figure 2



This conventional inverting power supply uses a relatively inefficient p-channel MOSFET.

Figure 3



IC_1 in Figure 1 normally operates as a high-power buck converter.

configuring a high-power buck converter, IC_1, as an inverter, thus exploiting an all-n-channel design. Efficiency is 90% with a 12.35V input, −5.02V output, and 4.7A load. The efficiency is 84% with a 4.56V input, −5.02V output, and 3.3A load. You can easily accommodate −5.2V applications by changing the values of R_1 and R_2. (Operation at −5.2V incurs a small penalty on maximum output current.) Input and output ripple voltages directly relate to the input and output capacitors' ESR (equivalent series resistance), so you should carefully select these capacitors. Circuit layout is also extremely important, as for all dc/dc converters. You may want to consider the MAX1636 evaluation kit from Maxim (www.maxim-ic.com). The kit includes a small pc board with optimized layout and all components necessary for operating the MAX1636. Because the board's layout is similar to the one required in **Figure 1**, the kit can serve as a rough layout guide for this Design Idea.□

Low-loss circuit powers solar lantern

Ramsesh Kumar, Bangalore, India

The solar-lantern circuit in **Figure 1** is a low-loss configuration that uses a 7W, four-pin CFL (compact fluorescent lamp) and a 12V, 7-Ahr, sealed, maintenance-free battery. The inverter features greater-than-85% efficiency, less-than-2-mA quiescent current, and a shunt-charge controller with deep-discharge and overcharge protection for the battery. The low quiescent current and the deep-discharge and overcharge protection ensure long life for the battery. The preheating feature in the inverter avoids the blackening of the end of the CFL, thereby ensuring long life. The circuit finds application in rural areas as a reliable, compact, portable light source and in urban areas as an emergency-lighting system. The shunt charge-controller circuit comprises IC_1, a low-current, voltage-reference 2.5V LM385, and IC_2, an LM324 comparator. IC_{2A}, with resistors R_1 through R_8 and transistor Q_1, provides protection against deep discharge of the battery.

The circuit switches off the load, including the inverter and the lamp, when the battery voltage falls below 10.8V and thus protects the battery from deep discharge. Under a no-load condition, the discharged battery voltage is approximately 12.2V. Hence, the circuit provides a deep-discharge reset level of 12.3V to avoid oscillations. Red LED_1 indicates a low-battery condition. IC_{2B} with resistors R_9 through R_{14} and transistor Q_2 provides protection against overcharging the battery. Q_2 switches on

TABLE 1–WINDING DETAILS FOR TRANSFORMER

Start pin	End pin	Wire gauge	Turns	Inductance
2	1	26	21	28 mH
3	4	26	21	28 mH
6	10	38	380	17 mH

Core: EE25/13/7

and shunts the solar array when the battery voltage exceeds 14.8V and thus protects the battery from overcharging. Q_2 turns off when the battery voltage drops below 12.5V and thus enables battery charging. D_2 is a reverse-blocking diode. It prevents the discharge of the battery through the solar cells when the cells are not generating electricity. Amber LED_2 indicates that the battery is in full-charge condition. Green LED_3, along with IC_{2C} and resistors R_{15} through R_{20}, provides an indication of charging.

Tables 1, **2**, and **3** give core and winding details for the magnetic components in the circuit. The inverter uses a Class D, push-pull, force-driven topology with MOSFETs as switching devices. IC_3, an SG3524, drives the inverter. The force-driven topology ensures trouble-free start-up in all environmental conditions. The switching frequency is approximately 26 kHz. Q_6, along with resistors R_{29}, R_{30}, and R_{31} and capacitor C_{10}, forms the preheating circuit. In addition to the 12V, 7-Ahr sealed, maintenance-free battery, the circuit uses a 10W, 12V single-crystalline-silicon solar-cell panel. The recorded backup time is approximately eight to 10 hours for a fully charged battery with a light output of 370 lumens using a 7W, four-pin CFL.□

TABLE 2–WINDING DETAILS FOR INDUCTOR L_2

Start pin	End pin	Wire gauge	Turns	Inductance
1	2	27	215	8.2 mH

Core: EE25/13/7

TABLE 3–WINDING DETAILS FOR INDUCTOR L_1

Wire gauge	Turns
26	100

Core: Ferrite rod, 5-mm diameter, 25 mm long.

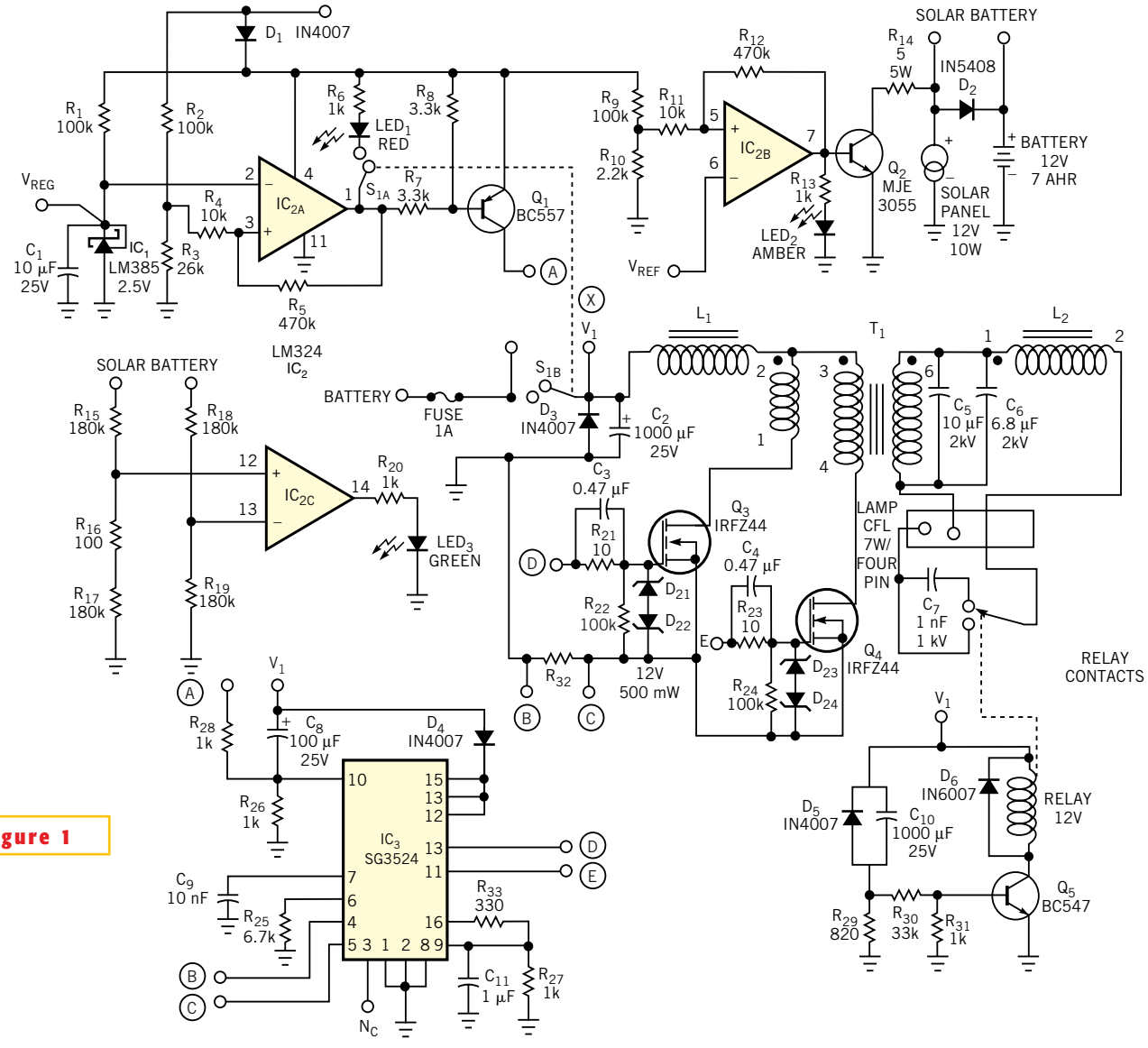


Figure 1

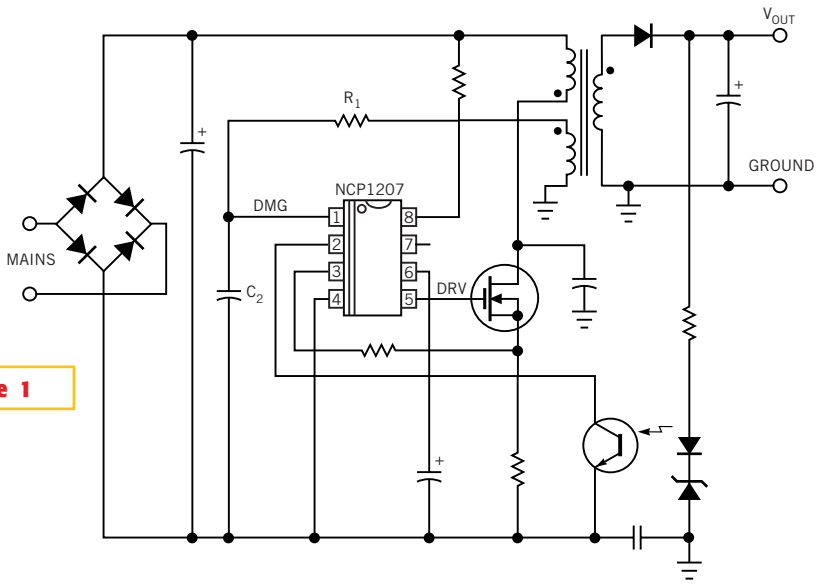
This solar-powered lantern driver can serve as an emergency lighting system.

RC network quashes auxiliary winding in quasiresonant converter

Nicolas Cyr, On Semiconductor, Toulouse, France

QUASI-SQUARE-WAVE-RESONANT converters, also known as QR (quasiresonant) converters, allow the design of flyback-type SMPSs (switch-mode power supplies) with a reduced EMI (electromagnetic-interference) signature and improved efficiency. You can achieve so-called QR operation by authorizing the turn-on of the switching MOSFET when the drain voltage reaches its minimum—hence, the name valley switching operation. The circuit usually externally detects the minimum drain voltage of an auxiliary winding, which delivers a voltage image of the core's internal flux activity. The circuit in **Figure 1** offers a solution that incorporates core-reset detection with the aid of an auxiliary winding. As you can see, the auxiliary winding solely performs the function of core-reset detection. To further simplify this schematic, you can remove the auxiliary winding and use the drain signal itself to generate the demagnetization signal that Pin 1 of the NCP1207 requires. **Figure 2** shows this arrangement. Thanks to its use of high-voltage technology, On Semiconductor's (www.onsemi.com) NCP1207 QR controller can derive its power directly from the rectified mains via its "dynamic-self-supply" feature.

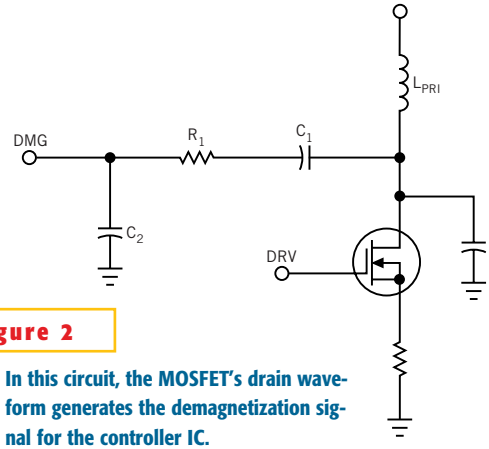
Figure 1



In this configuration, an auxiliary winding performs the function of core-reset detection.

Capacitor C_1 removes the dc component of the drain signal. R_1, together with the internal resistor on the NCP1207 demagnetization pin (Pin 1), creates a resistor divider. The divider safely limits the voltage you apply on the controller when the drain swings high. C_2 delays the signal to detect exactly the drain signal valley. Compared with **Figure 1,** where R_1 and C_2 were present, the only addition is C_1 (in replacement of the auxiliary winding. Because capacitor C_1 touches the MOSFET drain, it must sustain at least the same maximum voltage: A 220-pF, 1-kV or 1-nF, 1-kV ceramic capacitor perfectly fills the bill. The internal resistance of NCP1207's demagnetization pin is 28 kΩ. The value of R_1 ranges from 1 to 2 MΩ if you want to create a 5V signal with a maximum drain voltage of 600 and 900V. The value of capacitor C_2 depends on the frequency of the resonating network comprising the primary inductance, L_{PRI}, and the total capacitance of the drain node. You adjust the values of R_1 and C_2 directly on the board to reach the best valley detection possible. Because R_1 has a relatively high value, it is essential that the component resides close to the controller's Pin 1. The **Figure 3** waveforms show the final application results. The waveforms are captured on a single-output, 30W SMPS delivering 16V. In this application, C_1=220 pF/1 kV, R_1=1.5 MΩ, and C_2=100 pF. By properly adjusting the time constants, you can obtain perfect valley switching.□

Figure 2



In this circuit, the MOSFET's drain waveform generates the demagnetization signal for the controller IC.

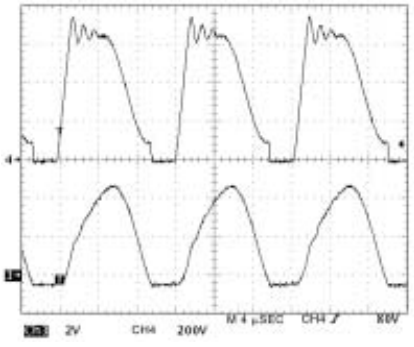


Figure 3

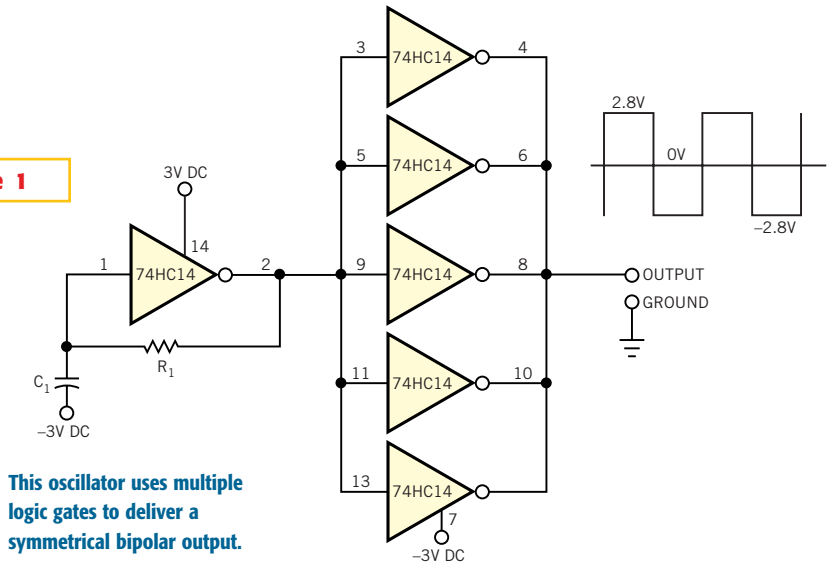
These waveforms illustrate the operation of Figure 1's circuit without the auxiliary winding.

Low-power CMOS oscillator has push-pull output

Shyam Sunder Tiwari, Sensors Technology Private Ltd, Gwalior, India

DIGITAL OSCILLATORS often generate TTL- or CMOS-level outputs, referred to ground. Generating a symmetric bipolar output with respect to ground presents a challenge. In this design, four 1.5V flashlight cells create ±3V voltage sources, and the midpoint of cells acts as the ground reference (**Figure 1**). The oscillator at the input, based on the R_1C_1 time constant, generates a ±2.8V bipolar output. The symmetrical output waveform requires no dc-blocking capability to drive a piezoelectric buzzer or loudspeaker. The circuit works well with ±1 to ±3V sources and delivers a symmetrical output over the full range of source voltages.□

Figure 1



This oscillator uses multiple logic gates to deliver a symmetrical bipolar output.

Edited by Bill Travis

Data-acquisition system uses fault protection

Catherine Redmond, Analog Devices, Limerick, Ireland

Sensitive systems, such as those in aircraft, must withstand fault conditions, thereby avoiding component and system damage, because a sensor failure could cause a catastrophic event to occur. A channel protector, comprising two n-channel MOSFETs connected in series with a p-channel MOSFET, can protect sensitive components from voltage transients in the signal path, whether or not the power supplies are present (**Figure 1**). The channel protector acts as series resistor during normal operation. If the input exceeds the power-supply voltages, one of the MOSFETs turns off, clamping the output within the supply rails, thus protecting the circuitry in the event of overvoltage or supply-loss conditions. Because channel protectors work regardless of the presence of the supplies, they are also ideal for applications in which correct power sequencing cannot be guaranteed and for hot-insertion rack systems. **Figure 2** shows an ADG465 channel protector with an input signal that exceeds the power-supply voltage. The protector clamps the output signal, protecting the sensitive components that follow the channel protector.

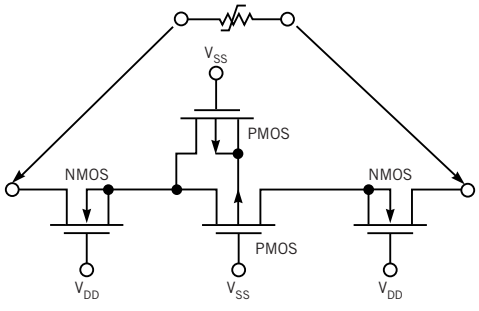
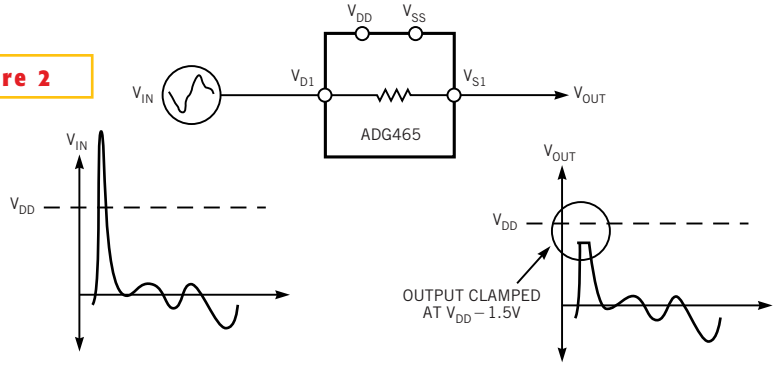


Figure 1 A channel protector can protect sensitive circuitry from voltage transients.

When a fault condition occurs, the voltage on the input of the channel protector exceeds a voltage set by the supply-rail voltage minus the MOSFET's threshold voltage. For a positive overvoltage, this voltage is $V_{DD}-V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistor (typically, 1.5V). In the case of a negative overvoltage, the voltage is $V_{SS}-V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (typically, −2V). When the input of the channel protector exceeds either of these voltages, the protector clamps the output within them. These devices offer bidirectional fault and overvoltage protection, so you can use the inputs or outputs interchangeably. **Figure 3** shows the voltages and MOSFET states for a positive-overvoltage event.

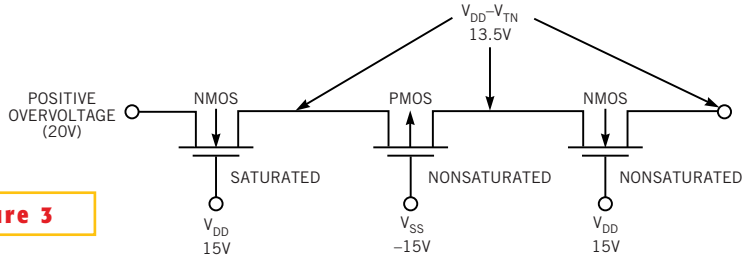
The output load limits the current during the fault condition to V_{CLAMP}/R_L (**Figure 4**). If the supplies are off, the protector limits the fault current to nanoamps. **Figure 5** shows how you can use the ADG466 channel protector to protect the sensitive inputs of an instrumentation amp from a sensor fault. In applications that require a multiplexer in

Figure 2



The channel protector clamps overvoltage transients to a safe level.

Figure 3



NOTE: V_{TN} = NMOS-THRESHOLD VOLTAGE (1.5V).

The voltages and MOSFET states appear like this during a positive-overvoltage event.

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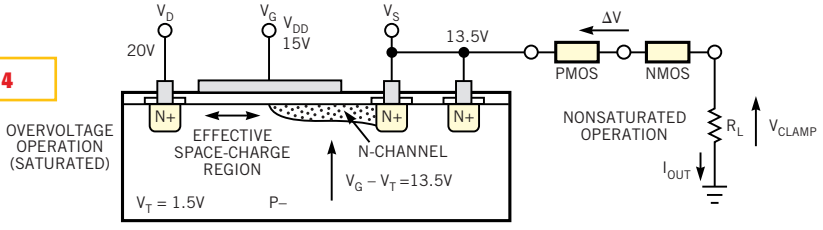
addition to channel protection, you can use the ADG439F fault-protected, four-channel analog multiplexer (**Figure 6**). These multiplexers use a series n-channel, p-channel, n-channel MOSFET connection. During fault conditions, the inputs or outputs appear as open circuits, protecting the sensor or signal source as well as the output circuitry.□

Figure 4



The output load limits the current to V_{CLAMP}/R_L during a fault condition.

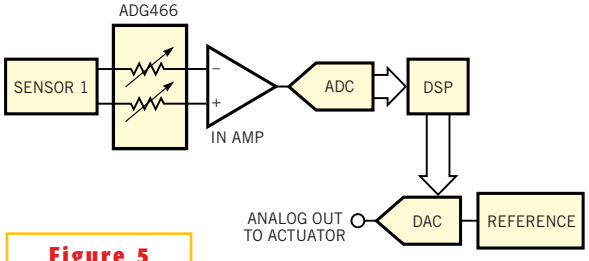


Figure 5

In this circuit, the ADG466 channel protector guards the sensitive inputs of an instrumentation amplifier from a sensor fault.

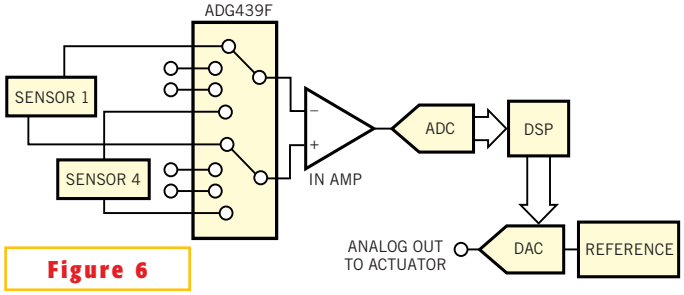


Figure 6

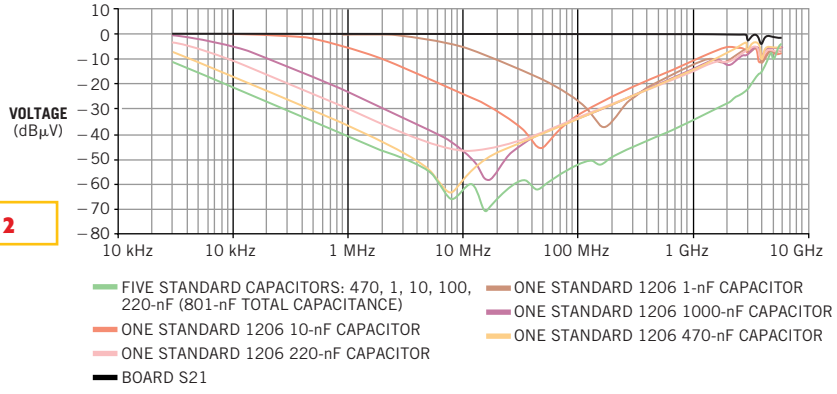
A multiplexer in a data-acquisition system protects the signal source as well as the output circuitry.

Take steps to reduce antiresonance in decoupling

Dale Sanders, X2Y Attenuators, LLC, Farmington Hills, MI

To maintain power integrity on pc boards, you need multiple capacitors to decouple the power-distribution system. A typical configuration might comprise five capacitors connected in parallel between the power and the ground traces or planes. To provide broadband decoupling performance, assume the individual values of the capacitors are 470, 1, 10, 100, and 220 nF (**Figure 1**). This parallel network provides 801-nF total capacitance to the power-distribution system. If you measure each capacitor with a vector-network analyzer, you can identify each capacitor's SRF (self-resonant frequency). **Figure 2** is a plot of each capacitor's SRF, as well as the SRF of the overall parallel connection. Each SRF can cause antiresonance in the parallel decoupling configuration. The antiresonance occurs when one capacitor is still capacitive, while another has become inductive.

Figure 2



Measurements with a vector-network analyzer reveal undesirable antiresonance effects.

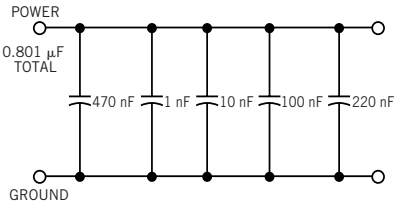


Figure 1

A typical decoupling configuration uses several multilayer-ceramic capacitors connected in parallel.

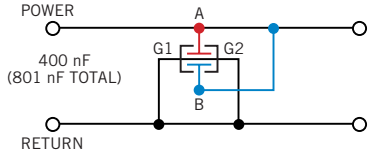
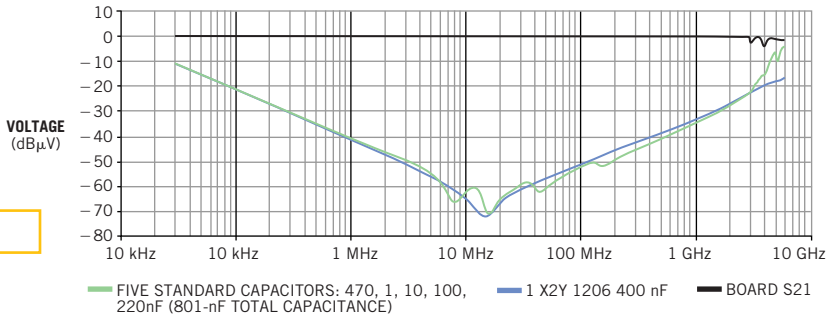


Figure 3

A 400-nF X2Y capacitor yields a total decoupling capacitance of 800 nF.

A way to considerably reduce the antiresonance effects is to use a single 400-nF X2Y capacitor for decoupling. (Capacitors using X2Y technology are available, for example, from Johanson Dielectrics (www.johansondielectrics.com). You measure the capacitance rating for an X2Y component from line to ground; in other words, from an A or a B terminal to either of the G1 or G2 terminals in **Figure 3**. So, the total capacitance a 400-nF X2Y component supplies, connected as in **Figure 3** would be double the capacitance rating, or 800 nF. **Figure 4** shows that a single X2Y capacitor with the same total capacitance as in **Figure 1** provides the same broadband decoupling as the standard decoupling configuration but without the antiresonance effects. In addition, because X2Y components come in the same package sizes as standard capacitors (1812, 1210, 1206, 0805, and 0603), the use of X2Y components saves pc-board space and reduces layout complexity.□

Figure 4



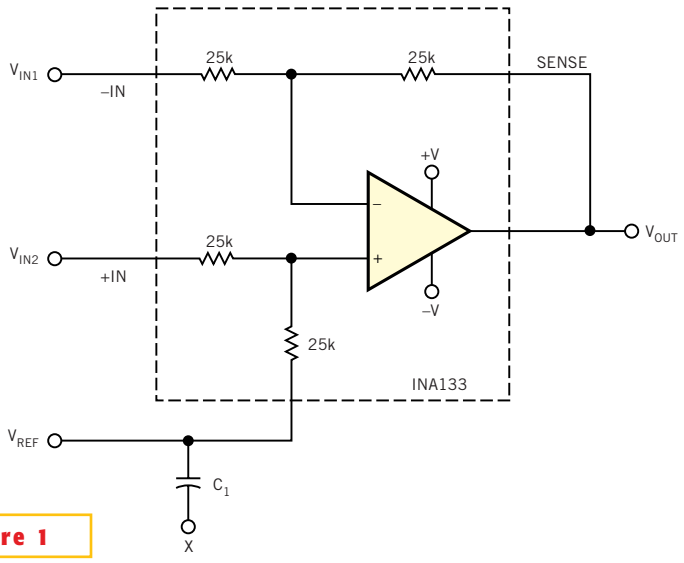
The single X2Y decoupling capacitor displays no antiresonance effects.

Precision level shifter has excellent CMRR

Ronald Mancini, Texas Instruments, Bushnell, FL

Most designers make level shifters with op amps and 1%-tolerance discrete resistors. Discrete-resistor mismatching limits the op amp's CMMR (common-mode rejection ratio) to 40 dB, so you cannot use op amps in circuits that require high CMRR. Differential amplifiers contain precision matched internal resistors, so ICs such as the INA133 can readily achieve CMRRs of approximately 90 dB. They can offer such high CMRR by trimming internal matched resistors. Assume that each input in the circuit of **Figure 1** has an associated noise voltage (V_{N1}, V_{N2}, and V_{NREF}). The transfer function of the amplifier circuit is $V_{OUT}=(V_{REF}+V_{NREF})+(V_{IN2}+V_{N2})-(V_{IN1}+V_{N1})$. Note that the reference voltage shifts the output signal, either single or differential. Once this level shifting occurs, you can turn your attention to the noise cancellation. Careful cabling and differentially coupling the signal into the differential amplifier's inputs force the noise on the signal inputs to be equal ($V_{N1}=V_{N2}$). The input noise is a common-mode signal, so the differential amplifier rejects it to the best of its ability (nominally, 90 dB). Now, $V_{OUT}=V_{IN2}-V_{IN1}+V_{REF}+V_{NREF}$.

Figure 1



C_1 allows the level shifter to act as a lowpass filter that rejects the reference noise.

Now, you need to eliminate the reference noise to obtain a clean level-shifted signal. You could connect the X end of C_1 to ground to shunt the reference noise to ground, but this solution may be ineffective because the source impedance of the reference is low. When, however, you connect the X end of C_1 to the V_{IN1} signal source, the differential amplifier acts as a lowpass filter and rejects the reference noise. This circuit keeps the input impedance of the differential amplifier low (approximately 25 kΩ for the INA133) to facilitate matching. Thus, you must keep the signal source impedance low to prevent gain errors. The source impedance should be less than 1/1000 the input impedance to minimize gain error. If this situation doesn't occur naturally, then it is best to buffer the inputs.□

Celsius-to-digital thermometer works with remote sensor

Elana Lian and Chau Tran, Analog Devices, Wilmington, MA

You can use a single-supply system to precisely measure the temperature at a remote location with less than 1°C error over a 0 to 100°C range (**Figure 1**). The circuit includes T_1, a low-cost AD590 temperature sensor; IC_1, an AD8541 rail-to-rail amplifier; four resistors; a trimming potentiometer; and an ADC. You can omit the ADC if you need an analog output. You could replace the trimming potentiometer with an AD8400 or AD5273 digital potentiometer for easier calibration. The feedback resistor, R_F, should be a precision resistor to minimize the scale-factor error, but the accuracy of the remaining resistors is not critical. You can choose the grade of the AD590 sensor to achieve the required accuracy.

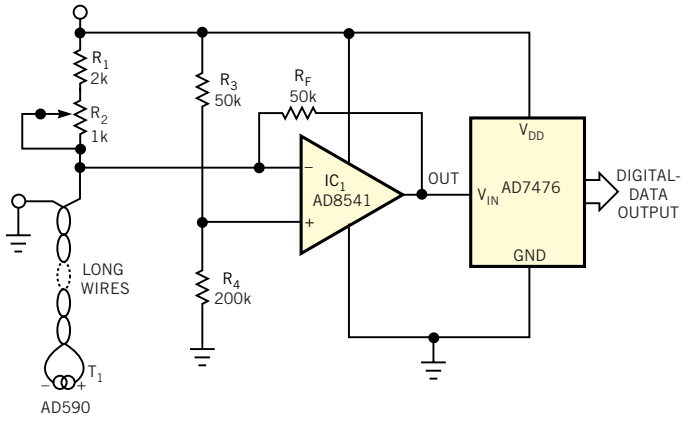


Figure 1 This system precisely measures temperature at a remote location, with less than 1°C error over a 0 to 100°C range.

The AD590 provides an output current proportional to absolute temperature (1 µA/K). In this application, the circuit offsets and scales the output to provide a full-scale range of 0 to 5V with a scale factor of 50 mV/°C over the chosen temperature range of 0°C—the freezing point of water—to 100°C, the boiling point of water. The AD8541 is a low-cost, low-power, rail-to-rail operational amplifier. It has a high common-mode voltage range and extremely low bias currents. You can calibrate out its 1-mV typical offset, the resistor, and AD590 errors. The output swing of the amplifier is 25 mV to 4.965V with a single 5V power supply, limiting the output by about 0.5°C on either end.

This circuit can derive its power from a single 5V power supply. The output of the AD590 varies from 273.15 to 373.15 µA as the temperature varies from 0 to 100°C. The positive input of the AD8541 has an offset of 4V to provide sufficient headroom for the AD590. The series combination of R_1 and R_2 develops a 1V drop, and you adjust R_2 to provide a nominal current of 353.15 µA. Thus, the current through the feedback resistor, R_F, varies from −80 to +20 µA as the temperature varies from 0 to 100°C. The voltage across this resistor varies from −4 to +1V. The 4V offset causes the output voltage of the amplifier to vary from 0 to 5V.

To guarantee the accuracy of 1°C throughout the range, you need to perform a calibration procedure. At a known temperature, such as 25°C, adjust trimming potentiometer R_2 to obtain the desired voltage at the output of the amplifier, 1.250V, or the desired code at the output of the ADC, 400H. Once you perform the calibration, you can calculate the temperature in Celsius at any measured point inside the range by multiplying the output voltage by 20. Because the sensor has a current output, it is immune to voltage-noise pickup and voltage drops in the signal leads; you can thus use it at a remote location. You should use a twisted-pair or shielded cable.□

Quasiresonant converter uses a simple CMOS IC

Francesc Casanellas, Aiguafreda, Spain

Figure 1 shows a flyback power supply that has low noise and uses a simple CMOS 4093 IC for its control. The electrical noise of a converter arises mainly when current switches on. Diode recovery and charging parasitic capacitances create high di/dt, which is the main cause of noise. The converter in **Figure 1** (pg 76) has a low noise level, because it slowly switches current on at nearly zero voltage. The converter works in the boundary between discontinuous and continuous mode and switches on when the drain voltage is at its lowest value. To avoid working with low gate voltages, which would cause excessive MOSFET losses, ZD_1 conducts and enables the input gate of the 4093 when the voltage is high enough. When the supply starts, the auxiliary nonisolated winding through D_3 keeps the gate input high. When the MOSFET is on, current increases linearly until the base of Q_5 starts to conduct, and this transistor turns the MOSFET off. The flyback operation then starts, and the primary energy charges the output capacitors. During this phase of operation, D_5 and R_6 keep Q_5 conducting and the MOSFET off. When the energy has discharged,

(continued on pg 78)

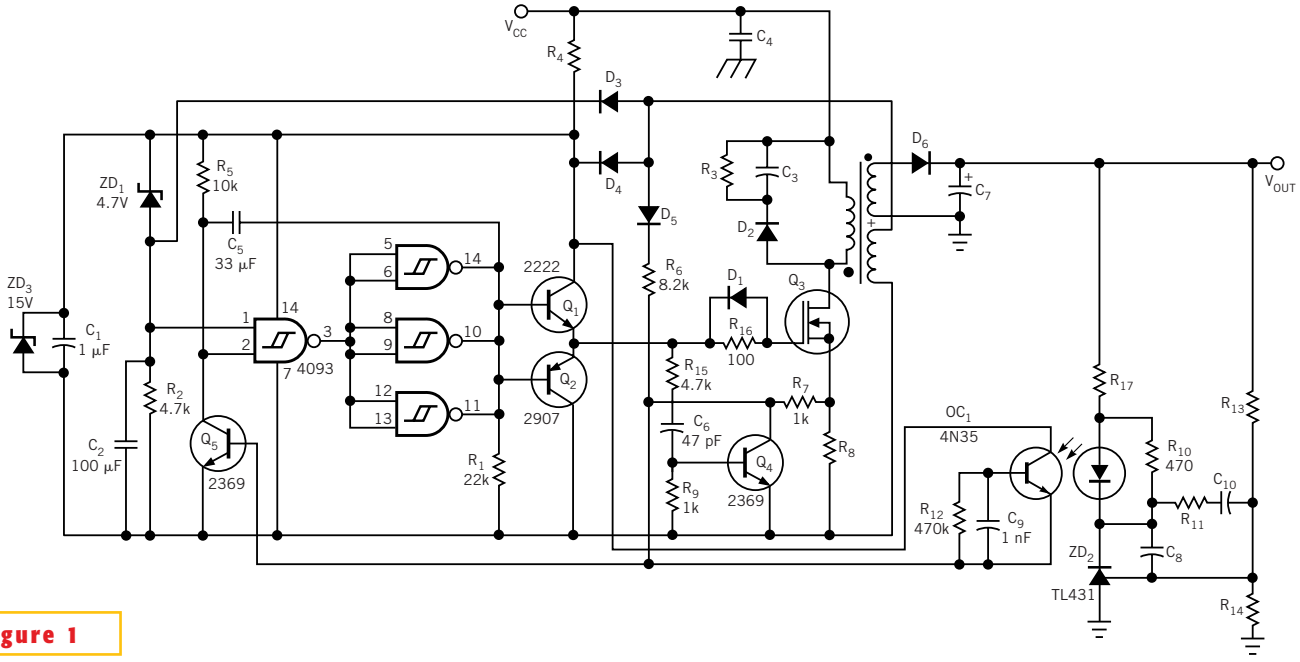


Figure 1

Using a simple CMOS IC, this flyback power-supply circuit exhibits extremely low noise.

(continued from pg 74)

D_5 stops conducting, as do the secondary diodes, so no recovery problems exist.

The time constant of R_5 and C_5 keeps the MOSFET off for a while. The output capacitance of the MOSFET plus the parasitic capacitance of the primary resonate with the primary inductance and the voltage decreases. R_5 and C_5 allow the MOSFET to turn on when the voltage has reached the minimum value. The values are valid only for this case. The circuit of **Figure 1** not only minimizes turn-on losses, but also reduces electrical noise. Voltage regulation uses traditional techniques, using a TL431. The optocoupler current adds to the shunt current. Because the MOSFET turns on when current is zero, the gate resistor may be high, so parasitic capacitances charge slowly, further reducing switching noise. The circuit around Q_4 is optional; you can use it in most power supplies. It kills the current glitch when Q_3 turns on. It is more effective than the usual RC circuit, and it allows a low duty cycle at low loads. Note that many of the component values in **Figure 1** are undesignated; you should determine these values to fit the application.□

Simple circuit serves as milliohmmeter

AM Hunt, Lancaster Hunt Systems Ltd, Shepperton, UK

When I was recently debugging a design, I discovered that a short circuit existed from a ground plane to a power plane. I did not have access to a milliohmmeter or an equivalent tester for locating this type of short circuit. So, I logged onto the Internet to find an easily constructible milliohmmeter. I found the answer in a manufacturer's data sheet, which outlined the basic four-wire method of making low-resistance measurements. The method uses a voltage-reference IC as the input stage for a controlled constant-current source. A quick dig in the old component bucket revealed a supply of LM317 variable-voltage regulators. These ICs provide 1.25V between their V_{OUT} and V_{ADJ} terminals, a constant voltage to attack the constant-current problem. The other problem to attack was the output-voltage range of the constant-current source. The circuit I was working on used a 3.3V supply, so I had to limit the voltage to 3.3V. An

LM317, configured as a constant-current source, delivers an output voltage equal to the input if the output resistance is too high. Because I wanted to use a bench supply or a 9V battery, the voltage would fry any 3.3V logic on the board. Ideally, I wanted voltage to be limited to 1.5V. So, I came up with the configuration in **Figure 1**.

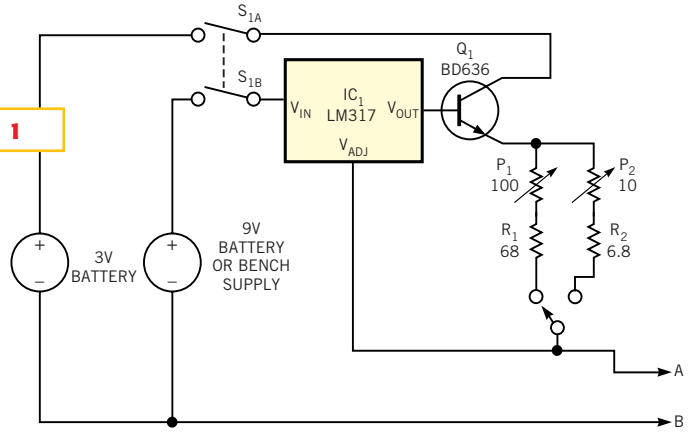


Figure 1

Make your own milliohmmeter, using a voltage-regulator IC and some resistors.

IC_1 controls the base of the npn Darlington transistor, Q_1. The IC regulates the voltage across the selected resistor to form the constant-current source. The current source delivers either 10 or 100 mA, depending on which emitter resistor is in the circuit. The purpose of S_1 is to give longer battery life. You can calibrate the current source by strapping a resistive load between test points A and B and measuring the voltage across the resistor using a DVM (digital voltmeter). I used 5 and 10Ω and set one S_2 position for 10 mA and the other for 100 mA. To measure a small resistance, you attach test points A and B across the resistance. You set the DVM on a millivolt range. The DVM reads a voltage that is proportional to the resistance under test. If you calibrate the circuit as suggested, then the reading is 10Ω/V on the 100-mA range and 100Ω/V on the 10-mA range.

To track down pc-board short circuits, attach the unit with test points A and B across the suspected shorted signals. Attach one DVM probe to test point A and use the other to probe the circuit. Constant voltage along a trace indicates that no current is flowing and that the trace is not the source of the short circuit. Look for high readings on the trace with the low reading and low readings on the trace with the high reading, to locate the source of the short circuit.□

Edited by Bill Travis

Transformerless dc/dc converter produces bipolar outputs

David Kim, Linear Technology Corp, Milpitas, CA

THE CONVENTIONAL WAY to produce dual (positive and negative) outputs from a single positive input is to use a transformer. Although such designs are relatively simple, the transformer inherently introduces the problem of size. It can be challenging to fit a transformer into an application in which it's important to minimize the circuit footprint and height. The circuit in **Figure 1** generates ±5V from a 3 to 10V input and fits into applications that lack the room to accommodate a transformer. The circuit uses a topology that allows the disconnection of both outputs when the dc/dc converter is in shutdown mode; thus, the quiescent current is low during shutdown (standby) mode. The circuit also produces a regulated positive and negative 5V, regardless of whether the input is higher or lower than 5V. Therefore, the circuit can operate from various input sources, such as a 3 to 4.2V lithium-ion battery or a 3.3 to 10V wall adapter. By slightly modifying the circuit, you can increase the input range to 2.5 to 16V and the output range to 3 to 12V.

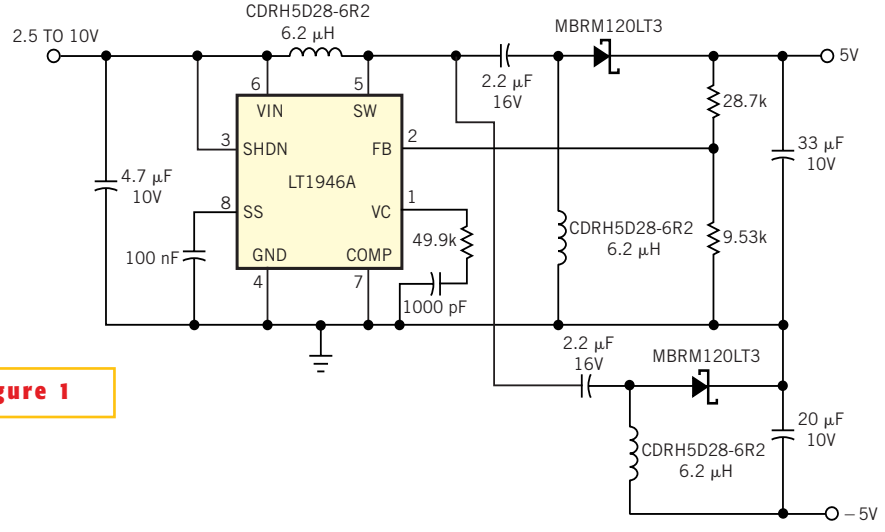


Figure 1

A simple circuit produces ±5V from a single positive input without the need for a transformer.

The 2.7-MHz switching frequency of the dc/dc converter allows the use of small, low-profile external components (input/output capacitors and inductors). Using three small inductors instead of one bulky transformer not only reduces the size and height of the converter, but also evenly distributes the power dissipation over the board, thus eliminating concentrated hot spots. The output-current capability of the circuit increases as the input voltage increases (higher input voltage, lower input current). **Figure 2** shows the maximum output current versus the input voltage. The "both" curve represents the maximum allowable output current of both ±5V outputs when you load them with the same current. The "single" curve represents the maximum allowable output current of each output when you load either output alone. When the current from one output decreases, the current capability of the other output increases, as long as you do not exceed the current rating of the dc/dc converter.

Cross-load regulation is another important design consideration in this type of circuit. Because the −5V output does not have control of the dc/dc converter's PWM feedback, the −5V output voltage

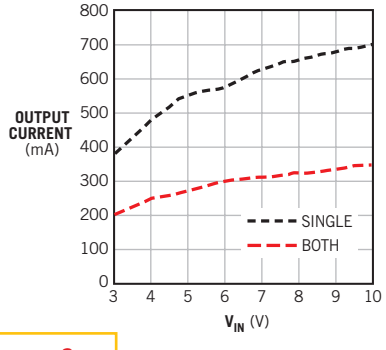


Figure 2

This graphic shows maximum output current versus input voltage for both outputs or a single output.

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changes with output current. You can greatly improve the cross-load regulation by adding a 10- to 20-mA preload at each output. The preload ensures that the dc/dc converter operates in continuous-conduction mode, in which the inductor current is stable enough to provide constant current. **Figure 3** shows the −5V output voltage regulation under different load conditions at the positive (**Figure 3a**) and negative (**Figure 3b**) outputs. In this case, to improve cross-load regulation, both the outputs connect to a 20-mA preload.□

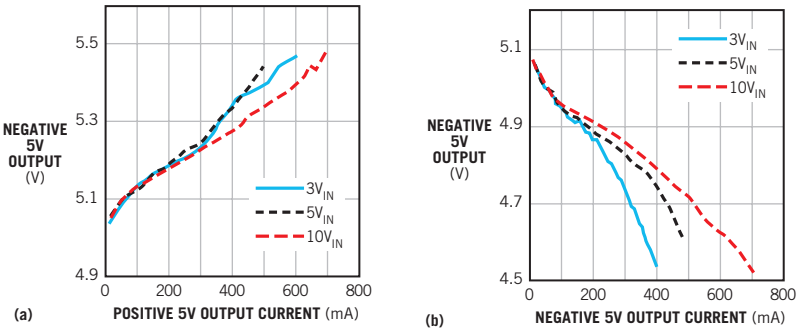


Figure 3

These curves show the regulation of the −5V supply as a function of the 5V output current (a), and the regulation of the same output as a function of the −5V output current (b).

Single processor pin controls on/off function

Michael Sirkis, Radio Systems, Logan Township, NJ

A recent Design Idea prompted me to offer the simpler solution that I used in a recent project (**Reference 1**). We needed a momentary power switch with processor supervision. This supervision would allow the processor to delay a power-down request from a press of the power switch until all routines exited properly. In addition, in periods of inactivity, the processor could shut down the product to conserve battery life. The project also required a boost converter to convert two or three AA batteries to 5V. The design uses IC_1, a Texas Instruments (www.ti.com) TPS61032 boost converter (**Figure 1**). It features an enable pin (Pin 9), which, when you pull it low, not only shuts down the converter, but also completely removes the load from the battery. The processor is a PIC16F874. A key element of the design is that you can first configure the processor-I/O pin as an output to keep the converter's enable pin high and then reconfigure it to test the logic level of the power switch.

When the circuit is not running, closing momentary power switch, S_1 (push-on) pulls IC_1's Pin 9 high, thereby turning on the converter and providing 5V to the processor. The processor boots up with its I/O pin configured as an output and pulled high. This action keeps IC_1's Pin 9 high and the converter running after the release of the power switch. Every few milliseconds, the processor's I/O pin reconfigures as an input, and the processor checks the switch for a high (pressed) or low (released) condition. The processor pin then returns to its previous output mode. Capacitor C_4 holds IC_1's Pin 9 (enable) high to keep the converter running while the switch undergoes testing. When you release the power switch from power-up and then press it again, the processor begins the push-off sequence. After performing whatever housekeeping it requires, the processor pin configures itself as an input and remains an input. Capacitor C_4 then completely discharges, bringing IC_1's Pin 9 (enable) low, thereby shutting down the converter and the rest of the circuitry. Diodes D_1 and D_2 allow the battery voltage to start the converter and the processor to test the power switch using the higher output voltage from the converter. The TPS61032 also features a low-battery comparator whose trip point is a function of R_1 and R_2. A different processor could read the comparator's output (IC_1, Pin 10) to perform a safe shutdown when the battery voltage gets too low.□

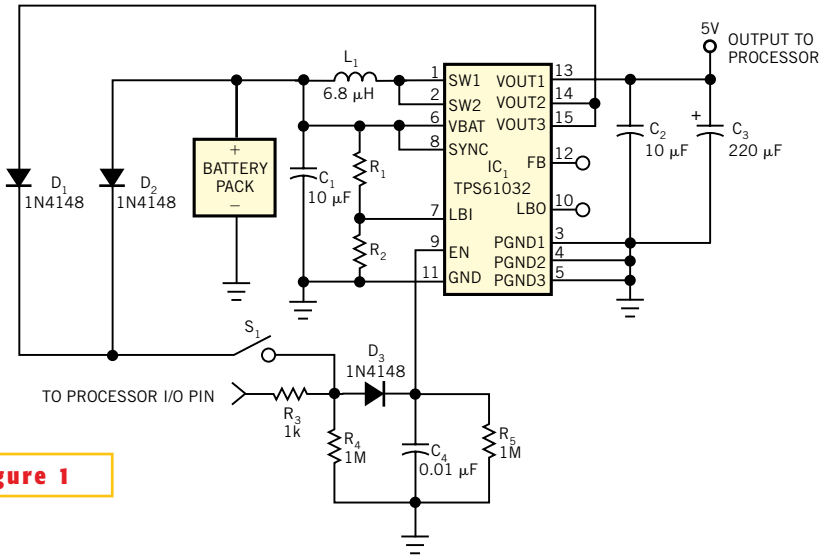


Figure 1

This circuit configuration provides a momentary power switch with processor supervision.

Reference

1. Gehrke, Dirk, "Microcontroller or DSP circuit controls on/off function," *EDN*, Nov 13, 2003, pg 104.

Isolated MOSFET driver has wide duty-cycle range

Jesus Doval-Gandoy and Moises Pereira Martinez, ETSI Industriales, Vigo, Spain

THE MAIN APPLICATION for the circuit in **Figure 1** is for driving power MOSFETs with signals ranging in frequency from 1 Hz to 300 kHz and with duty cycles from 0 to 100%. You achieve this goal by using a coreless pc-board transformer. The switching frequency in most power-electronics circuits ranges from a few hertz to a few hundred kilohertz. To design a coreless transformer-isolated gate drive that can switch in the range of frequencies lower than 300 kHz, you implement the modulation of a high-frequency carrier by a low-frequency control signal. The energy transfer from the primary side occurs through the use of a high-frequency carrier signal of 3 MHz. The control-gate signal couples to the secondary output by the modulation process. The binary counter, IC_3, divides the 24-MHz signal from clock-oscillator IC_2 by eight to obtain 3 MHz. The true/complementary buffer, IC_6, yields two complementary 3-MHz signals with low delay between them. The NAND gates, IC_5, implement the modulation process.

The design uses the value of C_3 to obtain maximum impedance at the working frequency. A voltage doubler (D_1, D_2, C_4) furnishes the gate-drive voltage. This design uses a 555, IC_7, as a Schmitt trigger because of its low power consumption. D_3 prevents the energy stored in C_6 from discharging into R_1. As you can see in **Figure 2**, when the control voltage is high, a 3-MHz ac signal appears across the transformer primary, thus charging capacitor C_5 and energy-storage capacitor C_6. The input to IC_7 goes high, thus turning on the MOSFET. When the control voltage goes low, the voltage across the transformer primary drops to zero, and the input to IC_7 goes low, thus turning off the MOSFET. **Figures 2** and **3** show the control voltage, the voltage across the transformer secondary, and the gate voltage of the MOSFET.

The dimensions of the transformer

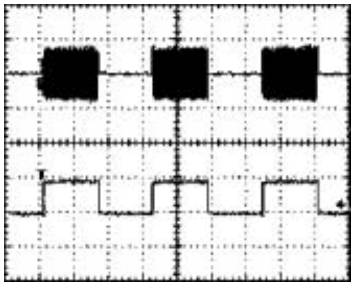


Figure 2 The top trace is the ac signal across the transformer secondary; the bottom trace is the low-frequency control voltage.

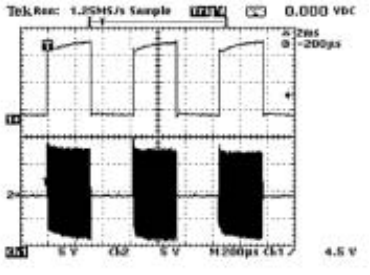


Figure 3 The top trace is the gate-drive voltage to the MOSFET; the bottom trace, the ac signal across the transformer secondary.

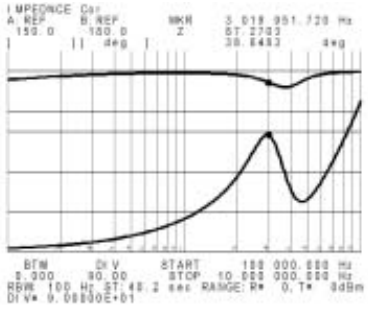


Figure 4 The input impedance of the transformer peaks at 3 MHz.

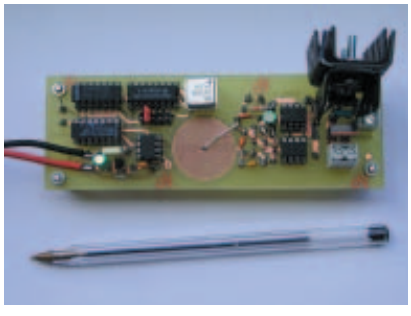
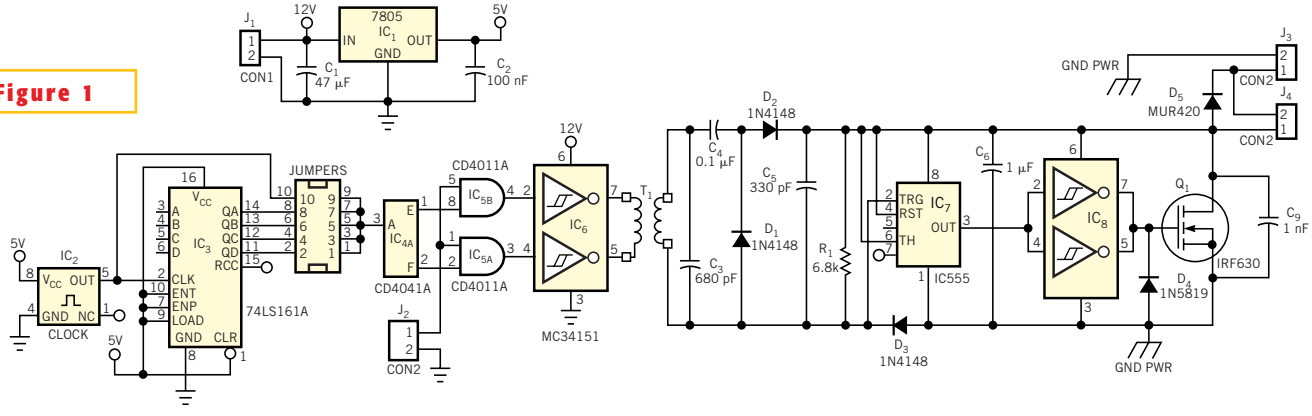


Figure 5 The prototype of the coreless transformer has a wide duty-cycle range.

Figure 1



A modulation scheme makes it possible to obtain isolated gate drive for a power MOSFET over a wide duty-cycle range.

and the carrier frequency yield a good relationship between the secondary and the primary voltages and minimize the input power of the gate drive. The transformer has a circular spiral primary winding on the bottom of the pc board. The primary winding has 20 turns of 0.3-mm-wide conductor. The circular spiral secondary winding is on top of the pc board. It has 15 turns and a 0.4-mm-wide conductor. For both windings, the conductor thickness is 35 microns, and the outermost radius is 25 mm. The pc board is 1.54 mm thick. **Figure 4** shows a frequency plot of the input impedance of the transformer with the secondary winding terminated by C_3. The network analyzer shows that the maximum impedance occurs at approximately 3 MHz. **Figure 5** is a photograph of a working prototype.□

Optoelectronic position control simplifies motor movements

Marie Rivera, Apex Microtechnology Corp, Tucson, AZ

The optoelectronic technique for achieving position control provides an inexpensive, easy- to-design method of achieving simple, repeatable movement using fixed index points with linear- or rotary-motion components. The simple, basic design in **Figure 1** for sequential position control exploits the quick response time of a power op amp, working in tandem with a pair of photodiodes. The result is a low-component-count system that provides high reliability, accuracy, and repeatability when you use it in well-defined operating conditions. The circuit in **Figure 1** achieves sequential position control by using a power op amp to integrate the differential output of a pair of photodiodes to drive the motor in the proper direction until the photodiode currents are equal. Movement between index points occurs when you momentarily switch a fixed input current to the amplifier's input, causing the amplifier to drive the motor in the desired direction. The charge on C_F maintains motor drive as the input current switches off before reaching the index point.

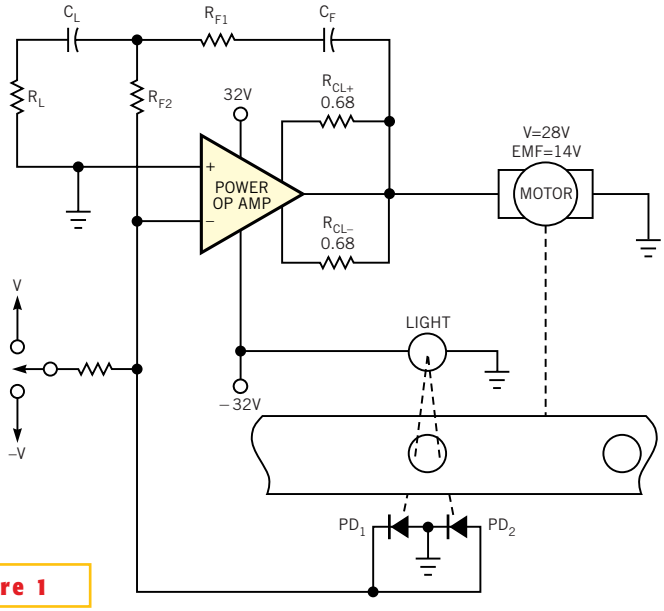


Figure 1

An optoelectronic circuit uses a power op amp to achieve sequential position control.

To ensure continued motion in the desired direction, the motor drive receives reinforcement by the output from the first photodiode as it illuminates. As the second photodiode illuminates, its current reverses the motor drive, causing the system to lock to the index point. The use of a differential configuration eliminates errors from temperature and time instability in the optoelectronic devices. The entire system uses a simple switch, as **Figure 1** illustrates, to generate both forward and backward motion. Because motor response time and system inertia vary greatly in different applications, you achieve proper damping by selecting C_F and R_F based on the application. C_F needs to be small enough to allow drive reversal before the index point passes the second photodiode; otherwise, the system continues on to the next index. If the value of C_F is too small, severe overshoot or oscillation can occur, resulting in drive-train failure or motor burnout.

To help minimize overshoot, R_{F1} and R_{F2} in **Figure 1** stabilize the control loop at the unity-gain point. You can also improve response time by applying a braking force, which you create by using R_L and C_L to form a lead network, which enables the amplifier to modify the motor drive based on a change in the sensor output. The motor in **Figure 1** has EMF (electromotive force) of 14V and can apply a 46V stress across the conducting output transistor when you reverse it. This power dissipation is a worst-case scenario; you need to check it against the SOA (safe operating area) of the amplifier. **Figure 2** shows optimum

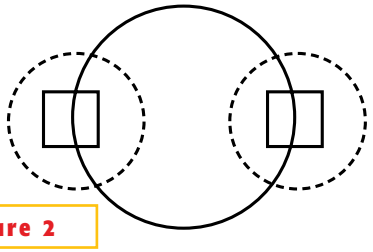


Figure 2

With optimum beam-sensor alignment, the light beam illuminates half the photosensitive area of each diode.

alignment for the beam sensor. You achieve optimum alignment by centering the light beam in relationship to the active areas of each photodetector. The light beam needs to illuminate half the photosensitive area of each diode. When sizing the "hole," consider the distance between the location of the light beam and the photodiodes. If the beam is too large, the sensors do not produce any change for a range of positions. Too small a beam produces a nonlinear transfer function along the center line between the photosensitive areas. This nonlinearity can create difficulty in selecting the value of C_F for dampening the circuit and requires a light source with higher intensity.

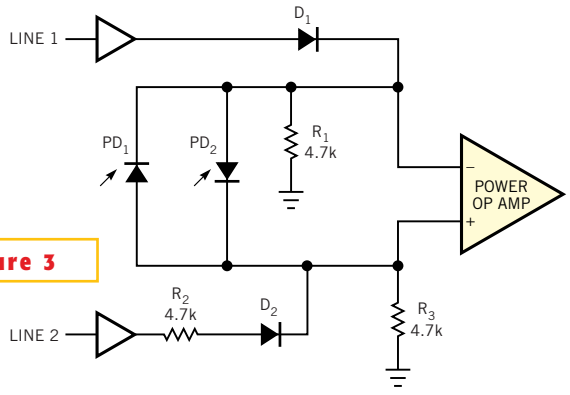


Figure 3

This circuit imparts digital-interface control to the circuit in Figure 1.

Figure 3 illustrates how you can use a nonbipolar signal without digital-to-analog conversion for systems that integrate digital control. When logic lines are low, the signal diodes do not conduct. This condition allows the photodiodes to control the circuit. A high level on Line 2 causes current to flow to the summing junction and swing the amplifier negative. A high level on Line 1 raises the summing junction voltage above ground and swings the amplifier positive. By selecting a resistance value that allows a logic-level supply high enough to provide at least twice the maximum current from each photodiode, the circuit maintains system control regardless of the photodiode signals.□

Dual-polarity supply provides ±12V from one IC

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Well-regulated, dual-polarity power supplies find wide use in disk-drive, handheld-device, automotive, and notebook-computer applications. In these applications, board space and allowable component heights are continually shrinking. So, power-supply designers face the challenge of providing split rails with as few parts as possible, thus saving board space and cost. Some dual-polarity dc/dc-converter topologies—for example, overwindings and flyback converters with multiple-winding transformers—require excessive board space, component height, or both; offer poor load regulation; or provide limited load current. **Figure 1** shows an alternative approach that uses a single boost regulator using a dual-polarity SEPIC (single-ended, primary-inductance-converter) architecture. The circuit saves space and offers good regulation and current-handling capability. The boost regulator, IC_1, usually figures in step-up-converter configurations, but the low-side power switch in IC_1 allows the use of the IC in both SEPIC and negative-SEPIC circuits.

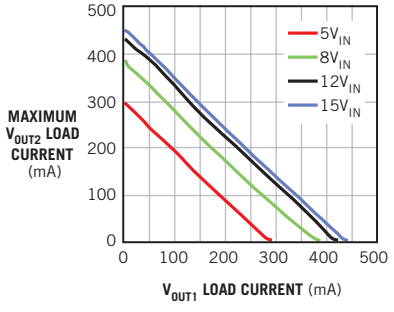


Figure 2

This graph shows the maximum load current at the V_{OUT2} terminal versus the V_{OUT1} load current.

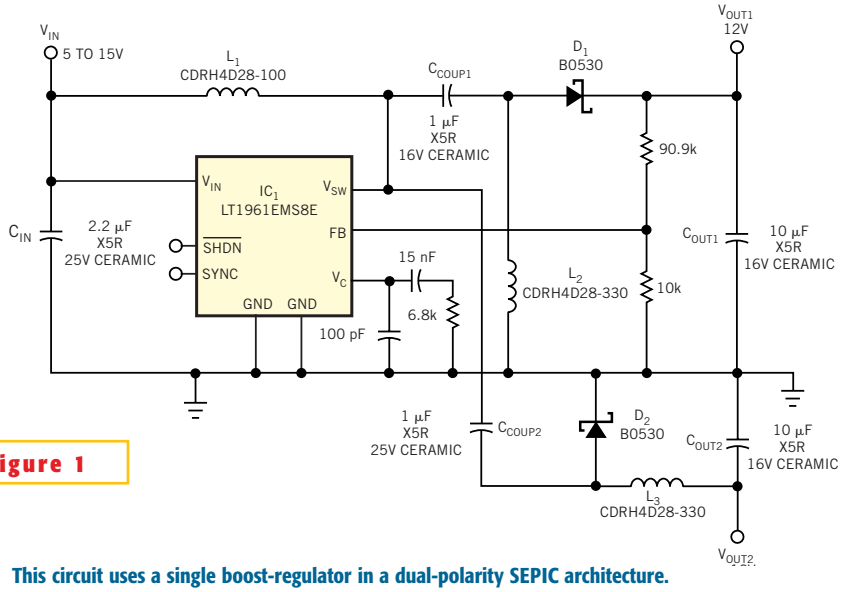


Figure 1

This circuit uses a single boost-regulator in a dual-polarity SEPIC architecture.

The combination of the two topologies creates a dual-polarity SEPIC, an excellent source for multiple-rail bias power. The circuit provides well-regulated

±12V outputs at varying load currents (5W power with 12V input and 3.6W with 5V input). **Figure 2** shows the maximum available current at V_{OUT2} as a function of the load current at V_{OUT1}. **Figure 3** shows the efficiency of the converter as a function of the load current at V_{OUT1}. Although the positive feedback comes from V_{OUT1}, V_{OUT2} maintains excellent regulation (**figures 4** and **5**). The circuit maintains the regulation as long as each load draws a minimum of 5-mA current. The SEPIC topology accommodates input voltages both above and below the output voltage. The use of three small power inductors as opposed to a transformer keeps the component height below 3 mm, reduces board space, and allows layout flexibility. The high-frequency, current-mode boost-regulator IC uses all ceramic capacitors, thus minimizing ripple and overall cost.□

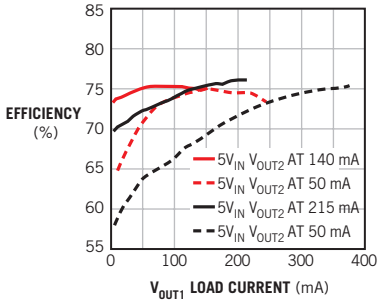


Figure 3

Efficiency of the circuit in Figure 1 is more than 70% for most of the range of load-current values.

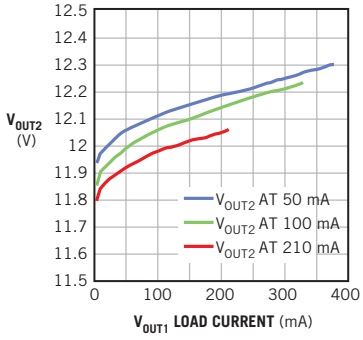


Figure 4

Regulation of the V_{OUT2} voltage as a function of V_{OUT1} load current is reasonably tight.

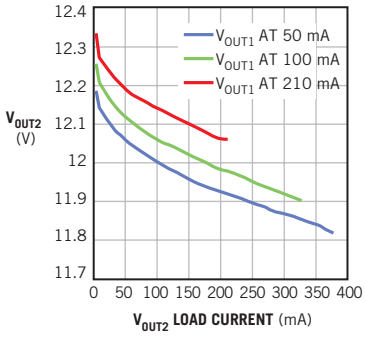


Figure 5

Regulation of the V_{OUT2} voltage is within ±200 mV over almost all of the range of V_{OUT2} load currents.

Edited by Bill Travis

Circuit forms simple, low-cost, 1-kV driver

Tai-Shan Liao and Prasit Champa, National Science Council, Hsinchu, Taiwan

HIGH-VOLTAGE DRIVERS have recently received much attention, because they play an important role in driving piezoelectric and electro-optical components, for example. **Figure 1** shows a simple, low-cost, 1-kV driver. The circuit uses offline, current-mode-control techniques and a flyback switching-power-supply design. IC_1, a UC3844, is the major control component, using a switching frequency of 100 kHz. The IC provides frequency modulation to reduce the switching frequency under light- and no-load conditions. The feedback voltage, which you derive from the output of the error amplifier, serves as the indicator for load conditions. Once the feedback voltage becomes lower than the green-mode threshold voltage, the switching frequency starts to decrease.

All the power losses are in direct proportion to switching frequency. These losses include the switching losses of the transistor, core losses in the transformer and inductors, and the power loss of the snubber. The frequency modulation in the PWM-controller IC reduces the power consumption in the supply under

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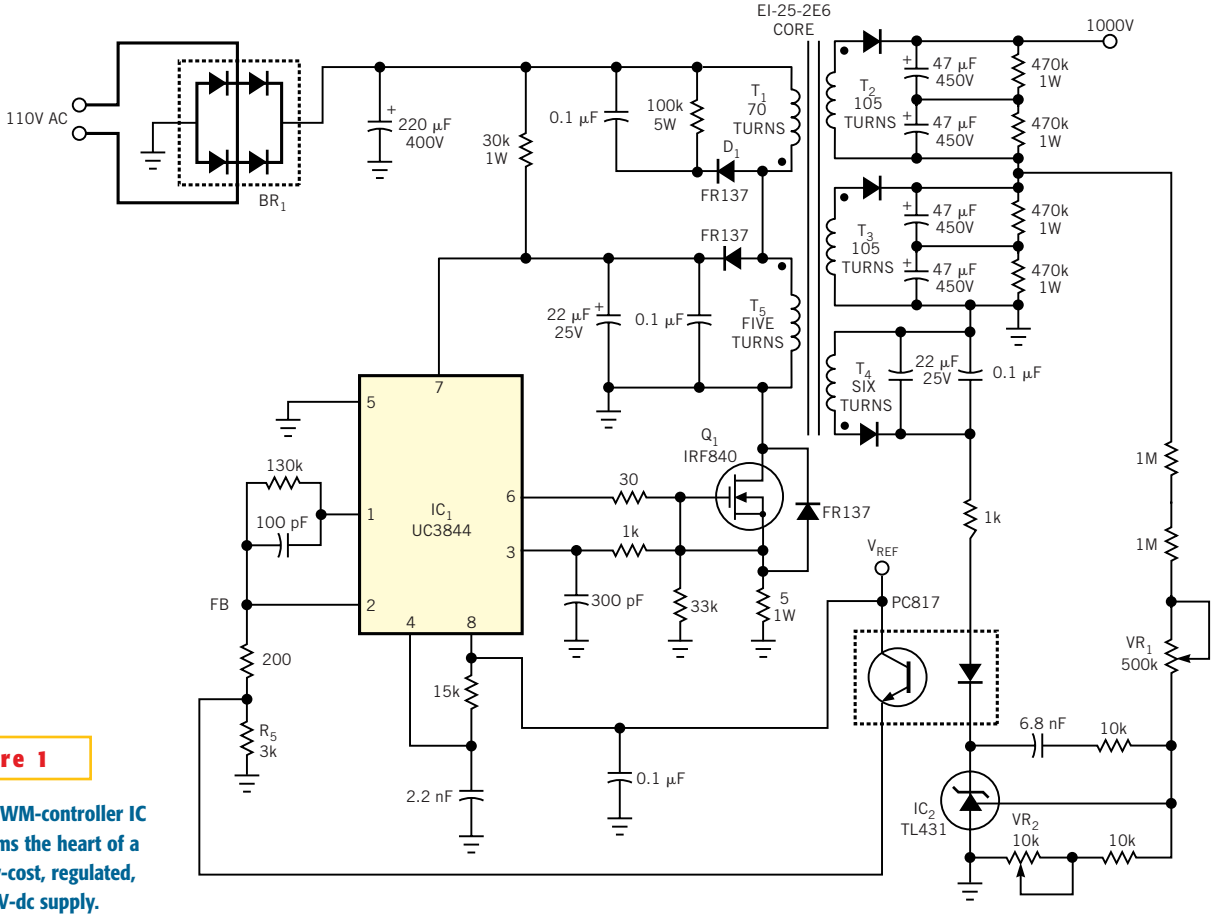

Figure 1

A PWM-controller IC forms the heart of a low-cost, regulated, 1-kV-dc supply.

light- and no-load conditions. But the frequency modulation has no effect on the PWM operation under normal- and high-load conditions.

Pin 2 (the feedback pin) of the UC3844 sums the current-sense signal, the output-voltage feedback signal, and any added slope compensation. The feedback-control circuit uses a TL431 adjustable shunt regulator to detect the output signal. A PC817 passes the signal to the feedback pin of the UC3844. The TL431 acts as an open-loop error amplifier with a 2.5V temperature-compensated reference. When the output voltage is lower than the desired level, the feedback to the UC3844 automatically compensates the pulse-width modulation of the output triggering signal. Ceramic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground provide low-impedance paths for high-frequency transients. This design uses a Tomita (www.tomita-electric.com) EI25-2E6 core set to fabricate the transformer. To prevent core saturation, the gap is approximately 1 mm. The primary winding has 70 turns of 28-gauge wire. Both the secondary windings have 105 turns of 34-gauge wire. The primary and secondary auxiliary windings have five and six turns, respectively, of 34-gauge wire. The dc output voltage of the circuit in **Figure 1** is 1 kV (fixed). You can adjust the output voltage in a 50V range by adjusting VR_1. Both load and line regulation are less than 1%, and power efficiency is 80% at full load.□

Make a printer-port EEPROM programmer and dongle

GY Xu, XuMicro, Houston, TX

You can easily use a PC's printer port for serial-EEPROM programming. You can use a device-programmer circuit used to program the MicroWire serial EEPROM 93CXX (**Figure 1**). The circuit is so simple that any further simplification seems impossible. This programmer circuit contains no microcontroller, as most device programmers do. It needs neither a separate power supply, or "wall-wart," nor a cable. When in use, it directly plugs into the PC's printer port. However, you still can use a cable if convenient—for PC printer ports behind the PC, for example. The circuit also requires neither a resistor nor a decoupling capacitor.

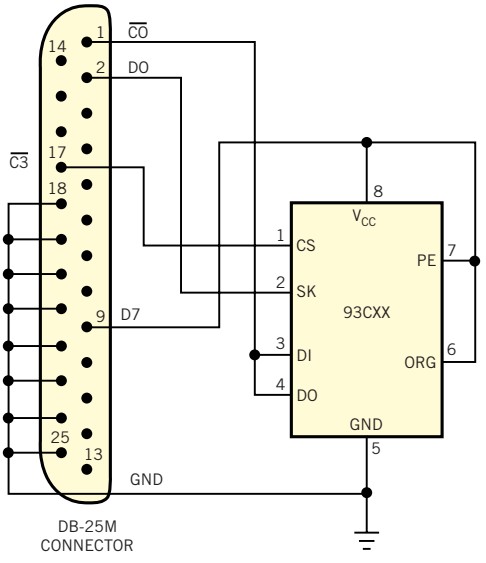

Figure 1 This printer-port serial EEPROM programmer can also act as a dongle once you program the device.

These advantages come from the PC's printer-port resources and the architectural simplicity of the MicroWire serial EEPROM. The printer port comprises the 8-bit data, status, and control registers. Each register has its unique address. On the classic IBM PC, the data port serves solely for output, but the control port can serve as either input or output. The eight-pin, tiny, serial EEPROM consumes less than 1-mA current in the active state, and the printer port's data pin can supply a few milliamps, so this design uses D7 (Pin 9) as a power-supply pin. No decoupling capacitor is necessary in practice.

The MicroWire chip uses the CS (chip-select), SK (clock-signal), DI (data-input), and DO (data-output) pins to control its read/write operations. This design uses the chip-select signal from the reverse level of the control bit $\overline{C3}$ (Pin 17). It also ties together pins DI and DO and connects them to the Control bit $\overline{C0}$ (Pin 1), which can serve as input or output, thereby saving one pin. These selections caused no problems in practice. Because control Pin 1's logic is the reverse of the logic level on bit C0, the software must take care of the inversion. The MicroWire interface normally requires a pullup resistor on the DO pin, but such a resistor is already inside the PC, so it's unnecessary.

Once you settle on the hardware design, the main task is to write software. This task is not difficult. For many embedded-system-software engineers, it's routine and interesting. A freeware executable program, Pseep2.exe, is available for this purpose. A sample demo program, secret.bin, allows you to practice the programming. You can download the software from the Web version of this Design Idea at www.edn.com. It handles only one MicroWire device—the popular 93C46's read/write operation as an example. Another important feature of this circuit is that, once you program the 93CXX device, the system becomes a primitive dongle. You can then use it as a hardware-protection device for your valuable software. Only you know whatever was programmed in the device.

When the protected software runs, it first checks whether the device is present at the printer port and whether the code matches what you programmed. If a match doesn't exist, the software refuses to continue and exits. The dongle is primitive, but it does illustrate the basic principle of dongle-protection technology. You can build the circuit using wire-wrapping or point-to-point soldering techniques on a solderless breadboard, in which case you'll need a cable, or with your own pc board. It's a one-evening project.□

Circuit controls ratiometric or simultaneous power-up of multiple rails

Dirk Gehrke, Texas Instruments, Freising, Germany

Many applications use FPGAs, ASICs, or DSP chips, which usually require multiple voltage rails, typically two: the core voltage and the I/O voltage. The core voltage is usually lower than the I/O voltage. Guidelines for determining how to power up two or more voltage rails depend on the part and the manufacturer you use. The first implementation in **Figure 1** shows how to realize ratiometric sequencing, which means that both power-supply output rails simultaneously start and simultaneously reach their final regulated output voltage. This implementation uses resistor R_{15} connected to ground; the path and components in red are deleted. You can achieve the ratiometric function by stacking together multiple converters that share one soft-start capacitor. This connection ensures that both controllers ramp up their output voltage at the same time during power-up. Both the IC_1 and IC_2 controllers share a soft-start capacitor, C_{14}. This example uses two buck converters with integrated synchronous-rectification FETs. From a 5V input-voltage rail, IC_1 generates the 3.3V I/O voltage. Buck converter IC_2 generates the 1.5V output voltage.

The soft-start pin, available on both controller ICs, serves two purposes. You can use it to enable the controller circuitry if required—an implementation you could realize by tying an open-collector or open-drain gate to the SS Pin. If the transistor or FET is active, it ties the SS Pin to ground potential, forcing both controllers to stay off. Once you release the SS Pin, both ICs start to charge C_{14} with their internal 5-µA current sources. In total, 10-µA current flows into C_{14}. Once C_{14} reaches the threshold voltage of 1.2V, both controllers start to operate. You can easily calculate the delay versus the capacitor's value: Delay time=C_{14}(1.2V/10 µA). As the output activates, a brief ramp-up at the internal soft-start ramp may occur before the external soft-start rate takes control. The output then rises at a rate proportional

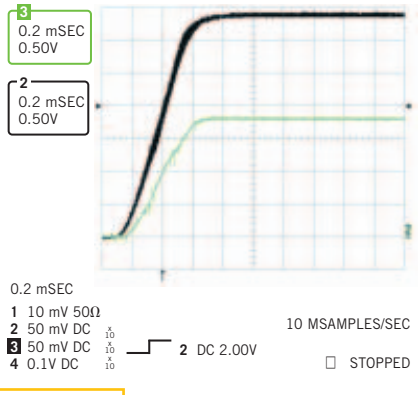

Figure 2

This graphic shows measurement results for the ratiometric implementation.

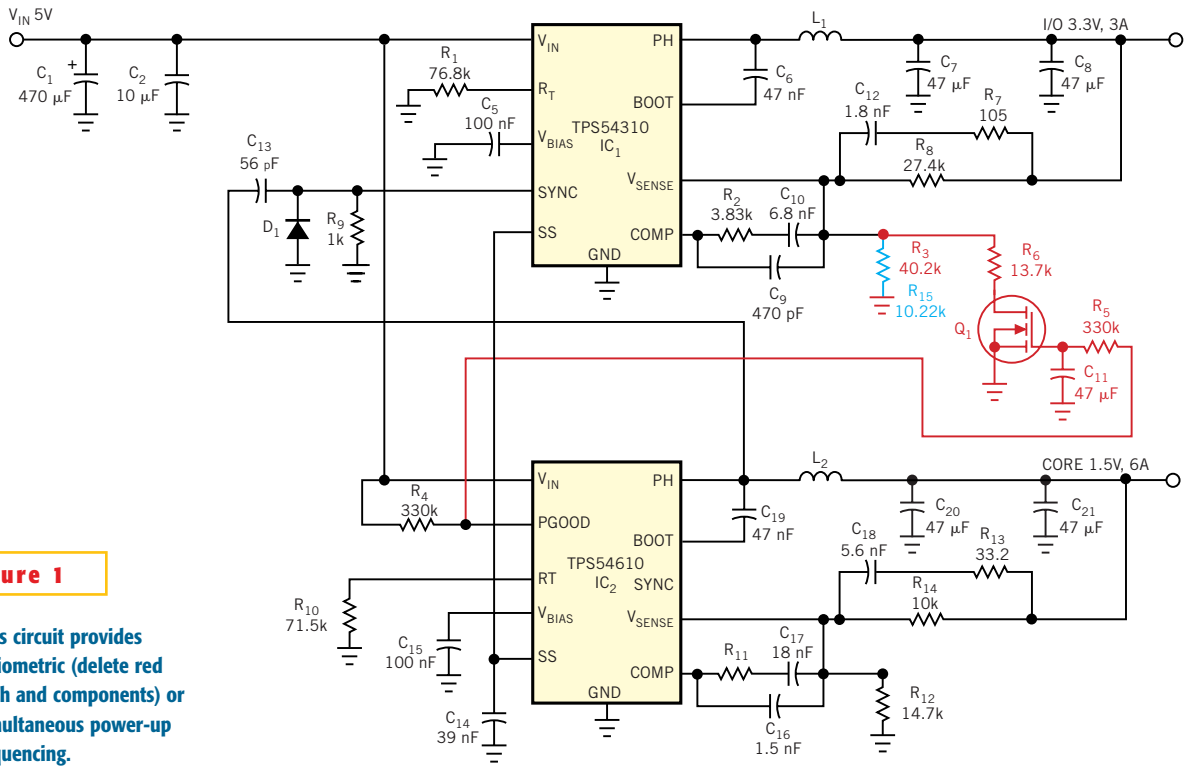

Figure 1

This circuit provides ratiometric (delete red path and components) or simultaneous power-up sequencing.

to the soft-start capacitor. You can program the soft-start time via C_{14}. The next equation represents the soft-start time calculation. The actual soft-start time is likely to be less than the calculated approximation because of the brief ramp-up at the internal rate. Soft-start time=C_{14}(0.7V/10 µA). If you set IC_1 for

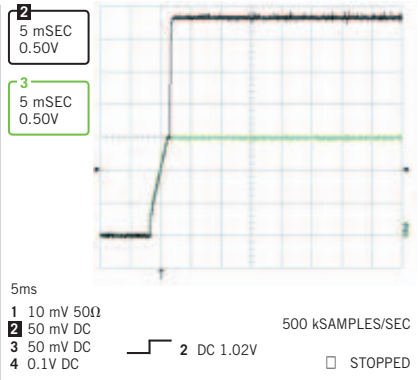

Figure 3

These curves, distinctly different from those in Figure 2, show simultaneous-sequencing results.

3.3V and IC_2 for 1.5V, they both reach their final voltage level at the same time. **Figure 2** shows measured results of the ratiometric sequencing.

In the simultaneous-sequencing scenario, IC_2 acts as the master controller. You program its output voltage via R_{14} and R_{12} to a value of 1.5V. R_8 and R_3 program the slave controller IC_1's output voltage to a value of 1.5V. As the ratiometric scenario describes, both voltages start at the same time with the same ramp, reaching their final value at the same time. Once both rails reach 1.5V, you must increase IC_1's output voltage to 3.3V, its final value. To make that increase happen, Q_1 places R_6 in parallel with R_3. You can calculate the value of R_6 using the next three equations. The given parameters are: $V_{OUTCORE}$=1.5V; R_8=27.4 kΩ; V_{REF}=0.891V, the internal bandgap-reference voltage of IC_1; and R_3=40.2 kΩ. You can program $V_{OUTI/O}$ via R_8 and R_X. R_X represents the value of R_3 and R_6 in a parallel connection.

$$R_3 = \frac{V_{REF}}{\left[\frac{V_{OUTCORE}-V_{REF}}{R_8}\right]}.$$

$$R_X = \frac{V_{REF} \times R_8}{(V_{OUT\ I/O}-V_{REF})}.$$

R_X must have a value of 10.22 kΩ to produce $V_{OUTI/O}$=3.3V.

$$\frac{1}{R_X} = \frac{1}{R_3} + \frac{1}{R_6} \Rightarrow R_6 = \frac{1}{\frac{1}{R_X} - \frac{1}{R_3}}.$$

In this example, R_6 needs a value of 13.7 kΩ. Applying 5V to the input-voltage rail activates both controllers at once, allowing them to start at the same time. Once the master controller, IC_2, reaches an output voltage level equal to or greater than 90% of the initial value, the IC releases the power-good open-drain-comparator output pin. This action forces the pin to rise immediately to the output-voltage level because of resistor R_4's pullup action. A lowpass filter consisting of R_5 and C_{11} forms a delay circuit, driving MOSFET transistor Q_1's gate. This delay circuitry determines when Q_1 becomes active. Q_1 has a threshold voltage, V_{GSTH}, of 1.6V. Once the gate voltage reaches or exceeds the threshold voltage, V_{GSTH}, Q_1 starts to conduct, putting R_6 in parallel with R_3. Because of the resistor-ratio change, IC_1's output voltage ramps up to its final I/O-voltage value of 3.3V. The MOSFET this design uses has an on-resistance of roughly 10Ω. This figure might sound high, but, because of the high-ohmic-resistive divider, this value does not affect performance. **Figure 3** shows the results of the described implementation during power-up.

Significantly, in this implementation both converters run at the same switching frequency. IC_2 is the master controller, programmed to a 700-kHz switching frequency. IC_1 starts at a lower initial switching frequency of roughly 630 kHz, 10% below the switching frequency of IC_2. Once IC_2 begins to operate, it synchronizes IC_1 via the Sync Pin. Diode D_1 limits negative voltage spikes at the Sync input. Placing a well-chosen Schottky diode between both output voltage rails can ensure that, even during power-down, both rails have a voltage difference of 400 to 600 mV for safety reasons. The cathode connects to the I/O-voltage rail, and the anode connects to the core rail.□

Scheme provides automatic power-off for batteries

Miguel Gimenez, Altair-Equipos Europeos Electronicos, Madrid, Spain

The circuit in **Figure 1** provides a simple and inexpensive way to protect one of the most valuable components in portable applications: the battery. Applications include all portable equipment that requires a limited time of operation, such as test instruments, guitar tuners, and electronic toys. Pressing the on/off momentary switch starts the cycle, and the circuit provides power to the application circuit. If you again press the switch at any instant, the circuit switches off and "sleeps" until the next cycle. In case you forget to switch off the circuit, the circuit incorporates an auto-power-off function with a time period that is a function of preprogrammed time constants.

IC_1 and related parts provide a bistable toggle function and also ensure protection against switch-contact bounce. IC_{1C} buffers the toggled signal and isolates the R_1-C_1 charging current. This signal feeds the IC_2 timer, configured as a monostable multivibrator that remains activated until it times out, according to the expression $t=1.1\times R_T C_T$. This figure is the auto-power-off time. In the example, this interval is approximately six minutes. The timer's output feeds the Q_1 inverter that activates medium-power, pass-through Q_2 transistor. This circuit is configured as a pnp block to ensure low losses to the load. The loss comes only from $V_{CE(SAT)}$—approximately 0.2V at 100 mA, or 20 mW. For applications demanding more current, you can choose a more suitable transistor. A MOSFET can be an efficient approach when you need either lower standby losses or a lower voltage drop between the battery and the application circuit.

Standby losses in the switched-off state

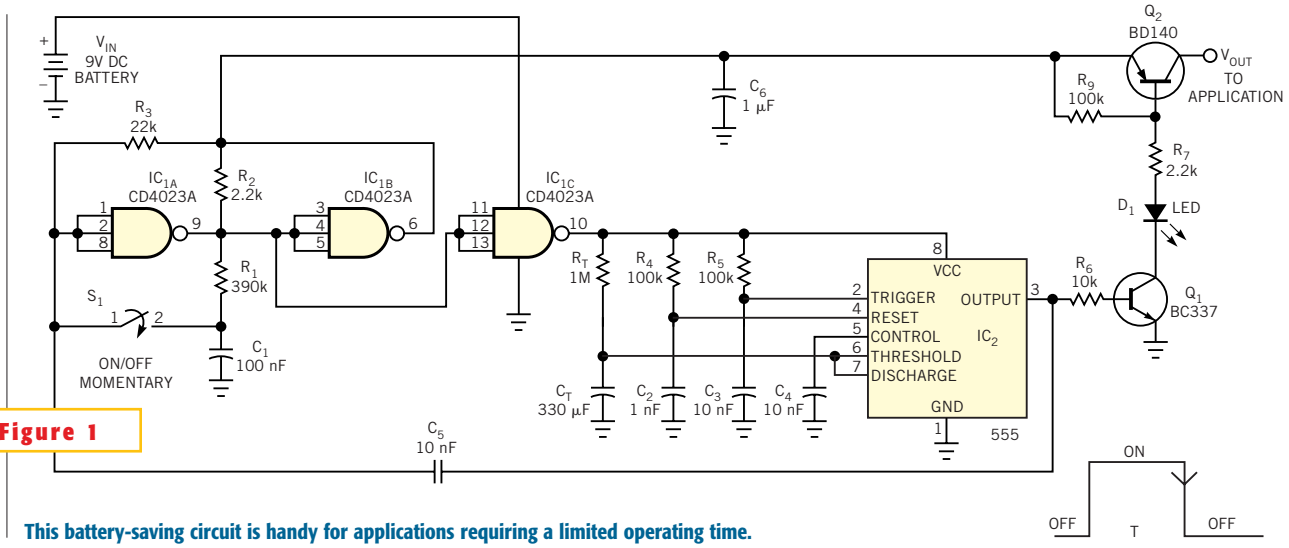

Figure 1

This battery-saving circuit is handy for applications requiring a limited operating time.

are negligible, because the circuit draws power only from the CMOS gate in the inactive off-state. LED D_1 indicates the on-off status of the circuit. No extra power comes from the battery to drive this LED, because it is connected in the current-source leg of the driver transistor. The output transition to 0V during timeout ensures the timed power-off by means of the C_5 feedback loop that toggles the bistable circuit to the off state, performing the same role you might have forgotten with the on/off switch. This simple circuit is useful when the application doesn't require a microcontroller.□

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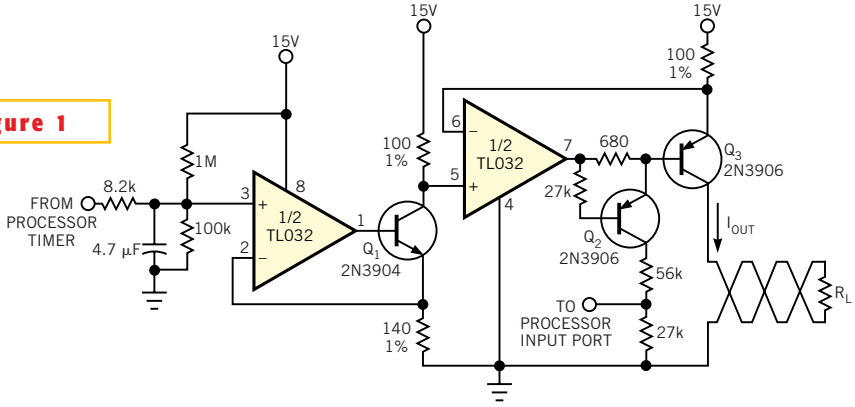
Edited by Bill Travis

Circuit provides 4- to 20-mA loop for microcontrollers

Robert Most, Dow Corning Corp, Auburn, MI

THE 4- TO 20-MA current loop is ubiquitous in the world of controls in manufacturing plants. Discrete logic, microprocessors, and microcontrollers easily cover the digital portions of control schemes, such as limit switches, pushbuttons, and signal lights. Interfacing a 4- to 20-mA output to a rudimentary microcontroller can be problematic. A built-in A/D converter would be nice, but such a device is sometimes unavailable in the "economy" line of these processors. Serial 4- to 20-mA chips exist but are relatively expensive and require serial programming and involve microcontroller overhead. Most lower end chips lack dedicated serial ports and require pin-programming.

Figure 1



This configuration provides both a 4- to 20-mA loop and an open-circuit indication.

This circuit is a low-cost alternative that provides not only a 4- to 20-mA output, but also a digital feedback signal that indicates an open wire in the current loop (**Figure 1**). One output-port pin sets the current, and one input-port pin monitors an open circuit in the loop wire. The circuit does not require the open-loop feedback portion of the circuit for the current loop to operate; you can omit it for further cost savings.

The circuit derives its drive from a simple timer output in the microcontroller. The duty cycle of the timer determines the output current of the circuit. The input RC network in front of the first operational-amplifier signal conditions the pulse train from the processor, so that the op amp interprets it as a dc voltage. In addition, the network ensures that the minimum input voltage is close to 100 mV, even if the input is at ground potential. This minimum voltage ensures that the feedback loop of the first op amp does not fold back to the positive rail when you cut off npn transistor Q_1. If you use a dual supply, the transistor has the additional voltage swing below ground potential to keep it in its active region and does not cut off. The emitter resistor of npn transistor Q_1 sets the current span of the circuit. With a 5V drive from the microcontroller, the output current is 20 mA. A grounded input results in less than 1 mA. A duty cycle of 12.5% drives the loop at 4 mA and exhibits linear control to full scale. Although it may not be mandatory, most current loops prefer a grounded return path. The purpose of the second operational amplifier is to provide a current source, rather than the current sink of the first stage, and the grounded return path. Hence, pnp transistor Q_3 provides this high-side drive. Bipolar-junction transistors Q_1 and Q_3 meet cost considerations, but you could also use MOSFETs for slightly better performance.

The open-loop feedback portion of this circuit lets the microcontroller know that a fault condition exists on the line. The processor can then execute alarm, shutdown, or other control functions to mitigate possible safety concerns. When an open-loop condition occurs, Q_3 shunts the entire loop current back through its emitter-base junction and through the 680Ω resistor to the op amp. The voltage developed across the 680Ω resistor turns on Q_2, resulting in a logic-one feedback to the microcontroller. Note that the open loop requires at least 1 mA of current for the open indication to function, which is below the normal 4 mA—a "zero" output condi-

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tion for this type of control system.

Response time for a step change is approximately 500 msec, which is acceptable for most current-loop control devices, such as control valves. If the microcontroller you select has a built-in A/D converter, response time can decrease by a couple of orders of magnitude with the elimination of the input-filtering network. Op-amp selection is important if you use a single-supply topology. An operational amplifier that can maintain stability close to its negative, or ground, rail is an important asset.□

Minimize the short-circuit current pulse in a hot-swap controller

Jim Sherwin and Thong Huynh, Maxim Integrated Products, Sunnyvale, CA

Because of internal circuit-breaker delay and limited MOS-gate pulldown current, many hot-swap controllers do not limit current during the first 10 to 50 µsec following a shorted output. The result can be a brief flow of several hundred amperes. A simple external circuit can counter this problem by minimizing the initial current spike and terminating the short circuit within 200 to 500 nsec. A typical 12V, 6A, hot-swap-controller circuit contains, as do many others, slow and fast comparators with trip thresholds of 50 and 200 mV (**Figure 1**). The 6-mΩ sense resistor, R_S, allows a nominal slow-comparator trip at 8.3A for overload conditions and a fast-comparator trip at 33.3A for short circuits. Only circuit resistances limit the initial short-circuit current spike during a period that includes the fast-comparator delay and the 30 µsec it takes to complete interruption of the short circuit by discharging M_1's gate capacitance. Various elements, such as R_S and the on-resistance of M_1, contribute to the circuit resistances. The waveform recorded during a short circuit indicates a peak current of 400 from the 2.4V peak across R_S, decreasing to 100A in 28 µsec (**Figure 2**).

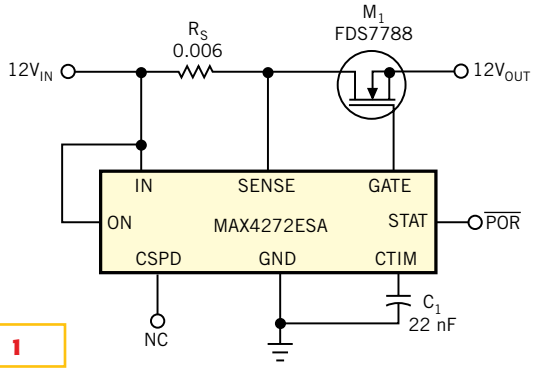


Figure 1 A typical hot-swap controller circuit exhibits a 30-µsec short-circuit current pulse of 400A peak.

You can limit the short-circuit current duration to less than 0.5 µsec by adding a Darlington pnp transistor, Q_1, to speed the gate discharge (**Figure 3**). D_1 allows the gate to charge normally at turn-on, but, at turn-off, the controller's 3-mA gate-discharge current is directed to the base of Q_1. Q_1 then acts quickly to discharge the gate, in less than 100 nsec. Thus, the high-current portion of the short circuit is limited to slightly more than the fast comparator's delay time of 350 nsec. The apparent reverse overshoot current and the steep rise in the waveform of **Figure 4** arise from parasitic series inductance in the sense-resistor chip. The circuit of **Figure 5** can limit short-circuit current to approximately 100A for less than 200 nsec. The pnp transistor, Q_{1A}, which triggers when the voltage across R_S reaches approximately 600 mV, drives the npn transistor, Q_{1B}, to quickly discharge M_1's gate capacitance. The steep voltage waveform aids quick triggering of the pnp transistor.

The oscilloscope's ground lead introduces an artifact, which appears as the leading-edge oscillation in **Figure 6**. Again, as in **Figure 4**, the apparent reverse-overshoot current and the steep rise in the waveform of **Figure 6** arise from parasitic series inductance in the sense-resistor chip. C_2 connects between the gate and source of M_1 to reduce the positive-transient step voltage applied to the gate during a short circuit. Zener diode D_1 reduces $I_{D(ON)}$ by limiting V_{GS} to less than the 7V available from the MAX4272. Although D_1

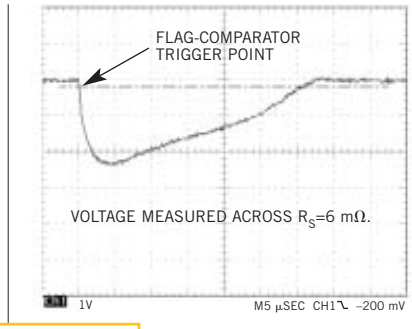


Figure 2 The short-circuit current in Figure 1 is 400A, decreasing to 100A in 28 µsec.

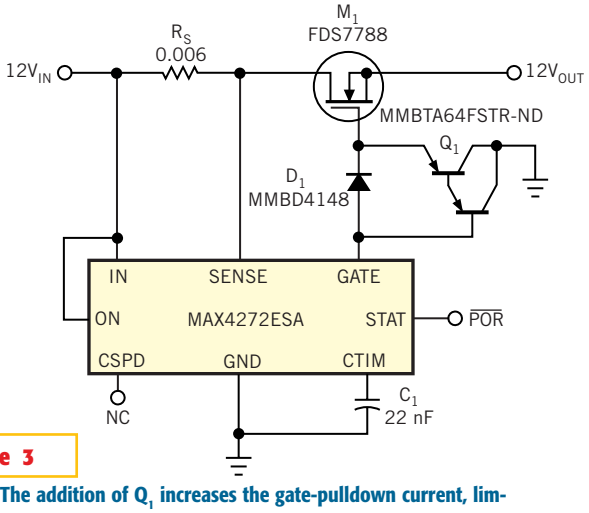


Figure 3 The addition of Q_1 increases the gate-pulldown current, limiting the short-circuit-current duration to less than 0.5 µsec.

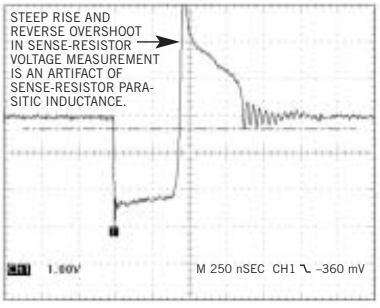


Figure 4 The steep rise and reverse overshoot in Figure 3's circuit are artifacts of sense-resistor parasitic inductance.

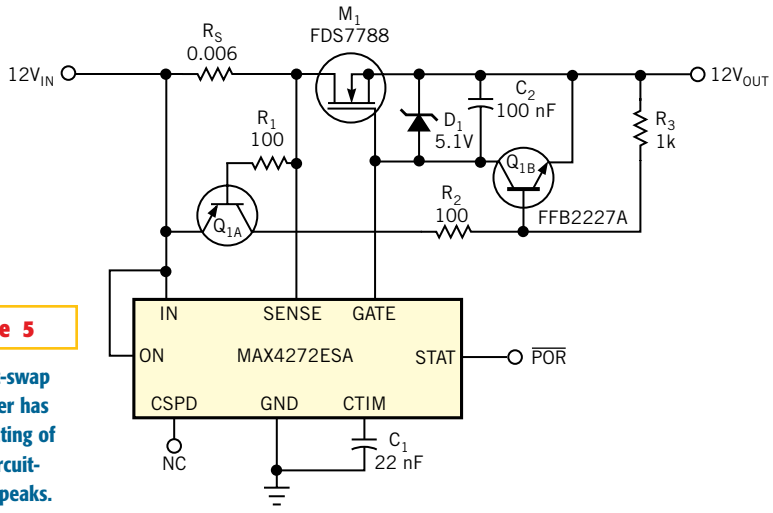


Figure 5 This hot-swap controller has fast limiting of short-circuit-current peaks.

is rated at 5.1V when biased at 5 mA, it limits V_{GS} to approximately 3.4V in this circuit because only 100 µA of gate-charging current (zener-bias current) is available from the IC. The limited V_{GS} lowers $I_{D(ON)}$—at some expense to on-resistance—and allows a quicker turn-off of M_1. You could also use D_1 and C_2 to some advantage in **figures 1** and **3**, to reduce $I_{D(ON)}$ during short circuits.

Either of the two circuits can protect a backplane power source by minimizing the energy dissipated when a hot-swap-controller circuit incurs a short circuit. The simpler circuit (**Figure 3**) dramatically shortens the short-circuit-current interval to somewhat less than 500 nsec, and the slightly more complex circuit (**Figure 5**) reduces the peak short-circuit current to 100A, as well as truncating the pulse width to less than 200 nsec. You can apply either technique to most hot-swap-controller circuits. Individual results vary according to the impedance of the power source, the impedance of the short circuit, and the quality and attack time of the short circuit itself. Note that it is inordinately difficult to achieve a repeatable low-resistance short circuit by manual manipulation of a shorting bar. You require careful layout and low-ESR capacitors to create a power source with very low ESR.□

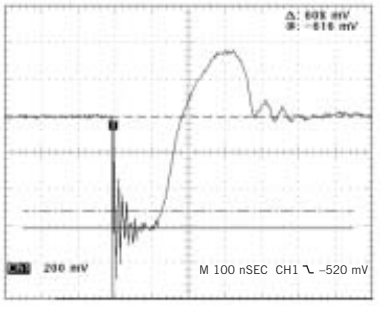


Figure 6 This waveform depicts the short-circuit-current peaks for the circuit in Figure 4.

Reduce EMI by sweeping a power supply's frequency

John Betten, Texas Instruments, Dallas, TX

Switching power supplies can be notorious noise generators. You should prevent this noise, which is conducted, radiated, or both, from returning to the input source, where it can potentially wreak havoc on other devices operating from the same input power. The goal of an EMI (electromagnetic-interference) filter is to block this noise and provide a low-impedance path back to the noise source. The larger the noise, the greater the size, expense, and difficulty of the filter design. Power supplies that operate at a fixed frequency have their largest EMI emission at this fundamental, fixed frequency. Emissions also occur at multiples of the switching frequency but at diminished amplitudes. The simple circuit in **Figure 1** makes the switching converter operate over multiple frequencies rather than one, thereby reducing the time average at any one frequency. This scheme effectively lowers the peak emissions.

The circuit in **Figure 1** is a self-starting oscillator with an oscillation frequency of approximately 500 Hz. When you apply power, C_3 begins to charge up from 0V, and the output of the TL331 comparator is in a high-impedance state because its noninverting input sees a higher voltage than that of the inverting input. As C_3 charges, its voltage crosses the voltage reference of the R_1-R_6 divider, and the comparator output trips to a low state. The voltage on R_6 instantly drops to a lower reference level because R_5 is now in parallel with R_6. C_3 begins to discharge toward this new reference level because R_3 is simultaneously in parallel with C_3. The cycle repeats after C_3 discharges to the voltage on R_6 when the comparator output reopens. You must carefully select the components to ensure that the two voltage-reference states of R_6 are lower than the upper and lower possible charge states of C_3. The circuit uses C_3 to adjust the oscillator frequency; you should select C_3 to have a lower value than C_2. The oscillator's frequency is approximately equal to

$$f = \frac{1}{-2R_2C_3 \ln\left[1-\frac{\Delta V_{REF}}{V_{BIAS}}\right]}.$$

Capacitor C_2 ac-couples the ramp voltage of C_3 into the UCC3813's oscillator pin. The injected signal adds to the charging current of C_T during its positive portion (ac signal), thus increasing the controller's operating frequency. During the injected signal's negative portion, some of C_T's charging current disappears, slowing the controller's operating frequency. **Figure 2** shows the effects of the injected signal on the charging of C_T. R_4 controls the magnitude of the current that is injected. Reducing R_4's value increases the range, or spread, of the operating frequency around its nominal fixed frequency. The injected signal's oscillation frequency, which C_3 sets, controls the frequency-sweep rate.

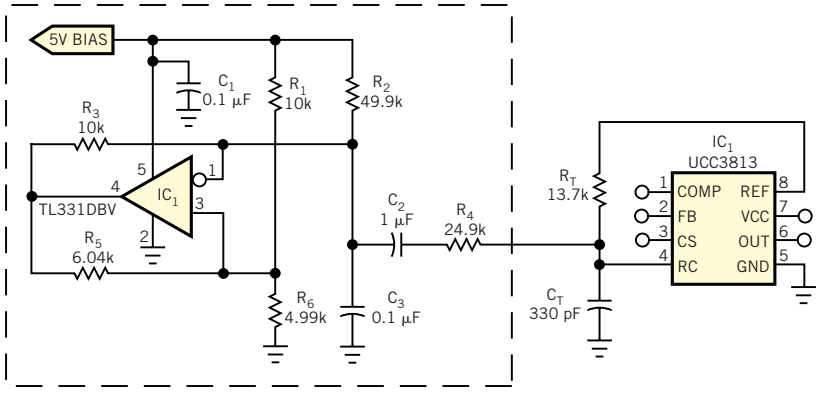


Figure 1 A low-frequency oscillator ramp, injected into the RC pin, modulates the supply's switching frequency.

The differential EMI-current measurement of **Figure 3** (1 dBµV=1 dBµA) shows the before-and-after effects of adding the frequency-shifting oscillator. This design easily achieves a 10-dBµA reduction with a 12-kHz sweep window. A wider window further reduces EMI, but the modulator frequency may be noticeable in the converter's output ripple voltage. It is also desirable to make the injected ramp voltage as linear in shape as possible to prevent the switching converter from spending excess time at its switching-frequency limits. The nonlinearity can result in an EMI response with two distinct frequencies. You must take care not to operate the circuit below the power converter's low-frequency limits, or saturation of magnetics may occur. This circuit demonstrates a low-cost, small-area approach to reducing conducted-EMI emissions.□

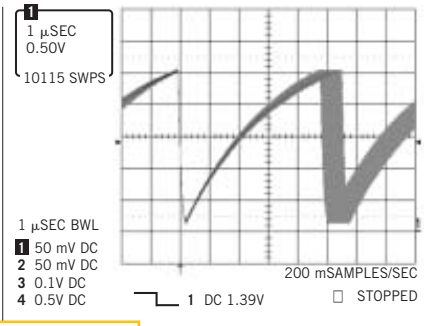


Figure 2 The external oscillator varies the charging of the timing capacitor.

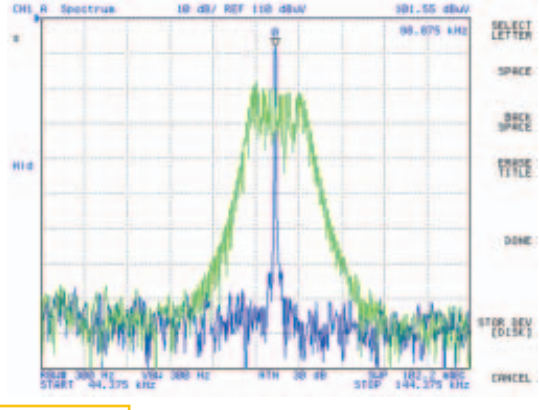


Figure 3 The EMI of the flyback converter differs with and without external modulation.

Get just enough boost voltage

Kieran O'Malley, On Semiconductor, East Greenwich, RI

Adding a current-mirror circuit to a typical boost circuit allows you to select the amount of boost voltage and to ensure a constant difference between the input and the output voltages (**Figure 1**). This circuit is useful for high-side-drive applications, in which a simple voltage doubler is unacceptable because of the voltage range of the components involved or where the input voltage can vary widely. You can also use the circuit at the front end of a power supply to ensure that the PWM controller has enough voltage to start correctly in low-input-voltage con-

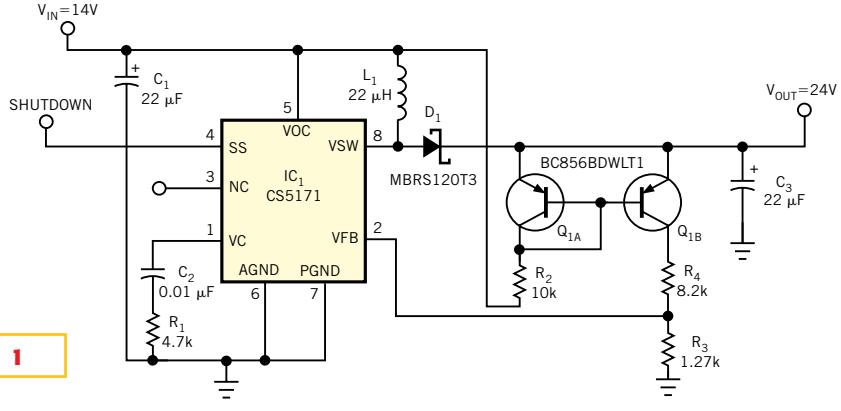


Figure 1 Adding a current-mirror circuit to a boost circuit allows you to get just enough boost voltage.

ditions. The circuit maintains a 10V difference between V_{IN} and V_{OUT}, but you can easily change it to provide other voltages. The PWM circuit in **Figure 1** is the CS5171 from On Semiconductor (www.onsemi.com), but you can use the idea with any boost circuit. The current-mirror circuit, comprising the dual-pnp transistor, Q_1, and the associated resistors, establishes a current that depends on the voltage difference between V_{IN} and V_{OUT}. The dual-pnp transistor has a V_{CEO} of 65V. In this case, V_{IN}=14V (nominal), so you need V_{OUT} to be 24V (nominal). First, calculate a value for R_2, thus establishing the reference current. If you select a reference current of 1 mA, you obtain

$$\frac{(V_{IN}-V_{OUT}-V_{BE}(Q_{1A}))}{1\ mA}=R_2$$

$$\frac{(14V-24V-0.6V)}{1\ mA}=9.4\ k\Omega.$$

Because the output voltage is not critical, you use a 10-kΩ resistor.

Q_{1B} mirrors the current and sets up the feedback voltage to the PWM circuit. The CS5171 has an internal voltage of 1.28V (typical), so R_3 yields the correct feedback voltage when the current flowing through it is 1 mA. In this case, by selecting 1.27 kΩ for R_3, you obtain an output voltage of 24V. As V_{IN} varies, V_{OUT} tracks it and maintains a 10V difference between the input and the output. R_4 helps reduce the power dissipation in Q_{1B}.□

Processor's PWM output controls LCD/LED driver

Joe Neubauer, Maxim Integrated Products, Sunnyvale, CA

The PWM (pulse-width-modulation) output available from many microprocessors is based on an internal 8- or 16-bit counter and features a programmable duty cycle. It is suitable for adjusting the output of an LCD driver (**Figure 1**), a negative-voltage LCD driver (**Figure 2**), or a current-controlled LED driver (**Figure 3**). The circuit comprises simply the PWM source, capacitor C, and resistors R_D and R_W. For CMOS circuits, you calculate the open-circuit output voltage as $V_{CONT}=D\times V_{DD}$, where V_{CONT} is the control circuit's output voltage, D is the PWM duty cycle, and V_{DD} is the logic-supply voltage. The control circuit's output impedance is the sum of the resistor values R_D and R_W: $R_{CONT}=R_D+R_W$. For the circuit of **Figure 1**, the output voltage, V_{OUT}, is a function of the PWM average voltage, V_{CONT}:

$$V_{OUT}=V_{REF}\left[1+\frac{R_1}{R_2}\right]+\frac{(V_{REF}-V_{CONT})\times R_1}{R_{CONT}},$$

where V_{REF} is the reference voltage at the feedback input.

Bear in mind that the initial charge on filter capacitor C produces a turn-on transient. The capacitor forms a time constant with R_{CONT}, which causes the output to initialize at a voltage higher than that intended. You can minimize this overshoot by scaling the value of R_D as high as possible with respect to R_1 and R_2. As an alternative, the microprocessor can disable the LCD until the PWM volt-

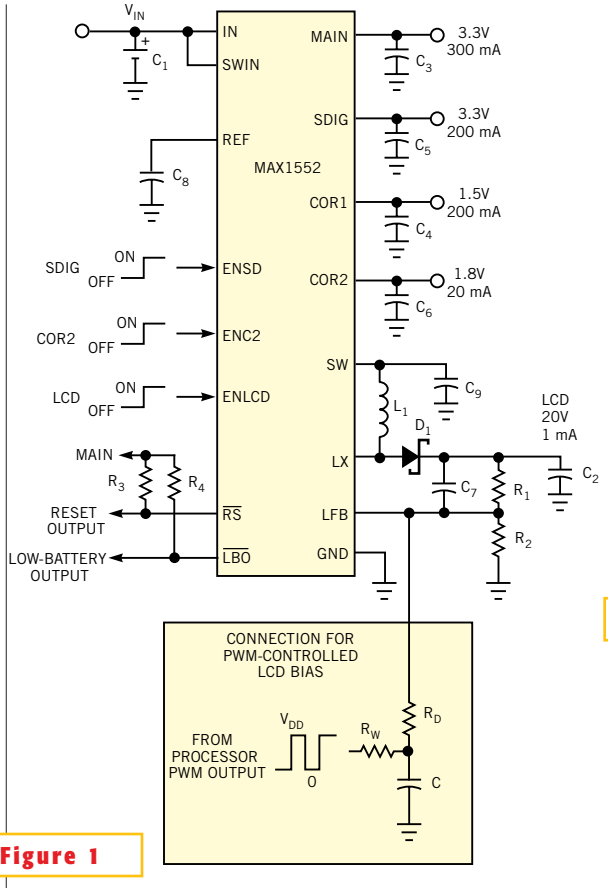


Figure 1

This simple circuit provides positive-output voltage LCD drive.

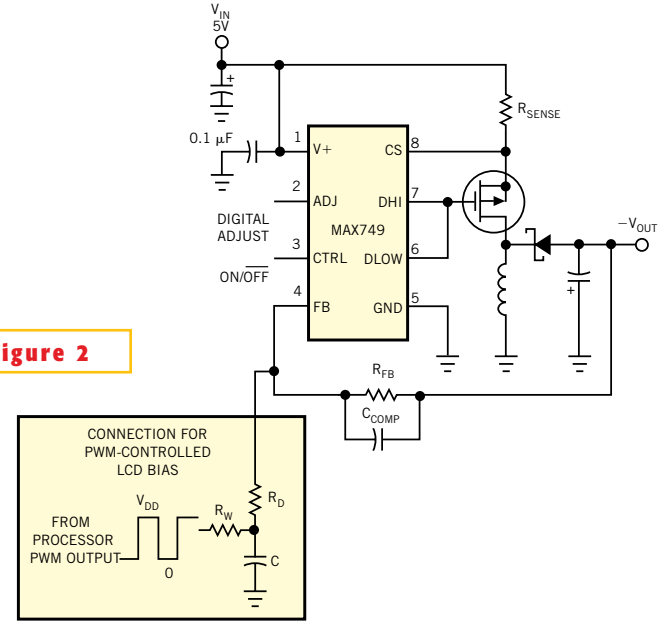


Figure 2

This configuration provides negative-output-voltage LCD drive.

age stabilizes. For **Figure 2**, the output voltage, V_{OUT}, is a function of the PWM average voltage, V_{CONT}:

$$V_{OUT} = V_{REF} + \frac{(V_{REF} - V_{CONT}) \times R_{FB}}{R_{CONT}},$$

where V_{REF} is the reference voltage at the feedback input. For **Figure 3**, the output current is a function of the PWM average voltage, V_{CONT}:

$$I_{OUT} = \left[\frac{V_{REF} + \frac{(V_{REF} - V_{CONT}) \times R_{SET}}{R_{CONT}}}{R_{SET}} \right] \times K,$$

where V_{REF} is the reference voltage at the Set output and K is the current-scaling factor.

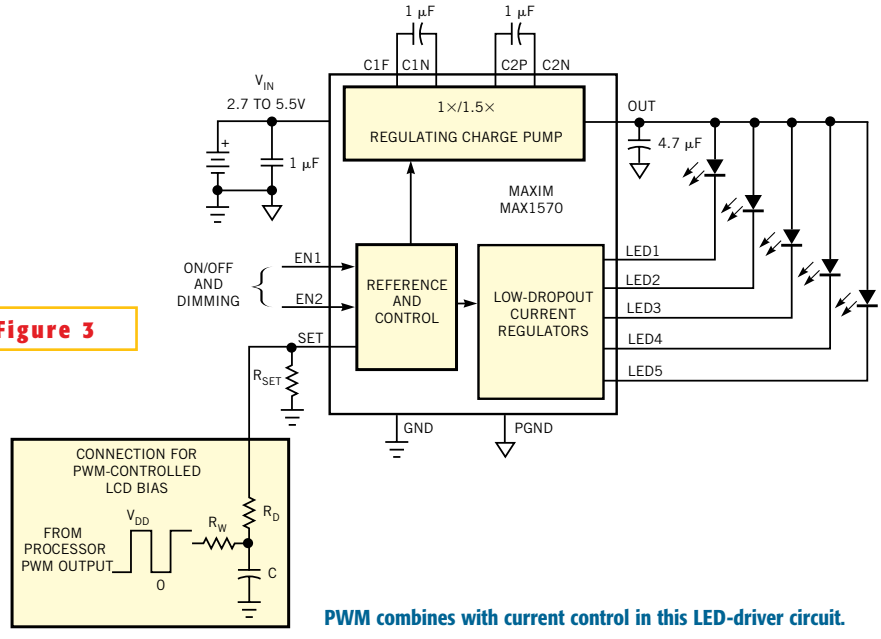


Figure 3

PWM combines with current control in this LED-driver circuit.

R_D isolates the capacitor from the feedback loop in the PWM-control methods. Assuming a stable voltage at the feedback point, the following equation defines the lowpass filter's cutoff frequency: $f_C = 1/(2\pi RC)$, where $R = R_D || R_W$. To minimize ripple voltage at the output, you should set the cutoff frequency at least two decades below the PWM frequency.□

Method provides automatic machine shutdown

Jean-Bernard Guiot, Mulhouse, France

Some machines need to run for long periods and therefore may finish their work in the middle of the night or during the weekend. For the time remaining, until the operator returns, the machines stay idle, uselessly consuming power. This Design Idea allows a machine to completely shut itself down after finishing its work. In addition, the method allows for informing the machine operator by phone. You insert the circuit into the area that **Figure 1** indicates as a dashed line into the main supply line of the machine. The relay, K_{STOP}, connects to a free output of the programmable controller of the machine. You must program the controller in such a way that relay K_{STOP} is energized as long as the process is running. In normal operation, switch S_1 stays in manual position; thus, the power contactor, K_1, is on, and the machine receives power. When an operator starts the process, relay K_{STOP} energizes, and the indicator, H_1, lights, signaling the operator that switch S_1 is ready for operation. The timer relay, K_{2T}, is also on, closing its contact 18-15. Switching S_1 to automatic now has no effect.

At the end of the process, relay K_{STOP} and indicator H_1 turn off. Because contact 18-15 of relay K_{2T} incurs a delay before opening, because K_{2T} is a time-delay relay, the machine stays on during the delay time. This delay allows a second contact of K_{STOP} to control an automatic telephone dialer (not shown) to inform the remotely located operator and allows the process to finish supplementary tasks, such as cooling down, removing chips, allowing coolant to flow back into the tanks, for example.

Once the delay time expires, the contacts of K_{2T} open, K_1 turns off, and the machine completely turns off. The varistors, V_{R1}, suppresses voltage spikes. You must select V_{R1}, K_1, K_{2T}, and H_1 in accordance with the power-mains voltage and the power rating of the machine. You select K_{STOP} according to the controller's output (the relay coil) and the power-mains voltage (the relay contacts). The circuit has worked satisfactorily in hundreds of machines over a five-year period.□

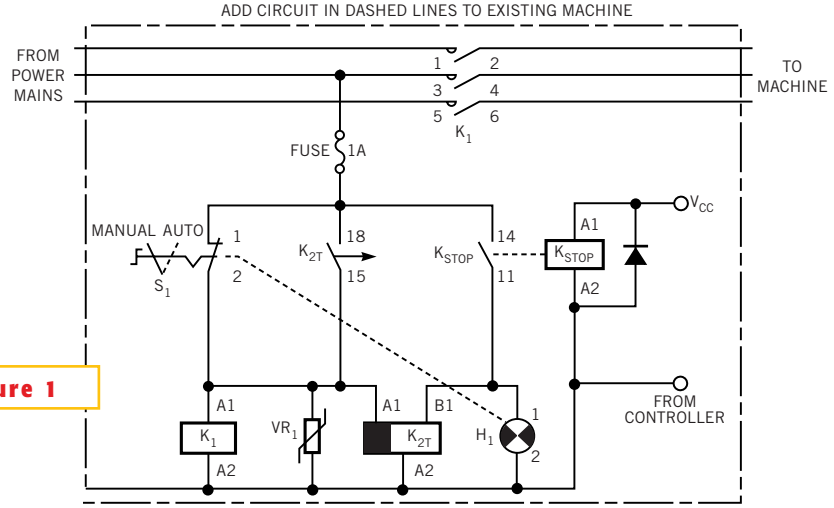


Figure 1

This circuit allows a machine to completely shut itself off after doing its assigned task.

Circuit makes simple high-voltage inverter

Francesc Casanellas, Aiguafreda, Spain

A SIMPLE HIGH-VOLTAGE MOSFET inverter solves the problem of driving a high-side MOSFET, using a low-voltage transistor, Q_1, and a special arrangement involving D_6 (**Figure 1**). This inverter is much faster than those that optocouplers drive, so dead-time problems are minimal. The inverter has the usual blocking diodes D_4 and D_6, and the parallel diodes D_5 and D_8. Q_3 provides the turn-off signal to Q_2. When Q_3 turns on, Q_2's gate short-circuits to ground through R_4. R_4 limits current and dampens oscillations. Q_2's gate discharges quickly; only the value of R_4 limits discharge time. Q_1 stays off, thanks to R_2, and C_3 charges to 12V through D_2. The gate pulse creates a current through C_4, and D_3 protects the

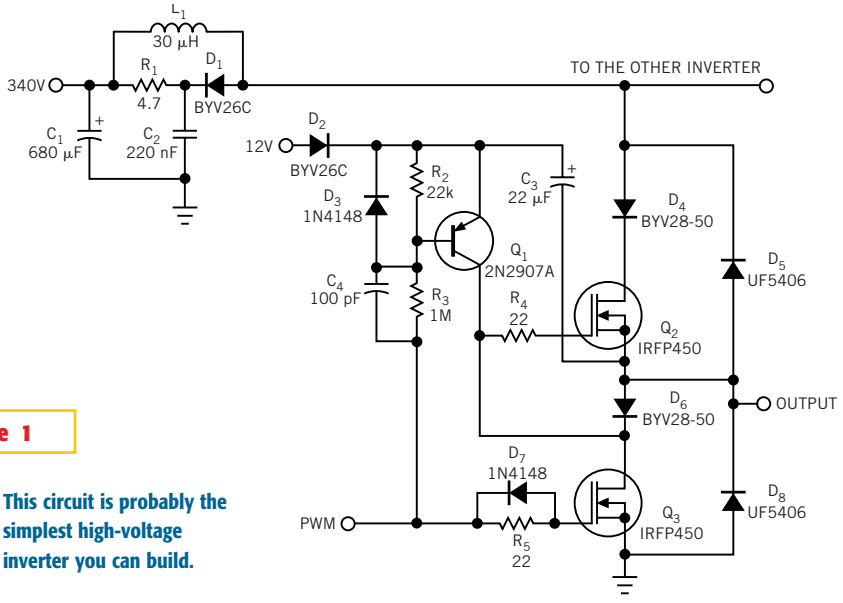


Figure 1

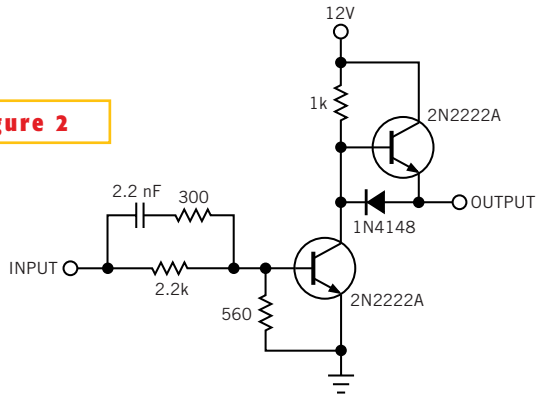
This circuit is probably the simplest high-voltage inverter you can build.

base-emitter junction of Q_1.

In the turn-on of Q_2, the following scenario occurs: When the control input, PWM, goes low, Q_3 quickly turns off, thanks to D_7. A displacement current, $C_4 \times dV/dt$, flows through C_4 to the base of Q_1. Q_1 charges the output capacitance of Q_3 and the gate capacitance of Q_2, and Q_2 turns on. C_3 supplies the collector current. If the period is long, Q_1 keeps conducting and compensating the leakage of Q_3. If D_6 were a Schottky diode, which is leaky, you would have to reduce the value of R_1. A short cross-conduction period exists between the two MOSFETs, a phenomenon that is more apparent when Q_3 turns off and Q_2 turns on. A small inductor, L_1, in series with the main supply limits the current spikes. The inductor needs a snubber comprising D_1, R_1, and C_2. Note that the inductor value is conservative and can be smaller.

The values are for a 370W, three-phase inverter with 150% overload capacity. If you change the MOSFET, the value of C_4 has to change according to the total gate charge plus the output capacitance of Q_3, which is much lower and, in fact, negligible. Q_1 amplifies the capacitor current, so C_4 is proportional to $Q_{G2} \times h_{FE1}$. Make C_4's value no higher than necessary, because the base current in Q_1 would be too high. To obtain all the speed advantages of the circuit, the PWM signal should be able to quickly drive Q_3. If necessary, you can use a buffer circuit (**Figure 2**). You can drive the circuit with a single CMOS gate. The circuit in **Figure 1** is probably the simplest high-voltage inverter you can design. It has served in thousands of three-phase motor drives from 0.37 to 0.75 kW.□

Figure 2



This buffer enhances speed at the PWM input of Figure 1's circuit.

Edited by Bill Travis

Circuit provides ISFET-sensor bias

Brian Harrington, Analog Devices, Wilmington, MA

ISFETs (ion-sensitive field-effect transistors) are useful for measuring the acidity of fluids. Accurate measurements require that the ISFET's bias conditions (I_D and V_{DS}) be held constant while the gate is exposed to the fluid under test. The acidity of the fluid changes the channel width, resulting in a gate-source voltage, V_{GS}, that is proportional to the fluid's pH. A recently published Design Idea shows a biasing circuit for the ISFET (**Reference 1**). The circuit in **Figure 1** provides a simpler and more accurate implementation. Voltage V_A sets I_D, the drain current, through ISFET Q_1, while voltage V_B sets V_{DS}, the drain-source voltage across Q_1. Both AD8821 high-precision instrumentation amplifiers, IC_1 and IC_2, are configured for unity gain. IC_3, the AD8627 precision JFET-input amplifier, buffers the drain voltage, V_D, ensuring that all of the current flowing through R_1 flows through Q_1.

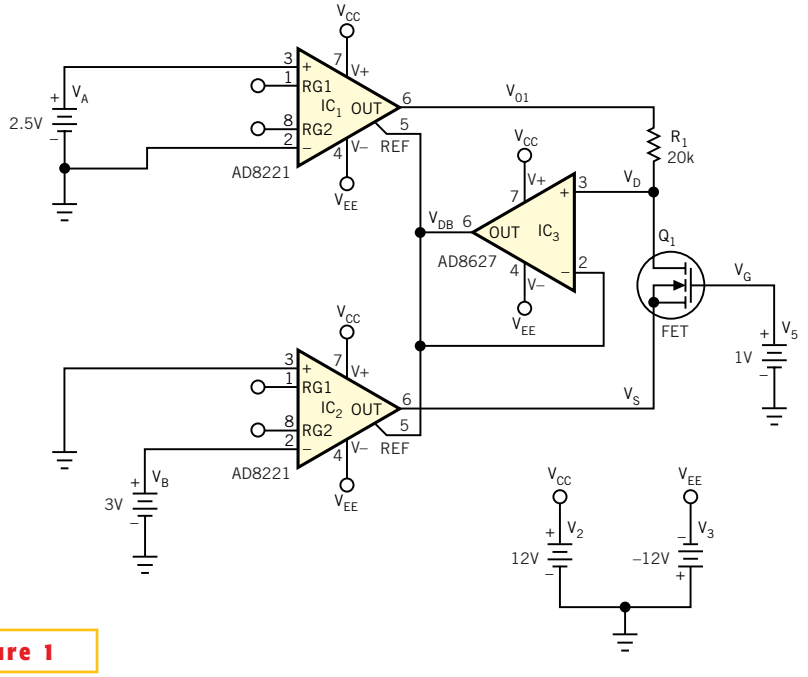


Figure 1

This circuit provides ideal bias for an ISFET, a sensor used to measure fluid acidity.

To control I_D, amplifier IC_1 forces the differential voltage between its output and the reference input to equal its differential input voltage, V_A. Because the sensed differential voltage is equal to the voltage across R_1, $I_D = V_A / R_1$. With R_1 set to 20 kΩ, I_D scales to 50 µA/V. Similarly, amplifier IC_2 forces the differential voltage between its output and the reference input to equal its differential input voltage, V_B, thus forcing V_{DS} to equal V_B. (Note: If your design does not require independent adjustment of V_{DS} and I_D, the circuit can operate from a single control voltage. Tie V_A and V_B together and drive it with the desired voltage V_{DS}. R_1 is then equal to V_{DS}/I_D.) The voltage of interest, V_{GS}, appears between the gate voltage and the output of IC_2. A useful feature of this circuit is that the current source floats, enabling the gate voltage to connect to any voltage within the common-mode range of the circuit. For this circuit, the range of V_G is $(V_A+2-V_{EE}) < V_G < (V_{CC}-2-V_A)$.

Figure 2 shows the advantage of the

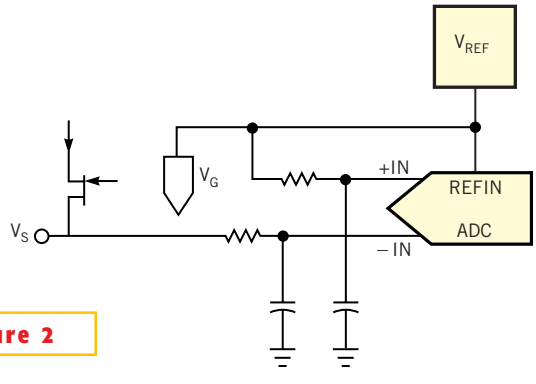


Figure 2

This configuration shows the advantage of the floating gate when the circuit of Figure 1 connects to an ADC.

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floating gate when the circuit is connected to the AD7790 differential-input sigma-delta ADC. The gate voltage connects directly to the ADC's reference. The only signal-conditioning circuitry required between V_S or V_G and the ADC's input is a simple RC filter. The 0.1% error in resistor R_1 dominates the current-source errors for currents higher than 1 µA and, therefore, are less than 250 nA for drain currents as high as 250 µA. The V_{DS} errors originate from the gain error of IC_3 and input offset voltages of IC_2 and IC_3. The error in drain-source voltage is less than 450 µV for drain-source voltage as high as 2V.□

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1. Casans, S, AE Navarro, and D Ramirez, "Circuit forms novel floating current source," *EDN*, May 1, 2003, pg 92.

Microprocessor supervisor and regulator form in-range voltage monitor

Ilie Poenaru and Sabin Eftimie, Catalyst Semiconductor, Bucharest, Romania

Low-cost microprocessor supervisors reset controllers when power-supply voltages fall below given levels. As added protection, you can also reset the microcontroller when the power supply is too high by combining a low-cost shunt-voltage regulator with a supervisor that has a manual reset input. A simple overvoltage/undervoltage-protection circuit is easy to make (**Figure 1**). The circuit's output is active (low) when the monitored supply voltage, V_{CC}, is outside a predefined range. After the supply voltage returns to within the functioning limits, the reset output, $\overline{RST}$, remains active for a minimum of 140 msec. This interval gives the system time to stabilize before you remove the reset. The threshold voltage of the CAT811 microprocessor reset circuit, IC_2, sets the lower limit of the voltage range, V_{LOW}. This threshold can be 2.32 to 4.63V using standard products. Custom threshold devices with thresholds as low as 1.8V are also available. The 1.24V CAT431L shunt regulator, IC_1, and two resistors, R_1 and R_2, set the upper limit, V_{HIGH}: $V_{HIGH}=V_{REF}(1+R_1/R_2)$, where V_{REF} is the internal reference voltage of IC_1 ($V_{REF}=1.24V$). The maximum V_{HIGH} that you can set is 5.5V, and the maximum supply voltage is 9V.

This design uses the CAT811 supervisor with a threshold voltage of 4.63V

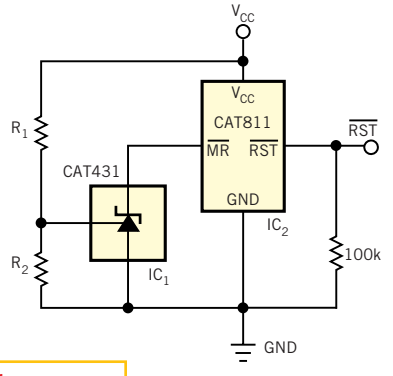


Figure 1

This simple circuit uses a microprocessor supervisor and a shunt regulator to form an overvoltage/undervoltage-protection circuit.

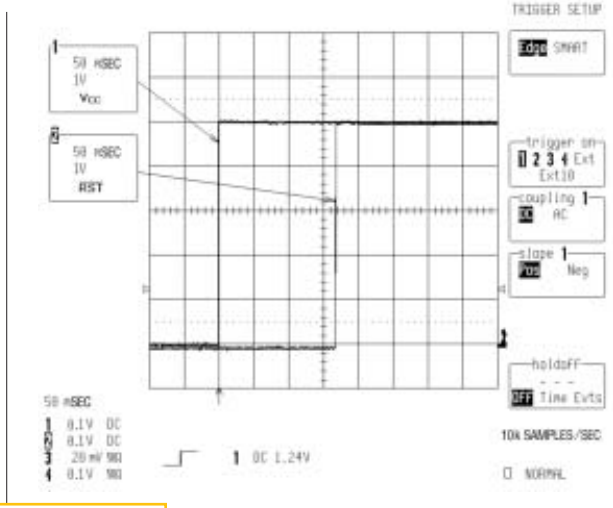


Figure 2

As the supply voltage rises into range, the reset pin in Figure 1 becomes active low.

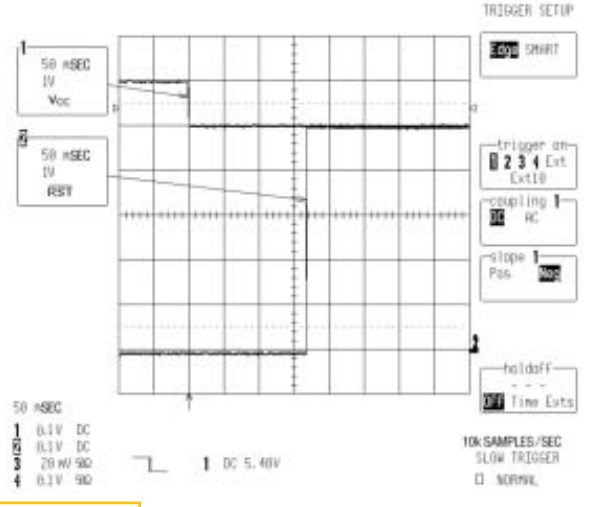


Figure 3

As the supply voltage falls into range, the reset pin in Figure 1 becomes active low.

for tests. The upper limit of the voltage range is 5.5V using a 10-kΩ potentiometer with R_1=7.75 kΩ and R_2=2.25 kΩ. As the supply voltage rises into range, the reset pin becomes active (low) for a minimum of 140 msec (**Figure 2**). When the supply voltage falls into range, the reset pin also becomes active (low) for a minimum of 140 msec (**Figure 3**). A reset signal asserts when the supply voltage increases out of range (**Figure 4**). A reset signal also asserts when the supply voltage falls out of range (**Figure 5**).□

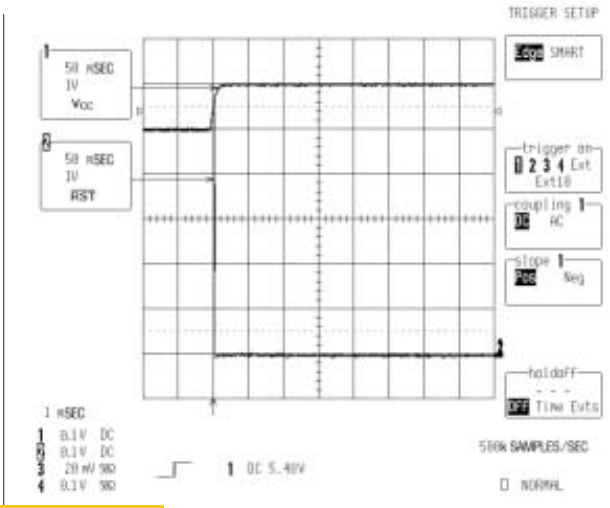


Figure 4

The reset signal in Figure 1 asserts when the supply voltage increases out of range.

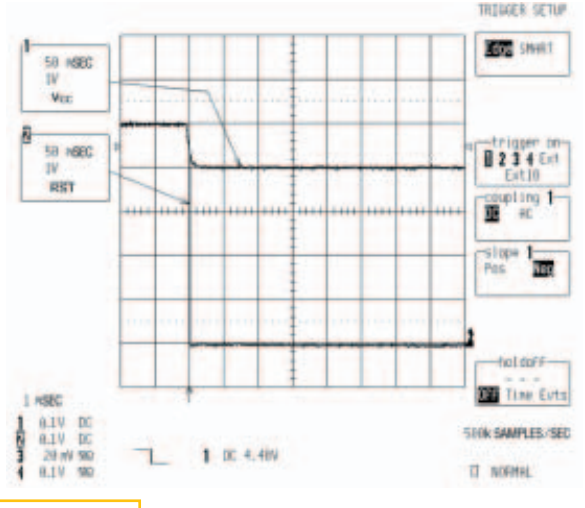


Figure 5

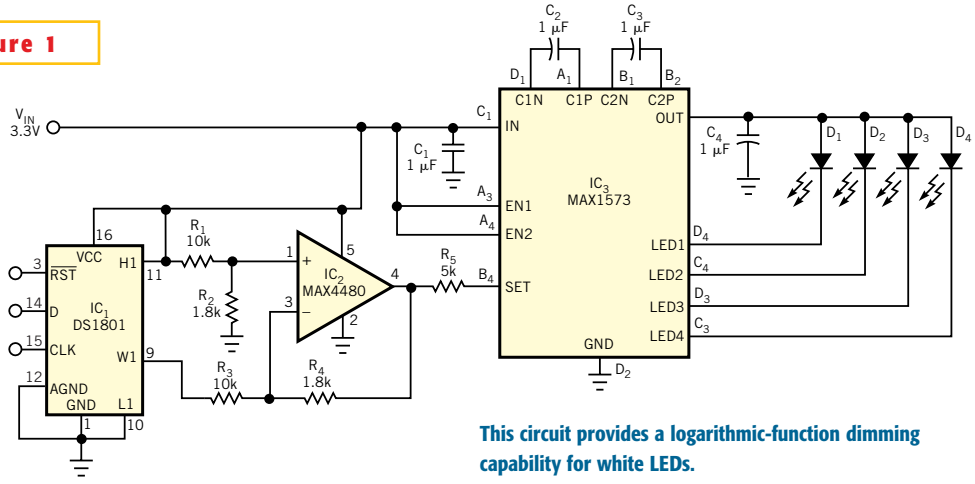
The reset signal in Figure 1 asserts when the supply voltage falls out of range.

White-LED driver provides 64-step logarithmic dimming

William Hadden, Maxim Integrated Products, Sunnyvale, CA

The circuit of **Figure 1** is designed for portable-power applications that require white LEDs with adjustable, logarithmic dimming levels. The circuit drives as many as four white LEDs from a 3.3V source and adjusts the total LED current from 1 to 106 mA in 64 steps of 1 dB each. The driver is a charge pump that mirrors the current I_{SET} (sourced from IC_3's SET terminal) to produce a current of (215•I_{SET}±3%) through each LED. Internal circuitry maintains the SET terminal at 0.6V. To control the LED brightness, op amp IC_2 monitors the difference between the high-side voltage and the wiper voltage of digital potentiometer IC_1. The op amp then multiplies that voltage by a gain to set the maximum output current. Zero resistance at the potentiometer's W1 terminal corresponds to minimum LED current and, therefore, minimum brightness. Because the SET voltage is fixed at 0.6V, any voltage change at the left side of R_5 changes I_{SET}, and the resulting change in LED

Figure 1



This circuit provides a logarithmic-function dimming capability for white LEDs.

currents alters their brightness level. R_5 sets the maximum LED current: $R_5 = 215 \times 0.6/I_{LED(DESIRED)}$, where I_{LED} is the current through one LED.

IC_1 is a digital potentiometer with a logarithmic taper and an analog-voltage wiper. Each wiper tap corresponds to 1 dB of attenuation between H1 and W1 (pins 11 and 9). The IC contains two potentiometers controlled by a 16-bit code via a three-wire serial interface. To set the LED current, drive $\overline{RST}$ high and clock 16 bits into the D terminal of IC_1, starting with the LSB. Each pulse at CLK enters a bit into the register. The circuit uses only one potentiometer, so bits 0 through 7 are "don't-care" bits. Bits 8 through 14 determine the wiper position: Bits 8 through 13 set the code, and bit 14 is "mute." (Logic one at bit 14 produces the lowest possible output current by setting the left side of R_5 at approximately 0.599V.) After entering all 16 bits, enter the code and change the brightness level by driving $\overline{RST}$ high. **Figure 2** shows the logarithmic relationship between an LED current and the potentiometer's input code.□

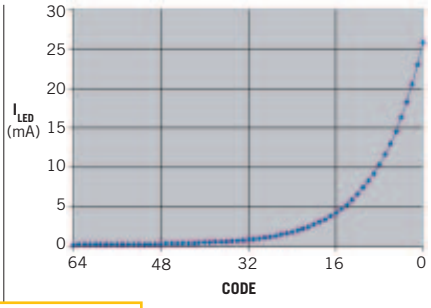


Figure 2

LED current versus input code changes for the circuit in Figure 1.

Switcher improves overvoltage-protection circuit

Jason Rubadue, National Semiconductor, Thornton, CO

Overvoltage-protection circuits often protect electronic devices from power-supply transients, such as a rise from plugging in batteries or an external power adapter. Although these devices traditionally find use as hysteretic switching controllers, you can reconfigure the LM3485 (**Figure 1**) to provide a robust overvoltage-protection circuit.

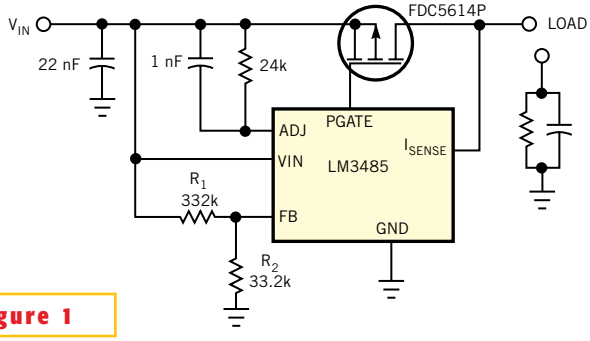


Figure 1

A hysteretic switching controller can do double duty as an overvoltage-protection circuit.

By selecting the feedback resistors using the formula $V_{IN} = 1.252(R_1+R_2)/R_2$, you can program the IC to trip off at any level from 4.5 to 35V. In **Figure 1**, R_1 and R_2 turn off the PFET when V_{IN} exceeds 13.8V. You can calculate the hysteresis using the formula $V_{HYS} = 0.01(R_1+R_2)/R_2$. In this example, the expression calculates a hysteresis of 110 mV. The accompanying oscilloscope plot of V_{OUT} versus V_{IN} shows the sample circuit with a hysteresis of roughly 800 mV (2V/division, 0V level at lowest line, 500 nsec/division). Why isn't it 110 mV as calculated? We measured the turn-off propagation delay of the sample circuit at approximately 450 nsec, almost one complete time division, whereas the turn-on propagation delay was only 70 nsec (all measured using a 40Ω load). By taking these propagation delays into account, the scope plot approaches the calculated hysteresis and 13.8V trip level. However, compare these times with competing ICs with larger typical propagation delays of 500- to 6000-nsec turn-off times and 1800- to 7000-µsec turn-on times. The improved propagation delay is a result of the LM3485's driver, which can sink 320 mA and source 440 mA, as opposed to other overvoltage-protection circuits, which sink only approximately 60 mA.

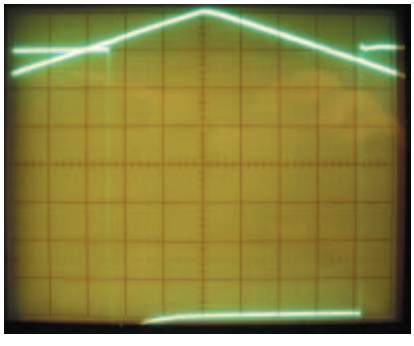


Figure 2

This plot shows the hysteresis and the overvoltage trip point.

The LM3485 also has an adjustable overcurrent-protection feature. In the sample circuit, when the current exceeds 1.1A, the LM3485 turns off the FET. After 9 µsec, the LM3485 turns back on the FET and begins sensing the current again through the FET's on-resistance. For more precise current sensing, add an external current-sense resistor between the FET and V_{IN} and then move the I_{SENSE} line of the LM3485 over to the source of the FET. The sample circuit in **Figure 1** is derived from the standard LM3485 evaluation board. You can easily modify this board to create an overvoltage-protection circuit by removing a few components—the inductor, the diode, and the C_{FF} capacitor—by moving the feedback line from V_{OUT} to V_{IN}, and by selecting suitable resistor values.□

Precision peak detector uses no precision components

Jim McLucas, Longmont, CO

When you need a precision peak detector, you would usually implement it with one or several op amps and a few other associated components. This technique usually works well unless your design requires operation higher than a few kilohertz. In designs requiring such operation, the accuracy of the circuit severely deteriorates unless at least one of the amplifiers has a high slew rate and frequency response extending to tens or even hundreds of megahertz. Performance depends on the desired frequency response and peak-to-peak input-voltage range of the peak detector (**Reference 1**). The circuit in **Figure 1** uses a moderately fast, inexpensive comparator instead of a high-slew-rate op amp to implement the peak detector. This circuit provides wide bandwidth and high accuracy without the use of precision components, and it's simple and inexpensive—about $3.50 (1000).

The high-input-impedance FET source follower, Q_1, and the associated circuitry enclosed by the dotted line in **Figure 1** buffer the input to the comparator. This buffer is essentially the design published in **Reference 2**. Op amp IC_{2D} forces the dc voltage at the input to the comparator at the junction of D_1 and R_3 to be equal within a few millivolts to the dc voltage at the FET gate. If the peak detector has a driver with an impedance of less than approximately 150Ω, you can eliminate the buffer in the dotted-line box. However, as the source impedance increases, the accuracy of the peak detector decreases if you don't use the buffer. An LM306 comparator, IC_1, provides sufficient speed and current to charge the holding capacitor, C_3, over an input range of 25 Hz to more than 1 MHz, with an input-voltage range of 500 mV peak to more than 4V peak. The comparator exhibits a few millivolts of hysteresis, which improves its switching speed and prevents random oscillation when its input voltage is in its linear range.

This circuit works by essentially creating its own reference for the negative input of the comparator. If the voltage on the positive input of the comparator is greater than the voltage at the negative input, the comparator's output goes high and charges capacitor C_3 until the voltage on the capacitor is a few millivolts greater than the voltage on the positive input. Then, the comparator stops charging C_3 until the cycle repeats. This action ensures that the voltage on holding capacitor C_3 is nearly equal to the peak voltage at the input to the comparator. Schottky diodes D_2 and D_3 couple the output to the holding capacitor, C_3. The feedback from the output of IC_{2A} to the junction of D_2 and D_3 keeps D_3 biased to 0V when it is off, thereby preventing reverse leakage through D_3 (**Reference 2**). The feedback

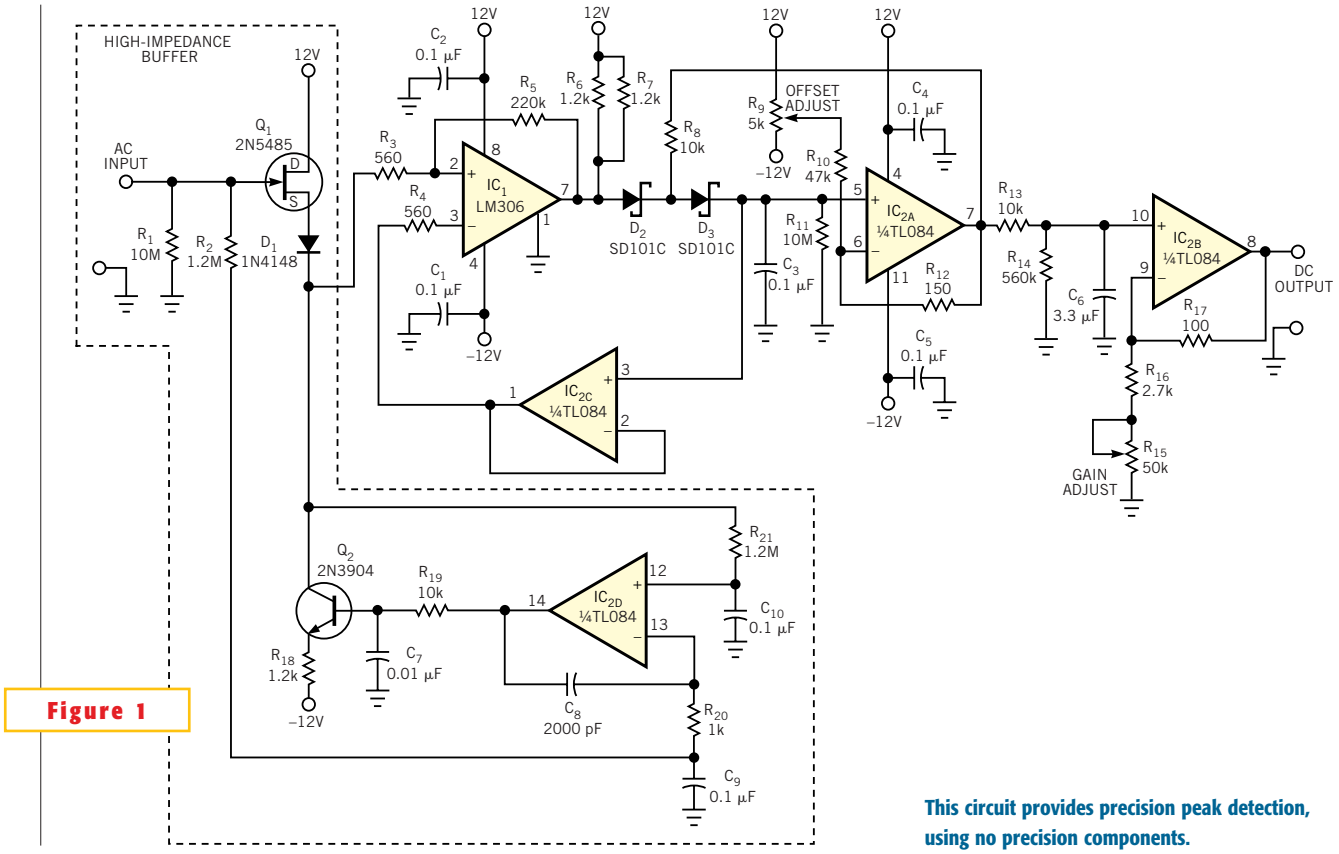


Figure 1

This circuit provides precision peak detection, using no precision components.

also provides reverse bias to D_2 when the output of the comparator is pulled low. The IC_{2A} FET-input op amp has low input-bias current, so it does not discharge C_3 between charging pulses. IC_{2C} buffers the negative input of the comparator for the same reason. The 10-MΩ resistor, R_{11}, provides sufficient discharging of C_3 so that the dc output from IC_{2B} decay to a negligible level in two to three seconds after removal of the ac-input signal.

R_{13} and C_6 filter the dc output to remove most of the noise that the comparator causes. R_{14} provides a small amount of attenuation of the dc output, so that R_{15} can provide approximately ±2% adjustment of the dc output. For best precision, set R_{15} for minimum gain and apply a 500-mV, 10-kHz signal to the input. Adjust R_9 for 500-mV dc output. Then, apply a 4V, 10-kHz signal and adjust R_{14} for 4.010V-dc output. Check and repeat these two adjustments if necessary. If a precision ac source is not available, you can use an accurate dc source and a high-impedance voltmeter for calibrating the circuit. Apply 500-mV dc to the input and adjust R_9 for 499 mV at Pin 10 of IC_2. Then, apply 4V dc to the input and adjust R_{15} for 3.980V output (Pin 8 of IC_2). The maximum peak input voltage is approximately 5V, because the maximum input-voltage specification for the LM306 is ±7V. The accuracy of the circuit decreases when the input peak is higher than 4V. Remember to use a blocking capacitor in series with the input if the signal to be measured includes a dc offset that can cause the peak input voltage to exceed approximately 5V. **Table 1** shows measured results for the circuit. If desired, you can delete R_9, R_{10}, R_{14}, R_{15}, and R_{16} from the circuit and still obtain good performance.□

TABLE 1–MEASURED RESULTS FOR PEAK-DETECTOR CIRCUIT

Frequency (Hz)	**25**	**50**	**100**	**1000**	**10K**	**100K**	**1M**	**2M**	**3M**
% error (500 mV peak input)	2	0.6	0.2	0	1	0.8	−0.5	−3.2	−5.4
% error (1V peak input)	1.8	0.4	0	0.1	0.8	0.7	−1.3	−3	−5.2
% error (2V peak input)	2.1	0.4	0.1	0.3	1.0	1.4	−0.6	−2	−3.8
% error (4V peak input)	2	0.8	0.5	0.5	0.8	0.8	−0.5	−1.8	−3.5

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Edited by Bill Travis

Circuit produces variable numbers of burst pulses

Michael Kornacker, Northrop Grumman Corp, Rolling Meadows, IL

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THE ADD-ON CIRCUIT in **Figure 1** can produce one to 15 burst pulses with the same number of spaces between the bursts at a pulse width (frequency) that an external square-wave generator at the input sets. The add-on circuit produces a variable number of bursts and a variable number of spaces between the bursts by using an external square-wave generator as a source. The project in this design required a TTL burst signal, but resources did not allow for the expense of a burst generator. The circuit basically comprises two hexadecimal, divide-by-16 counters set up so that the counter on the left produces a user-selectable zero to 15 pulses and the counter on the right produces a user-selectable zero to 15 spaces. The two hexadecimal thumbwheel switches select the number of pulses and spaces.

Counter IC_1 controls the number of bursts, and counter IC_2 controls the number of spaces. The two hexadecimal thumbwheel switches, S_1 and S_2, select the count value. Each switch position is numbered zero to 15. S_1 controls the number of burst pulses, zero to 15, and S_2 controls the number of spaces, zero to 15. For either the IC_1 or the IC_2 counter to count, Pin 7 must be high. If Pin 7 is low, then the counter remains disabled. For a counter to be loaded with a desired count, Pin 9 must be low and then high. The carry output at Pin 15 is normally low until the counter reaches a count of 15, and then it goes high. When the circuit is powered on, resistor R_1 and capacitor C_1 form an RC-time-constant power-on-reset circuit at Pin 1. This feature initializes the counters to the zero state upon power-up. After that, the thumbwheel switches set the count value.

When a clock signal arrives at the counters' Pin 2 with the desired frequency, counter IC_1 starts counting up, and counter IC_2 remains in the off-state because the low signal at IC_1's Pin 15 carry output applied to IC_2's Pin 7 disables counter IC_2. When IC_1's count reaches the end (15), it goes high and enables IC_2 to count. IC_1's carry output also goes through inverter gate IC_{3A} and then to the OR gate IC_4's Pin 1. The low signal on one input of IC_4—and the fact that, because IC_2 is now counting, its carry output at Pin 15 is also low at IC_4's Pin 2—means that a low signal appears at IC_1's Pin 7, and thus IC_1 now becomes disabled. Both IC_1 and IC_2 counters' Enable pins are cross-con-

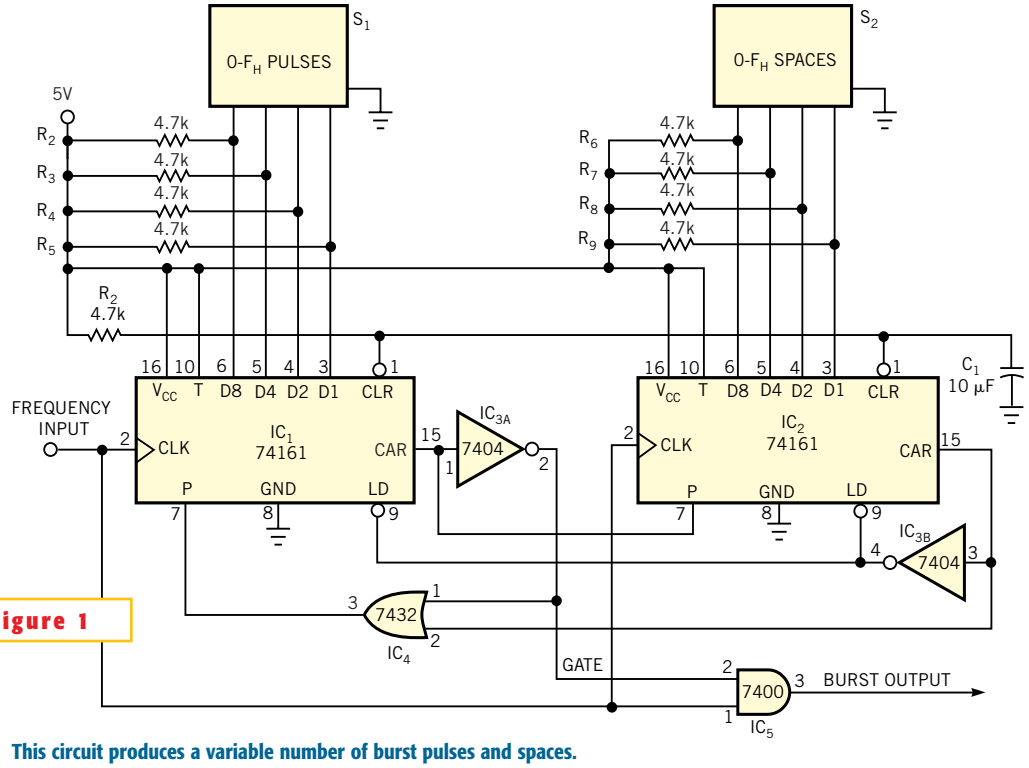


Figure 1

This circuit produces a variable number of burst pulses and spaces.

nected, so that when one counter is counting, the other counter becomes disabled. The two counters work in this way, back and forth, counting up to 15 and enabling and disabling each other. And finally for the two counters, when the carry output on IC_2 goes high, the circuit then, after it reaches a count of 15 through the inverter IC_{3B}, loads a new count or reloads the old count into the counters as set by the thumbwheel switches for the next count.

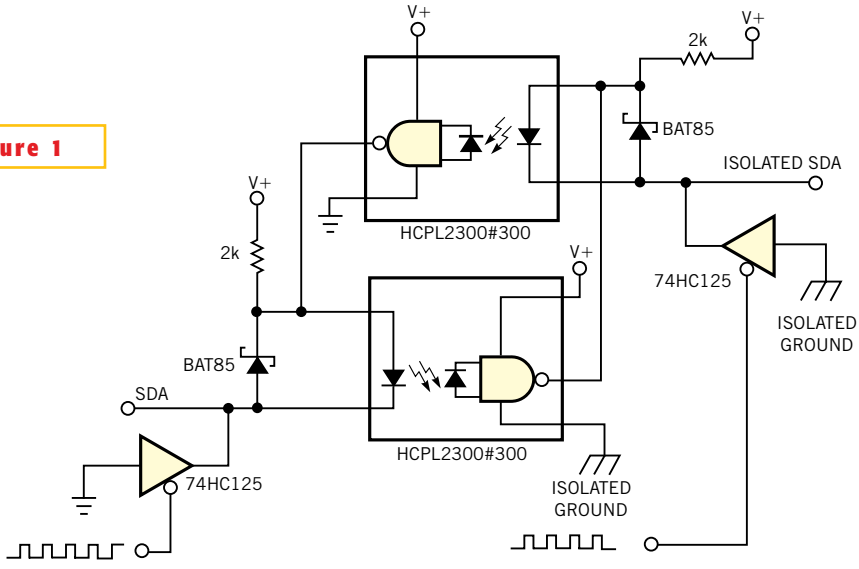
When IC_1 is counting, the output of IC_{3A} (the gate signal), assumes a high level at AND gate IC_5's Pin 2. This state allows the clock signal to pass through IC_5 unimpeded to the output. The output of IC_5 is the burst output. When IC_1 is disabled and IC_2 is counting, the gate signal from IC_{3A} asserts a low signal at IC_5's Pin 2. The output is also low and produces no bursts. You can configure this circuit to produce even more pulses or spaces by simply cascading more counter chips where needed. Also, you can replace switches S_1 and S_2 by an 8-bit write-output register, making the pulse and space counts software-controlled, or you could apply the gate signal to the control input of a CMOS switch to burst analog signals, such as sine waves at its input.□

Method provides fast, glitch-free isolation of I²C and SMBus signals

Mark Thoren, Linear Technology Corp, Milpitas, CA

I²C is a popular serial protocol for power controllers, ADCs and DACs, EEPROMs, and other devices. In certain data-acquisition and power-control situations, you must isolate the I²C master from one or more slave devices for noise, grounding, or safety issues. Also, although 128 peripherals may connect to the bus, at some point, differences in ground potential and excessive bus capacitance begin to erode noise and timing margins. This Design Idea shows how to provide fast, glitch-free optical isolation of I²C or SMBus signals by using a method that meets the requirements for the 400-kHz enhanced-I²C-bus specification. The I²C bus consists of bidirectional clock and data lines (SCL and SDA) that are pulled up with resistors or current sources. Devices connect to the bus with open-collector I/O pins. One way to isolate I²C signals is with a variation of the circuit shown in **Figure 1**, which shows only SDA; SCL operation is identical.

Figure 1



This circuit represents a simple I²C isolator.

The circuit in **Figure 1** works on the principle that a device pulling the nonisolated SDA line low turns on an optocoupler LED, pulling the isolated SDA line low and disabling the isolated side's optocoupler LED and vice versa. However, if devices on both sides of the isolation barrier are pulling their respective SDA lines low, the optocouplers are in an indeterminate state, with both LEDs partially on. When the nonisolated device releases its SDA line, the voltage on the line rises until the isolated side's LED can turn fully on. Only then will the nonisolated SDA line go low again. This situation occurs at various times during I²C communications, including clock synchronization (on the SCL line), multimaster arbitration, and SMBus interrupt arbitration (on the SDA line). **Figure 2** shows details of the operation of the circuit in **Figure 1**. The 74HC125 tristate noninverting buffers simulate the open-drain outputs of two I²C devices. A logic low on the $\overline{EN}$ line forces the output low, and a logic high puts the output in a high-impedance state. Traces 1 and 2 show the inputs to the enable lines of the SDA and isolated-SDA buffers. Traces 3 and 4 show the outputs, respectively.

This type of circuit has been published in a number of forms, often with slow optocouplers that require 5 to 10 mA of LED drive. These circuits may work in a limited set of applications, but they are slow and still produce glitches, and trying to overcome speed and drive issues with high-speed components makes the circuits almost unusable. The

circuit in **Figure 1** uses fast HCPL2300 optocouplers that require only 500 µA of LED drive. If both SDA lines are held low and then released at the same time, the optocouplers fight each other and form an oscillator (**Figure 3**). The characteristics of this oscillation depend on

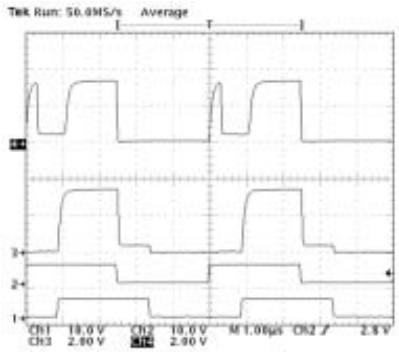


Figure 2 The simple I²C isolator produces large glitches under some circumstances.

pullup resistance, supply voltage, and capacitance on the data lines. (Removing one of the 9-pF scope probes stops the oscillation, and replacing it with a 10-pF capacitor starts it up again.)

The circuit shown in **Figure 4** solves these problems by setting up three logic levels: "high" (pulled up to 5V), "pulling low," and "being pulled low." When both sides are idling high, both optocouplers are off. When one side pulls its line below 0.4V (a safe assumption for both open-collector and open-drain outputs), the comparator turns on its LED. The other side's line pulls down to approximately 0.6V, which is still interpreted as a logic low but does not result in that side's LED turning on. When both sides are pulling their lines low, both LEDs are on. In this state, if one side releases its line, it rises cleanly from the low level of the I²C device's output to approximately 0.6V.

Figure 5 shows details of the operation of the circuit in **Figure 4**. The combination of the LT1719 comparator and Agilent (www.agilent.com) HCPL2300 optoisolator meets the timing requirements of the 400-kHz enhanced I²C-bus specification. Total propagation delay is approximately 100 nsec, and you can adjust the logic thresholds to suit other requirements. Although you can use this circuit for both SDA and SCL lines to support full clock synchronization, the extra circuitry is unnecessary as long as the master never tries to communicate faster than the slowest slave device. If you don't need clock synchronization, you can use a single optocoupler for SCL.□

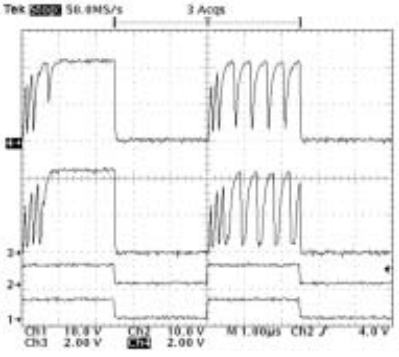


Figure 3 Using high-speed components in Figure 1's circuit causes unpredictable behavior.

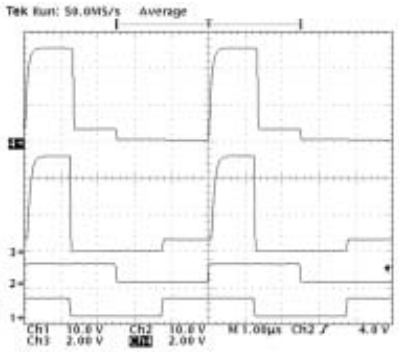


Figure 5 This scope photo shows the operation of the improved I²C isolator.

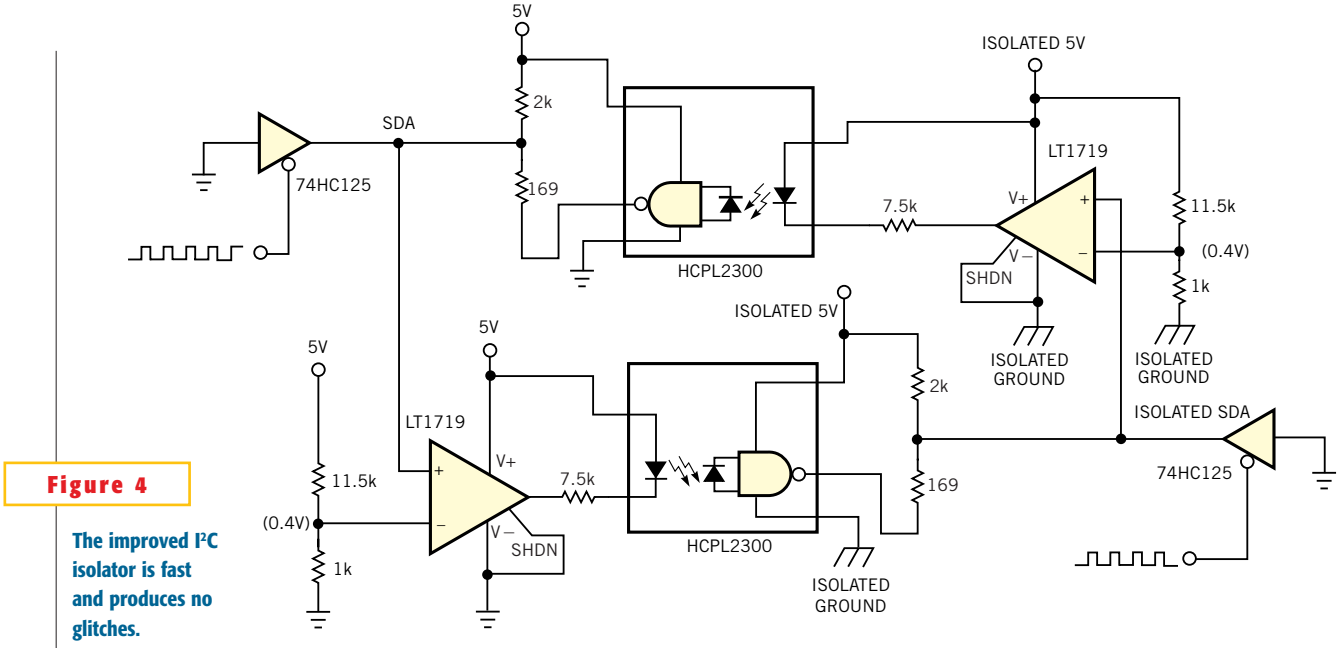


Figure 4 The improved I²C isolator is fast and produces no glitches.

Simulate input-offset current for current mirrors

Johan Bauwelinck, Gent University, Gent, Belgium

Simulating the output-offset current of a current mirror is straightforward. You simply have to apply an input current, measure the output current, and calculate the difference. This output-offset current, however, is not equal to the input-offset current, especially when the circuit is not a 1-to-1 mirror. Simulating the input-offset current with high accuracy is more complicated. Suppose you're dealing with a 1-to-1 mirror and you want to know what input current is needed to obtain an output current of 10 µA. Ideally, the input current would be 10 µA, assuming that the input offset current is zero. However, because of the finite beta of bipolar transistors, finite output impedances, mismatches, and so on, the input offset current is not equal to zero. The design in **Figure 1** provides high accuracy and a low simulation time.

You use feedback to force the current of a CCCS (current-controlled current source) to equal the input-offset current. The current that flows into voltage source V_{OUT} is the difference between the output current of the mirror and the ideal output current. This current is the "error current" (I_{ERROR}). When the CCCS equals the input-offset current, then the error current is zero. The high-gain CCCS amplifies the error current, and the CCCS adds to the input current. In this way, you create a feedback loop, and the current that you measure through the CCCS is the input-offset current. The feedback loop implements a high gain that ensures a high accuracy (negligible error current). And, because you obtain the result by calculating the dc operating point, the simulation time is small.

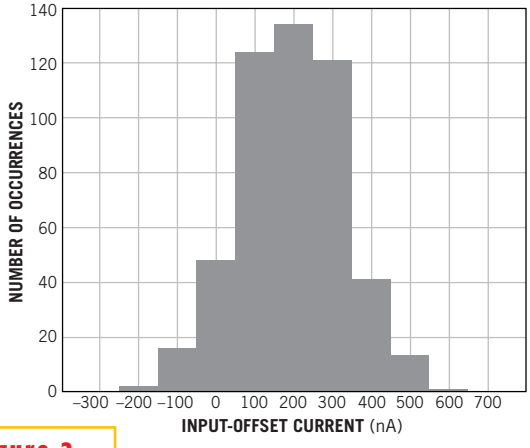


Figure 2 This bar graph shows the input offset-current distribution.

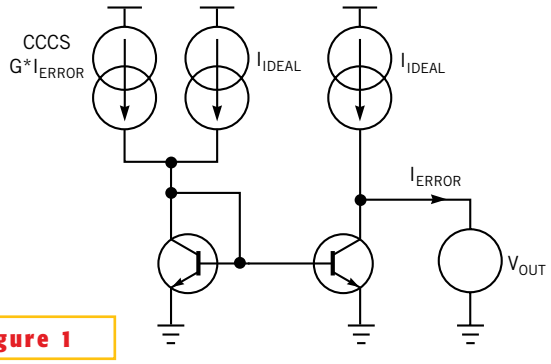


Figure 1 Use this circuit for simulation of current-mirror input-offset currents.

Figure 2 shows simulation results of 500 Monte Carlo runs for I_{IDEAL}=10 µA, gain G=1000, and V_{OUT}=1V. The npn transistors have an emitter length of 40 microns and use a 0.35-micron silicon-germanium BiCMOS process, but you can use the simulation method for all current mirrors and all types of transistors. The average of the distribution in **Figure 2** is 194 nA, and the standard deviation is 131 nA. The average is not zero because of the base-current error.□

Designing high-current chokes is easy

Louis Vlemincq, Belgacom, Evere, Belgium

Somewhat unusually, this Design Idea deals with a formula rather than a circuit. You might think that all the basic formulas of magnetic phenomena were discovered more than a century ago. In fact, they probably were, but, at the time, some were of little practical interest and were essentially disregarded and never included in books or formula tables. I developed the formula describe here because I had to design many inductive components subjected to high peak currents, such as dc filter chokes, ac reactors for resonant converters, and flyback transformers. In such cases, you have to consider two main aspects: One is the current-carrying capacity of the wire, and the other is the peak induction that the core material supports. The first point is well-known and relatively easy to deal with, but the magnetic induction is much more problematic to determine.

The traditional methods of selecting a suitable core size and air gap are generally based on tables or graphical information. Examples of such methods include Hannah curves and energy-storage-capacity graphs. I found these methods cumbersome, inflexible, and almost impossible to automate; hence, I looked for a better approach. I wanted a formula as compact and elegant as the

one that is at the base of a symmetrical converter's design: N=V/(4BFA), where N is the number of turns required to achieve the target induction, V is the voltage applied to the winding in volts, B is the peak magnetic induction in the core material in tesla, F is the frequency of operation in hertz, and A is the effective core area in square meters.

This formula is attractive because you need only essential parameters; you need not mess around with the permeability or the length of the magnetic path, for example. By combining and algebraically manipulating the fundamental equations of the magnetic formula, I arrived at a similarly simple equality applicable to inductors: N=(LI)/(BA), where L is the inductance in henries, and I is the instantaneous peak current in amperes. Here again, you need no more parameters than the bare minimum. Using this formula, a typical design procedure is:

1. Select a core size that seems likely to suit your application (The selection information that the manufacturer provides can be useful.)

2. Use the formula and the core's data sheet to compute the number of turns required for the worst-case situation—in other words, the maximum peak current and magnetic induction below the saturation limit for the whole temperature range.

3. Check that the resulting winding does not exceed the capacity of the coil former; if it does, select the next-higher size.

4. Compute the air gap required to achieve the target inductance using the manufacturer's data or the following formula (approximate):

$$\Delta = \frac{A}{\frac{L}{\mu_0 N^2} - 3k\sqrt{A}},$$

where μ_0 is the permeability of a vacuum ($4\pi\times10^{-7}$), and k is a factor that depends on the implementation of the air gap. For a single air gap, as in a potentiometer core in which the center pillar is machined, k=2. If, instead, you use spacers such as in a U-core, the air gap is split in two, and the factor k=1. If you need high accuracy for the inductance value, you should build a sample to optimize the gap. Also, for small or large gaps, the formula loses its accuracy because it assumes that the magnetic material has a negligible reluctance compared with the air gap. If the gap is small or if the core material has a low permeability, the assumption about negligible reluctance is no longer true. At the other extreme, the first-order term of the formula does not sufficiently compensate for the apparent increase in the core area that fringe fields cause. Thus, discrepancies can exist be-

tween the calculated and the measured values.

The relationship N=(LI)/(BA) can also be useful in a different manner. You may want to reverse-engineer off-the-shelf components to check that they do not risk saturation at the intended peak current. (In converter circuits, the peak current can be much higher than the rms current.) To do this reverse-engineering, you can use the form B=(LI)/(NA). For most general-purpose ferrites, a peak induction of 0.2 to 0.25 tesla is acceptable, whereas materials for power applications can tolerate more than 0.4 tesla. Metal-powder cores accept inductions as high as 1 tesla. If you want to know what maximum current is acceptable for a component, then the following form is convenient: I=(BNA)/L. At first sight, this formula looks counterintuitive or even erroneous, because it seems to imply that you can increase the current for a given induction if you also increase the number of turns. How can this situation be?

Increasing the current or the number of turns results in an increase in ampere-turns that the core sees, which should also increase the induction. The key to understanding this apparent paradox is to take into account what the formula implies: If L has to remain constant with more turns, the air gap must be wider to reduce the apparent permeability (μ) of the core, resulting in a greater current capacity, although the air gap appears nowhere in the formula. The paradox may explain why hardly anyone ever mentions this family of formulas. If you try to superficially make sense of the implications of the formulas, you have to conclude that there must be a mistake somewhere.

You can also apply the results to open-circuit magnetic components, such as cylindrical coils wound on a rod of magnetic material. In this case, the air gap becomes almost as large as the core, yielding two implications: Because the surrounding vacuum or air contributes as much as the core itself to the inductance, you can double the core area the formula uses with respect to the physical value, and, even when saturation does occur, the effect is much less brutal than in a closed magnetic circuit. Second, the simplified inductance formula is no longer valid.

To conclude, the user-friendly versions of the formulas, expressed in more convenient units are: N=0.01(LI)/(BA), with L in microhenries, I in amperes, B in tesla, and A in square centimeters.

And the user-friendly expression for the air gap is

$$\Delta = \frac{A}{7.96\frac{L}{N^2} - 0.3k\sqrt{A}},$$

where Δ is in millimeters, A is in square centimeters, and L is in microhenries.□

Edited by Bill Travis

Build a transformerless 12V-to-180V dc/dc converter

Francis Rodes, ENSEIRB/IXL, Talence, France

Some transducers for portable or automotive applications need accurately regulated, high-voltage bias and draw little current. To produce such high voltages from a low battery voltage, designers typically use switch-mode dc/dc converters—generally, flyback converters. These converters exhibit high efficiency at medium or high output power. However, for the low output power for biasing some transducers, the fixed amount of power the power-switch driver and the regulator circuitry require can have a detrimental effect on efficiency. Furthermore, the associated transformer is rarely available off the shelf, so it requires a custom-design effort. This effort can account for 70% of the entire design time.

The circuit in **Figure 1** overcomes the transformer-related problem, thanks to a transformerless, switched-capacitor topology that requires only off-the-shelf components. You can describe the operating principles of the circuit by first considering the behavior of a single switched-capacitor cell and then extending the concept to an N-cell voltage multiplier. **Figure 2** represents the equivalent circuit of the first switched-capacitor cell.

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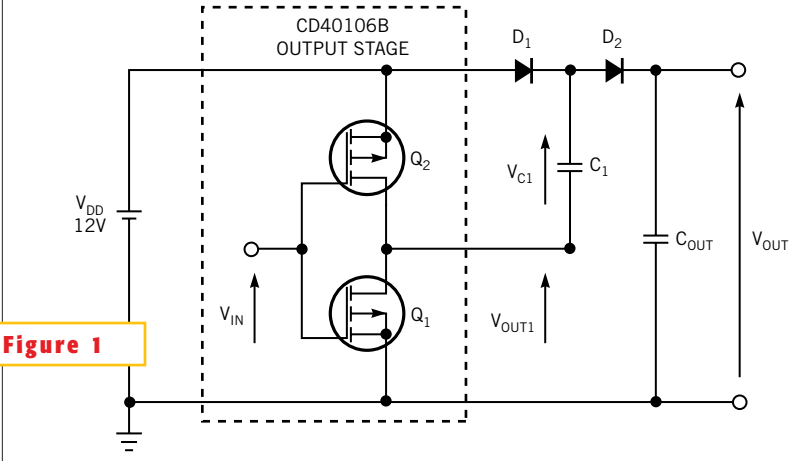

Figure 1

This four-IC circuit uses no transformers and converts 12V to 180V, using off-the-shelf components.

The two complementary MOSFETs, Q_1 and Q_2, mounted in a push-pull configuration, represent the output stage of one CD40106 Schmitt-trigger inverter. The input signal, V_{IN}, drives the push-pull stage, producing a 0 to 12V square wave at 150 kHz. If you assume that V_{IN} is 12V during the first half-period, then Q_1 is on, and Q_2 is off. Consequently, D_1 is forward-biased, and C_1 charges positively to $V_{C1}=V_{DD}-V_D$, where V_D is D_1's forward-voltage drop (0.7V). Meanwhile, D_2 is forward-biased, and C_{OUT} charges to $V_{OUT}=V_{DD}-2V_D$. During the second half-period, the states reverse: V_{IN} is 0V, Q_1 is off, and Q_2 is on, thus connecting the negative terminal of C_1 to the supply voltage. This action forces the positive terminal of C_1 to elevate itself to a voltage higher than the supply voltage, V_{DD}. D_1 now becomes reverse-biased and allows C_2 to charge up again through D_2. If you assume that C_{OUT}'s value is considerably lower than the value of C_1, then you can calculate that V_{OUT} attains the value $V_{OUT}=V_{OUT1}+V_{C1}=2(V_{DD}-V_D)$. Thus, assuming $V_{DD}>>V_D$, you can see that the circuit in **Figure 2** acts as a voltage-doubler cell.

If you cascade N voltage-doubler cells in the chainlike structure of **Figure 1**, an extension of the voltage-doubler principle yields $V_{OUT}=(N+1)(V_{DD}-V_D)$. From this equation, you can determine the number, N, of inverters you need to produce a given high output voltage:

$$N=\frac{V_{OUT}}{V_{DD}-V_D}-1.$$

To produce 180V output voltage from a 12V lead-acid battery, which can fluctuate from 11 to 13.5V, an application of the equation with worst-case V_{DD} of 11V yields

$$N=\frac{180}{11-0.7}-1=17.47\approx 18.$$

So, your design requires three CD40106 hex Schmitt-trigger inverters, as **Figure 1** shows. An inspection of the equation $V_{OUT}=(N+1)(V_{DD}-V_D)$ reveals that the 11 to 13.5V fluctuation of the lead-acid battery produces a proportional 195 to 243V output-voltage fluc-

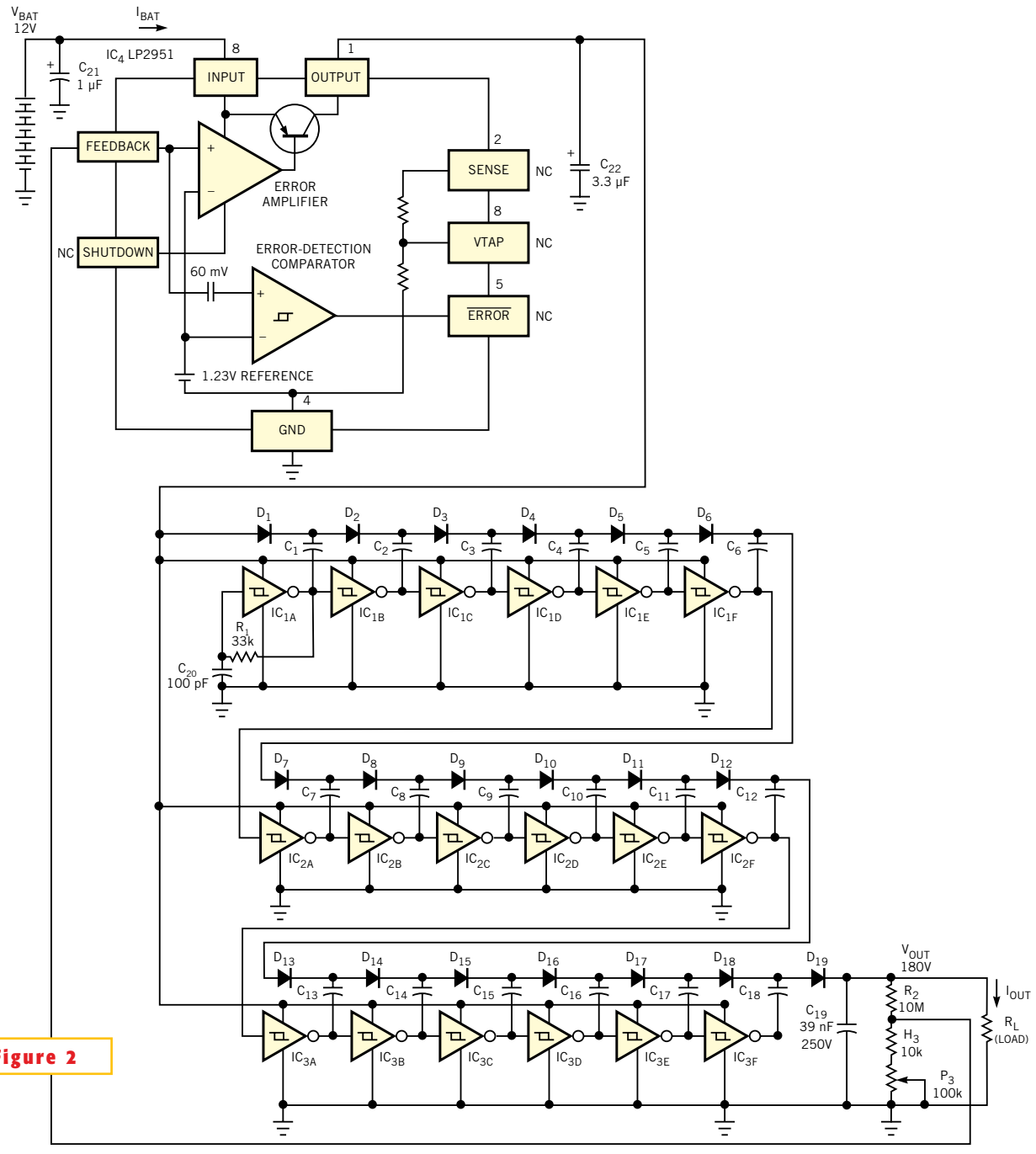

Figure 2

NOTES:
C_1 TO C_{18}: 33 TO 100 nF (63V).
D_1 TO D_{19}: 1N4148 OR EQUIVALENT.
IC_1 TO IC_3: CD 40106B.
IC_4: LP2951 (NATIONAL SEMICONDUCTOR).

This circuit illustrates the operating principle of the basic voltage-doubler cell.

tuation. This variation is unacceptable for biasing applications requiring accuracy. The obvious solution to this problem is to regulate the output voltage, V_{OUT}. You could use either of two regulation techniques: Connect a high-voltage regulator directly to the output terminal, V_{OUT}, or control the low-supply voltage, V_{DD}, of the CMOS inverters to indirectly regulate the output voltage, V_{OUT}. Because of the high cost and low efficiency of linear high-voltage regulators, the circuit in **Figure 1** uses the second regulation technique.

The key element of the feedback loop

is the low-cost, low-dropout regulator, IC_4, the LP2951 from National Semiconductor (www.national.com). The output of this regulator produces the variable-supply voltage, V_{DD}, to the 16 Schmitt-trigger inverters (IC_1 to IC_3). With this arrangement, IC_4 has to deal with input voltages ranging from only 11 to 13.5V. The output voltage, V_{OUT}, feeds back to IC_4's error amplifier via the resistive divider, R_2, R_3, and P_3. IC_{1A}, the first multiplier cell, produces the square waveform that the 18-cell, switched-capacitor voltage multiplier needs. Using the feedback network (R_1, C_1), this Schmitt-trigger inverter constitutes a free-running oscillator that produces a 150-kHz square waveform at its output. **Tables 1** and **2** show the measured electrical characteristics of the regulated 12-to-180V dc/dc converter. The input-regulation characteristic in **Table 1** proves that the output voltage does not fluctuate significantly for battery voltages ranging from 11 to 14V. From the output-regulation characteristic in **Table 2**, you can see that the overall power efficiency attains 61%, the maximum output current reaches 1 mA, and the peak-to-peak output ripple voltage does not exceed 0.2V.□

TABLE 1–INPUT REGULATION AT I_{OUT}=20 µA

V_{BAT} (V)	V_{OUT} (V)
11	180.3
12	180.3
13	180.3
14	180.3

TABLE 2–OUTPUT REGULATION AND EFFICIENCY AT V_{BAT}=12V

I_{OUT} (mA)	V_{OUT} (V)	Ripple p-p (V)	I_{BAT} (mA)	Efficiency (%)
0	180.3	0.08	3.4	NA
200	180.6	0.1	7.6	40
400	180.7	0.1	11.7	52
800	180.2	0.15	19.8	61
1000	179	0.2	25	60

Build a simple one-chip phototimer

Abel Raynus, Armatron International, Malden, MA

RECENTLY, I NEEDED to automatically switch on a lamp when it became dark and keep it on for a given time. Trying not to reinvent the wheel, I looked through what was available on the market, but I could not find an inexpensive device that satisfied the requirement. Some products worked like a photoswitch, lighting a lamp when it becomes dark and keeping it on while it is dark—in other words, the whole night. Others were designed as timers to turn a load on and off at a given time and had no correlation with darkness. These devices had more functions than I needed, and they were rather expensive. As a result, I had to design the phototimer from scratch, and it turned out to be simple and inexpensive. The phototimer (**Figure 1**) is based on the low-end, eight-pin flash microcontroller MC68HC908QT2 from Motorola (www.motorola.com).

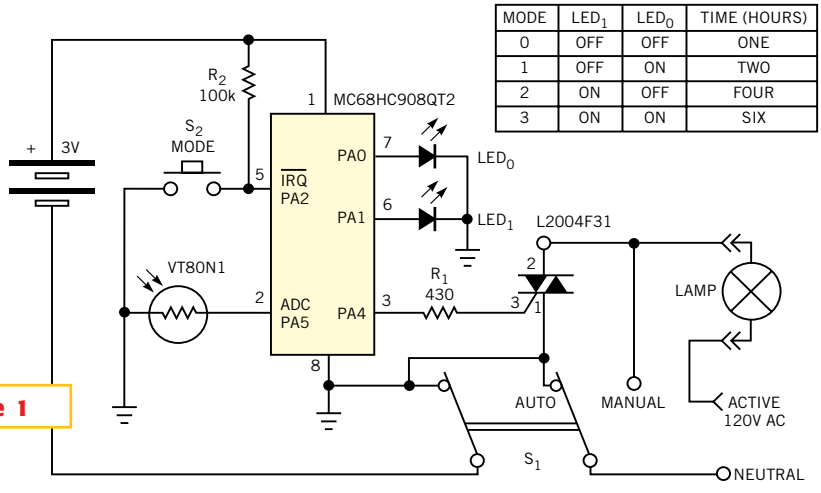

Figure 1 This simple phototimer allows you to program the switch-on time after darkness falls.

When switch S_1 is in the Manual position, the microcontroller disconnects from the battery, and the lamp immediately switches on. When this switch is in the Auto position, the microcontroller waits until it becomes dark and, after that, switches the lamp on for a predetermined time that the designer chooses. This project has time settings for one hour and two, four, and six hours. During initialization, the timer sets the one-hour delay as the default. You set the other delays by the pushbutton mode, switch S_2. LED_0 and LED_1 indicate the prevailing mode. After the delay time, the microcontroller switches the lamp off and waits for the next night to automatically repeat the process.

An advantage of the MC68HC908QT2 is that it generates the time delay with its internal oscillator (12.8 MHz with 5% tolerance), meaning that you need not use RC timing circuitry and struggle with component tolerances. I took some additional steps to simplify the design. The microcontroller's PA5 input has an internal, 30-kΩ pullup resistor, so there is no need for an external resistor for the photocell. The LTL-4231T-R1 LEDs from LiteOn (www.liteon.com) come with built-in in resistors. You could also eliminate resistor R_2, but, in this case, Mode1 would be the start-up default mode. The Teccor (www.teccor.com) L2004F31 logic triac needs 3-mA gate current from the microcontroller, and it can deliver 4A load current. **Listing 1** is the C program for controlling the phototimer. You can download the routine from the Web version of this Design Idea at www.edn.com.

You can also modify the timer. You can easily add time-delay modes making software changes plus adding indicating LEDs; available microcontroller pins lim-

it the number of LEDs you can add. For more advanced projects, you can even use a seven-segment display, either directly or via a decoder, for time indication. You can eliminate the Auto/Manual switch by modifying Mode 0, for, example, as a continuous mode to light the lamp just after power-up, without waiting for night. You can use any type of microcontroller in the project. For example, using the 16-pin microcontroller MC68HC908QY2 from the same Motorola family allows you to increase the number of bidirectional I/O lines to 13. Also, instead of the photocell, you could use a different kind of sensor— temperature, pressure, or motion, for example—to activate the time delay.□

Solenoid trip circuit works at battery's end of life

Brad Peeters, Theta Engineering, Costa Mesa, CA

This Design Idea involves a low-power motion-detector circuit that operates from battery power for extended times. Part of the design includes a solenoid-operated trip mechanism that triggers whenever it detects motion. The drive circuit for the solenoid in the original design worked fine as long as the battery was fresh but failed as the battery got into the middle of its life, even though sufficient energy remained in the battery to operate the solenoid. The culprit was the battery's internal resistance. The internal resistance of a standard alkaline cell increases as the cell's life accumulates, whereas the cell's open-circuit voltage hardly changes. This increased resistance causes a sharp drop in supply voltage whenever the drive circuit attempts to energize the solenoid. This drop upsets the drive circuit, preventing reliable operation.

The original design solved this problem by using a large electrolytic capacitor across the battery supply. This capacitor functioned as an energy reservoir and prevented the supply voltage from sagging so dramatically, allowing the device to continue functioning much further into the battery's life. However, the electrolytic was bulky and expensive, and presented an awkward packaging problem.

The circuit in **Figure1** solves the problem by incorporating feedback in such a way that any drop in supply voltage only turns on the drive circuit harder. In testing, this circuit functioned even when the nominally 6V battery sags as low as 2V. Q_1 is a 3A, high-beta, low-saturation-voltage pnp transistor that drives the solenoid. To energize the solenoid, Q_1 has to turn on hard to minimize voltage drop and get the most from the battery's life. The circuit achieves the full turn-on by using three sections of an LP339 quad comparator in parallel. The LP339 is similar to the venerable LM339 but with lower power consumption, making it more suitable for battery-powered applications. Interestingly enough, it also has higher output drive. The three parallel devices provide approximately 200 mA to the base of Q_1, sufficient for Q_1 to supply 2A to the solenoid and remain well-saturated. The design requires no current-limiting resistor in series with the base of Q_1 because the outputs of the LP339 are naturally current-limited to approximately 60 or 70 mA each.

Once the trip mechanism triggers, S_1 opens, removing all power from the circuit. The device remains in this state until you manually reset the trip mechanism. An entire trip event takes only about 10 msec, thus conserving the battery and preventing excessive power dissipation in Q_1 and the LP339. The remaining section of the LP339 implements a single-section window comparator. A window comparator is necessary because motion detectors are commonly ac-coupled circuits. You must apply the detection threshold equally to positive or negative excursions. In other words, any excursion outside the window should trigger detection. In a quiescent state with no input signal, the network comprising R_3, R_5, and dual-diode D_2

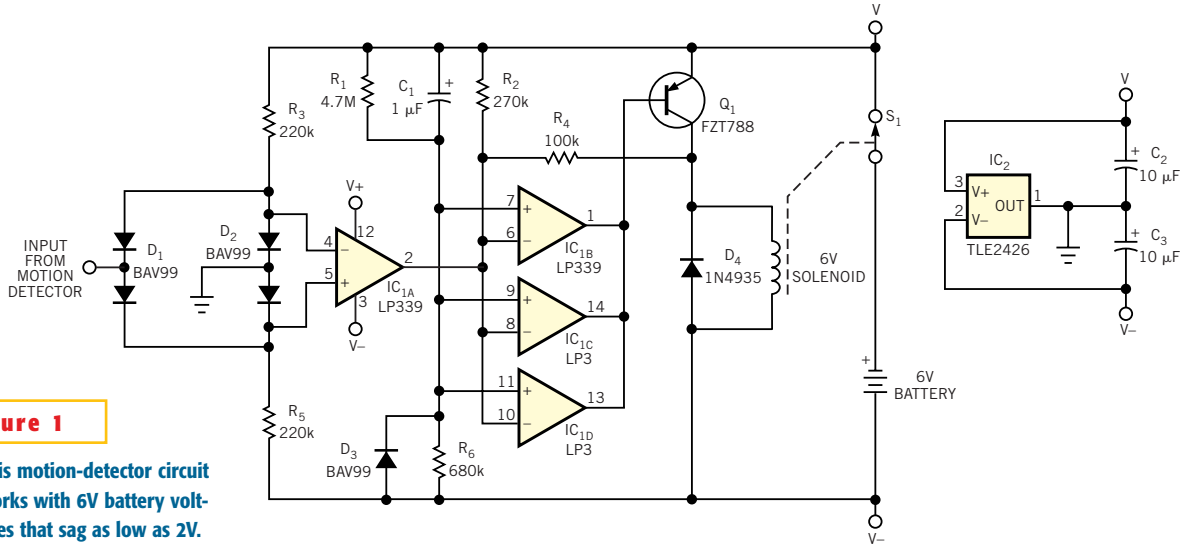

Figure 1

This motion-detector circuit works with 6V battery voltages that sag as low as 2V.

keeps the negative input of IC_{1A} one diode drop above ground and the positive input one diode drop below ground. This level keeps IC_{1A}'s output and, hence, the negative inputs of IC_{1B}, IC_{1C}, and IC_{1D}, low. Because R_1 and R_6 bias the positive input of IC_{1B}, IC_{1C}, and IC_{1D} at approximately 0.75V, the comparators' outputs remain off.

The circuit trips if the input goes more than two diode drops above or below ground. For example, if the circuit's input goes below ground, the negative input of IC_{1A} pulls down until it is lower than the positive input. If the input goes up, the positive input of IC_{1A} pulls up until it is higher than the negative input. Either case results in the output of IC_{1A}'s going high. This action in turn causes the IC_{1B}, IC_{1C}, and IC_{1D} outputs to turn on, turning on Q_1 and energizing the solenoid. R_4 provides positive feedback. If Q_1 even starts to turn on, the partial turn-on causes IC_{1B}, IC_{1C}, and IC_{1D} to turn on more, precipitating a latch-up to ensure that Q_1 turns on all the way. Thus, all possible battery energy is delivered to the solenoid. C_1 provides further positive feedback when the supply sags. D_3 protects the LP339's inputs from being driven more than a diode drop below ground when the power-supply sag is severe.

A beneficial side effect of the time constant formed by C_1 and R_6 is to prevent false triggers on start-up by holding off the IC_{1B}, IC_{1C}, and IC_{1D} stage until the motion detector has had time to stabilize. IC_2 is a "ground-generator" chip, used to create a circuit ground midway between the supply rails. In contrast to the original circuit, everything in this circuit is going in the proper direction to ensure positive actuation of the solenoid once it reaches a trip threshold. The circuit uses only common, low-cost, and small components. The circuit offers full usage of battery life and needs no bulky energy-reservoir capacitor.□

Servo loop improves linear-regulator efficiency

Aurel Gontean, Technical University, Timisoara, Romania

Linear regulators are easy to implement and have better noise and drift characteristics than switching approaches. Their largest disadvantage is inefficiency: excess energy dissipated as heat. Several well-known techniques are available to minimize the input-to-output voltage across a linear regulator. I had been looking for an inexpensive, easy-to-implement, and efficient preregulator to reduce the dropout voltage of a linear regulator. Closed-loop, self-oscillating preregulators built around a switching transistor, a comparator, and a filter are difficult to predict in terms of frequency. Thus, the power-mains input filter is also difficult to implement. The best option is a fixed-frequency preregulator combined with a linear, low-dropout regulator. The arrangement shown in **Figure 1** fulfills all the requirements. The LM2576T-ADJ, IC_1, switcher uses a 52-kHz fixed frequency. The LT1085, IC_2, is a good choice for the linear regulator. The preregulator feedback loop uses an operational amplifier, IC_3.

When the servo loop is closed, the feedback voltage for IC_1 is:

$$V_{FB} = V_A \frac{R_3}{R_3 + R_4}\left[1 + \frac{R_5}{R_6}\right] - V_{OUT}\frac{R_5}{R_6}. \quad (1)$$

If $R_3 = R_5$ and $R_4 = R_6 = kR_3$, **Equation 1** becomes:

$$V_{FB} = V_A \frac{R_3}{R_3 + kR_3}\left[1 + \frac{R_3}{kR_3}\right] - V_{OUT}\frac{R_3}{kR_3} = \frac{V_A - V_{OUT}}{k}. \quad (2)$$

Equation 2 yields the relationship $V_A - V_{OUT} = V_{DROPOUT} = kV_{FB}$. You can set the dropout voltage according to the linear-regulator requirements. If you select an LT1085, maximum $V_{DROPOUT}$ is 1.5V; for the LM2576T, $V_{FB} = 1.23V$ and if $k = 1.5$, $V_{DROPOUT} = 1.89V$, slightly higher than the value in the data sheet. The dropout voltage is the same regardless of the output voltage and thus ensures reasonable efficiency. (The overall efficiency is greater than 56% for $V_{OUT} = 5V$ at 3A and at least 72% for $V_{OUT} = 30V$ at 3A.) The output voltage, V_{OUT}, ranges from 0 to 30V, and V_{IN} must be at least 5V greater than the maximum V_{OUT}. IC_3 has no special requirements, and IC_2 may be any kind of linear regulator. C_6 reduces the output ripple, and C_2 filters some of the 52-kHz noise on the control line coming from IC_3. The result is a simple, robust, and high-performance laboratory power supply that can supply 3A in a 0 to 30V output-voltage range, using only a small heat sink.□

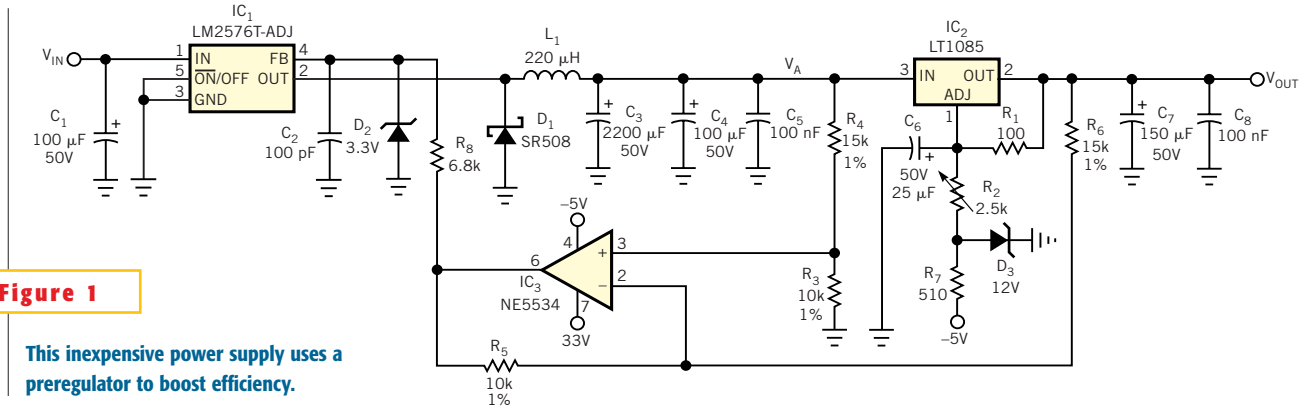

Figure 1

This inexpensive power supply uses a preregulator to boost efficiency.

Boole helps simplify wiring and save money

Jean-Bernard Guiot, Mulhouse, France

To safely observe the positions of two cylinders, you need two signals: one circuit, X, which is open only when both cylinders are in a safe position (two normally closed switches in parallel), and one circuit, Y, which is closed only when both cylinders are in a safe position (two normally open switches in series, **Figure 1**).

This redundancy enables the detection of errors, such as a short circuit within a cable. The Boolean-logic equations of these two circuits are $X=\overline{A}+\overline{B}$, and $Y=A\cdot B$. The problem is that most small limit switches are SPDT (single-pole, double-throw) switches, with which you cannot configure the circuit of **Figure 1**. Using Boolean arithmetic, you can derive $X=\overline{A}+\overline{B}=\overline{A}+A\overline{B}$, which corresponds to the schematic in **Figure 2**. You can easily make a circuit equivalent to that of **Figure 2** using two ordinary SPDT limit switches (**Figure 3**).□

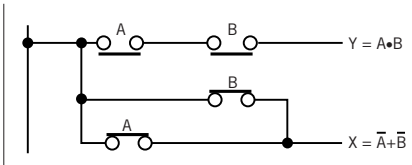

Figure 1 This circuit offers redundancy in machine-control applications.

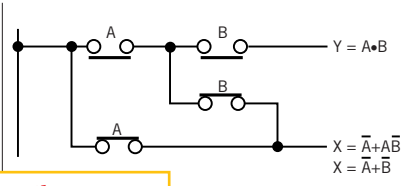

Figure 2 Boolean arithmetic proves that this circuit is equivalent to that of Figure 1.

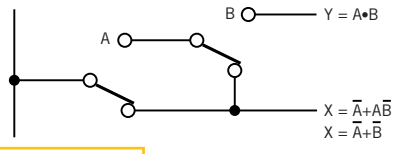

Figure 3 Further simplification yields this circuit, which uses only two SPDT switches.

Edited by Bill Travis

High-side current monitor operates at high voltage

Greg Sutterlin and Brian Whitaker, Maxim Integrated Products, Sunnyvale, CA

THE SIMPLEST technique for measuring current in an actuator or a motor is to monitor the ground current with a resistive element between the load and the ground. Because the device and its associated electronics share a ground potential, you need to amplify only the ground-current signal. This approach, however, does not detect device short circuits to ground, which can overload the high-side drive circuitry. To avoid such potential fault conditions, you should use a high-side current monitor to detect short circuits and similar faults that can occur following the current monitor. High-side current monitoring has advantages, but it finds limited use because of the dearth of devices able to handle the high voltage levels—24V to many hundreds of volts—prevalent in the industry. Off-the-shelf devices can operate to 32 and 76V, but even 76V is insufficient for many applications. **Figure 1** shows a simple way to adapt a standard 32V device for use at any voltage level, subject to limitations of the external components. (The components in **Figure 1** can accommodate 130V.)

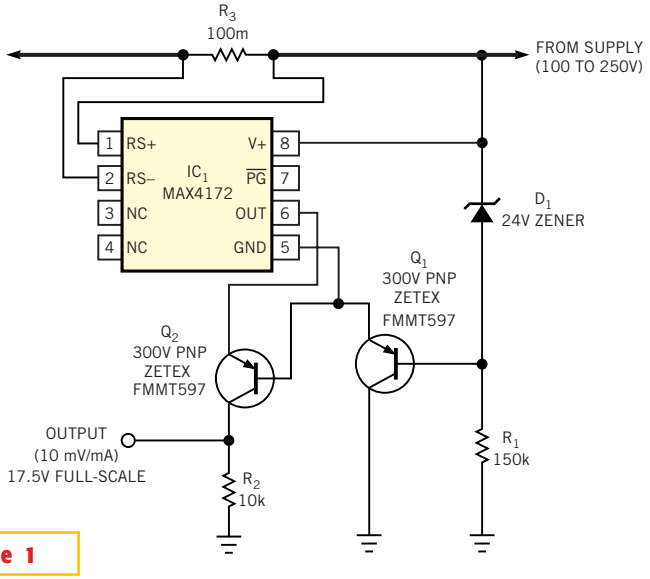

Figure 1

This circuit enables a 36V current-monitoring IC to operate at common-mode voltages as high as 130V.

The accuracy of the circuit is better than 1% for load currents greater than 30 mA. IC_1's current-output stage allows easy implementation of the current mirror needed for level-shifting the output signal to ground. Thus, you can easily monitor the ground-referenced signal by using an A/D converter or a comparator. The circuit monitors load current in the presence of a 130V-dc common-mode level. You must ensure that you do not violate IC_1's absolute maximum rating—36V with respect to the ground pin—for the RS+, RS−, and V+ pins. For that purpose, zener diode D_1 limits the voltages between the V+, RS+, and GND pins to 24V. Thus, the typical voltage between these pins is 24V minus the V_{BE} of Q_1, or 23.3V. The zener-diode current for this circuit is approximately 700 µA. Note that the manufacturer's suggested bias current is 500 µA, but the zener diode's di/dt slope goes *negative* below 300 µA, a condition that can introduce noise or even oscillation. The minimum specified bias—300 to 500 µA—sets the maximum value of R_1, and the maximum allowed power dissipation for R_1 and D_1 combined sets the minimum value for R_1. Thus, for supply rails of 100 to 250V, a reasonable R_1 value is 150 to 225 kΩ—150 kΩ in this case.

Q_1 and R_1 form a shunt regulator. The design uses Q_1 because of its maximum V_{CE} rating of −300V, high gain of 100V/V at 1 mA, and its ability to handle 500 mW of power. Output current is proportional to the voltage difference, V_{SENSE}, between RS+ and RS−: $I_{OUT}=g_m \times V_{SENSE}$, where $V_{SENSE}=R_{SENSE} \times I_{LOAD}$. Transconductance for IC_1 is 10 mA/V. If the maximum monitored load current, I_{LOAD}, is 4A, and R_{SENSE} is10 mΩ, then the maximum I_{OUT} is 10 mA/V×10 mΩ×4A=400 µA. Thus, I_{OUT} is proportional to I_{LOAD}, and the maximum expected output is 400 µA. For applications of wide dynamic range in which V_{SENSE} can approach the absolute maximum rating of the differential pair, 700 mV, you should protect the sense pins by adding series resistors between R_{SENSE} and RS+ and between R_{SENSE} and RS−. You should select the resistor values to limit input currents to within 10 mA when the RS+ to RS− difference is 700 mV.

I_{OUT} is now proportional to I_{LOAD}, but, for easy monitoring, you must level-shift it to ground by using the Q_1-Q_2

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current mirror. Q_2's high gain forces the collector current to closely approximate the emitter current which, when you apply it to R_2, produces a measurable voltage at V_{OUT}. As with Q_1, Q_2 needs a maximum V_{CE} rating of −240V. The device in **Figure 1** is rated at −300V. V_{OUT} now equals $I_{OUT} \times R_2$. (The actual output current at Q_2's collector is slightly less, because of Q_2's base current.) At I_{LOAD}=4A, V_{OUT}=400 μA×10 kΩ=4V. You can accommodate designs with lower or higher operating voltages by properly selecting Q_1, Q_2, and the base resistor, R_1.□

Digital potentiometers enable programmable biquadratic filter

Deborah Mancuso and Donald Schelle, Maxim Integrated Products, Sunnyvale, CA

Of the many types of analog filters available to designers, few allow easy adjustments of the filter parameters. The biquadratic, or biquad, filter is an exception, however. You can change that filter's corner frequency (ω_0), Q, and gain (H) by adjusting the values of three resistors. For that purpose, the lowpass biquad circuit of **Figure 1** includes three digital potentiometers configured as variable resistors in the feedback loops. Altering the settings of these potentiometers changes the filter characteristics. The circuit produces corner frequencies of 5.5 to 55 kHz; Q values of 0.055 to 5.5, depending on the selected corner frequency; and gain of 1 to 100, also depending on the selected corner frequency. To tune the biquad filter, you set a corner fre-

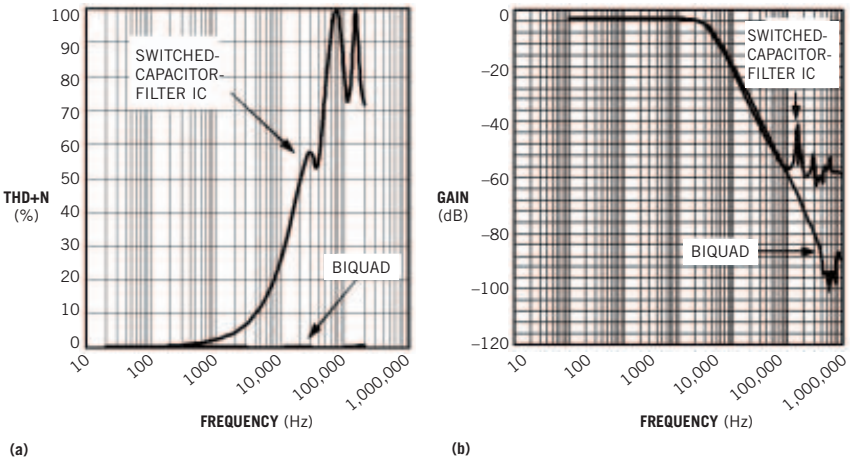
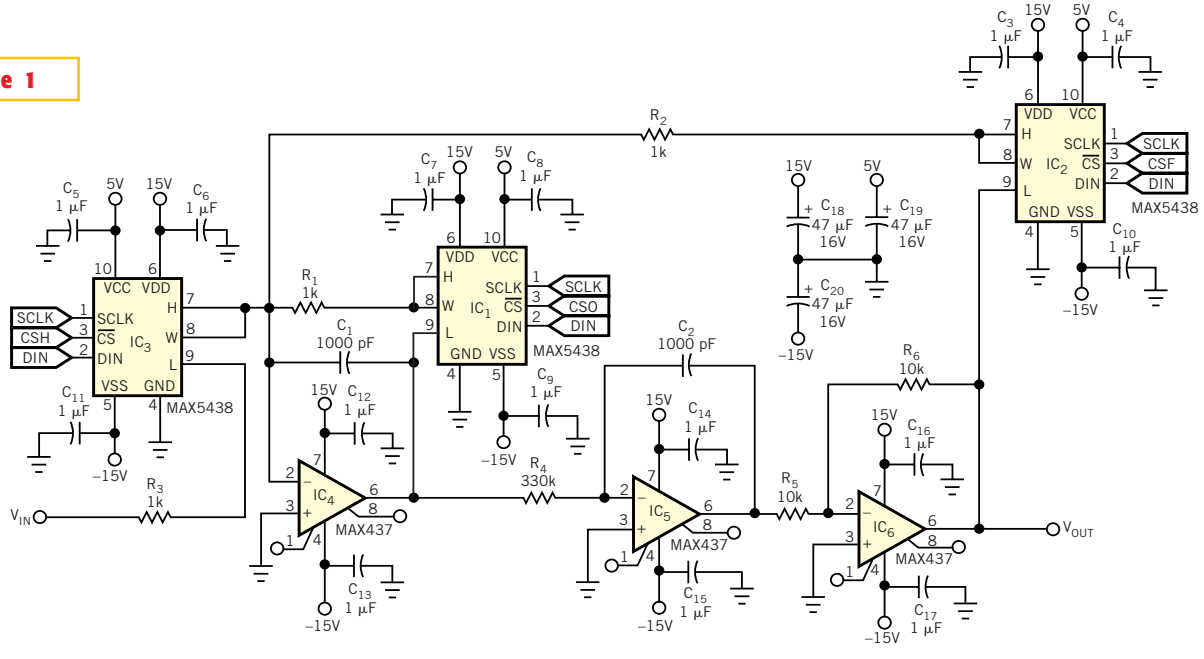


Figure 2 Noise (a) and low bandwidth (b) plague switched-capacitor filters. The biquad filter of Figure 1 maintains less than 1% THD+N over the range 20 Hz to 200 kHz.

Figure 1



Digital potentiometers adjust the corner frequency, Q, and gain for this biquad analog filter.

quency ω_0 in radians per second by adjusting digital potentiometer IC_2 via the SPI interface. In the same fashion, set Q by adjusting IC_1 and gain by adjusting IC_3.

Note that adjusting Q does not affect the corner-frequency setting, and a gain adjustment does not affect the settings of Q or the corner frequency. The three **equations** below demonstrate this orthogonal tuning for the biquad filter:

$$\omega_0^2 = \frac{1}{(R_2 + R_{IC2})R_4C_1C_2}.$$

$$Q = \sqrt{\frac{(R_1 + R_{IC1})^2 C_1}{(R_2 + R_{IC2})R_4C_2}}.$$

$$H = \frac{R_2 + R_{IC2}}{R_3 + R_{IC3}},$$

where R_{IC1}, R_{IC2}, and R_{IC3} are the input resistances of IC_1, IC_2, and IC_3, respectively. The circuit in **Figure 1** is substantially more complex than the switched-capacitor approach usually integrated into an IC, but the switching noise and low bandwidth of a switched-capacitor filter are unacceptable in many applications (**Figure 2**). A biquad filter offers better frequency and noise performance in exchange for more pc-board real estate. And, because monolithic switched-capacitor filters are usually expensive, the biquad circuit of **Figure 1** may be a cost-competitive solution. Many filter applications require higher supply voltages, bipolar operation, or both, so the single 5V supply associated with most switched-capacitor filters may be inadequate for a given application. You can implement ±15V voltage rails using digital potentiometers and high-voltage op amps, such as the MAX5438 and MAX437. The biquad filter is not limited to the lowpass response. You can implement highpass, bandpass, bandstop, and allpass filters by adding a fourth op amp to selected terminals of the original lowpass design (**Figure 3**).□

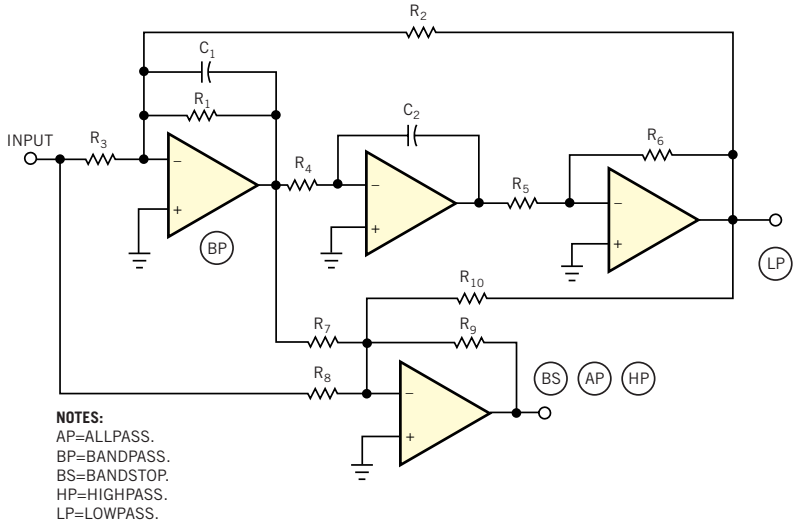


Figure 3 The standard biquad filter circuit produces lowpass and bandpass responses, and the addition of a fourth op amp produces a highpass response. Removing R_{10} and adjusting various component values produce a notch or bandstop response or an allpass response.

High-current supply uses standard three-terminal regulator

I Hakki Cavdar, Karadeniz Technical University, Trabzon, Turkey

Voltage-regulator design for high output currents can be a critical and difficult task. Although voltage regulators with 1A maximum output current are simple to design, thanks to 78xx three-terminal voltage regulators, at output currents higher than 1A output, problems arise. For high output currents, voltage regulators usually use parallel-connected power transistors. The design of the operating points of these power transistors is a difficult task, because the transistors need critical power resistances at the collector and the emitter to set the dc operating point. Both the power transistors and the power resistors dissipate high power, so the design needs heat-sinking. This Design Idea implements a simple voltage regulator that delivers high output current. The basic idea is to parallel-connect multiple three-terminal regulators. These 78xx regulators each handle 1A and are available in 5, 6, 8, 9, 10,12, 15, 18, and 24V versions. In **Figure 1**, two 7812 regulators are connected in parallel.

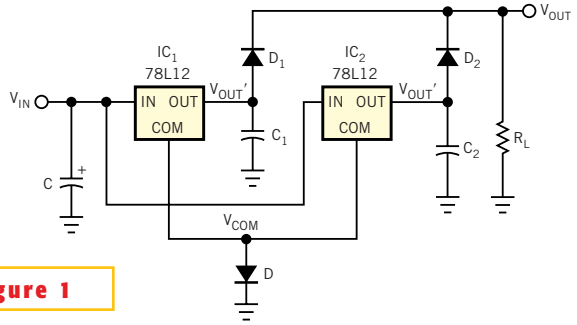
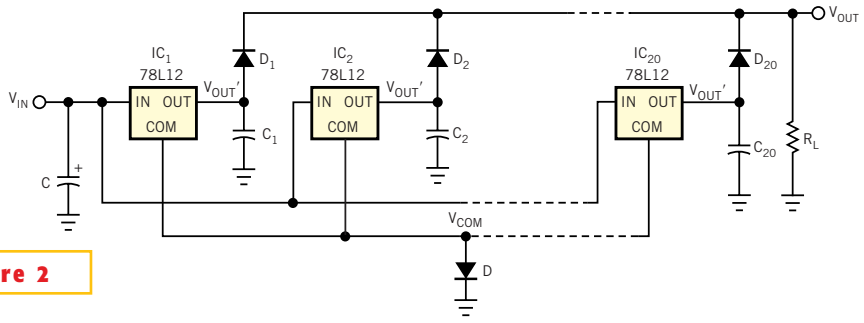


Figure 1 Two 7812s connect in parallel to double the available output current to 2A.

The two 7812s operate independently, and each delivers a maximum of 1A. D_1 and D_2 separate and isolate the two regulators. The output voltage is the regulator's nominal output minus a diode drop: $V_{OUT} = V_{REG} - V_D$. The output voltage of the regulators is the specified value if the COM pin connects to ground (0V). To increase the output voltage of the circuit in **Figure 1** to the desired value, the COM pin must connect to a voltage point one diode drop

above ground. C, C_1, and C_2 are filter capacitors. **Figure 2** shows a voltage regulator that uses 20 7812s and delivers 20A. All the diodes are 1N4007 types. C=47,000 µF, and all the numbered capacitors have a value of 4700 µF. The 7812s all connect to a heat sink that a small fan ventilates. You can expand the concept of this Design Idea to hundreds of amperes.□

Figure 2



A total of 20 7812 regulators extend the capability of Figure 1's circuit to 20A.

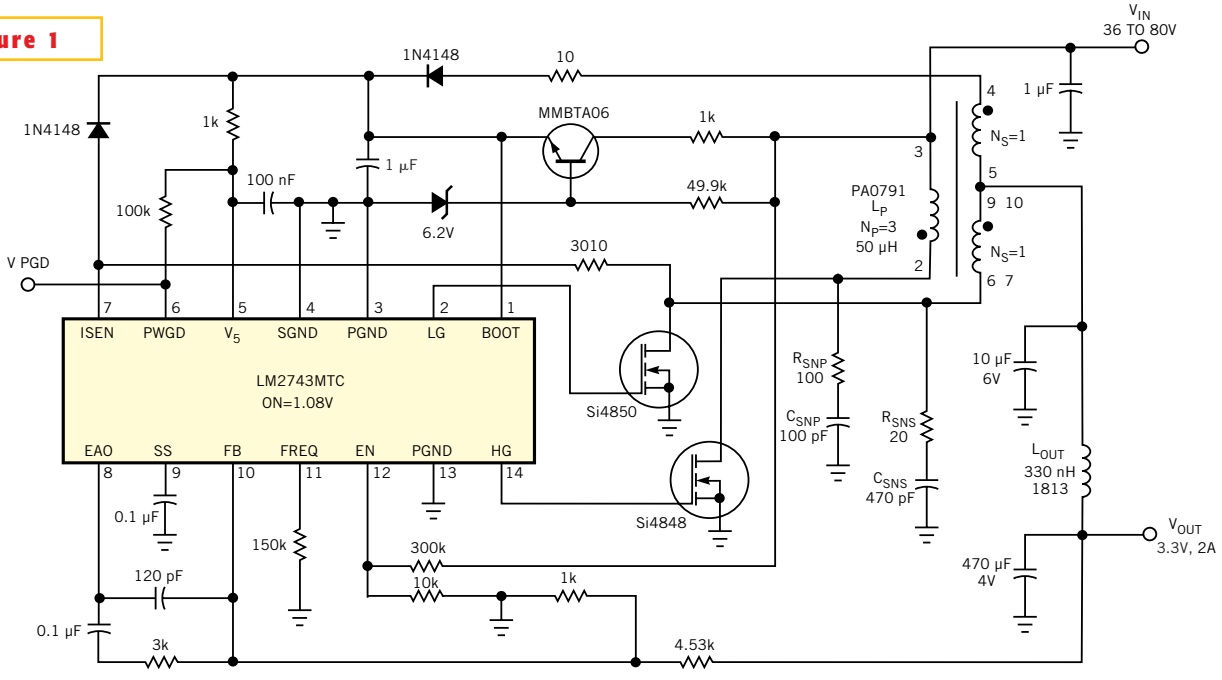
Synchronous flyback circuit provides high-efficiency conversion

Wayne Rewinkel, National Semiconductor, Phoenix, AZ

Buck regulators are usually the first choice when you design nonisolated step-down regulators unless the ratio of V_{IN} to V_{OUT} is greater than 10, the input voltage is high, or both. Low duty cycle can be problematic for FET drivers and cause current-mode control loops to lose control. Efficiency can fall dramatically to 60 to 70% at low V_{OUT} and current of only a few amps. The efficiency loss arises from switching losses, because the upper switch always sees full load current. **Figure 1** presents a circuit that looks a little like a buck regulator and uses a buck controller but is actually a voltage-mode, synchronous flyback circuit. The application it targets needs 3.3V at 2A with an efficiency requirement of greater than 85% and an input-voltage range of 36 to 60V. This one appeared the most promising of several evaluated technologies because of efficiency and cost advantages over buck and asynchronous-flyback approaches.

The LM2743 controller derives its power after start-up from the MMBTA06 transistor and 6.2V zener diode and from a bootstrap winding. Its EN (enable) input is a comparator for UVL (undervoltage lockout) to prevent start-up below 28V. The controller drives a synchronous switch that provides lower loss than a Schottky diode and uses the lower FET's on-resistance as the sense resistor for current limiting. The 150-kΩ resistor at Pin 11 produces a switching frequency of 250 kHz. The flyback transformer, designed by Pulse Engineering (www.pulseengineering.com), is a low-

Figure 1



This synchronous flyback circuit provides high efficiency with wide input/output ratios.

cost unit that provides 50 µH of primary inductance and a 3-to-1 turns ratio in a 13L×15W×11H-mm footprint. Its 3-to-1 turns ratio prevents the primary switch from seeing full output current, resulting in less switching loss than that of a buck regulator. The small LC filter at the output allows a single 10-µF ceramic capacitor to handle the high rms ripple current, and a low-cost aluminum capacitor also removes ripple and buffers load transients.

Figure 2 plots measured data at three input voltages and several output currents for the circuit in **Figure 1**. Efficiency is displayed on the left for the three uppermost curves, and the three lower curves show total loss in watts measured by the scale on the right. V_{OUT} ripple measured 6 mV p-p at no load, rising to 20 mV p-p at 4A. The rapid fall in efficiency at 3.5A comes from current limiting. As with any switcher and especially for flyback designs, pc-board layout is important. You obtain best performance with four or more layers, separate power and ground planes, and short and wide gate-drive connections. Although the circuit of **Figure 1** targets use in a 7W, single-output requirement, this synchronous flyback circuit applies to a wider power range; you can easily extend it to multiple outputs by adding secondary windings. The additional outputs can use either diode rectifiers or additional FETs driven from the low-gate driver.□

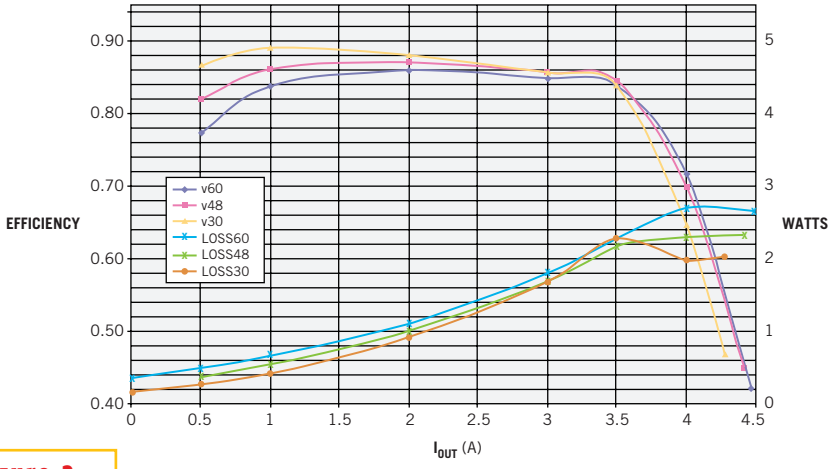


Figure 2 The circuit in Figure 1 provides more than 85% efficiency over a wide range of output currents.

design ideas

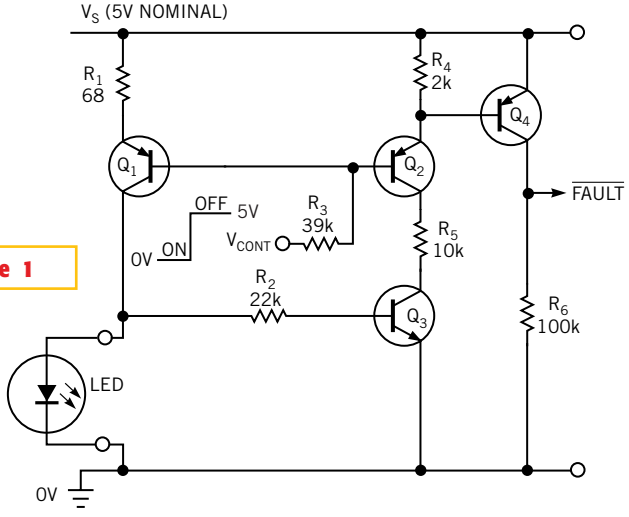
Edited by Bill Travis

LED driver doubles as fault monitor

Anthony Smith, Scitech, Biddenham, Berdfordshire, England

LEDs find wide use as indicators and as light emitters in devices such as optocouplers. In some applications, the LED or the emitter may be located remotely at some distance from the main unit. Typical examples are dashboard-mounted automotive indicators and industrial optosensors. In critical applications, you may require some means of monitoring the integrity of the LED. Using just four transistors and six resistors, this circuit provides switchable, constant-current drive for an LED and indicates both open- and short-circuit fault conditions (**Figure 1**). And there's a bonus, too. Control signal V_{CONT} switches the LED on and off. When V_{CONT} is high, Q_1 and the LED are off. When V_{CONT} is as low as 0V, Q_1 turns on and sources a constant current to the LED. Because most LEDs have a forward-voltage drop of at least 1.2V, adequate base-bias voltage exists for Q_3, which turns on, thereby providing a conduction path for Q_2. This conduction, in turn, provides bias for Q_4, which turns on and pulls high, thus indicating a healthy LED.

Figure 1



This LED driver doubles as a fault monitor and limits short-circuit current to boot.

Because Q_2 and Q_4 are both now on, the base potential of Q_1 sits at roughly two V_{BE} drops below the positive-supply rail, V_S, thereby placing one V_{BE} drop across R_1. Consequently, with R_1=68Ω, Q_1 sources a steady current of approximately 10 mA to the LED. Provided that the value of R_2 is large enough, little of the LED's forward current diverts into Q_3's base. As long as the LED remains undamaged, $\overline{\text{FAULT}}$ stays high, signaling normal drive conditions. Should the LED go open-circuit, Q_1's collector load becomes just R_2 in series with Q_3's base. Because R_2 is much larger than R_1, Q_1 saturates, the voltage across R_1 falls to around 20 mV or so, and the emitter potentials of Q_1 and Q_2 rise toward V_S. With insufficient base drive, Q_4 now turns off, and the output falls to 0V to signal the fault condition.

On the other hand, if a fault puts a short circuit across the LED, Q_3 immediately turns off and deprives Q_2 of collector current. Q_2's base-emitter junction now behaves like a diode, clamping Q_1's base to a potential dictated mainly by Q_2's V_{BE} drop and by the ratio of R_3 to R_4. Because R_4's value is smaller than that of R_3, Q_2's emitter potential now rises toward V_S. Once again, Q_4 turns off and goes low to indicate the fault condition. With the resistor values shown in **Figure 1**, Q_1's base now sits at approximately 4V, leaving only 200 to 300 mV across R_1. Therefore, the short-circuit current is effectively "choked back" to less than a third of the normal value, thereby saving power—the bonus. Under normal conditions, with the LED on, Q_1 conducts more current than Q_2, causing its V_{BE} drop to be slightly larger than that of Q_2. Consequently, the potential across R_1 is slightly less than a diode drop, and you may need to experiment with the value of R_1 to set the desired LED current.

You must select R_3 to satisfy the base-current requirements of Q_1 and Q_2 when V_{CONT} is low. Tests on the prototype circuit produced good results with R_3=39 kΩ, although a smaller value may be required, depending on the LED current and the current gain of Q_1 and Q_2. When the LED is on, both Q_2 and Q_3 are fully on, so a reasonably large value of R_5 is required to limit their joint collector current to an acceptable level. However, R_5 must not be too large, or Q_2 will be unable to furnish the current that R_4 and Q_4's base require. Making R_5 approximately four or five times larger than R_4 is a good starting point.

Although the circuit in **Figure 1** has a

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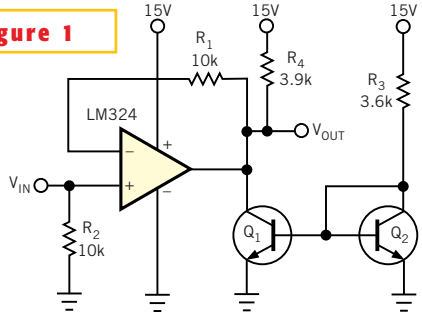
5V supply, you could use other voltages, provided that you scale the resistor values accordingly. Operation at lower voltages is possible as long as Q_1 has adequate "headroom" to stay out of saturation, but beware of problems if you use a blue or a white LED, because these devices tend to have relatively high forward-voltage drops. The transistor types are not critical; most small-signal devices with high current gain should be adequate, although Q_1 may need to be a power device if your design requires a high LED current, a high supply voltage, or both.□

Current source enables op amp's output to go to ground

Frank Chan, Vancouver, BC, Canada

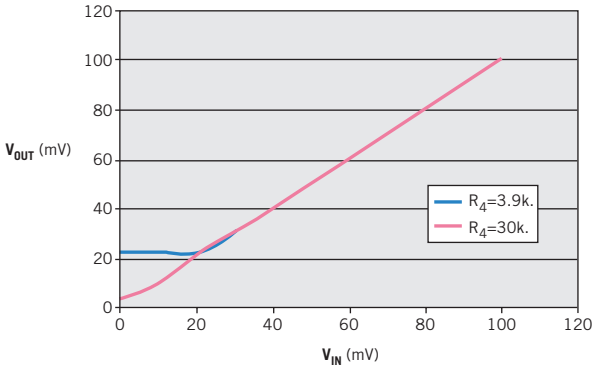
The LM324 is a cost-effective choice for an op amp, especially when you need to apply ground-level inputs. Although its output purportedly includes ground, its poor current-sinking capability limits the applications. At output voltages lower than 0.5V, the op amp's sinking current ranges only from 2 to 100 µA. You can add an external current-sinking circuit to bring the usable output voltage down to the millivolt level. In **Figure 1**, Q_1, Q_2, and R_3 form a 4-mA current source that drains the output of the LM324. R_4 is the load, demanding a sink current of 4 mA. This design uses a 2N2222 transistor for its low saturation voltage. The output characteristic becomes the saturation characteristic of the added transistors, Q_1 and Q_2. Using this current source, the output voltage is linear down to 22 mV above ground. **Figures 2** and **3** show the output characteristics. The lowest usable output voltage depends on the load (sink) current. When the load current is 0.5 mA (R_4=30 kΩ), the output voltage is linear down to 4 mV. **Figure 4** is the original output characteristic of the LM324 driving R_4 (3.9 kΩ) without the added sinking current source. The current source presents a constant load to the LM324. You can configure a leftover op amp as a voltage comparator to cut off the current source when the output voltage is higher than 1V.□

Figure 1



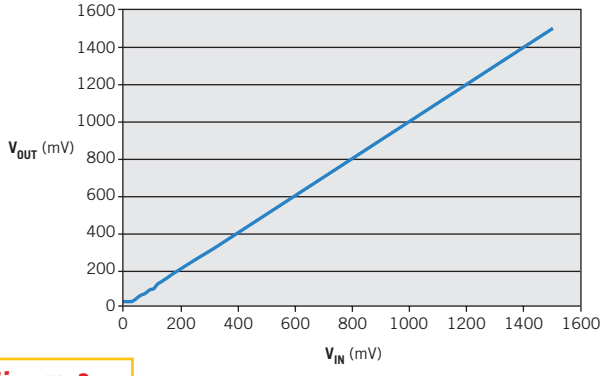
An external current source can bring the usable output level of an LM324 down to the millivolt level.

Figure 3



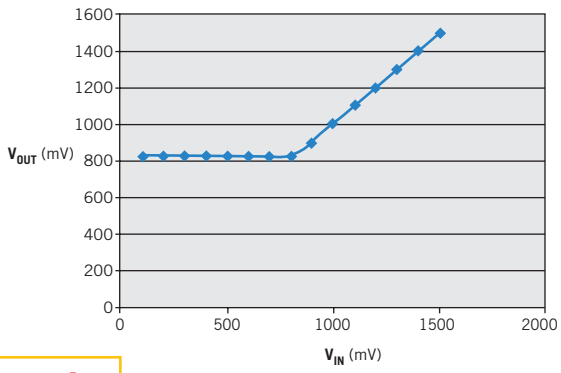
With 0.5-mA load current, the output voltage is linear down to 4 mV.

Figure 2



The transfer function of Figure 1's circuit is linear down to the low-millivolt level.

Figure 4



This graphic shows the LM324 transfer function without the added current source.

Circuit distorts duty cycle for CML inputs

Dieter Verhulst and Xin Yin, Ghent University, Belgium

To test a gigabit-speed data-recovery chip, you need a clock with a controllable duty cycle. Because most pattern and clock generators have a fixed duty-cycle output of 50%, the design may require a small circuit to distort the duty cycle. The signal with controllable duty cycle drives a standard CML (current-mode-logic) input with on-chip termination resistors. One side, V_P, of the differential CML input takes single-ended drive from a PECL (positive-emitter-coupled-logic) circuit (**Figure 1**). The other input, V_N, connects to a controllable dc voltage. If this dc voltage is equal to the average voltage of the single-ended signal, the duty cycle stays 50%. If the signal has nonzero rise and fall times (T_{RF}), you can distort the duty cycle by lowering the dc voltage (**Figure 2**). The distortion generated is equal to the time difference between the crossing of the single-ended signal and its average and the crossing between the single-ended signal and the set dc voltage (DT). Thus, the theoretical maximum distortion that you can generate is T_{RF}.

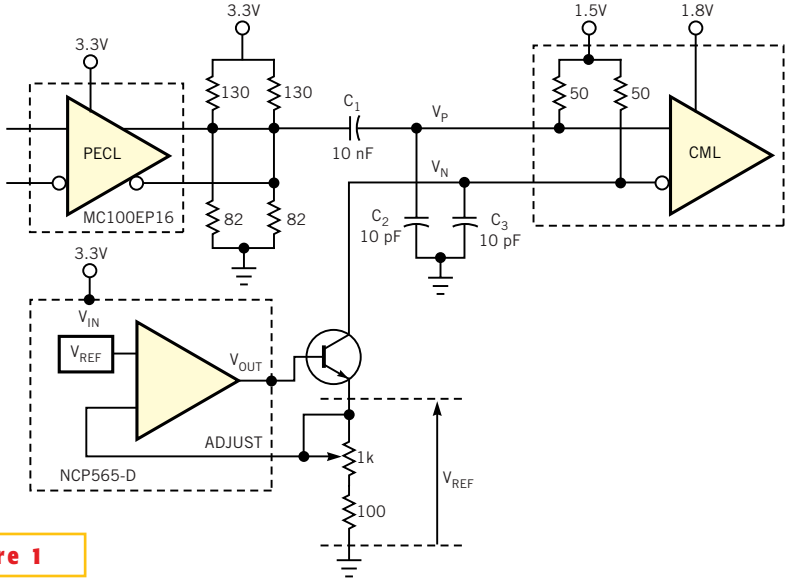


Figure 1

This circuit can make slight adjustments to the duty cycle you apply to a CML input.

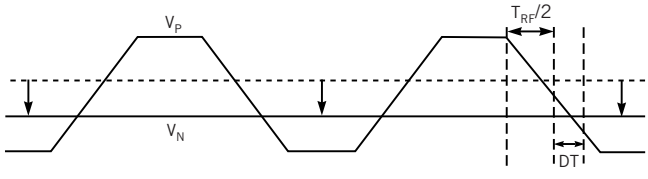


Figure 2

By exploiting the rise and fall time of a signal and manipulating a dc bias voltage, you can control the duty cycle of a CML signal.

You can control T_{RF} by selecting a buffer with the desired T_{RF} value, the MC00EP16 buffer in this design, and by changing the output capacitance for this buffer (C_2). To set the voltage at node V_N, the design uses the internal termination resistors and a controllable current source instead of applying a dc voltage source. This procedure makes the circuit more immune to power-supply changes. Because the single-ended signal is ac-coupled, the average voltage of this signal at node V_P is equal to the internal ter-

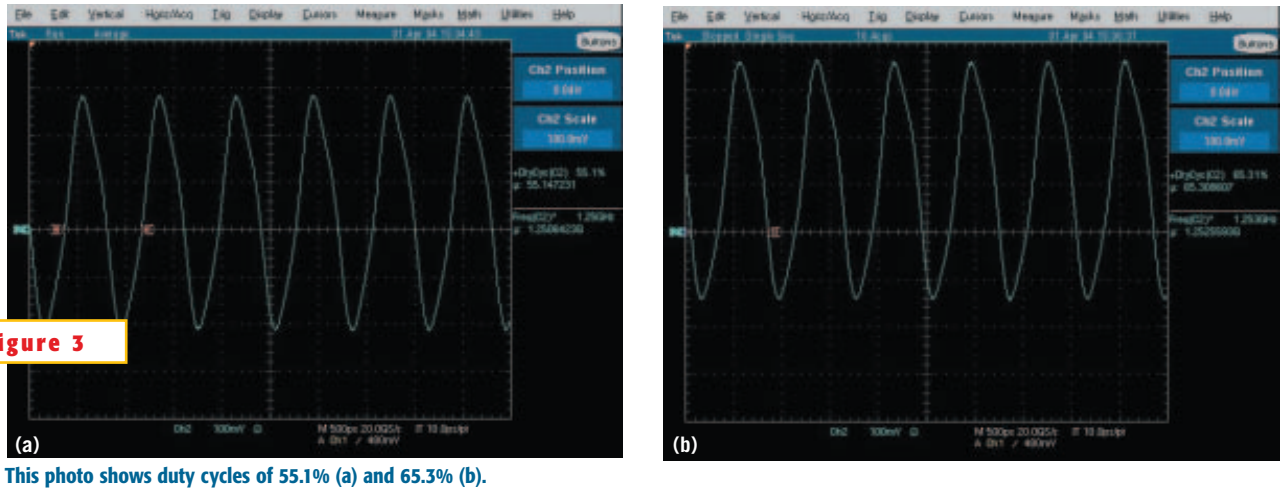


Figure 3

This photo shows duty cycles of 55.1% (a) and 65.3% (b).

mination voltage of the CML input. If no current enters the V_N input, this node also assumes the internal termination voltage, and the duty cycle is 50%. This voltage is independent of the average voltage of the single-ended signal at the buffer's output and the internal termination voltage.

The NCP565-D voltage reference, using a reference voltage, V_{REF}, of 0.9V, creates a stable, controllable current source. The buffer inside the reference drives the bias voltage of an npn transistor and changes it until the voltage at Adjust is equal to V_{REF}. The current pulled through the transistor and the V_N input is equal to V_{REF}/R. R is the resistance between the emitter of the transistor and ground. Changing R changes this current, the voltage at V_N, and, therefore, the duty cycle for the signal that the CML input sees. The circuit was tested with a 1.25-GHz clock. **Figure 3** shows the waveforms of the differential signal ($V_P - V_N$) at the CML input set at 55% (**Figure 3a**) and 65% (**Figure 3b**). The described circuit increases the duty cycle; if the duty cycle needs to decrease, you'd connect the single-ended signal to V_N and the current source to V_P.□

Build a charge pump with ultralow quiescent current

Greg Sutterlin, Maxim Integrated Products, Sunnyvale, CA

Portable battery-powered devices often spend most of their life in standby mode, in which the quiescent current of an internal boost converter continuously bleeds the battery. The quiescent current during standby can be larger than the actual load current. Though several inductor-based converters offer maximum quiescent current of less than 10 µA, designers usually prefer or require a regulated charge pump for cost-sensitive designs that must be intrinsically safe. Off-the-shelf regulated charge pumps with output-current capabilities of at least 10 mA have typical minimum quiescent currents of 50 to 100 µA. If that level of quiescent current is unacceptable, you can reduce the overall average by adding circuitry that remotely monitors the regulated voltage and toggles the charge pump into and out of shutdown. That approach, however, may not achieve the desirable quiescent-current level of less than 10 µA. The advent of low-on-resistance analog switches and ultralow-current comparators and references makes possible a charge-pump circuit whose maximum quiescent current is approximately 7 µA (**Figure 1**).

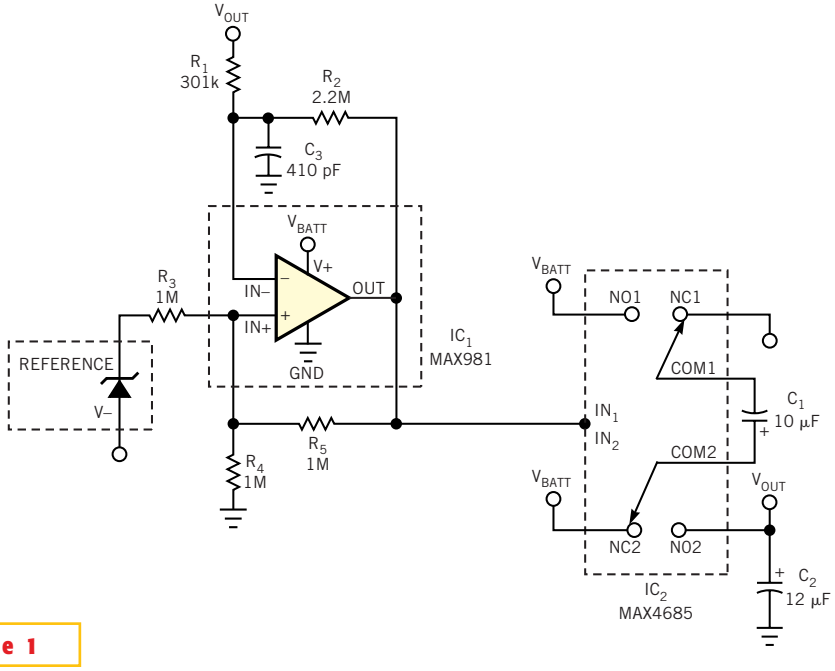


Figure 1

This charge-pump circuit uses analog switches to achieve ultralow quiescent current.

Charge pumps use an ac-coupling technique to transfer energy from a transfer capacitor to a storage capacitor. The transfer capacitor first charges via analog switches to the level of V_{BATT}, and then other analog switches transfer the energy to a storage capacitor tied to V_{OUT}. The transfer capacitor then charges again, and the cycle repeats. With ideal analog switches exhibiting zero loss, the V_{OUT} level equals two times V_{BATT}. As expected, however, the analog switches' finite on-resistance produces an output level that drops in proportion to the load current. The basic regulated charge pump in **Figure 1** includes an oscillator, several analog switches, a voltage reference, and a comparator. The comparator serves as a voltage monitor and an oscillator. When the circuit is in regulation, the comparator output is low, which closes the NC (normally closed) switches and allows C_1 to charge to V_{BATT}. When the voltage at V_{OUT} dips below the output-regulation threshold—3.3V in this case—the comparator output goes high. The NO (normally open) switches close, transferring C_1's

charge to C_2. This cycle repeats until V_{OUT} regains regulation.

Resistors R_3 to R_5 provide the hysteresis necessary for oscillation. Their value, 1 MΩ, creates a notable level of hysteresis and minimizes V_{BATT} loading. As the comparator output changes state, feedback resistor R_5 creates hysteresis by moving the threshold you apply to the comparator's positive input. For the resistor values shown, reference value nominal for IC_1 (1.182V), and V_{BATT}=3V, the V_{IN}+threshold swings between approximate values of V_{IN}+(low)=0.39V and V_{IN}+(high)=1.39V. When the circuit is in regulation, V_{IN}− slightly exceeds V_{IN}+, the comparator output is low, the R_1-R_2 divider senses the voltage at V_{OUT}, and the threshold at V_{IN}+ is low (0.39V). With V_{IN}+ at 0.39V, you can calculate the R_1 and R_2 values from the equation $V_{IN}+=V_{OUT}[R_2/(R_1+R_2)]$. The resistance of R_1+R_2 should be greater than 1 MΩ to minimize V_{BATT} loading. If V_{OUT}=3.3V and R_2 is 2.2 MΩ, R_1 calculates to 301 kΩ. Capacitor C_3 connects to the comparator's V_{IN}− input. Along with R_1 and R_2, C_3 sets the oscillation frequency according to the following simplified relationships: $t_{DISCHARGE}=t_{LOW}=-(R_2C_3)\ln[(V_{IN}+(LOW))/(V_{IN}+HIGH))]$; $t_{CHARGE}=t_{HIGH}=-(R_2C_3)\ln[1-(V_{IN}+(HIGH)-V_{IN}+(LOW))/(V_{BATT}-V_{IN}+(LOW)]$; and $f_{OSC}=1/t_{PERIOD}$, where $t_{PERIOD}=t_{LOW}+t_{HIGH}$.

To maximize efficiency and reduce the effects of comparator slew rate, you should set a relatively low frequency. Choosing C_3=470 pF yields the following: t_{LOW}=178 µsec, and t_{HIGH}=68 µsec; thus, f_{OSC}=4 kHz.

Select the values of C_1 and C_2 to achieve the desired load current and ripple. For this application (I_{LOAD}=10 mA), C_1=10 µF. To calculate the value of C_2, make an approximation based on the desired ripple voltage: $C_2=(I_{LOAD}\times t_{LOW})/V_{RIPPLE}$. With I_{LOAD}=10 mA and V_{RIPPLE}=150 mV, C_2=12 µF.

With these component values, the circuit draws a maximum quiescent current of 6.9 µA and offers a considerable improvement over off-the-shelf charge pumps. You can further lower the quiescent current by increasing the resistor values, but that effect is minimal because IC_2's maximum quiescent current of 3.8 µA dominates the total. This circuit lets you implement an ultralow-quiescent-current-regulated charge pump. Until off-the-shelf options are available, it provides an alternative for designers seeking to implement a low-cost design without the use of inductors.□

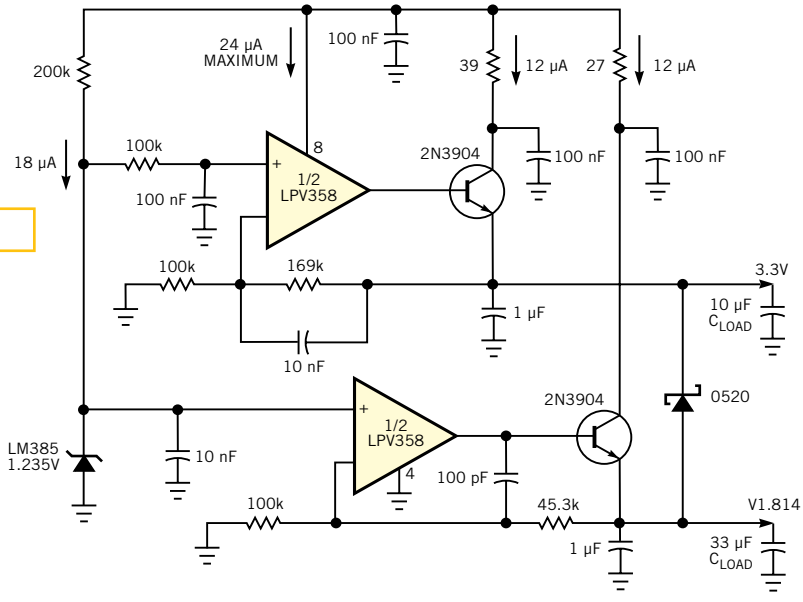
Edited by Bill Travis

Dual-voltage regulator meets USB-power needs

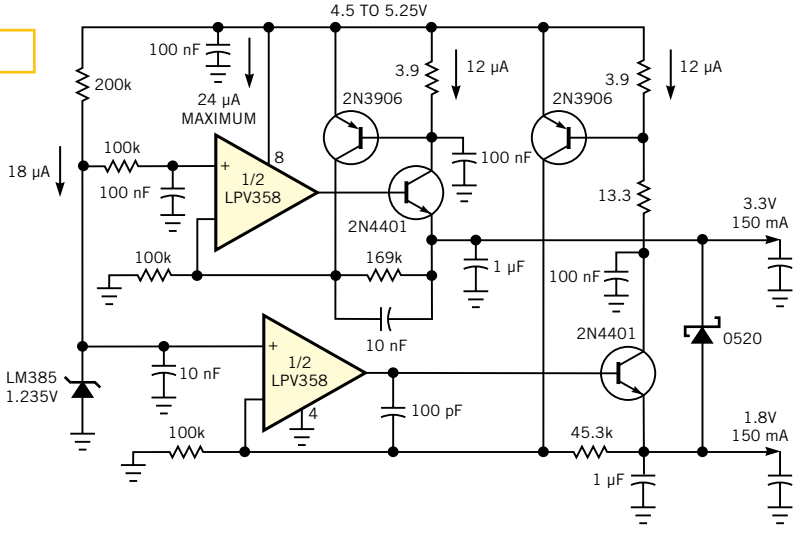
Wayne Rewinkel, National Semiconductor, Phoenix, AZ

THIS DESIGN IDEA stems from the limited availability of IC voltage regulators that can meet key USB-power specs, coupled with the need for turn-on sequencing and rise-time control at each output. As always, for PC-related designs, minimum cost is a primary motivation. USB specs require all loads to limit inrush current to less than 100 mA plus 50 µC of charge when powered on. If permission is granted to increase the load to 500 mA, inrush limiting may be required again to prevent excursions over the 500-mA limit. The other troublesome USB-power requirement is the "suspend"-current maximum of 500 µA, of which you may use only 250 µA; a termination resistor requires the rest. Suspend requires the load to power down but keep alive just enough to listen for permission to power up again. So, the sum of the regulators' operating currents plus load current must be less than 250 µA. The dual-regulator circuit meets the USB spec and powers an ASIC that requires a core voltage of 1.8V and I/O voltage of 3.3V to rise with a controlled sequence and slew rate (**Figure 1**).

Specifically, the core and I/O voltages track within 0.5V until the core voltage reaches 1.8V. The controlled slew rate limits inrush current to less than 100 mA. Two micropower linear regulators use a very-low-power bandgap voltage reference and a dual op amp. The dual op amp must draw low power, have inputs active to ground, provide rail-to-rail drive, and not reverse polarity as you apply power. Each op amp has an npn transistor buffering its output to provide greater than 100 mA. The regulator loops are stable with these components and



This circuit meets USB specs for controlled power-up sequence and slew rate.



This configuration boosts the output current of Figure 1's circuit to more than 200 mA.

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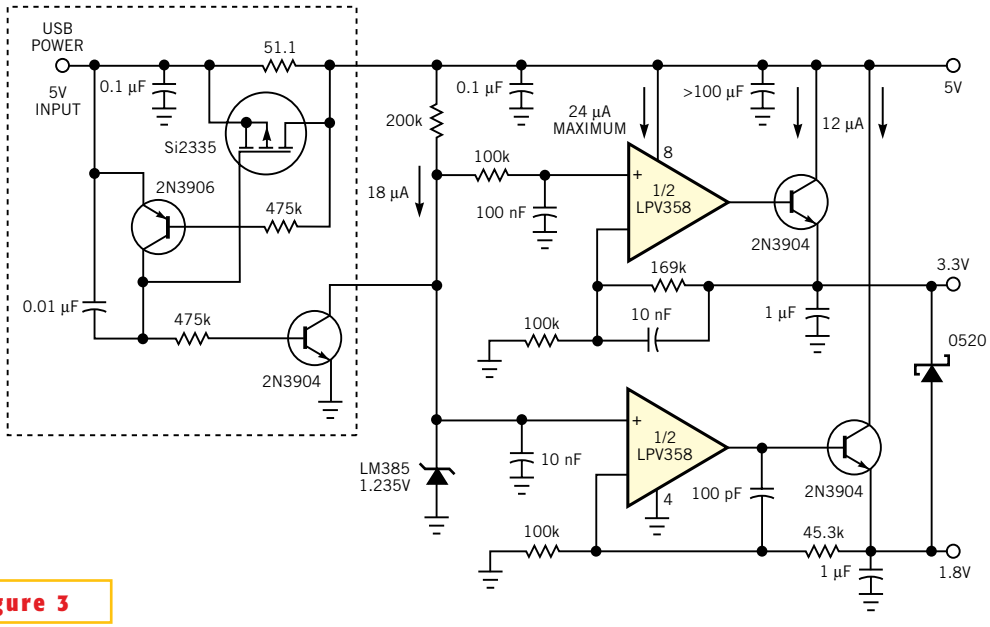


Figure 3

For USB applications requiring 5V, this circuit provides precise inrush limiting.

values. Simple current limiting accrues from a resistor in series with each 2N3904 collector lead.

A 200-kΩ resistor that connects to the 10-nF bypass capacitor at the voltage reference controls the 1.8V power-up rise time. The resulting rise time is approximately $t_{RISE}=20\ \mu A\times 1.235V/10\ nF=2.5$ msec. The 3.3V supply follows the 1.8V supply, according to the 10-msec time constant of its 100-kΩ, 100-nF input filter. A small Schottky diode connected between 1.8V and 3.3V guarantees the 3.3V to be within 0.5V of the 1.8V during start-up. Inrush current of approximately 38 mA is $I_{INRUSH}=C_{LOAD}(dV/dt)$, where C_{LOAD} is the total load capacitance, $dV=1.8V$, and $dt=t_{RISE}$. The total operating quiescent current of this dual regulator measures just 56 µA, and the worst-case maximum spec for the circuit in **Figure 1** is 64 µA. This figure leaves 194 µA available for the load during suspend mode. **Figure 1**'s application requires regulator current of less than 150 mA from each output. You can easily modify the circuit to provide more than 200 mA per channel by substituting a 2N4401 for the 2N3904 and adding active current limit with a 2N3906 (**Figure 2**).

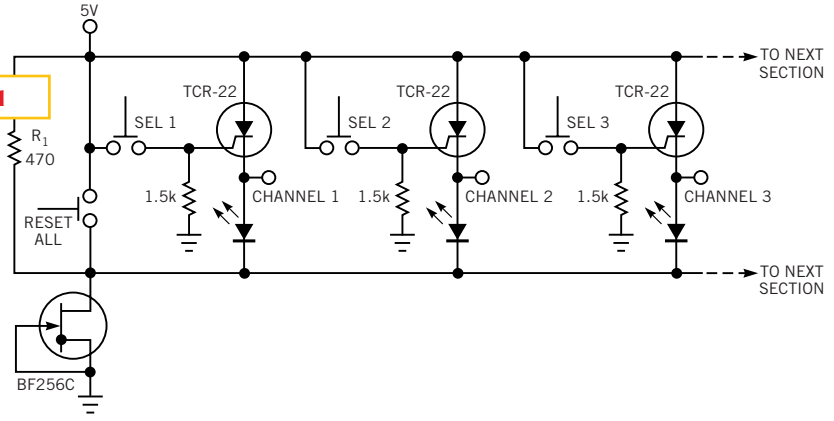
Many USB-powered supplies also require a 5V output. The circuit of **Figure 3** provides precise inrush limiting for 5V and a signal to enable other supplies or loads. The portion of the circuit in broken lines limits inrush current to less than 100 mA at power-on. The 51.1Ω resistor charges the 5V load capacitance to approximately 4.5V, and the 2N3906 then releases the PFET's gate, allowing it to short-circuit the resistor. Finally, the 2N3904 turns off, enabling the linear regulators to start. This inrush circuit precisely limits peak inrush current independently of capacitive load. Use of a large load capacitance prevents load-current spikes from reaching the USB input line.□

Scalable latch requires no capacitors or clock

Robert Most, Dow Corning S&T Electronics, Midland, MI

CIRCUITS THAT LATCH one-of-N switches usually use a digital approach. Such circuits are often useful in human-interface situations, such as audio-mixing consoles, video-feed selection, or current-loop-control redundancy systems. In high-precision analog systems, such as high-fidelity audio or video, elimination of clocking circuits, whenever possible, reduces the chances of coupling noise back into the signals of interest. The circuit in **Figure 1** is a scalable one-of-N latch that has the advantages of no clock and no capacitors, and it has an intrin-

Figure 1



This one-of-N latching circuit uses no clock or capacitors. The LEDs double as channel indicators.

sic "active-channel" indication.

The operating principle of this circuit is based on current steering. A current sink comprising an n-channel JFET, the BF256C, provides approximately 5-mA current draw, which is approximately the hold current of any one of the small-signal SCRs (silicon-controlled rectifiers). When you select a channel by momentarily depressing the corresponding switch, the associated SCR turns on, lighting the LED connected to its cathode and providing a logic one on the CHANx line. The SCR automatically latches the selected line until you depress another channel switch. When you actuate any other channel switch, the corresponding SCR latches, releasing the previous channel. This latch behavior is the result of the inability of the current sink to draw enough current to sustain more than one SCR at a time.

The circuit needs blocking diodes to isolate the cathodes of the SCRs. If you use an LED, as in **Figure 1**, it also doubles as an "active-channel" indicator. You can

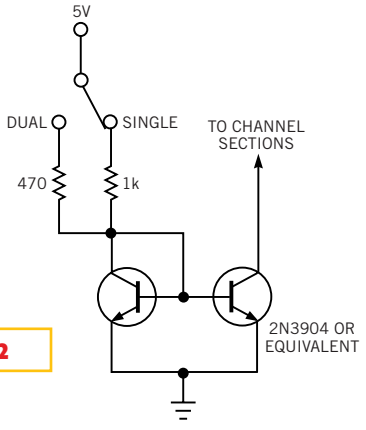


Figure 2

A current mirror replaces the JFET in Figure 1 and allows the choice of single or dual channels.

the use the CHANx line to select an analog switch, a mechanical relay, or another device. Scalability is straightforward: Additional channel sections require only the momentary switch, a 1.5-kΩ resistor, an SCR, and a diode. Because this method uses a current-based scheme, the use of long lines is not an issue. Channel sections can be across control rooms. Upon initial power-up, all channels are in the off-state. In addition, **Figure 1** shows an optional reset-all pushbutton. Depressing the reset-all switch steers the entire current sink's capacity through this switch, thus delatching any SCR that was active.

You can substitute other n-channel JFETs, but you must accordingly scale the drain current of the chosen JFET by varying the value of R_1. You can easily modify this circuit to allow more than one SCR to be active at a given time. For a multiple-active-channel system, you must set the current level to activate only the number of SCRs desired and no more. For example, a system with two active channels would require a current level of 8 to 10 mA in the current sink. **Figure 2** shows a possible alternative current sink, replacing the JFET and R_1, for this arrangement. If you use indicating LEDs in a multiple-channel arrangement, you should take proper precautions with maximum LED current.□

Phone-line-voltage monitor meets FCC specs

Brad Peeters, Theta Engineering, Costa Mesa, CA

When you design equipment that interfaces to a phone line, it is often desirable to be able to monitor the dc voltage on the line. This ability can be useful, for example, to determine whether a line is in use before attempting to go off-hook and possibly interrupting somebody's phone call. FCC regulations place strict limits on the amount of leakage current an on-hook device can draw from a phone line. The specifications work out to approximately the equivalent of 5 MΩ as the minimum leakage resistance. So, you have the challenge of monitoring the line voltage without exceeding the regulatory limits and also maintaining the galvanic isolation required between the phone line and your equipment. The circuit in **Figure 1** shows a method of meeting this challenge with 100% margin. In other

(continued on pg 76)

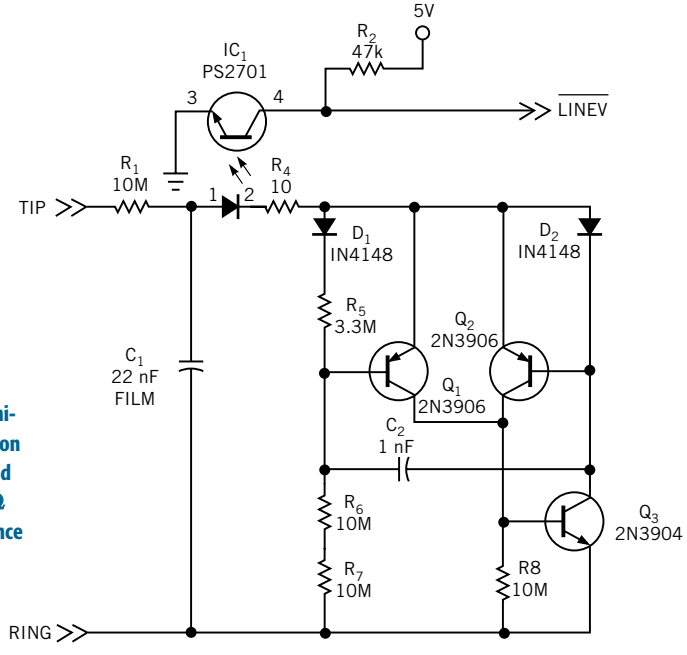


Figure 1

This circuit monitors dc voltage on a phone line and presents 10-MΩ leakage resistance across the line.

words, it presents approximately 10-MΩ leakage resistance across the line.

The basic relaxation oscillator has the LED of an optoisolator in the discharge path of the main capacitor. It delivers a pulse train, the frequency of which varies with the voltage on the phone line. By measuring the period between pulses, the equipment's microcontroller can easily determine the approximate line voltage. C_1 is the timing capacitor. It should be a film-type capacitor rather than ceramic for good results. It slowly charges through R_1, a 10-MΩ resistor. When the voltage across C_1 reaches approximately 3V, the remainder of the circuit turns on, causing C_1 to rapidly discharge through R_4 and the optoisolator's LED. This action causes the optoisolator's output transistor to briefly turn on, creating a low-going pulse approximately 200 µsec wide (the signal labeled $\overline{\text{LINEV}}$). This width is sufficient for even a slow microcontroller to capture an interrupt. When C_1 discharges to approximately 1.5V, the circuit turns off, and the cycle repeats.

Q_2 and Q_3 form an SCR (silicon-controlled-rectifier)-like regenerative pair. D_2 and Q_2 function basically as a current mirror. Normally, you construct a current mirror using two or more identical transistors. By using a 1N4148 diode rather than another 2N3906, you reduce the gain of the current mirror to well below unity. The 1N4148 functions as though it has many times the base-emitter diode area of the 2N3906. Reducing the gain in this fashion helps the regenerative pair to turn off at the appropriate point, keeping the oscillator from "sticking" on. Q_1 and the diode-resistor network driving its base function as the trigger circuit. When the voltage across C_1 gets high enough, Q_1 starts to turn on and inject current into Q_3. Once Q_3 starts to turn on, regeneration kicks in, and Q_3 and Q_2 turn on hard and stay turned on until the capacitor discharges sufficiently. C_2 provides additional positive feedback through Q_1; it improves the operating characteristics of the circuit.

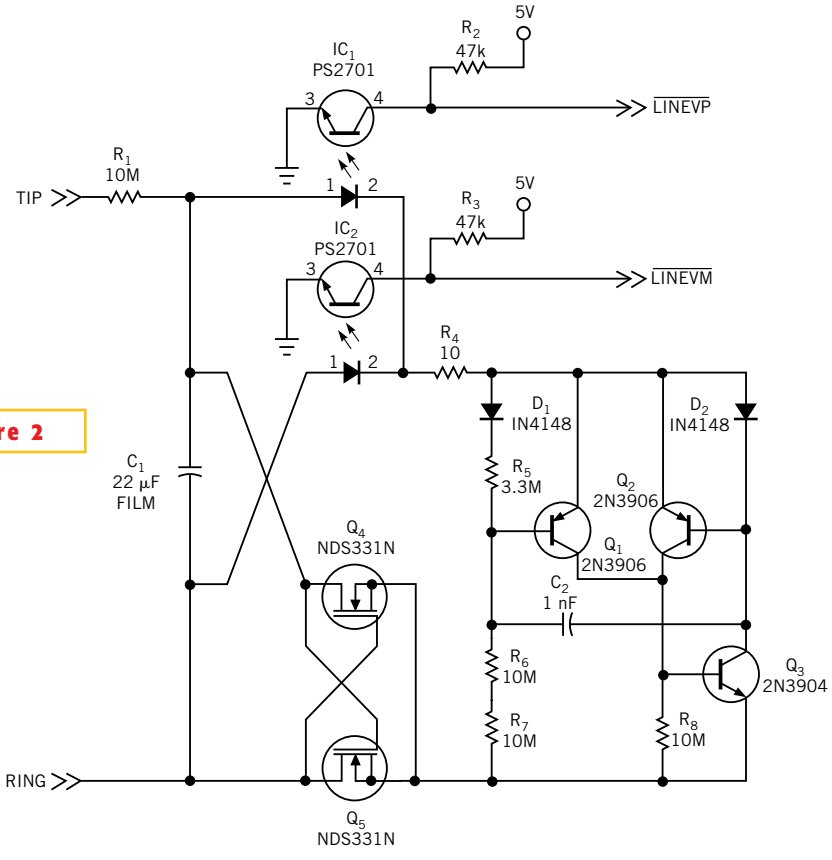


Figure 2

This circuit works with either the Tip or the Ring polarity and reports the polarity of the line to the host microcontroller.

This circuit assumes that Tip and Ring have protection against polarity reversal such that Tip is always more positive. The circuit of **Figure 2** works with either polarity and reports the polarity of the line to the host microcontroller. This circuit is suitable when you need to know not only the magnitude, but also the polarity of the line voltage. As you can see, it has two outputs, one for each polarity. Q_4 and Q_5 are low-threshold n-channel MOSFETs, connected in such a way as to always connect the bottom rail of the relaxation circuit to the most negative side of the timing capacitor. The positive rail of the relaxation circuit connects to the most positive side of the timing capacitor using diode isolation, taking advantage of the fact that the optoisolator LEDs are diodes.

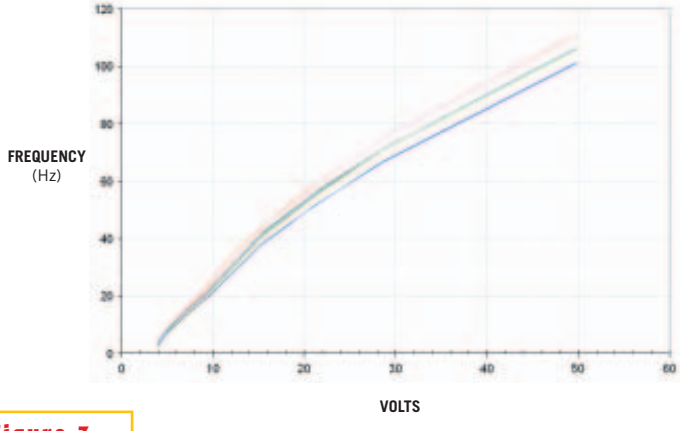


Figure 3

The frequency-versus-voltage response for the circuit of Figure 2 shows the spread across a sampling of five units for both polarities of line voltage.

Figure 3 shows a plot of the frequency-versus-voltage response of the circuit of **Figure 2**. It shows the

spread across a sampling of five units for both polarities of line voltage. Generally, the responses for the positive and negative voltages in a given unit are so close that the plot lines overlay each other. The unit-to-unit variations are larger and in production are mostly attributable to variations in C_1. Although not highly precise, the circuit is more than adequate for distinguishing between on-hook (typically, greater than 18V) and off-hook (typically, less than 12V) conditions. You can also use it to detect the small voltage changes that might be of interest in detecting barging in—when another device on the line goes off-hook while this device is using the line.□

Instrumentation amp has differential outputs

Moshe Gerstenhaber and Stephen Lee, Analog Devices, Wilmington, MA

State-of-the-art ADCs accept differential inputs, allowing you to differentially implement the entire signal path from sensor to converter. This structure provides significant performance advantages, because differential signals increase the dynamic range, reduce hum, and eliminate ground noise. **Figures 1a** and **1b** show two common differential-output instrumentation-amplifier circuits. The first provides unity gain, and the second implements a gain of two. Both circuits, however, suffer from increased noise, offset error, offset drift, gain error, and gain drift as compared with an instrumentation amplifier with a single-ended output. **Figure 2** shows a differential-output instrumentation amplifier that has none of these deficiencies. The design exploits the fact that the output of an instrumentation amplifier is the difference between the output pin, V_{OUT}, and the reference pin, V_{REF}. This application adds an inverter with a gain of −1 between the two pins.

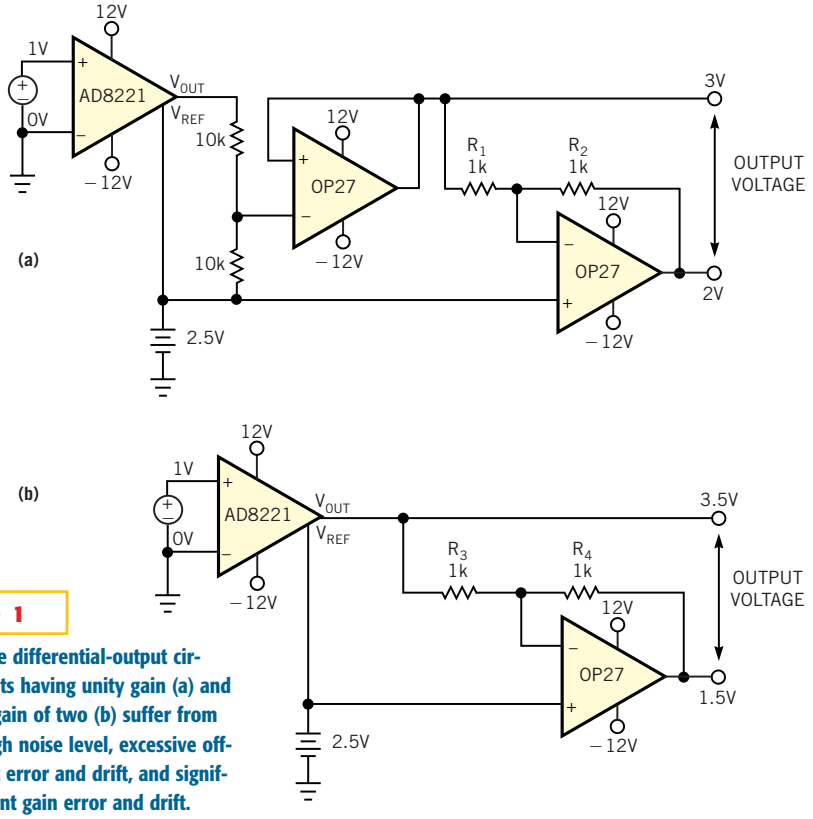


Figure 1

The differential-output circuits having unity gain (a) and a gain of two (b) suffer from high noise level, excessive offset error and drift, and significant gain error and drift.

With an input voltage, V, the output voltage ($V_{OUT}-V_{REF}$) must also be equal to V. The reference pin's voltage is opposite in polarity to the output pin's voltage. Therefore, the output must produce $V_{OUT}=V_{IN}/2$ and $V_{REF}=-V_{IN}/2$ to satisfy $(V_{OUT}-V_{REF})=V$. Applying a 2.5V signal to the noninverting terminal of the op amp sets the common-mode output level. The op amp establishes 2.5V at Node B. Accordingly, if you apply 1V to the input, 3V appears at Node A, and 2V appears at Node C. Thus, the output is 0.5V higher than and 0.5V lower than 2.5V. Errors from $V_{OUT}-V_{REF}$ are a function only of the instrumentation amplifier. Errors such as offset, noise, and gain error that stem

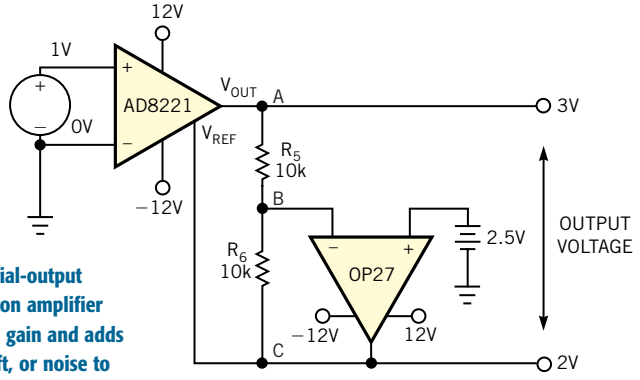


Figure 2

This differential-output instrumentation amplifier preserves the gain and adds no offset, drift, or noise to the output signal.

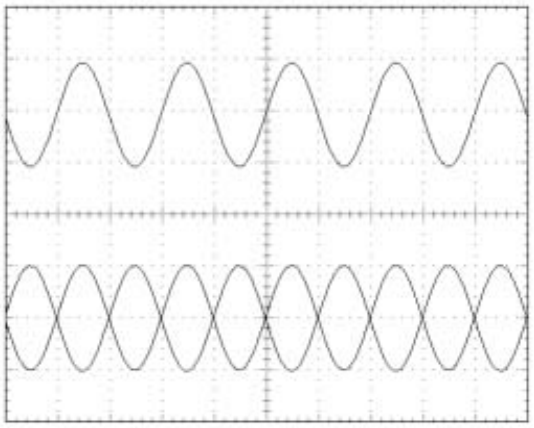


Figure 3 A 2V p-p, 1-kHz input signal (top), and 1V p-p differential-output signals (bottom) have an output common-mode voltage of 2.5V.

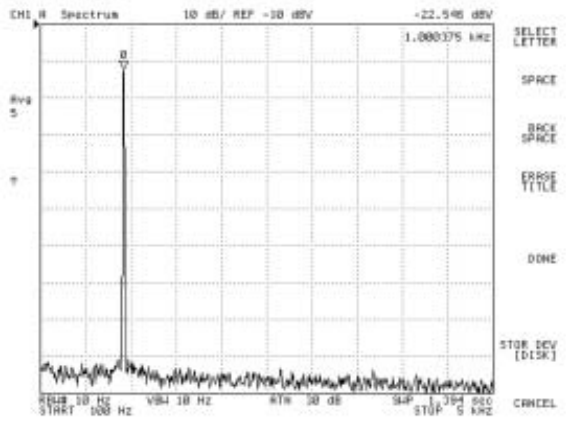


Figure 4 The spectral analysis of the differential-output signal shows that input to the instrumentation amplifier is 2V p-p, 1 kHz.

from the inverter amplifier and resistors equally affect both outputs. Thus, they contribute only to the common-mode output, which the ADC rejects. The top waveform in a performance photo shows the 2V p-p, 1-kHz input (**Figure 3**). The two outputs appear at the bottom. The output common-mode voltage is 2.5V. Another performance photo shows the spectral density of the differential output (**Figure 4**).□

Edited by Bill Travis

Buffer adapts single-ended signals for differential inputs

Randall Carver, Analog Devices Inc, Greensboro, NC

DC COUPLING of single-ended signals into differential-input, single-supply ADCs can be challenging. The input signal requires level shifting from ground to $V_S/2$ as well as single-ended-to-differential conversion. In addition, you must balance the differential inputs of the ADC to cancel even-order harmonics and common-mode noise. Systems often require this signal translation to take place without injecting dc bias currents back into the signal source. Processing wideband signals with large dynamic range (12- to 14-bit ADCs) can also add to the circuit complexity. Wideband amplifiers address nearly all these issues, but their standard implementation requires the use of ac coupling.

This Design Idea describes a new circuit that eliminates this requirement through the use of an external dc feedback loop. It also allows the lower end of the passband to extend to dc. The basis of the circuit is a simple level-shifting circuit (**Figure 1**). Tying two series resistors between V_S and a signal source attenuates the signal by a factor of two and biases it to $V_S/2$. The center tap is buffered; single-sided supply circuits can then process the signal. Two additional series resistors connected between the source and a negative supply of equal value remove dc bias currents from the source.

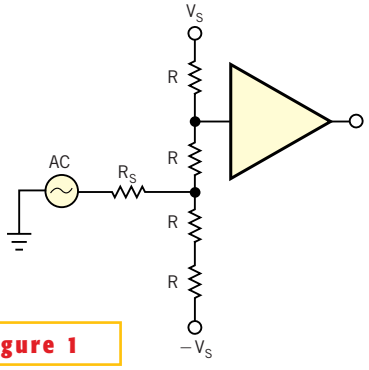


Figure 1

This simple circuit level-shifts ac signals to accommodate the $\pm V_S$ supplies.

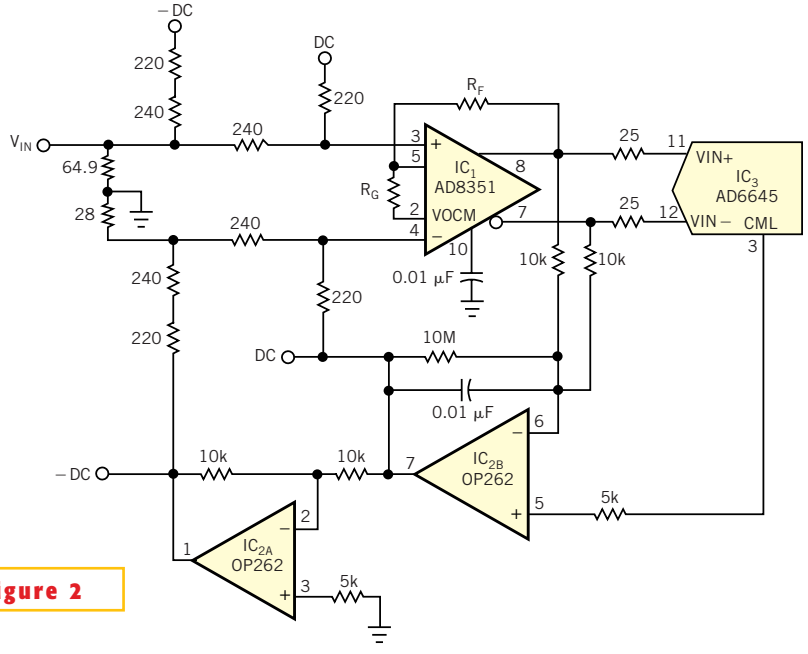


Figure 2

This circuit is a wideband, dc-coupled, single-ended-to-differential buffer.

The circuit of **Figure 2** expands upon this simple concept by replacing the supply voltages $\pm V_S$ with precise $\pm V_{DC}$ levels that track one another. In addition, this design implements differential signaling by doubling the number of level-shifting resistors. You produce the $\pm V_{DC}$ levels by subtracting the 2.4V ADC reference signal (CML pin) from the common-mode level of the amplifier, which you form by summing the two amplifier outputs through equal-value resistors. The circuit amplifies, filters, and inverts the difference to create the $\pm V_{DC}$ levels. The dc feedback-loop gain of approximately 1040 allows the amplifier to track the output common-mode level to within (2.4V/1040)=2.3 mV of the ADC's reference (CML) signal. The addition of this external dc feedback path allows you to open the VOCM pin of IC_1 and de-

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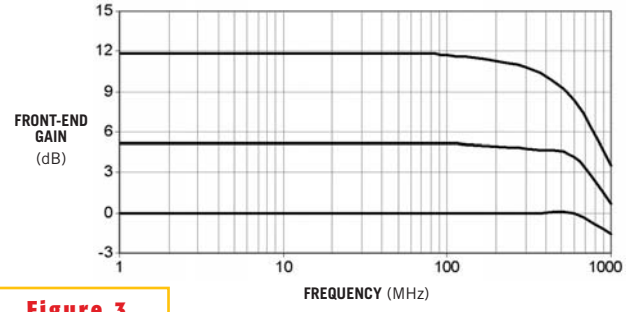


Figure 3

This graphic shows the frequency response of the circuit in Figure 2 for various values of gain.

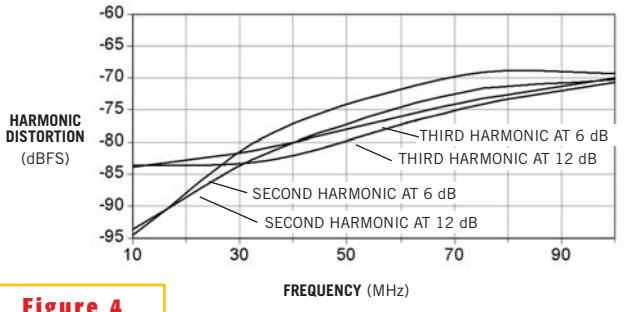


Figure 4

This plot shows harmonic distortion versus frequency for a −1-dB (referred to full-scale) input to the ADC at 80 MHz.

couple it to ground, disabling the AD8351's internal dc feedback path.

The level-shifting resistors have a ratio of 1.09-to-1 to reduce the required swing of the $\pm V_{DC}$ levels to ± 2.4 $[(1.09+1)/1.09] = \pm 4.6$V. The design uses accurate networks with excellent tracking to ensure good CMRR (common-mode-rejection ratio) and minimize the injection of dc bias currents into the source. IC_2 uses a rail-to-rail feedback amplifier to allow the use of ±5V supplies. The remaining circuits are powered from 5V. Resistor R_G varies the overall gain of the front end. For a front-end gain of 0 dB, the bandwidth extends beyond 1 GHz (**Figure 3**). After you determine the required gain, you adjust resistor R_F to balance the two differential signals into the ADC. **Table 1** shows typical values of R_G and R_F for various gain levels. The 64.9Ω resistor provides for a 50Ω source impedance. The 28Ω resistor provides for a balanced input that the amplifier sees. You can accommodate a differential-input signal structure by replacing the 28Ω resistor with a 64.9Ω resistor and tying the additional negative input signal to the junction of the new 64.9Ω resistor and the two 240Ω level-shifting resistors. This differential-input structure allows you to remove R_F. The circuit maintains the excellent distortion performance of the AD8351 amplifier, allowing the circuit to drive 12- and 14-bit ADCs with minimal degradation of the ADC's dynamic range (**Figure 4**).□

TABLE 1—RESISTOR VALUES FOR VARIOUS FRONT-END GAINS

R_G (Ω)	R_F (Ω)	Front-end gain (dB)
56.2	1540	12
154	698	6
1000	316	0

Triac lighting and heating controller uses few parts

David Caldwell, Flextek Electronics, Carlsbad, CA

THE TRIAC LIGHTING-control circuit in **Figure 1** is small and inexpensive because load and housekeeping power come directly from the line voltage, thereby eliminating bulky, expensive supplies. The CLZD010 closed-loop controller maintains constant light intensity by automatically adjusting the timing of the triac's firing until the feedback signal and setpoint command are equal. The 5V supply is a charge pump that energizes C_1 on the negative swing of the line voltage and then transfers charge to C_2 on the positive swing. Zener diode D_2, minus the forward drop of rectifier D_1, sets the 5V. Triac Q_1 is a latching switch that conducts in either direction until you remove gate drive and load current drops below its holding threshold, which occurs at the zero-crossing point of the line voltage.

The circuit pulses the triac gate for 100

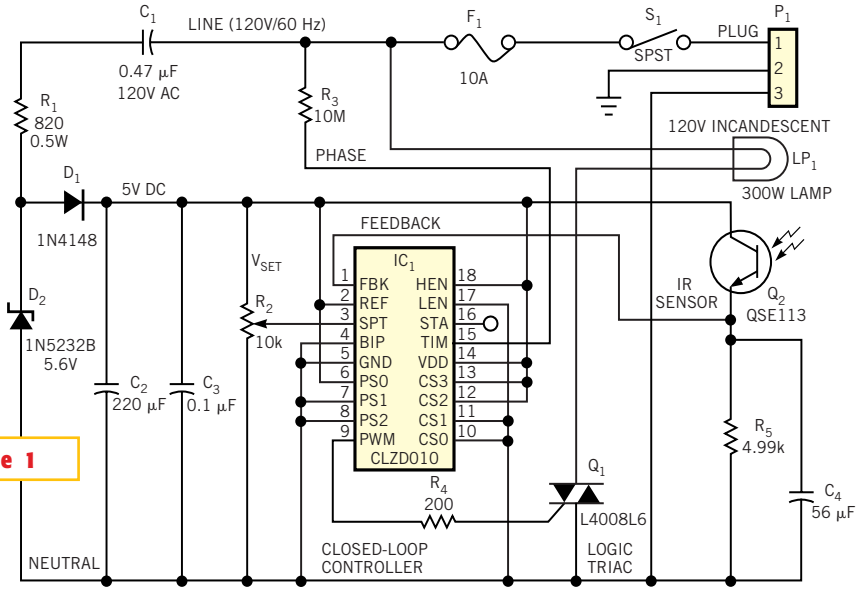


Figure 1

This closed-loop lighting-control system uses a few inexpensive parts.

µsec to turn on the load for the remainder of each 60-Hz half-cycle, so higher power accrues by turning on earlier in the half-cycle. R_3, at the timing pin of the controller chip, detects line phase. Controller pins CS3 to CS0 set the closed-loop configuration for an application. You can easily modify the lighting-control circuit for thermal control (**Figure 2**). Closed-loop timing is 134 sec for optimized temperature response, using controller pins CS3 to CS0. The circuit initially drives the heater at high power levels until the temperature nears its final value and then reduces the power to avoid overshoot. The CLZD010 controller is available from Flextek Electronics (www.flex-tek.com).□

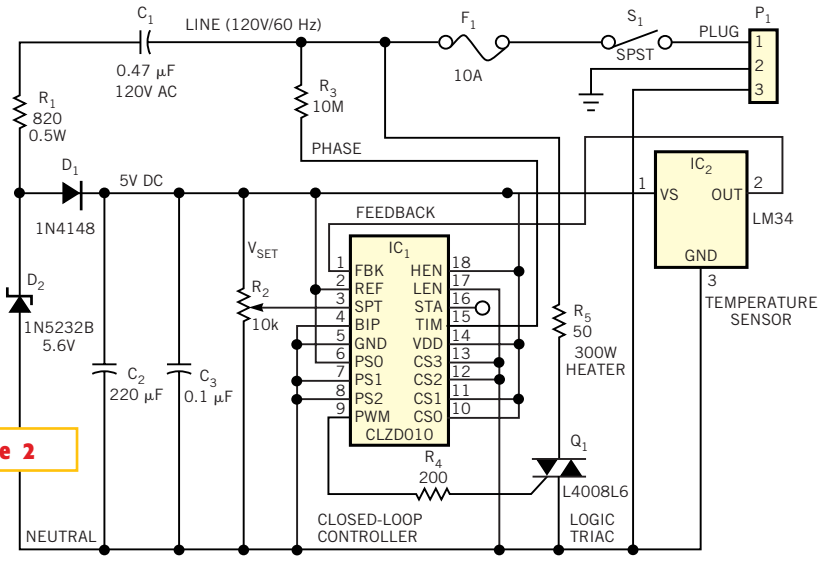


Figure 2

A slight modification adapts Figure 1's circuit to for heating control.

Constant-current, constant-voltage converter drives white LEDs

Keith Szolusha, Linear Technology Corp, Milpitas, CA

LEDs usually take their drive from a constant dc-current source to maintain constant luminescence. Most dc/dc converters, however, deliver a constant voltage by comparing a feedback voltage to an internal reference via an internal error amplifier. The easiest way to turn a simple dc/dc converter into a constant-current source is to use a sense resistor to convert the output current to a voltage and use that voltage as the feedback. The problem is that 500 mA of output current with a 1.2V drop—the typical reference voltage—in the sense resistor incurs relatively high power losses and, thus, a drop in efficiency.

One approach is to use an external op amp to amplify the voltage drop across a low-value resistor to the given reference voltage. This method saves converter efficiency but significantly increases the cost and complexity of a simple converter by using additional components and board space. A better approach is to use the LT1618 constant-current, constant-voltage converter, which combines a traditional voltage-feedback loop and a unique current-feedback loop to operate as a constant-voltage, constant-current dc/dc converter.

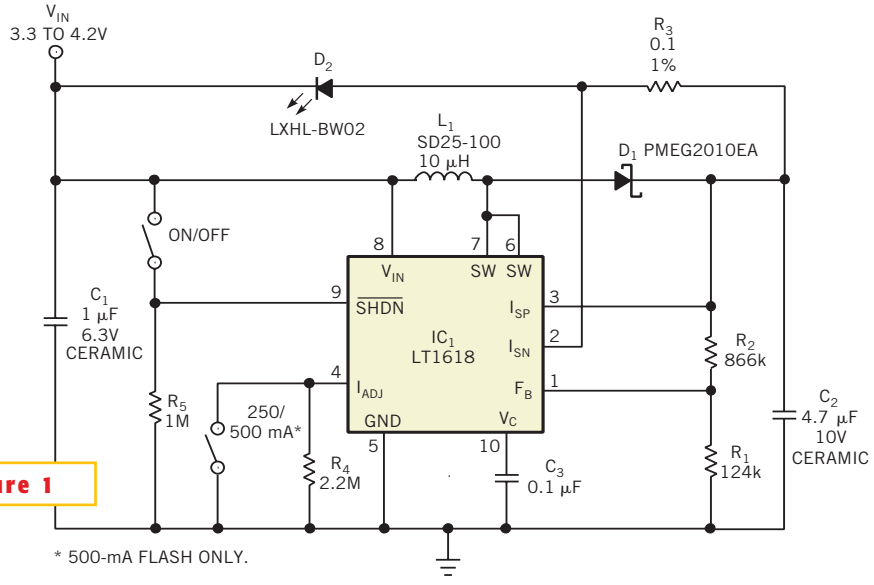


Figure 1

The LT1618 white-LED driver supplies 250-mA constant current and 500-mA flash from a lithium-ion battery.

Figure 1 shows the LT1618 driving a 1W, white Lumileds (www.lumileds.com) LXHL-BW02 Luxeon LED.

You need no external op amps for this compact approach. The LXHL-BW02 has a forward voltage of 3.1 to 3.5V for 250 mA of current. Although the maximum dc rating of the LED is 350 mA, you can pulse it up to 500 mA for a camera flash. R_4 is set for a 250-mA torch or dimming operation. The I_{ADJ} (current-adjustment) pin provides the ability to dim the LED during normal operation by varying the resistor setting or injecting a PWM signal. Access to both the positive and the negative inputs of the special in-

ternal constant-current amplifier allows you to place the sense resistor anywhere in the converter's output or input path and provide constant output or input current. Without access to both inputs, you would need a ground-referenced sense resistor, some additional level-shifting transistors, or an op amp. In this case, the floating sense resistor's value is only 100 mΩ; at 500 mA, it consumes an average of 50 mW of power. The sense resistor connects directly to the positive and the negative input pins of the LT1618.

Although the LT1618 conventionally serves as a high-frequency boost converter with the load connected between V_{OUT} and ground, this method of tying the load from V_{OUT} back to V_{IN} allows the IC to drive the LXHL-BW02 from a lithium-ion battery input. Tying the load back to V_{IN} allows the forward voltage of the LED (the load voltage) to be either above or below the input voltage as the battery voltage changes. This topology avoids the need for an additional inductor. This design uses one small, low-cost inductor, matching the all-ceramic capacitors and low-profile IC. Tying the load back to V_{IN} increases the inductor current by summing both the input and the output currents. The internal switch losses double, and the overall efficiency of the approach is approximately 70% over the input-voltage range. Even at this efficiency, it is difficult to match the compactness and low cost of this approach.□

Sequential state machine aids in automatic control

Abel Raynus, Armatron International, Malden, MA

Creating a sequential state machine is a common approach for automatic-control design. The method finds wide use for controlling sequential processes in industry, robotics, and measuring. The concept of a state machine is simple: A number of states describe a process under control; each state produces some output signals and advances to the next state according to received input signal.

Two kinds of state machines exist. In a Moore machine, only the current state determines an output. A Mealy machine's output depends on both the current state and the inputs. A state diagram uniquely and completely specifies a Moore machine (**Figure 1**). Based on this diagram, you can create a microcontroller program that assigns five assembler directives to each state: an address offset, the outputs, a time to remain in this state (delay value), the next state to go to for an input of zero, and the next state to go to for an input of one.

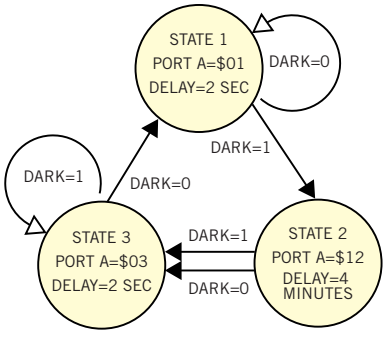


Figure 1 This state diagram uniquely and completely specifies the workings of a Moore state machine.

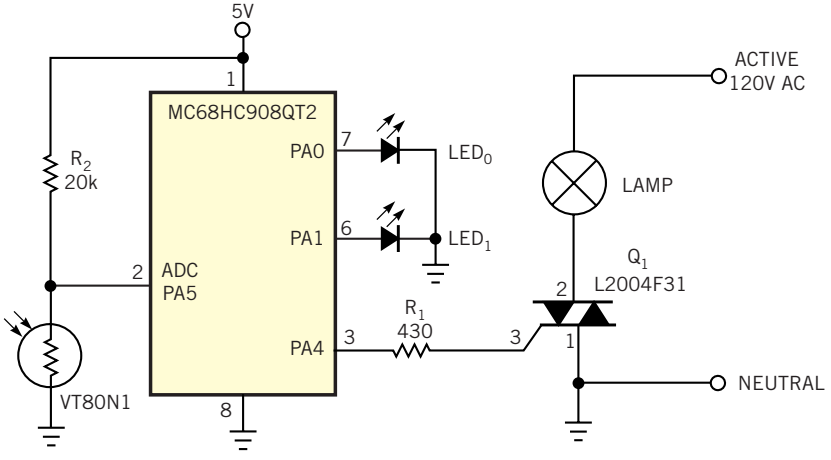


Figure 2 This simple circuit uses a Moore state machine to control a phototimer.

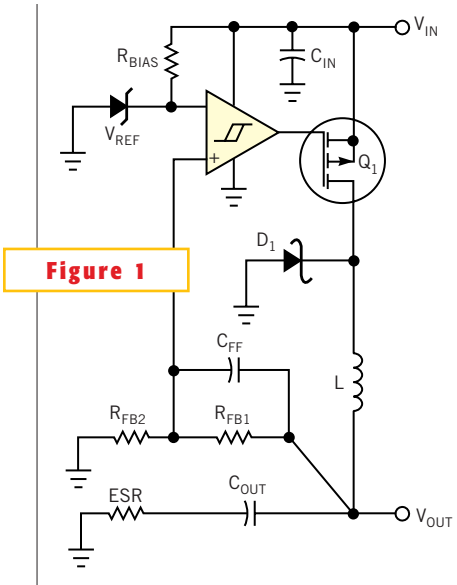
As an example of a Moore machine, consider a phototimer, which automatically lights a lamp for a given time when it becomes dark. After that time expires, it switches off the lamp and waits for the next night to repeat the process (**Figure 2**). The design uses an eight-pin Motorola (www.motorola.com) MC68HC908QT2 microcontroller; **Listing 1** at www.edn.com shows the program code. The photocell determines the Moore machine's input signal. The threshold of darkness is equal to 1.6V, which corresponds to a value of 52H after built-in analog-to-digital conversion. The sensitive triac, Q_1, model L2004F31 from Teccor (www.teccor.com) activates the lamp. The triac needs a gate current of 3 mA from the microcontroller can drive load current as high as 4A rms at a maximum voltage of 200V. The two LEDs with built-in resistor, LTL-4231T-R1s from LiteOn (www.liteon.com), indicate a current state in binary code. Thus, the Moore machine has two outputs—the lamp and the state indicator—both of which the Port A setting determines. The delays occur at 2 sec for states 1 and 3, and 4 minutes for state 2. In a real project, you can set any delay, even several hours or days. The delay affects only the complexity of the timer-interrupt routine. You can download the program code in **Listing 1** from the Web version of this Design Idea at www.edn.com.□

Hysteretic regulators provide high performance at low cost

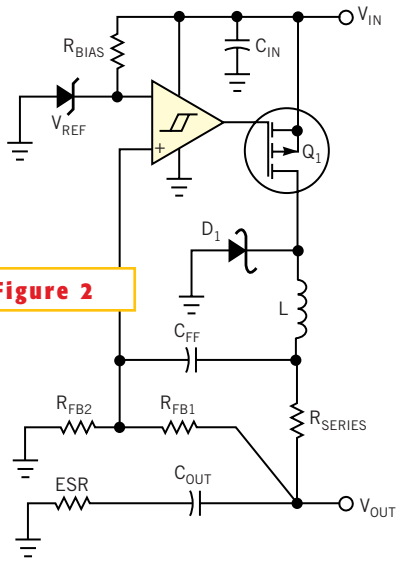
Wayne Rewinkel, National Semiconductor, Phoenix, AZ

Hysteretic voltage regulators offer the potential advantages of simplicity, fast response, 100%-duty-cycle operation, high efficiency at light loading, and low cost. They need no loop-compensation components to add delays; thus, response time to a load change is less than one switching cycle. What's the catch? You must be able to accept a switching frequency that is not precisely controlled and a sensitivity to noise that requires layout skill.

Figure 1 shows a simple hysteretic switching regulator made from a comparator with a fixed hysteresis and a PFET. The comparator switches on the PFET whenever V_{OUT} falls to its low threshold and off again when V_{OUT} rises to its high threshold. The time V_{OUT} lingers between the thresholds determines the on-time and, hence, the switching frequency. The inductor's ripple current flowing through the ESR of C_{OUT} provides a triangular voltage-ripple waveform, which produces predictable operation.



This hysteretic regulator suffers from unpredictability of the switching frequency because of C_{OUT} ESR variance.



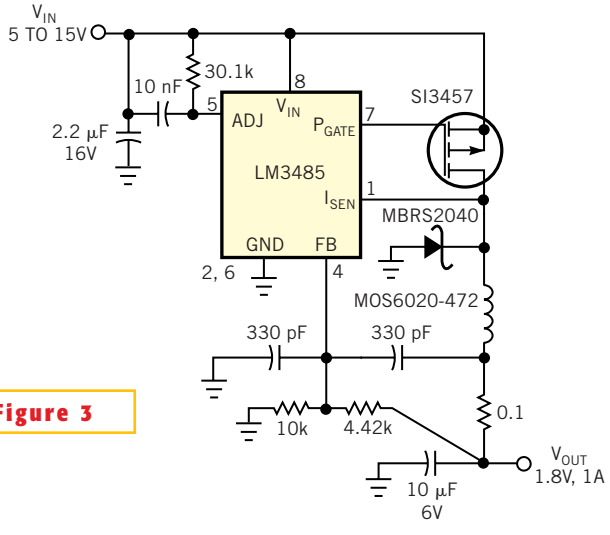
An added series resistor makes this circuit's switching frequency more predictable.

Herein lies a potential problem with simple circuits of this type. ESR is a major factor in determining switching frequency, and ESR can vary over a wide range for any given capacitor type. This variance is seldom a good thing and can lead to inductor saturation if the frequency falls too low or FET overheating arising from switching losses if the frequency rises too high. A simple solution to the ESR-variance problem is to use a ceramic C_{OUT} capacitor in series with a resistor. Although this technique works nicely in the lab, it often poses problems in the real world, in which several ceramic capacitors bypass loads.

Another approach to predictable frequency control allows the use of low-ESR capacitors (**Figure 2**). It is almost identical to **Figure 1**'s circuit except for the added resistor, R_{SERIES}, and the new connection point for C_{FF}. The inductor's ripple current induces the ac voltage present across R_{SERIES} and connects to comparator by C_{FF}. This controlled ac voltage eliminates the need for any C_{OUT} ESR. The feedback loop eliminates the dc voltage drop that R_{SERIES} creates. This new configuration produces predictable switching frequency with even zero-ESR capacitors and offers the potential of nearly zero V_{OUT} ripple at the cost of a resistor and the small added dissipation of R_{SERIES} carrying full load current.

The following equation approximates the switching frequency for either circuit, provided that C_{OUT}'s reactance at the switching frequency is lower than the ESR and C_{FF}'s reactance is much lower than R_{FB1}: $F_S=(V_{OUT}/V_{IN})(V_{IN}-V_{OUT})\times ESR/(V_{HYST}\times L+2ESR\times T_{PD}(V_{IN}-V_{OUT}))$, where ESR is the sum of C_{OUT}'s ESR and R_{SERIES}, V_{HYST} is the comparator's hysteresis voltage, and T_{PD} is the average propagation delay of the comparator plus the PFET.

You can build the circuits of **figures 1** and **2** as drawn, using a comparator, such



This circuit occupies an area smaller than a postage stamp.

as the LMV7219, which claims 7.5-mV built-in hysteresis, or by using a controller, such as the LM3485, which provides a current-limiting feature, wider V_{IN} range, and lower cost. You cannot overemphasize the layout sensitivity for hysteretic regulators. You cannot allow the feedback connection to pick up any stray signals. Open-core inductors are attractive for cost reasons but difficult to use, because any induced voltages from stray magnetic fields can produce unpredictable switching frequencies and ripple.

You can build the circuit in **Figure 3** in an area smaller than a postage stamp. This circuit produces output current of at least 1A, using small ceramic capacitors, a SOT-6 PFET, a 6×7-mm inductor, and an SMB-package, surface-mount Schottky diode. F_S varies from 600 to 700 kHz over a V_{IN} range of 5 to 15V for V_{OUT}=1.8V and V_{OUT} ripple less than 5 mV p-p. The 30.1-kΩ resistor and the PFET's on-resistance of 0.1Ω set the current limit to trigger at 1.5A. The no-load bias current is lower than 500 µA. Most impressive is the dynamic V_{OUT} change of only 10 mV for a load transient greater than 0.5A.□

Power-supply IC drives multiple LEDs

John Lo Giudice and Vee Shing Wong, STMicroelectronics, Schaumburg, IL

Bright LEDs are becoming prominent sources of light. They often have better efficiency and reliability than do conventional light sources. Although LEDs can operate from an energy source as simple as a battery and a resistor, driving a string of LEDs in constant-current mode can better match the luminance between the devices without needing to match LEDs for their forward-voltage drop. A switching supply also gives better efficiency than methods using a linear ballast resistor to limit the current.

The circuit in **Figure 1** uses IC_1, the integrated offline Viper22A switching regulator in a constant-current configuration to drive two to eight 1W LEDs. The circuit operates by monitoring the voltage drop across the sense resistor, R_6, and uses this voltage as feedback to regulate the current through R_6 and the LEDs. An operational amplifier in the TSM103, IC_2, monitors the voltage drop across R_{SENSE} and compares it with the 0.175V reference, which resistor divider R_5-R_7 sets, and closes the loop to maintain a 0.175V drop across the sense resistor. The output of the TSM103 drives the optocoupler, IC_3, which transfers the feedback to the Viper22A on the primary side. **Figures 2a**, **2b**, and **2c** show the completed board and the top and bottom layouts.

The LED's drive current is $I_{OUT}=V_5/R_6$, where V_5 is the voltage at Pin 5 of IC_2. You could easily modify the circuit to drive 3 or 5W LEDs, as long as you respect the maximum power rating, by simply changing the sense resistor to set a higher current value. When you design a con-

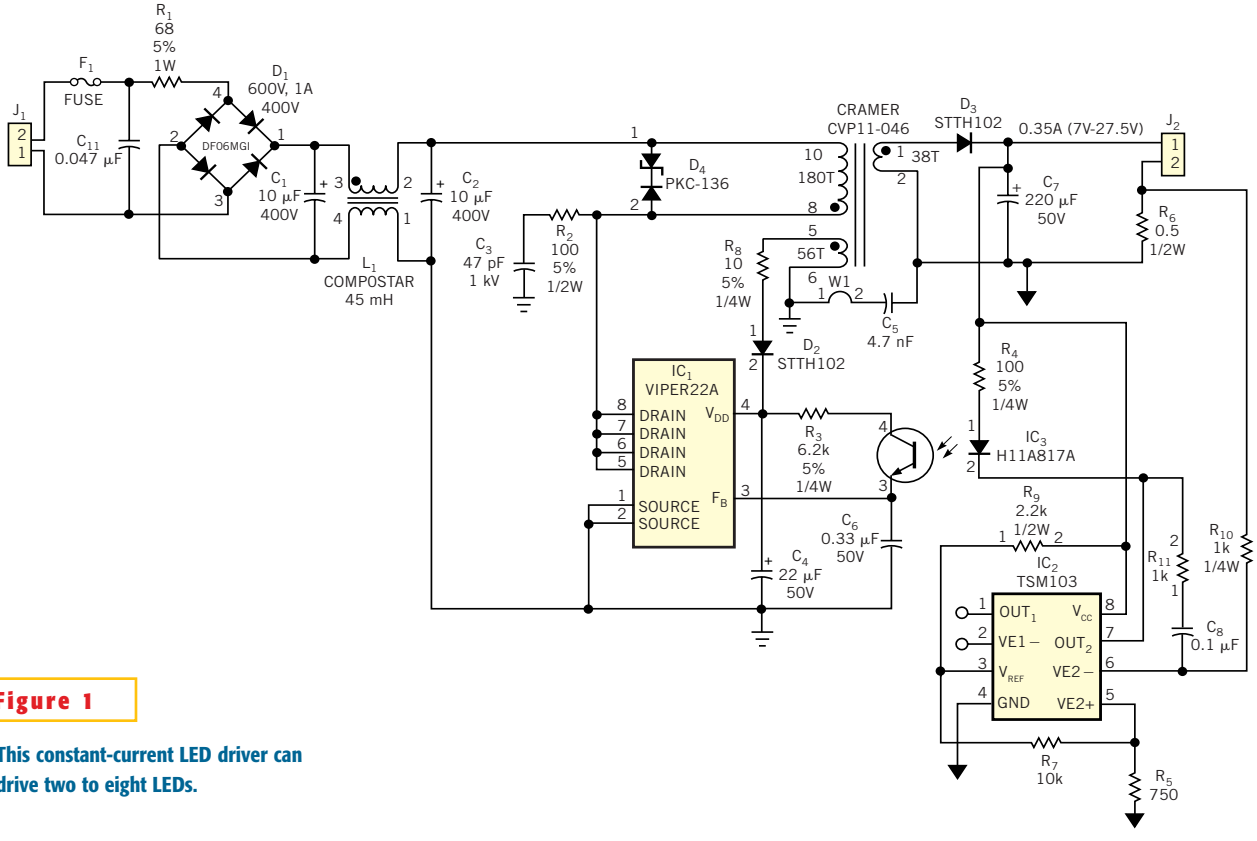


Figure 1

This constant-current LED driver can drive two to eight LEDs.

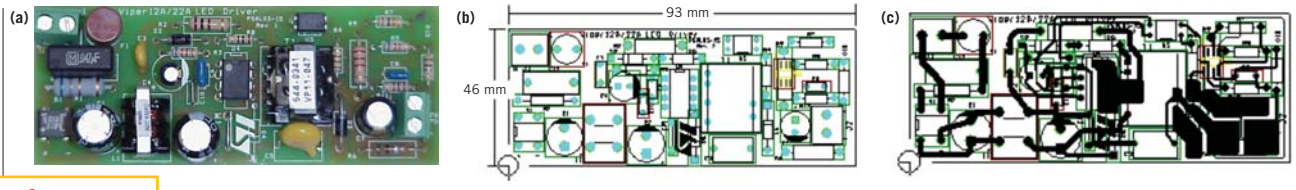


Figure 2 These photos show the completed board (a) and the top (b) and bottom (c) layouts.

stant-current power supply, the design of the transformer and the operating limitations of the circuit directly determine the output-voltage compliance of the constant-current source. For a design that can drive two to eight LEDs in series, the voltage drop across the LEDs can vary from approximately 7V for two LEDs to 28V for eight LEDs. This output voltage reflects back across the transformer and in turn changes the V_{DD} voltage to the control circuit and the peak V_{DS} across the power MOSFET.

The designers of the transformer in this application considered three limiting factors: the allowable V_{DD} for the Viper22, which has a range of 9 to 38V for the undervoltage and overvoltage thresholds, respectively; the maximum wattage of 12W for the Viper22A; and the fact that the reflected voltage across the drain of the MOSFET, which takes account of the turns ratio $[(N_P/N_S)V_{OUT}]$, added to the input voltage, must be less than 730V.

For a design that can drive two to eight LEDs, you must design the system taking into account the fact that the reflected voltage on V_{DD} is proportional to the output voltage. To keep the reflected voltage manageable, the transformer's design uses a turns ratio of primary to secondary output voltage for the maximum number of LEDs. Using these criteria, as the number of LEDs decreases, so does the reflected voltage. If you base the transformer on two LEDs, then the reflected voltage quadruples with eight LEDs and may exceed the rating of the Viper. The turns ratio between secondary to the V_{DD} winding is set for an output voltage of two LEDs to the minimum V_{DD} voltage of 9V. As you add LEDs, V_{DD} increases proportionally until it reaches the overvoltage-shutdown point of 42V nominal.□

Supercapacitor boosts current from small battery

Yongping Xia, Navcom Technology, Torrance, CA

Some battery-powered devices require large amounts of current in a short period of time but spend most of the time in sleep (power-down) mode. The momentary large-load current demands large batteries to meet the time requirement, even though the average current consumption is low. For instance, a system operates for 1.5 sec every 10 hours and needs 500 mA at 3.3V during the operation. Although the average current is only 21 µA, small, "coin" batteries cannot drive such a heavy load.

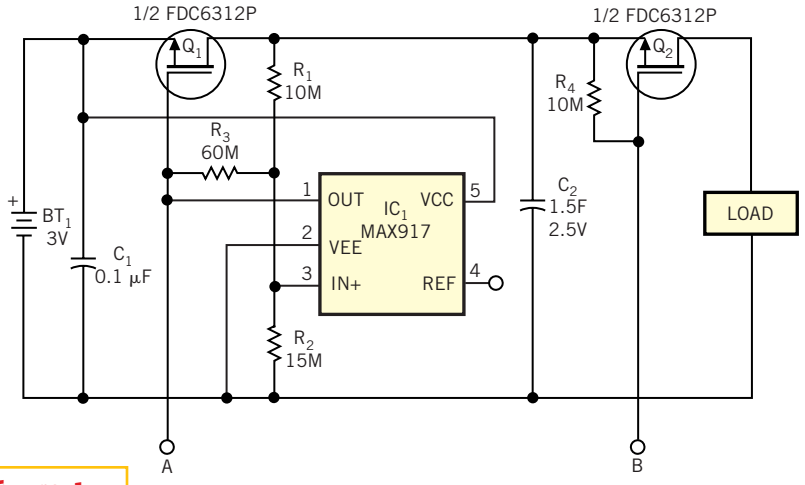
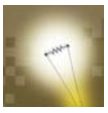


Figure 1 A supercapacitor helps a small battery to deliver large pulses of energy.

To eliminate the need for larger batteries, the circuit in **Figure 1** solves the problem by gradually building up energy in a supercapacitor. The device releases the energy when it is needed. Because the supercapacitor has low internal impedance, the momentary current can easily exceed several amperes.

Because a coin-type lithium battery delivers 3V and the supercapacitor's rated voltage is 2.5V, the circuit uses a voltage-controlled switch to cut off the battery once the voltage on the supercapacitor reaches 2.2V. This design uses a 1.5F, 2.5V supercapacitor from PowerStor (www.powerstor.com), model A10-30-2R5155. IC_1, a micropower voltage comparator with built-in 1.245V reference, senses the voltage on the supercapacitor. R_3 provides 0.5V hysteresis to the comparator. When the voltage is lower than 1.7V, the comparator's output is low and thus turns on the p-channel MOSFET, Q_1. The battery charges the supercapacitor. Once the voltage on the supercapacitor reaches 2.2V, the comparator switches high to shut off Q_1. You could use this low-to-high transition at Point A as a battery-charge-complete indicator or to trigger another device, such as a microcontroller's interrupt line.

Q_2, another p-channel MOSFET, controls the discharge of the supercapacitor. When Point B is floating, the switch is off. When an open-drain or open-collector device pulls down Point B, the switch is on. Because the voltage on the supercapacitor continuously drops when the switch is on, you can use a boost dc/dc converter to generate a constant output voltage. Select a boost converter with the lowest possible working input voltage to obtain the maximum energy from the supercapacitor. For example, you can use an LTC3402 to generate a stable 3.3V output. Once it starts, the LTC3402 can work with input voltages as low as 0.5V. The energy from the supercapacitor is $1/2V^2C$, or $1/2[(2.2V)^2\times 1.5F-(0.5V)^2\times 1.5F]=3.4J$.□



Edited by Bill Travis

Slow diodes or handy timing devices?

Louis Vlemincq, Belgacom, Evere, Belgium

Most designers consider slowness in diodes to be an imperfection or a limitation. Why not take a more positive view of the situation? After all, a zener or an avalanche diode is no more than a diode with a limited breakdown voltage, and you can view a varactor as a diode with a large and nonlinear parasitic capacitance. Similarly, could you view the slowness of a diode as a property or even a feature? For example, consider a PIN diode. Few people are aware that the key property of a PIN diode is indeed its slowness; without it, it would generate large amounts of distortion and require a larger control current to function properly. You can put this ability of slow diodes to store large amounts of electrical charge to good use in a variety of other circuits. **Figure 1** shows how to generate dead time using such diodes. A PWM sandcastle (stepped) waveform feeds a half-bridge.

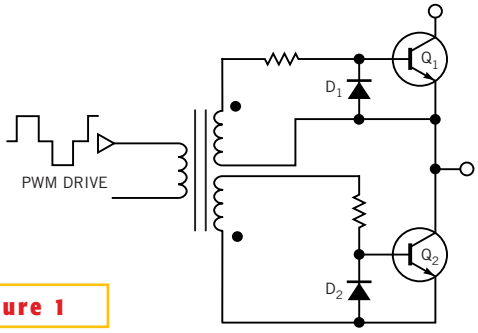


Figure 1 You can use slow diodes to generate dead time in a half-bridge configuration.

In a classical implementation, you must insert dead time in the control circuitry to avoid the simultaneous conduction of the two transistors when the duty cycle approaches 100%. This dead time is a standard feature of PWM-control ICs. If you use slow diodes for D_1 and D_2, you need no dead time. If, for example, Q_1 receives a positive base, or gate, drive and is therefore conducting, D_2 becomes forward-biased. When the control signal reverses its polarity, a negative bias appears immediately on Q_1, but D_2 cannot instantly cease conducting and short-circuits the base drive to Q_2 during all of its reverse recovery time. The advantage of generating a dead time in this way lies in the fact that you need include only a small safety margin: The phenomena governing the recovery time of a diode are similar to those resulting in storage times in power devices. In particular, they both display a strong positive-temperature coefficient, for which this scheme compensates. The ability to operate at duty cycles close to 100% allows a better usage of the power components, translating into savings and higher performance: A universal-input supply, for instance, can operate at lower supply voltages.

Figure 2 shows another example. This standard clamping circuit protects the switching transistor of a flyback converter against the voltage spike generated by the imperfect coupling between the primary and the secondary windings of the transformer. In an equivalent schematic, this scenario translates into a leakage inductance, L_F, in series with the primary winding. The circuit works in the following way: Each time the transistor turns off, the current in the leakage inductance continues to flow, but D_1 intercepts it and "redirects" it to C_1. C_1 has a large enough capacitance that cycle-to-cycle variations do not influence it. The average voltage on C_1 results from a balance between the charging input from the leakage inductance and the current that bleeds from R_1. Usually, D_1 is a fast diode, but, if you substitute it with a slow one, interesting things happen: Instead of switching off when the voltage on C_1 reaches its peak, D_1 continues to conduct, thus transferring back charge and energy from C_1 to the transformer and ultimately to the load. The overall efficiency is therefore better, and R_1 can have higher resistance and can be smaller. Added to the lower cost of a standard diode versus a fast one, the method provides non-negligible benefits.

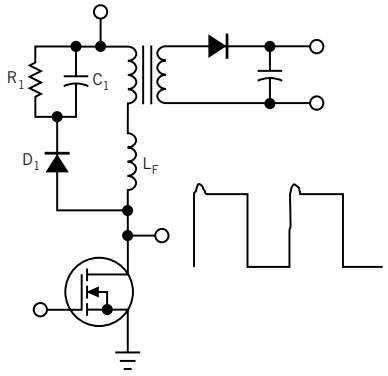


Figure 2 In this circuit, a slow diode protects the switching transistor from destructive voltage transients.

It is preferable to select a diode with a recovery time as long as possible. Popular types, such as the 1N400X series, have recovery times of approximately 2.5 µsec, but some models reach more than 5 µsec. Ideally, C_1 and L_F should resonate at a period equal to twice the diode's recovery

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time. When the component values are nearly optimum, R_1 can have a large value, its only role being to provide a "seed" current to prime the circuit. You pay a small penalty for these advantages: The peak clamping voltage increases by several volts, because you must add the positive cycle of the resonance to the average clamping voltage and because slow diodes often exhibit a slightly poorer forward-recovery characteristic than do their fast counterparts. This characteristic results in a step of several volts at the beginning of the conduction.

Normally, these small snags should pose no problem; you can substitute the new components in a design without any other change. The circuits in **figures 1** and **2** are only two examples, but you can apply the same useful principles to a variety of other circuits.□

Diode compensates distortion in amplifier stage

S Chekcheyev, Pridnestrovye State University, Moldova

The voltage amplifier in **Figure 1** exhibits smaller nonlinear distortion than does the conventional amplifier in **Figure 2**. Diode D_1 compensates for the distortion inherent in the npn transistor. The voltage gain of a common-emitter amplifier depends on the transconductance of the transistor. The transconductance of the bipolar transistor is as follows:

$$S = \frac{eI}{k(273 + T°C)} = nI,$$

where e is the charge of an electron, k is Boltzmann's constant (approximately 1.38×10^{-23}J/°K), T°C is temperature in degrees Celsius, I is the emitter current, and $n=e/[k(273+T°C)]$. So, the transconductance is proportional to the emitter current. Consequently, the instantaneous voltage-gain coefficient of the conventional common-emitter amplifier is proportional to the instantaneous emitter current. As a result, the negative half-cycle of the output signal gets more amplification than does the positive half-cycle (**Figure 3**).

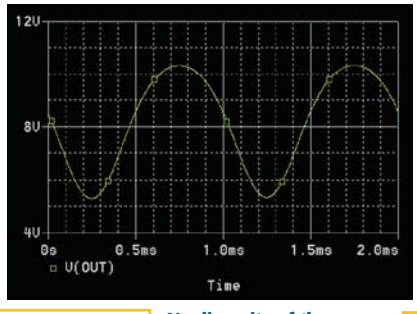

Figure 3 Nonlinearity of the transconductance of Q_1 results in this distorted waveform.

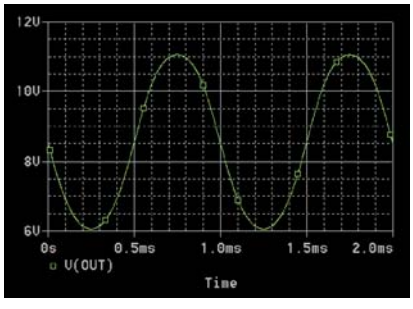

Figure 4 The diode in the circuit of Figure 1 produces varying, beneficial, negative feedback.

The dynamic resistance of diode D_1 in **Figure 1** is inversely proportional to the instantaneous current. That dynamic resistance forms part of the negative-feedback circuit of the amplifier. The average current of diode D_1 is equal to the average emitter current of transistor Q_1. However, the instantaneous current of D_1 becomes smaller, and the instantaneous dynamic resistance of D_1 becomes larger when the instantaneous emitter current of Q_1 becomes larger, and vice versa. Therefore, the negative feedback becomes stronger during the negative half-cycle of the output signal. As a result, the output signal of the amplifier becomes more symmetric (**Figure 4**). The circuits in **figures 1** and **2** have the same average collector current and the same load resistance**. Figures 3** and **4** show the results of their PSpice simulation. The amplitude of the output signal is 5V p-p in both cases with a 1-kHz sinusoidal signal applied to the input. You can see that the linearized amplifier yields a more symmetrical output signal. **Figure 5** gives the quantitative results of the simulations. The improvement in harmonic distortion accrues because of the suppression of the even harmonics in the output of the linearized amplifier.□

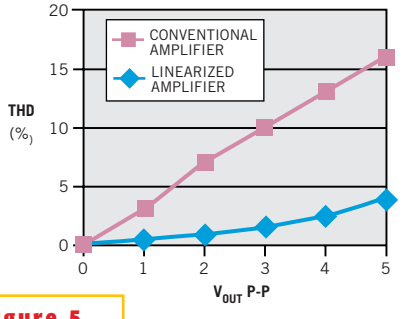

Figure 5 The linearized amplifier produces less than one-third the harmonic distortion of the conventional amplifier.

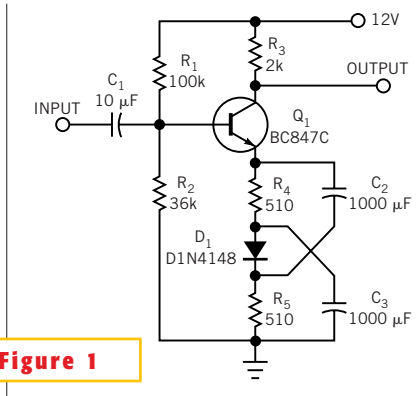

Figure 1 The addition of a simple diode in the emitter circuit yields the symmetric waveform of Figure 4.

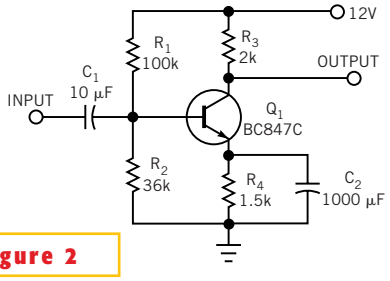

Figure 2 This amplifier circuit produces the distorted waveform of Figure 3.

Transistors offer overload delay

Christophe Basso, On Semiconductor, Toulouse, France

Although an SMPS (switch-mode power supply) can protect itself against permanent short circuits, it sometimes has problems when dealing with transient overloads. Transient overloads are not short circuits but can push the power supply above its nominal load value. This scenario occurs with typical loads such as printer heads and small motors. When facing such a load profile, the power supply can easily trigger its protection circuit, especially if the open-loop gain is high. You will see any decrease in the output voltage on the primary side as a loss of feedback current, because the controller cannot keep the voltage constant.

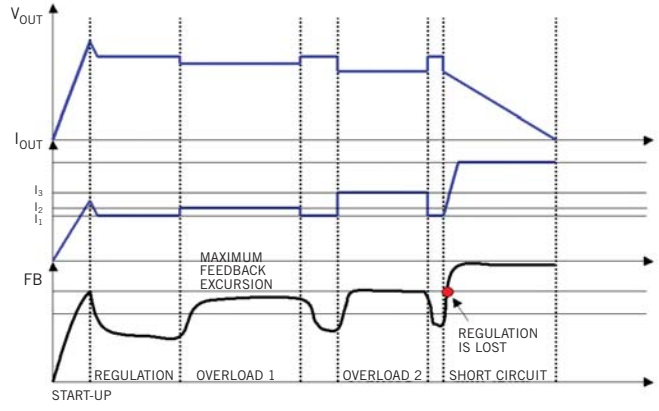

Figure 1 Overloads and short circuits can be similar in this typical power profile for a printer.

Figure 1 shows a typical power profile for a printer. You can clearly see the power variations and the corresponding feedback-voltage swings that occur. The start-up sequence is a short circuit because, with V_{OUT} far from its target, the feedback current is not yet established. The nominal output current, I_1, corresponds to the regulation zone, in which the load is constant. When a first overload occurs (I_2 in **Figure 1**), the feedback pin pushes the primary-current setpoint (in a current-mode controller), but the waveform's excursion starts to diminish, because it is approaching its maximum level. In I_3, the power supply has difficulty remaining in regulation and, in short-circuit condition, V_{OUT} collapses to ground. If the primary PWM controller has a simple short-circuit-protection scheme, the protection mechanism can trigger in the overload zones 1 and 2, whereas it should trigger only in the final one. **Figure 2** portrays an approach based on the NCP1200 from On Semiconductor (www.onsemi.com).

This circuit permanently monitors the feedback line (Pin 2) to detect whether a short circuit is present on the secondary side. If so, Pin 2 jumps to its internal pullup voltage and triggers a protective burst mode. Note that this protection acts independently of any badly coupled auxiliary level, because the high-voltage source (Pin 8) directly powers the controller. In the presence of overloads 1 and 2, Pin 2 would jump to the maximum of its capability and would trigger the protection. This circuit does not delay the rise of the feedback voltage but momentarily increases the output-power level by a given percentage. When I_{OUT} is within regulation, Pin 2 is below 3V and D_1 is not biased. As a result, Q_2 is blocked and Q_1 pulls R_3's lower terminal to ground. The current-sense pin therefore sees a current image, which the voltage-divider ratio of R_2 and R_3 affects.

In this example, $V_{PIN4} = V_{SENSE} \times R_3/(R_3+R_2) = 0.82 \times V_{SENSE}$, where V_{SENSE} is the voltage across R_{SENSE}. If the NCP1200 imposes a maximum-current setpoint of 1V, the IC authorizes 1.2V over R_{SENSE} as long as Q_1 is biased (instead of 1V in a regular configuration). As soon as Pin 2 jumps to a higher value, such as 4V, indicating a loss of regulation or a severe overload, D_1

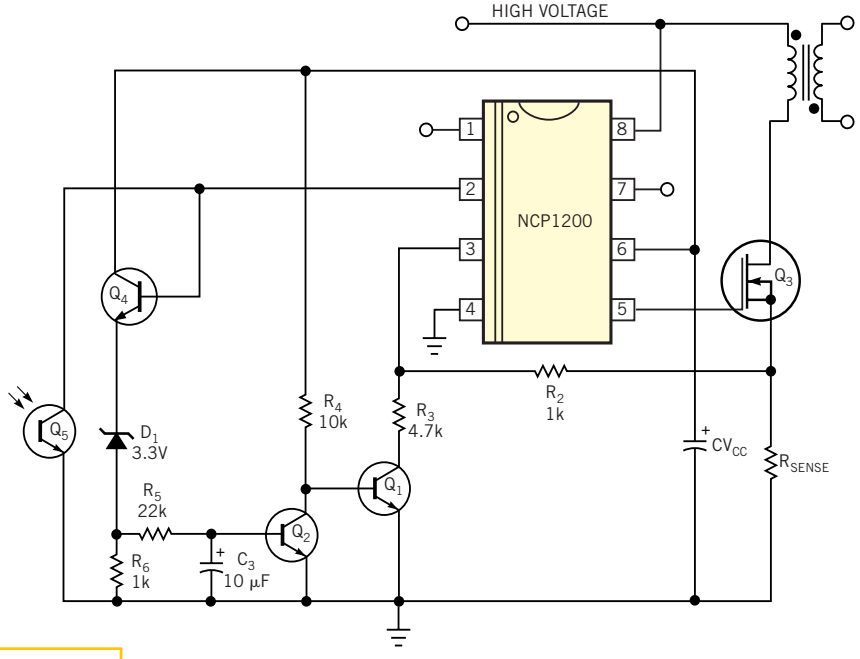

Figure 2 A transistor network increases the peak current for a moment until the power supply gives up by reducing the peak setpoint.

starts to conduct via Q_4.This transistor buffers the feedback-pin impedance: C_3 starts to charge up via R_5, and, when it reaches approximately 0.7V at 25°C, Q_1 opens. The divider goes away, the power supply no longer ensures a large peak current, and V_{OUT} goes down, thereby properly triggering the protection. As result, by dimensioning the R_5 and C_3 elements, you can insert a delay to enable the supply to cope with transient loads.□

Inertial-navigation system uses silicon sensors

Tom Niemi, Rockwell Collins, Cedar Rapids, IA

A STRAP-DOWN inertial-navigation system uses silicon sensors to measure displacement without entailing the bulk and expense of moving parts or GPS receivers. For example, a three-axis accelerometer and three angular-rate sensors can determine the position and velocity of a vehicle such as a robot or radio-controlled aircraft. This hardware configuration requires that you read and integrate the sensor outputs and then combine and process them to obtain stabilized location values. **Figure 1** shows one such complete system. An inexpensive 8-bit microcontroller can handle the sensor reading and integration tasks, and perform simple lowpass filtering of the accelerometer's output to remove conversion noise. The microcontroller can even run a basic position and velocity algorithm; alternatively, you can pass the preprocessed data to a DSP system. The NEC (www.necelam.com) μPD78F9418A microcontroller has seven ADC inputs, so it can handle the six inputs from the sensors.

Because a Crossbow (www.crossbow.com) CXL04M3 accelerometer delivers 0.5V/g (9.8m/sec^2), it can directly feed three of the microcontroller's ADC inputs. Each NEC/Tokin CG-16D angular-rate sensor generates only 1.1 mV/°/sec, so it requires the aid of an instrumentation amplifier. The Burr-Brown (www.ti.com) INA118 fills the bill. The microcontroller has enough I/O lines to drive three Varitronix (www.varitronix.com) VIM-503 41/2-digit LCDs that display the x, y, and z location relative to the starting point. One of the fundamental tasks in this application is to initialize the sensors and A/D converters to minimize bias error. **Listing 1** at the Web version of this Design Idea at www.edn.com shows the code to calibrate the accelerometer. The routine calculates the average value of the accelerometer's outputs over 1000 samples and uses this information to calculate bias-error adjustments for each axis. You apply each bias value by adding it to the readings for that axis. Using the x axis as an example, you determine the vehicle's movement from its starting point by integrating: Multiply the x-axis reading by the time squared, halve that quantity, and then add the result and the bias value to the previous x position. You find velocity by multiplying the bias-corrected x-axis reading by the time and then adding it to the previous x velocity. You can download the microcontroller code from the Web version of this Design Idea at www.edn.com.□

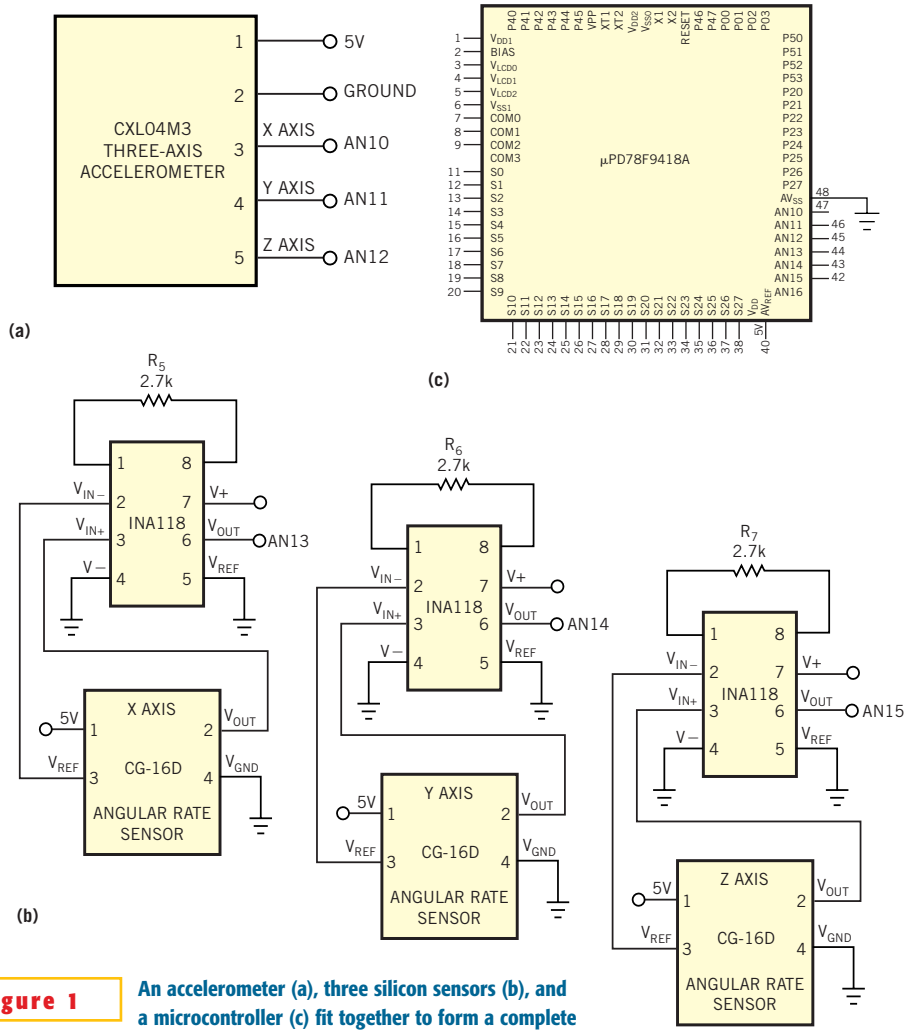

Figure 1 An accelerometer (a), three silicon sensors (b), and a microcontroller (c) fit together to form a complete inertial-navigation system.

LED driver provides oscillator for microcontroller

Wallace Ly, National Semiconductor, Santa Clara, CA

The major building blocks for a white-LED driver are an oscillator, a charge pump, and a regulated current source. National Semiconductor (www.national.com) produces a device that contains all these building blocks in the highly integrated LM2791/2 IC. You usually use white-LED drivers in tandem with cellular baseband controllers or microcontrollers. You can easily adapt the LM2791/2 to provide a clock source. You can realize a simple yet useful circuit by accounting for the fact that a pseudo square wave is present across the flying capacitor's (C_1) pins. You can take this pseudo square wave from these pins and clean it up.

To accomplish this task, you inject the signal, via a 330Ω resistor, R_1, into a simple inverter gate, such as a DM7404 hex inverter (**Figure 1**). The net signal is a clean, 2-MHz clock source. The oscilloscope graph depicts the pseudo square wave and the resultant square wave at the output of the inverters (**Figure 2**). You can use this signal as a simple clock source for a baseband controller or microcontroller to perform simple tasks such as keypad decoding or battery-identification detection.□

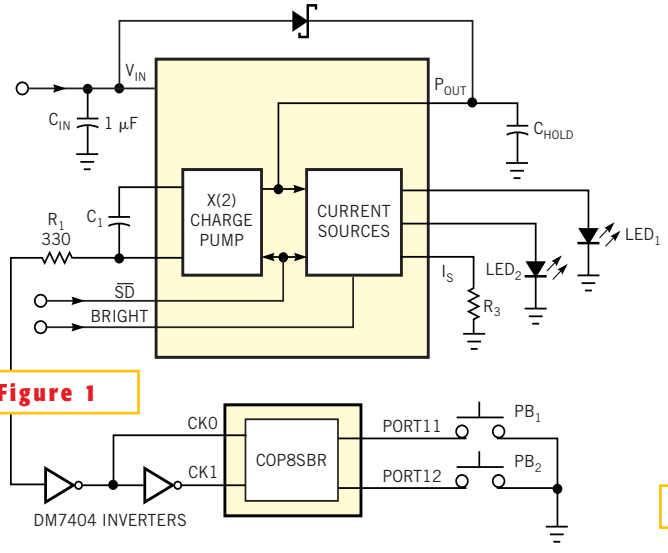

Figure 1

A white-LED driver doubles as a clocking source for a microcontroller.

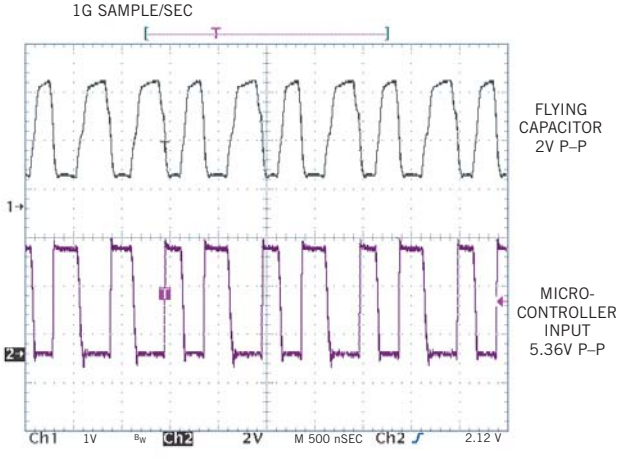

Figure 2

A logic inverter cleans up the pseudo square wave (top) from the flying capacitor; the result (bottom) is a stable clock source for the microcontroller.

Use op-amp injection for Bode analysis

Martin Galinski, Micrel Semiconductor, San Jose, CA

Bode analysis is an excellent way to measure small-signal stability and loop response in power-supply designs. Bode analysis monitors gain and phase of a control loop. It performs this monitoring by breaking the feedback loop and injecting a signal into the feedback node and then comparing the injected signal with the output signal of the control loop. The method requires a network analyzer to sweep the frequency and compare the injected signal with the output signal. The most common method of injection is the use of transformer. **Figure 1** demonstrates how a transformer injects a signal into the feedback network. A 50Ω resistor affords impedance matching to the network-analyzer source. This method allows the dc loop to maintain regulation and allows the network analyzer to insert an ac signal on the dc voltage. The network analyzer then sweeps the source while monitoring A (voltage channel) and R (reference channel) for an A/R-ratio measurement. Although this method is

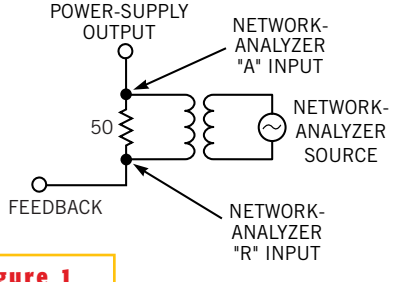

Figure 1

Bode analysis using transformer injection yields gain and phase information in a control loop.

the most common for measuring the gain and phase of a power supply, it has significant limitations. First, to measure low-frequency gain and phase, the transformer needs high inductance. Frequencies lower than 100 Hz, therefore, require a large and expensive transformer.

Also, the transformer must be able to inject high frequencies. Transformers with these wide frequency ranges generally are custom-made and usually cost several hundred dollars. By using an op amp, you can avoid the cost and frequency limitations of an injection transformer. **Figure 2** demonstrates the use of an op amp in a summing- amplifier configuration for signal injection. R_1 and R_2 reduce the dc voltage from the output to the noninverting input by half. The network analyzer is generally a 50Ω source. R_1 and R_2 also divide the ac signal from the network analyzer by half. These two signals "sum" together at half their original input. The output then gains up by a factor of two by R_3 and R_4 and goes to the feedback output. (The 50Ω resistor balances the network analyzer's source impedance.) This action essentially breaks the loop and injects the ac signal on top of the dc output voltage and sends it to the feedback terminal. By monitoring the feedback terminal (R) and output terminal (A), the analyzer measures gain and phase. This method has no minimum frequency. Make sure that the bandwidth of the op amp is much greater than the expected bandwidth of the power supply's control loop. An op amp with at least 100-MHz bandwidth is more than adequate for most linear and switching power supplies.□

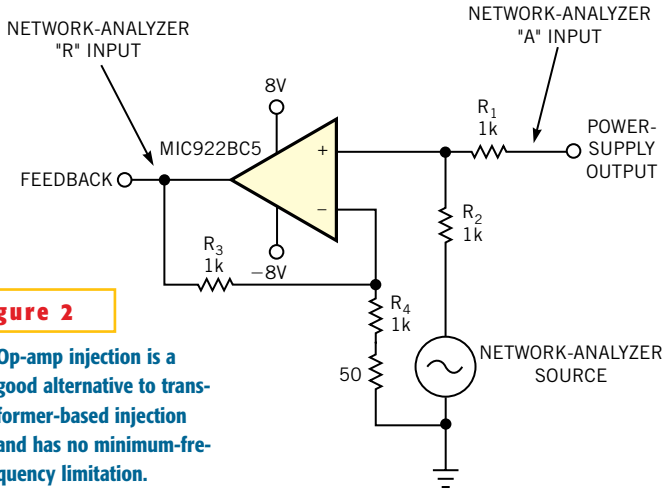

Figure 2

Op-amp injection is a good alternative to transformer-based injection and has no minimum-frequency limitation.

Edited by Bill Travis

Combine two 8-bit outputs to make one 16-bit DAC

Steve Woodward, Chapel Hill, NC

Inexpensive, 16-bit, monolithic DACs can serve almost all applications. However, some applications require unconventional approaches. This Design Idea design concerns circuitry I recently designed for a tunable-diode laser spectrometer for a Mars-exploration application. The control circuitry included two 16-bit DACs that interface to the radiation-hardened, 8051-variant 69RH051A microcontroller. Because of the intended space-flight-qualified specification, everything in the design had to consist solely of components from the NPSL (NASA parts-selection list). This restriction posed a challenge, because, at design finalization, the NPSL included no appropriate, flight-qualified, 16-bit DACs, and the budget included no funds for certification of new devices. I escaped from this impasse by exploiting two fortuitous facts: The update rate of the two DACs was only tens of hertz, and the 69RH051A had a number of uncommitted, 8-bit, 14.5-kHz PWM outputs. These outputs made one 16-bit DAC; a second pair of PWM bits and an identical circuit made the other (**Figure 1**).

Hex inverter IC_1's V_{CC} rail connects to a precision 5V reference. The inverter's outputs are accurate analog square waves. The low-order PWM-signal output, PWM0, of the 8051 controls the V_3 square wave, and the high-order PWM output, PWM1, controls the V_1 square wave. R_2 and R_6 passively sum the two square waves in the ratio $R_2/R_6 = 3290/1$ million $= 1/255$ to produce V_4, duplicating the 2^8 ratio of the 16-bit sum. This action makes the dc component of V_4 equal to $5V(REF)(PWM0 + 255PWM1)/256$. Thus, if you write the 0 to 255, high-order byte of a 0 to 65,535, 16-bit DAC setting to the CEX1 register of the 8051 and write the 0 to 255, low-order byte to CEX0, a corresponding 16-bit analog representation appears in the dc component of V_4. The accuracy of the R_2-to-R_6 ratio is the only limit on the monotonicity and accuracy of this circuit. For example, one part in 25,500 = 14.5 bits for 1%-tolerance R_2 and R_6 and a full 16 bits for 0.3% tolerance or better. But the story doesn't end there. Two problems remain.

The first problem is the extraction of V_4's desired dc component from all—or

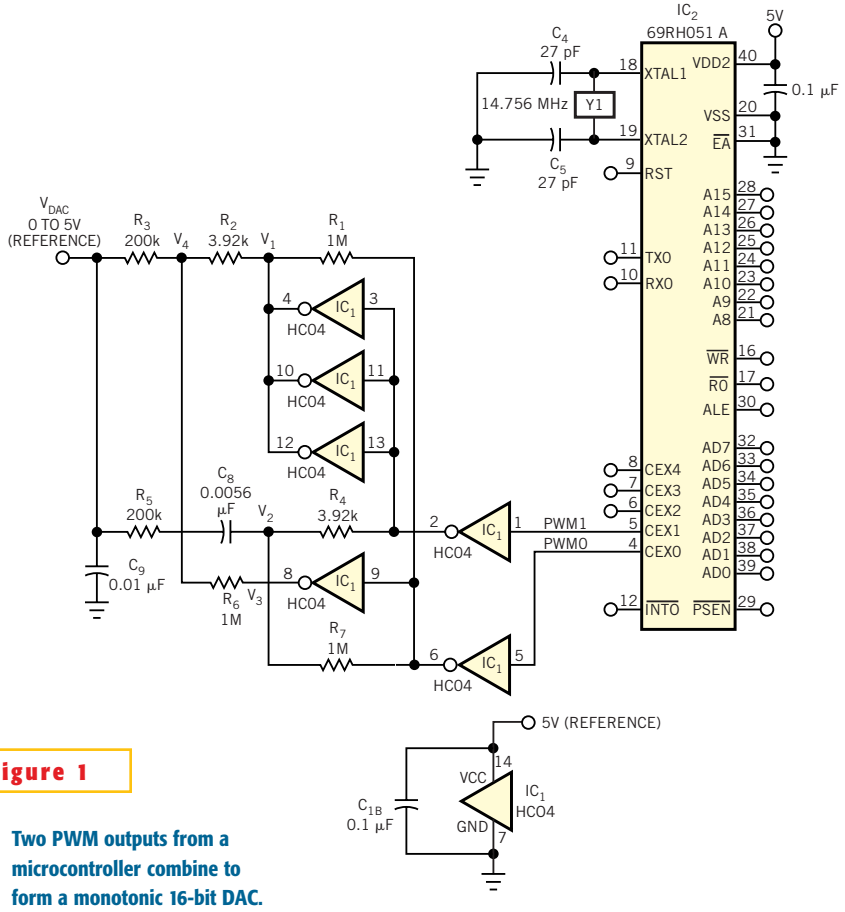

Figure 1

Two PWM outputs from a microcontroller combine to form a monotonic 16-bit DAC.

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at least 15 or 16 bits=99.995%—of the undesired square-wave ac ripple. The R_3-C_9 lowpass filter does some of this work. If you make C_9 large enough, in principle, the filter could do the whole job. The reason this simple approach wouldn't work is that, to get such a large ripple attenuation of approximately 90 dB with a single-stage RC filter would require an approximately 300-msec time constant and a resultant 3-sec, 16-bit settling time. This glacial response time would be too slow even for this undemanding application. To speed things, the R_4, R_5, R_7, C_8 network synthesizes and then sums V_2: an inverse-polarity duplicate of V_4's 14.5-kHz ac component. This summation actively nulls out approximately 99% of the ripple. This nullifying action leaves such a small residue that an approximately 2-msec and, therefore, approximately 25-msec-settling-time R_3C_9 product easily erases it.

The other problem is compensation for the low, but still nonzero, on-resistance of the HC14 internal CMOS switches, so that the resistance doesn't perturb the critical R_2-to-R_6 ratio. This issue is of no particular concern for R_6, because the R_6-to-on-resistance ratio is greater than 10,000-to-1, making any associated error negligible. This situation is not the case for R_2, however, in which, despite the triple-parallel gates, the R_2-to-on-resistance ratio is approximately 300-to-1, which is small enough to merit attention. Load-cancellation resistor R_1 provides such attention. R_1 sums a current into the R_2 driving node that, because it is equal in magnitude but opposite in phase to the current through R_6, effectively cancels the load on the R_2 drivers. This process makes the combined on-resistance approximately 100 times less important than it otherwise would be. The result is a simple, highly linear and accurate voltage-output DAC with a respectable, if not blazingly fast, settling time of approximately 25 msec. And the most important result, in this case, was a parts list with an impeccable NPSL-compliant pedigree.□

LED driver provides software-controlled intensity

Neda Shahi and Bjorn Starmark, Maxim Integrated Products, Sunnyvale, CA

Recent advances in operating efficiency have expanded the use of LEDs from one of mere indicators to becoming driving forces in electronic lighting. Increased reliability and ruggedness (versus other lighting technologies) gives the LED a bright future indeed. Vendors in recent years have introduced many ICs for driving LEDs, but the problem of driving serial chains of LEDs has received less attention. One approach to that problem adapts a bias-supply IC for APDs (avalanche photodiodes) to provide adjustable-current, software shutdown, and logic indication of open-circuit faults (**Figure 1**). This design reconfigures the APD-bias IC, IC_1, to allow its low-voltage DAC output to modulate the high-voltage, current-sense feedback via a high-voltage-output transconductance stage comprising Q_2 and Q_3. These two complementary transistors provide first-order temperature-compensation sufficient for the application.

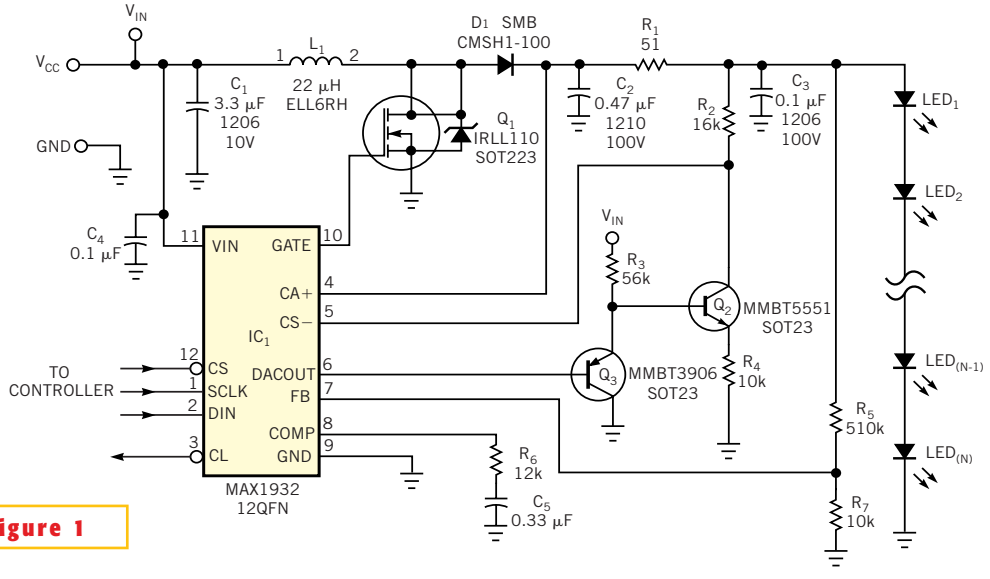


Figure 1 The APD driver, IC_1, provides high-voltage LED modules with software-adjustable intensity control.

Equations from the MAX1932 data sheet help you select components for the step-up dc/dc converter. The current-adjustment transfer function is:

$$I_{OUT} = \frac{V_{CL} - \frac{CODE \times 1.25V}{256} \times \frac{R_2}{R_4}}{R_1},$$

where V_{CL} is the current-limit threshold (2V), CODE is the digital code to the DAC in decimal format, and I_{OUT} is the desired output current. For this circuit, these conditions correspond to a full-scale output of 39 mA and a resolution of 150 µA. The three-wire serial interface that controls IC_1 allows you to shut down IC_1 by writing code 00hex to the DAC. The circuit also provides an output-voltage limit. If an LED fails open, the R_5-R_7 divider limits the output voltage, in this case, to 50V. Simultaneously, the CL pin goes high to indicate the open-fault condition.□

Improve roll-off of Sallen-Key filter

Doug Glenn, Teledyne, Lewisburg, TN

The well-documented Sallen-Key active filter is a staple of analog design. This Design Idea shows a way to obtain better roll-off by adding just a few common passive components. **Figure 1a** shows a typical implementation of a three-pole, lowpass version. In operation, you adjust the ratio of capacitors C_1 and C_2 to give a peaked response for the two poles within the feedback loop. The peaked response compensates for the initial roll-off in the third pole formed by the R_3-C_3 section at the input. In **Figure 1b**, a twin-tee notch filter replaces the R_3-C_3 section at the input. The notch frequency, $F=1/(2\pi R_4C_4)$, is equal to approximately twice the desired cutoff frequency.

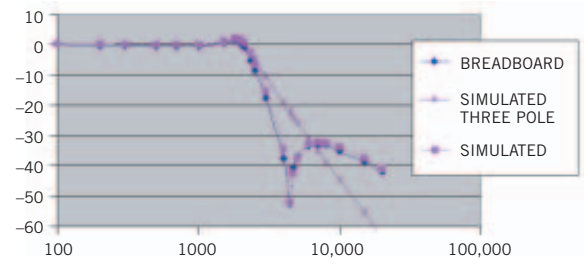


Figure 2 The improved cutoff rate of the filter results in a quasi-elliptical response.

Select a value for R_4 that's approximately one-third to one-fourth the value of R_1, and then adjust R_4 as needed to allow use of standard capacitor values. The graph in **Figure 2** shows the improvement in the cutoff rate of the filter; the result is a quasi-elliptic response. A breadboard of the circuit in **Figure 1b** uses 5% parts. The measured results show good agreement with the Spice simulation. To take advantage of the faster roll-off, just scale the frequency and impedance to your application. The highpass dual of this circuit works as well as the lowpass version.□

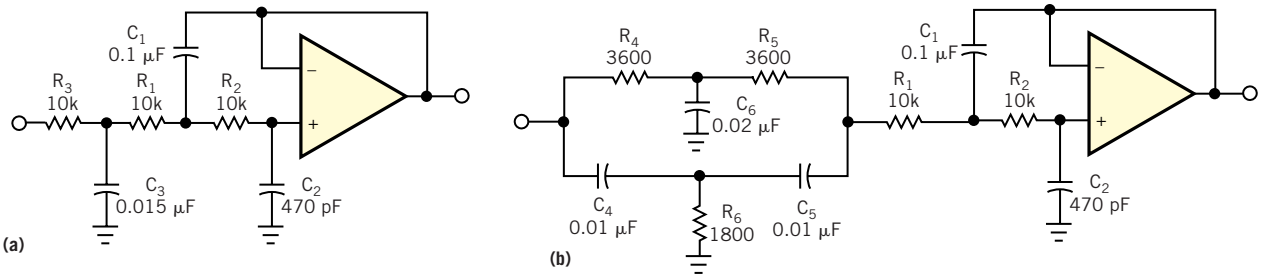


Figure 1 The addition of a twin-tee network (b) considerably improves the roll-off rate of the circuit (a).

AC-coupling instrumentation amplifier improves rejection range of differential dc input voltage

Francis Rodes, Olivier Chevalieras, and Eliane Garnier, ENSEIRB, Talence, France

The need for conditioning low-level ac signals in the presence of both common-mode noise and differential dc voltage prevails in many applications. In such situations, ac-coupling to instrumentation and difference amplifiers is mandatory to extract the ac signal and reject common-mode noise and differential dc voltage. This situation typically occurs in bioelectric-signal acquisition, in which metallic-electrode polarization produces a large random differential dc voltage, ranging from ±0.15V, which adds to low-level biological signals. Input ac-coupling is one approach to removing the differential dc content. But this technique requires adding a pair of capacitors and resistors to ac-couple the inputs of the difference amplifier. The manufacturing tolerances of these components severely degrade the CMRR (common-mode-rejection ratio) of the amplifier. If cost is not an issue, you could perform an initial trim, but this operation is useless for biological applications plagued by wide variations in electrodes and tissue impedances. The differential topology in **Figure 1** addresses these problems (**Reference 1**).

The principle of this ac-coupled instrumentation amplifier is to maintain the mean output voltage at 0V. To do so, you insert an autozero feedback loop, comprising IC_4, R_{FB}, and C_{FB}, in a classic three-op-amp instrumentation amplifier. This feedback loop produces a frequency-dependent transfer function:

$$\frac{V_{OUT}}{V_{IN1}-V_{IN2}}=\left(1+\frac{2R_2}{R_1}\right)\frac{jR_{FB}C_{FB}\omega}{1+jR_{FB}C_{FB}\omega}.$$

Consequently, the ac-coupled instrumentation amplifier behaves as a high-pass filter with a −3-dB cutoff frequen-

(continued on pg 92)

cy from the equation $f=1/2\pi R_{FB}C_{FB}$. At first glance, you might think that the output-autozeroing behavior of the ac-coupled instrumentation amplifier is perfect. Unfortunately, the output autozeroing capability of this circuit is strongly limited. You can determine this limitation by expressing the output voltage as a function of the input signals and the integrator's output voltage, V_Z: $V_{OUT}=(1+2R_2/R_1)(V_{IN1}-V_{IN2})+V_Z=A_D(V_{IN1}-V_{IN2})+V_Z$, where V_{OUT} is the output voltage. In this expression, $A_D=1+2R_2/R_1$ is the differential gain in the passband. At dc, the output voltage is 0V as long as the integrator's output does not reach its saturation voltage, $V_{Z(MAX)}$. Therefore, setting the output voltage at 0V in the above expression yields the maximum differential-input dc voltage that this circuit can handle:

$$\Delta V_{IN(MAX)}=(V_{IN1}-V_{IN2})(MAX)=\pm\frac{V_{Z(MAX)}}{\left(1+\frac{2R_2}{R_1}\right)}=\pm\frac{V_{Z(MAX)}}{A_D}.$$

Consider, for instance, the typical performance and constraints of a portable biotelemetry system: differential gain of 1000, ±5V split power supplies, and op amps with rail-to-rail output-voltage swing. In this system, the application of the formula for ΔV_{IN} yields a maximum differential-input dc voltage of only ±5 mV. This limited performance is unacceptable for biological applications, in which you encounter differential-input dc voltages of ±0.15V. The ac-coupled instrumentation amplifier in **Figure 2** overcomes this limitation, thanks to the addition of "active feedback," which includes voltage divider R_3-R_4 and the associated buffer amplifier, IC_5. With this arrangement, the following equations give the new transfer function and high-pass cutoff frequency, respectively.

$$A_D=\frac{V_{OUT}}{V_{IN1}-V_{IN2}}=\left(1+\frac{2R_2}{R_1}\right)\left(1+\frac{R_4}{R_3}\right)\frac{jR_{FB}C_{FB}\omega}{1+jR_{FB}C_{FB}\omega}.$$

$$f_C=\frac{\left(1+\frac{R_4}{R_3}\right)}{2\pi R_{FB}C_{FB}}.$$

The expression for the output voltage as a function of the input signal and the integrator's output voltage, V_Z, becomes:

$$V_{OUT}=\left(1+\frac{2R_2}{R_1}\right)\left(1+\frac{R_4}{R_3}\right)(V_{IN1}-V_{IN2})+\left(1+\frac{R_4}{R_3}\right)V_Z=A_D(V_{IN1}-V_{IN2})+\left(1+\frac{R_4}{R_3}\right)V_Z.$$

In this expression, $A_D=(1+2R_2/R_1)(1+R_4/R_3)$ is the new differential gain in the passband.

At dc, the output voltage remains 0V as long as the integrator's output does not reach its saturation voltage, $V_{Z(MAX)}$. Therefore, setting the output voltage at 0V in the new expression for output voltage yields the new maximum differential-input dc voltage and differential gain. They are, respectively:

$$\Delta V_{IN(MAX)}=(V_{IN1}-V_{IN2})(MAX)=\pm\frac{V_{Z(MAX)}}{A_D}\left(1+\frac{R_4}{R_3}\right).$$

$$A_{D(MAX)}=\frac{V_{Z(MAX)}}{\Delta V_{IN(MAX)}}\left(1+\frac{R_4}{R_3}\right).$$

In the above equations, the additional term, $1+R_4/R_3$, is the gain of the active-feedback stage.

The new expressions for $\Delta V_{IN(MAX)}$ and $A_{D(MAX)}$ clearly show the advantages of **Figure 2**'s ac-coupled instrumentation amplifier with active feedback: For an identical differential gain, you can extend the polarization-voltage range, $\Delta V_{IN(MAX)}$, by a factor equal to the gain of the active-feedback stage. Conversely, for a given polarization-voltage range, $\Delta V_{IN\ (MAX)}$, you can increase the differential gain by the gain of the active-feedback stage.

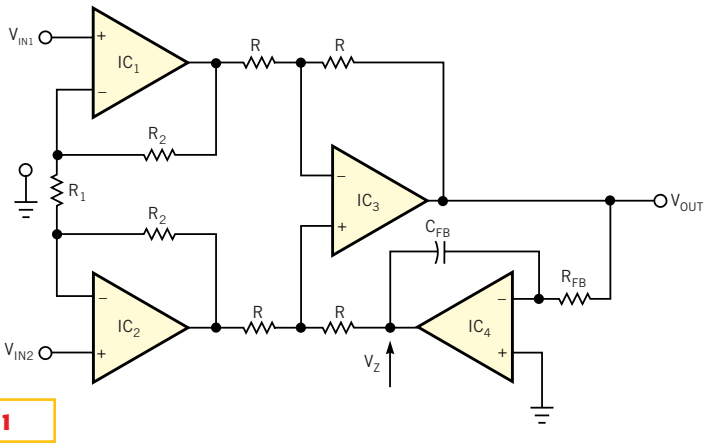
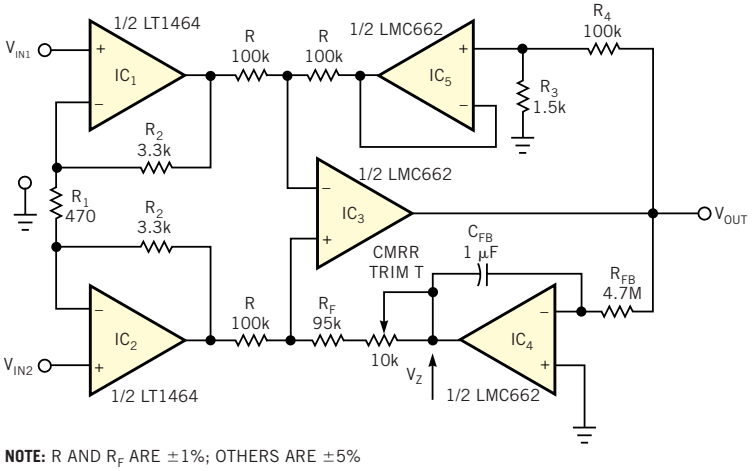


Figure 1 This ac-coupled instrumentation amplifier accommodates only ±5-mV maximum input.



NOTE: R AND R_F ARE ±1%; OTHERS ARE ±5%

Figure 2 This instrumentation amplifier can accommodate a differential-input range of ±0.34V.

The only drawback of this topology is apparent in the expression for f_C, the highpass cutoff frequency. You multiply this frequency by the gain of the active-feedback stage. Therefore, to maintain a given cutoff frequency, you must multiply the time constant by a factor equal to the active-feedback stage gain. This factor can be an issue in processing signals whose spectrum includes low-frequency components. In such applications, R_{FB} and C_{FB} can reach prohibitive values. Consequently, you must make a trade-off between the time constant and the active-feedback stage gain. The component values in **Figure 2** are a typical example of such a trade-off: The values are for an EEG (electroencephalogram) amplifier with ±5V split power supplies. The amplifier has a differential gain of 1000 and a highpass cutoff frequency of 2.3 Hz, and it can handle a differential-input dc-voltage range of ±0.34V.

To obtain this performance, you set the active-feedback stage gain and the differential-amplifier gain, respectively, to 67.6 and 15. With these gain values, the noise performance of the ac-coupled instrumentation amplifier of **Figure 2** is similar to that of a classic instrumentation amplifier. This situation occurs because the autozeroing and active-feedback stages, IC_4 and IC_3, are after the input differential stage, IC_1 and IC_2. Consequently, the gain of the differential stage roughly divides their respective noise contributions, which are therefore negligible. You can use several low-noise op-amps for IC_1 and IC_2. For portable biotelemetry applications, the LT1464 is a good compromise for input-noise density, noise-corner frequency, input-bias current and current drain. (Respectively: V_{NOISE}=26 nV/$\sqrt{Hz}$, f_C=9 Hz, I_{BIAS}=0.4 pA, and I_{CC}=230 µA.)

A theoretical analysis using the LT 1464's noise parameters shows that under worst-case conditions, the input-noise voltage should not exceed 11 µV rms. Tests on prototypes confirm this prediction; the tests effectively measure input-noise voltages of 3 to 6 µV rms. To sum up, an ac-coupled instrumentation amplifier with active feedback is well-suited for applications requiring high differential gain, a capability for handling large differential-input dc voltages, and low-noise performance.□

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1. Stitt, Mark, "AC-Coupled Instrumentation and Difference Amplifier," Burr-Brown, AB-008, May 1990.

Simplify computer-aided engineering with scientific-to-engineering conversion

Alexander Bell, Infosoft International, Rego Park, NY

THE SIMPLE yet useful formula in this Design Idea enables conversion from scientific format (for example, 2.2^{-9}), which is typical for CAE (computer-aided-engineering), double-precision output values, into "human-friendly" engineering format (for example, 2.2 nF). The engineering format is more suitable for bills of material and other electrical and electronic-engineering documents and specifications.

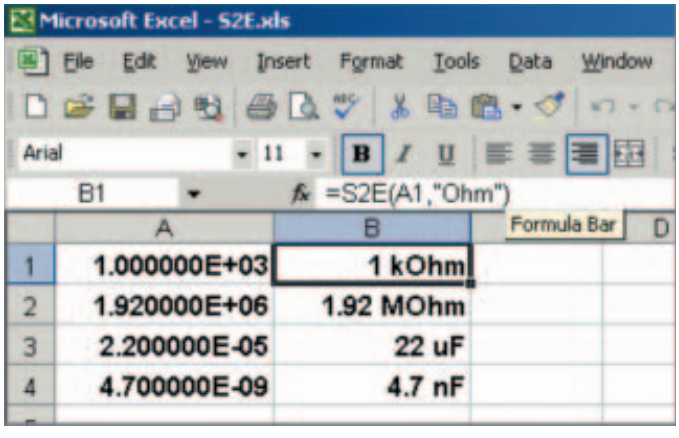


Figure 1 The formula appears in the formula bar, taking the first numeric parameter from the column to the left. The unit of electrical resistance, "ohm," is a second parameter.

The formula is rather straightforward. It takes two parameters. The first is the numerical value, and the second one specifies the unit of measurement—ohms, farads, or henries, for example. Alternatively, it could be of any random text, including an empty string, "." The formula calculates the mantissa/order of magnitude and returns the text string, formatted in compliance with commonly accepted electrical-engineering practice. **Listing 1**, available at www.edn.com, shows details of the formula. The tricky part of the formula is the conversion to a decimal type after the formula calculates the ratio of two log values (**Reference 1**). This step ensures the correct order-of-magnitude calculations in cases in which the mantissa of the input value is close or equal to one.

The formula is in VB; you could use it in any VB/VBA-backed software applications. In this example, the function is in a code module of an MS Excel file (**Figure 1**). You could also use it as an Excel Add-In (.xla) or a "pure-VB," compiled-DLL component. You can download **Listing 1** and the Excel file from the Web version of this Design Idea at www.edn.com. The input numerical value in this formula has double-precision accuracy, and its range spans from approximately -1.79^{308} to $+1.79^{308}$, which is sufficient for any practical engineering calculations. Note that the maximum value is even bigger than the famous "googol," which is represented by 100 digits.□

REFERENCE

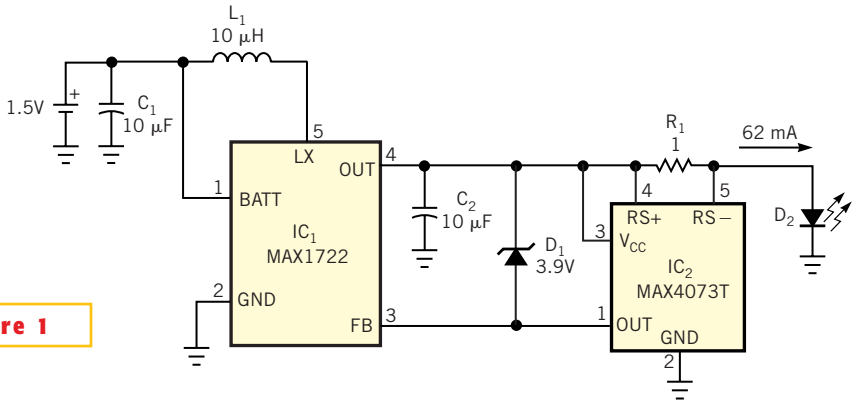
1. Bell, Alexander, "What's wrong with INT(LOG) in VBA?" *Access-VB-SQL Advisor*, October 2002, pg 65.

1.5V battery powers white-LED driver

Steve Caldwell, Maxim Integrated Products, Chandler, AZ

Although white LEDs are common in a variety of lighting applications, their 3 to 4V forward-voltage drop makes low-voltage applications challenging. Charge pumps and other ICs are available for driving white LEDs, but they generally don't work with the low supply voltage of 1.5V in single-cell-battery applications. The low-voltage circuit of **Figure 1** provides a current-regulated output suitable for driving white LEDs. The boost converter, IC_1, can supply load currents to 62 mA with input voltages as low as 1.2V, making it suitable for use with a 1.5V, single-cell battery. Because a white LED draws negligible load current until the output voltage rises above 3V, the boost converter can start with input voltages as low as 0.8V.

Figure 1



Powered from a single-cell battery, this circuit provides a regulated output current suitable for driving a white LED.

By deriving feedback from a high-side current-sense amplifier, IC_2, the circuit allows current regulation without sacrificing efficiency. IC_2's 1.8-MHz bandwidth also eliminates instability in the feedback loop. IC_2 amplifies the voltage across R_1 with a gain of 20. This high gain boosts efficiency by enabling use of a small-valued current-sensing resistor. You can calculate the value of R_1 from the desired output current: $R_1 = 1.235V/(20 \times I_{OUT})$. For 1.5V input and 62-mA output, the circuit efficiency of **Figure 1** is approximately 80%. Zener diode D_1 provides overvoltage protection at the output. When the output voltage rises above the sum of the zener voltage (V_Z) and IC_1's 1.235V feedback voltage (V_{FB}), the feedback voltage (Pin 3) rises and causes IC_1 to stop switching. Thus, for an open-circuit output, the output voltage is regulated at $V_Z + V_{FB}$.□

Simple V_{COM} adjustment uses any logic-supply voltage

Peter Khairolomour and Alan Li, Analog Devices, San Jose, CA

All TFT (thin-film-transistor) LCD panels require at least one appropriately tuned V_{COM} signal to provide a reference point for the panel's backplane. The exact value of V_{COM} varies from panel to panel, so the manufacturer must program the voltage at the factory to match the characteristics of each screen. An appropriately tuned V_{COM} reduces flicker and other undesirable effects. Traditionally, the V_{COM} adjustment used mechanical potentiometers or trimmers in the voltage-divider mode. In recent years, however, panel makers have begun looking at alternative approaches because mechanical trimmers can't provide the necessary resolution for optimal image fidelity on large panels. They also require a physical adjustment that technicians on the assembly line usually perform. This adjustment is not only time-consuming, but also prone to field failures arising from human error or mechanical vibration.

TABLE 1—OUTPUT-VOLTAGE RANGE

R_2 tolerance (%), scale	R_2 (kΩ)	V_{COM} (V)	Step size (mV)
−30, zero	0	3.5	3.9
−30 mid	3.5	4.0	
−30, full	7	4.5	
30, zero	0	3.3	6.8
30, mid	6.5	4.2	
30, full	13	5.1	

A simple alternative to achieving the increasing adjustment resolution for optimal panel-image fidelity is to replace the mechanical potentiometer with a digital potentiometer. Using digital potentiometers, panel makers can automate the V_{COM}-adjustment process, resulting in lower manufacturing cost and higher product quality. Unfortunately, many panels operate at higher voltages, and the choice of available supply voltages is limited. The system implementation for a 5V supply is straightforward (**Figure 1**). Without a 5V supply, the circuit can become more complex.

This Design Idea shows a simple way

that you can use any available logic supply to power the potentiometer providing the V_{COM} adjustment. The 6- or 8-bit AD5258/59 nonvolatile digital potentiometer demonstrates this approach. An I^2C serial interface provides control and stores the desired potentiometer setting into the EEPROM. The AD5259 uses a 5V, submicron CMOS process for low power dissipation. It comes in a space-saving 10-pin MSOP, an important feature in low-cost, space-constrained applications. For systems that have no 5V supply, many designers would be tempted to simply tap off the potentiometer's series-resistor string at the 5V location. This approach is not viable, because, during programming (writing to the

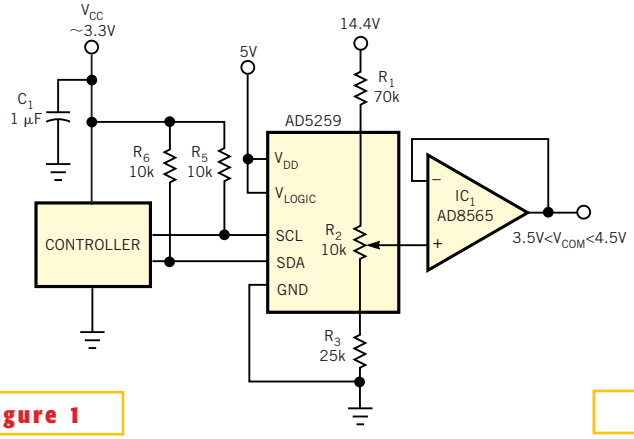


Figure 1

A digital potentiometer makes it easy to adjust V_{COM} to the desired value.

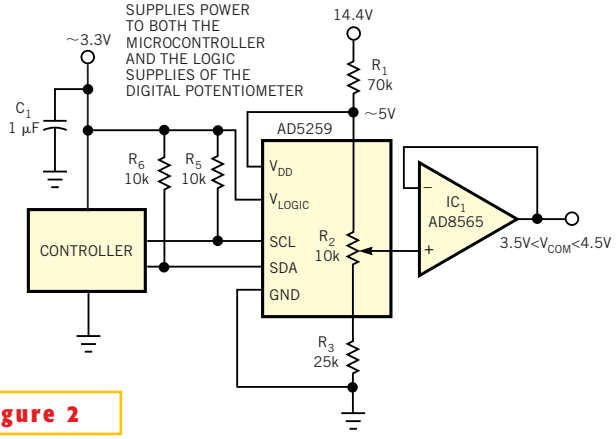


Figure 2

A separate V_{LOGIC} pin makes it possible to derive the V_{DD} supply from the potentiometer's resistor string.

EEPROM), the AD5259's V_{LOGIC} pin typically draws 35 mA. It cannot draw this current level through R_1 because the voltage drop would be too large. For this reason, the AD5259 has a separate V_{LOGIC} pin that can connect to any available logic supply. In **Figure 2**, V_{LOGIC} uses the supply voltage from the microcontroller that is controlling the digital potentiometer. Now, V_{LOGIC} draws the 35-mA programming current, and V_{DD} draws only microamps of supply current to bias the internal switches in the digital potentiometer's internal resistor string. If the panel requires a higher V_{COM} voltage, you can add two resistors to place the op amp in a noninverting gain configuration.

The digital potentiometer has ±30% end-to-end resistance tolerance. Assuming that the tolerances of R_1, R_3, and V_{DD} are negligible compared with those of the potentiometer, you can achieve the range of output values that **Table 1** shows. Assume that the desired value of V_{COM} is 4V±0.5V, with a maximum step size of 10 mV. As **Table 1** shows, the circuit in **Figure 2** guarantees an output range of 3.5 to 5.4V with a step size within ±10 mV. And, despite the ±30% tolerance of R_2, the midscale V_{COM} output meets the target specification. Also, because the digital potentiometer's logic supply matches the microcontroller's logic levels, the microcontroller can read data back if desired. **Figure 3** shows a block diagram of the digital potentiometer.□

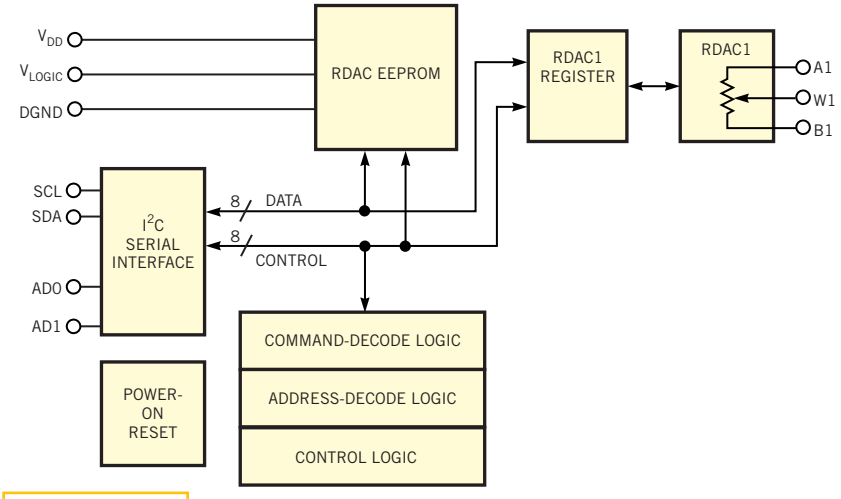


Figure 3 This block diagram shows the digital potentiometer's inner workings.

Edited by Bill Travis

Build a negative-voltage power-side switch

Michael English, Micrel Semiconductor, San Jose, CA

When you need to quickly connect a negative power supply under logic control, the negative power-side switch in **Figure 1** can help. Although originally intended for driving the gates of high-current MOSFETs, the MIC4451 can assume a different role. It provides complementary, low-on-resistance MOSFET switches to connect a system power-supply rail to a negative input voltage or to ground, enabled by a digital signal. The MIC4451 comprises an input buffer with a small amount of hysteresis and several logic inverter/buffers that ultimately drive a high-current output stage. **Figure 2** shows a block diagram of the MIC4451. The on-resistance of the n- and p-channel devices at the output is approximately 1Ω. So, the output can connect a 100-mA load to the negative input voltage with less than 100-mV voltage drop. A noninverting version, the MIC4452, simplifies inversion of logic control as needed. **Figure 1** shows details of the interface of the MIC4451 to TTL levels, using a common-base pnp transistor for level translation. The emitter current of Q_1 is approximately: $I_E=(V_{TTLH}-V_{BE})/R_1\approx(2.4-0.65)/R_1$, where V_{TTLH} is the TTL-high level, 2.4V. I_E should be ≤400 µA in accordance with TTL specs, so $I_E=(2.4-0.65)/R_1\leq 400$ µA.

Solving for R_1, you obtain $R_1\geq 1.8V/400\ \mu A=4.5\ k\Omega$. The V_{IH} (lowest permissible high input) logic-level specification of the MIC4451 is 2.4V. Ignoring base-current errors, $I_C\approx I_E$, so $R_2I_C\geq 2.4V$. Note that the MIC-4451's input voltage, V_{IH}, is specified with respect to the ground pin of the part. To determine R_2:$R_2=2.4V/$

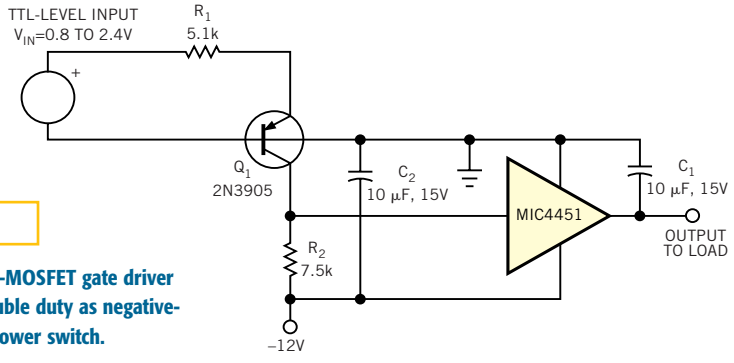


Figure 1 A power-MOSFET gate driver does double duty as negative-supply power switch.

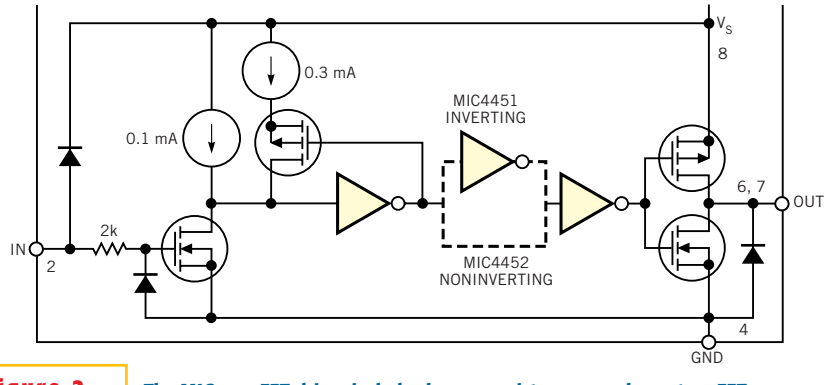


Figure 2 The MIC445x FET driver includes low-on-resistance complementary FETs.

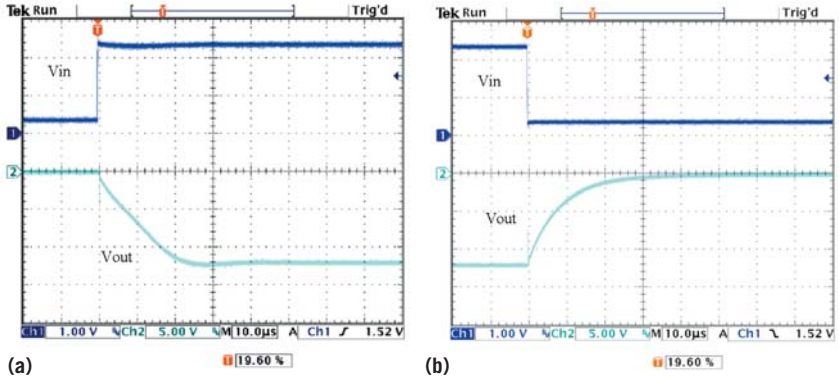


Figure 3 Turn-on (a) and turn-off (b) characteristics of the circuit in Figure 1 are for a −12V supply.

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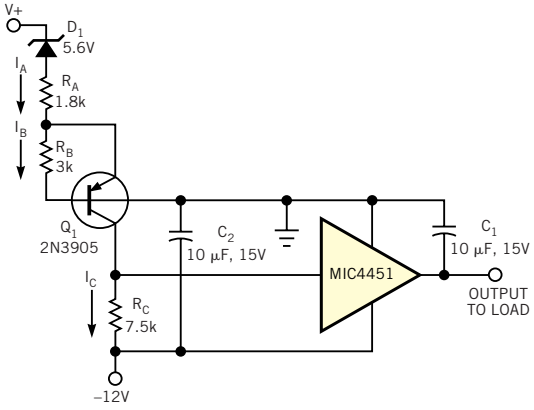


Figure 4 This circuit senses the magnitude of a positive supply and turns on a negative supply when the positive supply exceeds a threshold.

I_E=2.4V/0.4 mA=6 kΩ minimum.

You can comfortably choose real values for R_1 and R_2 somewhat higher than the worst-case limits calculated above, so choose R_1=5.1 kΩ and R_2=7.5 kΩ. Use 1% resistors to ensure worst-case logic levels are satisfied over temperature. **Figures 3a** and **3b** show power-switching times when driven from TTL. The output bypass capacitor and on-resistance of the MIC4451 determine the rise and fall times. **Figure 4** shows a simple circuit for sensing the level of a positive supply. The detection threshold, V^+, is a function of the breakdown voltage of zener diode D_1, V_{BE} of Q_1, resistor values, and the input threshold of the MIC4451. Referring to **Figure 4** and ignoring base-current errors, the collector current of Q_1 is approximately: $I_C = I_A - I_B$; $I_C = (V^+ - V_Z - V_{BE})/R_A - V_{BE}/R_B$.

Choosing V^+=7V and using a 5.6V zener diode with component values from **Figure 4** allows you to solve for I_C: I_C=(7−5.6−0.65)V/1.8 kΩ−0.65V/3 kΩ=(0.416−0.216) mA=0.200 mA. Because the input threshold of the MIC4451 is typically 1.5V, this level detector trips when $R_C I_C$ =1.5V, so rearranging: R_C=1.5V/0.2 mA=7.5 kΩ.

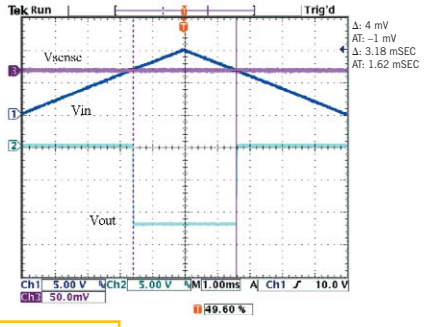


Figure 5 The circuit in Figure 4 turns on the negative supply when the positive supply exceeds 1.5V.

Figure 5 shows details of the operation of the negative power switch with positive-supply sensing. To sum up, a circuit intended for driving high-speed-MOSFET gates finds new use as a negative-power-supply switch. You can easily interface the MIC445x to logic-level control signals. You can use a simple circuit to detect the level of a positive supply voltage and connect a negative supply when the positive voltage has risen above a certain threshold level.□

Circuit offers series protection against power-line transients

Alfredo Saab and Travis Eichhorn, Maxim Integrated Products, Sunnyvale, CA

Voltage transients on low-voltage power lines can sometimes attain amplitudes many times the nominal voltage level. That behavior often calls for protection against the application of improper power levels. The usual way to protect sensitive circuitry against overvoltage is to add parallel clamps. Fuses or other current-limiting devices precede these clamps' high energy-absorption capability. Other cases require the use of high-voltage series protection (instead of parallel clamps) because of the difficulty in resetting or replacing fuses, an inaccessible operating environment, or the need for uninterrupted operation. The series-protection circuit of **Figure 1** turns off the power switch using a series-connected, high-voltage, n-channel MOSFET power switch, Q_1, and a fast overvoltage

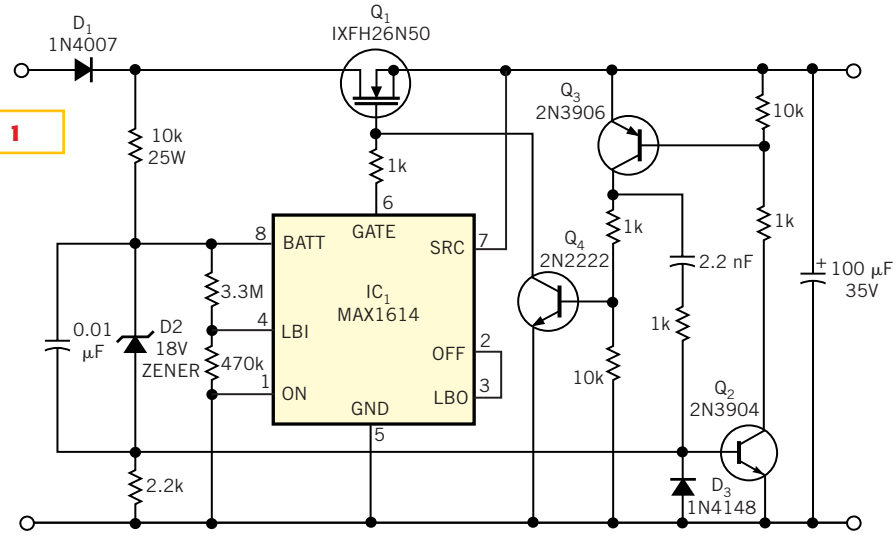


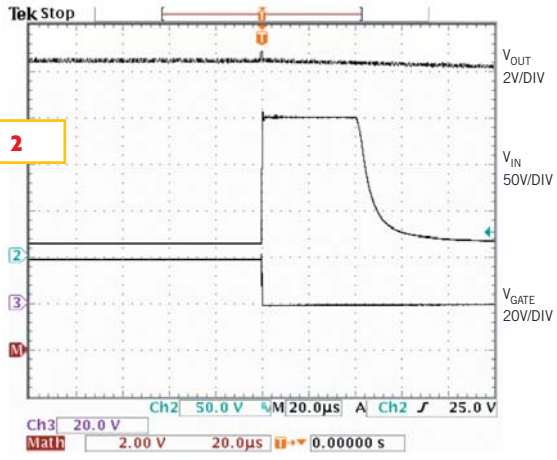
Figure 1 This circuit protects a load, connected to the right pair of terminals, from undervoltage and high-voltage transients in the supply voltage, connected to the left pair of terminals.

detector. The power switch and series-connected power rectifier, D_1, protect the load against high-voltage transients and continuous overvoltage as high as ±500V of either polarity.

In the circuit, which powers loads as heavy as 1A from a nominal 12V power line, a high-side-switch driver, IC_1, biases the power switch fully on. You can increase the maximum load current by changing D_1 and Q_1. To guard against low supply voltage, IC_1 includes an undervoltage-lockout feature that allows operation only when the line voltage is greater than 10V. To protect against overvoltage, the circuit includes a three-transistor, no-bias-current, 50-nsec-operation overvoltage detector that triggers when the input voltage reaches approximately 20V. At that time, Q_4 "crowbars" the gate of the power switch to ground, turning it off hard. Rising overvoltage first turns on zener diode D_2, which protects the IC by clamping the voltage across it to approximately 18V. Zener current flows through the 2.2-kΩ resistor, producing a base voltage that turns on Q_2. That action initiates a rapid sequence: Q_3 turns on, which turns on Q_4, which turns off Q_1 by quickly discharging its gate capacitance.

You can demonstrate the circuit's performance by applying a 150V transient to the supply voltage while the circuit output is delivering 1A at 12V (**Figure 2**). The internal impedance of the transient source is 1Ω, and the rise time of the applied voltage is 1 µsec. The circuit draws 20 µA during normal operation, including 3 µA by the undervoltage-lockout, voltage-sensing divider and 17 µA by IC_1. If your design needs high-temperature operation, note that the gate-current output of IC_1 is relatively limited. Your design calculations for high temperature should also pay close attention to leakage currents that the other circuit components contribute.□

Figure 2



A 150V transient applied to V_{IN} of the Figure 1 circuit has little effect on V_{OUT}.

Build a simple, soft-action muting switch

John Firestone, Bremerhaven, Germany

The circuit in **Figure 1** adds a soft muting switch with power-up/power-down muting to a line-level audio circuit. R_4, C_1, and JFET Q_1 quietly ground a signal in 100 to 200 msec when you close S_1 or release it when you open S_1. Potentiometer R_2, set to twice Q_1's cutoff voltage, makes the on/off transition times roughly equal. R_2 and D_3 quickly discharge C_1 and mute the signal during power-down. For this process to work, the signal path should remain stable to below roughly one-third the normal supply voltages—below ±4V in this example. Q_1 can then finish muting. Making Q_1 a more tightly defined PN4392 can soften this requirement and allow muting of lower impedance signals. R_3 unloads S_1 from R_2, so that D_3 does not shorten the earlier transition times. S_1's normally closed contact, resistor R_1, and dual-LED D_2 add an indicator light. D_1 raises the red LED's on-state threshold to indicate green when muting is off. Replacing D_1 with a short circuit causes the red LED to light. This scheme makes a more expensive DPDT (double-pole, double-throw) switch unnecessary, provides uninterrupted light as S_1 switches, and reduces the LED-current change for less noise (**references 1** and **2**).□

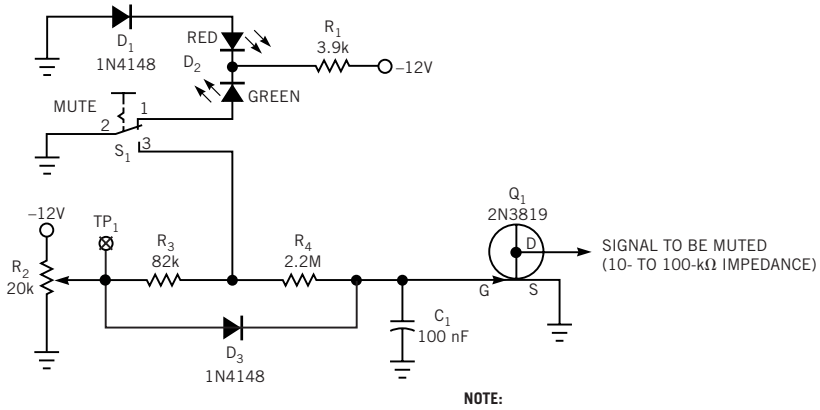


Figure 1

This simple circuit provides soft muting for line-level audio circuits.

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High-voltage amplifier uses simplified circuit

Jui-I Tsai, Jun-Ming Shieh, Tai-Shan Liao, and Ching-Cheng Teng, National Chiao Tung Unversity, Taiwan

Many scientific instruments and sensors need ac high-voltage drive. High-voltage drive is useful for driving electrodes in many applications. The challenge is to boost the output of a conventional op amp to high voltages. Available ac high-voltage amplifier modules are limited to approximately 1200V p-p. This Design Idea presents a simplified ac high-voltage amplifier that uses complementary, cascaded NMOS and PMOS transistors (**Figure 1**). The OP07 op amp has low input-offset voltage, low input-bias current, and high open-loop gain. These attributes make this op amp useful for high-gain instrumentation applications. In addition, the OP07 features excellent stability of offsets and gain over time and temperature. The ac gain of the LM356 stage, which R_3, R_4, R_7, and R_9 determine, is approximately 100.

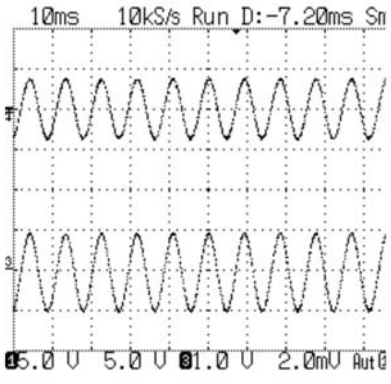


Figure 2 The sinusoidal input is 8V p-p (top trace), and output is 1800V p-p (bottom trace).

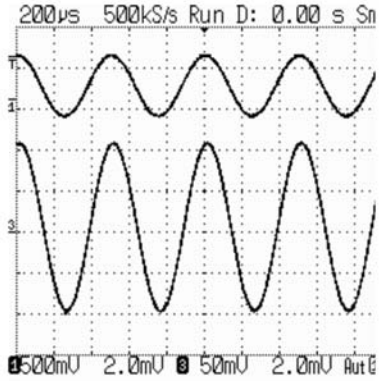


Figure 3 The input is 750 mV (top trace), and the output is 200V p-p (bottom trace).

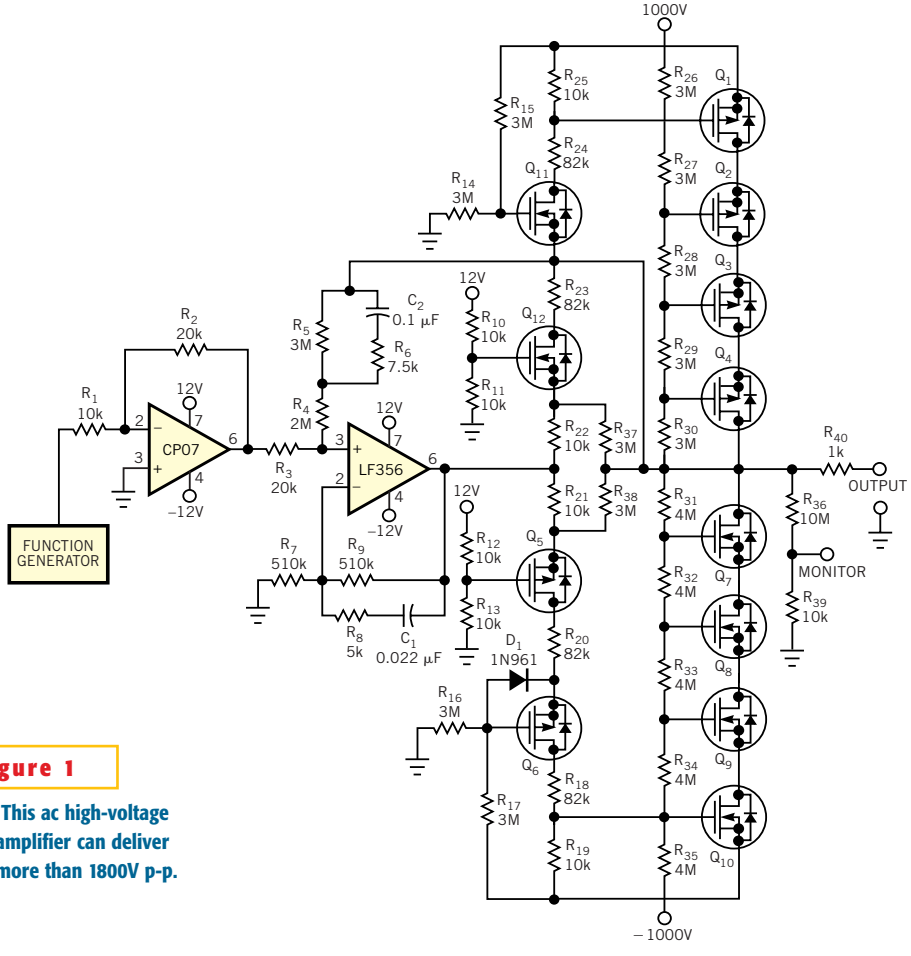


Figure 1 This ac high-voltage amplifier can deliver more than 1800V p-p.

The high-voltage MTP2P50E p-channel MOSFET has maximum drain-to-source- and gate-to-drain-voltage ratings of 500V. The high-voltage BUK456800B n-channel MOSFET has maximum drain-to-source- and gate-to-drain-voltage ratings of 800V. Q_1 through Q_6 are PMOS transistors, and Q_7 through Q_{12} are NMOS devices. These FETs are well-suited for high-voltage cascade circuits. They connect symmetrically in series to increase their overall breakdown voltage for power applications. The bias-voltage circuits comprise separate biasing-resistor pairs R_{10} to R_{13} and R_{14} to R_{17}; the result is a symmetrical output of the high-voltage amplifier. **Figure 2** shows a sinusoidal input of 8V p-p at 100 Hz and an output of 1800V p-p. **Figure 3** shows a sinusoidal input of 750 mV p-p at 2 kHz and an output of 200V p-p. The total power bandwidth of the circuit is approximately 200 kHz.□

Simple circuit provides power sequencing

John Betten, Texas Instruments, Dallas, TX

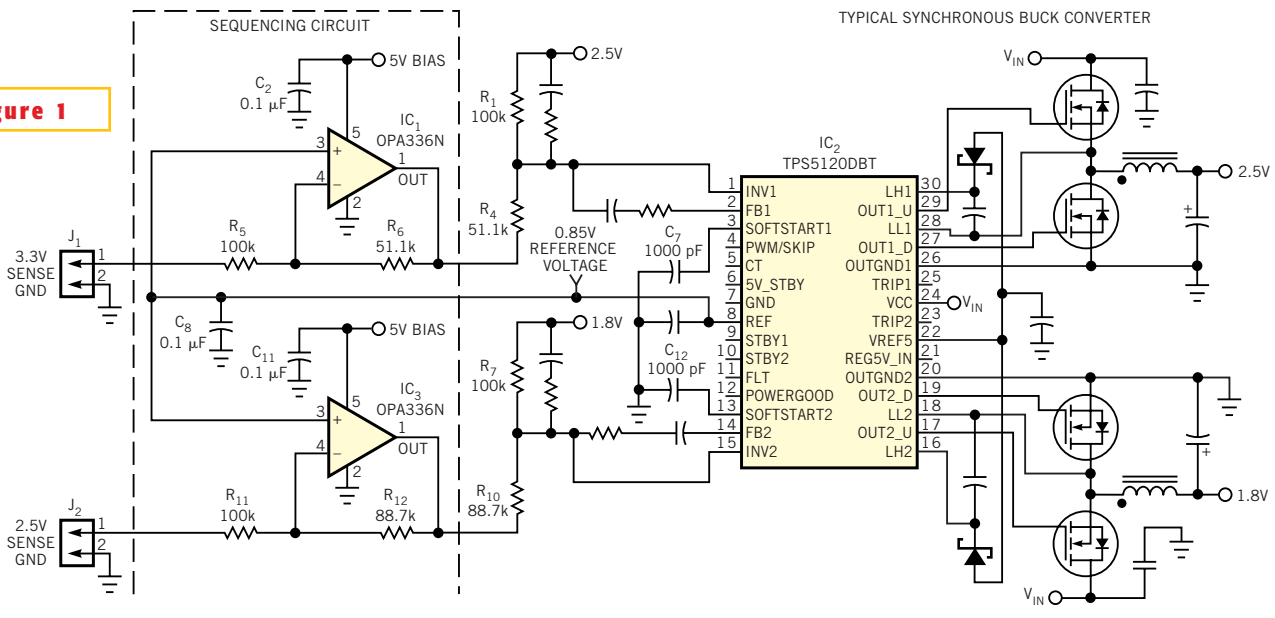
ASICs, FPGAs, AND DSPs can require multiple supply voltages with restrictions on their start-up sequencing. Often, I/O voltages, which usually have the highest voltage, must come up first, followed by all other voltage rails in a high-to-low order, with the core voltage last. This scenario may also require that one supply rail not exceed another by more than a diode drop; otherwise, excessive current may flow backward from the I/O voltage through the IC into a lower voltage, possibly damaging the expensive IC. Often, you can control this sequence by placing external diodes between successive voltage rails to clamp a higher voltage to within a diode drop of a lower voltage, thus preventing possible latch-up in the IC. The diode conducts only when a lower voltage rises above a higher one at turn-on, but not if a higher voltage were to increase above any lower voltage, because the diode is reverse-biased. A preferred method would be to use the power-supply controller to precisely control the start-up-voltage sequencing of the power-supply rails. **Figure 1** shows a simple op-amp circuit that integrates a dual switching power supply to provide simultaneous output-voltage sequencing.

In this power-sequencing circuit, three output voltages sequence at start-up, during which each output voltage tracks the next-higher voltage rail until it reaches its fixed regulation voltage. Assume that a 3.3V "master"-I/O voltage (not shown) powers up normally. The controller for this voltage uses its soft-start function to provide a smooth linear ramping of its voltage. The TPS5120 dual switching regulator generates two additional voltages, 2.5 and 1.8V. In most standard switching-regulator circuits, the bottom sides of R_4 and R_{10} would be grounded, thus fixing the output-voltage setpoints. In this circuit, the output of an amplifier controls the voltage at the bottom of each of these resistors. An amplifier output voltage of zero sets the output voltage to its predetermined fixed voltage, but any voltage greater than zero forces the output voltage to be lower than its setpoint.

The amplifiers are in an inverting configuration with the next-higher output voltage as its input or "sense" voltage. Thus, at power-on, when the 3.3V output is 0V, amplifier IC_1's output voltage is high, also forcing the TPS5120 controller to regulate its output voltage to 0V. The output voltage of amplifier IC_3 is also high, because the 2.5V output, which is also 0V, controls input voltage. As the 3.3V output rises linearly, the amplifier's output voltage decreases linearly to 0V. The 2.5V output voltage thus increases from 0V to its maximum setpoint of 2.5V. The 1.8V output voltage tracks the 2.5V output in a similar manner. Set the amplifier's component values such that when the sensing voltage, such as the 3.3V, reaches the tracking-voltage level—here, 2.5V—the amplifier's output voltage just attains 0V. Therefore, increases in the sense voltage higher than 2.5V cannot further raise the tracking output voltage, because the amplifier's output voltage has already saturated to ground level.

Simultaneous tracking requires several important design criteria. The amplifier's feedback ratio, R_5-R_6, must be equal

Figure 1

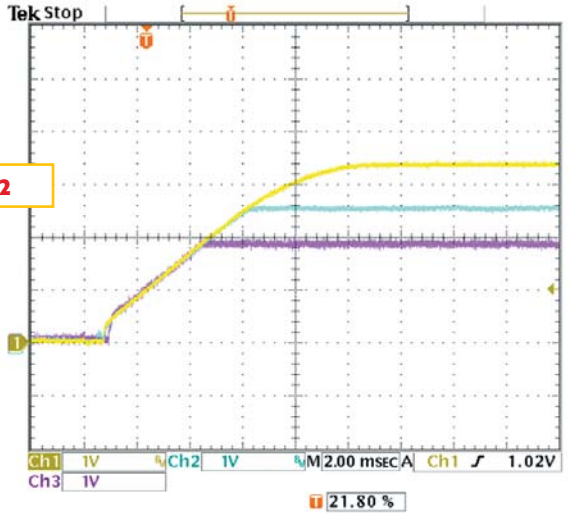


An amplifier circuit forces the converter's output voltages to track during start-up.

to the feedback-resistor divider ratio set by R_1 and R_4. In addition, you must use the TPS5120 controller's reference voltage, 0.85V in this example, as an input to the amplifier's noninverting terminal. Any reference-voltage value other than this one forces the tracking-voltage output to a voltage different from the sense voltage. The amplifier you select should have a low input-offset voltage and be capable of an output voltage at least as great as the controller's reference voltage.

A rail-to-rail amplifier works well in this application. Individual amplifiers to allow localized component placement, avoiding routing near any noise sources. This design uses an additional decoupling capacitor near the amplifier's noninverting input for the reference voltage. It uses a small, soft-start capacitor value for the TPS5120 controller so that the controller was inherently faster at start-up than the 3.3V sense voltage. A large soft-start capacitor value does not allow for fast tracking on the outputs. Too small a value may cause output-voltage overshoot when you initialize power. **Figure 2** shows the start-up voltages for three synchronous buck converters. The 3.3V acts as a master, and 2.5 and 1.8V track their respective higher voltages. You can set the sense voltage for the 1.8V output to track the 3.3V output rather than the 2.5V with equally good linear tracking during start-up. You can add this sequencing circuit to any power-supply controller that provides access to its reference voltage, soft-start capacitors, and output-voltage resistor-divider network.□

Figure 2



The 2.5 and 1.8V outputs track the 3.3V output at start-up.

Edited by Bill Travis

Latching power switch uses momentary-action pushbutton

Anthony Smith, Scitech, Biddenham, Bedfordshire, UK

Most inexpensive pushbutton switches, particularly pc-board-mounting and membrane types, have momentary action. Latching types are often larger and relatively expensive, and they frequently are unavailable in the style you'd like to use. You can thus have a problem if you need a small, inexpensive on/off switch for latching power to a load. The circuit in **Figure 1** shows how you can use a simple, momentary-action, SPNO (single-pole, normally open) pushbutton switch to latch power to a load. Requiring just a handful of common, garden-variety components, the circuit works over a wide voltage range and is ideal for single-cell applications, because it can operate at voltages as low as 1V or less. Transistors Q_2 and Q_3 form an SCR-like structure that functions as a simple latch, Q_4 switches power to the load, and S_1 is the momentary pushbutton switch.

When you first apply the supply voltage, V_S, all four transistors are off, and capacitor C_1 charges via R_1 and R_2 until its voltage, V_{C1}, is equal to V_S. The circuit is now in its off, or unlatched, state, and the load voltage, V_L, is 0V. A momentary closure of the pushbutton switch, however, causes C_1 to dump its charge into the base of Q_3, which conducts and furnishes bias for Q_2 and Q_4, which both turn on. Q_2 now provides base bias for Q_3 via R_5, and also for Q_1 via R_3. The circuit is now in its on, or latched, state and remains that way even though S_1 is open. The load is now energized, and V_L is roughly equal to V_S. Transistor Q_1 is now saturated, causing C_1 to discharge via R_2 such that V_{C1} falls to a few tens of millivolts (Q_1's collector-emitter saturation voltage). Another momentary closure of the pushbutton switch couples this low voltage to Q_3's base, turning it off. As a result, all four transistors turn off, and the circuit reverts to its off, or unlatched, state. The load is now de-energized, and V_L falls to 0V. Because Q_1 is now off, C_1 begins to charge again via R_1 and R_2, such that another momentary closure of S_1 latches the circuit on again.

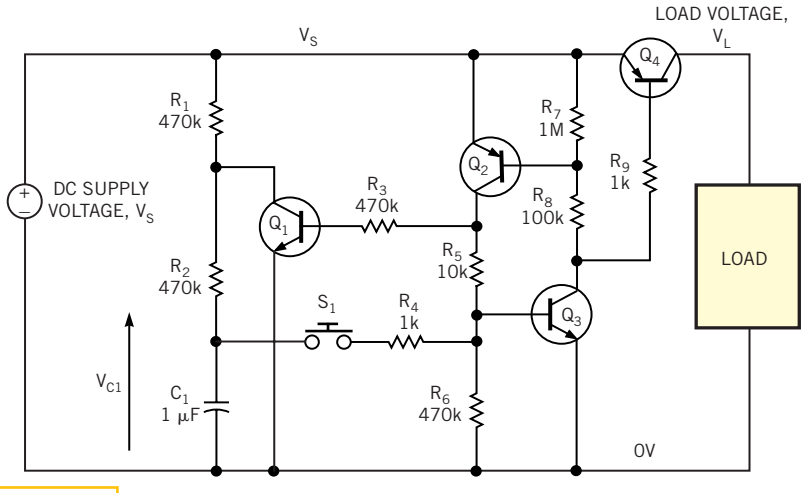


Figure 1 The momentary-action pushbutton switch, S_1, provides positive latching action in this circuit.

Timing capacitor C_1, acting with R_1 and R_2, provides debouncing for the pushbutton switch, such that contact bounce has no effect on the desired latching function. Without the RC time delay, the circuit would "chatter" on and off each time you pressed the pushbutton switch and would end up in an indeterminate state. Although **Figure 1** shows a value of 1 µF, other values may be more suitable for a particular application, so prepare to experiment. None of the resistor values is particularly critical, and the values shown in **Figure 1** are fairly optimal for a supply voltage of approximately 1 to 1.5V—in other words, a single cell. At higher voltages, the resistor values should increase proportionally, although you should hold R_2 and R_4 constant at approximately 470 and 1 kΩ, respectively. Keeping the R_2-C_1 time constant fixed at a few hundred milliseconds ensures that the time taken to discharge the capacitor is not excessive; otherwise, once the circuit has been latched, there may follow an unacceptable delay before it can be unlatched. Resistor R_4 limits the current flowing from C_1 into Q_3's base to a safe level; its value should be fairly small to ensure that R_5 and R_6 do

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not distort the voltage appearing at Q_3's base when the switch closes.

You should size resistor R_1 according to the supply voltage you use. For a given value of R_2, R_1 determines the time it takes V_{C1} to rise toward V_S immediately after the circuit has been unlatched. In other words, R_1's value determines the time needed to "prime" the circuit to make it ready to be latched on again. If R_1 is too large, it becomes impossible to latch the circuit on soon after it has been unlatched. On the other hand, if R_1 is too small, it may impose an unacceptable current drain on V_S when the circuit is latched on. Furthermore, for a particular value of V_S, R_1 should be large enough to ensure that V_{C1} does not rise too quickly after the circuit has been unlatched, or it could turn the latch back on again before the switch has opened. You may need some experimentation to determine the optimum value for R_1, but with C_1=1 µF and R_2=470 kΩ, the test circuit performed well with a value of approximately 470 to 680 kΩ at V_S=1V and approximately 4.7 MΩ at V_S=10V.

Transistors Q_1 to Q_3 can be any small-signal types with good current gain (moderate to high forward current gain). Power switch Q_4 should have low $V_{CE(SAT)}$ to ensure most of the supply voltage is delivered to the load when the circuit is latched. You should select resistor R_9 to furnish plenty of base drive for Q_4; the value depends mainly on V_S, on the load current, and on Q_4's saturated current gain. The circuit provides an inexpensive way of deriving a latching function from a momentary pushbutton, and, like a mechanical latching switch, the quiescent (unlatched) current drain is zero.□

Method provides overpower protection for quasiresonant supplies

Nicolas Cyr, On Semiconductor, Toulouse, France

The main characteristic of quasiresonant switch-mode power supplies is that they exhibit a varying frequency when the input voltage changes. For a flyback power supply, the power delivered to the output obeys the following equation: $P_{OUT}=1/2(L_P\times I_P^2\times F_{SW}\times\eta)$, where L_P is the primary inductance, I_P is the peak primary current, F_{SW} is the switching frequency, and η is the efficiency. Because L_P and η are fixed with a moving switching frequency F_{SW}, I_P has to move in the opposite direction to maintain a constant output power. So, when input voltage V_{IN} rises, F_{SW} increases; as

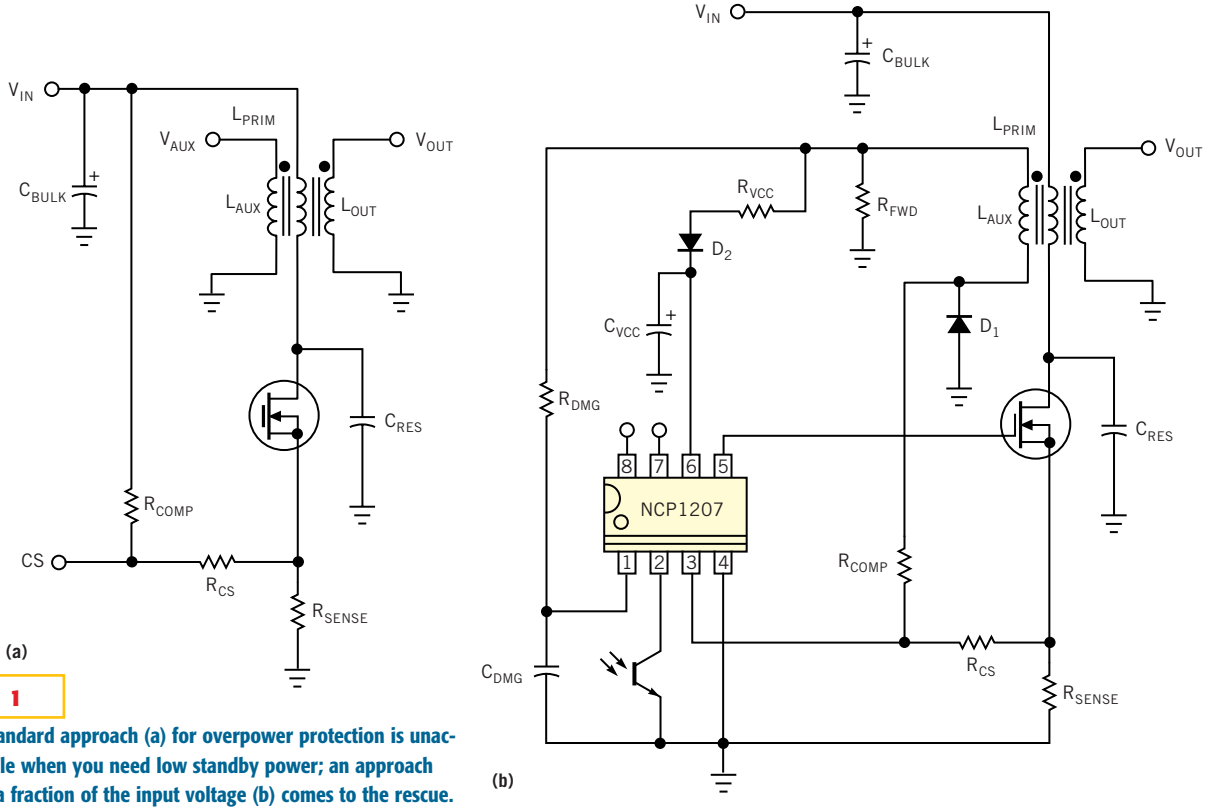


Figure 1

The standard approach (a) for overpower protection is unacceptable when you need low standby power; an approach using a fraction of the input voltage (b) comes to the rescue.

a result, I_p needs to decrease in response to the feedback-loop requirements. For a widely varying line-voltage application, the peak current almost doubles between high and low input voltages for a constant output power. But quasiresonant controllers feature only overcurrent protection. This limitation is part of a structural problem. The controller monitors the peak current, and, when they reach the maximum allowed value, the controller circuitry detects an overload. Unfortunately, if the power supply delivers its nominal power at the lowest worst-case input voltage, it delivers more power for a higher input voltage. For a widely varying line-voltage application, this power could be more than three times higher. This fact is the consequence of the flyback equation.

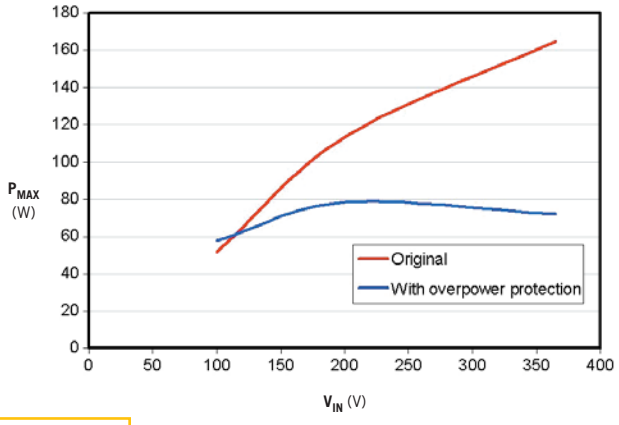


Figure 2 The output power rises to 165W without compensation but remains within 70W using the compensation scheme.

A classic way to compensate this variable-power effect is to create an offset on the current-sense pin that compensates for the peak-current variations as a function of the input voltage, V_{IN}. You obtain this effect using an overpower-protection scheme—wiring a compensation resistor from the high-voltage rail to the current-sense information (**Figure 1a**). Unfortunately, you cannot always implement this scheme. Whether you use the CS (current-sense) pin for another function or you need to keep the pin impedance low for noise purposes, it forces you to adopt a low value for resistor R_{CS} in series with the current-sense information. It then requires a low-value compensation resistor, R_{COMP}, wasting a lot of power. When you need low standby power, this approach is unacceptable. To overcome the problem, it might be useful to use a fraction of the input voltage to lower the voltage drop on R_{COMP}. The power the resistor wastes would then become negligible.

You achieve this method by using the forward voltage of an auxiliary winding. On a forward winding, a voltage proportional to V_{IN} occurs during the on-time, which is the scenario you are looking for. Usually, you use a flyback auxiliary winding to supply the controller and to detect the core-reset event. By modifying the arrangement of the winding, you can generate the flyback information for the demagnetization detection during off-time and combine, on the same winding, the forward information for the overpower compensation during on-time. By adding a diode in series with the auxiliary winding, you can access the forward voltage (**Figure 1b**). This forward voltage is proportional to $N \times V_{IN}$, where N is the turns ratio between the primary and the auxiliary windings. You add R_{FWD} to supply the reverse current during the forward activity.

Knowing the value of the forward voltage and the series resistor, R_{CS}, you can then easily calculate the value of compensation resistor R_{COMP} to create the desired offset on the current-sense signal at high input voltage. On a demonstration board built on the NCP1207 from On Semiconductor (www.onsemi.com), D_1 is a 1N4448 diode, $R_{CS}=680\Omega$, $R_{COMP}=18$ kΩ, and $R_{FWD}=4.7$ kΩ, the protection toggles at 60W at 100V dc and 70W at 365V dc, instead of 55W at 100V dc and 165W at 365V dc without compensation (**Figure 2**). **Figure 3** shows circuit waveforms of the line compensation at $V_{IN}=365$V, and **Figure 4** shows the waveforms at $V_{IN}=100$V.□

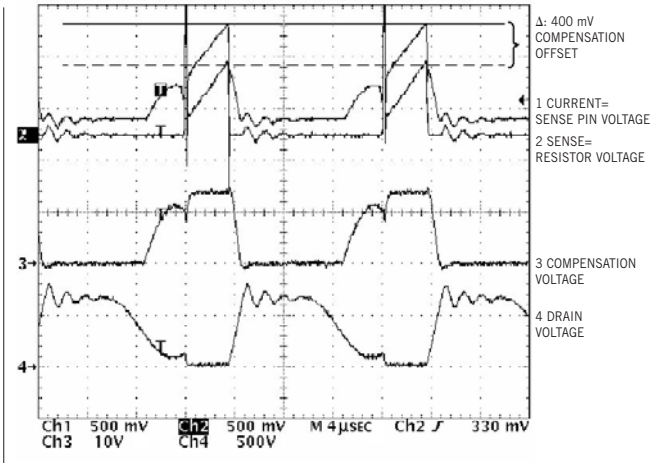


Figure 3 These waveforms represent line compensation at input voltage of 365V.

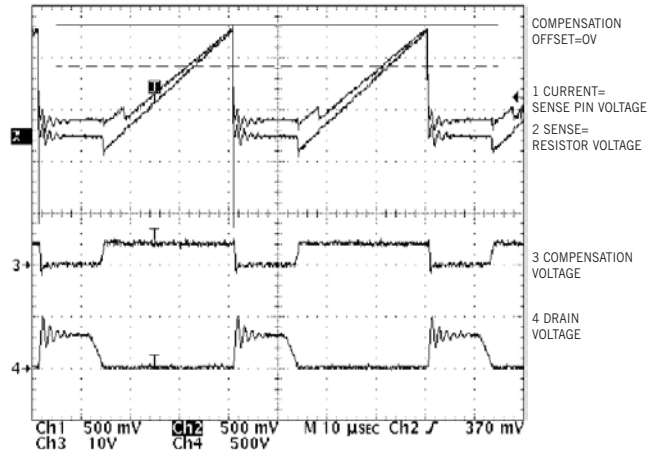


Figure 4 A set of waveforms accompanies line compensation at input voltage of 100V.

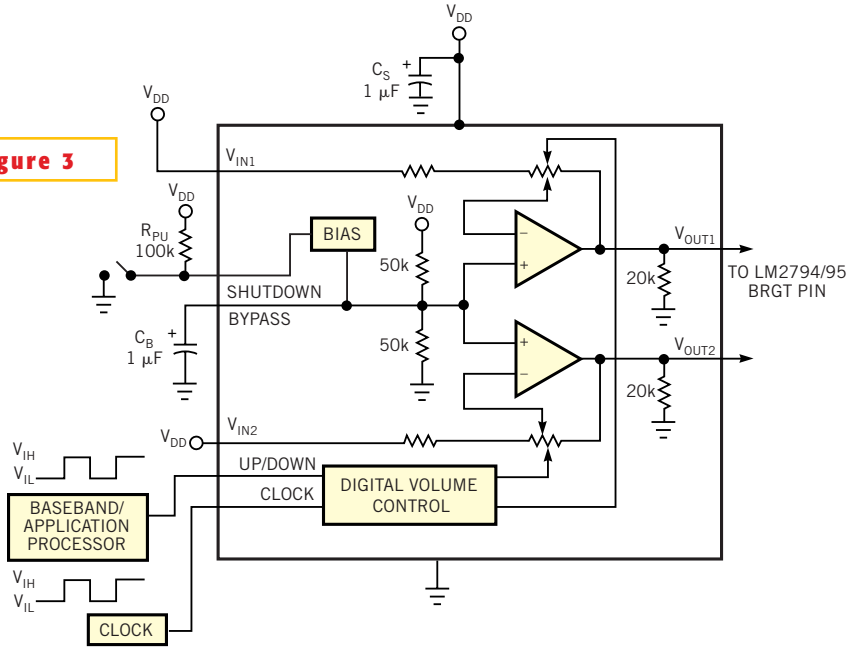
Circuit delivers dimming control for white-LED driver

Wallace Ly, National Semiconductor, Santa Clara, CA

THE DEMAND FOR POWER in color cellphone handsets is constantly increasing. New applications steadily emerge, making it imperative to reduce power consumption in the design. Examination of usage data shows that more than 50% of the power consumed is in providing backlighting for the color screen. People use the phones for playing games and MP-3s and a multitude of other heavy-duty, multimedia functions. **Figure 1** shows the classic way to use a backlight-driver IC to provide dimming. By modulating an external PWM signal, the circuit controls the white-LED current. By adjusting the on/off-time ratio, or duty cycle, the circuit can provide drive ranging anywhere from full-on to full-off. This circuit relies on the fact that the baseband or application processor has a PWM timer available. A second method of obtaining dimming is to use an adjustable analog-input interface (**Figure 2**). The drawback of this approach is that it requires a DAC block in the digital-baseband or application processor.

This Design Idea presents a more widely adaptable approach to the dimming challenge. Although the LM4811 headphone amplifier is not designed to operate as a DAC, you can tweak it to do so. **Figure 3** shows the dimming application. The implementation is straightforward. The output of the LM4811 attaches to the BRGT pin of the LM2794. The output current from the LM4811 is directly proportional to the digital value stored in the digital-volume-control block. The rising edge of the clock, along with the polarity of the Up/Down pin, sets the appropriate output current of the LM4811 and, thus, the output current of the white-LED driver. The resultant approach requires only two general-purpose input/output lines, which are available in all modern baseband and application processors. Moreover, this method requires zero processor cycles once the LED current is set. The approach is therefore optimal for both software and hardware.□

Figure 3



A headphone amplifier finds dual use in a white-LED dimming circuit.

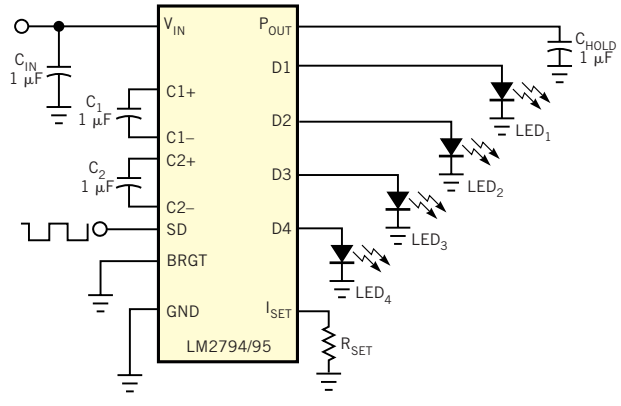


Figure 1 **In this classic LED-dimming configuration, an external PWM signal varies the duty cycle of the driver.**

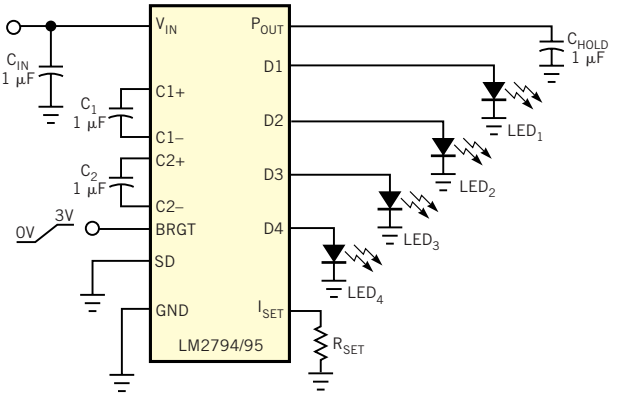


Figure 2 **This dimming circuit requires the existence of a DAC in the application processor.**

System implements digital-clock modulation

Dan Doberstein, DKD Instruments, Nipomo, CA

In spread-spectrum and direct-sequence receivers, it's often necessary to change the frequency of the clock oscillator, and thus the spreading-code clock, to lock the receiver's reference pseudorandom-noise code to the incoming code. The original design used a VCXO (voltage-controlled crystal oscillator) for this function, but this revised design implements an all-digital method that provided additional functions, using a midlevel CPLD from Altera (www.altera.com). A commercially available part, the 74HC297, provides the function. This part is an all-digital PLL chip that most engineers have never heard of. The 74HC297 can digitally modulate an applied clock. It performs this task by adding or subtracting a pulse to or from a divided-down clock.

Upon examining the functions of this part, two issues emerge. First, it divides the input clock by two before modulating it. Second, the modulation method inserts and subtracts pulses. Although the pulse-addition/subtraction issue is acceptable, the divide-by-two function reduces the phase/frequency-control resolution. With the inspiration of the 74HC297 in mind, we sought a method that had finer resolution in phase and frequency for the same applied clock frequency. At first, we tried discrete counters using a digital switch to select different divide ratios. This approach worked at low clock frequencies but failed as clock speed increased because of propagation-delay effects at the switch. Eventually, we devised a method that used a long shift register and a tap-selection switch to implement a variable clock divider/phase modulator. **Figure 1** shows the block diagram of the system.

You load the 21-bit shift register with a single one and the rest zeros. A switch-selectable tap point feeds back to the shift register's input. In effect, a single one now goes around and around at a frequency, F_{OUT}, determined by the tap point and the applied clock, F_{CLK}. The switch function allows selecting one of three divide ratios:

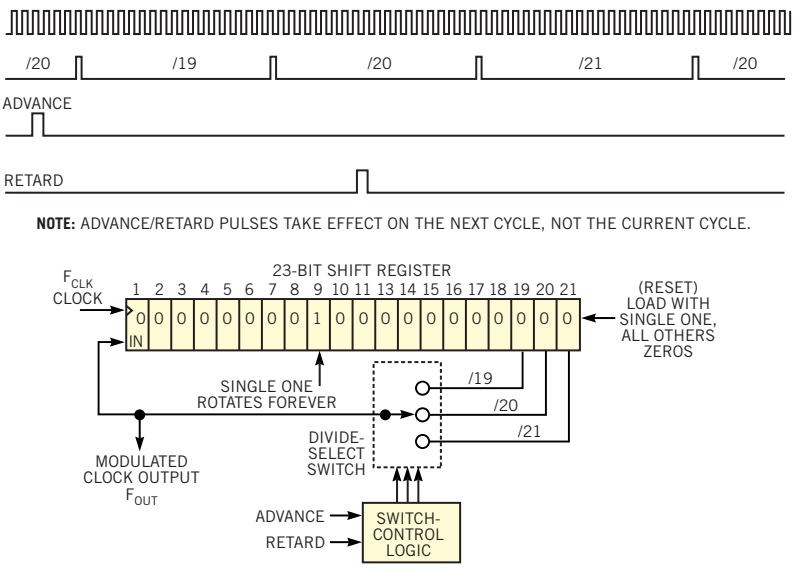


Figure 1 This scheme allows you to change the rate of the spreading-code clock in spread-spectrum applications.

19, 20, or 21. The choice of the tap points is a function of the target application's needs, although you can choose other tap points. In operation, if the system detects an Advance pulse, the switch selects the divide-by-19 for one F_{OUT} cycle. If the system detects a Retard pulse, the switch selects divide-by-21 for one F_{OUT} cycle. After every Retard or Advance pulse, the system returns the selection switch to the divide-by-20 position. The single one, as it shifts through the register, effects the setting and resetting of the switch. At first, it appears that this system will modulate the F_{CLK} input in an FM-like fashion. But, on second thought, it also acts as a phase modulator. On a single Advance pulse, approximately one-twentieth of an output cycle is subtracted, and a single Retard pulse adds approximately one-twentieth of an output cycle. If the Advance or Retard pulses are continuous streams at frequency F_{MOD}, the output frequency is $F_{OUT}=(F_{CLK}\pm F_{MOD})/N$, where N=20 in this case, and the sign is positive for Advance pulses and negative for Retard pulses.

So, this modulator can do both PM and FM on the applied clock, F_{CLK}. The tap numbers this design uses reflect those that fit the target application. The target application needs approximately 1-MHz final output frequency with a phase resolution of one-twentieth of a cycle, or the equivalent of 50 μsec in the time domain. If you need more phase resolution, increase the shift register's length. For example, a 101-stage shift register with tap points at 99, 100, and 101 has a phase resolution of approximately 3.6°. The advantages of the shift-register approach are speed and scalability. You can clock shift registers at extremely high speed. Additionally, the shift-register approach automatically provides you with clock signals that are exact advanced or delayed versions of the primary tap used for F_{OUT}. This feature is useful in creating precise phase-related signals. The feature also provides an advantage in the control of the switch function, so that you can manage propagation-delay issues.

Figure 2 shows the schematic in Altera's Max+Plus II design software. This software allows the use of standard logic-gate symbols in schematic format to cre-

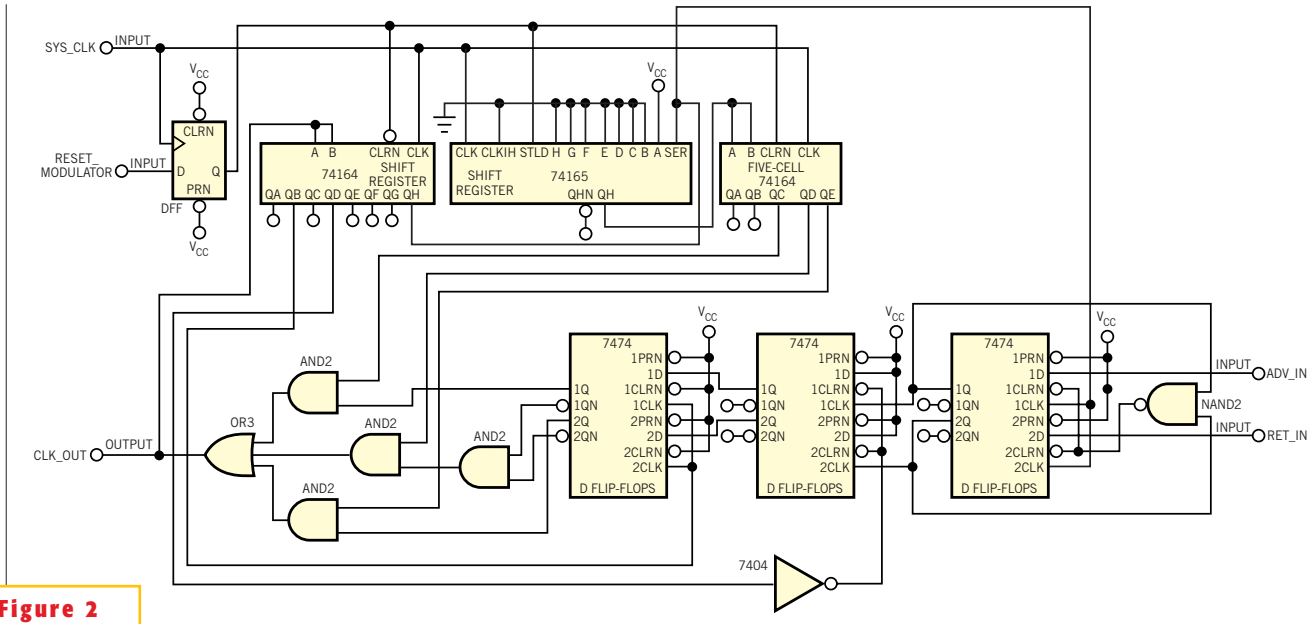


Figure 2

Altera's software allows you to enter standard logic-gate symbols to create a programmed CPLD.

(continued on pg 112)

ate a programming file for the device. Although this design uses a CPLD, a discrete version using digital-logic ICs, as the schematic shows, should also work. The F_{CLK} input connects to all the shift register's clock inputs. A Reset function initializes the registers with a single one and the rest zeros. Using a single flip-flop, F_{CLK} samples the asynchronous reset signal to ensure synchronous operation. Three sets of flip-flops prepare the Advance/Retard signal for use by the selection switch. From the right-hand side of **Figure 2**, the first set of flip-flops on the Advance and Retard inputs ensures that these signals are synchronous with the final output frequency, F_{OUT}, and stores them for the next cycle of F_{OUT}. We assumed that these signals would be asynchronous with the input clock, F_{CLK}. The NAND gate ensures that both of these flip-flops clear if Advance/Retard pulses arrive simultaneously, an illegal input condition.

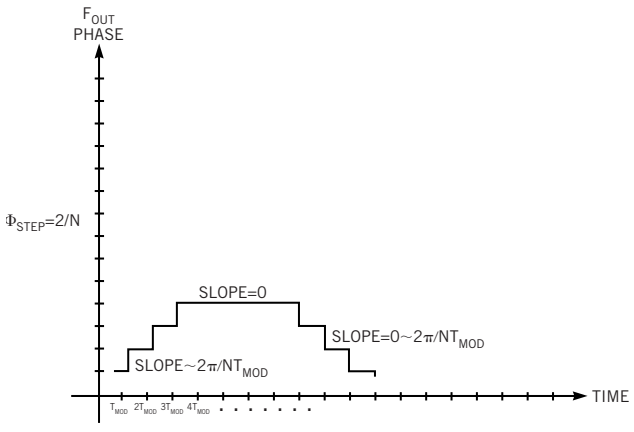


Figure 3 The stair-step portions of this graphic show where phase is added to or subtracted from F_{OUT}.

The second set of flip-flops captures the rising edges of the Advance/Retard inputs. Subsequent rising edges are ignored for a complete cycle of F_{OUT}. This set of flip-flops holds the state of the selection switch for the next cycle of F_{OUT}. After every cycle of F_{OUT}, these flip-flops reset to the divide-by-20 state. The output of the third set of flip-flops controls the AND/OR switch logic, which selects the divide ratio for the current cycle. As the single logic one shifts to the right, it first latches the selected switch position into the last set of flip-flops. This selection could be di-

(continued on pg 116)

vide-by-19, -20, or -21, depending on the Advance/Retard inputs. The AND/OR gates now can select which tap point connects to the shift register's input for that cycle of F_{OUT}. After one more shift, the single logic one clears the second set of flip-flops, thus returning to the divide-by-20 state.

A propagation delay is inherent in the Advance/Retard control inputs. If you apply an Advance/Retard pulse, it will not be applied to the selection of the tap point until the next cycle of F_{OUT}. We programmed the modulator into an Altera EPM7128-10 (10-nsec) device, and used an input-clock frequency, F_{CLK}, of 20 MHz. When the divide-select switch is in the divide-by-20 state, it is easy to compute the frequency output; it's just the input clock divided by 20. For an N-bit system, it would be the input clock divided by N. But how do you derive a general formula for F_{OUT} if Advance/Retard pulses arrive at a rate of F_{MOD}? Whenever an Advance or Return pulse is processed, a fixed amount of time is added or subtracted to the time between F_{OUT} pulses. You need an expression for the equivalent amount of added or subtracted phase—in other words, the phase step.

One complete cycle of F_{OUT} with no Advance/Retard modulation takes N/F_{CLK} seconds. This interval is just the period of the output with no modulation. If you add or subtract one clock period, how much phase does this represent with respect to $F_{OUT}=N/F_{CLK}$? In terms of the fraction of time that adding or subtracting one clock period from the nominal output cycle, you can write: Fraction of one output cycle per Advance/Retard pulse=(clock period)/(nominal-output period)$=(1/F_{CLK})(F_{CLK}/N)$ cycles$=1/N$ cycles.

Converting to radians and defining this step as the phase step or Φ_{STEP}, $\Phi_{STEP}=2\pi/N$ radians. Therefore, every time an Advance or Retard pulse is processed, the phase of the output changes by $\pm 2\pi/N$ radians. You can now use the fact that frequency is the time derivative of phase to derive the formula for F_{OUT}. **Figure 3** shows a time plot of phase of the output F_{OUT} for the three possible commands: Advance, Static (divide-by-N), and Retard. In **Figure 3**, at first phase is added, no change occurs in phase, and then phase is subtracted. The frequency is not changed where the slope is zero, and is equal to F_{CLK}/N. At the stair-step portions of the plot, you can approximate the slope as $\pm 2\pi/NT_{MOD}$. You can interpret this figure as the change in the output frequency (in radians). To convert to cycles, divide by 2π, which gives the change in output frequency as $\pm F_{MOD}/N$ for Advance or Retard pulses arriving at a rate of F_{MOD}.□

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Edited by Bill Schweber

Digitally control room light intensity

Donal McNamara, Analog Devices, Limerick, Ireland and Kieran Kelly, Analog Devices, Limerick, Ireland.

Many people favor different light and temperature settings for different rooms depending upon their mood or whether they are working or relaxing. The circuit in **Figure 1** controls the intensity of the artificial light in a room and monitors the temperature of two zones. The two main circuit blocks are the PIC16C67 master controller and the ADT7516 temperature-sensor interface, which includes a four-channel ADC and a quad voltage-output DAC. Other components include a photodiode and an op amp that monitor the ambient light; a rotary potentiometer that sets the light intensity; an LED bar array and display driver, which indicate the light-intensity setting; a light-dimmer-control circuit; and a 16×two-character LCD, which indicates the temperature of the two zones.

On power-up, the PIC16C67 configures its ports to control the LCD and the ADT7516. The ADT7516 has a dual interface, comprising I²C and SPI, so the master communicates in SPI mode. The ADT7516 operates in SPI mode, once the controller initializes the LCD.

The ADT7516 senses both its internal temperature and the temperature of a remote thermal diode (Q_1 configured as a diode), and the PIC16C67 displays these temperatures on the LCD. One of the ADT7516's analog inputs monitors a potentiometer that you adjust to set the required light intensity. The PIC controller reads the potentiometer value from the ADT7516 and outputs a corresponding DAC value. The DAC controls an LM3914 LED-bar-array controller that shows the potentiometer setting on the array. If you set the potentiometer half-

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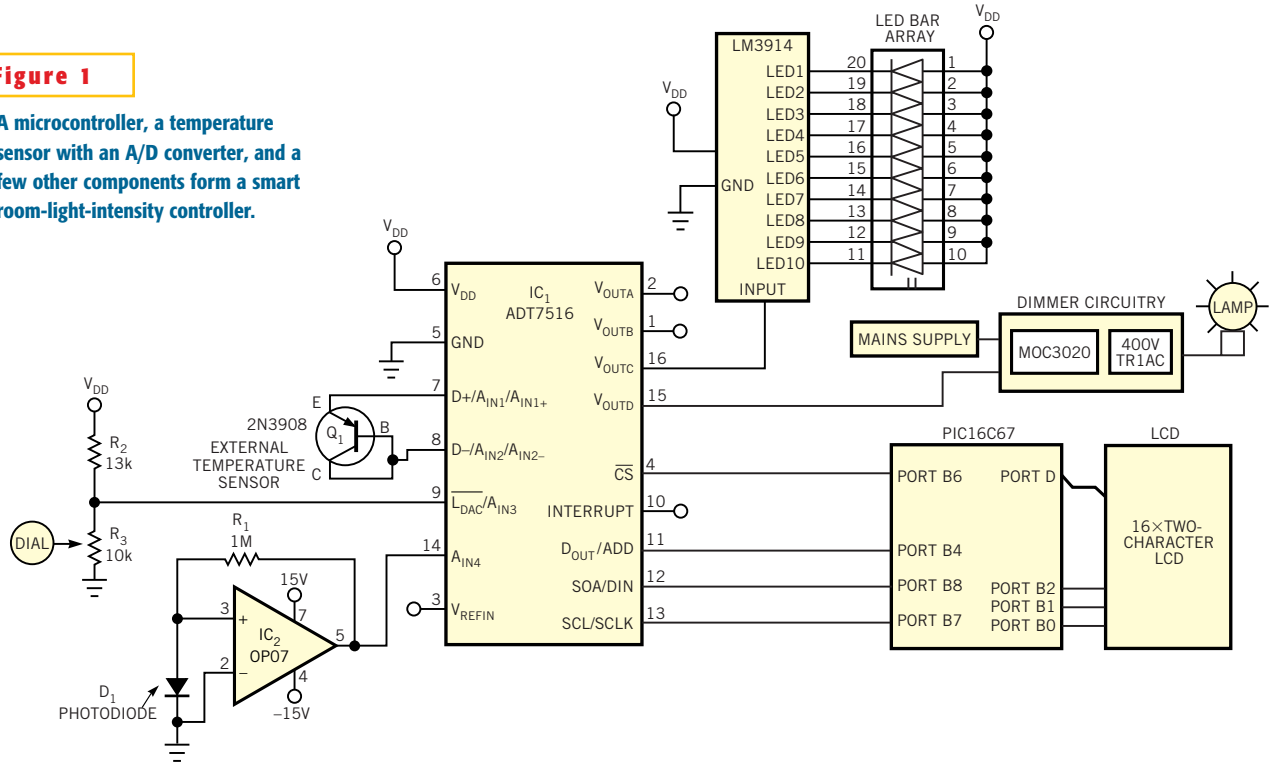
Figure 1

A microcontroller, a temperature sensor with an A/D converter, and a few other components form a smart room-light-intensity controller.



way, for example, then half of the LEDs turn on, indicating that you want an intensity that is half of what the light source can deliver.

A second DAC output controls a DIAC-based (X1) light-dimmer circuit. This dimmer circuit operates like any other light dimmer, except that the DAC controls it instead of a potentiometer. A photodiode monitors the intensity from the light bulb. An OP07 amplifies its output and feeds it into one of the ADT7516's analog inputs. The PIC controller uses the potentiometer and photodiode values, which the ADT7516 digitizes, to maintain equilibrium between the light intensity and the required light setting. If the photodiode reading is less than the potentiometer setting, the controller increases the dimmer DAC value; it decreases the dimmer DAC value if the reading is greater.

One of the features of the ADT7516 is its round-robin mode, in which it constantly monitors all of its measurement channels. The master need not initialize any conversions during its operation; all it has to do is read back from four value registers and act according to its program. This circuit ensures a constant light intensity within a room, saving power when daylight takes over as the main light source. It also extends the lifetime of a light bulb, thus saving on maintenance bills in a large office environment. You can also extend the application to include control of air conditioning and to memorize heat and light settings that suit individuals tastes.□

Circuit tests V_{COM} drivers

Soufiane Bendaoud, Analog Devices, San Jose, CA

Flat-panel LCD monitors offer excellent image quality and more compact form factor than CRTs—hence, their steadily increasing popularity. Unfortunately, the complexity of their manufacturing process makes LCD monitors considerably more expensive than CRTs. The amplifier that drives V_{COM}, the voltage on the backplane of the LCD panel, must be able to drive large capacitive loads, deliver high peak output currents, and maintain a constant output voltage. This Design Idea describes a simple test to measure the usefulness of an amplifier used as a V_{COM} driver. First, consider some video theory. Flat-panel television screens differ in the rate at which the screen refreshes. The refresh rate for TVs depends on the standard you use, such as NTSC, PAL, or SECAM. Computers, on the other hand, typically refresh the screen at a 75-Hz rate. A single picture element, or pixel, on an LCD screen comprises three subpixels, one each of red, green, and blue.

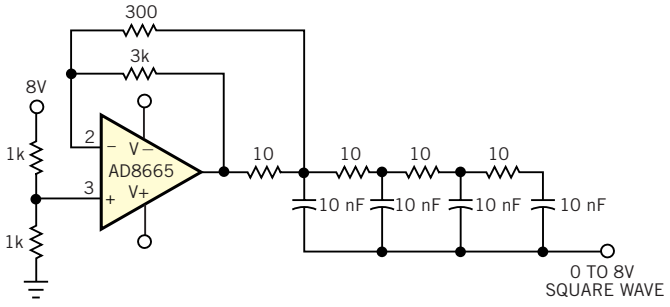


Figure 1 In this typical V_{COM} driver, an array of capacitors simulates the subpixel load.

Electrically, the subpixels behave like capacitors, storing a certain voltage until the next voltage arrives. Changing the voltages on the subpixels, one row at a time, refreshes the screen. These voltages use V_{COM} as a reference. The absolute value of the voltage differences, V_{COM}, represents the brightness of the subpixels. The video signal undergoes inversion on a frame-by-frame basis to ensure that the time average of the pixel voltages is zero, thus preventing screen burnout. The circuit of **Figure 1** tests the V_{COM} driver by applying a square wave to a capacitor array representing the subpixels in the panel. This circuit simulates the worst-case condition, in which all the subpixels switch on or off simultaneously. A pair of high-power, low-on-resistance MOSFETs generates the square wave. A nonoverlapping drive

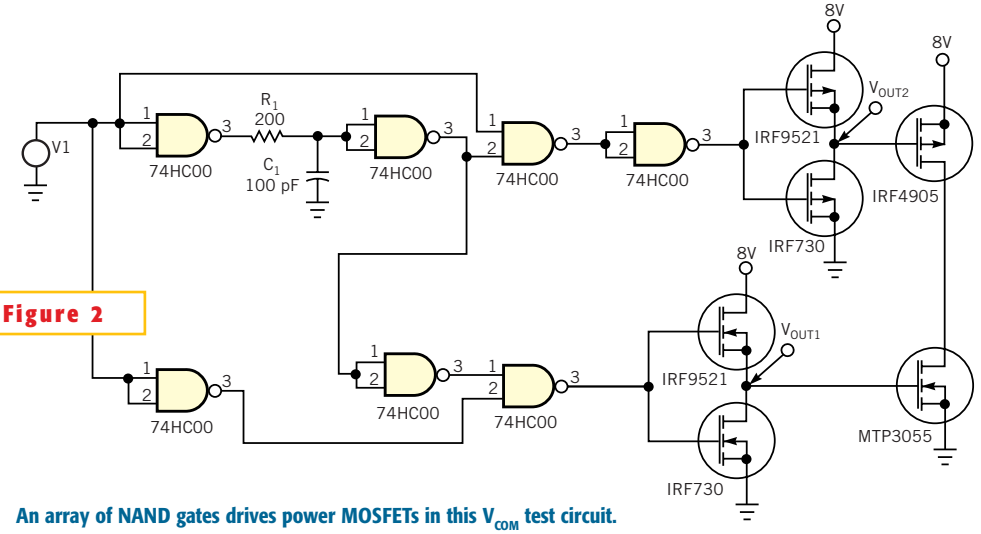


Figure 2 An array of NAND gates drives power MOSFETs in this V_{COM} test circuit.

scheme ensures that both MOSFETs do not turn on at the same time. Otherwise, simultaneous conduction would give rise to high shoot-through currents. **Figure 2** shows the MOSFETs and the nonoverlapping drive scheme. The drive scheme uses high-speed NAND gates. An RC network at the input of the second NAND gate controls the nonoverlap delay. The first pair of MOSFETs acts as predrivers to provide the current needed to drive the power-MOSFET output stage. **Figure 3** shows the nonoverlapping drive to the gates of the output stage. **Figure 4** shows the instantaneous peak output current of the AD8565 in **Figure 1** in response to a pulse from the test circuit.□

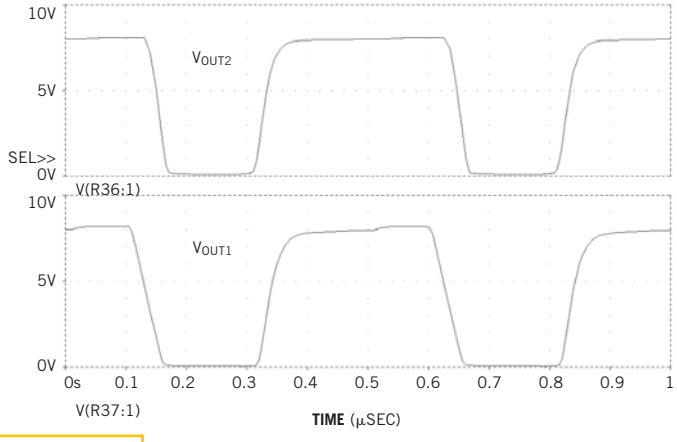


Figure 3 Nonoverlapping gate drive prevents large shoot-through currents in the output stage of Figure 2's circuit.

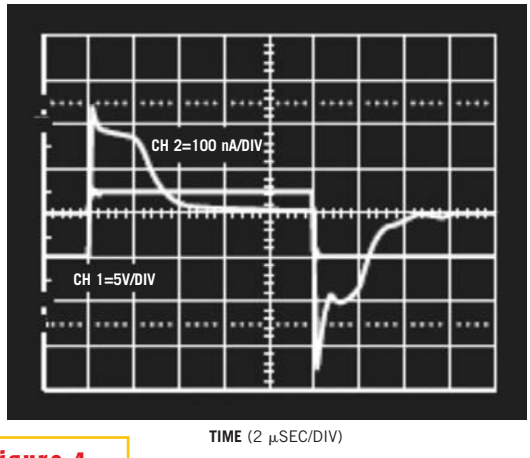


Figure 4 The AD8565 exhibits peak currents greater than 250 mA in response to a test-circuit pulse.

Use two picogate devices for bidirectional level-shifting

Bob Marshall, Philips Semiconductors

In new mixed-voltage systems, it is often necessary to level-shift a control signal from a high level to a low level. An open-drain device, such as the 74LVC1G07, easily performs this shift. However, when a bidirectional signal requires level-shifting, it takes a bit more circuitry, because simply tying two open-drain devices pins together generates just a latch function.

The circuit in **Figure 1** shows how to connect the 74LVC2G241 and 74LVC2G07 devices together to shift the signal at A from a high level to a low voltage at B and to shift a low level at B to a higher level at A. The $\overline{DIR}$ signal controls the direction of the transfer. When $\overline{DIR}$ is low, the A side is the input, and the B side is output. When $\overline{DIR}$ is high, B becomes the input, and A becomes the output. To have B behave as an input when the $\overline{DIR}$ signal is low, redo the circuit so that Pin 3 of the 74LVC2G241 becomes the input to Pin 1 of the 74LVC2G07 and Pin 4 of the 74LVC2G07 becomes the input to Pin 2 of the 74LVC2G241.

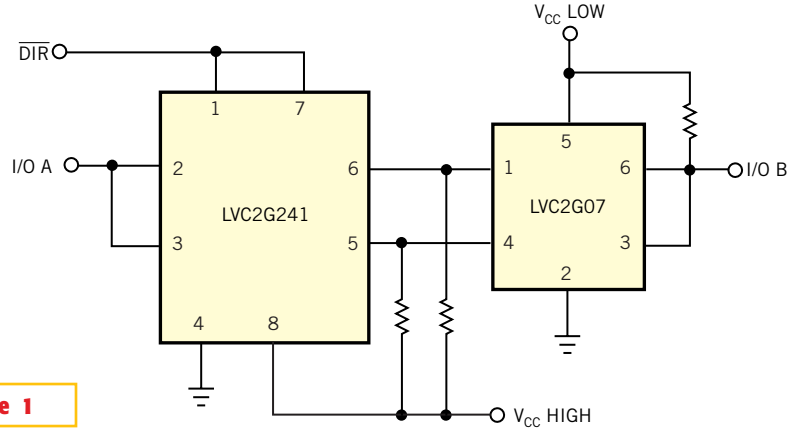


Figure 1 A two-IC circuit allows signal level-shifting in both directions; signal-flow direction is under circuit control.

The highest voltage V_{CC} should supply the 74LVC2G241, and the lowest voltage level supply necessary should supply the 74LVC2G07. For example, to shift a signal from 3.3 to 1.8V, the $1.8V_{CC}$ should supply the 74LVC2G07 device. The size

of the pullup resistor is unimportant, but, for best speed, it should be as small as practical to reduce the RC change time of the output signal of the 74LVC2G07. The current output of the74LVC07A is 24 mA at 3.3V; at that V_{CC}, the pullup resistor could be as low as 150Ω. It should be as large as possible to reduce power consumption.

The 74LVC2G07 supply level determines V_{OL} and V_{OH} at B. At 1.8V, the V_{OH} would be near V_{CC}, and V_{OL} is 0.45V or lower when driving a 4-mA load. The 74LVC2G07 and 74LVC2G241 provide a quick and easy way to obtain a bidirectional level translation and take up little board space.□

Simple nanosecond-width pulse generator provides high performance

Jim Williams, Linear Technology Corp

If you need to produce extremely fast pulses in response to an input and trigger, such as for sampling applications, the predictably programmable short-time-interval generator has broad uses. The circuit of **Figure 1**, built around a quad high-speed comparator and a high-speed gate, has settable 0- to 10-nsec output width with 520-psec, 5V transitions. Pulse width varies less than 100 psec with 5V supply variations of 65%. The minimum input-trigger width is 30 nsec, and input-output delay is 18 nsec.

Comparator IC_1 inverts the input pulse (**Figure 2**, Trace A) and isolates the 50Ω termination. IC_1's output drives fixed and variable RC networks. Programming resistor R_G primarily determines the networks' charge-time difference and, hence, delay at a scale factor of approx 80Ω/nsec.

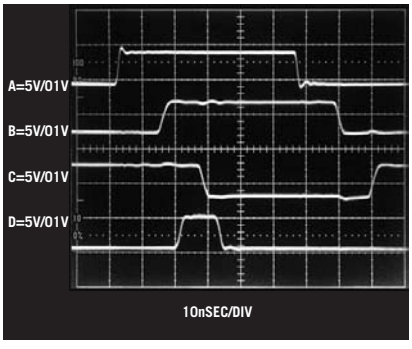


Figure 2 Pulse-generator waveforms, viewed in 400-MHz real-time bandwidth, include input (Trace A), IC_3 (Trace B) fixed and IC_2 (Trace C) variable outputs and output pulse (Trace D). RC networks differential delay manifests as IC_2-IC_3 positive overlap. G_1 extracts this interval and presents circuit output.

Comparators IC_2 and IC_3, arranged as complementary-output-level detectors, represent the networks' delay difference as edge-timing skew. Trace B is IC_3's fixed-path output, and Trace C is IC_2's variable output. Gate G_1's output (Trace D), which is high during IC_2-IC_3 positive overlap, presents the circuit output pulse. **Figure 2** shows a 5V, 5-nsec width, measured at 50% amplitude, output pulse with R=390Ω. The pulse is clean and has well-defined transitions. Post-transition aberrations, within 8%, derive from G_1's bond-wire inductance and an imperfect

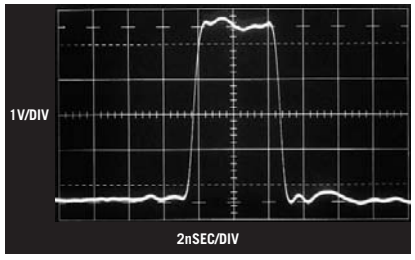


Figure 3 The 5-nsec-wide output with R=390Ω is clean with well-defined transitions. Post-transition aberrations are within 8% and derive from G_1 bond-wire inductance and an imperfect coaxial probe path.

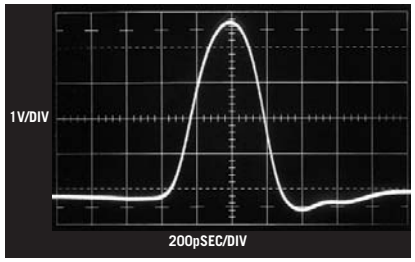


Figure 4 The narrowest amplitude pulse width is 1 nsec, and the base width measures 1.7 nsec. Measurement bandwidth is 3.9 GHz.

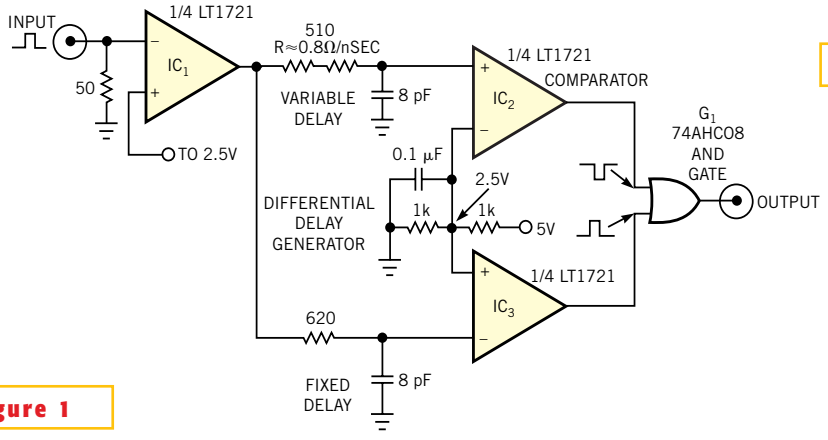


Figure 1 This pulse generator has 0- to 10-nsec width and 520-psec transitions. IC_1 unloads termination and drives the differential delay network. The IC_2-IC_3 complementary outputs represent delay difference as edge timing skew. G_1, which is high during IC_2-IC_3's positive overlap, presents circuit output.

coaxial probing path. **Figure 3** shows the narrowest full amplitude, 5V pulse available. Width measures 1 nsec at the 50% amplitude point and 1.7 nsec at the base in a 3.9-GHz bandwidth. Shorter widths are available if partial amplitude pulses are acceptable. **Figure 4** shows a 3.3V, 700-psec width (50%) with a 1.25-nsec base. G_1's rise time limits minimum achievable pulse width. The partial-amplitude pulse, 3.3V high, measures 700 psec with a 1.25-nsec base (**Figure 5**). **Figure 6**, taken in a 3.9-GHz sampled bandpass, measures 520-psec rise time. Fall time is similar. The transition of the probe edge is well-defined and free of artifacts.□

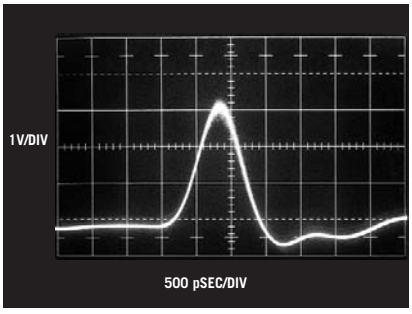


Figure 5 The partial-amplitude pulse, 3.3V high, measures 700 psec wide with a 1.25-nsec base. The trace granularity is an artifact of the 3.9-GHz-sampling-oscilloscope operation.

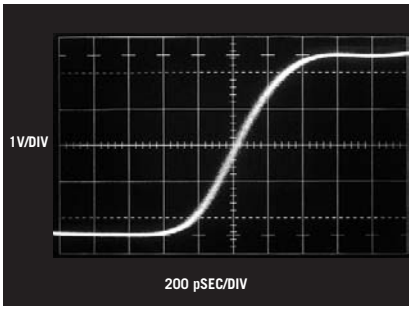


Figure 6 A transition detail in the 3.9-GHz bandpass with rise time of 90 psec shows 520-psec rise time; fall time is similar. The granularity derives from sampling-oscilloscope operation.

Accurately measure resistance with less-than-perfect components

Dave Van Ess, Cypress Semiconductor

For transducers, such as strain gauges or thermistors, you must accurately and inexpensively measure resistance using circuitry built with imperfect components and in which gain and offset errors can significantly limit the accuracy of ohmic measurements. The right circuit topology makes it possible to eliminate most error terms while measuring ohms, leaving the accuracy to be determined by just a single reference resistor.

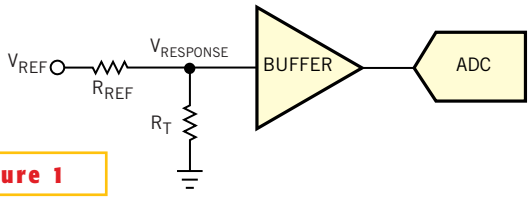


Figure 1 The resistive-divider topology provides a lower cost alternative to a current source and a precision resistor for calibration.

Unlike measuring voltage or current, measuring a passive attribute, such as resistance, requires a stimulus. One method of measuring resistance is to force a known current through a resistor and measure the voltage across the resistor. Measuring ohms in this way means that, with the correct selection of stimulus current, you need do no math, so this method was popular when the cost of computation was more than the cost of building an accurate current source. However, the accuracy of the current source directly limits the accuracy of the reading and any gain or offset errors from measuring the response voltage offsets the accuracy, as well. Additionally, the range of measurement is limited to the ADC's signal range, as the following equation shows:

$$R_T(MAX) = \frac{V_{RESPONSE}(MAX)}{I_{STIM}}.$$

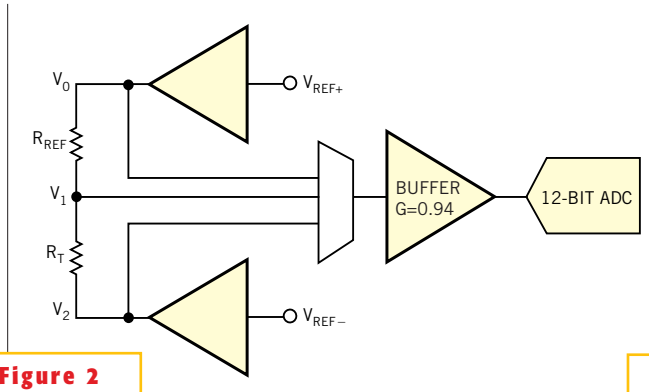


Figure 2 Remove most gain and offset errors using two measurements and a ratio calculation.

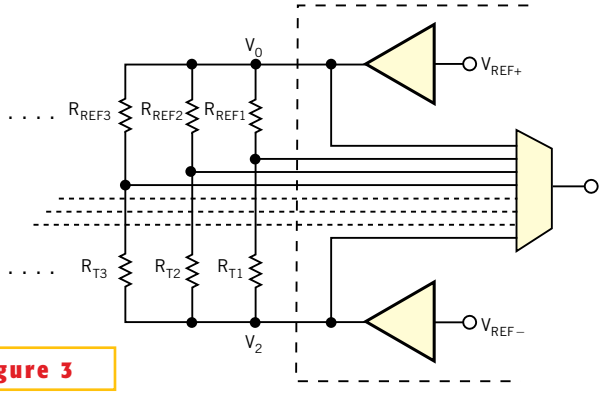


Figure 3 Extend the idea to handle multiple sensors and signal paths, using multiplexing through a single buffer and A/D converter.

With the development of more powerful microcontrollers and on-chip ratiometric ADCs, a resistor-divider block architecture (**Figure 2**) provides a less expensive approach:

$$R_T = R_{REF} \times \frac{V_{RESPONSE}}{V_{REF} - V_{RESPONSE}}.$$

This architecture has a theoretical range of measurement from short circuit to open circuit, but any offset error from measuring the response voltage limits the actual range; the reference resistance limits overall accuracy and any gain and offset errors from measuring the response voltage.

The cost of the reference resistor determines the error that the reference resistor introduces, and you derive the supply voltage, V_{CC}, from the reference voltage, V_{REF}. The gain error of a ratiometric ADC is generally small and does not contribute much to the overall error, but this situation is not the case for the offset error, which can be the largest contributor of error to the overall accuracy. Using more expensive and precise components reduces the offset error of any op amps in the measurement path.

Figure 2 shows how to significantly remove gain and offset errors, in which subtracting two measured voltages removes any offset errors in the measurement system:

$$R_T = R_{REF} \times \left(\frac{V_1 - V_2}{V_0 - V_1} \right).$$

The ratio of these two difference values removes any measurement-path gain error, leaving the reference resistance to determine the measurement error. This result is valid as long as the measured signal is never outside the range of the A/D converter. To guarantee this condition, set the sense buffer gain to slightly less than unity.

You can also measure multiple resistors, in which all the sense paths multiplex to a single buffer and A/D converter, and the eight analog pins let you measure as many as six transducers (**Figure 3**). Alternatively, you could connect each of four sense paths to its own buffer and converter.

Listing 1 at the Web version of this Design Idea at www.edn.com shows how you implement the circuit of **Figure 2** using a programmable analog system-on-chip controller. It uses the ADCINC12 user module, programmable-gain-adjustment user module, and two analog output buffers. Placing the analog block of the ADCINC12 just below the buffer and setting the clock for the ADCINC12 to 167 kHz for a sample rate of 10 samples/sec remove any 50- or 60-Hz interference from the signal. Increase the sample rate if the application requires a faster conversion. The control software is in C; the program calculates the resistance reading and leaves it in a global memory location.□

Edited by Brad Thompson

Quickly find pc-board shorts with low-cost tracer technique

Teno P Cipri, Engineering Expressions Consulting

A predominant failure mechanism for production pc boards is shorted traces. Finding hidden shorts is often time-consuming and frustrating. Typical techniques of cutting traces, lifting pads, and "blowing" shorts are, at best, questionable because they may affect the reliability of the circuit, and the ever-decreasing geometries and lower voltage ICs make these practices tricky and risky. High-end, four-wire DMMs (digital multimeters) or ohmmeters, which can accurately measure the small resistance values, are expensive and sometimes not available on a designer's bench.

An inexpensive alternative approach for finding short circuits, using the concepts of four-wire DMMs and ohmmeters is simple and requires only the tools you already have on your bench and a basic understanding of Ohm's Law. This approach uses the principal that all conductors have resistance properties, and a distinct voltage drop exists between the various nodes in the shorted circuit. This approach systematically locates the nodes with lowest impendence between them and isolates the fault to two nodes.

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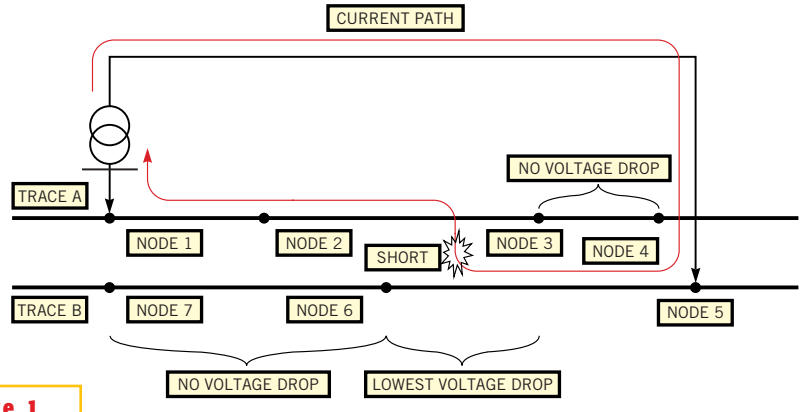


Figure 1

By applying a fixed current to various nodes and looking at the resultant voltage drops, you can home in on the likely location of a pc-board short circuit.

Most digital buses have at least 1Ω over the length of the run, but a trace impedance of only 200 mΩ still has a 2-mV drop with 10-mA current applied. Most lab-grade handheld DMMs can easily resolve to 1 mV. Because you are looking for relative values, the absolute accuracy of the instrument isn't critical. However, the current must be constant to achieve repeatable results, and you must isolate its current source from the ground of the circuit under test.

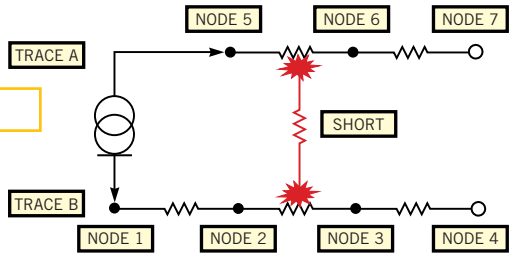
A 1.5V battery in series with a 1.5-kΩ resistor is an adequate current source for this purpose. The battery provides the isolation and relatively constant voltage; select the resistor to source around 10 mA. (For lower impedance traces, such as power-supply lines, or in situations in which the DMM lacks millivolt resolution, use a higher current.) An optional clamping diode, with a cathode connected to the battery's negative terminal and an anode connected to the resistor's free end, provides protection for low-voltage logic circuits. If you use the diode, you may also need to add a power switch to keep the battery from depleting when the circuit is not in use.

A node can be any accessible part of the circuit path under test, such as a via, a pad, or a test point (**Figure 1**). Note the current path: When current is flowing between two nodes, a minute voltage drop occurs across the two nodes. When the current doesn't flow between two nodes, there is no voltage drop across those nodes.

To find the short in this example, put one DMM probe on any node on Trace A and the other on any node on Trace B, and note the voltage drop. In this example, if you had started with the positive probe on Node 1 and the negative probe on Node 5 and moved the negative probe to Node 6, you would note a slight voltage drop. Next, you move the probe to Node 7 and note that the voltage drop is equivalent to the voltage drop at Node 6. From this test, you can deduce that the short must exist between nodes 5 and 6 because no current flows from Node 6 to Node 7. Then, move the positive probe to Node 2 and note a small voltage drop.

Continue down the line to Node 3 and note another small drop. Next, probe Node 4 and note there is no voltage drop. You can now deduce that the short must be between nodes 2 and 3 and nodes 5 and 6.

Figure 2



The equivalent circuit of the pc-board layout shows the principal of the source-and-probe technique.

Redrawing **Figure 1** with the equivalent circuit in **Figure 2** makes clear how this technique works. You are now looking at a simple series network of resistors and looking for voltage drops across any resistor that has current flowing through it. When a node is outside the current path, no voltage drop occurs. By understanding the relationship of each of the vias and their position in the current path, you can systematically isolate the short by looking for lower voltage (current flowing) or higher voltage (current not flowing). When current is flowing, the short is farther from the current source. If no current is flowing, then the short is closer to the current source. This two-valued logic makes it simple to isolate the problem. The beauty of this technique is that it doesn't matter to which two nodes the current source is connected, as long as one side of the current source is connected to any node on Trace A and the other side of the current source is connected to any node on Trace B.

In this example, the short is between two node pairs, and you can isolate the short only to those pairs. A little knowledge of the board layout and common sense now come into play. You need to know only where the two traces are adjacent between nodes 5 and 6 and nodes 2 and 3, and you have found the most likely place for the short. If it is underneath a component, you have to remove the component; removing the component often removes the short. If the short is on an internal layer, you may have to do some selective cutting and jumping to isolate the short from the traces, but at least you minimize the number of cuts on the board.□

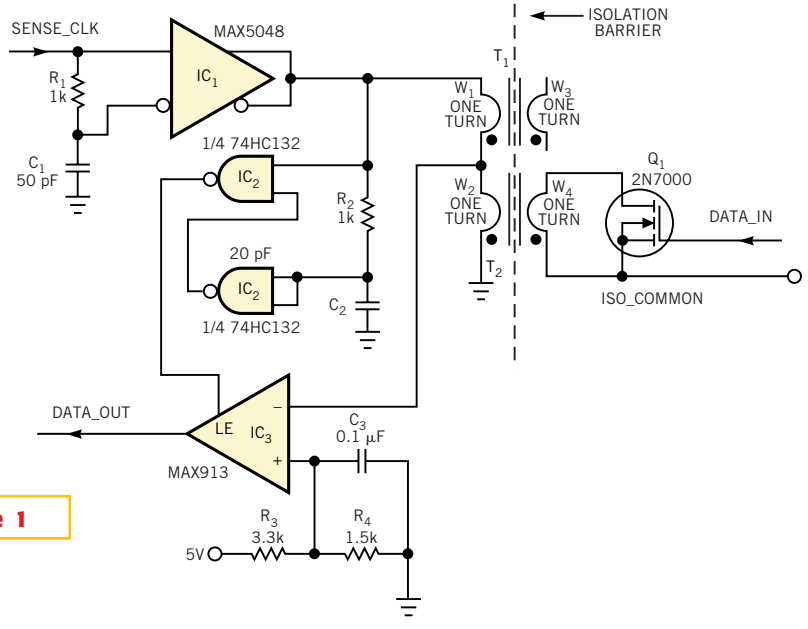
Read isolated digital signals without power drain

Alfredo H Saab and Joseph Neubauer, Maxim Integrated Products Inc, Sunnyvale, CA

Although optocouplers offer designers a straightforward method of establishing galvanic isolation between circuits that operate at different ground potentials, they do not provide an ideal approach. An optocoupler draws power from the isolated circuit, switches relatively slowly, and loses current-transfer ratio as its light emitter ages.

The circuit in **Figure 1** overcomes these limitations by replicating a digital signal's state, drawing no power from the isolated input, and consuming only modest power on the nonisolated side. As **Figure 2** shows, the circuit imposes only a 20-nsec input-to-output delay from the positive edge of SENSE_CLK to DATA_OUT.

Figure 1



You can use a simple ferrite-bead transformer to isolate logic-level signals.

MOSFET transistor Q_1 operates in either of two states—high resistance between source and drain ($R_{DS/OFF}$), or low resistance ($R_{DS(ON)}$) when a control signal drives Q_1 into conduction. When conducting, Q_1 imposes a low resistance across T_1's secondary winding, W_3. The remainder of the circuit senses the state of T_1's secondary resistance. Resistor R_1, capacitor C_1, and the complementary inputs of MOSFET-driver IC_1 differentiate the SENSE_CLK signal's positive-going input edge, producing a positive-going 5V pulse at IC_1's output and driving one end of winding W_1. **Figure 2** shows the relationship among the circuit's signals.

Connected in series-aiding mode, the two primary windings W_1 and W_2 of T_1

form a 2-to-1 inductive voltage divider whose center tap drives the inverting input of IC_3, a high-speed comparator. With Q_1 off and thus presenting an open circuit across the secondary of T_1, the junction of windings W_1 and W_2 applies a pulse of approximately 2.5V to comparator IC_3's inverting input and drives IC_3's internal state low. Meanwhile, IC_2's two gates, resistor R_2 and capacitor C_2 generate a short strobe pulse in the middle of IC_1's output pulse and applied to IC_3's LE (latch-enable) input.

Latching IC_3's internal state to its external output (DATA_OUT) produces a logic-low output that follows DATA_IN. If DATA_IN goes sufficiently positive to bias Q_1 on, Q_1's low resistance across W_3 reflects a low impedance to windings W_1 and W_2 of T_1. The reduced pulse amplitude at the junction of W_1 and W_2 and IC_3's inverting input of approximately 0.5V is insufficient to trigger IC_3, and IC_3's internal state goes high. The latching pulse at LE forces IC_3's DATA_OUT high, again following the state of DATA_IN.

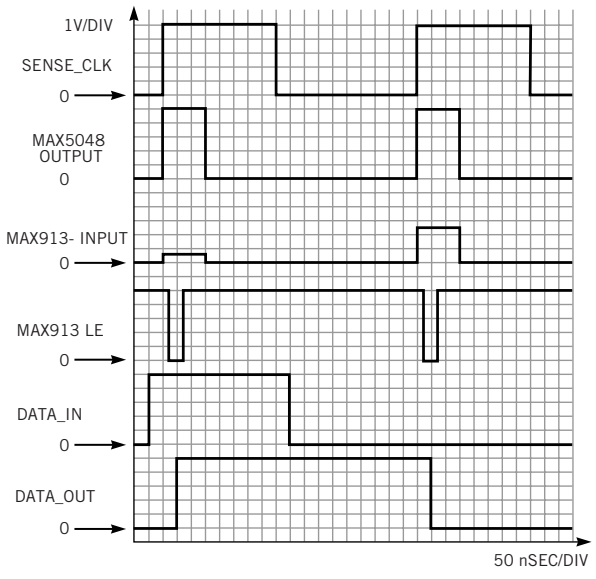


Figure 2 Each positive-going transition of SENSE_CLK transfers the state of the galvanically isolated digital signal at DATA_IN to DATA_OUT.

IC_1, IC_2, and IC_3 operate from a single 5V power supply. Separate bypass capacitors placed adjacent to each device's power pins minimize noise. Resistors R_3 and R_4 set IC_3's trigger-voltage threshold. Transformer T_1 provides a 1-to-1-to-1 turns ratio and comprises a single-hole ferrite bead (Fair-Rite part number 2673000101) with three identical single-turn windings. To minimize stray inductance, keep the connection to the junction of windings W_1, W_2, and IC_1 as short as possible. Also, the grounded end of W_2 should return to IC_1's ground connection.

The circuit's isolation capabilities depend on its pc-board layout and the properties of transformer T_1, whose type 73 ferrite core is moderately conductive. Thus, T_1's isolation properties depend on its windings' insulation. For example, Teflon or Kapton-insulated wire can withstand several kilovolts. If you carefully construct T_1 using the specified core and Teflon-insulated AWG #24 wire, the transformer can exhibit interwinding capacitances of 0.2 pF or less.□

MOSFET shunt regulator substitutes for series regulator

Stuart R Michaels, SRM Consulting

You would normally use a series linear regulator or a dc/dc converter to obtain 3V dc from a higher supply. However, when breadboarding a concept, you may be able to use a shunt regulator, especially if a series regulator of the correct voltage is unavailable. The MOSFET in **Figure 1** can replace a zener diode in a shunt regulator and provide lower output impedance than a zener diode.

The MOSFET is self-biased by connecting its drain to its source. The difference between the input voltage and the gate-to-source threshold voltage, V_{GS}, sets the current. The IRF521 in this example has a threshold voltage of 2 to 4V at 250 μA. The upper curve of **Figure 2** shows that the IRF521 achieves a gate-to-source voltage of 3V at a current of about 200 μA. MOSFETs can vary from device to device, but the typical MOSFET has a threshold at approximately the mean between the maximum and the minimum limits.

The lower curve in **Figure 2** is the output impedance, which you obtain from the upper curve by differentiating the upper curve. Although the output impedance, R_{OUT}, is near 800Ω at a current of 100 μA, it rapidly drops to less than 6Ω at 50 mA. Because you operate the MOSFET at or near threshold, its on-resistance spec doesn't apply, and the output impedance of this circuit is far higher than you would expect from the on-resistance. However, in general, the lower the on-resistance, the lower the output impedance at a specific current near threshold.

This circuit may require that R_2 and C_1 stop the oscillation in the MOSFET. Add a filter capacitor to the output to minimize the effect of load transients. Connecting a large filter capacitor from the gate to the source with short leads eliminates the need for R_2. You can use other

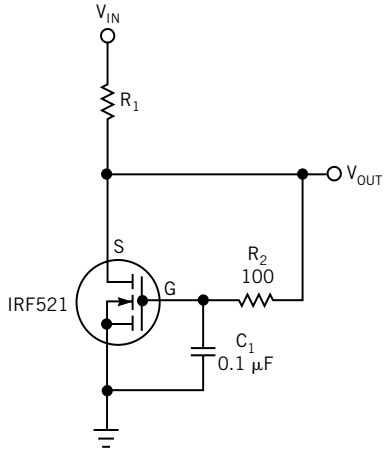


Figure 1 A MOSFET configured to replace a zer diode of a shunt regulator provides lower impedance than a diode-based implementation.

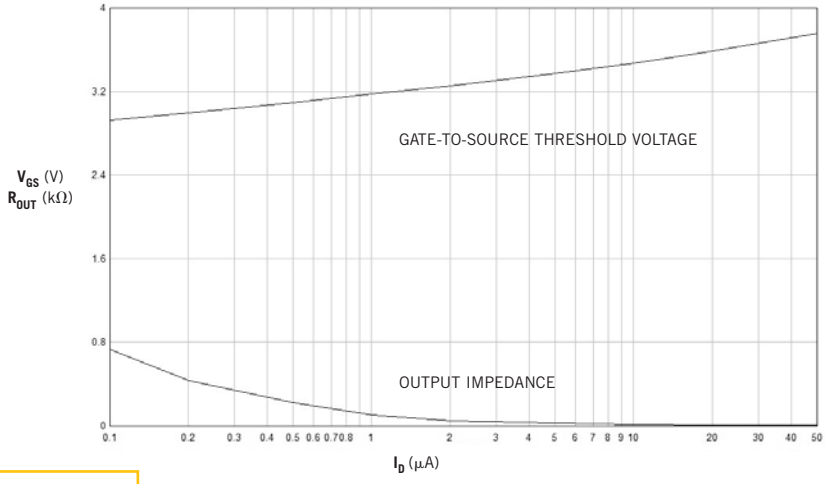


Figure 2 A plot of key parameters—gate-to-source voltage and output impedance—versus drain current shows smoothness of variation over two and one-half decades.

MOSFET families and other voltages if necessary.

Although you may be unable to get the exact output voltage you need at the current you prefer, many devices tolerate wide variations in operating voltage. For instance, many 3.3V-dc microcontrollers can operate as low as 2.5V dc and as high as 3.6V dc. Note that operating a MOSFET near its threshold causes a large negative-temperature coefficient of the gate-to-source voltage. This circuit has significant change in output voltage over a wide temperature range; it is suitable for only limited temperature ranges.□

Zener test circuit serves as dc source

John Jardine, JJ Designs, West Yorkshire, UK

This Design Idea describes a versatile test circuit for zener diodes after yet another misread zener diode had infiltrated the ranks of 1N4148 diodes assembled on a pc board. As a bonus, the circuit can serve as a moderate-voltage, power-limited adjustable dc source. Although conventional multimeters' resistance ranges typically apply enough voltage to forward-bias most diodes, few can drive a zener diode into reverse conduction. **Figure 1a** shows a simple variable-frequency dc/dc step-up converter whose output voltage depends on the device under test's breakdown voltage.

Upon power application, Pin 3 of IC_1 (one section of a 74HC132 quad dual-input Schmitt-trigger NAND gate) goes to logic one and switches on Q_1, an N-channel logic-level power MOSFET. Current flows through Q_1 and R_6 and stores energy in inductor L_1's magnetic field. Zener diode D_1 limits the voltage at IC_1's Pin 1 to 4.7V. Simultaneously, diode

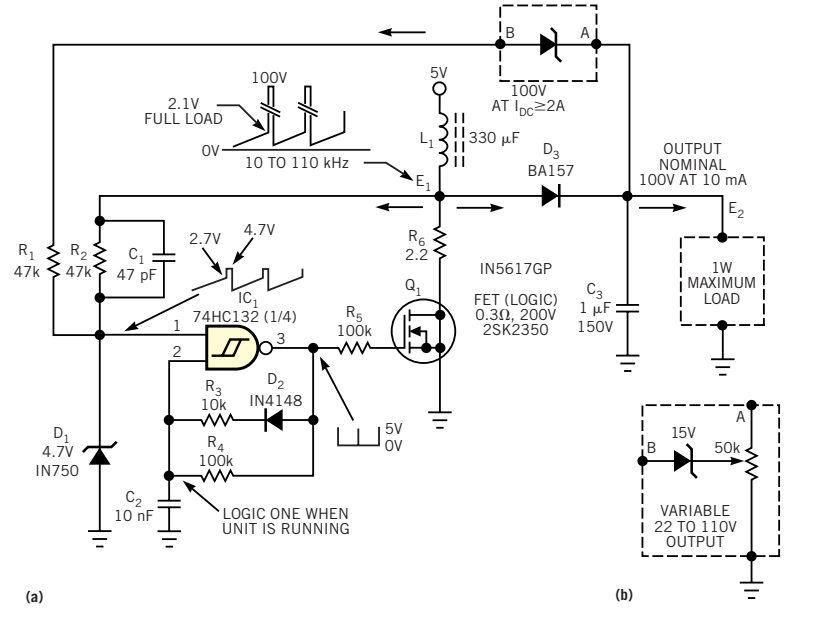


Figure 1 The output voltage of a simple variable-frequency dc/dc step-up converter depends on the device under test's breakdown voltage (a). To use the circuit as a variable medium-voltage power supply, replace the device under test with a network (b).

D_2 and resistor R_3 charge C_2 and establish a logic one at IC_1's Pin 2. When the voltage at point E_1 reaches approximately 2.7V, IC_1's input-voltage threshold, IC_1's output goes to logic zero, switching off Q_1.

Energy stored in L_1's magnetic field discharges through fast-recovery diode D_3 and charges C_3. Capacitor C_1 helps remove diode D_1's stored charge and helps restart the charging cycle.

After several cycles, the voltage at E_2 reaches the device under test's reverse-breakdown voltage and feeds current via R_1 to IC_1's Pin 1. As a result, the voltage at E_2 stabilizes at the sum of the device under test's reverse-breakdown voltage and a constant offset voltage of 5.4V comprising the voltage across D_1—4.7V—plus the forward voltage across D_3—0.7V. Thus, for a 100V zener as the device under test, the voltage at E_2 measures approximately 105.4V.

At start-up and under fault conditions, resistor R_4, diode D_2, and resistor R_3 produce an asymmetrical oscillation at approximately 2 kHz, which reduces the average current through L_1 and Q_1 to a safe level.

To use the circuit as a variable medium-voltage power supply, replace the device under test with the network in **Figure 1b**. Adjusting the potentiometer varies the voltage at point E_2 from 22 to 120V. Maximum current available from the circuit depends on the dc resistance, L_1's magnetic-saturation characteristics, and Q_1's on-resistance. For a nominal 5V power supply and 430 mA of input current, the circuit delivers 10 mA at 100V for a 100V output, yielding an efficiency of approximately 50%. Feeding L_1 from a separate 12V power supply improves efficiency.

If you design your own inductor for L_1, aim for a nominal inductance of 330 µH at 2A and a dc winding resistance of less than 0.5Ω. For optimum operation, use a fast-recovery diode for D_3 and a logic-level N-channel MOSFET with a breakdown voltage of 200V or greater and an on-resistance of less than 0.3Ω for Q_1. Note that zener-diode manufacturers specify breakdown voltages at specific test currents. Also, when you subject them to high reverse voltages, signal diodes exhibit zener behavior.□

Gain-programmable circuit offers performance and flexibility

Luo Bencheng, Key Laboratory of Mental Health, Institute of Psychology, Chinese Academy of Sciences

You can use a standard precision instrumentation amplifier, such as the INA118 or AD623, as a gain-programmable amplifier with high accuracy and wide gain range. However, the gain range of such parts is fixed at certain values, limiting their flexibility. To solve the problem, a usual way is to use a gain-adjustable circuit controlled by a microcomputer (**Figure 1**).

IC_2 is a programmable 1-of-8 analogy multiplexer that connects to eight weighting resistors, R_1 to R_8, to improve the gain range of the circuit based on IC_2, a general-purpose precision amplifier. The overall gain of the circuit depends on the value of the selected weighting resistor, as follows:

$$V_{OUT} = -V_{IN}\left(\frac{R_X + R_{ON}}{R_0}\right),$$

where R_{ON} is the on-resistance of IC_2, and R_X is one of the selected weighting resistors, R_1 to R_8. You control the port-select pins Z_0 to Z_2 of IC_2 with a microcontroller to provide self-adjustable gain according to the selected weighting resistor. Unfortunately, the performance and quality of the circuit cannot provide good performance and high quality due to the on-resistance of IC_2, which you also cannot control, especially as the temperature changes.

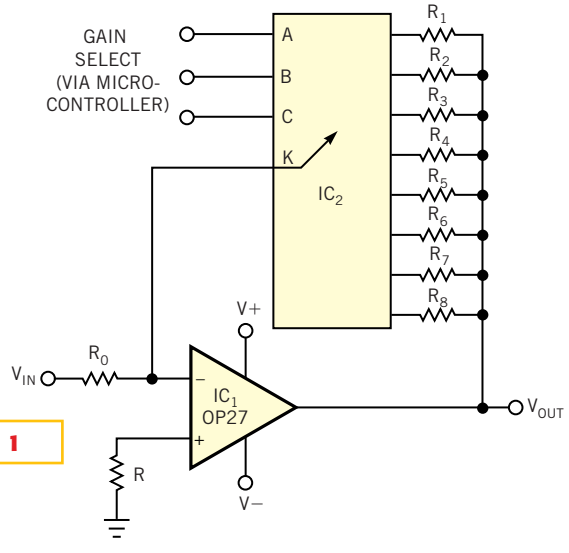


Figure 1

A basic gain-programmable amplifier circuit uses digital outputs from a microcontroller to set gain.

The modified gain-adjustable amplifier circuit in **Figure 2** uses the same IC_1 but changes IC_2 to a programmable 2-of-8 difference-input analog multiplexer, which connects to four balancing resistors, R_{01} to R_{04}, and eight weighting resistors, R_{G1} to R_{G8}, to improve the gain range of the circuit. By controlling the port-select pins Z_0 to Z_1 of IC_2 with a microcontroller, the

circuit provides self-adjustable gain with high quality. The overall gain of the circuit is:

$$V_{OUT} = V_{IN}\left(1+\frac{R_{GB}}{R_{GA}}\right),$$

where R_{GA} is one of the selected weighting resistors, R_{G1} to R_{G4}, and R_{GB} is one of the selected weighting resistors, R_{G6} to R_{G8}.

Analog multiplexer IC_2 is on the input side of amplifier IC_1. Resistors R_{01} to R_{04} balance the signal-input channel to decrease the level-shifting because of the on-resistance of multiplexer IC_2 and minimize the effect of that resistance. Additionally, two operational amplifiers, IC_{01} and IC_{02}, act as followers to improve the overall driver performance and common-mode-rejection capacity of the circuit.□

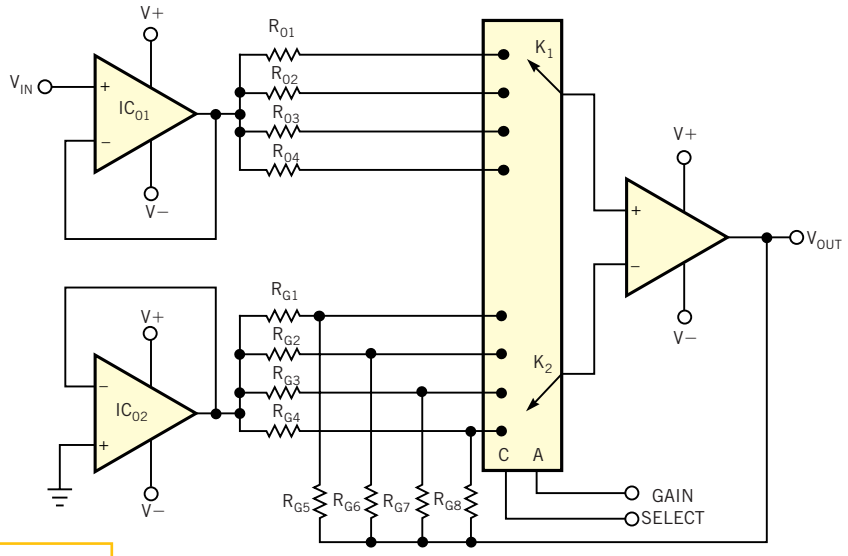


Figure 2

The modified circuit provides more flexibility, along with high performance.

Edited by Brad Thompson

Dual-output nonisolated SMPS powers appliances

Fabio Cacciotto, STMicroelectronics, Catania, Italy

Modern appliances offer a range of features that rely heavily on microcontrollers and auxiliary circuits. Although conventional iron-core transformers can provide ac line-isolated, low-voltage power for a microprocessor, coupling the processor's control signals to line-side power switches requires yet another layer of electrical isolation, such as optocouplers or pulse transformers.

Designers can avoid the complexity and expense of adding isolation components by powering the microcontroller and its auxiliary circuits from the nonisolated ac line. An offline SMPS (switched-mode power supply) can easily produce a single low voltage, but obtaining multiple voltages can prove more challenging and require a relatively complicated design.

As an alternative, you can use a single-chip SMPS controller, such as STMicroelectronics' Viper22A, IC_1, to derive as much as 3.3W of regulated dual-voltage power over an ac line-voltage range of 88 to 265V ac (**Figure 1**). For the values in the **figure**, this circuit delivers −5V±5% at currents as high as 300 mA and −12V±10% at currents as high as 150 mA.

The Viper22A's internal circuitry includes a 60-kHz clock oscillator, a voltage reference, overtemperature protection, and a high-voltage power MOSFET that can provide several watts of power. Although the Viper22A occupies an eight-lead package, operating requires only four connections: operating power, V_{DD}; feedback, FB; and the MOSFET's source and drain. The remainder of the pins, redundant source and drain connections, help dissipate heat into the pc board.

Resistor R_4 limits input surge current and doubles as a protective fuse. Diode D_1 rectifies the ac line voltage, providing approximately 160V dc to a filter comprising C_1, R_1, L_1, and C_2. In addition to smoothing dc ripple, the filter reduces

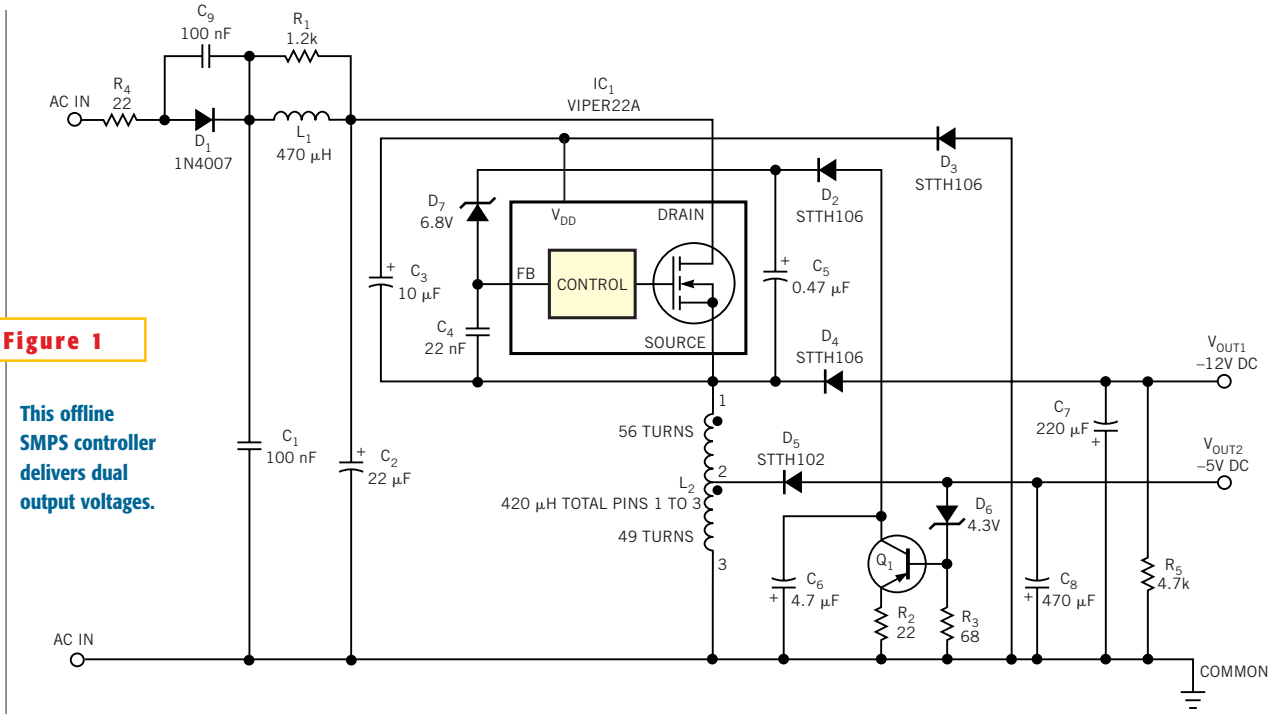


Figure 1

This offline SMPS controller delivers dual output voltages.

electromagnetic interference to help achieve compliance with EU standard 55014 CISPR14. Snubber capacitor C_9 across D_1 helps further reduce conducted emissions.

Reservoir capacitor C_3 acquires a positive charge via diode D_3 during the MOSFET's off-time and supplies V_{DD} to IC_1 during the MOSFET's on-time. Reverse voltage across D_3 can reach the sum of the peak rectified line voltage plus the magnitude of the maximum regulated dc output voltage, so use a fast-recovery diode rated for 600V peak-inverse voltage for D_3.

The voltage at V_{OUT2} provides feedback to close the regulation loop. The sum of general-purpose PNP transistor Q_1's base-emitter voltage plus D_6's reverse voltage sets V_{OUT2} at −5V. Zener diode D_7 shifts the voltage at IC_1's feedback input terminal into its linear range (0 to 1V).

To avoid high-frequency instability in the compensation loop, keep connections to ceramic capacitor C_4 as short as possible. Inductor L_2 comprises a TDK SRW0913 ferrite drum core with two windings whose turns ratio sets the output voltage at V_{OUT1}. To maintain regulation when V_{OUT1} is unloaded and V_{OUT2} is fully loaded, add bleeder resistor R_5 from V_{OUT1} to common ground.□

High-voltage amplifier drives piezo tubes

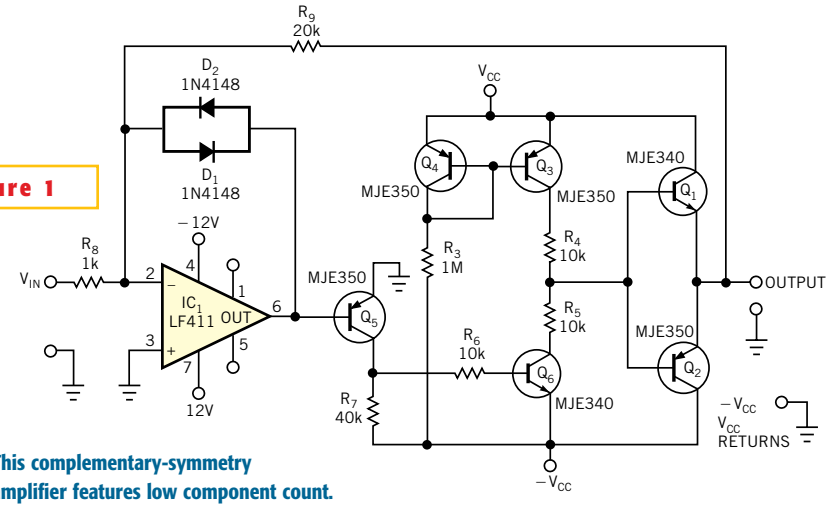
Bipin Duggal, Netaji Subhas Institute of Technology, New Delhi, India

Piezoelectric tubular positioners that drive manipulators in scanning tunneling microscopes require high-voltage, low-current drive circuits. The circuit in **Figure 1** can drive high-resistance, low-capacitance piezoelectric loads at a −3-dB bandwidth of 6 kHz. It offers a low-cost alternative to commercial drivers. Transistors Q_3 and Q_4 form a current mirror, with R_3 setting Q_4's collector current as the following equation determines: $I_C3=I_C4=[V_{CC}-(-V_{CC})-V_{BE}(Q_4)]/R_3$. Operational amplifier IC_1 provides base drive to Q_5, which in turn drives Q_6. With no signal applied to IC_1's input, the collector currents of Q_6 and Q_3 balance, and the output taken from the junction of emitter followers Q_1 and Q_2 rests at 0V.

Applying an input signal to IC_1 drives its output toward the positive or the negative 12V supply rail. Allowing IC_1's output to saturate would introduce sufficient slew-rate delay to cause oscillations. Although specifying a relatively fast operational amplifier, an LF411, improves the amplifier's bandwidth and slew rate, antiparallel diodes D_1 and D_2 improve stability by restricting IC_1's output excursion to one diode forward-voltage drop.

You can adjust R_7 to minimize output dc offset voltage and slew rate. As a rule of thumb, select resistor R_7 to be twice the value of R_9. The ratio of R_9 to R_8 sets the amplifier's gain. **Figure 2** shows the input and output waveforms using optimal values for R_7 and R_9. Note that the V_{CEO} ratings for Q_1 and Q_2 limit V_{CC} and $-V_{CC}$ to 300V or less.□

Figure 1



This complementary-symmetry amplifier features low component count.

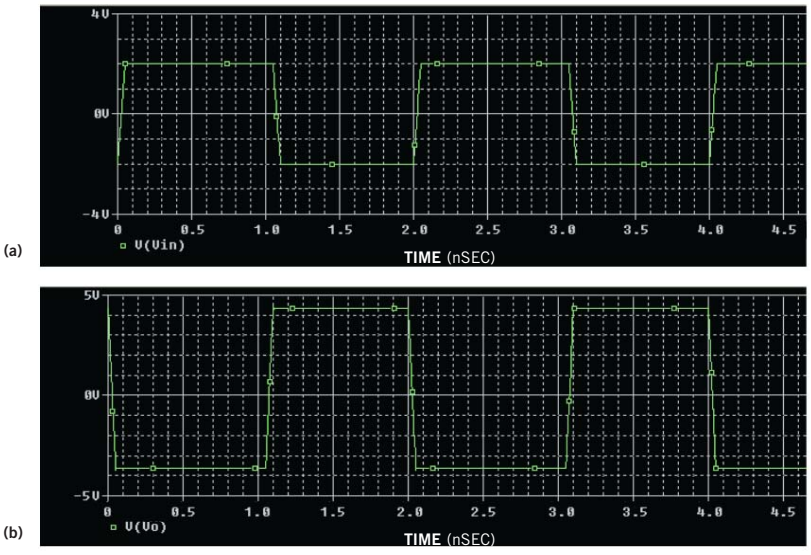


Figure 2 **The input waveform show input voltage applied as a pulse of −2 to +2V (a). The output waveform shows an amplifier gain of 20 and minimized output offset (b).**

Phone wire, RJ-11 jacks and optocouplers build a bus

Ernie Deel, EFD Systems, Marietta, GA

Although cutting-edge technology reaps publicity, the real world often runs on modest hardware that's just "good enough" for home automation, alarm systems, and equipment-monitoring applications. **Figure 1** shows a low-speed, multidrop digital data network that uses inexpensive optoisolators, telephone jacks, and two-pair wiring.

This version of the familiar current loop offers a simplified and somewhat novel implementation in which optocouplers serve triple duty as level converters, isolation/protection devices, and bus interfaces. Galvanic isolation avoids ground loops, increases the effective communications range, and adds a measure of protection for attached hardware.

However, inexpensive optocouplers introduce delays that can cause communications timing errors. Faster optocouplers can minimize errors at the expense of component cost and overall complexity, but using conservatively sized data packets at rates of 4.8 kbps or less allows the use of less expensive components. The H11A-817D optocouplers provide 5-kV isolation and current-transfer ratios of 300 to 600%.

A wall transformer/rectifier provides 12V-dc power for the isolated bus, and devices attached to the bus provide a few milliamperes of 5V power for communicating with isolated-side devices. You can implement RS-232, TTL, or inverted-TTL interfaces by configuring a single jumper and altering connections as appropriate. **Figure 1** illustrates representative examples of each interface.

When adding an RS-232 device, you can ensure compliance with the RS-232 standard by using a control line, such as DTR or RTS, to provide pull-up power, and negative voltage from the TX (transmit) line to passively pull the RX (receive) line low. You can devise a suitable master/slave-communication and error-detection protocol to meet your requirements. Using separate transmitter and

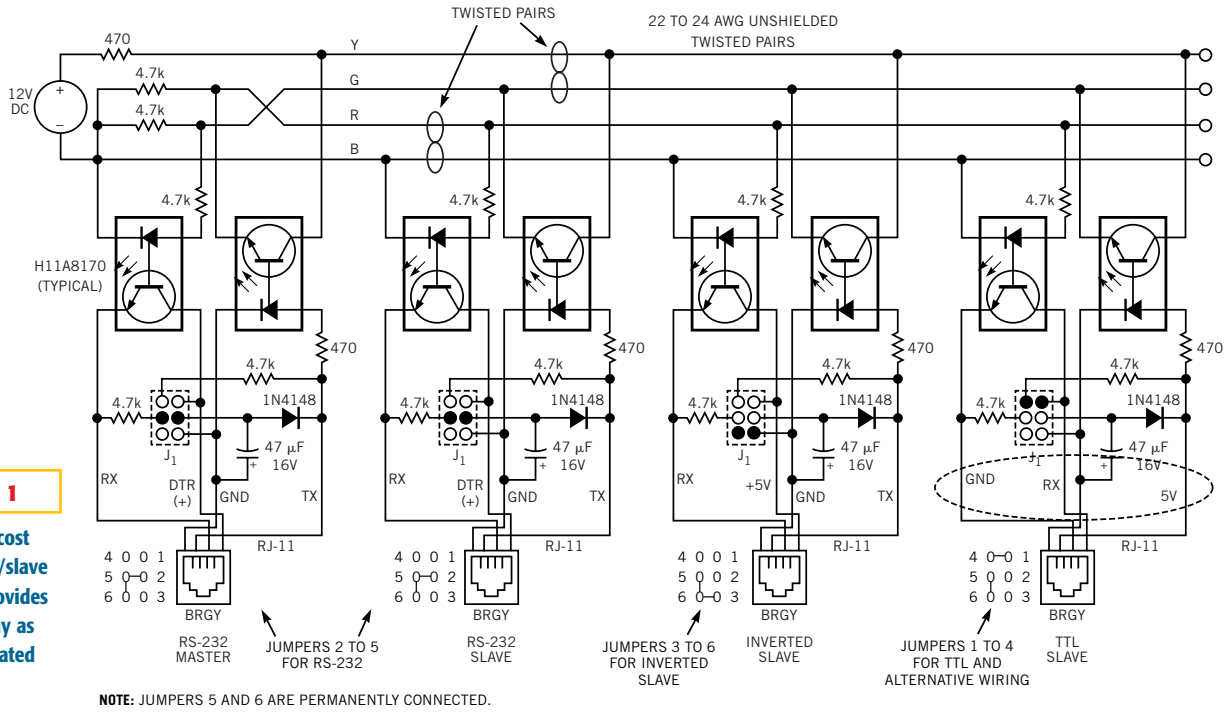


Figure 1

A low-cost master/slave bus provides as many as six isolated nodes.

NOTE: JUMPERS 5 AND 6 ARE PERMANENTLY CONNECTED.

receiver lines helps simplify the required software. The node-point hardware easily fits inside an ordinary surface-mount telephone jack, thus facilitating quick and easy RJ-11 hookups to master and slave devices. At a 4.8-kbps or lower data rate, the bus can extend as far as 500 ft. Inexpensive dual twisted-pair telephone wire forms the bus.□

Use a PC's parallel port to program a clock source

By William Grill, Honeywell BRGA, Lenexa, KS

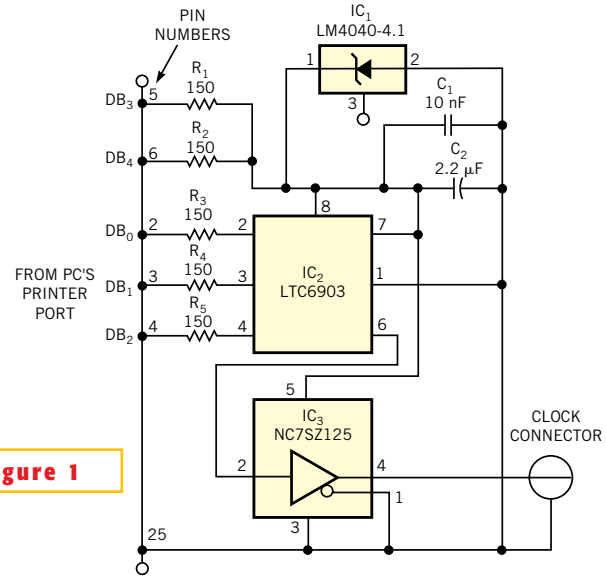


Figure 1

PC-programmable wide-range clock source features minimal component count.

THIS DESIGN IDEA shows how you can use Linear Technology's LTC6903 programmable oscillator as a clock source for direct-digital synthesis, data conversion, switched-capacitor filtering, clock, and voltage-controlled oscillator circuits. The LTC6903 operates from 2.7 to 5.5V with modest power consumption and can produce clock signals at frequencies of 1 kHz to 68 MHz. Typical frequency error and resolution over the range are 1.1 and 0.1%, respectively.

You can control the programmable oscillator circuit in **Figure 1** via an IBM-compatible PC's parallel port, which also provides power to the circuit. Resistors R_1 and R_2 limit power-supply current drawn from parallel-port data bits DB_3 and DB_4, and resistors R_3 through R_5 isolate programming bits DB_0 through DB_2. A precision micropower voltage reference, IC_1, provides 4.096V of stable power to IC_1 and IC_2. For optimal performance, minimize the lead lengths of bypass capacitors C_1 and C_2 with respect to IC_2's power and ground connections. High-speed buffer IC_3 isolates IC_2's output and prevents frequency pulling due to load variations. **Listing 1** on the Web version of this Design Idea at www.edn.com translates a user-supplied input into a 16 bit, SPI-compatible data stream that programs IC_1's output frequency. The LTC6903's output frequency depends on two control coefficients, OCT and DAC. The program derives the closest values for OCT and DAC by solving the equation: $f=(2^{OCT})\times 2078/(2-(DAC)/1024)$. At initial application of power, IC_2's output frequency defaults to 1.039 kHz.□

Constant-on-time buck-boost regulator converts a positive input to a negative output

Robert Bell, National Semiconductor Inc, Chandler, AZ

Buck regulators find wide application as step-down regulators for converting large positive input voltages into a smaller positive output voltages. **Figure 1** shows a simplified buck regulator that operates in continuous-conduction mode—that is, the inductor current always remains positive. The output voltage, V_{OUT}, is equal to $D \times V_{IN}$, where D is the duty-cycle ratio of the buck switch, Q_1, and V_{IN} is the input voltage. The duty cycle, D, is equal to T_{ON}/T_S, where T_{ON} is the on-time of Q_1 and T_S is the switching-frequency period.

You can reconfigure a buck regulator into a buck-boost circuit to convert a positive voltage into a negative voltage (**Figure 2**). The basic component configurations of both circuits are similar, and the inductor and the rectifier diode are transposed. Because the main switch, Q_1, remains in the same location for both configurations, you can use an IC buck regulator for either topology. Switching on Q_1 applies input voltage V_{IN} across power inductor L_1, and current in the inductor ramps up while Q_1 remains on. When Q_1 switches off, inductor current continues to flow through C_1, the load resistance and D_1, producing a negative output voltage. During Q_1's next on-time interval, the output capacitor supplies current to the load.

Figure 3 shows a low-cost buck-boost converter based on the LM5010 buck-regulator IC that converts a 10 to 50V positive supply voltage into −12V. Although many applications use a fixed switching frequency and modulate the output pulse width, this design features a constant-on-time approach in which the IC's internal output transistor turns on for an interval that's inversely proportional to the difference between the circuit's input and output voltage.

Inside IC_1, a regulation comparator monitors the output voltage from voltage divider R_1 and R_2 and a 2.5V internal reference, and, if the output voltage falls below the desired value, the comparator switches on IC_1's output transistor for an interval that an on-timer determines:

$$T_{ON} = K \times \frac{R_{ON}}{V_{IN} + V_{OUT}},$$

where K represents a constant, R_3 sets the buck switch's on-time interval, V_{IN} is the input voltage, and V_{OUT} is the magnitude of the output voltage. Substitute $T_{ON} = 1/F_S$ and then solve for F_S to yield:

$$F_S = \frac{V_{OUT}}{K \times R_{ON}}.$$

Providing that current through L_1 remains continuous, V_{OUT} remains regulated. Because R_3 and K are constants, switching frequency F_S remains constant. This relationship holds true provided that the current through the inductor remains continuous. At lighter loading, the current in the inductor becomes discontinuous—that is, the inductor current drops to zero for a portion of the switching cycle. At the onset of discontinuous operation, the

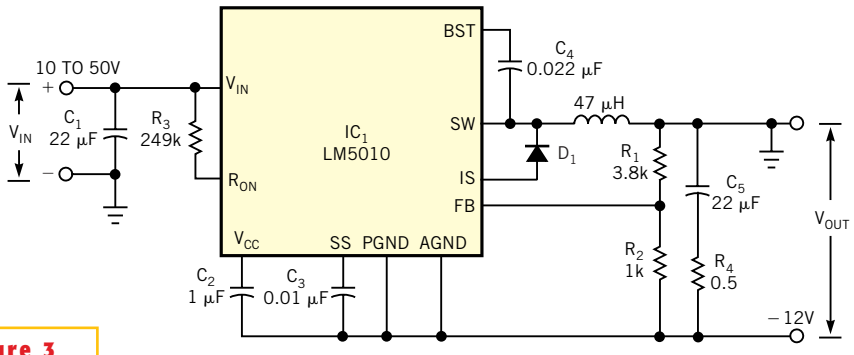


Figure 3 Based on National Semiconductor's LM5010, this buck-boost regulator operates over a wide input-voltage range.

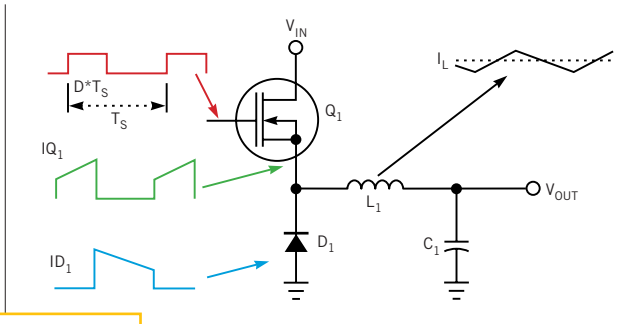


Figure 1 In the basic buck-regulator circuit, current flows continuously through inductor L_1.

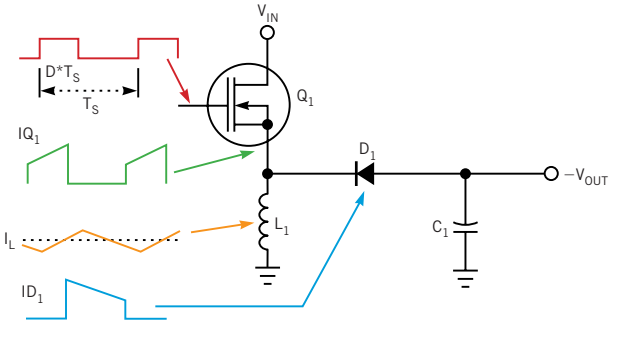


Figure 2 The buck-boost regulator circuit produces a negative output voltage.

switching frequency begins to drop and thus brings V_{OUT} back into regulation.

Operating a buck-boost regulator in fixed-frequency mode without an oscillator eliminates loop compensation and stabilization components and, as a bonus, offers fast transient response unlimited by feedback-network lag time. With the component values in **Figure 3**, the regulator operates at approximately 400 kHz, delivering 12V at approximately 0.5A for 10V input and approximately 1A of output current for 50V input. Resistor R_4 ensures that the minimum amount of output-ripple voltage necessary for regulation—approximately 25 mV—is available.

Fixed-frequency operation without an oscillator offers a low-cost, easily implemented regulator with no loop-compensation or stability issues to worry about. The transient response is fast, because there are no bandwidth-limiting feedback components. The regulator operates at approximately 400 kHz. The output-current capability varies with the input voltage. When you apply 10V input voltage, the output-current capability is approximately 0.5A, and, at 50V input, the output current is approximately 1A.□

Rainbow LED indicates voltage with color

David Prutchi, Impulse Dynamics, Haifa, Israel

Meters that indicate analog levels via a moving-pointer meter, a numeric display, or a column of LEDs typically occupy considerable panel area and require more than a casual glance to read. An indicator lamp or LED takes little space but indicates only an on or off condition. However, an unobtrusive LED that changes color as a function of a measured value would enable an observer to easily assess the measurement.

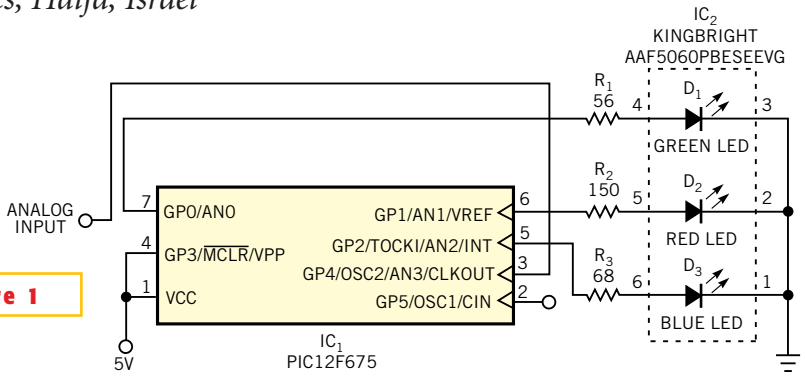


Figure 1

Using a minimal number of components, this voltage-to-color converter uses a single rainbow LED to monitor an analog voltage level.

The circuit in **Figure 1** comprises IC_1, a Microchip PIC12F675 microcontroller driving IC_2, a Kingbright AAF5060PBESEEVG "rainbow" indicator that contains three ultrabright LED chips (red, green, and blue) within one package. Modulating each LED's duty cycle produces all of the perceivable colors of the visible spectrum, including white light. **Listing 1** at the Web version of this Design Idea at www.edn.com contains a PIC program for the PicBasic Pro compiler, which is available from MicroEngineering Labs Inc (www.melabs.com). This program converts a 0 to 5V input applied to Pin 3 of IC_1 to an 8-bit digital value that corresponds to a perceived color containing certain amounts of red, blue, and green.

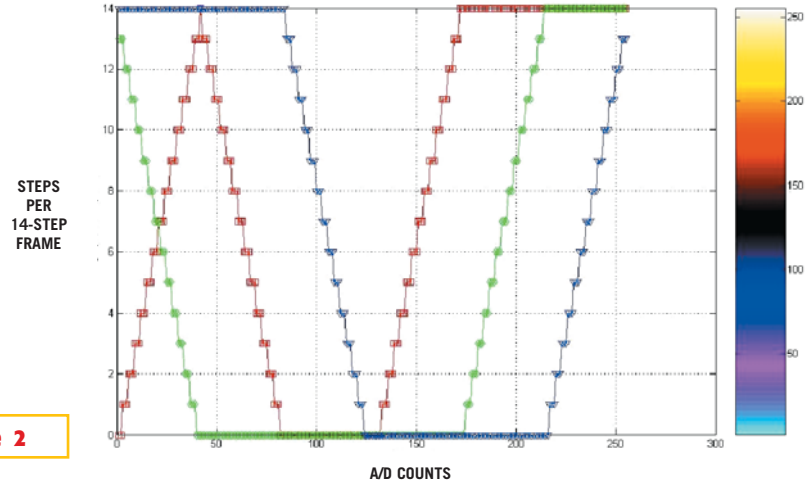


Figure 2

You can alter the color versus input-voltage palette by modifying the firmware.

Under control of a PWM routine, each LED flashes for an interval proportional to its corresponding content of red, green, or blue. During each PWM frame, an LED die receives power for as many as 14 steps per frame as the color map of **Figure 2** shows. (You can view the color map at the Web version of this Design Idea at www.edn.com.) Although not all LEDs are necessarily simultaneously illuminated, the eye's slow response integrates their output to create the illusion of a change in intensity proportional to the duty cycle. The RGB-encoding function in **Listing 1** assumes that the analog input to IC_1 has a zero-signal offset of 2.5V, which switches all LEDs off. "Cool" colors (shades of blue, purple, and aqua) denote an input in the 0 to 2.5V range, and "hot" colors (shades of red, orange, yellow, and white) denote an input in the 2.5 to 5V range. You can create different palettes by changing the primary-color proportions stored in the RGB encoding table.□

Edited by Brad Thompson

Impedance transformer flags failed fuse

Kevin Ackerley, Future Electronics, Vancouver, BC, Canada

FIGURE 1 DEPICTS a circuit that detects the opening of a miniature circuit breaker or high-rupture-capability fuse in a high-reliability telecommunications power supply. The circuit generates an alarm when a failure changes the impedance of an electromagnetic sensor. Traditional fault-detection circuits sense the voltage difference developed across an open fuse, leakage current flowing through a fused circuit, or closure of an auxiliary (volts-free) contact by an actuator fuse. All three methods suffer from disadvantages: Voltage-difference circuits can introduce unacceptable delays as long as 30 minutes because the system's batteries sustain the bus voltage. Leakage-current sensors rely on the presence of a load that may not be present under certain conditions. Adding auxiliary miniature-circuit-breaker support circuits or special high-rupture-capability indicator fuses and their connectors can significantly increase system cost.

Capacitor C_4 and the secondary inductance, L_2, of transformer T_1 resonate at approximately 42 kHz, a frequency that minimizes noise production in the audio, RF, and psophometric noise bands. Operational amplifier IC_1 and associated components form an ac-coupled positive-feedback amplifier with a gain of 20.

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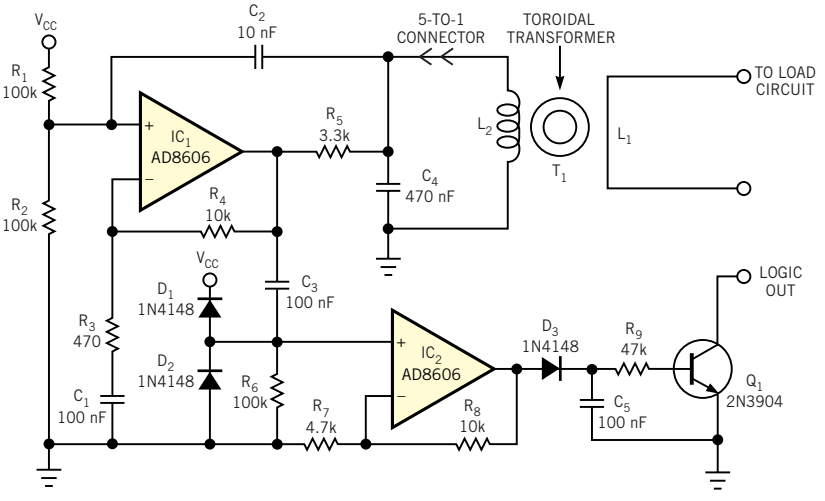


Figure 1 This sensor circuit operates from a single 5V power supply.

Under normal operation, an intact fuse or closed circuit breaker completes a low-impedance path through T_1's single-turn primary (sense) winding. Transformer action presents a low impedance at the junction of C_2, C_4, and R_5 and reduces the loop gain around IC_1 to an amount insufficient to sustain oscillation.

When a fault occurs and interrupts current through T_1's primary winding, its secondary impedance increases, allowing full loop gain and permitting IC_1 to oscillate at 42 kHz, which L_2 and C_4 determine. Under fault conditions, T_1's turns ratio injects less than 10 mV of wideband conducted noise into the dc bus. Capacitor C_3 couples the oscillating signal to IC_2, a gain-of-3 amplifier, which in turn drives a peak detector formed by D_3 and C_5. Transistor Q_1 saturates and provides a logic-low signal to an external alarm. **Figure 2** shows a typical application for sensing backup-battery-circuit failure.

To design transformer T_1, you calcu-

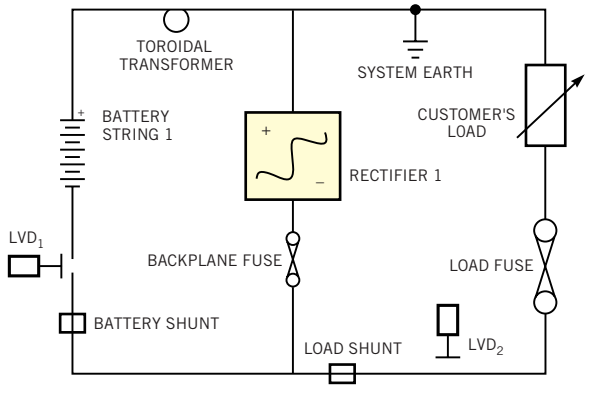


Figure 2 The system wiring diagram shows transformer T_1's primary winding. Low-voltage-disconnect units LVD_1 and LVD_2 isolate the 48V battery or the customer's load for maintenance.

late the required impedance and turns ratio. **Equation 1** describes the basic transformer relationship:

$$\frac{Z_1}{Z_2} \propto \left(\frac{N_1}{N_2}\right)^2, \qquad (1)$$

where Z_1 is the impedance of the primary winding, Z_2 is the impedance of the secondary winding N_1 is the number of primary turns, and N_2 is the number of secondary turns.

Under normal operation with current flowing in the primary winding, the secondary impedance comprises the low primary-side impedance plus T_1's leakage reactance. When no current flows in the primary winding, the number of turns in the secondary and the toroidal core A_L (inductance per turn) determine the secondary winding L_2's inductance and number of turns per **Equation 2**:

$$L_2 = N_2^2 A_L \text{ nH}, \qquad (2)$$

where N_2 is the number of turns around the toroidal core.

Ferrite-core manufacturers publish inductance-per-turn data that simplifies alteration of T_1's design, but if that data is unavailable, you can use **Equation 3** to calculate the inductance.

$$A_L = \frac{\mu_e \mu_o \times 10^6}{\sum(L/A)}, \qquad (3)$$

where μe, the effective permeability, equals the magnetic constant, $4\pi \times 10^{-7} \text{Hm}^{-1}$, I is the path length, and A is the cross-sectional area in millimeters squared.

Select a core that presents a high value of inductance to ensure that the difference between an open and a closed primary circuit causes a large change in relative secondary-winding impedance. Also, select a core material that doesn't saturate at full primary current.

Note that the core's central area must provide clearance for the battery cable (primary winding) and secondary winding. This application uses a Philips 3C85 toroidal ferrite core (part no. TN 16/9.6/6.3-3C85) with a secondary winding comprising five turns of 0.2-mm^2 insulated copper wire. (Philips, however, has discontinued the 3C85 ferrite core. Ferroxcube's type 3C90 ferrite may serve as a replacement. Specifications are available at www.ferroxcube.com.) **Figure 3** shows the completed transformer.□

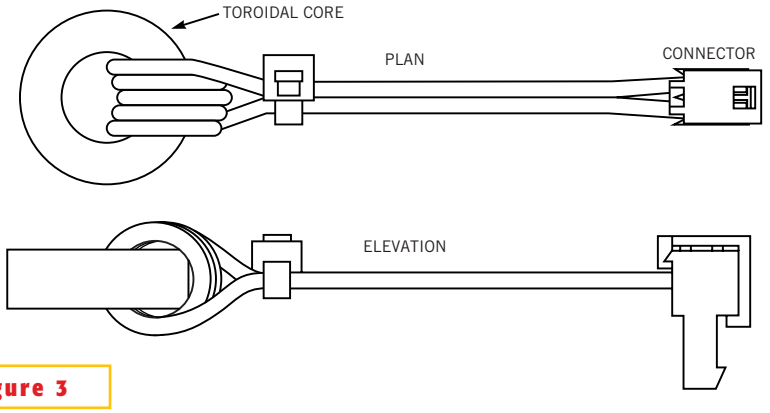


Figure 3

The primary winding (battery cable) passes through transformer T_1's center.

Digital waveform generator provides flexible frequency tuning for sensor measurement

Colm Slattery, Analog Devices, Limerick, Ireland

Variable-resistance sensors convert a fixed dc excitation voltage or current into a current or voltage that's a straightforward function of the quantity undergoing measurement. In another class of sensors, moving objects or fluids produce a sensor signal by altering an LC circuit's inductance or capacitance. **Figure 1** shows a basic ac-driven tuned-circuit proximity sensor, L and C, and sampling resistor, R. Under static conditions, L and C resonate and provide maximum impedance at one frequency. As an object approaches the sensor, the value of L or C varies and alters the circuit's resonant frequency. You can derive the object's position by exciting the sensor with a fixed frequency and measuring changes in the phase or amplitude of output voltage V_2 with respect to excitation voltage V_1. However, this approach limits the sensor's dynamic range and resolution.

As an alternative, you can drive the sensor with a swept-frequency ac source that tracks the sensor's resonant-frequency variation. **Figure 2** shows one approach in which IC_1, a DDS (direct-digital synthesis) device, produces a sine-wave excitation voltage. Lowpass filter IC_2 removes clock artifacts and harmonics, and amplifier IC_3 drives the sensor. Amplifi-

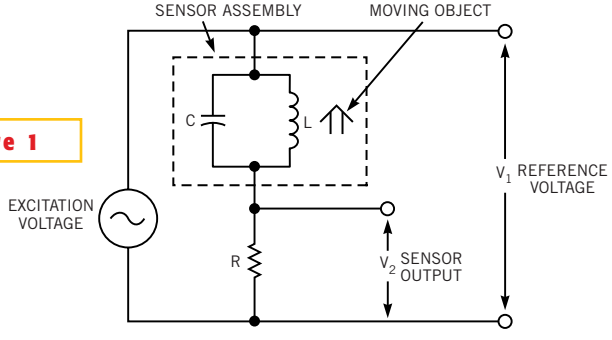


Figure 1

The amplitude and phase of the resonant-circuit sensor's output voltage, V_2, vary with moving object's position.

er IC_4 boosts the sensor's output voltage, V_2, and drives IC_5, a dual-channel, 12-bit ADC, which simultaneously samples and digitizes reference voltage V_1 and IC_4's output. IC_5, a DSP-capable microcontroller, analyzes the sensor output's amplitude and phase, setting the frequency of IC_1 via alternate programming of either of IC_1's dual frequency-control registers. One of IC_6's serial ports delivers position data to an external controller. Using a DDS/DSP combination offers considerable flexibility when using various types of sensors. For example, certain sensors require a relatively narrow but high-resolution range of excitation frequencies, and others may work best with broadly swept excitation.□

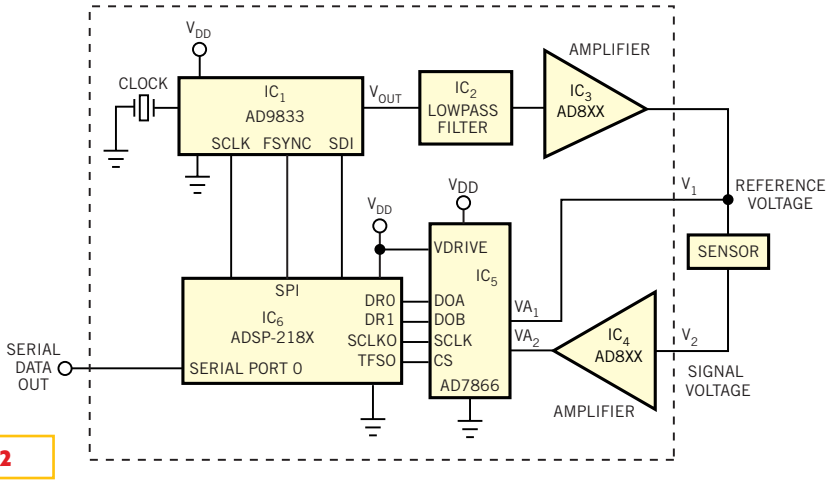


Figure 2

A swept-frequency source and a DSP controller combine to offer a versatile sensor-excitation system.

Battery-operated remote-temperature sensor drives 4- to 20-mA current loop

Scot Lester, Texas Instruments, Dallas, TX

You can remotely measure temperature using a 4- to 20-mA current loop as long as 4000 feet and a battery-powered, white-light LED driver. You usually configure this equipment to provide a programmable, constant current to an LED from a battery source. The TPS62300 series of ICs, for example, converts a battery voltage of 2.7 to 6.5V into a constant current, which you program using an external resistor and voltage on its I_{SET} pin. The current that normally drives the LED instead powers the loop (**Figure 1**).

In the sample circuit, which occupies 50 mm^2, the LED driver drives the 4- to 20-mA current loop proportionate to a sensed temperature of −10°C at 4 mA and 50°C at 20 mA. The driver applies 0.6V to the I_{SET} pin and monitors current flow from the pin. This current is multi-

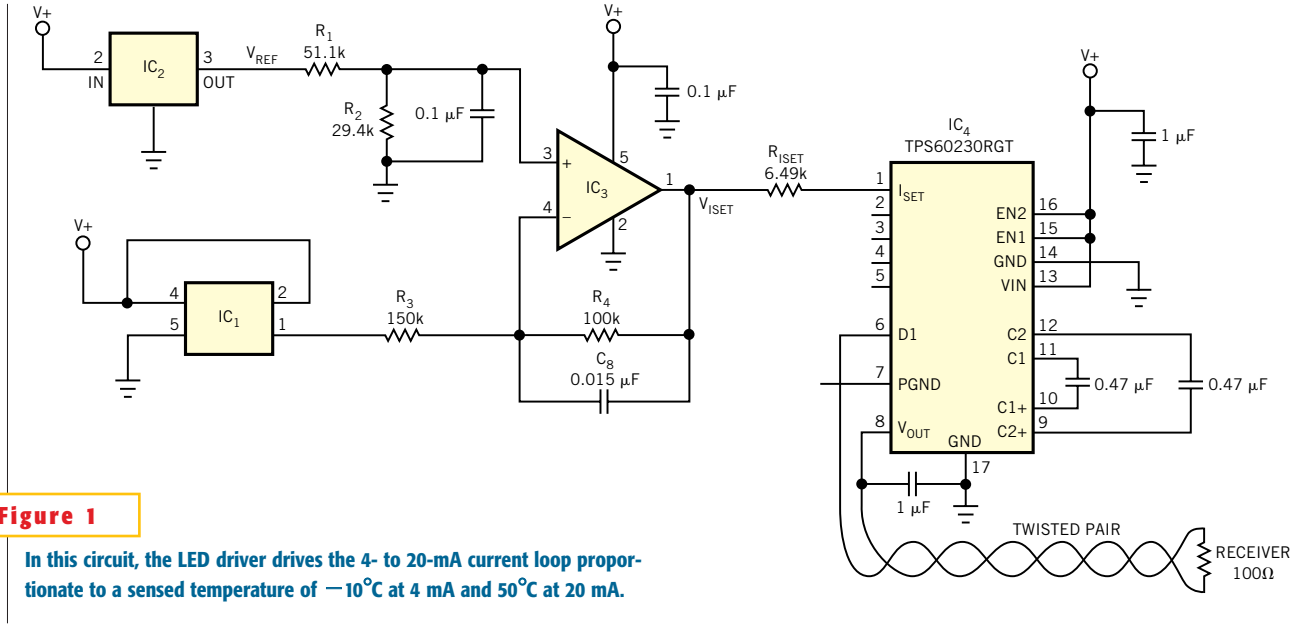


Figure 1

In this circuit, the LED driver drives the 4- to 20-mA current loop proportionate to a sensed temperature of −10°C at 4 mA and 50°C at 20 mA.

plied by 260 and mirrored to the LED drive output:

$$I_{LOOP} = 260 \times \left(\frac{0.6 - V_{ISET}}{R_{ISET}} \right).$$

Because resistor R_{ISET}, which is tied to the I_{SET} pin, is fixed in the example, the output current is proportional to the voltage, V_{ISET}, which the output of op amp IC_3 determines. Using a 6.49-kΩ resistor for R_{ISET} means that V_{ISET} needs to be 0.1V to provide 20 mA of loop current and 0.5V to provide 4 mA.

The TMP36 temperature sensor, IC_1, provides 750 mV of output at 25°C and varies its output voltage by 10 mV/°C. The output of the TMP36 is 0.4V at −10°C and 1V at 50°C. Because these voltages do not directly match the voltage requirements of V_{ISET}, you use a REF2912 voltage reference, IC_2, with the OPA374 op amp to scale the output of the TMP36 to the required voltage for the LED driver, IC_4. In general terms, the current in the current loop for the circuit is:

$$I_{LOOP} = \left(\frac{260}{R_{ISET}} \right) \times \left(0.6 - V_{REF} \times \left(\frac{R_2}{R_1 + R_2} \right) \times \left(\left(1 + \frac{R_4}{R_3} \right) + V_{TEMP} \times \left(\frac{R_4}{R_3} \right) \right) \right).$$

Substituting for the component values shown in the **figure** yields:

$$I_{LOOP} = 0.0267 \times V_{TEMP} - 0.00644.$$

The output of the LED driver can drive loops with as much as 180Ω of resistance with battery voltages as low as 2.7V. Therefore, the LED driver can drive more than 1500 feet of 24 AWG or 4000 feet of 20 AWG twisted-pair wire with a 100Ω load resistor at the receiver. You can achieve much longer distances with higher battery voltages. Because this circuit powers the current loop, the battery life for these circuits depends on the measured temperature. For the circuit shown, a loop current of 13.3 mA corresponds to a measured temperature of 25°C. Therefore, using two AA alkaline batteries in series should provide more than 120 hours of remote-temperature monitoring at room temperature. The accuracy for the circuit is about 2.5% of full scale without any calibration. For tighter accuracy, reduce the range of the measured temperature or calibrate the output.□

Precision current source is software-programmable

Joe Neubauer, Maxim Integrated Products Inc, Sunnyvale, CA

With the addition of a few inexpensive miniature components, the hard-wired, voltage-controlled current source of yesterday becomes a software-programmable voltage-controlled current source (**Figure 1**). A digital potentiometer, IC_1 in conjunction with a precision op amp, IC_2, sets current through a pass transistor, I_{SET}, and a shunt regulator, IC_3, provides a constant reference voltage across the digital potentiometer. By operating in its linear region, the transistor controls load current in response to the applied gate voltage. Each incremental step of the digital potentiometer increases or decreases the wiper voltage, V_{IN+}, at the op amp's noninverting input. Thus, V_{IN+} varies with respect to the reference voltage, which in turn remains stable with respect to the supply rail:

$$V_{IN+} = \frac{V_{REF}\left[R_{TOTAL(DP)}/(\text{TOTAL NO. OF STEPS})\right]}{R_{TOTAL(DP)}}.$$

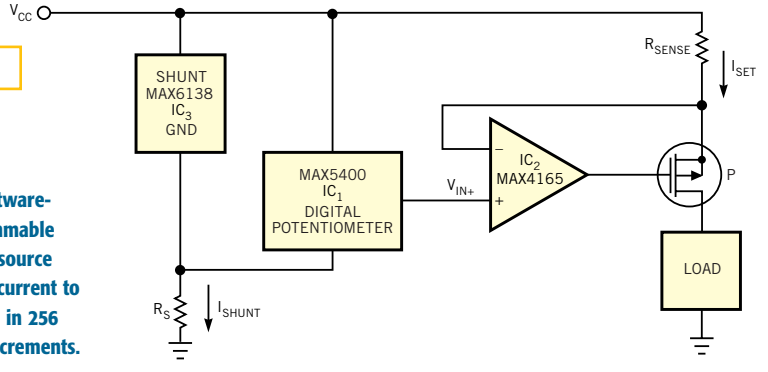
Many types of digital potentiometer are currently available, and the interface to these devices, besides the hard-wired type, can be one, two, or three wires. IC_1, for example, has a three-wire SPI interface, and provides an end-to-end resistance of 50 kΩ with 256 incremental settings. Thus, each increment of the digital potentiometer changes V_{IN+} by:

$$V_{IN+} = \frac{3V(50\,k\Omega/256)}{50\,k\Omega} = 11.72\ mV.$$

Op amp IC_2 regulates current through the pass transistor, and the digital potentiometer sets current through the R_{SENSE} resistor. The voltage across R_{SENSE} determines current through the pass transistor, I_{SET}: $I_{SET} = (V_{CC} - V_{IN+})/R_{SENSE}$.

The circuit can provide any current level for which the external components, R_{SENSE} and the pass transistor, can handle the associated power dissipation (P=IV). Because the ratio setting of digital potentiometers is good, with a typical ratiometric resistor temperature coefficient of 5 ppm/°C), precision and stability for the current source depend primarily on the precision and stability of IC_3 and R_{SENSE} combined.□

Figure 1



This software-programmable current source applies current to the load in 256 equal increments.