Design Ideas from EDN

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Two gates and a microprocessor form digital PLL
Camera serializer/deserializer chip set reduces wire count for keypad
Rearranged reference helps ADC measure its own supply voltage
Difference amplifier measures high voltages
Linear potentiometer provides nonlinear light-intensity control

May 2005 pag. 52
Versatile digital speedometer uses few components
Microprocessor, linear potentiometer deliver echo pulses
Passive-detector receiver keeps you informed, entertained during flights
Quickly estimate an electronic system's cooling requirements
Spreadsheet converts sound levels
Interrupt-driven keyboard for MCS-51 uses few components
Simplified white-LED flasher operates from one cell
Low power voltage-to-frequency converter makes a wireless probe for testing an inductive power supply
Simple circuit converts 5V to –10V

June 2005 pag. 62
Inrush limiter also provides short-circuit protection
Microprocessor-based dual timer features four outputs
Wide-range voltage regulator automatically selects operating mode
CMOS hex inverter generates low-distortion sine waves
Digital countdown timer may never need battery replacement
Wide-range regulator delivers 12V, 3A output from 16 to 100V source
Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output
Ultra-low-noise low-dropout regulator achieves 6-nV/vHz noise floor

July 2005 pag. 72
Contact-debouncing algorithm emulates Schmitt trigger
Inexpensive peak detector requires few components
Free program designs and analyzes passive and active filters
Power-supply interrupter fights ESD-induced device latch-up
High-impedance FET probe extends RF-spectrum analyzer's usable range
Watchdog circuit protects against loss of battery charger's control signals
Circuit adds foldback-current protection

August 2005 pag. 83
AGC amplifier features 60-dB dynamic range
Precision active load operates as low as 2V
Squeeze extra outputs from a pin-limited microcontroller
Build a precise dc floating-current source

Frequency dithering enhances high-performance ADCs
Memory-termination IC balances charges on series capacitors
Voltage reference is software-programmable

September 2005 pag. 94
Precision full-wave signal rectifier needs no diodes
1-Hz to 100-MHz VFC features 160-dB dynamic range
Cascode MOSFET increases boost regulator's input- and output-voltage ranges
Buffer amplifier and LED improve PWM power controller's low-load operation
Temperature controller has "take-back-half" convergence algorithm
MOSFET enhances low-current measurements using moving-coil meter
Shunt regulator serves as inexpensive op amp in power supplies
Keyboard links to microcomputer through one-wire interface
Added components improve switching-regulator stability
Electromechanical damping stabilizes analog-meter readings

October 2005 pag. 109
Dither a power converter's operating frequency to reduce peak emissions
Single-port pin drives dual LED
Network linearizes dc/dc converter's current-limit characteristics
Add a Schmitt-trigger function to CPLDs, FPGAs, and applications
LC oscillator has stable amplitude
Use a system's real-time clock to "hide" a code sequence
Shunt regulator eases power-supply-start-up woes

November 2005 pag. 119
Temperature-to-period circuit provides linearization of thermistor response
Two wires control SPI high-speed ADC
Volume-unit meter spans 60-dB dynamic range
Pacer clock saves subroutine calls
Stereo-amplifier IC's outputs drive multiple loads
Muscle power drives battery-free electronics
FET biasing targets battery-powered PWM applications

December 2005 pag. 129
Low-cost BER tester measures errors in low-data-rate applications
DMA eases CPU's workload for waveform generation
Bipolar current source maintains high output impedance at high frequencies
Shunt regulator speeds power supply's start-up
Build a USB-based GPIB controller
Programs calculate 1% and ratio-resistor pairs
Simplify worst-case PSpice simulations with customized measurement expressions
Tiny twisted-pair transmission line solves test-fixture woes

Edited by Brad Thompson

Laser simulator helps avoid destroyed diodes

Nick Cornford, Berkhamsted, Hertfordshire, UK

LASER DIODES CAN destroy themselves in a few nanoseconds, so testing the response and stability of a feedback-stabilized laser-diode driver can be expensive. The simulator circuit in **Figure 1** shows a typical laser-diode package, which contains not only the diode, which is driven by current I_L, but also a photodiode. The laser diode's front facet emits a main beam that goes to work in the outside world, and the rear facet emits a reference beam that falls on the photodiode.

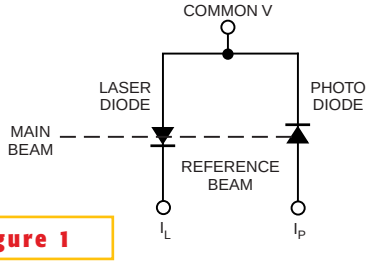

Figure 1 A P-type-laser diode assembly includes the photodiode power sensor.

Although much weaker than the main beam, the reference beam's power is directly proportional to the main beam, as is the current, I_p, that produces the photodiode. Connecting the photodiode back to the laser-diode driver via a carefully designed amplifier completes a feedback loop that should hold the main beam power stable and constant. Ensuring that the laser diode never sustains a destructive overload under any conditions is the tricky part.

A laser diode exhibits a current threshold, or "knee," below which its emission is weak and incoherent, as is photocurrent I_p. Above the knee, laser action occurs, and the optical output and photocurrent rise linearly with increasing drive current.

A simulator must reflect these characteristics, and the circuit in **Figure 2** comprises a basic voltage-controlled current source that presents a threshold. Based on a TO-92 or E-line-packaged PNP transistor and two resistors and packaged in a blob of epoxy, the simulator takes the place of the laser diode until circuit operation is stable. It's easy to build several modules to emulate laser diodes of various ratings.

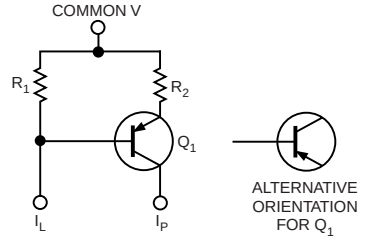

Figure 2 A laser-diode simulator requires only one transistor.

In operation, the laser driver sinks current I_L and develops a voltage, V_S, across R_1. When V_S exceeds Q_1's V_{BE}, Q_1 conducts and sources a simulated photocurrent, I_p, into the feedback-control circuitry. As I_L increases, I_p increases linearly in proportion.

As a design example, consider an average laser diode with a threshold current (I_{TH}) of 10 mA, an operating current at full optical output (I_{LMAX}) of 30 mA, and a photocurrent of 100 µA at full power. R_1 must then equal V_{BE}/I_{TH}, or 560 mV/10 mA and thus yields a value of 56Ω for R_1. Then, R_2 equals $((I_{LMAX} \cdot R_1) - V_{BE})/I_{PMAX}$, or approximately 11 kΩ. Using a value of 560 mV for V_{BE} produces the best practical relationship between I_L and I_P.

Inverting the transistor—that is, swapping Q_1's collector and emitter connections— produces a more abrupt conduction-threshold voltage of approximately 500 mV but decreases the slope of I_P versus I_L. In this example, inverting the transistor requires lowering the value of R_2 to approximately 7.5 kΩ.

The inverted-transistor circuit provides a sharper threshold and thus more realistic simulation, even though it may require some experimentation with resistor values for optimal performance. You can use almost any PNP bipolar-junction transistor for Q_1, such as a ZTX502, and decreasing R_2 by 30% renders I_P within 5% of the desired nominal value of I_P.

Note that laser diodes' characteristics vary widely, even within a batch, so using preferred-value resistors for R_1 and R_2 makes little practical difference in performance. Laser diodes exhibit a typical forward-voltage drop of about 2V, and the simulator circuit should thus drop no more voltage at full current. Also, the simulator circuit responds more slowly than a laser diode, but, if the feedback circuitry operates even more slowly, as it usually does, the simulator's slow response presents no problem.

A simulator for an N-type laser diode requires an NPN transistor and reversal of connections. More complex laser diodes may require more elaborate circuitry that includes current mirrors and additional connections. If adequate power-supply voltage is available for current-source compliance, you can connect an LED in series with the I_L lead to provide a visual indication of circuit operation. Connecting an oscilloscope across R_1 allows monitoring laser-drive and modulation currents. (In this context, "N-" and "P-type" refer not to laser-diode-device diffusions but to the polarity of the common terminal.)□

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Differential driver doubles as versatile RF-switch driver

John Ardizzoni, Analog Devices, Wilmington, MA

Designed as a high-speed driver for 12-bit ADCs, the AD8137 controls SPDT GaAs (gallium-arsenide) FET-MMIC (microwave-monolithic-IC) and PIN-diode RF switches and thus provides a low-cost and versatile alternative to conventional switch drivers. This circuit achieves typical switching speeds of approximately 7 to 11 nsec, including the propagation delays of the driver and RF load.

The GaAsFET-driver circuit (**Figure 1**) converts a single-ended, 0 to 3.5V TTL signal into a complementary, 0 to −4V differential-output signal. The divider formed by the 50Ω source impedance, R_S, and the input termination, R_T, imposes a 50% signal reduction. To compensate, the circuit amplifies its input by approximately 2.3 times to yield the proper output amplitude of 4V p-p. The circuit also shifts the output level by −2V to provide the proper GaAsFET bias. **Equation 1** determines the output voltage:

$$G = \frac{R_5}{R_1} = \frac{R_6}{R_4}. \quad (1)$$

For a symmetrical output swing, gain-setting resistors R_1 and R_4 must present the same Thevenin-equivalent resistance. In **Figure 1**, R_4 increases by 20Ω over R_1. This increase compensates for the fact that source resistor R_S and termination resistor R_T combine in parallel to introduce additional resistance of 25Ω. Setting R_4 to 1.02 kΩ (the closest standard value to 1.025 kΩ) ensures that the circuit will provide approximately equal gains at the differential outputs.

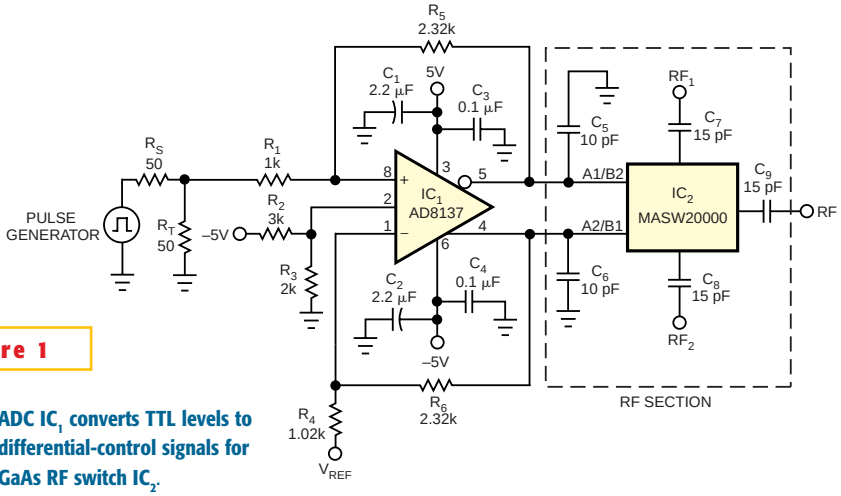

Figure 1 ADC IC_1 converts TTL levels to differential-control signals for GaAs RF switch IC_2.

The AD8137's V_{OCM} input (Pin 2) offers a convenient method of shifting the outputs' dc common-mode level. In **Figure 1**, R_2 and R_3 form a voltage divider, which sets the dc output level to −2V. Connecting the AD8137's inverting input to a reference voltage of 1.75V establishes the midpoint of the input signal and allows for proper switching of the AD8137's input stage.

Figure 2 shows the GaAs FET driver's turn-on switching speed of approximately 5 nsec for isolation to insertion loss—that is, 50% of the TTL input to 90% detected RF. **Figure 3** shows turn-off switching speed of approximately 11 nsec for insertion loss to isolation—that is, 50% of the TTL input to 10% detected RF.

As **Figure 4** shows, with only minor modifications, the GaAs switch-driver circuit can drive PIN-diode loads that require both positive and negative bias currents. IC_1's V_{OCM} input connects to ground to provide symmetrical outputs of 63.5V about ground and sinks and sources 10 mA of bias current. Altering

Figure 2 Vertical cursors denote GaAs switch turn-on time of approximately 5 nsec.

Figure 3 Turn-off time is approximately 11 nsec.

feedback resistors R_3 and R_4 to 2 kV provides an output swing of 63.5V. Resistors R_5 and R_6 set the steady-state PIN-diode current, I_{SS}, as **Equation 2** shows:

$$I = \frac{V_0 - V_D}{R_5}. \quad (2)$$

Capacitors C_5 and C_6 set the spiking current I_S, which removes stored charge in the PIN diodes. You can optimize a given diode switch's response time by using the AD8137's output slew rate for dV/dt and **Equation 3**,

$$i = -C_5 \frac{dV}{dt}, \quad (3)$$

to calculate spiking current.□

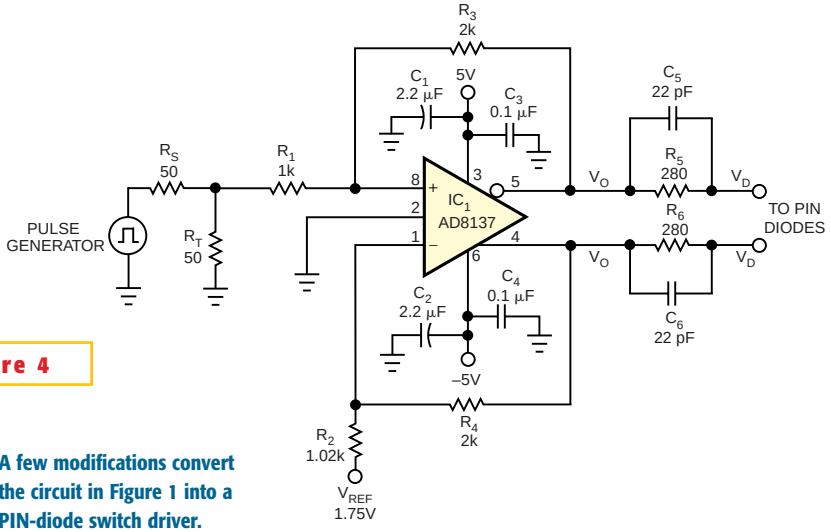

Figure 4

A few modifications convert the circuit in Figure 1 into a PIN-diode switch driver.

Pseudologarithmic thermistor signal conditioning spans wide temperature range

Stephen Woodward, University of North Carolina, Chapel Hill, NC

Given its low cost, small size, robust construction, accuracy, versatility and sensitivity, it's no wonder that the thermistor rates as one of the most popular temperature sensors available. However, in some applications, a thermistor can exhibit too much sensitivity for wide-range temperature measurements. For example, when you combine a thermistor's radically nonlinear exponential resistance-versus-temperature-response curve with a linear signal conditioner (**Reference 1**), the resultant graph resembles a difficult-to-characterize response, as Trace A shows (**Figure 1**).

Note that most of the thermistor's resistance range crowds into a small span of temperatures at the lower limit of the range. As Curve B in **Figure 1** shows, the change of resistance per degree of temperature change looks exaggerated at low temperatures. As temperature increases, the resolution diminishes and may become inadequate at the upper end of the temperature scale.

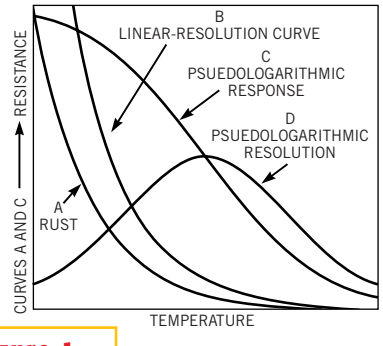

Figure 1

These resistance-versus-temperature curves highlight the improved resolution available in a pseudologarithmic circuit.

In contrast, the signal-conditioning circuit in **Figure 2** mitigates the thermistor's inherent nonlinearity by generating a compensating, pseudologarithmic response function that's Curve C in **Figure 1** represents. The following **equation** relates the circuit's ±10V output span for an ADC ±10V input span to thermistor resistance: Thermistor resistance=$R_4 \times (V_O + 10)/(102V_O)$.

Curve D in **Figure 1** shows the resultant resolution curve. Maximum resolution occurs at a temperature that corresponds to a thermistor resistance equal to R_4 and an output voltage of 0V. Although selection of this value optimizes resolution in the middle of the measurement range, the thermistor's nominal resistance is relatively noncritical. You can also select a different value of reference voltage, V_{REF}, to shift the ±10V output span to meet other requirements. For best performance, you can share the same reference source for V_{REF} and for the measurement system's ADC, which makes measurements ratiometric and thus insensitive to reference-voltage drift.

In addition to resolution, span, and

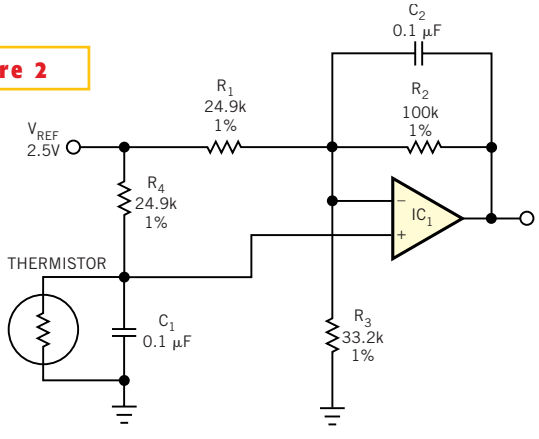

Figure 2

This pseudologarithmic thermistor signal conditioner uses a single operational amplifier and a few passive components.

reference-drift considerations, thermistors—and, for that matter, all temperature sensors—experience self-heating effects. The excitation current produces ohmic power that causes these effects. The limited thermal mass of miniature thermistors provides limited heat dissipation—often only a few microwatts per degree—and that dissipation can produce especially severe temperature shifts.

In the circuit in **Figure 2**, the power dissipated due to thermistor's self-heating reaches a maximum at midspan—that is, when output voltage is 0V and equals: $V_{REF}^2/(4\times R_4)=63\ \mu W$ for the component values illustrated. For all but the smallest thermistors, this level of self-heating produces acceptably low fractional-degree errors.□

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1. Woodward, Steve, "Optimize linear-sensor resolution," *EDN*, March 7, 2002, pg 131.

RF-telemetry transmitter features minimal parts count

Francis Rodes, Eliane Garnier, and Olivier Chevalerias, ENSEIRB Talence, France

REQUIREMENTS FOR portable, short-range telemetry systems frequently include low power consumption, small size, and low cost. The circuit in **Figure 1** meets these criteria and uses only three off-the-shelf ICs and a few passive components. Although dedicated to conditioning the low-level signal a strain-gauge bridge produces, the circuit can operate with almost any resistive transducer based on a Wheatstone bridge. The circuit comprises a VFC (voltage-to-frequency converter) that produces a PPM (pulse-position-modulation) output, and an OOK (on/off-keyed) RF transmitter. Based on direct digitization, the VFC in **Figure 1** comprises IC_1, IC_2, IC_{3A}, and IC_{3B}. A Wheatstone bridge containing strain gauge R_X produces an output of approximately 5 mV. An integrator stage comprising C_6 and IC_1, a Linear Technology LTC1250 offset-compensated, low-drift operational amplifier, connects directly across the bridge. (Note that the value of the remaining resistors in the bridge depends on the application.)

To yield a ratiometric conversion, the voltage applied to the bridge, V_{COMP}, varies with power-supply voltage and equals the difference between the two threshold voltages of a Schmitt-trigger circuit. In **Figure 1**, the Schmitt trigger comprises a Maxim MAX9075 comparator, IC_2; a CMOS inverter, IC_{3A}; and the positive feedback network comprising R_1, R_2, and C_1. **Equations 1** and **2** define the Schmitt trigger's high, V_{TH}, and low, V_{TL}, threshold voltages:

$$V_{TH} = V_{DD}\frac{R_1}{R_1+R_2}. \quad (1)$$

$$V_{TL} = V_{DD}\frac{R_2}{R_1+R_2}. \quad (2)$$

To understand the circuit's operation, assume that the comparator's output is high and, consequently, the inverter's output is low. Also assume that the series combination of the strain gauge, R_X, and the trimmer, R_T, is always equivalent to $R(1+X)>R$. That is, for linear operation, the sensor's resistance variation represents a small fraction of the arm resistance.

Under these conditions, the noninverting input of IC_1 biases to $V_{DD}/2$, and the Wheatstone bridge's active arm drives a positive current, I_I, into the summing node of IC_1. This current causes the integrator's output, V_{OI} ,to ramp down toward the low threshold voltage, V_{TL}, of the Schmitt trigger.

When $V_{OI}=V_{TL}$, the comparator's output goes to zero, and the inverter's output consequently rises to V_{DD} . This action inverts the direction of the integrator's input current, causing the in-

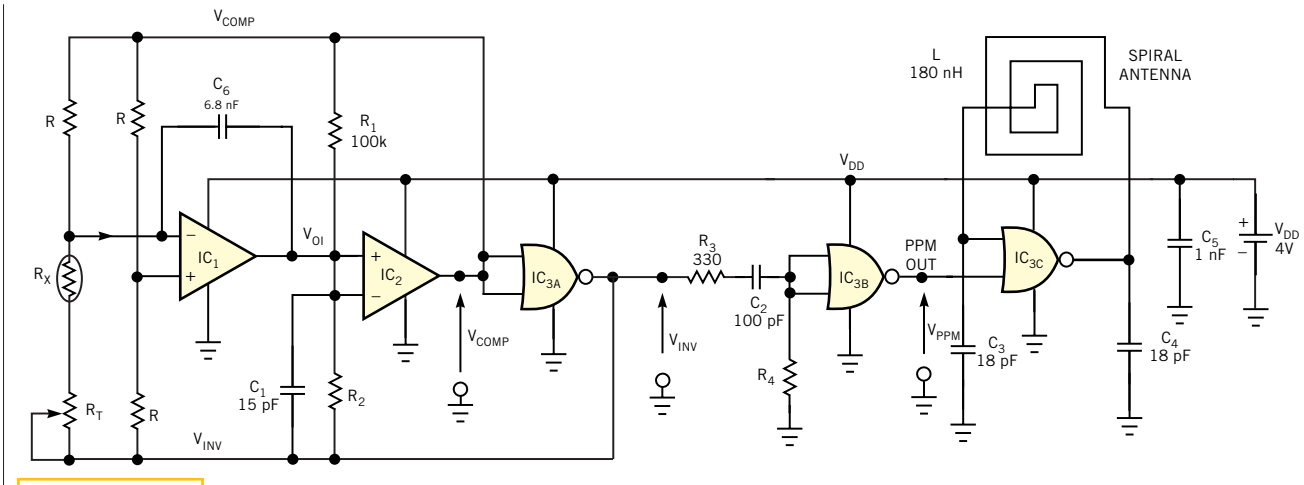

Figure 1 Thise RF-telemetry transmitter and strain-gauge amplifier use only three ICs.

tegrator's output to ramp upward to the Schmitt trigger's high threshold voltage. Finally, when $V_{OI} = V_{TH}$, the comparator's output goes high, and the above sequence repeats indefinitely, producing a free-running oscillation in which the integrator's output ramps up and down between the threshold voltages of the Schmitt trigger (Trace 1 in **Figure 2**). Meanwhile, the comparator's output and the inverter's output deliver two square waves with a 50%-duty-cycle ratio (traces 2 and 3, respectively, in **Figure 2**) that drive the bridge.

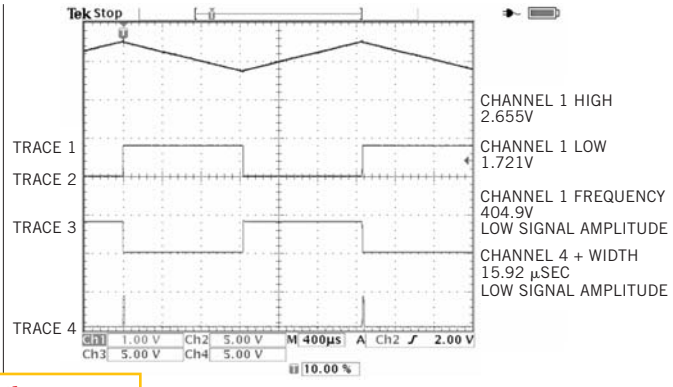

Figure 2 This oscilloscope photo shows circuit's internal waveforms: Trace 1 is the integrator's output voltage, Trace 2 is the comparator's output voltage, Trace 3 is the inverter's output voltage, and Trace 4 is the PPM-output voltage.

To produce the PPM signal (Trace 4 in **Figure 2**), the inverter's output drives a monostable circuit comprising a second inverter, IC_{3B}, and timing components R_4 and C_2, which produces a 15-µsec-wide pulse. Current-limiting resistor R_3 prevents latch-up of IC_3, and R_2 and C_4 set the output-pulse width.

To model the VFC's transfer function, calculate period T_X of the comparator's output. Due to the symmetry of IC_1's output, this period is twice the time the integrator's output takes to ramp linearly between the two threshold voltages of the Schmitt trigger. Consequently, you can express t_X as in **Equation 3**:

$$t_X = 2\frac{V_{TH} - V_{TL}}{\frac{dV_{OI}}{dt}}, \quad (3)$$

where dV_{OI}/dt is the slope of the ramp at the integrator's output. Assuming that the integrator's input current is constant during one period, **Equation 4** gives the slope:

$$\frac{dV_{OI}}{dt} = \frac{I_I}{C}. \quad (4)$$

After applying a Thevenin transformation of the bridge's active arm, you can express the integrator's input current as

$$I_I = \frac{V_{DD}}{2R} \times \frac{X}{1+X}. \quad (5)$$

Replacing V_{TL}, V_{TH}, and dV_{OI}/dt in **Equation 3** with the respective expressions from **equations 1**, **2**, and **4** finally yields the frequency in **Equation 6**.

$$f_X = \frac{1}{t_X} = \frac{1}{4RC} \times \frac{R_1 + R_2}{R_1 - R_2} \times \frac{X}{1+X}. \quad (6)$$

Knowing that $X << 1$, you can approximate the PPM's output frequency by **Equation 7**:

$$f_X \approx \frac{1}{4RC} \times \frac{R_1 + R_2}{R_1 - R_2} \times X. \quad (7)$$

This transfer function highlights the VFC's three most important features: that the modulation frequency, f_X, is directly proportional to the relative variation of the bridge's sensor resistance, R_X; that the modulation frequency is independent of the power-supply, V_{DD}; and, therefore, that this PPM converter is ratiometric. This feature is attractive for any portable-system application in which the supply voltage decreases as the battery ages. The modulation frequency is independent of the PPM pulse width, which eliminates the source of error you typically encounter with single-slope VFCs.

Using the components values shown in **Figure 1**, the converter's frequency span is: $200\ Hz < F_X < 600\ Hz$ for a relative variation of the strain-gauge resistance: $-4.2 \times 10^{-3} < \Delta R/R < 4.2 \times 10^{-3}$. Consequently, with zero force applied to the strain gauge, $\Delta R/R = 0$, and the converter produces a 400-Hz modulation frequency. The waveforms in **Figure 2** correspond to this case.

To transmit data over a distance of a few meters, the PPM signal modulates an 80-MHz OOK RF transmitter. This transmitter comprises an interruptible Colpitts oscillator based on a very-high-speed CMOS NOR gate, IC_{3C}; a 74VHC-02; and a tank circuit comprising two identical feedback capacitors, C_3 and C_4; and a square-spiral pc inductor, L. To obtain reliable oscillation start-up, set $C_3 = C_4 = C$. Neglecting the effects of stray capacitances, you can calculate the output frequency of the Colpitts oscillator via **Equation 8**:

$$f_C = \frac{1}{2\pi\sqrt{L\frac{C}{2}}}. \quad (8)$$

The values of L, C_3, and C_4 shown in **Figure 1** produce a carrier frequency, f_C, of approximately 80 MHz. Inductor L_1 also doubles as the transmitter's antenna, and its characteristics of eight turns in an 8×8-mm pc-board footprint stem from a process that ensures that the transmitter's radiated power never exceeds 250 nW at 80 MHz.

According to European Telecommunication Standard I-ETS 300 220, the transmitter requires no license and can operate at any carrier frequency within the 74- to 87.5-MHz band. Consult applicable regulations for unlicensed transmitter operation in your locality.

At a transmitted power of less than 250 nW, an AM receiver with a tangential sensitivity of 1 µV provides a reception range as long as 10m, which is sufficient for many indoor-telemetry applications. At a maximum PPM frequency of 600 Hz, the current drain of the circuit in **Figure 1** is approximately 2 mA at a supply voltage of 4V.□

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1. Williams, Jim, "Circuits allow direct digitization of low- level transducer outputs," *EDN*, Nov 29, 1984, pg 183.

2. Williams, Jim, "Digitize transducer outputs directly at the source," *EDN*, Jan 10, 1985, pg 201.

design ideas

Edited by Brad Thompson

Enhanced battery "gas gauge" keeps its data through glitches

Herbert Seidenberg, Costa Mesa, CA

Texas Instruments' BQ2010 battery-"gas-gauge" IC offers a convenient method for recording available charge stored in a nickel-cadmium or nickel-metal-hydride battery. However, even though plenty of charge remains available, under certain circumstances, transient-current spikes can fool the BQ2010 into registering a discharged battery. For example, spikes can occur when you connect a heating element or a switched-mode regulator containing a high-value input capacitor, or if you momentarily short-circuit the battery's terminals while making a connection.

During a current spike, the battery voltage decreases by the voltage drop across the battery's internal resistance plus the voltage drop across the circuit's current-sense resistor. The BQ2010 misinterprets the voltage decrease as a low-cell voltage condition normally seen during discharge. The device then loses data on the remaining battery capacity, and, depending on the application, of the BQ2010's Empty output, the load may inadvertently disconnect. Finally, the battery must contain a partial charge to un-

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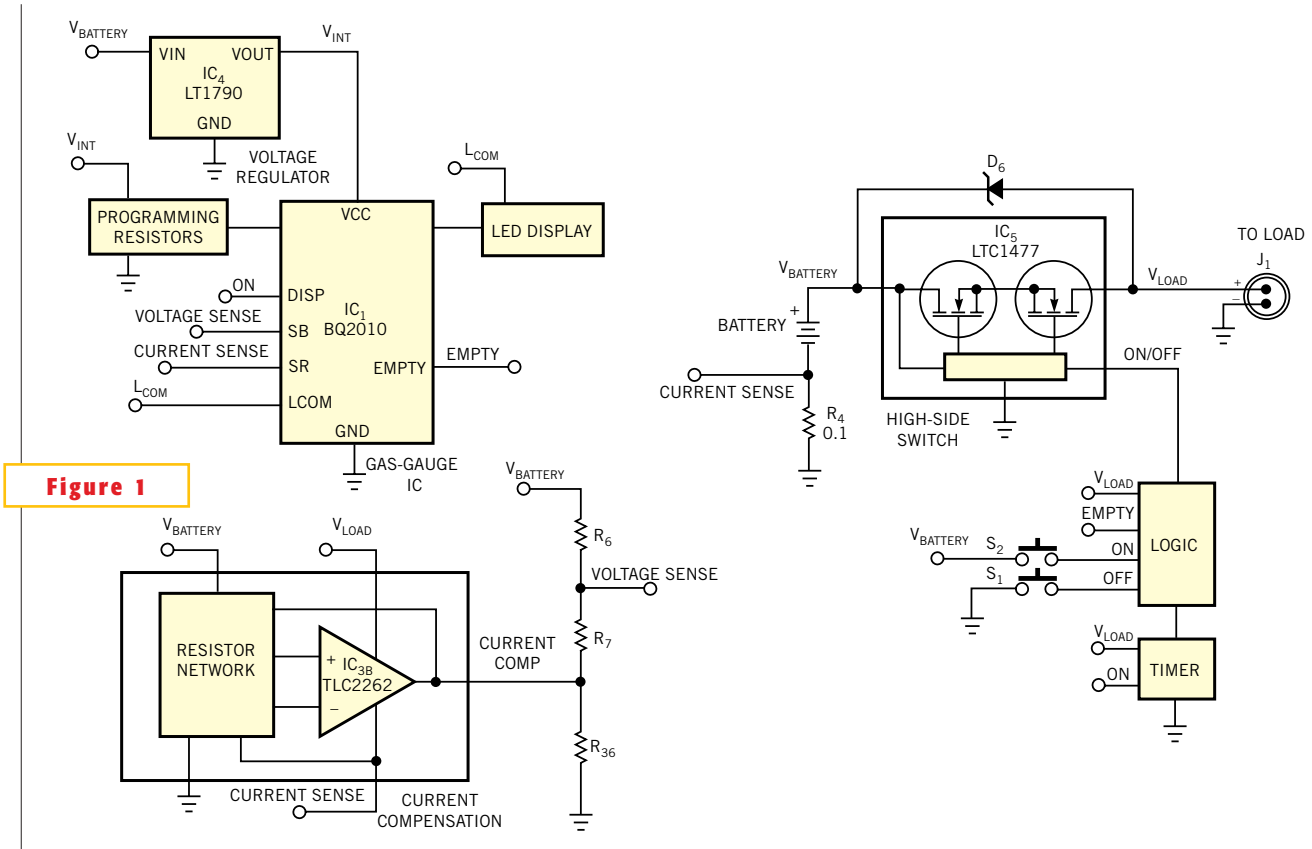
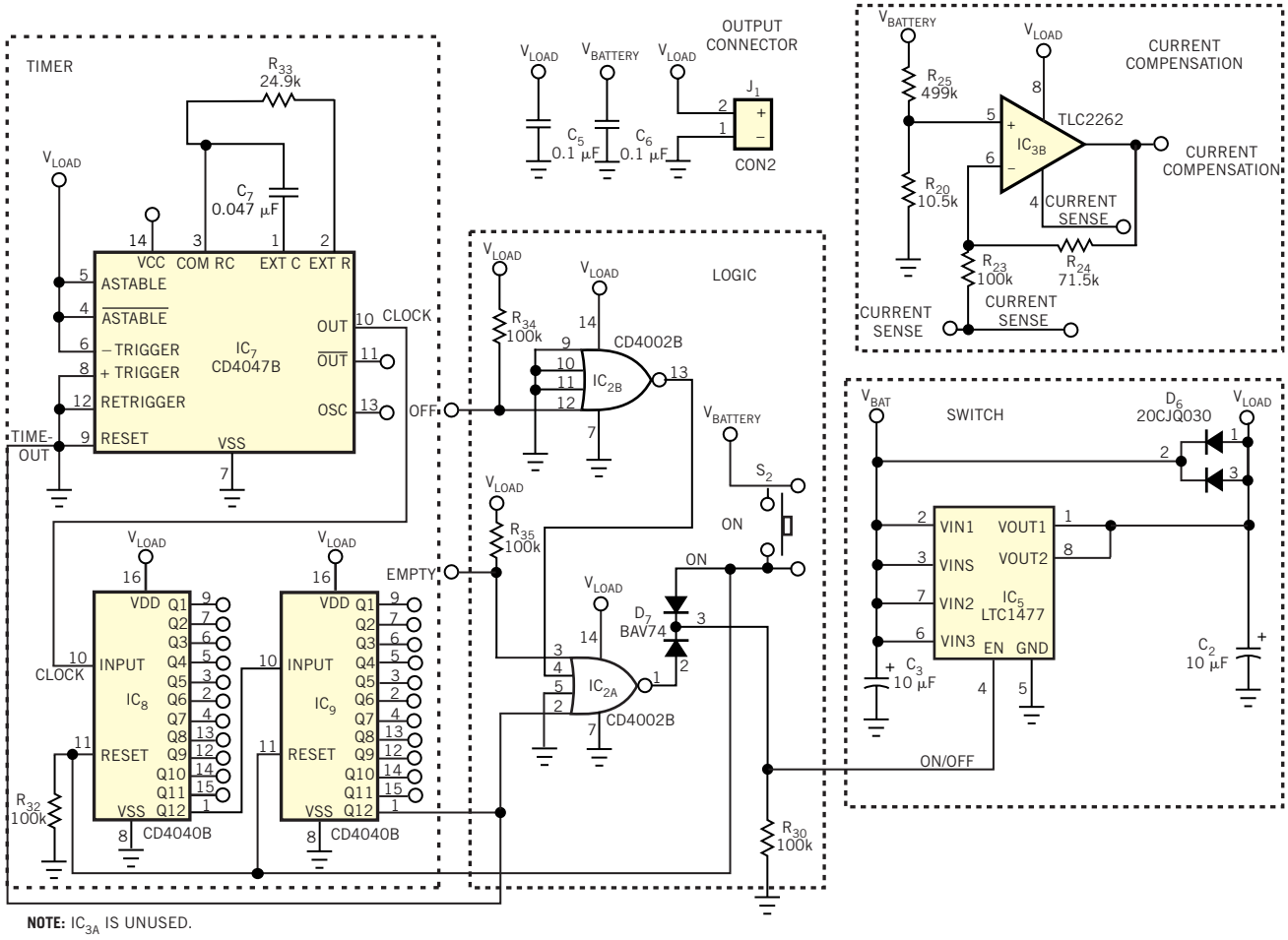


Figure 1

This circuit improves the BQ2010's current-spike immunity in several ways and adds several useful features.



NOTE: IC_{3A} IS UNUSED.

Figure 2 You can customize this circuit for a battery's chemistry, capacity, internal resistance, cell count, and timer and display options.

latch the BQ2010's Empty output.

The circuit in **Figure 1** improves the BQ2010's current-spike immunity in several ways and adds several useful features. First, a 3.3V, current-limited low-dropout voltage regulator, IC_4, supplies power to IC_1, the BQ2010. Second, an LTC1477 short-circuit-protected, high-side FET switch, IC_5, limits battery-to-load current to a maximum of 2A. To prevent IC_1's SB (single-cell voltage) monitor pin from sensing an invalid Empty state, current-compensation amplifier IC_{3B} makes the voltage to the SB pin current-independent. The negative rail of IC_{3B} connects to the active side of the ground-referenced current-sense resistor, R_4. With no load current, op amp IC_{3B}'s output should rest at 0V, but few rail-to-rail op amps provide outputs that go to 0V. The solution is to bias the positive side of the op amp enough to set the output above V_{OL} and compensate by lowering the gas-gauge-voltage sense-resistor ratio.

Additional features include a short-circuited load shutoff to prevent IC_5 from going into thermal-protection mode (**Figure 2**). Also, the entire circuit shuts off when the battery provides no current to the load or when the battery is discharged. A timer circuit consisting of IC_7, IC_8 and IC_9 provides an additional shutoff option. You can set the turnoff delay from minutes to days by changing R_{33} and C_7 to reduce the clock frequency, or by selecting other taps on binary ripple counters IC_8 and IC_9. Pressing switch S_2 or starting a recharging cycle turns the controller back on. The parallel-connected sections of Schottky diode D_6 provide a current path for recharging the battery.

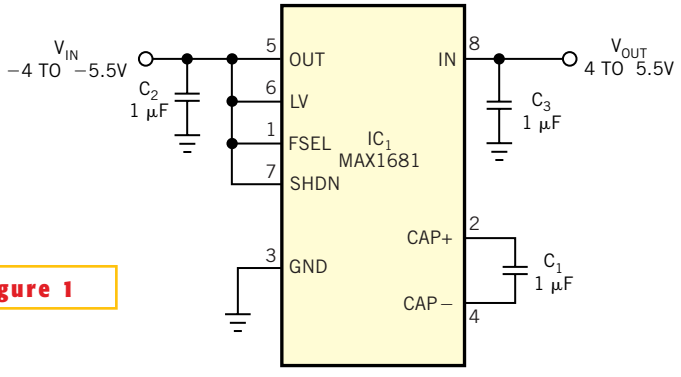
Although the resistor values shown in **Figure 2** apply to a specific application, you can customize the circuit for a battery's chemistry, capacity, internal resistance, cell count, and timer and display options. You can calculate component values via a Microsoft Excel 2002 spreadsheet in the Web version of this Design Idea at www.edn.com. All of the circuit's low-profile, surface-mounted components fit on one side of a 1.8-sq-in., four-layer board. The switches and LED readout connect to the pc board's underside.□

Charge pump converts −5V to 5V

Ken Yang, Maxim Integrated Products Inc, Sunnyvale, CA

VERSATILE SWITCHED-CAPACITOR charge-pump voltage converters can provide a negative supply voltage from a positive-voltage source or double a positive source's voltage. However, certain applications that consist entirely of ECL (emitter-coupled-logic) circuits provide only a negative-voltage supply—for example, −5.2V. **Figure 1** shows how you can use a switched-capacitor converter to obtain a positive power-supply voltage suitable for powering ECL-to-TTL (transistor-to-transistor-logic)-level translators and other circuits.

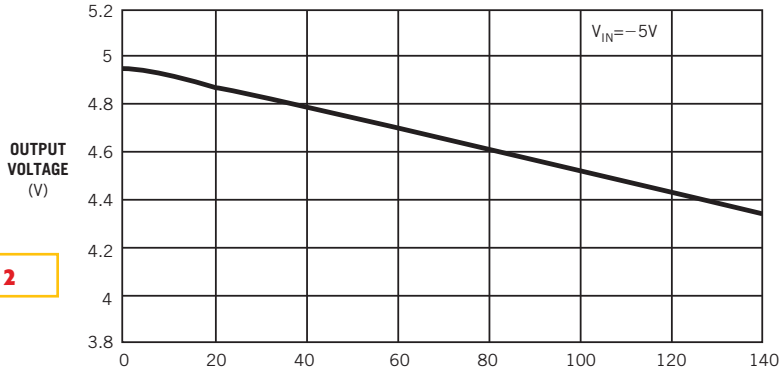
Figure 1



The "backwards" switched-capacitor converter converts −5V to 5V.

Although connections to IC_1 may appear to be reversed, the bilateral characteristics of IC_1's internal switches allow use of IC_1's output pin as its power input. Capacitor C_1 acquires a charge when IC_1's internal switches connect the CAP+ pin to ground and CAP− to the negative-voltage power source via the output pin, OUT. During the next half-cycle, IC_1 connects CAP− to ground and CAP+ to IN (normally used as the input), transferring C_1's positive charge to output capacitor C_3 and the load. With FSEL connected to OUT, an internal oscillator sets the charge-discharge cycle's frequency to approximately 1 MHz.

Figure 2



This load-voltage-versus-current graph shows the effects of the converter's nonzero output impedance on output regulation.

As **Figure 2** shows, IC_1's switches present internal resistances that affect the output voltage's magnitude, which is lower than the input voltage and subject to less-than-ideal regulation as output-load current increases. For optimum performance, use low-ESR capacitors for C_1, and input and output bypass capacitors C_2 and C_3.□

JFETs offer LC oscillators with few components

Herminio Martínez, Joan Domingo, Juan Gámiz, and Antoni Grau, Technical University of Catalonia, Barcelona, Spain

BY USING JFETs in unusual configurations, you can design simple, high-frequency LC oscillators with few passive components. The structure for implementing the amplifier stage comprises a JFET transistor that you configure as a common drain (**Figure 1**).

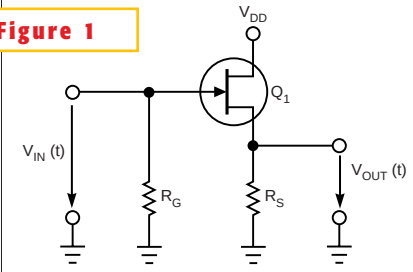
When the JFET transistor works in the saturation zone, the drain current, I_D, is:

$$I_D = \frac{I_{DSS}}{V_P^2} \times (v_{GS} - V_P)^2 = I_{DSS} \times \left(1 - \frac{v_{GS}}{V_P}\right)^2,$$

where I_{DSS} is the maximum saturation current and V_P is the pinch-off voltage. You can model the JFET in this saturation zone in the small-signal regime using an infinite input impedance and a current source that the gate-source voltage controls. The following **equation** determines the small-signal transconductance of the transistor:

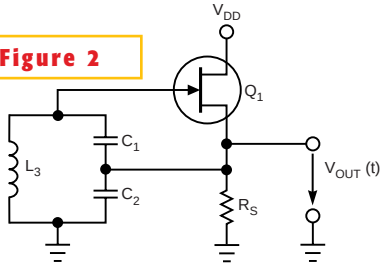
$$g_m = \frac{2I_{DSS}}{|V_P|} \times \left(1 - \frac{v_{GS}}{V_P}\right).$$

Figure 1



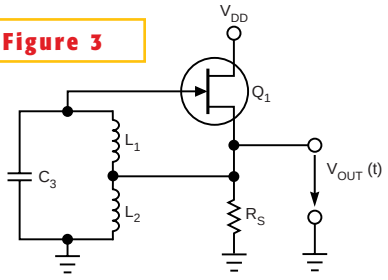
You can configure an amplifier stage, based on a JFET transistor, as a common drain.

Figure 2



To complete the oscillator circuit, you add an LC-resonant tank to the amplifier stage; the result is a Colpitts oscillator.

Figure 3



You can develop a Hartley oscillator based on a JFET transistor.

Gate resistance R_G provides the necessary connection from the gate to ground. Its typical value is in the low-megaohm range to provide the needed high impedance of the amplifier structure. Resistance R_S biases the transistor; the following **equation** determines resistance:

$$R_S = -\frac{V_{GSQ}}{I_{DQ}}.$$

To complete the oscillator circuit, you add an LC-resonant tank to the amplifier stage (**Figure 2**); the result is a Colpitts oscillator. The connection from the gate to ground for dc exists because of the inductance of the LC-resonant tank, removing the gate resistance of the amplifier.

Analyzing the circuit using the Barkhausen criterion, the frequency of oscillation f_O of the circuit is:

$$\omega_O = \frac{1}{\sqrt{L_3 \times \frac{C_1 \times C_2}{C_1 + C_2}}} \Rightarrow f_O = \frac{1}{2\pi\sqrt{L_3 \times \frac{C_1 \times C_2}{C_1 + C_2}}}.$$

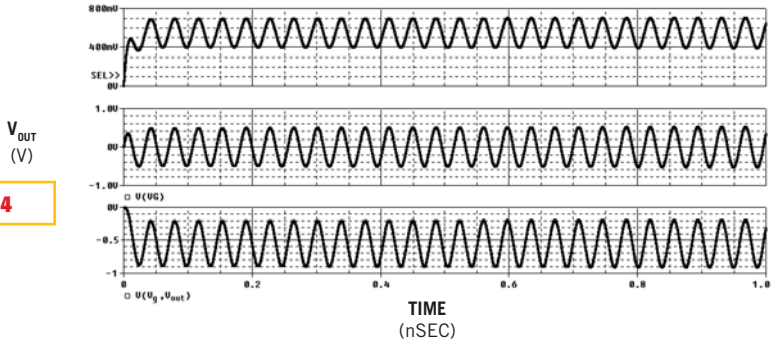
The necessary condition on the capacitors so that the circuit can oscillate is:

$$g_m \times R_S \geq \frac{C_1}{C_2},$$

or, equivalently, the voltage gain, A_V, of the amplifier stage, $V_{OUT}(t)/V_G(t)$, is:

$$A_V \geq \frac{C_1}{C_1 + C_2},$$

Figure 4



With C_1 having a value of 50 nF and C_2 having a value of 114 nF, the circuit oscillates.

where voltage gain of the common drain stage is:

$$A_V = \frac{g_m \times R_S}{1 + g_m \times R_S},$$

which demonstrates that the voltage gain in always lower than one.

Similarly, you can develop a Hartley oscillator based on a JFET transistor (**Figure 3**). The simulation and experimental results for the Colpitts oscillator circuit uses a 2N3819, an n-channel device, for the JFET. The PSpice parameters for this transistor are I_{DSS} of 12 mA and V_P of −3V. Simulation shows the voltage gain of the amplifier circuit is 0.3064V, and, with C_1 having a value of 50 nF and C_2 having a value of 114 nF, then

$$A_V = 0.3064 > \frac{C_1}{C_1 + C_2} = \frac{50}{164} = 0.3049,$$

and the circuit oscillates (**Figure 4**), which also shows the start-up process of the oscillator. The voltage gain also shows that the design meets the start-up conditions on the capacitors:

$$A_V = \frac{g_m \times R_S}{1 + g_m \times R_S} = 0.3064 \Rightarrow g_m \times R_S = 0.4417 > \frac{C_1}{C_2} = \frac{50}{114} = 0.4386.$$

Note that transconductance of the transistor is equal to the value of the slope of the curve $i_D = f(V_{GS})$ at this operating point. Depending on this point, the actual value of the transconductance will be larger or smaller. Confirming this value, when oscillations start up, the curve $i_D = f(V_{GS})$ restricts the amplitude of the output signal due to the reduction of the transconductance when V_{GS} decreases to values close to the pinch-off voltage; in this zone of the curve, its slope and, therefore, the transconductance is smaller. The intrinsic nonlinearity of the JFET transistor limits the gain of the amplifier stage, and no additional circuit stabilizing the amplitude of the output signal is necessary.□

Autostart circuit helps ATX motherboards resume operation after power interruptions

William Mohat , Ameritech, Cleveland, OH

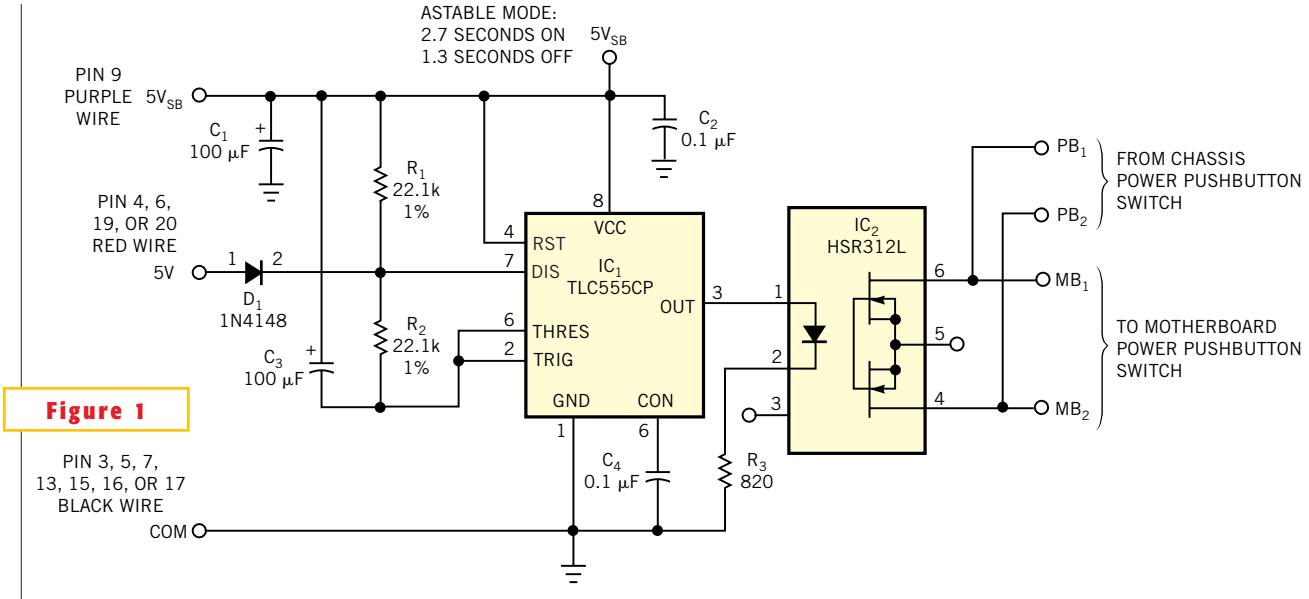


Figure 1

An inexpensive CMOS 555 timer generates power-on-switch closures upon restoration of ac power.

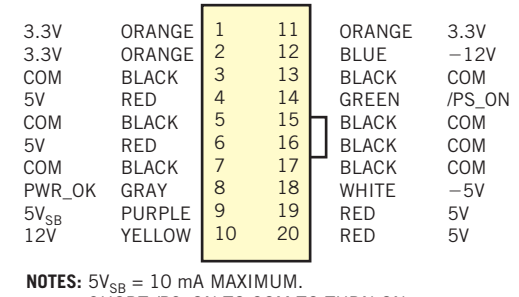
Unlike legacy PC motherboards, an ATX-style motherboard controls its power supply's on/off state. If ac power fails, many ATX motherboards do not automatically restart when power returns, and that behavior is unacceptable for a server system that must provide near-continuous service. Although some PCs provide BIOS configuration selections for "wake-on-LAN" or "wake-on-modem" operation, these options depend on another computer to provide the wake-up call. A few ATX motherboard chip sets offer an "always-on" BIOS option, but chances are, the motherboard that's available for your server system isn't one of these.

The circuit design in **Figure 1** offers a reliable method of recovery from a power interruption. Upon restoration of ac power, an ATX power supply delivers a standby voltage of 5V dc at a maximum of 10 mA via Pin 9 of its power connector (**Figure 2**). With standby power available, low-power CMOS timer TLC555 CP IC$_1$ functions as an astable oscillator and delivers pulses at approximately 4-sec intervals to MOSFET-output optoisolator IC$_2$. The output of IC$_2$ connects in parallel with the PC's front-panel power-on switch and in effect "pushes the power switch" every 4 sec.

In most astable-oscillator designs based on the generic 555 timer, timing capacitor C$_3$ connects from pins 2 and 6 to ground. Upon initial application of power, IC$_1$'s output goes low, activating IC$_2$ and generating an immediate power-on signal. Depending on the motherboard's design, an immediate start-up signal may cause the motherboard to lock up. Connecting C$_3$ as shown eliminates the initial start-up pulse.

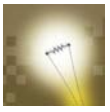
When the power supply switches on, primary 5V power becomes available at pins 4, 6, 19, and 20, driving diode D$_1$ into conduction and biasing Pin 7 of IC$_1$ to a level that stops oscillation. Although IC$_1$'s output (Pin 3) can directly drive a motherboard's power-on input, MOSFET-output optoisolator IC$_2$ removes the need to trace the polarity of the power-on switch's connections. In addition, IC$_2$ eliminates any possibility of incompatible logic levels that some 3.3V motherboards impose.

You can assemble the start-up circuit on a small section of prototyping board and splice its connections into the power supply's wiring harness and power-on pushbutton wiring. Variants of ATX connectors exist, so verify wiring before connecting the start-up circuit.□



NOTES: 5V$_{SB}$ = 10 mA MAXIMUM.
SHORT /PS_ON TO COM TO TURN ON.

Figure 2 **This view of an ATX power supply's connector shows color codes. Pinouts may differ slightly from manufacturer to manufacturer.**



Edited by Brad Thompson

Use an off-the-shelf signal source as a jitter/wander generator

Slobodan Milijevic, Zarlink Semiconductor

ENSURING THAT new networked products, such as routers, gateways or DSLAMs (digital-subscriber-line-access multiplexers) meet stringent timing specifications usually requires a specialized jitter/wander generator. As a substitute, you can use a standard function generator equipped with PM (phase modulation) or FM (frequency modulation) to measure jitter and wander tolerance. This Design Idea describes how to convert PM and FM parameters (phase deviation, frequency deviation, and modulating frequency) into jitter/wander parameters—amplitude in UIs (unit intervals) and frequency.

Network-communications engineers use the terms "jitter" and "wander" to describe phase noise in digital signals. "Wander" refers to phase noise at frequencies below 10 Hz, and "jitter" refers to phase noise at frequencies at or above 10 Hz. Defining phase noise requires specifying both its amplitude and its frequency.

As **Figure 1** shows, if you observe a clock with phase noise on an oscilloscope triggered by a clock of the same frequency but without phase noise, the rising and falling edges of the noisy clock appear blurred—that is, not clearly defined in time. If the clock has low frequency-phase noise (wander), the rising and falling edges move back and forth at a rate equal to the wander frequency. The range of this movement defines the jitter/wander amplitude.

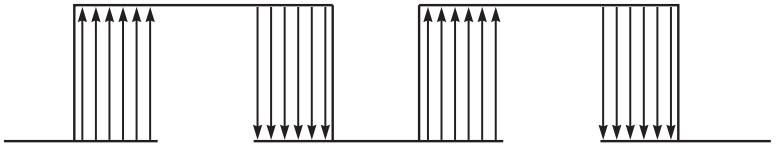


Figure 1 The effects of jitter or wander appear as position modulation of a pulse's leading and trailing edges.

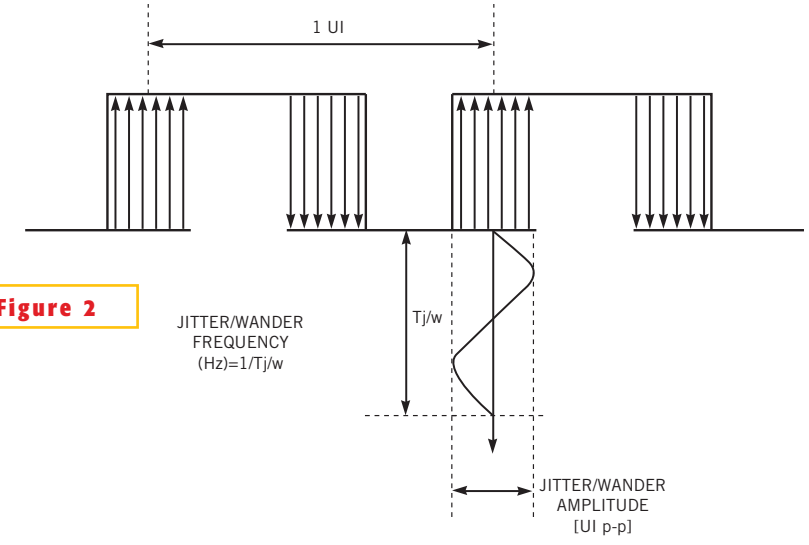


Figure 2 Applying an external signal source to a signal generator's phase- or frequency-modulation input produces a jittery output waveform.

Figure 2 illustrates an instance of sine-wave-shaped FM of jitter or wander. You can express jitter or wander amplitude in UIs; one UI is equal to the clock period. For example, the amplitude of the jitter/wander in **Figure 2** is 0.25 UI p-p.

You can use a signal generator to generate waveform jitter and wander by connecting a low-frequency signal source to the signal generator's PM or FM input. **Equation 1** applies to both FM and PM and describes the general form of an angle-modulating signal:

$$s(t)=A\cos[2\pi f_c t+\theta(t)]. \quad (1)$$

Although in digital communications, s(t) usually approximates a square-wave function, using a square wave instead of a sine wave complicates the math but doesn't affect the process of angle modulation. For simplicity, this Design Idea uses a sine-wave function for s(t).

For PM, the phase θ(t) in **Equation 1** is proportional to the modulation signal:

$$\theta(t)=D_{PM}\cos(2\pi f_m t), \quad (2)$$

where D_{PM} is the phase deviation (peak variation of the phase), and f_m represents the modulating frequency, which is also the jitter/wander frequency. The rela-

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tionship between phase deviation and jitter/wander amplitude is straightforward, and you can obtain it from:

$$\text{JITTER/WANDER[UI p-p]} = D_{PM}/180°, \quad (3)$$

where D_{PM} has units of radians in communications theory, but, for convenience, most signal generators specify units of degrees instead.

For FM, the phase θ(t) in **Equation 1** is proportional to the integral of modulating signal.

$$\theta(t) = 2\pi D_{FM} \int \cos(2\pi f_m t)\,dt, \quad (4)$$

where D_{FM} is the frequency deviation (peak variation of the frequency) and f_m is the modulating frequency. The FM modulating frequency is the same as the jitter/wander frequency. **Equation 5** yields the jitter/wander amplitude:

$$\text{JITTER/WANDER[UI p-p]} = \frac{D_{FM}}{\pi f_m}, \quad (5)$$

which derives from **Equation 6**:

$$\theta(t) = 2\pi D_{FM} \int \cos(2\pi f_m t)\,dt = 2\pi D_{FM} \frac{1}{2\pi f_m} \cos\left(2\pi f_m t - \frac{\pi}{2}\right). \quad (6)$$

Therefore, the peak-to-peak deviation of θ(t) is:

$$\theta_{PP} = 2\frac{2\pi D_{FM}}{2\pi f_m} = \frac{2D_{FM}}{f_m}, \quad (7)$$

in which the factor of 2 originates from the peak-to-peak amplitude of a sine-wave function. To get jitter/wander in peak-to-peak unit intervals, divide **Equation 7** by the period of the sine-wave function, 2π. Thus, you get **Equation 6**, which is valid only when the modulating signal comprises a sine wave because the integral of a sine wave is also a sine-wave function shifted in phase. Fortunately, most jitter/wander-tolerance tests almost exclusively use sine-wave modulation.

Some signal generators specify modulation in phase and frequency span instead of phase and frequency deviation. For PM, the span is the peak-to-peak variation of the phase, and, for FM, the span is the peak-to-peak variation of the frequency. That is, the span equals twice the deviation for both PM and FM. In this case, the jitter/wander amplitude for PM is:

$$\text{JITTER/WANDER[UI p-p]} = \frac{\text{SPAN}_{PM}}{360°}, \quad (8)$$

and it is:

$$\text{JITTER/WANDER[UI p-p]} = \frac{\text{SPAN}_{FM}}{2\pi f_m}. \quad (9)$$

for FM.□

Temperature controller saves energy

Tito Smailagich, ENIC, Belgrade, Yugoslavia

Given the high cost of electrical power, replacing a conventional on/off temperature control with a proportional controller can often save energy and money. **Figure 1** shows a low-cost, high-efficiency, time-proportional temperature controller for a residential water heater. An Analog Devices ADT14, IC_1, serves multiple functions as a temperature sensor, quad-setpoint, programmable analog temperature monitor and controller. Resistors R_1, R_2, R_3, R_4, and R_5 adjust desired temperature at setpoints SETP1, SETP2, SETP3, and SETP4, which IC_1 compares with the actual temperature from its internal sensor. The ADT14's active-low open-collector outputs drive Input Port A of IC_2, an 8-bit Motorola/Freescale 68HC908QT4 microcontroller that provides 4 kbytes of flash memory, 128 bytes of RAM, and an on-chip clock oscillator.

Available at *EDN*'s online version of this Design Idea at www.edn.com, **List-**

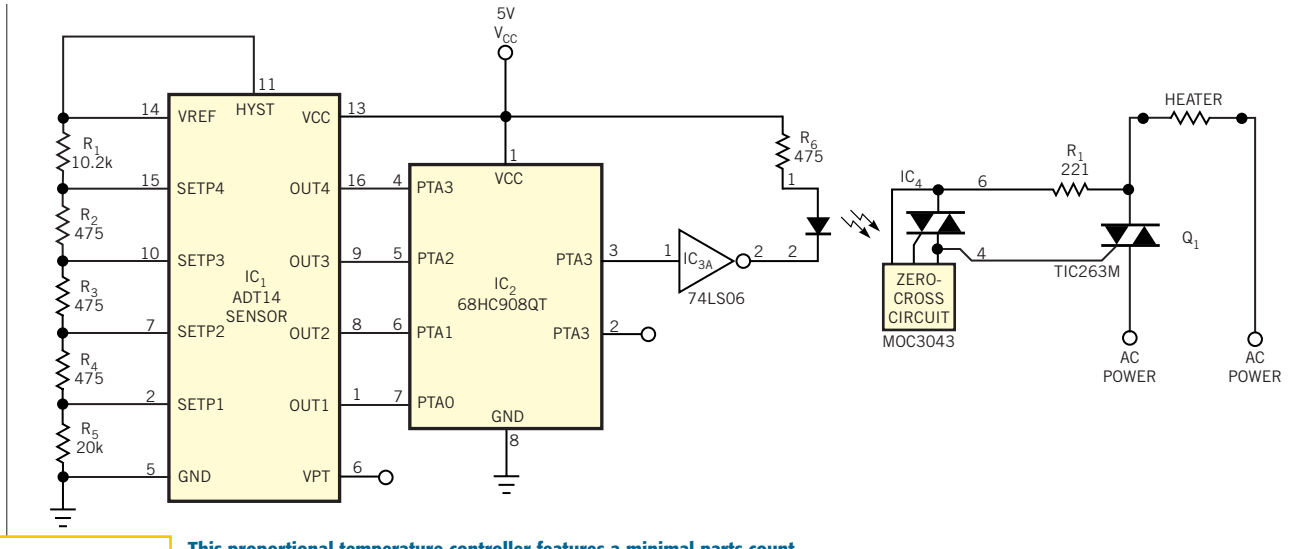

Figure 1 This proportional temperature controller features a minimal parts count.

ing 1 contains commented assembly-language software. When you load it into the microcontroller's flash memory, the software provides the time-proportional control algorithm. When IC_1's OUT1, OUT2, OUT3, and OUT4 outputs are inactive, IC_2 switches its output PTA4 to a totally on-state, 100% duty cycle for maximum heating. **Listing 2** at the Web version of this Design Idea contains an assembled version of the software, and **Listing 3** presents the hex code for programming IC_2.

When IC_1's OUT1 output is active, IC_2 produces a 75%-duty-cycle output on PTA_4. In similar fashion, when IC_1's OUT2 output goes active, IC_2 produces a 50%-duty-cycle output on $PTA4_,$ and when IC_1's OUT3 output goes active, IC_2 produces a 25%-duty-cycle output on PTA_4. When IC_1's OUT4 output goes active, IC_1 disables the output on PTA4 to produce a totally off state (0% duty cycle). **Table 1** summarizes the relationship of IC_2's inputs and output duty cycle.

TABLE 1–IC_2'S LOGIC STATES VERSUS OUTPUT DURATIONS

PTA3	PTA2	PTA1	On (%)	Off (%)	On (sec)	Off (sec)
1	1	1	100	0	10	0
1	1	1	75	25	7.5	2.5
1	1	0	50	50	5	5
1	0	0	25	75	2.5	7.5
0	0	0	0	100	100	10

To minimize component count, IC_2's internal oscillator generates a 12.8-MHz clock that divides to produce a sample pulse whose basic width is 0.1 sec for each 1% of output on-time. One cycle of output comprises 100 samples for a total duration of 10 sec. Thus, for a 25% duty cycle, IC_2's output PTA4 generates a 2.5-sec on interval followed by a 7.5-sec off interval. One section of an open-collector hex inverter, IC_{3A}, a 74LS06, drives optocoupler IC_4, an MOC3043, which features an internal zero-crossing circuit and pilot triac. Power triac Q_1, a TIC263M rated for 600V and 25A, controls application of power to the water heater's 2-kW resistive heating element. For best results, place IC_1 in close thermal contact with the water heater's inner tank.□

Calculator program finds closest standard-resistor values

Francesc Casanellas, Aiguafreda, Spain

Although it may not appear obvious to newcomers to the electronics-design profession, components' values follow one of several progressions that divide a decadewide span into equally spaced increments on a logarithmic scale. For example, when you plot the values of 1, 2.2, and 4.7 on a logarithmic scale, they divide the range 1 to 10 into three roughly equal increments (1... 2... 5). To meet requirements for greater precision, resistor manufacturers offer parts in several additional series. The most precise series divide a decade into 24, 48, or 96 increments by computing $10^{n/m}$, where n=1... (m−1), and m=24, 48, or 96, and then rounding the values to two or three digits. The results are the R_{24}, R_{48}, and R_{96} series and respectively contain 24, 48, or 96 values per decade.

TABLE 1–INPUT VALUE IN SELECTED SERIES RETURNS A CLOSEST VALUE OF:

47.8	R_{24}	47
490	R_{24}	510
12.2	R_{96}	12.1
12.3	R_{96}	12.4

You can use a Hewlett-Packard HP-48 or HP-49 calculator and one of the following programs written in RPN (Reverse-Polish Notation) to compute the nearest standard value that's closest to a required value. You enter a required resistor value, and the program returns the closest higher or lower value in the selected series. **Table 1** lists a few examples.

Each program acts as an operator by processing the first line of the calculator's stack and returning the new value in the same line of the stack. The R_{48} and R_{96} series are mathematically exact, and their programs consist of only a single line of code. The **Listings** at the Web version of this Design Idea at www.edn.com show the code. The values of the older R_{24} series are not as strictly rounded, and the program is thus somewhat more complex.

Note that the values of other components, such as capacitors, inductors, and zener diodes, also follow preferred-value series, making these programs universally applicable. You can view an earlier version of a standard-value calculator for IBM-compatible PCs at *EDN*'s online version of Design Ideas. David Kirkby of the Department of Medical Physics, University College London, UK, wrote the program in C. *EDN* first presented it, "Resistance calculator yields precise values," in the Aug 3, 1995, issue. You can read the instructions at www.edn.com/archives/1995/080395/16di5.htm. Note that certain portions of the software may require rewriting for better operation on today's PCs.□

Reduce voltage-reference output noise by half

Alfredo H Saab and Steve Logan, Maxim Integrated Products Inc, Sunnyvale, CA

Reducing low-frequency (1/f) noise generated by an IC voltage reference can prove difficult. In theory, adding a lowpass filter to a reference's output reduces noise. In practice, a lowpass RC filter for suppression of noise frequencies below 10 Hz requires large values of series resistance and shunt capacitance. Unfortunately, a high-value series resistor introduces resistance errors and thermal noise, and a shunt capacitor's leakage resistance forms an unpredictable and unstable shunt path. Together, the two components form a noisy and temperature-dependent voltage divider that directly affects the reference's accuracy and long-term stability. In addition, pc-board surface contaminants can add yet another possible leakage path and error source.

You can stack multiple voltage references in series to reduce their 1/f noise. The references' dc outputs add linearly, and their uncorrelated internal noise sources add geometrically. For example, consider a stack of four voltage references, each comprising a dc reference source, V_{REF}, in series with a random-noise generator, V_{NOISE}. Adding four reference sources produces the following outputs: $V_{REFTOTAL}=4\times V_{REF}$, and $V_{NOISE-TOTAL}=\sqrt{4\times(V_{NOISE})^2}=2\times V_{NOISE}$. The original ratio of noise voltage to dc reference voltage thus divides in half.

Figure 1 illustrates a method of adding multiple references to produce a single, less noisy reference voltage. The resistors are parts of a highly stable metal-film network, and buffer amplifier IC_5 offers low noise, low input-offset voltage, and low offset-temperature coefficients.

Tables 1 and **2** present the noise voltages that result from stacking four each of two types of 2.5V references. Each **table** shows the 0.1- to 10-Hz noise voltage for each of the four references, IC_1 through IC_4, and for the combination. Note that the dispersion in the ratios of rms to peak-to-peak values relates to subjectivity in the method of measuring the values. In addition to lower 0.1- to 10-Hz noise, the circuit also reduces long-term drift of the reference voltage.□

TABLE 1–NOISE VOLTAGES MEASURED IN FIGURE 1 USING FOUR 2.5V MAX6037 VOLTAGE REFERENCES

Measurement points	Noise (μV rms)	Noise (μV p-p)
Reduced noise output (op amp's output to V–)	1	10
Across Reference A (IC_1) (OUT to GND)	1.9	20
Across Reference B (IC_2) (OUT to GND)	1.6	19
Across Reference C (IC_3) (OUT to GND)	1.7	20
Across Reference D (IC_4) (OUT to GND)	2.7	30

TABLE 2–NOISE VOLTAGES MEASURED IN FIGURE 1 USING FOUR 2.5V MAX6143 VOLTAGE REFERENCES

Measurement points	Noise (μV rms)	Noise (μV p-p)
Reduced noise output (op amp's output to V–)	0.27	2.2
Across Reference A (IC_1) (OUT to GND)	0.52	4.7
Across Reference B (IC_2) (OUT to GND)	0.6	4.8
Across Reference C (IC_3) (OUT to GND)	0.5	4.3
Across Reference D (IC_4) (OUT to GND)	0.55	4.7

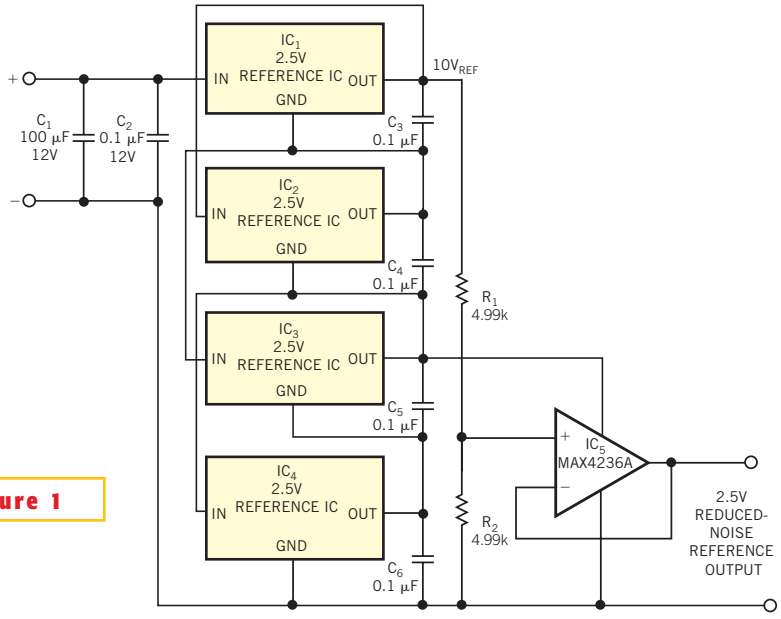

Figure 1

Four 2.5V references, IC_1 through IC_4, produce 10V. Resistors R_1 and R_2 form a voltage divider that reduces the 10V output to 2.5V and lowers the output-noise voltage by half. Buffer amplifier IC_5 isolates the reference circuit from the load.

Touch switch needs no dc return path

Brad Albing, Philips Medical Systems Inc, Cleveland, OH

Common designs for touch switches detect a decrease in resistance when a user's fingertip either connects a contact to the circuit's common ground or supplies an injection of 60-Hz ac voltage, resulting from immersion in the electrostatic field that nearby power lines radiate. But what if no nearby power lines exist and the equipment operates from a battery source, such as in an automotive application, or if a galvanic contact to circuit common is unavailable?

The circuit shown in **Figure 1** operates by sensing an increase in capacitance that results from touching a contact. Although a straightforward design might require a complex circuit, the design shown offers a low-cost approach that uses few components.

In **Figure 1**, IC_{1A} operates as a square-wave oscillator at approximately 150 kHz. The oscillator's output gets ac-coupled to potentiometer R_2 that sets the drive level and, hence, the sensitivity for the touch pad. Applying negative excursions of several volts of square-wave signal to its gate repetitively drive N-channel JFET Q_1 from conduction into cutoff. An approximation of the square wave swinging from 0 to 12V appears at Q_1's drain. A peak detector circuit formed by D_1, R_7 and C_4 provides sufficient dc voltage to force IC_{1B}'s output to a logic low.

However, if someone touches the touch pad, any added capacitance to ground or circuit common reduces the ac drive at the FET's gate, and Q_1 continuously conducts. The square-wave voltage applied to D_1 decreases. The voltage on C_4 drops below the logic threshold, and IC_{1B}'s output goes high. You can adjust R_2 to set sensitivity and compensate for device-to-device variations in the FET's pinch-off voltage. For novelty or nostalgia's sake, you can use one-half of a 12AX7 dual triode as an oscillator and the remaining half in place of Q_1. Selecting plate resistors allows operation with a 12V plate power supply.□

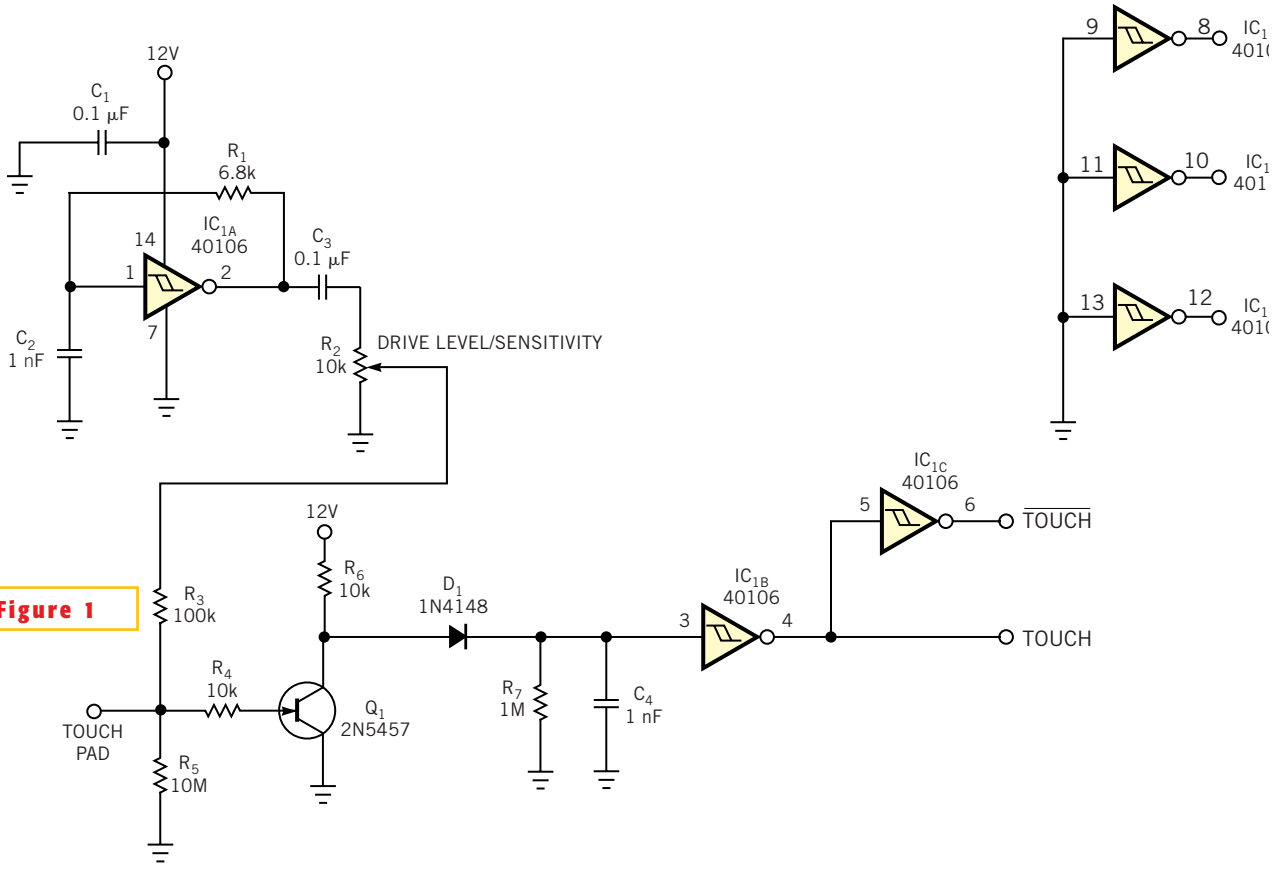

Figure 1

A low-cost touch-switch interface uses three Schmitt trigger hex inverters and a single JFET per channel.

Edited by Brad Thompson

Pushbuttons and digital potentiometer control boost converter

Simon Bramble, Maxim Integrated Products Inc, Wokingham, UK

DIGITALLY CONTROLLED potentiometers are useful for generating analog control voltages under the control of a microcontroller. In some applications, manual pushbutton switches could replace a microcontroller and simplify product design. Mechanical switches exhibit contact bounce, and, when a user actuates them, they may open and close many times before reaching a stable state.

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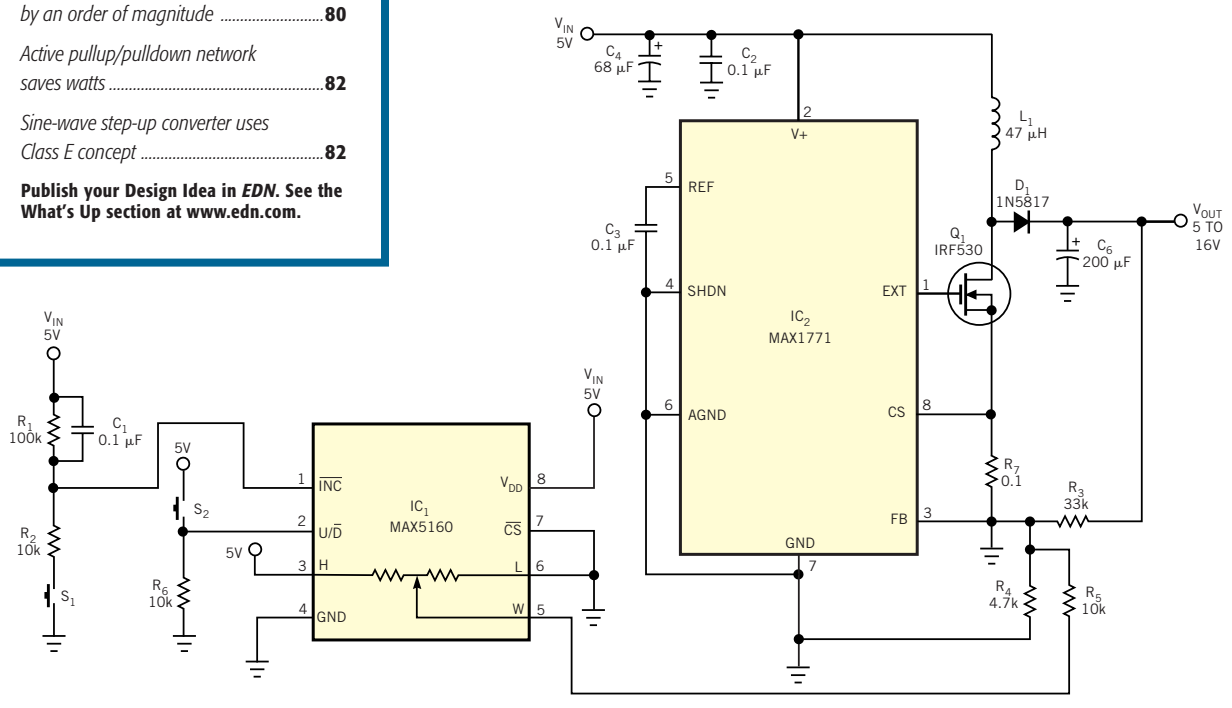
A digital potentiometer's control inputs lack switch-debouncing capabilities, and its up/down control is not suited for pushbutton operation. **Figure 1** illustrates solutions to these issues and shows how to use a digital potentiometer to control a boost converter.

The potentiometer, IC_1, a MAX5160M, presents an end-to-end resistance of 100 kΩ. To increment the wiper's position, W, you press and hold the U/$\overline{D}$ pushbutton, S_2, to pull the U/$\overline{D}$ pin high and then press and release pushbutton S_1 to pulse the $\overline{INC}$ input. Similarly, you decrement the wiper position by releasing S_2 and pulsing S_1.

A time-delay network comprising R_1, R_2, and C_1 masks S_1's switch bounce, which would otherwise toggle the wiper's position between V_{DD} and approximately 0V. When you press S_1, capacitor C_1 charges via R_2 and causes the $\overline{INC}$ pin to ramp slowly toward 0V, thereby removing the effects of S_1's contact bounce. The R_1C_1 time constant requires that you depress S_1 for several milliseconds before the INC input takes effect.

In this application, switching converter IC_2, a MAX1771, operates as a standard boost converter and increases its 5V input to a higher voltage positive output. You can use **Equation 1** to set IC_2's out-



A digital potentiometer, IC_1, and two pushbutton switches, S_1 and S_2, let you adjust the regulated output voltage of boost converter IC_2 over a 10V range.

Figure 1

put to a nominal 12V output without the digital potentiometer:

$$V_{OUT} = \frac{1.5 \times (R_3 + R_4)}{R_4}. \quad (1)$$

Connecting IC_1's wiper via 10-kΩ resistor R_5 to IC_2's FB (feedback) node sets IC_2's voltage-feedback level. Although inclusion of feedback resistors R_3, R_4, and R_5 and digital potentiometer IC_1 complicates the precise calculation of IC_2's output voltage, you can simplify the math by calculating the output voltages at the potentiometer's extreme settings. Thus, with IC_1's wiper set to 0V, R′ equals the paralleled resistance of R_4 and R_5, and IC_2's maximum output voltage becomes **Equation 2**:

$$V_{MAX} = \frac{1.5 \times (R_3 + R')}{R'}, \quad (2)$$

or V_{MAX}=16.84V.

With IC_1's wiper set to 5V, you can attempt to calculate the minimum output voltage by summing voltages into the feedback node:

$$V_{MIN} = \left[\left\{ \frac{V_{FB}}{R_4} - \left(\frac{5 - V_{FB}}{R_5} \right) \right\} \times R_3 \right] + V_{FB}. \quad (3)$$

which simplifies to V_{MIN}=0.48V. However, **Equation 3** provides an incorrect value for V_{MIN} because a boost converter's output voltage cannot go below its input voltage. You can approximate V_{MIN} by substituting a value of 10 kΩ for R_5 in **Equation 3** and solving for V_{MIN}: V_{MIN}=4.93V. Refer to the manufacturer's application notes for additional component information.□

Microcontroller protects dc motor

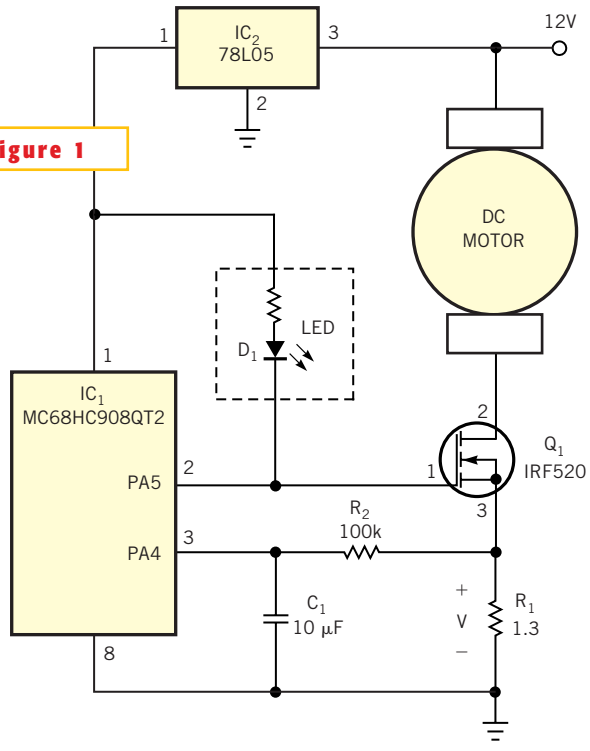
Abel Raynus, Armatron International Inc, Malden, MA

Although any overloaded dc motor can draw excessive current and sustain damage, a cooling fan's motor is particularly vulnerable due to fouling by dust, insects, or misplaced objects. A few fans include built-in overload protection, and others can use an external warning device, such as Microchip's TC670 fan-failure detector.

In many products, it's essential not only to detect an overloaded motor, but also to switch off the motor to prevent failure. Although you can design a protection system around the TC670, a low-end microcontroller can offer a less expensive, more flexible, and easier to implement alternative. If a product includes a microcontroller, only two spare pins are necessary for motor protection.

Figure 1 shows a dedicated protection circuit based on a small microcontroller and a power FET. This project uses an eight-pin flash-memory MC68HC908QT2 from Freescale and an IRF520A FET from Fairchild to control a dc brushless-fan motor rated for 0.72A at 12V dc. A high or low output voltage on output PA5 of IC_1 controls Q_1, an N-channel FET that in turn controls the motor. Current through the motor develops a voltage, V, that's proportional to the motor current across sense resistor R_1. A lowpass filter comprising R_2 and C_1 reduces noise on the sense voltage you apply to input PA4 and IC_1's built-in A/D converter. Voltage regulator IC_2 provides stable 5V power for IC_1.

Figure 1



NOTE: D_1, A LITE-ON LTL-4223-R2, INCLUDES A BUILT-IN RESISTOR.

Controller for dc brushless fan motor features minimal parts count.

Under normal operation, the voltage across R_1 measures approximately 0.52V. When the motor undergoes an overload, voltage increases until it reaches a preset upper limit of 0.85V. The output on PA5 then drops to a low level, switching off transistor Q_1 to stop the motor, and lighting D_1 to indicate the overload. When the motor stops, it draws no current, and the sense voltage falls below the minimum threshold value of 0.3V. The microcontroller's output on PA5 remains low and holds off Q_1, a state that it maintains indefinitely until you cycle the circuit's power off and then on.

The control program, in assembly language for the MC68HC908, features a straightforward algorithm adaptable to other microcontrollers that include an A/D converter. A 2.5-sec delay routine prevents the motor from starting until the system's power-supply voltage stabilizes. You can download the listing from the online version of this Design Idea at www.edn.com.□

Improved Kelvin contacts boost current-sensing accuracy by an order of magnitude

Craig Varga, National Semiconductor Corp, Phoenix, AZ

Many power-supply designs rely on accurately sensing the voltage across a current-sense element. Multiphase regulators use the sense voltage to force current sharing among phases, and single-phase regulators to control the current-limit setpoint. As internal complexity and clock speeds increase, processors impose narrower operating margins for power-supply voltages and currents, which in turn make accurate current sensing critically important. The most accurate of several available methods involves inserting a low-value current-sensing resistor in the power supply's output path. Another popular technique uses the parasitic resistance of a switching regulator's output inductor as the sense element. For either method, currents of 20A or more per power-supply phase impose a sense-resistance limit of approximately 1 mΩ. Precision resistors of 1% accuracy are available at reasonable cost, but an error of 1% of 1 mΩ amounts to only 10 μΩ.

The resistance of solder joints that attach a sense resistor or inductor can easily exceed 10 μΩ and, worse yet, can vary significantly during a production run. In the past, discrete four-wire resistors provided separate high-current and sense-voltage connections, allowing accurate Kelvin sensing and excluding voltage drops that the high-current connections introduce. Unfortunately, four-wire sense resistors or inductors are unavailable in low cost SMD packages. Thus, most power-supply designers use two-wire sense components and apply a Kelvin-connection pc-board-layout technique (**Figure 1**). However, test results reveal that applying conventional Kelvin sensing techniques to low-value resistors introduces transduction errors as high as 25%—an unacceptable error margin for designs that require high accuracy.

So, what's a power-supply designer to do? The answer involves a slight variation on an old idea that requires only a minor change in a sense resistor's mounting footprint. To compare performance of conventional Kelvin connections versus the proposed method, a test board includes three pc-layout footprints for installation of 1-mΩ, 1%-accurate, surface-mount resistors. In all three patterns, current enters and exits the resistor via traces (not shown) on the pads' left and right sides, respectively.

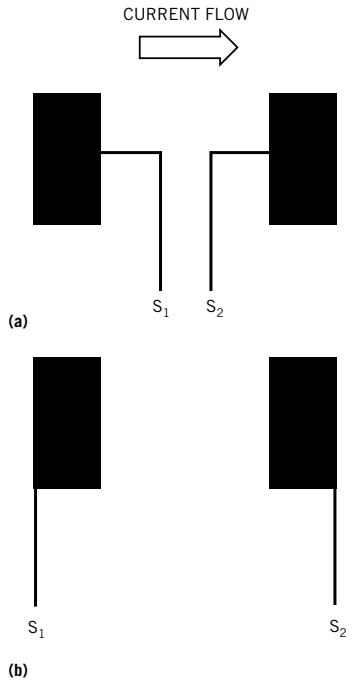


Figure 1 Conventional solder pads offer two choices for Kelvin connections: on the pads' inner edges (a) or outer corners (b).

In **Figure 1a**, applying a current of 4.004A produces a sense voltage at the Kelvin terminals of 4.058 mV, a 1.35% error. At 8.002A, the sense voltage at the Kelvin terminals measures 8.090 mV, a 1.1% error. In **Figure 1b**, a current of 4.004A produces a sense voltage at the Kelvin terminals of 5.01 mV, a 25% error. At 8.002A, the sense voltage at the Kelvin terminals measures 9.462 mV for an error of 18.2%. **Figure 2** shows an improved component footprint. Each large solder pad includes a central cutout area that partially surrounds a narrow pad that solders directly to the sense element and thus carries no current. This approach removes from the sense path the large-area solder joints that mount the part and carry high load current.

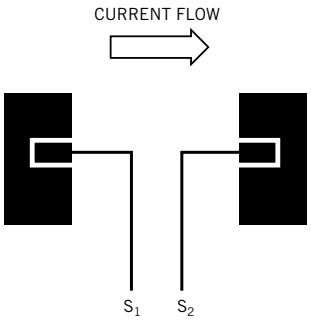


Figure 2 Modified pads provide isolated Kelvin connections that eliminate errors introduced by voltage drops across soldered connections carrying high current.

When you apply a current of 4.002A to the pads in **Figure 2**, voltage at the Kelvin terminals measures 4.004 mV, a 0.05% error. At 8.003A, the sense voltage measures 8.012 mV, an error of only 0.11% and an order of magnitude improvement over **Figure 1a**. Sense-voltage variation over temperature should greatly improve, and solder-thickness variation no longer affects the sense voltage. Best of all, the technique costs nothing to implement.

Obviously, the technique in **Figure 2** works only with terminations sufficiently wide to allow dividing the solder pad into three sections and still retain adequate soldering area to handle the high-current connections. However, for many designs, this simple technique can significantly improve the accuracy of current sharing, V-I load-line characterization, and current-limit setpoints.□

Active pullup/pulldown network saves watts

JB Guiot, DCS Dental AG, Allschwil, Switzerland

The control circuit in **Figure 1** presents a relatively low input resistance and thus imposes a low value on external pulldown resistor R_1 to provide the desired low-level input voltage. In turn, R_1 wastes power by drawing a relatively high current through switch S_1. For example, suppose that the control circuit presents an input resistance of 2.2 kΩ and requires a logic-low input of 5V or less. At a V_{CC} of 24V, R_1 must not exceed 500Ω for a current drain of 24/500=48 mA. The power dissipated in R_1 is thus $24^2/0.5=1152$ mW, which requires a 2W resistor for reliable operation.

In this application, the system includes three controls with three input circuits, which present a total current of 432 mA and adds approximately 10W to the power budget. To reduce wasted power, it uses an active pulldown circuit (inside the dashed line in **Figure 2**). As long as switch S_1 remains closed, PNP transistor Q_1's base voltage exceeds its emitter voltage due to diode D_1's forward voltage drop. Thus, Q_1 doesn't conduct, and the control circuit's input voltage rests at $V_{CC}-0.7V$ (D_1's forward voltage drop).

Opening S_1 reverse-biases D_1, and the base current flowing through resistor R_1 turns on Q_1, which saturates and pulls the circuit's input to $V_{CE(SAT)}$. Closed-circuit current through S_1 is thus V_{CC}/R_1. For example, with V_{CC} of 24V and R_1 having a value of 10 kΩ, I=24/10=2.4 mA, and R_1 dissipates 0.058W, or approximately 20 times less power than in **Figure 1**. In this application, current demand of the nine control-circuit inputs decreases from 432 to 22 mA and saves pc-board space by eliminating the need for using 2W. As a variant, **Figure 3** shows an active-pullup version of the circuit.□

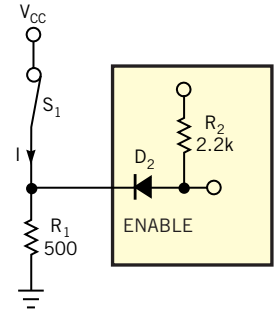


Figure 1 A conventional network requires a low-value pulldown resistor.

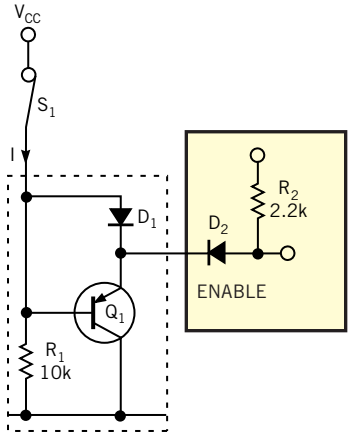


Figure 2 An active pulldown circuit substitutes a saturated transistor for a power-consuming pulldown resistor.

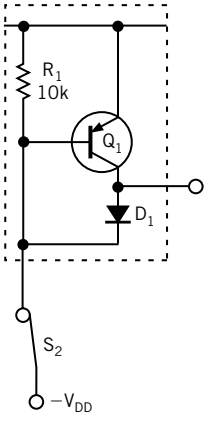


Figure 3 Rearranging the circuit and using an NPN transistor for Q_1 yields an active-pullup network.

Sine-wave step-up converter uses Class E concept

Louis Vlemincq, Belgacom, Evere, Belgium

Many power applications ranging from luminescent and fluorescent lighting to telephone-ringing voltage generators require a more or less sinusoidal-drive voltage. These applications typically require a waveform of only moderate quality, and its frequency isn't especially critical. However, avoiding waveform discontinuities that cause unwanted current peaks, excessive device dissipation, and EMC problems rules out using filtered square waves or other stepped waveforms. Sometimes, a trapezoidal drive may be acceptable but it's only a second choice at best. This Design Idea proposes a method of generating sine waves that offers a number of advantages over more complex methods:

The circuit requires only one power-switching device, and you can use an analog or a digital signal to drive the switching device. The circuit also requires only a few components: a diode, a switching transistor or a MOSFET, an inductor or a transformer, and a capacitor. Further, the design's circuit losses are low, and the switching device experiences minimal stress during operation. **Figure 1** shows the basic circuit, and **Figure 2** illustrates

(continued on pg 86)

(continued from pg 82)

waveforms within the circuit.

In operation, the sine-wave output appears across inductor L in a series LC circuit. An external clock source produces gate drive for transistor Q at a frequency that's lower than the LC circuit's natural resonant frequency. When the transistor conducts, the inductor receives a charging current via diode D. When conduction ends, energy stored in the inductor transfers to capacitor C, and a damped oscillation begins (uppermost trace in **Figure 2**). The voltage across capacitor C approximates a sine wave (top trace). Drain current in transistor Q shows that no current flows until the capacitor voltage forward-biases diode D (middle trace). The gate-drive pulse interval is lower than the series-resonant frequency that L and C present (bottom trace).

During the negative-going portion of the cycle, the external clock source applies gate drive to the transistor. Diode D is still reverse-biased, and thus no current flows into Q. When the voltage across C goes positive, diode D conducts and allows current to recharge the inductor and replenish energy lost in the previous cycle. In balanced operation, energy supplied during the conduction phase replenishes energy supplied to the load and dissipated in component losses.

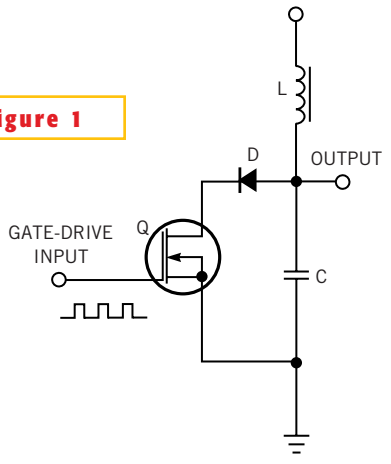
To produce a higher peak voltage, you extend the conduction interval by raising the drive frequency or by extending the on interval. You can regulate the output voltage by applying conventional closed-loop feedback techniques to a variable-frequency clock oscillator or, in digital systems, by altering the clock's duration. For most applications in which load current is relatively fixed, such as in an electroluminescent panel lamp, an open-loop adjustment or manual control offers sufficient flexibility once you determine a clock-frequency range that corresponds to the desired degree of illumination.

For peak voltages not exceeding 10 times the power-supply voltage, you can connect the load directly to the junction of D, L, and C. You can achieve higher voltage-to-step-up ratios at the expense of applying additional voltage and current stress to L and C. Instead, you can add an isolated secondary step-up winding to the inductor. For optimum efficiency, use components designed for high-frequency power handling—for example, a polypropylene-dielectric capacitor and a low-loss inductor.

If the load consists of an electroluminescent panel that behaves as a lossy capacitor, you may be able to eliminate the use of external capacitor C. Transistor Q must obviously be able to withstand peak voltages and currents that the circuit imposes, but its specifications are otherwise relatively noncritical. No switching loss occurs at the beginning of the conduction due to the Class E mode of operation, and the output capacitor assists the device's turn-off recovery. For output voltages not exceeding approximately 50V, you can improve efficiency by selecting a Schottky or other fast-recovery diode for use in the circuit.

For powering lamps and generating telephone-ringing signals, the sine wave's "flat spots" are of little consequence because of their relatively short duration and low harmonic-energy content. You can minimize these intervals by reducing the LC ratio and thus increasing the loaded Q factor of the LC circuit. However, for a given output voltage, increasing Q factor also increases the peak current because the same amount of energy must transfer to the inductor in less time.□

Figure 1



Few components are necessary to produce a pseudo sine wave.

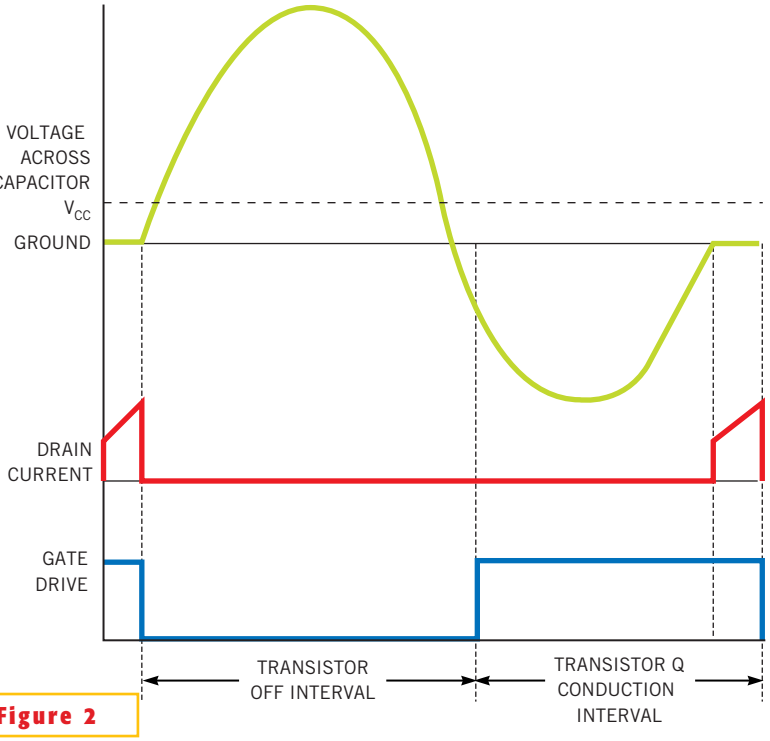
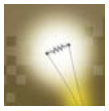


Figure 2

The circuit in Figure 1 produces these waveforms.



Edited by Brad Thompson

Bandpass filter features adjustable Q and constant maximum gain

Herminio Martínez, Joan Domingo, Juan Gámiz, and Antoni Grau, Technical University of Catalonia, Barcelona, Spain

Applications such as audio equalizers require bandpass filters with a constant maximum gain that's independent of the filter's quality factor, Q. However, all of the well-known filter architectures—Sallen-Key, multiple-feedback, state-variable, and Tow-Thomas—suffer from altered maximum gain when Q varies. **Equation 1** expresses the second-order bandpass transfer function of a bandpass filter:

$$H_{BP}(s) = K\frac{\left(\frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1}, \quad (1)$$

where K represents the filter's gain constant. When the input frequency equals ω_O, the filter's gain, A_{MAX}, is proportional to the product, KQ. Thus, modifying the quality factor alters the gain and vice versa.

This Design Idea describes a filter structure in which K is inversely proportional to Q. Altering Q also modifies K, producing a magnitude-plot set in which the curves maintain the same maximum gain at the central frequency ω_0—that is, KQ remains constant. **Figure 1** shows the filter, which comprises a twin T cell with an adjustable quality factor and a differential stage. The differential stage comprises op amp IC_3 and resistors R_{5A} through R_{5D}. This stage outputs the difference between the filter's input signal and the twin-T network's output. Capacitors C_1 and C_2 are of equal value, $C=C_1=C_2$, capacitor C_3 equals 2C, resistors R_1 and R_2 are also equal and of value $R=R_1=R_2$, and R_3 equals $R/_2$. **Equation 2** describes the twin-T circuit's transfer-function response as a notch filter producing output $V_{BR}(t)$:

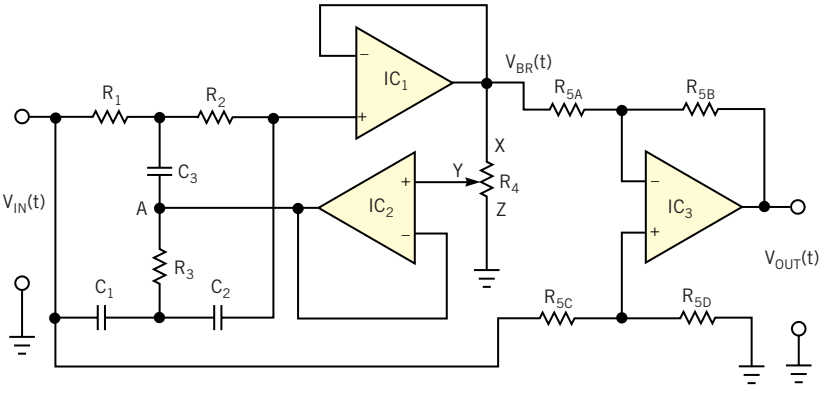


Figure 1 This bandpass active filter features adjustable Q and maximum gain in the passband and consists of a twin-T cell with Q adjustment and a differential output stage. You can also extract a frequency-notch output from the voltage-follower stage.

$$H_{BR}(s) = \frac{V_{BR}(s)}{V_{IN}(s)} = \frac{(RCs)^2 + 1}{(RCs)^2 + 4RC(1-m)s + 1}. \quad (2)$$

Equation 3 describes the compete circuit's transfer function, a bandpass-filter response with output $V_{OUT}(t)$:

$$H_{BP}(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{4RC(1-m)s}{(RCs)^2 + 4RC(1-m)s + 1}, \quad (3)$$

where m represents the twin-T cell's feedback factor. If you designate R_{XY} as the resistance potentiometer R_4's upper terminal, Point X; the rotor as Point Y; and R_{YZ} as the resistance between the rotor and the bottom terminal, Point Z, you can express m as the quotient of **Equation 4**:

$$m = \frac{R_{YZ}}{R_{XY} + R_{YZ}} = \frac{R_{YZ}}{R_4}. \quad (4)$$

Comparing **Equation 3** with the respective normalized transfer functions of a bandpass filter, **Equation 1**, **Equation 5** expresses the central frequency of the filter, ω_O, coincident with the transmission zero of the twin-T network:

$$\omega_0 = \frac{1}{RC}. \quad (5)$$

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Equations 6 and **7**, respectively, give quality factor Q and gain constant K:

$$Q = \frac{1}{4(1-m)}; \quad (6)$$

$$K = \frac{1}{Q} = 4(1-m). \quad (7)$$

The maximum gain, A_{MAX}, at $\omega=\omega_O$, always remains constant and equal to 1 (0 dB) and is independent of Q. The minimum quality factor is 1/4 for m=0, which corresponds to the potentiometer's rotor connected to ground. The maximum gain is theoretically infinite, but, in practice, it's difficult to achieve a quality factor beyond 50. In most applications, Q ranges from 1 to 10.

Figure 2 shows the filter's magnitude and phase Bode plots for the frequency-notch output $V_{BR}(t)$ (available at IC_1's output) for values of m from 0.1 to 0.9. **Figure 3** shows Bode plots for the filter's bandpass output, $V_{OUT}(t)$, for the same values of m. In both graphs, frequency f_O equals 1061 Hz. To minimize frequency-response variations and improve response accuracy, you can build the filter with precision metal-film resistors of 1% or better tolerance. Likewise, use close-tolerance mica, polycarbonate, polyester, polystyrene, polypropylene, or Teflon capacitors. For best performance, avoid carbon resistors and electrolytic, tantalum, or ceramic capacitors.□

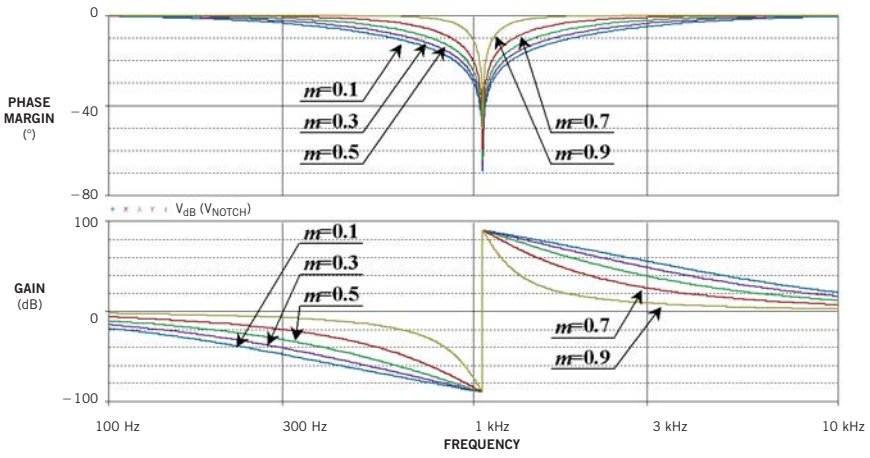


Figure 2 Magnitude and phase Bode plots at the frequency-notch output, $V_{BR}(t)$, show effects of varying twin-T-cell feedback factor, m, from 0.1 to 0.9.

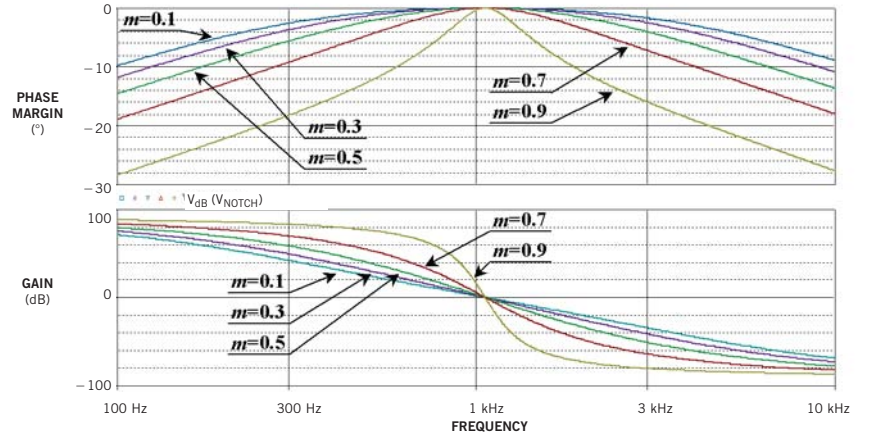


Figure 3 Magnitude and phase Bode plots at the bandpass output, $V_{OUT}(t)$, show effects of varying twin-T-cell feedback factor, m, from 0.1 to 0.9.

Moving-coil meter measures low-level currents

Kevin Bilke, Maxim Integrated Products Inc, Hook Hants, UK

Although an analog moving-coil meter may lack the resolution and accuracy that a digital readout provides, a meter remains the display of choice for certain applications. A digital readout simply cannot provide information about a measurement's rate of change, and tracking a reading's trend is easier on an analog meter.

Large moving-coil meters may require significant amounts of current for full-scale deflection, and using a shunt resistor may prove impractical when the meter current is larger than the current you are measuring. You can solve the problem by driving the meter from a separate power supply (**Figure 1**). In this example, an 8-in. moving-coil meter that requires 15 mA for full-scale deflection displays a current range of 0 to 1A dc. This technique can also simplify specifying or fabricating shunt resistors for custom current ranges. Unlike other current-sense amplifiers that derive operating power from the current you are measuring, IC_1 provides a separate supply-voltage terminal for its internal circuitry. In operation, IC_1's output current, I_{OUT}, equals $V_{SENSE}/100V$, where V_{SENSE} is the voltage across R_{SENSE1}.

This Design Idea uses IC_1 rather than the many current-sense amplifiers available because it provides a separate supply-voltage terminal for the internal circuitry, whereas other devices take power from the current you are measuring. In this application, a full-scale current of 1A develops 1V across R_{SENSE1}, which IC_1 converts to a maximum output current

of 10 mA that produces a maximum voltage of 1V across R_1. Operational amplifier IC_2 and transistor Q_1 form a voltage-controlled current sink that draws current through meter M_1. A full-scale reading of 15 mA develops 1V across 66Ω resistor R_{SENSE2}. You can adjust the resistor's value to calibrate the meter or to alter the full-scale current range.

This circuit also allows separation of the measurement point and meter location. Moving-coil meters are not intended for applications that require precision measurement, and you can use relaxed-accuracy passive components. Bypass the instrument-supply voltage with decoupling capacitors that the electrical-noise environment requires.□

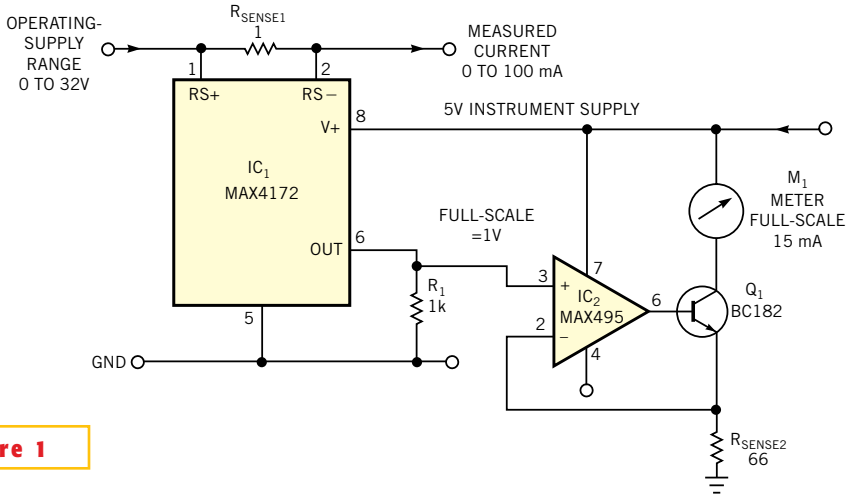


Figure 1

This circuit displays current on a moving-coil meter that consumes a substantial fraction of the current you are measuring.

MOSFET enhances voltage regulator's overcurrent protection

Herb Hulseman, Eagle Test Systems, Mundelein, IL

The classic LM317 adjustable-output linear voltage regulator offers a relatively high, if package-dependent, current-handling capability. In addition, the LM317 features current limiting and thermal-overload protection. With the addition of a few components, you can enhance an LM317-based voltage regulator by adding a high-speed short-circuit current limiter (**Figure 1**). Under normal operation, resistors R_2 and R_3 apply V_{GS} bias to power MOSFET Q_1, an IRF4905S, which fully conducts and presents an on-resistance of a few milliohms. The voltage drop across current-sampling resistor R_1 is proportional to IC_1's input current and provides base drive for bipolar transistor Q_2.

As load current increases, the voltage across R_1 increases, biasing Q_2 into conduction and decreasing Q_1's gate bias. As Q_1's gate bias decreases, its on-resistance increases, limiting the current into IC_1, according to $I_{MAX}=V_{BE}Q_2/R_1$, or approximately 0.6V/1Ω.

Resistors R_5 and R_6 set IC_1's output voltage, as the LM317's application notes describe. By varying the value of R_1, you can adjust the circuit's limiting current from milliamperes to the LM317's maximum current-handling capability.

Diodes D_1 and D_2, respectively, protect against capacitive-load discharge and polarity reversal. Depending on the circuit's requirements, IC_1 and Q_1 may require heat dissipators.□

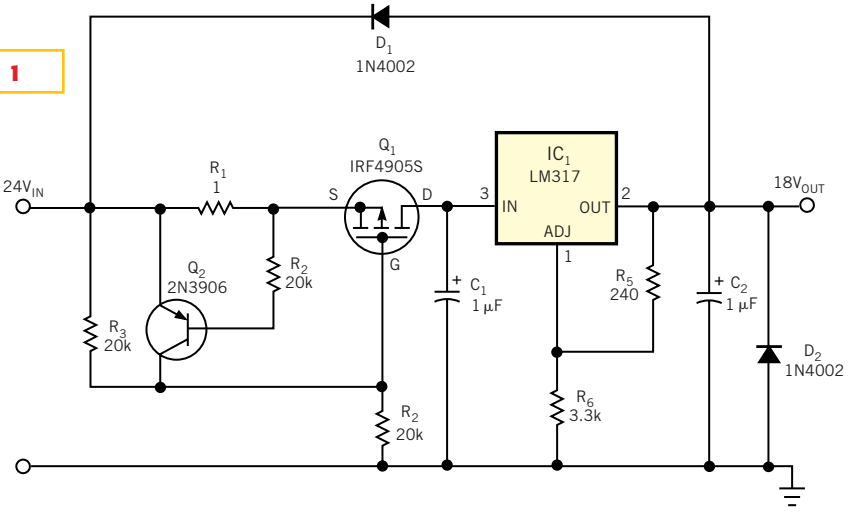


Figure 1

A few added components extend this linear regulator's overcurrent protection.

Digitally programmable resistor serves as test load

Francesc Casanellas, Aiguafreda, Spain

FIGURE 1 ILLUSTRATES a digitally programmable precision resistance that can serve as a microprocessor-driven power-supply load in custom-designed ATE (automatic-test equipment). An 8-bit current-output DAC, IC_1, a DAC08, drives current-to-voltage converter IC_{2A}, which in turn drives the gate of power MOSFET Q_1. The device under test connects to J_1 and J_2. In operation, current from the device under test develops a voltage across sampling resistors R_{8A} and R_{8B}. Amplifier IC_{2B} drives IC_1's reference input and closes the feedback path. Transistor Q_2 provides overcurrent protection by diverting gate drive from Q_1 when the voltage drop across R_{8A} and R_{8B} reaches Q_2's $V_{BE(ON)}$. V_O and I_O represent the output voltage and current, respectively; N represents the decimal equivalent of the binary input applied to IC_1; and A represents the gain of the amplifier stage IC_{2B}. R_1 comprises the parallel combination of R_{1A} and R_{1B}. **Equation 1** describes the circuit's load current:

$$\frac{V_0}{R_1} = I_{OUT} = \frac{V_I}{R_6} \times \frac{N}{256} = \frac{I_0 \times R_8 \times A}{R_6} \times \frac{N}{256}. \quad (1)$$

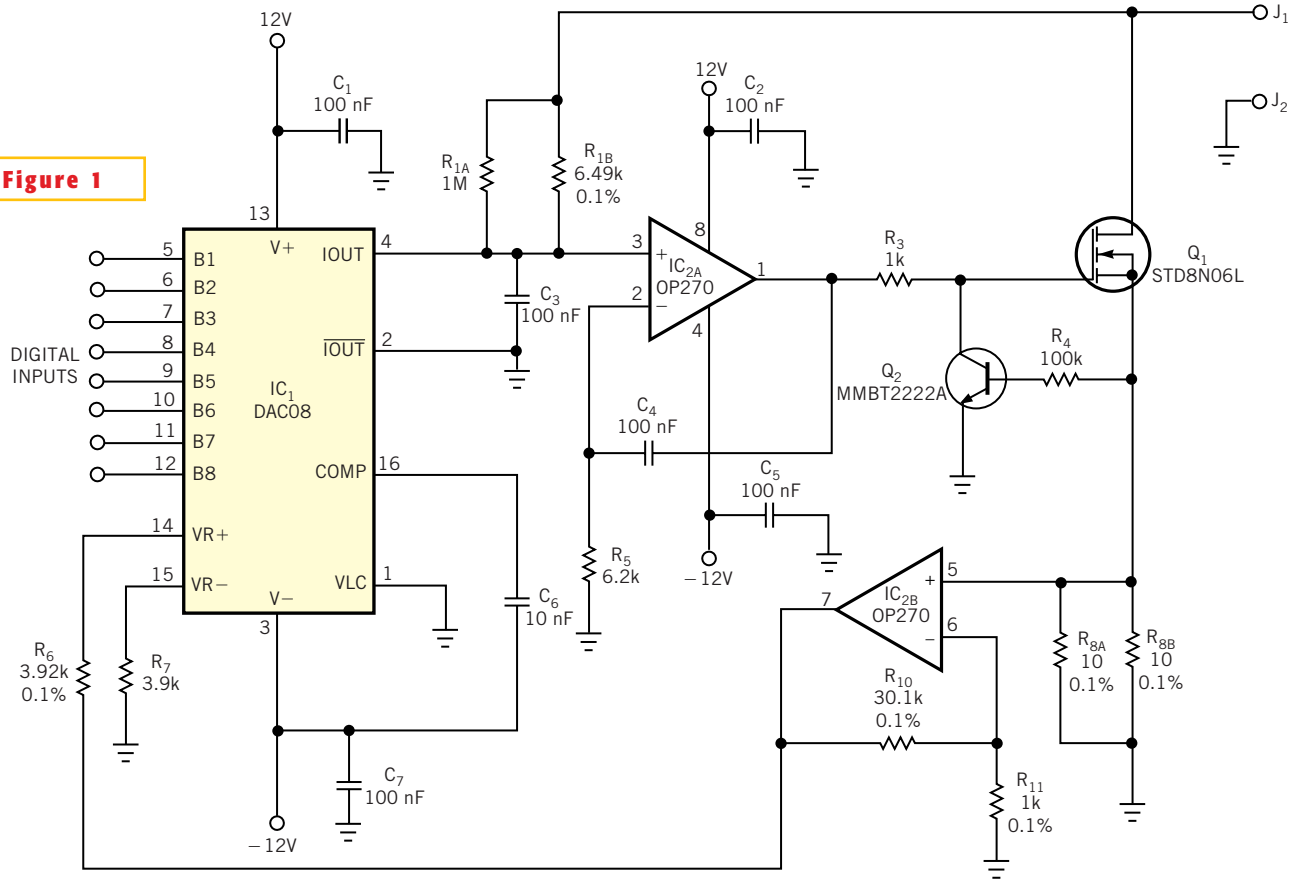
Solving **Equation 2** yields the circuit's output resistance:

$$\frac{V_0}{I_0} = \frac{A \times R_8}{R_6} \times \frac{N}{256}. \quad (2)$$

Using the component values shown, the circuit's equivalent resistance ranges from approximately 5.5Ω for N=0, an all-zero binary input, to 255Ω for N=255, an all-one binary input.

You can modify circuit values to cover other resistance ranges. Replacing the 8-bit DAC08 with a 10-bit D/A converter increases resistance resolution. To increase the circuit's power-handling capability, replace Q_1 with a higher power MOSFET and an appropriately sized heat dissipator. Capacitors C_3 and C_4 control the circuit's bandwidth.□

Figure 1



This digitally programmable resistor features low component count and inexpensive parts.

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Edited by Brad Thompson

Power up a microcontroller with pre-power-down data

Stephan Roche, Santa Rosa, CA

It is sometimes necessary to retrieve data at power-up in the same way that they were at the last power-down, so that the product wakes up in the state it had before shutdown or to retrieve some measurement. One approach is to save critical variables into EEPROM or flash memory as soon as they change. This approach is generally not a good idea, because flash is typically limited to 100,000 write cycles, and EEPROM is typically limited to 1 million cycles. These numbers may seem large, but a product can easily reach them during their lifetimes.

Another approach is to use a battery to keep the microcontroller supplied so that it doesn't lose its RAM contents. This Design Idea presents an alternative option: detecting a power-down and triggering an interrupt routine that saves all the parameters in EEPROM or flash before the microcontroller supply falls below the operating threshold. **Figure 1** implements such an approach for a PIC18F6720 microcontroller.

One of the many features of this microcontroller is its low-voltage detection, which can trigger an interrupt when its LVD input goes below a threshold. You can set the threshold at 2.06V to 4.64V.

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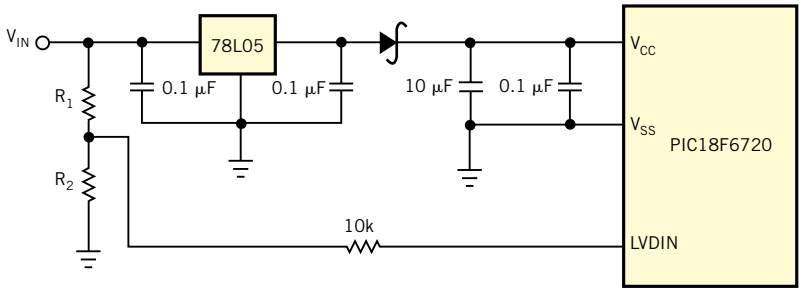


Figure 1 Use a power-down-detection scheme with a PIC18F6720 to save data before the microcontroller ceases to function.

The PIC18 microcomputer ceases functioning when its voltage supply is less than 4.2V. Because the EEPROM/flash-saving cycle is fairly time-consuming, the tactic is to monitor the voltage at the input of the 5V regulator to detect the power drop even before the microcomputer's supply starts to drop.

Select the LVD trip point inside the PIC18F6720 to be 1.22V, and calculate the required value of R_2/R_1 with the following equation:

$$\frac{R_1}{R_2} = \frac{V_{IN\_THRESHOLD}}{1.22} - 1,$$

where $V_{IN\_THRESHOLD}$ is the trip point below which a "data-save" function triggers. You should select this trip point to be as high as possible but not too high to avoid triggering on the ripples and noise on V_{IN-}.

Figure 2 shows the V_{IN} and V_{CC} waveforms when a power-down occurs. The ΔT represents the time allowed for saving data, which starts when the circuit detects the drop of V_{IN} and finishes when the voltage on the microcontroller goes below 4.2V, at which point it ceases to function. If the same 5V supply powers other devices , add a Schottky diode in series to ensure sufficient energy storage for the microcontroller to save the data. **Listing 1** in the Web version of this article at www.edn.com contains the assembly code that saves the data when a power-down occurs and retrieves the saved data at power-up.□

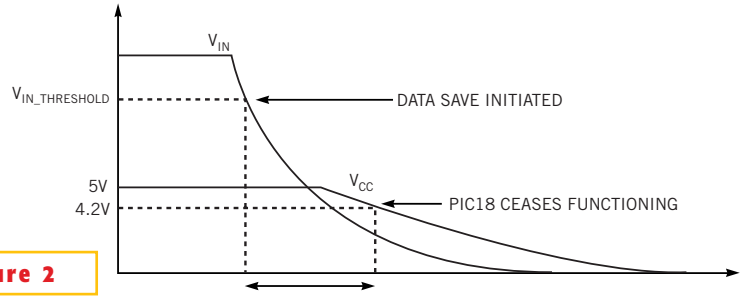


Figure 2 The V_{CC} and V_{IN} waveforms at power-down indicate the relationships in the sequence of events.

Power MOSFET is core of regulated-dc electronic load

Ausias Garrigós and José M Blanes, University Miguel Hernández, Electronic Technology Division, Elche, Spain

Designers use electronic dc loads for testing power supplies and sources, such as solar arrays or batteries, but commercial ones are often expensive. By using a power MOSFET in its linear region, you can build your own (**Figure 1**). It uses two simple feedback loops to allow the transistors to work as a current drain in current-regulation mode or as a voltage source in voltage-regulation mode. Designers use current-regulation mode when they are characterizing voltage sources, in which the power source must deliver current value that is set in the electronic load. They use voltage-regulation mode with current sources because it forces the sources to operate at a voltage that the load sets.

In current mode, R_{SHUNT} senses I_{LOAD}, and the resultant voltage feeds back to the inverting input of op amp IC_{1A}. Because the dc gain of this amplifier is high in the linear-feedback operating range, the inverting input stays equal to the

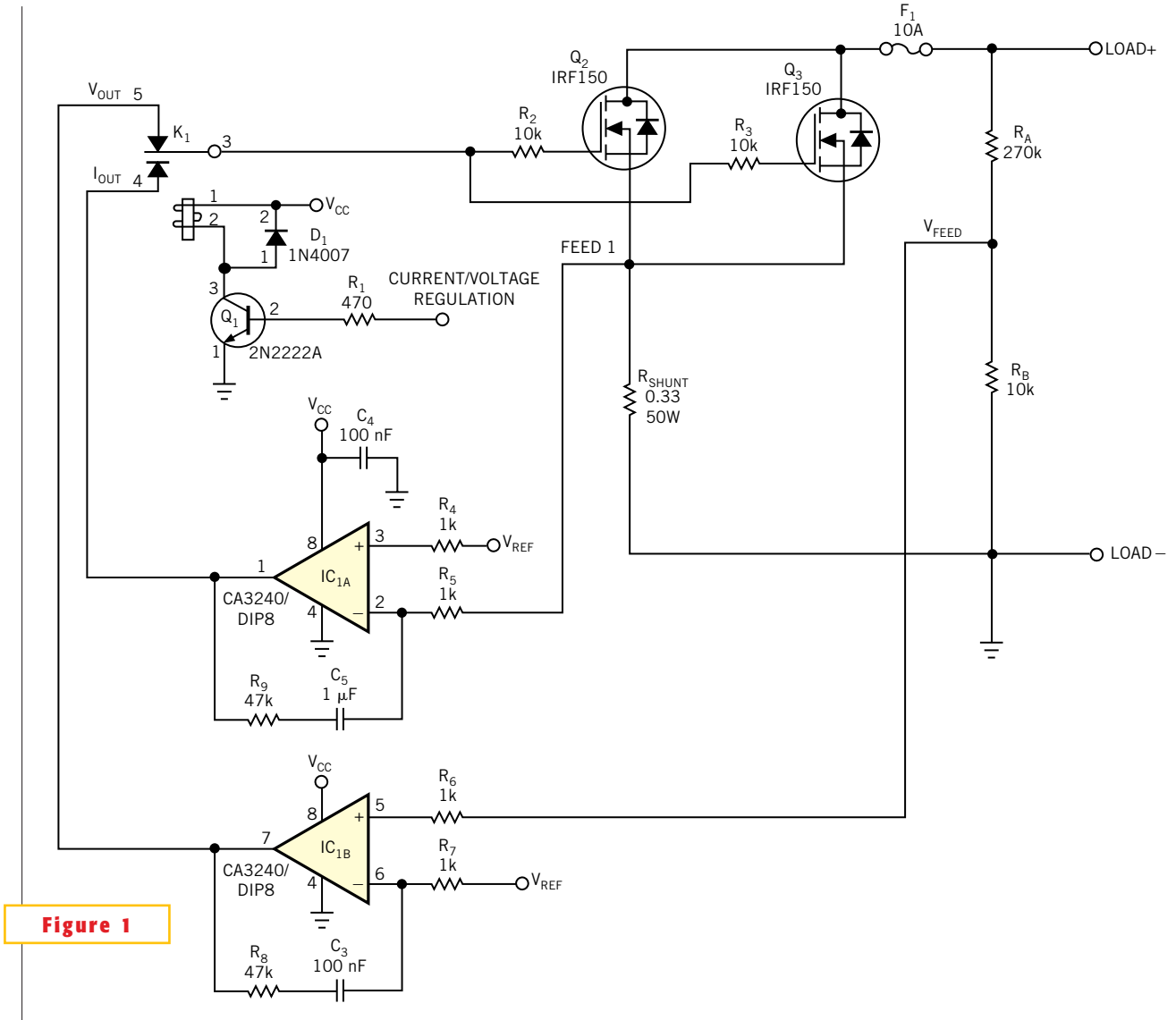


Figure 1

Using MOSFETs and a relay, this electronic load can operate in both current- and voltage-regulation modes.

noninverting input, which corresponds to V_{IREF}. The amplifier establishes its output value to operate MOSFETs Q_2 and Q_3 in a linear region and, therefore, dissipate the power from the source. The value of the source current is proportional to the current-loop reference, V_{IREF}, and is $I_{LOAD}=V_{IREF}/R_{SHUNT}$. Set V_{IREF} using a resistive voltage divider connected to a stable reference, or use the output of a D/A converter from a PC-based I/O card for flexible configuration.

Voltage-operating mode is similar, but now the sensed variable is the output voltage, which voltage divider R_A/R_B attenuates, so that the electronic load can operate at higher voltages than the op-amp supply voltage. The sensed voltage feeds back to the noninverting input of IC_{1B}, and the MOSFETs again operate in the linear region. Load voltage $V_{LOAD}=V_{VREF}\times(R_A+R_B)/R_B$.

The dual-op-amp CA3240, IC_1, can operate with an input voltage below its negative supply rail, which is useful for single-supply operation, but you can use any op amp if you have a symmetrical supply. Relay K_1 switches operating mode through a digital control line driving Q_1. The MOSFET is critical; you can add the IRF150 devices this design uses in parallel to increase the current-handling capabilities due to their positive-temperature coefficient, which equalizes the current flowing in the parallel MOSFETs. With the two MOSFETs in the circuit, the load handles 10A, and power consumption is greater than 100W, so using a heat sink and small fan is a good idea.

This circuit is useful for characterizing photovoltaic modules, which have two source modes. With this circuit and a PC-based setup, the I-V characteristic of a photovoltaic module from Helios Technology (www.heliostechnology.com) shows a region above V_{MPP} (voltage in the maximum point), at which a sharp transition corresponds to a voltage source (**Figure 2**). At voltages below V_{MPP}, the photovoltaic modules look like a current source. It is normally difficult to characterize this flat region of the curve with a simple current-mode electronic load, because the voltage output is sensitive to small variations in current, and thus a constant-voltage mode load is a better choice.□

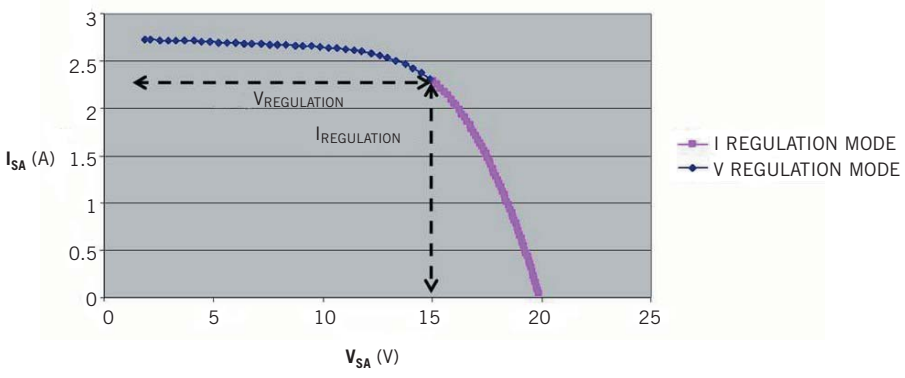


Figure 2 The I-V characteristics of a photovoltaic module, using the electronic load, show the special attributes of these power sources.

Use PSpice to model distributed-gap cores

Jeff Fries, GE Transportation Systems Global Signaling, Grain Valley, MO

PSpice software lets you create magnetic-core models that simulate nonlinear magnetic devices (**Figure 1**). These simulations are useful for observing hard-to-measure magnetic parameters such as core flux density, especially when you cannot quickly procure a sample device. The required inputs to the PSpice magnetic-core model are initial permeability of the core material, data points from the B-H magnetization curve, and the physical properties of the core, such as magnetic-path length, cross-sectional area, and air-gap length.

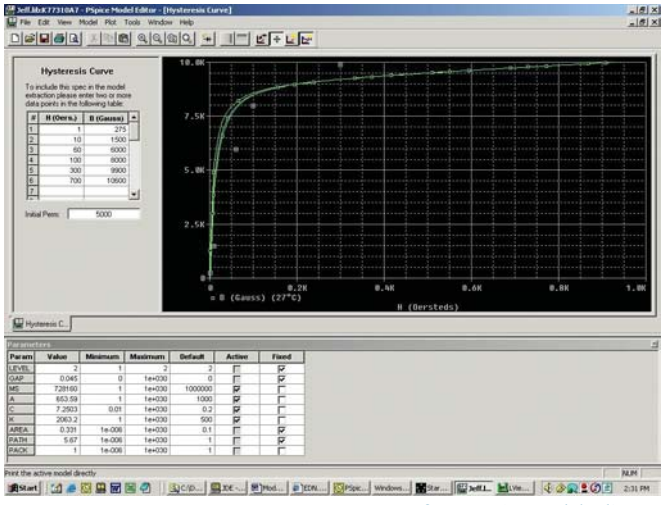


Figure 1 You use a screen capture from PSpice Model Editor to create a magnetic-core model.

All of the needed inputs for the magnetic-core model are typically available from core manufacturers' data sheets. However, in the case of a distributed gap with powder cores such as MPP or KoolMu, you need to determine the equivalent air gap to model the core using PSpice, because it relies on the air-gap length as input data to the model. Using the conservation of flux and manipulating Ampere's Law for a magnetic

circuit with an air gap result in: $1/U_E=(1/U_I)+(L_G/L_E)$, where U_E is the effective permeability of the core, U_I is the initial permeability of the core material, L_G is the length of the gap in centimeters, and L_E is the magnetic-path length of the core in centimeters. Assuming that the initial permeability, U_I, of the core is high, which is typical of distributed-gap cores, then the term $1/U_I$ drops out, and you can rearrange the equation to solve for the gap length as $L_G=L_E/U_E$. Using the magnetic-path length, L_E, and effective permeability, U_E, that the core manufacturer's data sheet specifies, calculate the equivalent air-gap length of the distributed gap-core for use in the PSpice model.

As an example, take the KoolMu 77310-A7 toroidal powder core from Magnetics Inc (www.mag-inc.com). Because the data sheet does not specify the initial permeability of the KoolMu core, arbitrarily use 5000. (This parameter is insignificant in the model due to the air gap.) Use the magnetization curve for the KoolMu material and mark the data points in **Table 1**.

Physical data for the 77310-A7 core shows a magnetic path length of 5.67 cm, cross-sectional area of 0.331 cm^2, and effective permeability of 125. From this data, you calculate the effective air-gap length of 0.045 cm. Enter this data into PSpice for the core model.

A quick and easy way to verify the accuracy of the model is to create an inductor in PSpice using your magnetic-core model. Place the inductor in a series-tuned RLC circuit (**Figure 2**). Using PSpice, run an ac sweep of the circuit, and use a probe to find the resonant frequency, f_{RES}. Using the resonant frequency, you can calculate the measured inductance of the PSpice model as $L_{MEAS}=1/(4\times\pi 2\times f_{RES}2\times C)$. If your magnetic-core model is correct, this should be close to the expected inductance calculated as $L_{EXP}=(N^2)\times A_L$, where N is the number of turns, and the core data sheet typically supplies the inductance factor, A_L.□

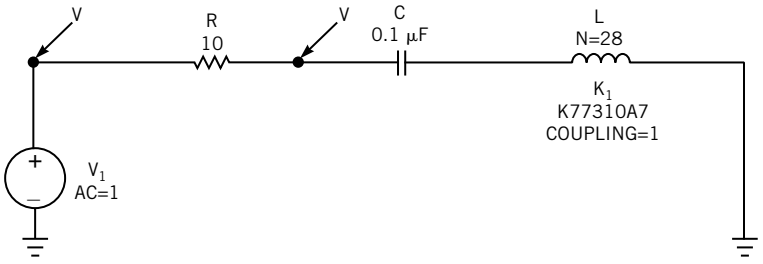


Figure 2 You can use this RLC-resonant circuit to measure the modeled inductance in PSpice, using an ac sweep analysis.

TABLE 1–DATA POINTS FOR KOOLMU CORE

B (Gauss)	H (Oersteds)
275	1
1500	10
6000	60
8000	100
9900	300
10,600	700

Precision divide-by-two analog attenuator needs no external components

Moshe Gerstanhaber and Chau Tran, Analog Devices, Wilmington, MA

Many modern A/D converters offer only a 5V input range, and using these converters with a ±5V or larger input signal gives the designer a problem: how to discard half of a good analog signal without introducing errors and distortion. To solve the problem, you can use an attenuator comprising two operational amplifiers and two resistors (**Figure 1**). However, this approach can reduce a system's performance by introducing gain errors due to amplifier offset and drift and resistor mismatch.

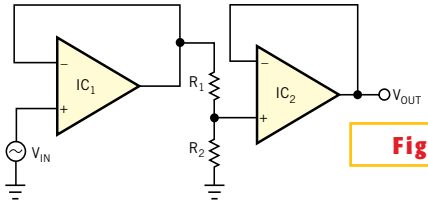


Figure 1 A conventional active voltage divider requires two op amps, IC_1 and IC_2, and two resistors, R_1 and R_2, that form a 2-to-1 voltage divider.

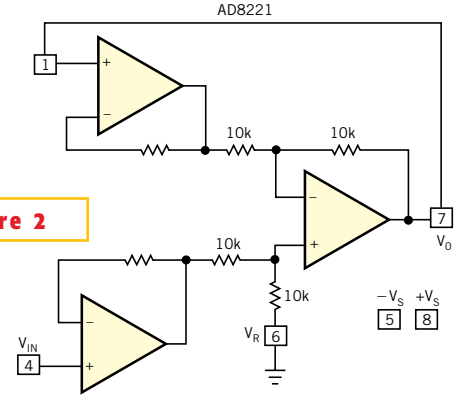


Figure 2 You can use an instrumentation amplifier to halve an analog signal's amplitude. All resistors are internal to the IC.

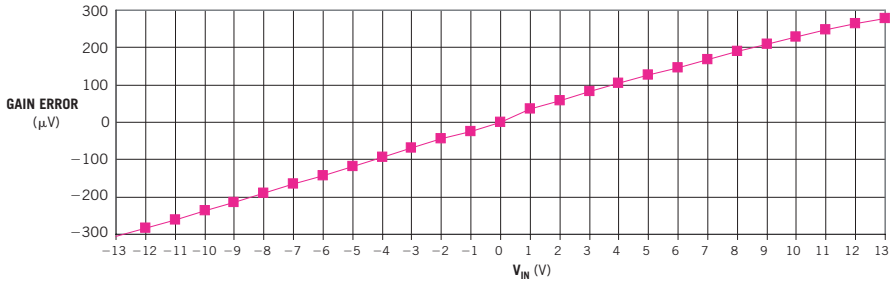
Figure 2 shows an alternative circuit that provides a precision gain of one-half with low offset, low drift, and low input-bias currents and that uses an AD8221 instrumentation amplifier.

The amplifier's output, V_O, equals the difference between the two inputs, V_{IN+} and V_{IN-}: $V_O=(V_{IN+})-(V_{IN-})$. Connecting the amplifier's output to its inverting input and substituting V_O for V_{IN-} yields: $V_O=(V_{IN+})-(V_O)$, or $V_O=(V_{IN+})$.

Thus, the circuit provides a precision gain of one-half with no external components and, in this configuration, is unconditionally stable. The performance plots of **figures 3** and **4**, respectively, show a gain error of less than 300 µV and a maximum nonlinearity error of about 1 ppm over a 26V input-voltage range.

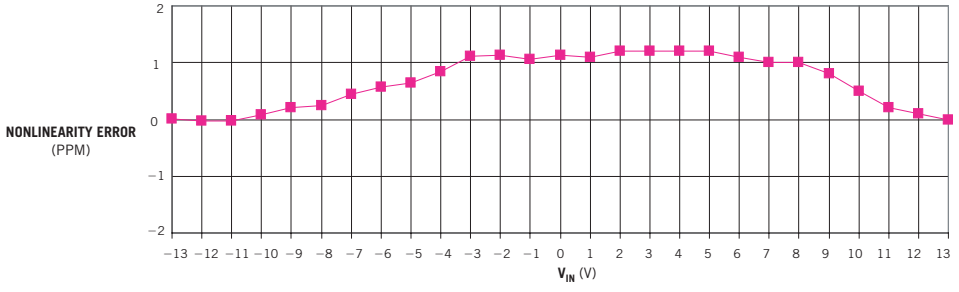
To introduce an offset voltage, V_{OS}, that equals half of a reference voltage ($V_{OS}=V_R/2$), connect the AD8221's reference input (Pin 6) to voltage V_R. To bias the attenuator's output at half of the positive- or negative-power-supply voltage, connect the reference pin to the appropriate power supply.□

Figure 3



The circuit in Figure 2 introduces a full-scale gain error of less than 300 µV over a 26V input-voltage range.

Figure 4



The circuit in Figure 2 introduces a maximum nonlinearity error of about 1 ppm over a 26V input-voltage range.

Quartz crystal-based remote thermometer features direct Celsius readout

Jim Williams and Mark Thoren, Linear Technology Corp

Although quartz crystals have served as temperature sensors, designers haven't taken advantage of the technology because few manufacturers offer the sensors as standard products (**references 1** and **2**). In contrast to conventional resistance- or semiconductor-based sensors, a quartz-based sensor provides inherently digital-signal conditioning, good stability, and a direct digital output that's immune to noise and thus ideally suited to remote-sensor placement (**Figure 1**, pg 100).

An economical and commercially available quartz temperature sensor, Y_1 and IC_1, an LTC-485 RS485 transceiver in transmitter mode, form a Pierce crystal oscillator. The sensor, an Epson HTS-206, presents a nominal frequency of 40 kHz at 25°C and a temperature coefficient of −29.6/ppm/°C (**Reference 3**). The transceiver's differential-line-driver outputs deliver a frequency-coded temperature signal over a twisted-pair cable at distances as far as 1000 ft.

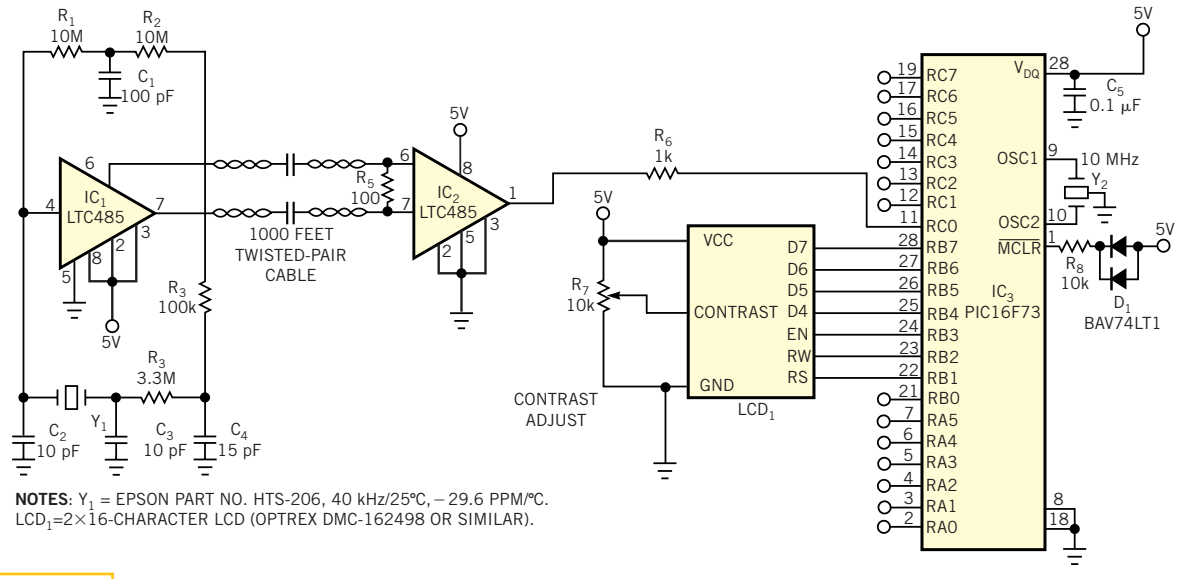
A second LTC-485, IC_2, in receiving mode, accepts the differential data and presents a single-ended output to IC_3, a PIC-16F73 processor that converts the frequency-coded temperature data and presents the temperature in Celsius format on LCD_1. You can view and download the conversion program's source code in the Web version of this Design Idea at www.edn.com.□

References

1. Benjamin, Albert, "The Linear Quartz Thermometer—A New Tool for Measuring Absolute and Differential Temperature," *Hewlett-Packard Journal*, March 1965.

2. Williams, Jim, "Practical Circuitry for Measurement and Control Problems," Application Note 61, August 1994, Linear Technology Corp.

3. HTS-206 specifications, Epson Corp, www.eea.epson.com.



NOTES: Y_1 = EPSON PART NO. HTS-206, 40 kHz/25°C, –29.6 PPM/°C.
LCD_1=2×16-CHARACTER LCD (OPTREX DMC-162498 OR SIMILAR).

Figure 1 A quartz-crystal temperature sensor provides Celsius-temperature readouts accurate to 2% over a −40 to +85°C range.

design ideas

Edited by Brad Thompson

Single-wire keypad interface frees microcontroller-I/O pins

Israel Schleicher, Prescott Valley, AZ

In most keypads, pressing a key closes a contact that bridges two lines in an xy matrix. If you use a microcontroller to detect a key closure, checking the states of (x+y) lines requires an equal number of I/O pins. Occupying only one free I/O pin, the circuit **Figure 1** communicates with a microcontroller by generating a single pulse each time someone presses a key. The pulse's width is proportional to the number of the pressed key, and the microcontroller identifies the pressed key by measuring the pulse's width.

IC_2, a CMOS LMC555 version of the popular 555 timer, operates as a monostable one-shot multivibrator. In the circuit's resting state, a transistor internal to IC_2 at Pin 7 shunts C_6, and IC_2's output at Pin 3 remains at logic low. Pressing any key on the keypad connects two resistors from two groups—R_1 and R_2 in one

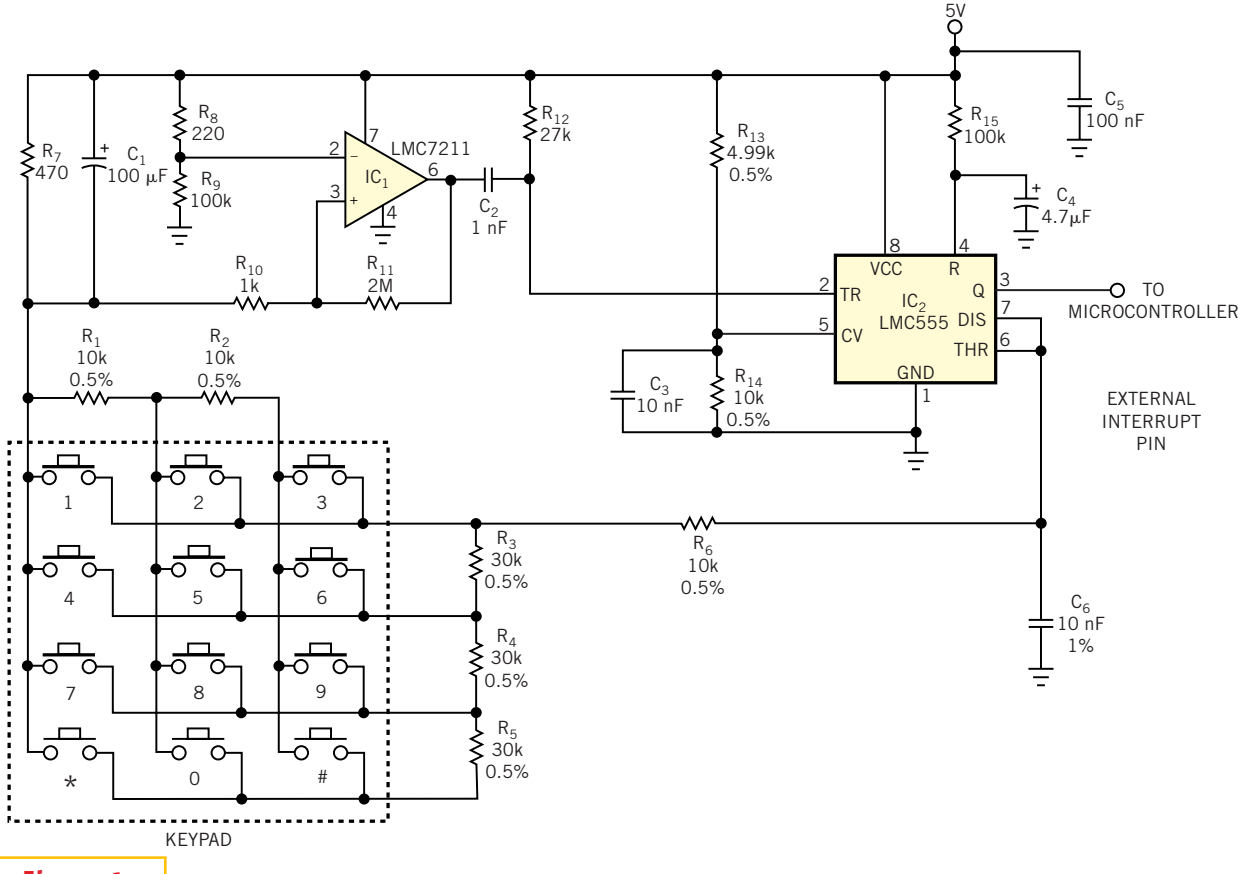


Figure 1 Two ICs form a pulse-width-modulated keypad interface that uses only one microcontroller-input pin.

group and R_3, R_4, and R_5 in the other—in series with R_6. The sum of the two resistors varies in 10-kΩ increments, and the total resistance is proportional to the number of the pressed key.

Pressing any key draws current through R_6, R_7, and the selected keypad resistors and raises the voltage at IC_2's Pin 7. After C_1 charges, introducing a short delay that's sufficient to eliminate keypad-switch contact-closure bounce, CMOS comparator IC_1 detects the small voltage drop established across R_7. The output of IC_1 (Pin 6) goes from 5 to 0V, which in turn triggers Pin 2 of IC_2. Timer IC_2's output (Pin 3) goes high and begins to charge capacitor C_6 at a time constant that depends on the selected key. When the voltage across C_6 reaches two-thirds of V_{CC}, or 3.333V, Pin 3 goes low and discharges C_6. The following equation calculates IC_2's output pulse width, T: $T = 1.1 \times R_S \times C_6$, where R_S equals the sum of the selected keypad resistors and ranges from 10 to 120 kΩ. The pulse width spans a range of 110 to 1320 μsec in increments of 110 μsec.

The smallest relative change in pulse width occurs at the longest pulse ratio, 110/1320, or 8.33%. This ratio provides sufficient margin to allow use of standard ±1% tolerance or better components for those in **Figure 1** that are ±0.5 and ±1%. Resistors R_{13} and R_{14} compensate for variations in IC_2's internal voltage dividers by forcing the voltage at Pin 5 to two-thirds of power-supply voltage V_{CC}.

The keypad circuit's output pulse drives the external interrupt input, RA_2, of a Microchip 16F630 microcontroller. **Listing 1**, available at the online version of this Design Idea at www.edn.com, presents an interrupt routine for the 16F630 that measures the pulse width, verifies that its tolerance is within ±40 μsec, and returns a numerical value of 1 to 12 that corresponds to the pressed key. As a safeguard against erroneous data, the routine returns an error code if the pulse width falls outside certain limits.□

Calculator program evaluates elliptic filters

Fernando Salazar-Martínez, Alan Altamirano-Cruz, and David Báez-López, Department of Engineering Electronics, University of the Americas, Puebla, Mexico

Many designers consider the elliptic-transfer function to be the most useful of all analog-filtering functions, because of its steep roll-off at the band edges. You can use a Texas Instruments model V200 Voyage programmable calculator and the program in **Listing 1** at the Web version of this Design Idea at www.edn.com to evaluate a lowpass elliptic filter by finding its characteristic's poles and zeros. To do so, this program implements Darlington's algorithm (**Reference 1**). The program accepts as input the filter's maximum passband-attenuation ripple in decibels, its stopband and passband frequencies in radians per second, and its order, or number of poles (**Figure 1**).

As an example, calculate the zeros, poles, and stopband attenuation of an elliptic, fifth-order, analog lowpass filter with maximum gain of 0.1 dB and stopband frequency of 1.05 radians/sec. **Figure 2** illustrates the calculator's display screens during program execution.□

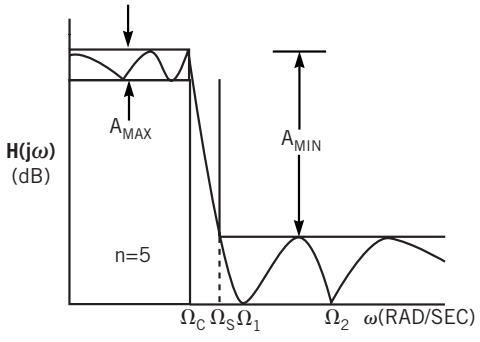


Figure 1 The characteristics of an elliptic filter's amplitude response include in-band ripple, passband-attenuation and stopband frequencies, and stopband attenuation.

Figure 2 These screens show the calculator's display from the introductory menu (a), entering filter parameters (b), calculating values for filter-response zeros (c), calculating value for out-of-band attenuation (d), and calculating values for filter-response poles (e).

Reference

1. Darlington, Sidney, "Simple Algorithms for Elliptic filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Volume CAS-25, No. 12, December 1978, pg 975.

Dynamic-load circuit determines a battery's internal resistance

Jim Williams, Linear Technology Corp, Milpitas, CA

THE SIMPLEST MODEL of a battery comprises an ideal voltage source that connects in series with a resistance whose value—often a few milliohms—depends on the battery's electrochemical condition and construction. If you attempt to use an ordinary ac milliohmmeter containing a kilohertz-range ac excitation source to measure a battery's internal resistance, you get erroneous results due to capacitive effects, which introduce losses. A more realistic battery model includes a resistive divider that a capacitor partially shunts (**Figure 1**). In addition, a battery's no-load internal resistances may differ significantly from their values under a full load. Thus, for greatest accuracy, you must measure internal resistance under full load at or near dc.

The circuit in **Figure 2** meets these requirements and accurately measures internal resistance over a range of 0.001 to 1Ω at battery voltages as high as 13V. One section of an LTC6943 analog switch, IC_{2A}, alternately applies 0.110 and 0.010V derived from 2.5V voltage reference IC_3 and resistive divider R_2, R_3, and R_4 to IC_1's input.

Amplifier IC_1, power MOSFET Q_1, and associated components form a closed-loop current sink that provides an active load for the battery under test via Q_1's drain. Diode D_1 provides reversed-bat-

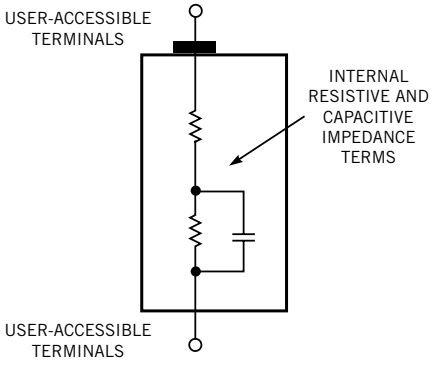


Figure 1 An elementary model of a battery's internal impedance includes resistive and capacitive elements, but the capacitive elements introduce errors in ac-based impedance measurements. For improved accuracy, analyze the battery's voltage drop at a frequency near dc.

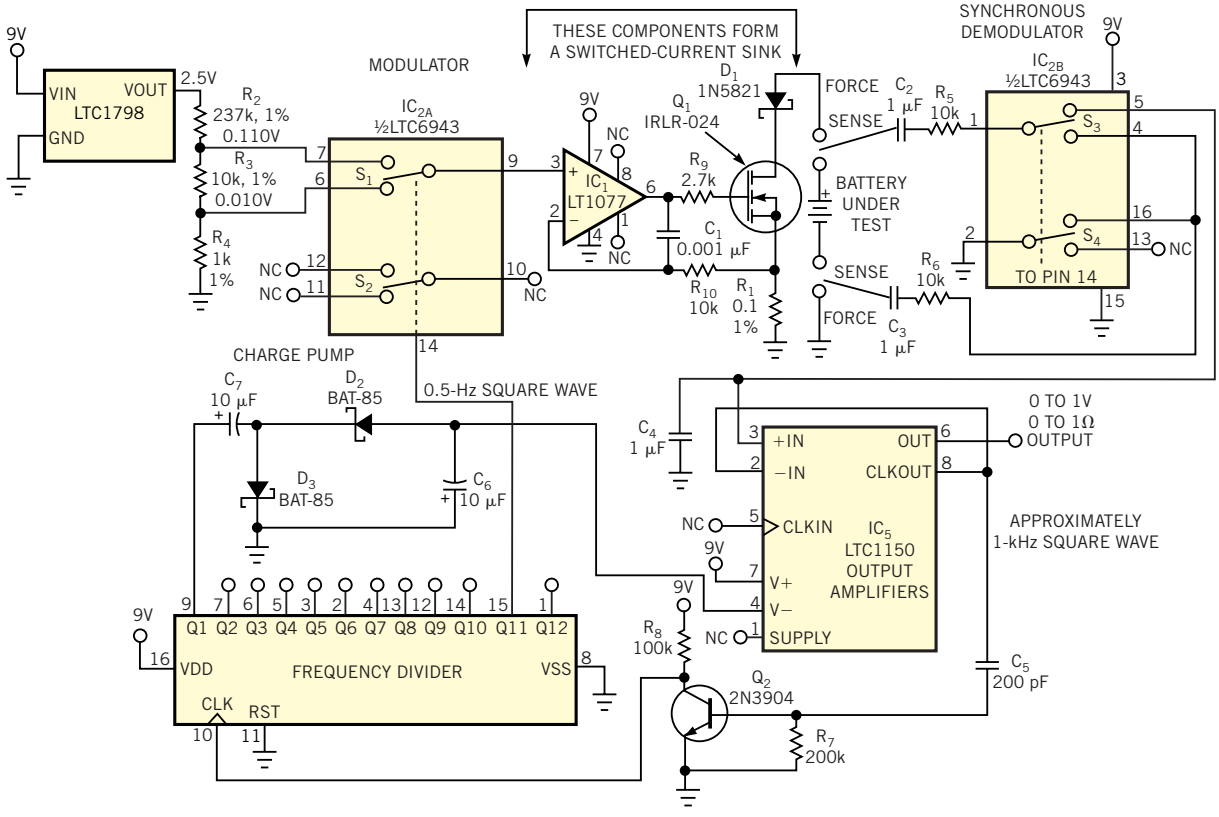


Figure 2 This circuit determines a battery's internal resistance by repetitively applying a calibrated discharge current and measuring the resultant voltage drop across the battery's terminals.

tery protection. The voltage at amplifier IC_1's positive input and the voltage drop across R_1 determine the load applied to the battery. In operation, the circuit applies a constant-current load comprising a 1A, 0.5-Hz square wave biased at 100 mA to the battery.

The battery's internal resistance develops a 0.5-Hz amplitude-modulated square-wave signal at the Kelvin connections attached to the battery. A synchronous demodulator comprising analog switches S_2 and S_3 in IC_{2B} and chopper-stabilized amplifier IC_5 processes the sensed signal and delivers a 0 to 1V analog output that corresponds to a battery-resistance range of 0 to 1Ω.

Via transistor Q_2, amplifier IC_5's internal approximately 1-kHz clock drives CMOS binary divider CD4040, IC_4, which supplies a 0.5-Hz square-wave clock drive for the switches in IC_2. In addition, a 500-Hz output from IC_4 powers a charge-pump circuit that delivers approximately −7V to IC_5's negative power-supply input and thus enables IC_5's output to swing to 0V.

The complete circuit consumes approximately 230 µA, allowing nearly 3000 hours of operation from a 9V alkaline-battery power supply. The circuit operates at a supply voltage as low as 4V with less than 1-mV output variation and provides an output accuracy of 3%. The circuit accommodates a battery-under-test voltage range of 0.9 to 13V, but you can easily alter discharge current and repetition rate to observe battery resistance under a variety of conditions.□

Battery automatic power-off has simpler design

Yongping Xia, Navcom Technology, Torrance, CA

A previous Design Idea describes a simple way to automatically turn off a battery after a preset on period to save battery life (**Reference 1**). This Design Idea presents a simpler way to perform the same function (**Figure 1**). Two gates of IC_1, a quad two-input NAND Schmitt trigger, form a modified flip-flop. When you apply a 9V battery to the circuitry, the output of IC_{1A} goes high because the initial voltage on C_1 is zero. The output of IC_{1B} is low, which feeds back to IC_{1A} through R_2. C_3 charges up through R_3. The output of IC_{1C} goes high because R_6 is connects to ground. A P-channel MOSFET switch, Q_1, is off, and the output IC_{1D} goes high, which in turn charges C_4 through R_2.

When you push momentary switch S_1, IC_{1A}'s output goes low because both of its inputs are high, and this output forces IC_{1B}'s output high. The value of R_2 is much smaller than R_3, so that C_3 holds a logic-level high when S_1 stays on. When S_1 goes off, C_3 discharges through R_3.

You can turn off the MOSFET switch in one of two ways. When tantalum capacitor C_2 is charged up such that the voltage on IC_{1C}'s input becomes lower than its threshold V−, IC_{1C}'s output changes from low to high; this action turns off the MOSFET switch. C_2 and R_6 determine the duration of this automat-

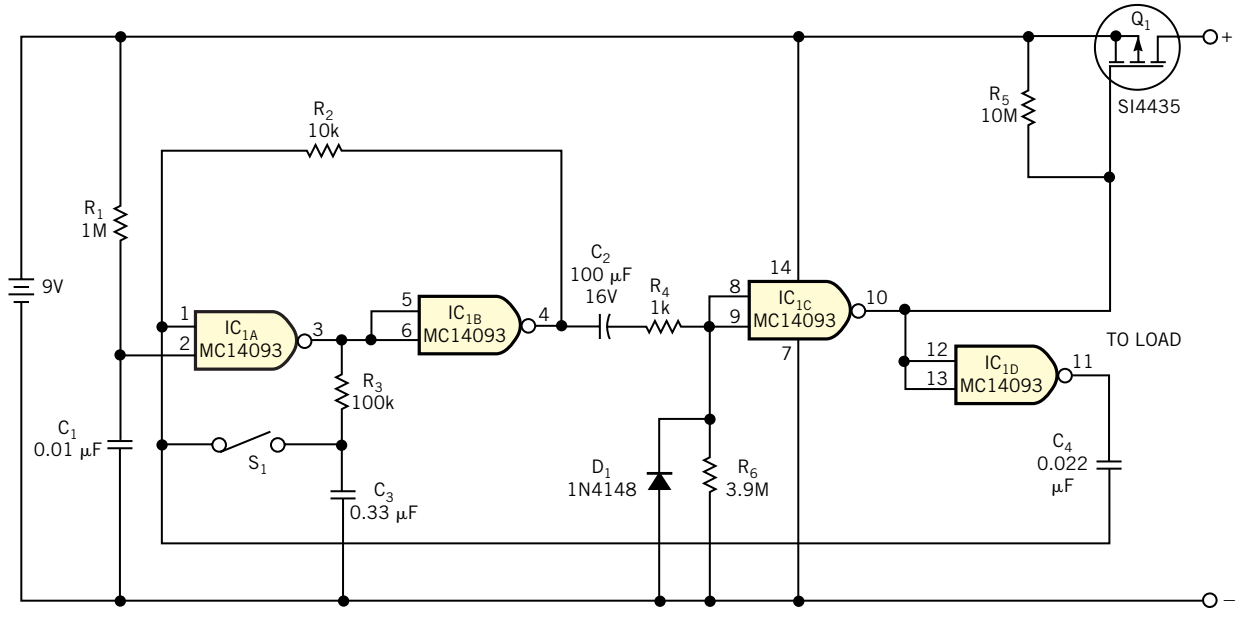


Figure 1 An improved power-off circuit automatically disconnects the battery after a preset on period.

ic turn-off. With the values shown, the turn-off takes approximately six minutes. Meanwhile, the high-to-low transition on IC_{1D}'s output forces IC_{1A} and IC_{1B} back to standby status through C_4.

Alternatively, you can manually turn off the MOSFET switch by pushing S_1. Because the voltage on C_3 is low, closing S_1 forces IC_{1A}'s outputs high and IC_{1B}'s outputs low. The high-to-low transition on IC_{1B}'s output forces IC_{1C}'s output to be high, which turns off the MOSFET. Because the value of C_2 is fairly large, D_1 provides a quick discharge route, and R_4 limits the discharge current.

This circuitry consumes less than 0.2 µA of power during standby operation. Because the MOSFET switch has a low on-resistance, it has only a 2-mV loss when the load current is 100 mA. Add an LED with a current-limiting resistor in series to the load side if you need a power-on indicator.□

Reference

1. Gimenez, Miguel, "Scheme provides automatic power-off for batteries," *EDN*, May 13, 2004, pg 92.

Control a processor's power supply in real time

Yogesh Sharma, Analog Devices, San Jose, CA

In battery-powered applications in which power management is key, a microprocessor may adjust its core voltage corresponding to an increase or a decrease in clock speed, allowing full processing power when necessary but not wasting excess power when idle. The circuit of **Figure 1** shows how an embedded processor can control its own supply voltage via a simple step-down converter and inexpensive digital potentiometer.

In this application, an embedded ADSP-BF531 Blackfin processor adjusts the wiper setting of IC_2, an AD5258 digital potentiometer, via its I^2C interface. In turn, IC_2 controls the output of IC_1, an ADP3051 current-mode, PWM step-down converter that supplies as much as 500 mA at output voltages as low as 0.8V. When its output is in regulation, IC_1's feedback input rests at 0.8V, and IC_2 and R_2 form a voltage divider.

The ADSP-BF531 imposes several design requirements: Its core power-supply voltage must maintain its accuracy to within 25 mV and offer an adjustment resolution of 50 mV per step from 0.8 to 1.2V. Also, the processor requires 1.2V at start-up to initialize its clocks. Finally, the power controller must prevent its output

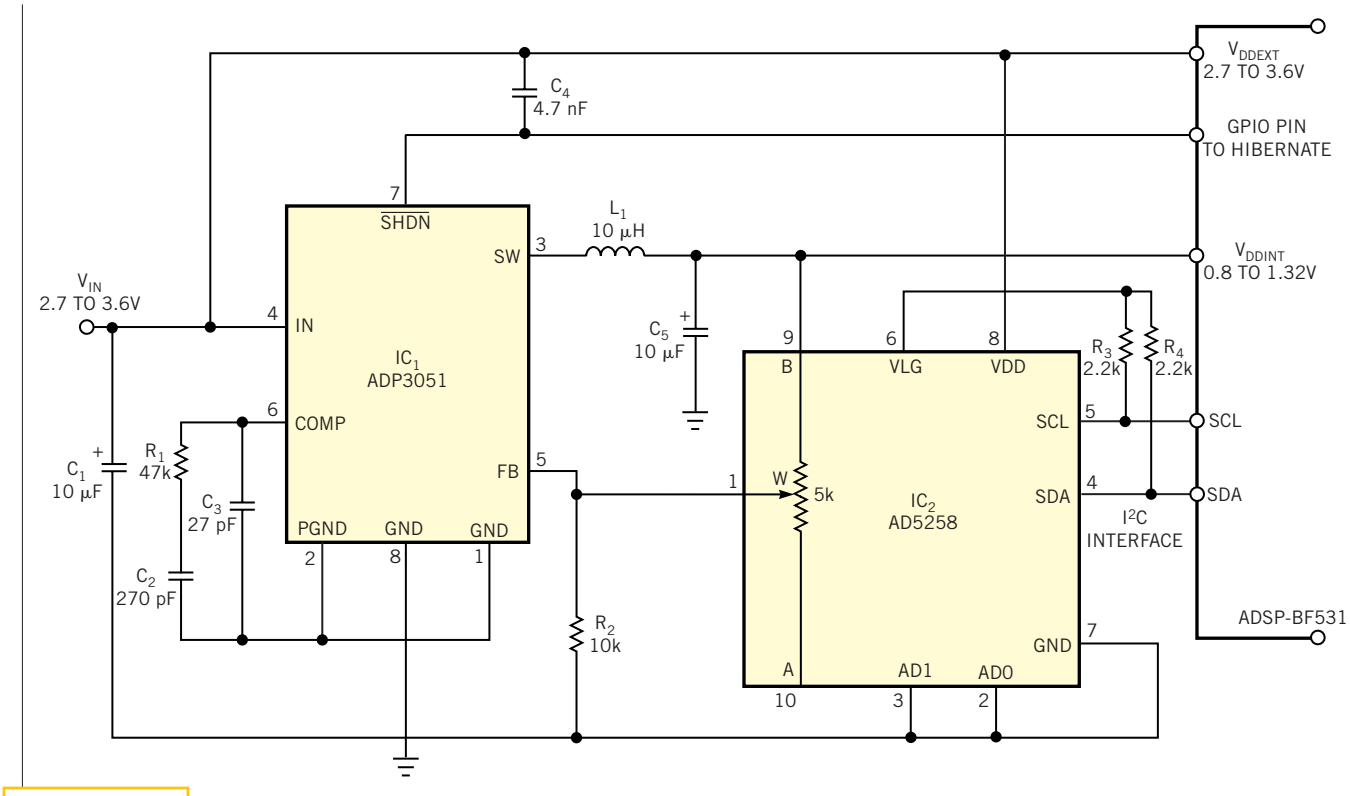


Figure 1 Under control of its host processor, digital potentiometer IC_2 adjusts the processor's core power-supply voltage.

voltage from exceeding 1.2V if a software glitch occurs.

A digital potentiometer typically presents a highly variable absolute resistance value but can accurately set its internal resistance ratio. In this design, the AD5258's internal resistor forms a voltage divider with an external resistor to set the output voltage. To improve the ADP3051's output-voltage accuracy, the ADSP-BF531 uses a simple algorithm to compute and store an appropriate maximum resistance for a given operating voltage in the AD5258's nonvolatile memory via its I^2C port.

Using the AD5258 with an external resistor provides hardware protection to prevent the output voltage from going above 1.2V. If the AD5258 is set to zero resistance, the resulting output voltage is $0.8V\times(0\Omega+10\ k\Omega)/10\ k\Omega=0.8V$. If you set it to its maximum resistance of 5 kΩ, the resulting output voltage is $0.8V\times(5\ k\Omega+10\ k\Omega)/10\ k\Omega=1.2V$. When the embedded processor directs the AD5258 via its I^2C port to ramp the core voltage from 0.8 to 1.2V, IC_1's output voltage monotonically increases within 40 µsec (**Figure 2**).□

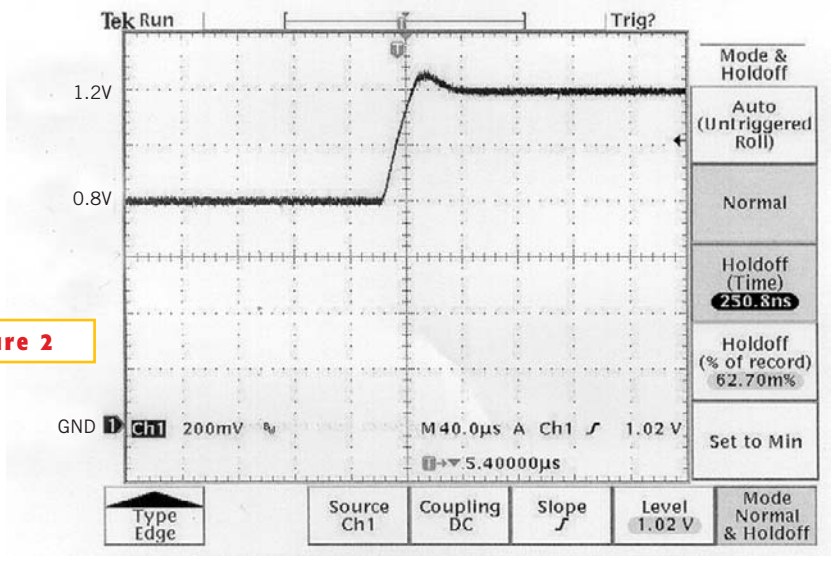


Figure 2

Applying power-supply voltage to the host processor ramps voltage from 0.8 to 1.2V with only 60-mV overshoot.

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Edited by Brad Thompson

High-side current-sensing switched-mode regulator provides constant-current LED drive

Bradley Albing, Philips Medical Systems Inc, Cleveland, OH

Many suitable circuits exist for driving LEDs in constant-current mode and from low-voltage sources. For example, **references 1**, **2**, and **3** show circuits that use switched-mode-regulator ICs and low-voltage sources to supply LED current. To produce a constant-current output using the circuit in **Reference 2**, you configure the regulator IC as a boost-mode switcher and use a resistor to sense the load current flowing in the LED string's low side, or negative-return leg. The sense resistor produces a proportional voltage that's applied to the LT1300's Sense input through a 2.5V reference diode. A voltage of 3.3V appearing at the LT1300's feedback-input terminal, Pin 4, indicates that the circuit's output is within regulation.

In applications that require a series string of LEDs to operate with its low side connected to ground, current sensing must take place in the string's high side. You can use either a rail-to-rail op amp and a handful of passive components or a dedicated current-sensing IC, such as Maxim's MAX4073T, to accomplish high-side sensing. However, adding a current-sensing IC increases circuit cost. To complicate matters, in this applica-

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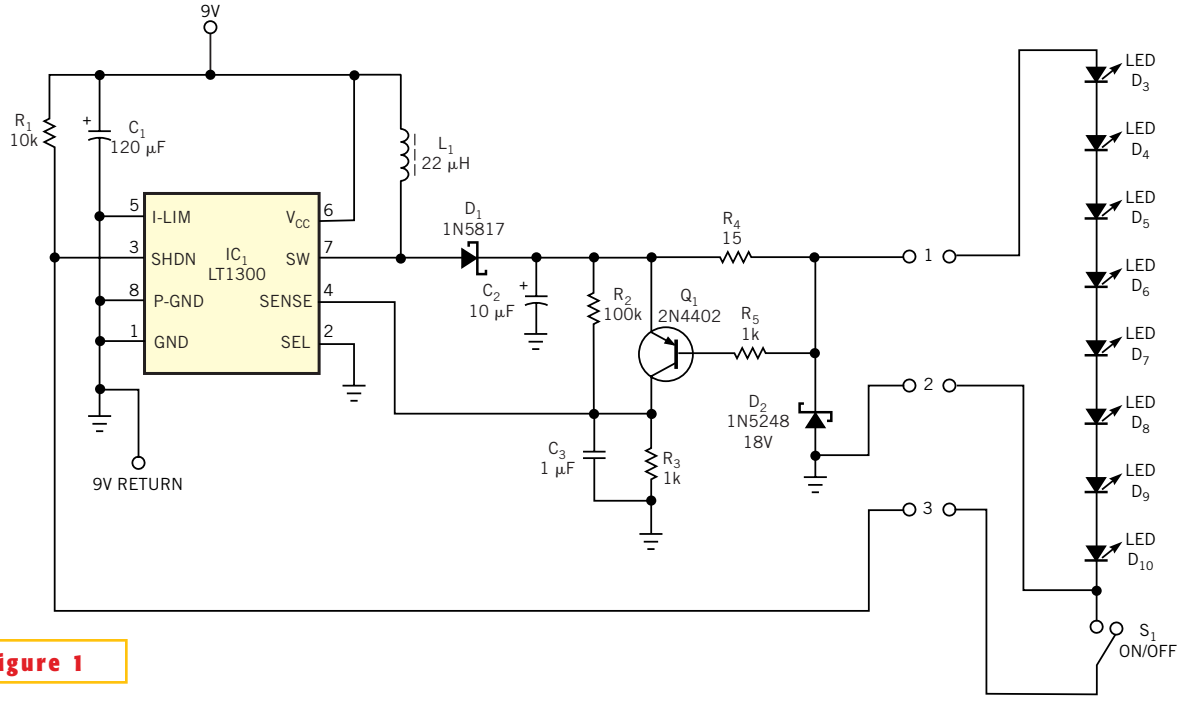


Figure 1

A single switched-mode-regulator IC drives a series-connected string of LEDs in constant-current mode.

tion, only three conductors are available to connect a remotely mounted LED string, D_3 through D_{10}, and on/off switch S_1 to the regulator circuitry.

In this Design Idea, an LT1300, IC_1, boosts 9V to drive the LED string, which presents a total forward-voltage drop of approximately 12V (**Figure 1**). Resistor R_4 serves as a current-sense resistor. At a current of approximately 40 mA, transistor Q_1 conducts and forces current through R_3, developing sufficient voltage drop to produce the requisite 3.3V at Sense Pin 4 of IC_1, bringing its output current into regulation. Zener diode D_2 limits the regulator's output voltage in case the LED string or connector opens. Switch S_1 turns on the circuit by grounding IC_1's Pin 3.□

References

1. LT1300 data sheet, Linear Technology Corp.
2. Application Note 59, Linear Technology Corp.
3. Caldwell, Steve, "1.5V battery powers white-LED driver," *EDN*, Sept 30, 2004, pg 96.

Microcontroller's DAC provides code analysis

Dave Bordui, Cypress Semiconductor, Heathrow, FL

Finding out where your microcontroller's firmware spends most of its time can be a tedious task when you use a conventional in-circuit emulator and breakpoint techniques. Other such tasks include discovering why a state machine doesn't work as you intended and where your code goes during real-time operation or during an error condition. Classic debugging methods can also become cumbersome when you attempt to observe error states or debug a program-flow problem. Fortunately, a technique that takes advantage of a feature that many microcontrollers now include offers a simple debugging aid that allows designers to easily monitor these and other operations.

The technique uses the DAC in microcontrollers such as Cypress Microsystems's PSoC (programmable-system-on-chip) family (**Figure 1**). These devices provide a microcontroller core and an array of mixed-signal building blocks that includes true DACs that can deliver fixed dc levels. Other types of DACs that deliver pulse-width-modulated outputs are unsuitable for this application. To use this technique, you create firmware "state constants" that represent operating states of your design. If your code structure comprises a state machine or contains a large "switch/case" statement, then you have already defined these constants. Otherwise, you can easily add the constants as needed.

Once you define the constants, you enable a DAC and configure it to drive one of the microcontroller's unused analog output pins. Then, you write the state constant to the DAC whenever the firmware enters a particular location. If you use an 8-bit DAC, you can also monitor the value of any 8-bit variable. Next, you connect an oscilloscope's vertical input to the DAC's output pin and observe its output voltage, which the instrument displays as a characteristic waveform that represents the firmware's operation. If your oscilloscope includes measurement cursors, you can easily determine which portion of the firmware is executing simply by measuring the DAC's dc output voltage at a given time.

You can define state constants to highlight certain conditions. For example, by reserving all state constants' values greater than 127 for error states, you can set the oscilloscope's horizontal sweep generator to trigger at a level that indicates an error. As a precaution, make sure that the microcontroller's DAC operates within its allowable update-rate range.□

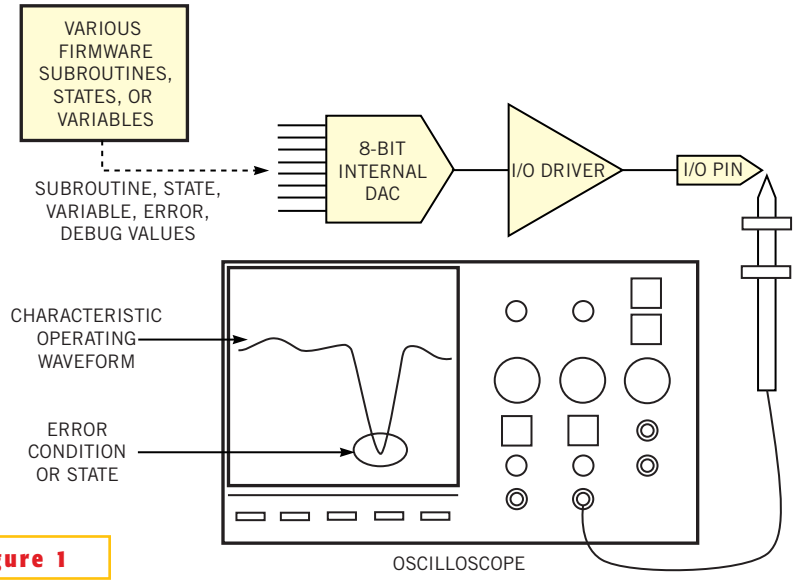


Figure 1

Put an unused internal DAC to work as a code analyzer and see where a microcontroller's routines go wrong.

Two gates and a microprocessor form digital PLL

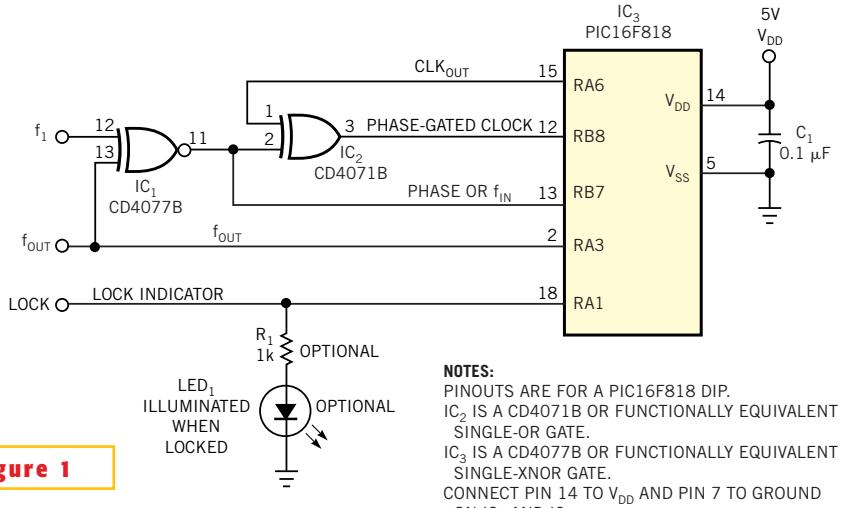
Kenneth Martin, TareTronics Inc, Corinth, MS

You can use Microchip's low-cost PIC16F818 microprocessor and a pair of gates to construct a digital PLL that can clean noisy digital signals over a range of 4 to 40 kHz. Featuring programmable lock range, phase differential, and loop gain, the digital-PLL engine and lock detector can extract clock and data information from noisy, short-range radio signals (**Figure 1**). When you construct it using a QFN-packaged microprocessor and discrete single-gate logic devices, the circuit occupies a pc-board area that's approximately as large as an aspirin.

Figure 2 is analogous to a first-order analog PLL (**Reference 1**). With its associated period register, Timer 2 functions as a DCO (digitally controlled oscillator). When Timer 2's count matches the byte in its period register, the timer generates an interrupt. The microprocessor then computes a byte of information that writes to the period register to set the duration of the next half-period. In addition, the interrupt toggles an I/O port's output to produce square-wave signal-output frequency, which drives one input of the external XNOR (exclusive-nor) gate, IC_1. The external input signal's input frequency drives the XNOR gate's remaining input to produce an output signal, which represents the phase difference, between the output and the input frequency. This XNOR-based phase detector provides good performance with noisy digital input signals.

The phase difference signal's duty cycle remains linear over a 0 to 180° range of two same-frequency signals. Applying the phase detector's output along with clock-signal clock frequency to OR gate IC_2 produces an output burst of 2-MHz clock pulses during each half-period interval of output frequency. The burst's length and the number of clock pulses it contains depend directly on the duty cycle or phase interval of the output frequency relative to the input frequency.

The circuit applies phase-difference pulses from IC_2 to the internal prescaler associated with IC_3's Timer 1, which divides them by a preset factor of one, two, four, or eight. During each of the output frequency's half-periods, Timer 1 accumulates (integrates) the prescaled pulses.



NOTES:
PINOUTS ARE FOR A PIC16F818 DIP.
IC_2 IS A CD4071B OR FUNCTIONALLY EQUIVALENT SINGLE-OR GATE.
IC_3 IS A CD4077B OR FUNCTIONALLY EQUIVALENT SINGLE-XNOR GATE.
CONNECT PIN 14 TO V_{DD} AND PIN 7 TO GROUND ON IC_1 AND IC_2.
GROUND ALL UNUSED GATE INPUTS.

Figure 1

This microcomputer-based digital-PLL circuit locks to signals over a 4- to 40-kHz range and requires a minimal number of components.

The interrupt-service-routine software for Timer 2 closes the loop and determines the digital PLL's key parameters. This routine comprises 19 instructions that execute in about 10 µsec when IC_3's internal clock oscillator runs at 8 MHz. After each Timer 2 interrupt, the interrupt-service routine toggles the output frequency, checks for phase lock, and then divides the output of Timer 1 by two, making K equal to one, two, four, eight, or 16. The routine subtracts the resulting value from N_0 and writes the difference to Timer 2's period register, which sets the length of the output frequency's next half-period. Although some interrupt-service-routine operations slightly modify the result, this count is typically as follows:

$$\frac{f_{CLK}}{2f_{OUT}} = N_0 - \frac{|\Phi C_{OUT}|}{K}. \qquad (1)$$

For phase lock, the output-frequency half-period must equal the input-frequency half-period. The computed variable half-period count adjusts the output's frequency and phase. If the input frequency is within lock range, the variable count changes in the direction necessary to achieve and maintain phase lock between the input and the output frequency. As an example, assume that the input frequency is 10 kHz; the maximum clock-frequency cycle count for each output-frequency half-period, N_0, is 110; the division factor for the clock-frequency count that represents the phase of the output frequency, K, is two; and the output frequency is phase-locked to the input frequency. The half-period of 10 kHz is 50 µsec, or 100 counts, when the clock frequency is 2 MHz. Substituting these values in **Equation 1** and solving for the variable phase count yields a value of 20, which corresponds to a phase of 0.1, or 36°. Thus, with these parameters, the digital PLL's output frequency locks to the input frequency with a phase difference of 36°.

If the input frequency decreases, its half-period lengthens, and the variable phase count becomes smaller. According to **Equation 1**, after the division factor divides the variable phase count and you subtract it from the maximum half-period clock-frequency count, the half-period of the output frequency increases, lowering the output frequency and driving it toward a new match with the input

frequency. If the input frequency increases, the reverse occurs.

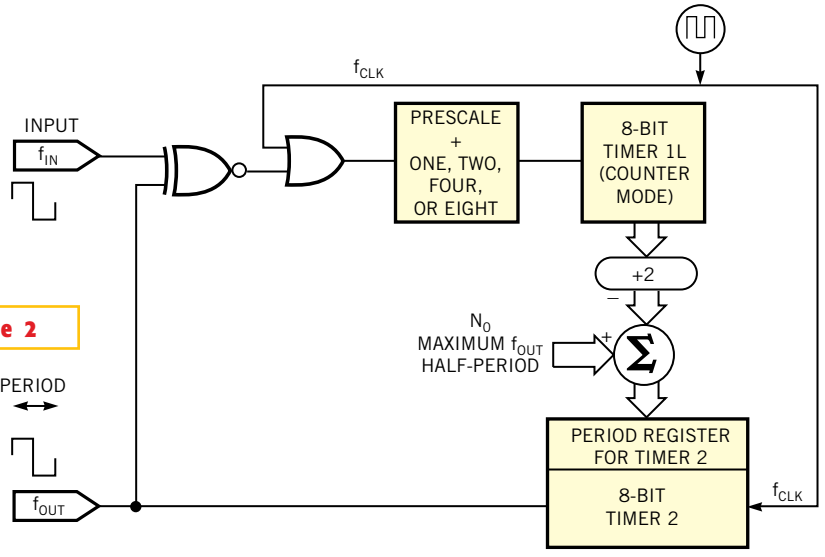
Equation 2 defines the digital PLL's operation in phase-lock frequency, and design-selected system parameters:

$$f = \frac{f_{CLK}}{\frac{2N_0}{\left(1+\frac{2\Phi}{K}\right)}+2.5}\ \text{Hz}, \qquad (2)$$

$\sim 34 \le N_0 \le 255$; K=two, four, eight, or 16; and $0 \le \Phi \le 0.5$, where f is the frequency, f_{CLK} is the clock frequency, N_0 is the maximum clock-frequency cycle count for each output-frequency half-period, Φ is the phase of the output frequency relative to the input frequency, and K is the division factor for the clock-frequency cycle count that represents the output phase of the output frequency relative to the input frequency. Adding a constant value of 2.5 to the output frequency's period count compensates for interrupt-service-routine operations that slightly affect the timing. The calculated value of phase-lock frequency is accurate to within ±1.5% over most of the PLL's usable range. Because the PLL comprises only digital circuits and software, operation with any combination of parameters is repeatable.

You can manipulate **Equation 2** to solve for any variable in terms of the remaining four. To calculate the upper and lower limits of the lock range, set Φ at 0.5 and 0, respectively. To calculate the digital PLL's "center frequency," set Φ at 0.25, which corresponds to a 90° phase angle. In the previous example, maximum frequency is 13,408 Hz, center frequency is 11,204 Hz, and minimum frequency is 8989 Hz. The lock range is 13,408 to 8989, or 4419 Hz. Increasing K to 16 yields a maximum frequency of 9544 Hz a center frequency of 9266 Hz, a minimum frequency of 8989 Hz, and a lock range of 555 Hz.

Figure 2



An XNOR-gate phase detector provides good performance with noisy signals, and a microprocessor handles signal processing.

Resolution of the DCO using Timer 2 establishes the time jitter of the output frequency relative to the input frequency. Depending on the integer count written to its period register, Timer 2 produces discrete frequencies for output frequency. When the input frequency falls between discrete output frequencies that two adjacent counts produce, the PLL switches between the counts to produce an averaged but jittery output-frequency signal at the same frequency as the input frequency. Using a relatively large value of N_0 reduces jitter, whereas a smaller value increases jitter. To improve resolution and reduce jitter, you can increase the clock frequency to 5 MHz by configuring the microprocessor's on-chip oscillator to use an external 20-MHz crystal.

You can adapt the digital PLL's basic design to a variety of applications by modifying the software and extending the interrupt-service routine. For example, stopping updates to Timer 2's period register puts the PLL in "coast" mode. Other expansion possibilities include implementing more sophisticated lock-detection circuitry to determine whether the input frequency falls within a certain frequency range and making dynamic adjustments of the values of N_0 and K for better performance. You can download **Listing 1**, which is the assembly-language source code, as well as the hex programming file for IC_3, from the online version of this Design Idea at www.edn.com.□

REFERENCE

1. Gardner, Floyd M, *Phaselock Techniques, Second Edition*, Wiley-Interscience, 1979, ISBN 0-471-04294-3.

Simple sine synthesizer generates 19-kHz pilot tone for FM baseband signal

Carlos Bernal and Diego Puyal, Departamento Ingeniería Electrónica y Comunicaciones, Universidad de Zaragoza, Zaragoza, Spain

A multiplex signal comprises baseband information transmitted on a stereo analog FM-broadcast system, plus one or more SCA (Subsidiary Communications Authorization) channels (**Figure 1**). This Design Idea presents a low-cost method of generating the basic 19-kHz pilot tone. The 19-kHz pilot tone comprises a baseband signal, and the L+R and L−R signals consist of DSBSC (double-sideband-suppressed-carrier) modulation centered at 38 kHz. For a re-

LISTING 1- ASSEMBLY-LANGUAGE SOURCE CODE
"Two gates and a microprocessor form digital PLL," EDN, April 14, 2005, pg 98.

```
;*****************************************************************
;    Filename:     DPLL.asm                                       *
;    Date:         9/14/04    10/20/04                            *
;    File Version: 00                                            *
;                                                                *
;    Author:       Kenneth W. Martin    martin@taretronics.com     *
;    Company:      TareTronics, Inc.    www.taretronics.com        *
;                                                                *
;*****************************************************************
;    Files required:                                             *
;       p16F818.inc                                              *
;                                                                *
;*****************************************************************
;    Notes:                                                      *
;       1.      PLL code locks internal Timer2 to square wave digital signal. *
;       2.      Uses external Exclusive-NOR gate (Phase Detector), and OR Gate*
;   3.  Includes simple phase lock detector & lock indicator signal.  *
;*****************************************************************

        list      p=16f818           ; list directive to define processor
        #include <p16F818.inc>        ; processor specific variable definitions

        errorlevel  -302             ; suppress message 302 from list file

        __CONFIG   _CP_OFF & _WRT_ENABLE_OFF & _CPD_OFF & _CCP1_RB2 & _DEBUG_OFF &
_LVP_OFF & _BODEN_OFF & _MCLR_OFF & _WDT_OFF & _PWRTE_OFF & _INTRC_CLKOUT

;***** VARIABLE DEFINITIONS
w_temp        EQU     0x40        ; variable used for context saving
status_temp   EQU     0x41        ; variable used for context saving
N0                      EQU             0x42            ;sets lock range lower
frequency - Period_count/2
Lock_cnt        EQU             0x43            ;counter for Lock detection
Phase_clk       EQU             6                       ;PORTB  - Phase-gated Clock
input
Fout            EQU             3                       ;PORTA  - PLL output
Phase           EQU             7                       ;PORTB  - Phase input
Lock_ind        EQU             1                       ;PORTA  - Lock indicator

;*****************************************************************
        ORG     0x000             ; processor reset vector
                goto    main              ; go to beginning of program


        ORG     0x004             ; interrupt vector location

                ;movwf   w_temp            ; save off current W register contents
                ;movf    STATUS,w          ; move status register into W register
                ;movwf   status_temp       ; save off contents of STATUS register

                ;btfsc  PIR1, TMR2IF
                ;goto   PLL_out

PLL_out bcf             STATUS, C
                movlw   b'00001000'
                xorwf   PORTA, F                ;toggle Fout

                btfss   PORTB, Phase    ;check for Phase Lock
                movwf   Lock_cnt                ;not Phase Locked - reload Lock counter

                rrf             TMR1L, W                ;divide phase count by 2
                clrf    TMR1L
```

```
                subwf   N0, W                    ;N0 - Ph Count/K
                btfss   STATUS, C
                movlw   0
                ;bsf            STATUS, RP0
                movwf   INDF                    ;update count in PR2, to set next Fout
half-period
                ;bcf            STATUS, RP0
                bcf             PIR1, TMR2IF

                decfsz  Lock_cnt, F
                goto    Unlock
LOCKED  bsf             PORTA, Lock_ind
                incf    Lock_cnt, F
                retfie
Unlock  bcf             PORTA, Lock_ind
                retfie

        ;movf    status_temp,w     ; retrieve copy of STATUS register
        ;movwf  STATUS            ; restore pre-isr STATUS register contents
        ;swapf   w_temp,f
        ;swapf   w_temp,w          ; restore pre-isr W register contents
        ;retfie                    ; return from interrupt

main    clrf    PORTA                   ; Initialize PORTA by clearing output data
latches
                bsf             STATUS, RP0             ; go to Bank 1
                movlw   b'01110000'             ;set Internal Clock to 8 MHz
                movwf   OSCCON                  ;Fclk for DPLL = 2 MHz
                movlw   0x06                    ;Configure all pins as digital inputs
                movwf   ADCON1
                movlw   b'10110101'             ;set RA3(Fout), RA6(CLKOUT), &
RA1(Lock_ind) to output
                movwf   TRISA
                movlw   b'11010111'
                movwf   OPTION_REG
                movlw   0xFF
                movwf   PR2
                bcf             STATUS, RP0             ;go back to Bank 0
                clrf    TMR1H
                clrf    TMR1L
                movlw   b'11000000'             ;enable GIE,& PEIE interrupts
                movwf   INTCON
                movlw   PR2
                movwf   FSR

                movlw   D'110'                  ;sets N0, low frequency end of lock
range
                movwf   N0

                movlw   b'00000111'             ;Prescale value = 1:1, resulting in K=2
                movwf   T1CON                   ;enable Timer 1 (Counter mode) & set
Prescale value
                bsf             T2CON, TMR2ON   ;enable Timer 2
                clrf    TMR2
                bsf             STATUS, RP0
                bsf             PIE1, TMR2IE    ;enable Timer 2 interrupt
                bcf             STATUS, RP0
                clrf    PIR1

        wait    goto    wait    ;wait for interrupt


        END                       ; directive 'end of program'
```

ceiver to correctly demodulate the signal, the transmitted pilot tone and L−R signal must synchronize at their respective zero crossings. In addition, any distortion in the pilot tone produces harmonics that can interfere with adjacent sections of the signal.

The low-distortion, 19-kHz pilot-tone generator comprises a resistive voltage divider, R_1 through R_{11}, connected between the V_{CC} and $-V_{CC}$ supply rails (**Figure 2**). The resistors' values are weighted to provide N=8 approximate sampled values of a sine wave and are relatively low to present "stiff," low-impedance sources to eight-channel analog multiplexer IC_1. An up/down counter, IC_2, drives IC_1 and takes advantage of a sine wave's inherent symmetry to enhance the resolution and reduce the distortion of the 19-kHz pilot sine wave.

In effect, analog multiplexer IC_1 acts as a zero-order hold circuit, producing an N times Nyquist oversampled sine wave of frequency f_{SIN}, plus several attenuated alias frequencies centered at: $f_{ALIAS} = m\times(2\times N\times f_{SINE})$, where m=1, 2, 3. For most applications, a simple passive RC filter at the multiplexer's output adequately removes the alias frequencies. Binary counter IC_3 generates a 608-kHz clock signal plus a 19-kHz up/down control signal for counter IC_2, and sections of hex inverter IC_1 serve as a crystal oscillator and buffer.

You can expand the basic circuit by duplicating the resistor network, multiplexer, and up/down counter. An external audio source drives the resistor network's upper and lower ends with L and R audio signals that have undergone lowpass-filtering to eliminate components with frequencies greater than 15 kHz. A 1.216-MHz signal clocks the second up/down counter and a 38-kHz up/down control signal derived from higher frequency taps on counter IC_2. The added circuitry generates the baseband L+R channel, and the L−R modulation in synchronism with the 19-kHz pilot tone because all clock pulses originate from a common counter. To produce the composite multiplex signal, the outputs of both analog multiplexers sum in an external network.

Using the specified components, the circuit generates a 19-kHz pilot tone with harmonics 60 dB below the fundamental and synchronous with the maximums of the suppressed 38-kHz carrier. The same circuit structure produces L+R- and L−R-channel generation without changing components' values. Potentiometer P_1 allows a 90±10° fine phase adjustment to correct distortion and to resynchronize at zero crossing.□

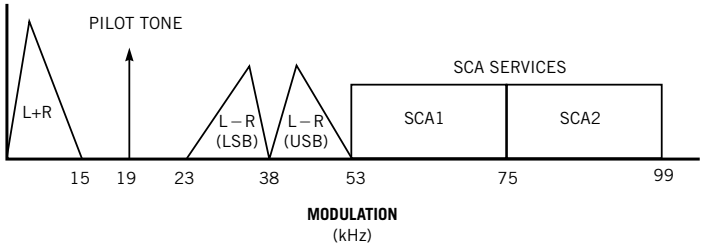


Figure 1 A typical FM-broadcast signal contains a complex spectrum.

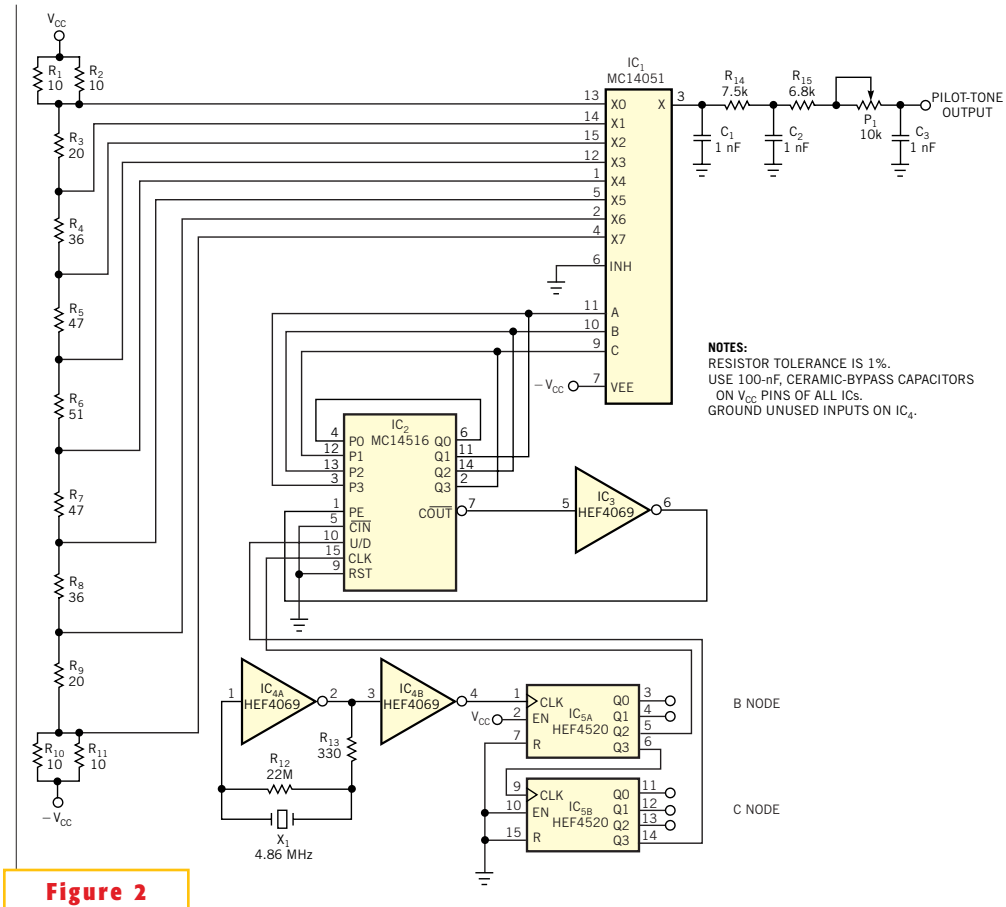


Figure 2 The pilot-tone-generator circuit uses low-cost CMOS-logic circuits plus an analog multiplexer.

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Edited by Brad Thompson

Camera serializer/deserializer chip set reduces wire count for keypad

Wallace Ly, National Semiconductor Corp

Many systems that require a user to manually enter data feature a keyboard similar to that in **Figure 1**. Although early keypads comprised arrays of individually wired switches, a typical modern keypad comprises a matrix of x and y lines. Pressing a key creates a momentary connection between an x line and a y line. For example, an individually wired keypad comprising discrete switches arranged in four rows and three columns (also known as a 4×3 layout) would require 24 wires. The more economical matrix approach in **Figure 2** requires only seven signal wires, but even that number can sometimes prove difficult to route to a microcontroller. To further reduce the number of interconnecting wires from seven to three, plus a ground return, you can adapt a configurable serializer/deserializer such as National Semiconductor's LM2501.

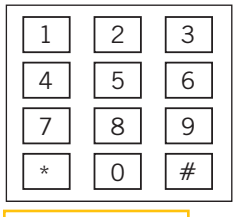


Figure 1

A typical keypad provides a limited number of numeric keys and two symbols–the asterisk (*) and the octothorpe (#).

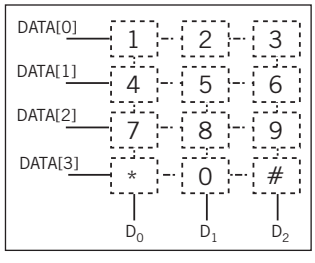


Figure 2

In a matrix keypad, pressing a key creates a connection between a row wire and a column wire.

The device typically finds use in adapting video buses, such as wide, low-voltage CMOS-video interfaces for portable electronics to Mobile Pixel Link service. The LM2501's typical application circuit features low-voltage and low-current operation and produces low levels of EMI (**Figure 3**). The circuit requires only two support devices—a counter (a CMOS CD4017 decade counter) and a 10-MHz clock-oscillator module (**Figure 4**). In operation, the host microcontroller drives the deserializer's WCLK input pin with a low-voltage-CMOS clock pulse,

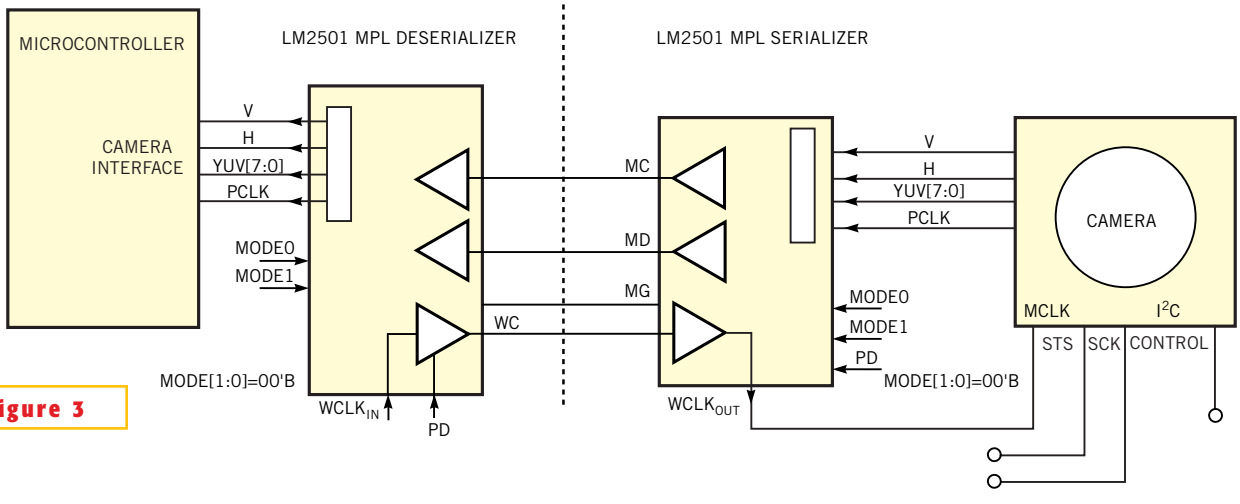


Figure 3

In a typical application, a pair of LM2501s converts multiconductor video data to serial data and restores the data to multiconductor format.

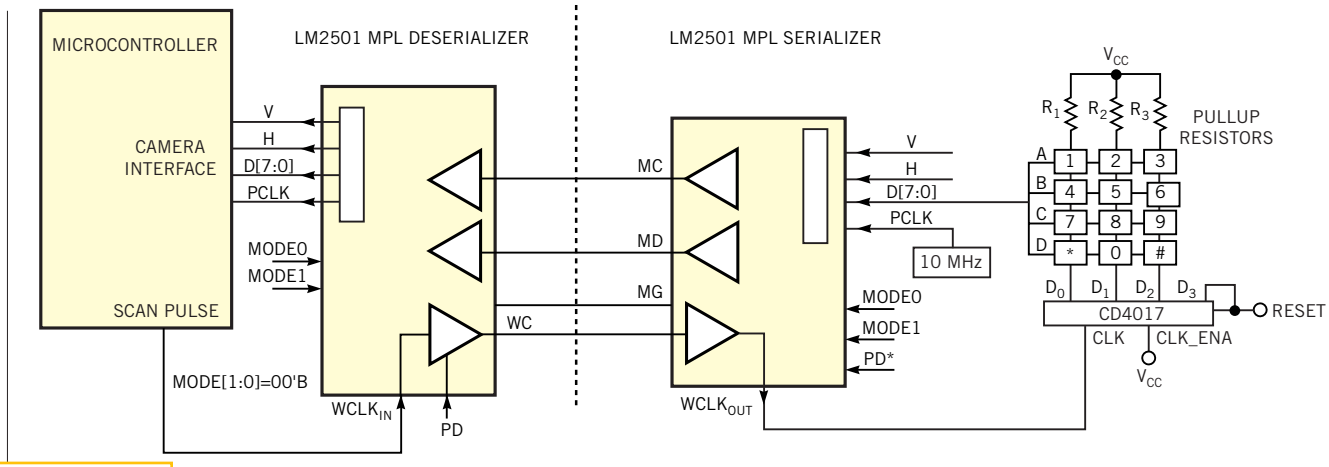


Figure 4 You can apply the LM2501 to reduce the number of signal lines a keypad-to-microprocessor interface requires.

which translates to an MPL-level signal and then is applied to the serializer. The serializer reconverts the WCLK pulse, which drives the counter's clock input.

Unlike divide-by-10 encoded-output decade counters, the CD4017's internal organization comprises a Johnson counter that activates only one of its 10 outputs at a time. Thus, the counter's outputs D_0, D_1, and D_2 sequentially apply a logic one to the keypad's column lines, and output D_3 resets the counter to zero. When a user presses a key and connects a column line to one of four row lines, the serializer samples the keypad's row lines, converts the selected active line to a serial signal, and transmits the signal to the deserializer.

For example, suppose that the user presses the 5 key. The first clock pulse that the CD4017 receives drives column line D_0 to a logic one, but, because the user does not press keys 1, 4, 7 and *, row lines A, B, C, and D remain at logic zero. The second clock pulse drives column line D_1 to a logic one, and pressing key 5 connects row line B to logic one, whereas lines A, C, and D remain at logic zero. The pseudocode fragment in **Listing 1**, available in the online version of this Design Idea at www.edn.com, instructs the microcontroller to decode which key a user is currently pressing. In practice, additional code enables the microcontroller to reject multiple simultaneous key closures.

You can expand the architecture to accommodate a keypad matrix as large as 8×10 keys by using more of the counter's outputs and wiring the Nth output to the counter's reset input. The keypad's rows connect to the serializer's data inputs, and both of the LM2501s' unused inputs connect to pullup resistors, ground, or V_{CC}.□

Rearranged reference helps ADC measure its own supply voltage

Björn Starmark and Orville Buenaventura, Maxim Integrated Products Inc, Sunnyvale, CA, and Sören Käck, Audioväxlar, Sweden

If you use an ADC to monitor a system's power-supply voltage, you may encounter situations in which the supply voltage exceeds the ADC's reference voltage (**Figure 1**). However, the ADC's input voltage cannot exceed its reference voltage. You can use an external resistive divider to bring the supply voltage within the ADC's input range, but even 0.1%-

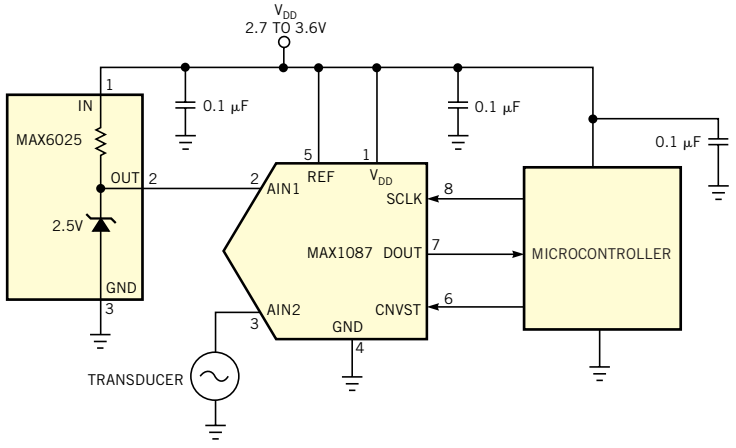


Figure 2 A precision resistive divider brings the power-supply voltage within this ADC's input range but introduces measurement errors.

tolerance resistors may introduce an objectionable error. You can solve the problem by eliminating the divider, connecting the ADC's reference input to its power supply, and connecting one of the ADC's inputs to a precision voltage reference—in this case, a 2.5V MAX6025A (**Figure 2**).

In this configuration, the ADC measures its inputs with respect to the supply voltage. Using the digitized reference voltage as a standard, the system's software computes the ratio of the reference voltage with respect to the power-supply voltage and corrects the remaining inputs' measurements. The ADC must accommodate an external reference voltage that equals its power-supply voltage, and any noise on the supply rail disturbs measurements of all channels. Thus, to quiet the supply rail in electrically noisy environments, you may need to add a lowpass filter to provide extra decoupling at the ADC.□

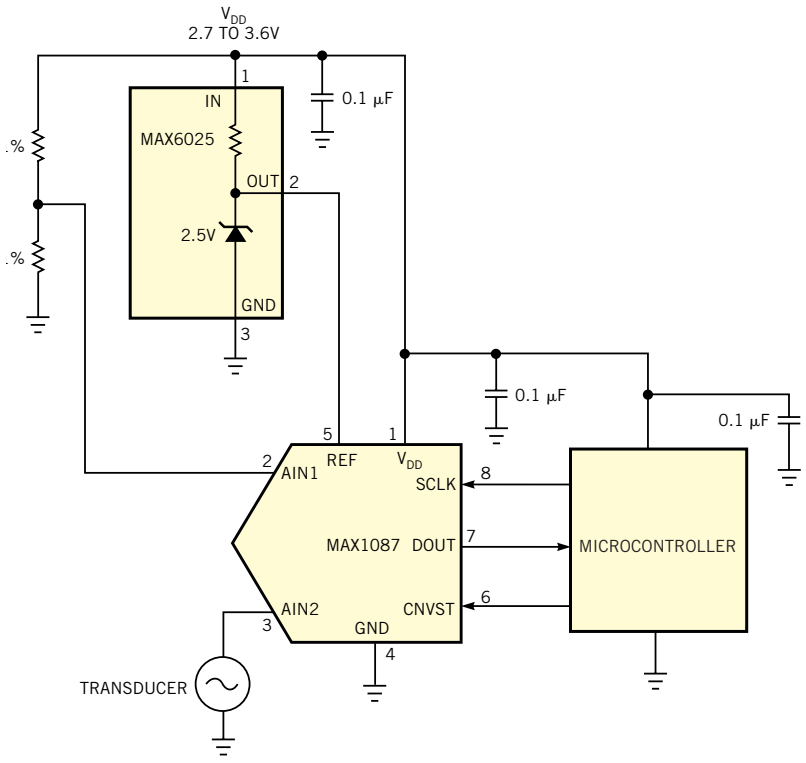


Figure 1 To eliminate the resistive divider, you connect the ADC's reference voltage to its power supply and measure the precision voltage reference's output.

Difference amplifier measures high voltages

Moshe Gerstanhaber and Chau Tran, Analog Devices, Wilmington, MA

FIGURE 1 shows two large-signal-measurement methods. The first uses a two-resistor voltage divider and an output buffer, and the second comprises an attenuating inverter and a high-value input resistor. Both of these approaches introduce measurement-linearity errors because only a single resistor dissipates power, which leads to self-heating and its associated change in resistance. In addition, the amplifier and the remaining resistors introduce a combination of offset current, offset voltage, CMRR (common-mode-rejection-ratio) effects, gain error, and drift, which may significantly reduce the system's overall performance.

Based on Analog Devices' AD629, the circuit in **Figure 2** can measure inputs in excess of 400V p-p with less than 5-ppm linearity error. The circuit attenuates its input signal by a factor of 20 and delivers a buffered output. Packaging the amplifier and attenuator resistors together ensures that both resistors in the attenuator string operate at the same temperature. The amplifier's input stage employs superbeta transistors to minimize offset current and errors due to bias current errors. Applying 100% feedback at low frequencies introduces no noise gain, and the offset voltage and its drift add almost no error.

The AD629 is unstable with 100% feedback, and the 30-pF capacitor adds a pole and a zero to the feedback gain to stabilize the circuit and maximize the

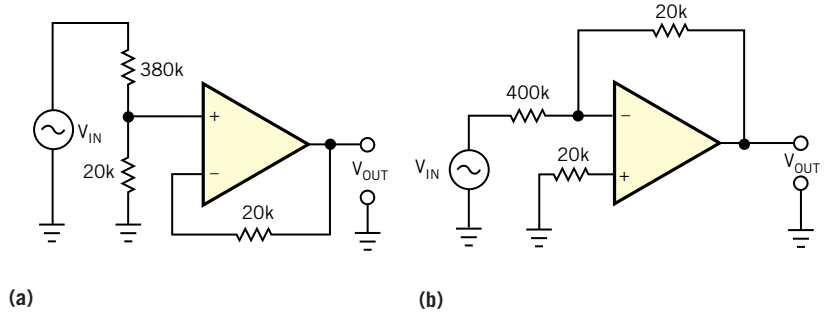


Figure 1 To measure high voltages, you can use discrete resistors to assemble an input voltage divider and buffer (a) or an attenuating inverter (b), but performance suffers due to thermal mismatch.

system bandwidth. The following equation calculates the pole frequency, f_p: $f_p = 1/(2\pi(380\ k\Omega + 20\ k\Omega) \times 30\ pF) = 13$ kHz. The following equation determines the zero frequency, f_Z: $f_Z = 1/(2\pi(20\ k\Omega) \times 30\ pF) = 265$ kHz.

Figure 3 shows the amplifier's performance with a 400V p-p input (upper trace) and its corresponding 20V output (lower trace). In **Figure 4**, a cross plot shows linearity for a 50V/division input signal and a 5V/division output. **Figure 5**, a linearity-error plot, shows nonlinearity versus a 400V p-p input signal.□

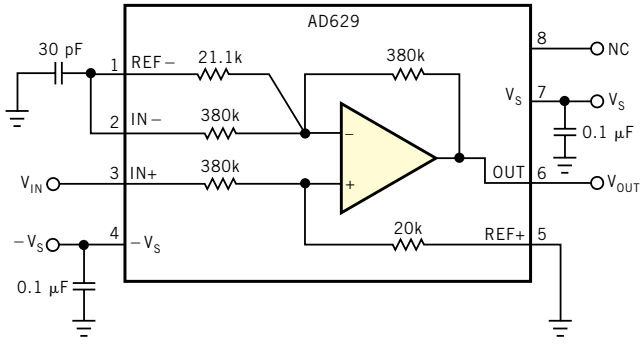


Figure 2 An integrated approach moves external resistors into the device's package for improved thermal tracking and greater accuracy.

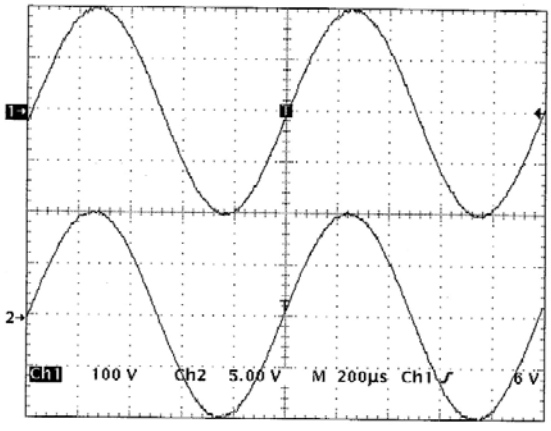


Figure 3 The circuit in Figure 2 delivers a 20V p-p output for a 400V p-p input.

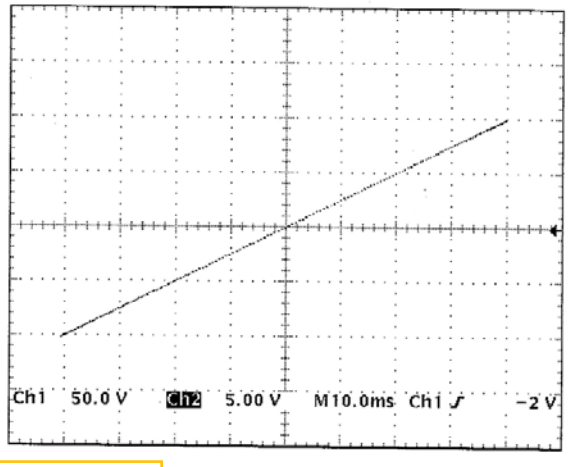


Figure 4 Plotting input versus output shows minimal departure from an ideal straight line for a 400V p-p input.

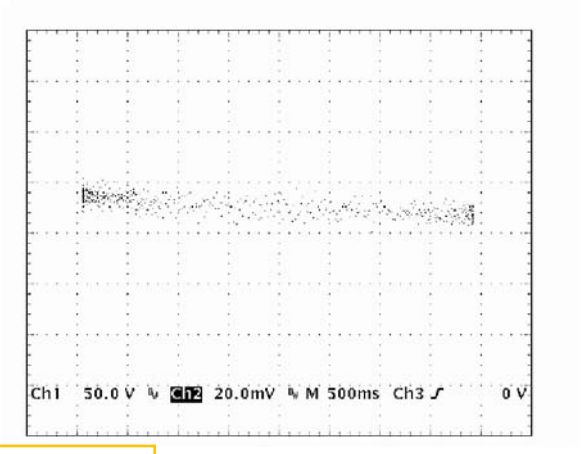


Figure 5 A scatter plot of nonlinearity error for a 400V p-p input displays error of less than 10 ppm over the input range.

Linear potentiometer provides nonlinear light-intensity control

Stephan Goldstein, Analog Devices, Wilmington, MA

THE HUMAN EYE'S highly nonlinear response to light levels poses problems for designers of adjustable lighting. Simple hardware or software linear-control methods compress most of the apparent intensity variation into a relatively small portion of the adjustment range. A strongly nonlinear control characteristic is necessary. Such a characteristic

spreads the intensity adjustment over a wider range and offers a more natural feel. This Design Idea shows how to use an inexpensive linear potentiometer to develop a satisfactory hardware technique. In an experiment in a darkroom, one of the room's corners was too dark because a fixed barrier shielded safe light. Using spare parts from a junk box, you could assemble a simple red LED-based auxiliary safe light, but if the light level were adjustable, you could balance the light levels and minimize the risk of fogging the printing paper. However, the experimenters in this case lacked an audio-taper intensity-control potentiometer and wanted to avoid paying for one.

Figure 1 shows a simplified version of the technique. Diode-connected transistor Q_1 and an AD589 1.235V reference, IC_1, produce a reference voltage of $1.235V+V_{BE}(Q_1)$ at Node A. Connected between Node A and Q_2's emitter, linear potentiometer R_2 and resistor R_3 cause Q_2's emitter and collector current to vary as $1.235V/(R_2+R_3)$. The relationship isn't exact because the V_{BE} voltages of Q_1 and Q_2 vary slightly as you adjust the potentiometer, but, in practice, this nonlinear—if not logarithmic—characteristic works well.

Transistor Q_2's collector current generates the control voltage across R_4, and, whereas Q_2 always operates close to saturation, the components limit Q_2's collector-base forward bias to an acceptable 200 mV. When you set R_2 to its minimum resistance for maximum light intensity, resistor R_3 limits LED current, and, when you set R_2 to its maximum resistance for minimum intensity, R_1 limits the current through IC_1.

The reference voltage produced at Q_2's collector drives a standard integrating servoamplifier comprising an AD8031 rail-to-rail op amp, IC_2; an IRFD010 low-power MOSFET, Q_3; R_5 ;R_6; and C_2. The servo sets the current through R_5 to R_4/R_5 times the current through R_4. Resistor R_7 isolates Q_3's gate capacitance to prevent load-induced instability in IC_2. A 12V-dc module supplies power to the circuit and allows the use of four LEDs per string, for a total voltage drop of approximately 8V across each string. To prevent current hogging and provide a maximum of approximately 20 mA for each series-connected LED string, resistors R_8 through R_{11} divide Q_3's drain current into four. Voltage drop across each resistor is 1V, leaving Q_3 to support a 3V drain-source voltage and an approximately 250-mW power dissipation. If you increase the number of LEDs or the power-supply voltage, you may need to replace Q_3 with a higher dissipation MOSFET.□

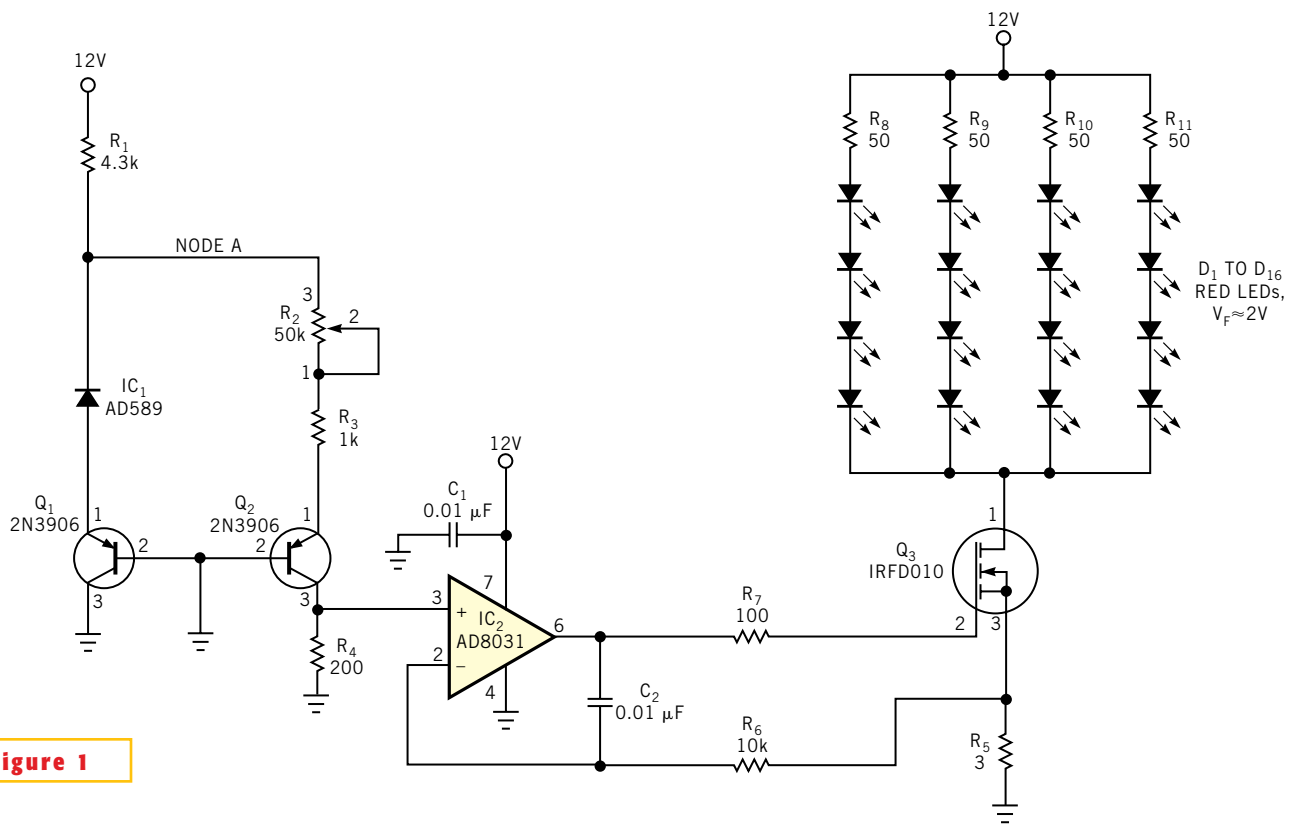
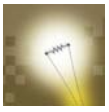


Figure 1

A handful of components provides linear adjustment of a darkroom's safe light.



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Edited by Brad Thompson

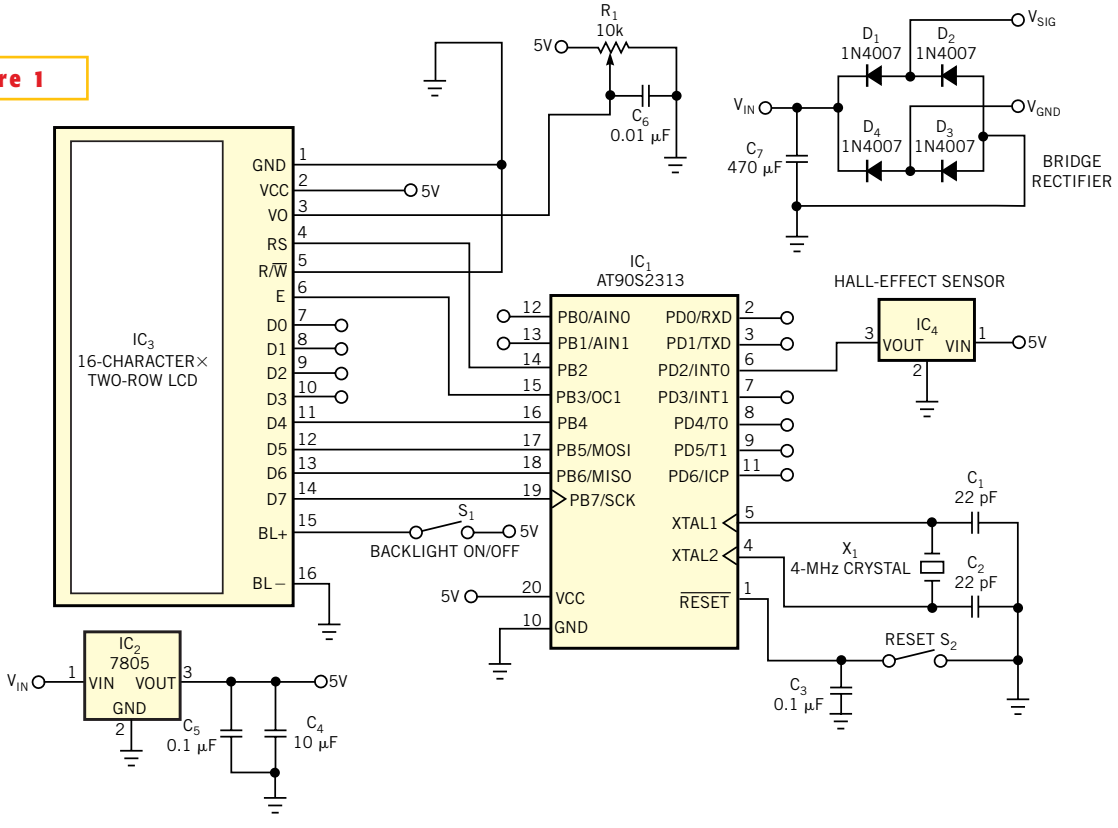
Versatile digital speedometer uses few components

Abhishek Jain, Netaji Subhas Institute of Technology, Dwarka, New Delhi, India

A speedometer measures a wheel's rotational speed. Unlike conventional mechanical and moving-magnet designs that use analog moving-pointer displays, the electronic speedometer in this Design Idea features a digital readout and a power-saving device that uses few components. **Figure 1** shows the digital speedometer's circuit design. An Atmel AVR AT90S2313 microcontroller, IC_1, drives IC_3, a 16-character, two-row LCD. All components except IC_4, an Allegro A3121 Hall-effect sensor reside on a pc board within the reach and view of the vehicle's operator. The Hall-effect sensor attaches to the vehicle near its periphery and a fixed distance from the wheel's axle. When the wheel rotates, a permanent magnet attached to the wheel passes the sensor, activating it and generating one short pulse for each revolution of the wheel.

After you apply the pulse's rising edge to the IC_1's INT0 input, the rising edge generates a high-priority interrupt. The AVR calculates the elapsed time between two interrupts, computes the speed and distance traveled, and displays the results on the LCD. One of IC_1's internal timers, $Timer_0$, increments after every N clock

Figure 1



Three ICs and an LCD form a versatile digital speedometer.

pulses. Distance traveled equals $2\pi R$, where R is the wheel's radius. To calculate speed, IC_1 divides the distance the elapsed time travels. In this application, the display shows speed in kilometers per hour.

In addition, IC_1 keeps the track of distance traveled by incrementing a register every time a sensor interrupt occurs. It compares this register value with a number that's equivalent to a 100m distance traveled, and, when the register value exceeds the 100m constant, IC_1 increments the distance register. The display shows the distance traveled in kilometers, and a location in IC_1's EEPROM retains the distance even when a users switches off power to the speedometer. Maximum values of the design include speeds of 0 to 255 km/hour and distances as far as 9999.9 km.

The design requires a 5V-dc power supply to work properly. To accommodate higher power-supply voltages, a bridge rectifier and a 7805 voltage regulator, IC_2, accept power supplies ranging from 6 to 24V dc or ac for indoor applications. At 12V-dc input, the speedometer draws approximately 43 mA, or approximately 500 mW, under normal conditions. Switching on the LCD's backlight for night operation increases current drain by approximately 11 mA for a power consumption of approximately 730 mW.

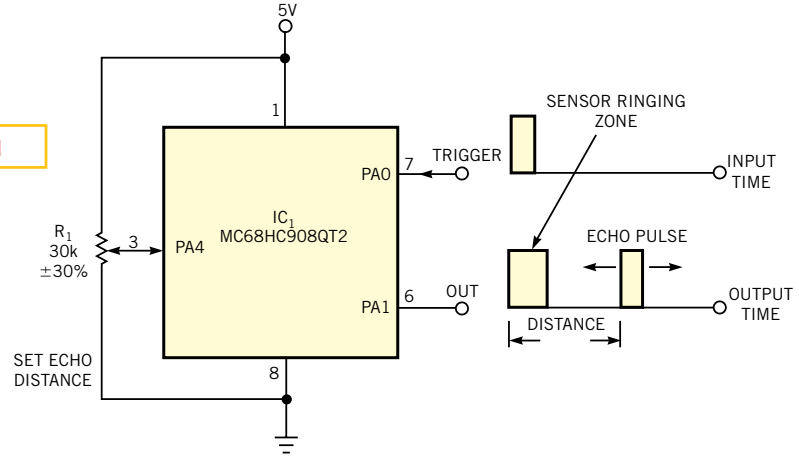
You can download the source code for IC_1's program from the online version of this Design Idea at www.edn.com and assemble the software with Atmel's AVR Studio 4 software. You can alter constants within the software to accommodate wheels of various radii for other applications. Future enhancements to the software would allow measurement and display of a rotating object's speed in revolutions per minute or show elapsed distances when you use the device as a trip meter.□

Microprocessor, linear potentiometer deliver echo pulses

Abel Raynus, Armatron International Inc, Malden, MA

For designers of radar or sonar echo-ranging systems, an echo imitator can ease development and adjustment chores by generating a controllable pulse that's similar to an incoming echo signal. A decade ago, you'd probably use several 555 timers and their associated RC circuits to design an echo imitator. As **Figure 1** shows, today's version uses only two components: linear potentiometer R_1 and a small, low-end microcontroller, IC_1. An external trigger pulse applied to IC_1's pA0 input pin triggers the first of two pulses delivered to output pin pA1. For ultrasonic-receiver testing, the optional first pulse imitates 2 msec of post-trigger sensor ringing that limits the minimum reception distance. You can also use this pulse to synchronize an oscilloscope.

Figure 1



The firmware's features determine the characteristics of this radar and sonar echo simulator.

Linear potentiometer R_1, a Panasonic model EVA-JGTJ20B14, sets the echo pulse's delay time. Microcontroller IC_1, a Freescale MC68HC908QT2 8-bit flash-memory device, includes four 8-bit successive-approximation ADCs, one of which digitizes the voltage at R_1's sliding contact. For this application, the firmware divides the digitized potentiometer readings by four to match the system's reception range. Every 0.5 msec, the firmware also generates internal timer-overflow interrupts that determine the resolution of the simulated target's return echo. The interrupt-service routine increments the distance counter, and, when the counter's value equals the distance setting that R_1 supplies, output pin pA1 produces a 0.5-msec-wide echo pulse. Thus, the echo's delay time tracks the potentiometer's sliding-contact position. Although this Design Idea features a Freescale microcontroller, you can use others that include an ADC. To download the firmware's assembler code, view the online version of this Design Idea at www.edn.com.□

Passive-detector receiver keeps you informed, entertained during flights

David Prutchi, PhD, Voorhees, NJ

FAA (Federal Aviation Administration) regulations generally forbid the use of receivers onboard commercial aircraft because a superheterodyne receiver's local oscillator can radiate signals that could interfere with aircraft communication and navigation systems. The crystal radio in **Figure 1** directly detects nearby AM signals in the very-high-frequency aircraft band, 118 to 137 MHz, and thus cannot interfere with aircraft equipment. Communications between the pilot and the flight controllers are brief and infrequent, and listening to the aircraft band as a passenger can get boring. However, the circuit in this Design Idea improves on an earlier passive aircraft-band receiver by allowing you to enjoy an aircraft's in-flight-entertainment system while monitoring pilot-to-ground communications (**Reference 1**).

In **Figure 1**, the shields of the headphone's wires double as an antenna. A series network comprising L_2 and C_3 couples RF energy into a resonant LC tank circuit comprising L_1 and trimmer capacitor C_1. You adjust C_1 to peak the tank circuit's resonant frequency within the 118- to 137-MHz aircraft band. The crystal detector comprises Schottky diode D_1 that is forward-biased through R_1 and R_2. Depending on the diode's characteristics, you may have to adjust R_1 to optimize the diode's bias current.

Both sections of IC_1, a Maxim MAX474 single-supply, 2.7 to 5.25V, rail-to-rail, dual op amp, boost the level of demodulated audio that D_1 and C_4 recover. Lowpass filters R_5 and C_{12} and R_7 and C_{13} limit audio bandwidth to voice-range frequencies to improve intelligibility and reduce power consumption. Capacitors C_{10} and C_{11} split the amplified audio signal into two channels to drive stereo-headphone amplifier IC_2, a Texas Instruments TPA4411. Capacitors C_8 and C_9 drive IC_2's inputs with stereophonic audio signals from the aircraft's entertainment system or a portable CD/DVD player. The TPA4411 headphone amplifier provides a fixed gain of −1.5, which allows you to maintain a comfortable listening level by adjusting the aircraft-entertainment device's volume control. Potentiometer R_6

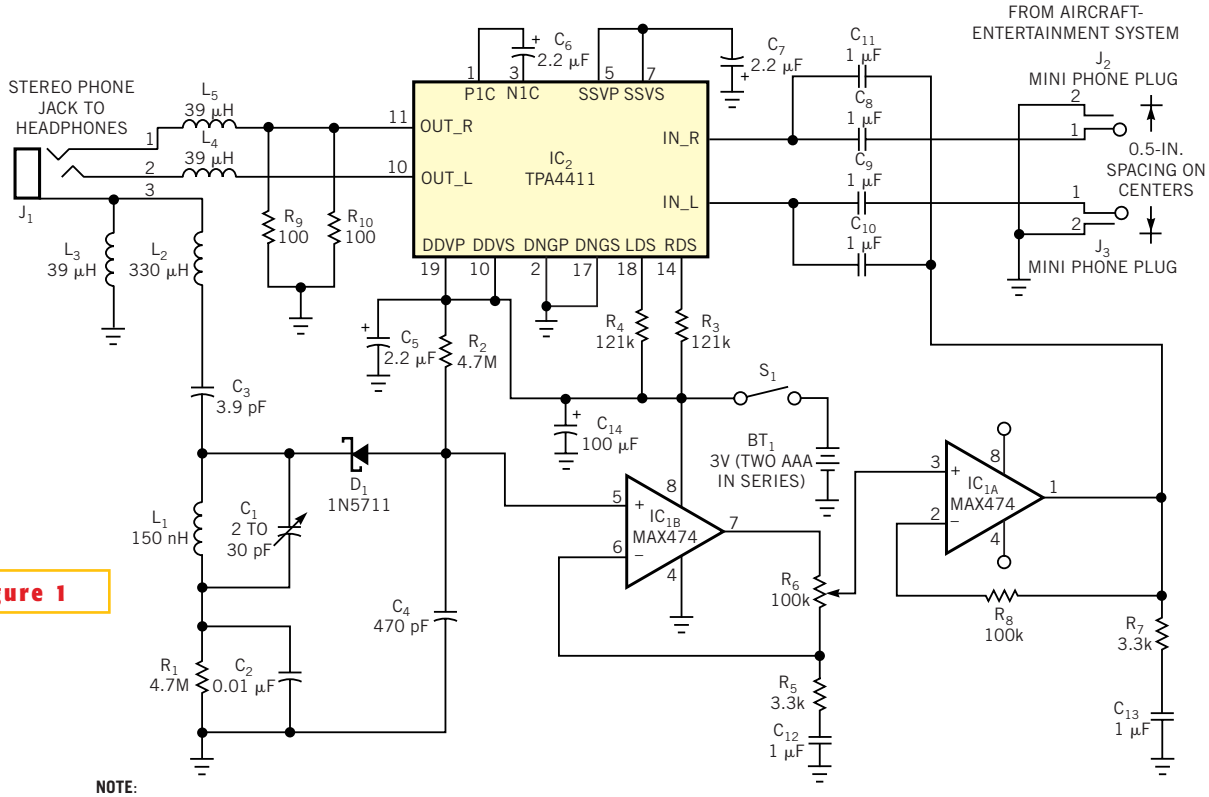


Figure 1

NOTE:
MOUNT PHONE PLUGS J_2 AND J_3 ON 0.5-IN. CENTERS TO MATCH AIRCRAFT-ENTERTAINMENT SYSTEM'S AUDIO-JACK SPACING.
SELECT R_1 TO BIAS DIODE.

This modern version of the crystal radio allows you to monitor aircraft communications while listening to in-flight-entertainment programs.

controls the aircraft-band audio level, and the user should adjust it during quiet radio periods to minimize noise introduced into the entertainment audio program.

The TPA4411 integrates pop-noise-reduction circuitry, can drive as much as 80 mW into a typical headphone's 8 to 16Ω load, and operates over a power-supply range of 1.8 to 4.5V. Inductors L_3, L_4, and L_5 allow audio to pass unimpeded to the headphones and prevents the amplifier's outputs from shunting RF signals meant to be coupled to the receiver's resonant LC tank circuit.

To use the receiver, slowly adjust C_1 until you hear a pilot's communication in progress. Then, quickly tune C_1 to maximize the signal. The tuned circuit's selectivity is low enough such that, once you adjust C_1, it doesn't require retuning. Although you can use this receiver while awaiting your flight's boarding call, always ask permission from the flight crew before using the receiver aboard an aircraft. You can explain that the circuit does not interfere with the aircraft's navigation and communication systems. Airport-security personnel may regard any user-constructed electronic device with suspicion, however.

This receiver's sensitivity is low, and you generally hear only the pilot-to-ground side of two-way traffic. Fortunately, in controlled airspace, a pilot must repeat all commands so that air-traffic controllers can verify that the pilot clearly understood their instructions. Although a comprehensive survey of aircraft-band communications procedures is beyond the scope of this Design Idea, the following example explains certain terms.

While the aircraft remains at the departure gate, you typically hear a pilot repeating flight clearance, altitude restrictions, and other instructions—for example, "KLM 657 heavy, cleared for Amsterdam ... FL320 five minutes after departure. Departure frequency is 127.4, squawk 4312." "Heavy" means that the aircraft is a large jet, "FL320" means that the aircraft is cleared to fly at 32,000 feet, and "squawk" is the aircraft's four-digit identification number. To contact departure control, the pilot retunes the aircraft radio to 127.4 MHz. When the pilot enters the squawk into the aircraft's transponder, the flight controllers can identify the aircraft on-radar screens as KLM flight 657. Each time the aircraft enters a new segment of the taxiway on its way to the runway and again for takeoff clearance, the pilot contacts ground control to get taxi clearances.

Shortly after takeoff, the pilot contacts departure control: "KLM 657, radar contact, climb and maintain FL320, turn right heading 120, proceed on course." From then on, the pilot contacts flight controllers upon reaching predefined altitudes or when entering a different flight-control center's airspace. Approximately 30 minutes before reaching its destination, the aircraft begins its descent, and the pilot contacts approach control. Just before landing, you hear the final clearance: "KLM 657 heavy, winds 030 at 12, cleared to land runway 31."□

REFERENCE

1. Wenzel, Charles, "Passive aircraft receiver," www.techlib.com/electronics/aircraft.htm.

Quickly estimate an electronic system's cooling requirements

James Gabel, Thermo Electron Corp, San Jose, CA

DURING NORMAL OPERATION, an electronic system generates wasted heat that can cause malfunctions and damage components unless you remove it. In an ideal world, you would have the time and resources to perform a rigorous evaluation of an electronic system's cooling requirements early in the design phase and thus avoid the cooling errors others have made in the past (**Reference 1**). However, circumstances often demand a diagnostic evaluation of a system's cooling methods or a rapid estimate of a proposed system's cooling requirements. For these purposes, you don't need an advanced degree in computational fluid dynamics; this Design Idea outlines a method that may be all that's necessary.

Figure 1 shows a typical cabinet-mounted electronic system that includes

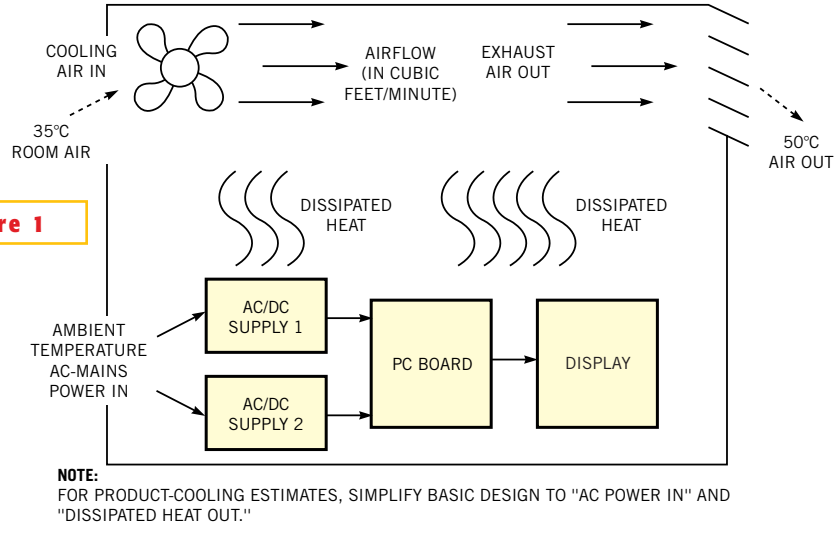


Figure 1

To estimate a system's cooling requirements, you can simplify the thermal model to comprise an ac-power input and a dissipated-heat output.

two power supplies, a pc board, and a display. For simple products, you can assume that all of the power entering the cabinet from the ac power line ultimately converts into heat that dissipates within the cabinet. After you calculate the system's ac and dc power requirements, you can estimate the amount of power that the cooling method must dissipate. As a rule of thumb, the thermal capacity of air is 0.569W-minute/°C/ft^3 (**Reference 2**). That is, one cubic foot per minute of moving air can transfer 0.569W of dissipated heat for a 1°C temperature change. You can also express this rule as its reciprocal: To dissipate the heat 1W of power produces and maintain a 1°C temperature change, you need to provide an air stream of 1.757 cfm (cubic feet/minute). Thus, once you determine the wattage dissipated within a system and specify an allowable internal temperature rise, you can estimate a cooling fan's required air-movement capacity rating in cubic feet/minute.

However, a cooling fan's maximum rating in cubic feet/minute occurs only at zero static pressure, or back pressure, an operating condition that you don't realize in practice. You derate the fan's air-movement ability based on either measurements or estimates of the back pressure in the system's cabinet. (A manometer-style gauge measures air-pressure differentials in units of inches of water—that is, the height in inches of a column of water supported by the difference between ambient air and pressurized air within an enclosure.) For example, a manometer might display a pressure differential of 0.10 to 0.15 in. of water across a mostly clogged dust filter. When you plot the pressure versus airflow-volume curve for a typical 100-cfm fan, this pressure differential might reduce the fan's airflow volume to only 50 cfm.

In a sample calculation, a system uses 70% of a single ac/dc 400W power supply's output that operates at 75% efficiency—that is, the supply contributes 25% of its output as heat. The system's fan or fans must remove all of the resultant waste heat, as follows: $P_{DISS}=125\%\times400W=500W$; $70\%\times500W=350W$. Design the system for operation in ambient air that's no hotter than 35°C (95°F). The system's heated exhaust air must not exceed a worst-case temperature of 50°C (122°F), producing a temperature difference, T_D, of 15°C. Next, calculate n, the effective airflow required, in units of cubic feet/minute: $n(cfm)=k\times P_{DISS}/T_D$, where $k=1.757$ cfm×°C/W. Solving for n yields: $n=1.757$ cfm×°C/W×350W/15°C= 40.99 cfm.

Select a fan and examine its pressure versus-airflow-volume curve (**Figure 2**). At an airflow of 41 cfm, the fan's static pressure curve shows 0.1 in. of water within the fan's normal operating range. (For additional information on fans and their characteristics, see **Reference 3**.)□

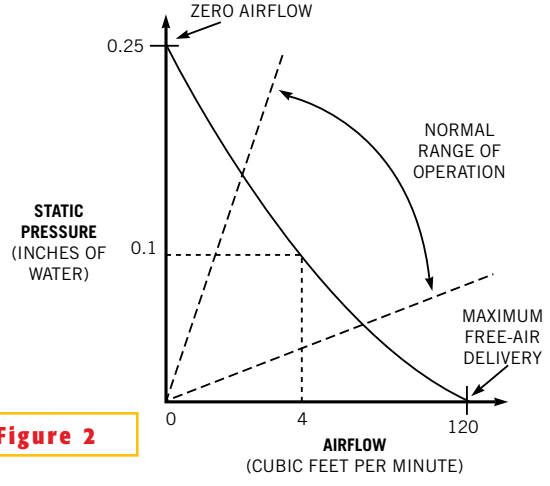


Figure 2

You can use a fan's airflow-versus-pressure difference curve to determine whether the fan will provide adequate cooling in your application.

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Spreadsheet converts sound levels

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As everyone who attempts to get someone's attention from a distance intuitively knows, sound level decreases as the distance between the source and the detector increases. For distances less than 50 ft, the rule of thumb states that sound level drops 6 dB for every doubling of the distance between the sound source and the detector.

If your work involves generation of audible signals, the rule of thumb may appear simple, but putting it into practice takes valuable time to ensure that you correctly calculate the conversion. To complicate matters, there's no standard single distance for measuring sound level, and thus conversion of sound levels for different separations or between metric- and nonmetric-measurement units requires rethinking and recalculation.

For example, if an audible signal source measures 90 dBa at a distance of two feet, what's the equivalent sound level at a distance of 10 cm? If you can perform this conversion without putting pencil to paper, you're several steps ahead of your competition. To ease sound-level conversions, you can use an Excel spreadsheet (available for downloading at the online version of this Design Idea at www.edn.com). You enter a sound level in decibels acoustic, and the calculation returns sound levels for various commonly used measurement distances.□

Edited by Brad Thompson

Interrupt-driven keyboard for MCS-51 uses few components

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Designers of microcontroller-based products that require a keypad for user data entry can select from dedicating an input line for each key, continuously polling the keypad's x and y lines, or generating an interrupt whenever a user presses a key. Although conceptually simple, dedicating lines to a keypad can tie up most of the microcontroller's I/O resources. Continuously polled keypads can burden the microprocessor's resources and consume excessive amounts of battery power.

The third method, an interrupt-driven keypad, offers several benefits. First, using interrupts frees the microcontroller to perform other tasks or to switch into an idling or power-down mode while awaiting the next key closure. Second, using interrupts helps reduce electromagnetic interference produced by continuously scanning the keypad's lines. **Figure 1** shows an interrupt-driven keypad implementation that's based on Atmel's AT89C52 version of the popular MCS-51 family of microcontrollers. Here, the rows of a 16-key keypad, S_1 through S_{16}, implemented as a 4×4-key matrix connect to the lower nibble (P1.0 to P1.3) of IC_1's Port 1. The keypad's columns connect to IC_1's Port 1 upper nibble (P1.4 to P1.7) and a network of four diodes (D_1 through D_4) and a 10-kΩ resistor, R_9. The junction of R_9 and the diodes' anodes connects to Port Pin 3.2 and generates an interrupt whenever the user presses a key.

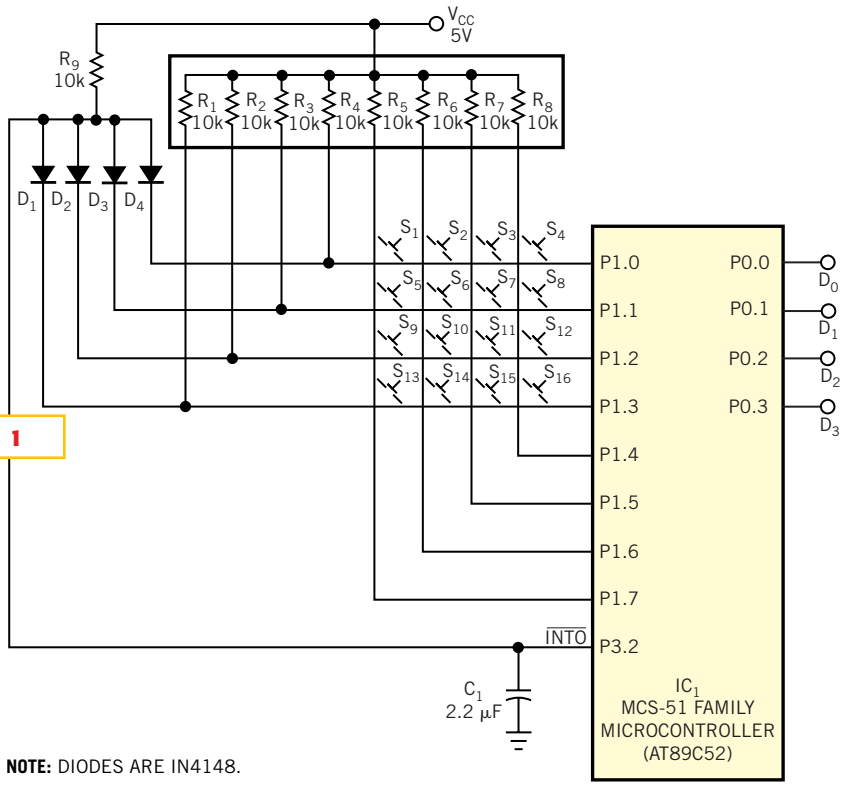

Figure 1

NOTE: DIODES ARE IN4148.

Adding an interrupt-driven keypad to an MCS-51 family microcontroller requires only a few components.

Initially, Port 1's lower nibble sits high at logic one, and the upper nibble is grounded at logic zero, applying reverse bias to the diodes and pulling the $\overline{\text{Int0}}$ signal high. Pressing a key applies forward bias to the diode corresponding to that row and causes $\overline{\text{Int0}}$ to go low, generating an external interrupt to the microcontroller. Upon receiving an interrupt and after a 20-msec software-debouncing interval, the microprocessor sequentially reads the row and column lines. Capacitor C_1 provides a hardware-based debouncing interval of approximately 25 msec.

In this design, the microcontroller's software returns a binary-formatted input corresponding to the pressed key's number as sensed at Port P1 (P1.0 to P1.3). As the commented assembly-language routine, available with the online version of this Design Idea at www.

edn.com, explains, the software ignores invalid key combinations. Idle and power-down modes available in CHMOS (complementary high-density MOS) versions of the MCS-51 family save power and thus make these microcontrollers ideal choices for battery-operated devices. For example, a 5V, 12-MHz Atmel AT89C52 consumes approximately 25 mA in active mode, 6.5 mA in idle mode, and only 100 µA in power-down mode. Any enabled interrupt can switch the microprocessor from idle to active modes.

However, recovery from power-down mode to active mode normally requires a hardware reset—an apparent limitation of the MCS-51 microcontroller. However, an earlier Design Idea overcomes the problem and allows use of an interrupt-driven keypad even in hardware-reset-based systems (**Reference 1**).□

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Simplified white-LED flasher operates from one cell

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THE WHITE-LED FLASHER in **Figure 1** offers an alternative approach to a previously published idea (**Reference 1**). Targeting use in portable appliances and products powered by a single cell, this circuit flashes an LED to provide a highly visible warning signal—for example, to indicate power on, battery low, or another eye-catching visual signal. However, white LEDs typically present a forward-voltage drop of 3 to 5V. Given that a single cell's end-of-life output voltage decreases to 1V, flashing a white LED from such a low voltage demands special circuit techniques. The circuit in **Figure 1** exploits the low-voltage capabilities of Fairchild's universally configurable two-input NC7SV57 logic gate. The NC7SV-57 operates from a supply voltage as low as 0.9V, a key requirement for single-cell applications.

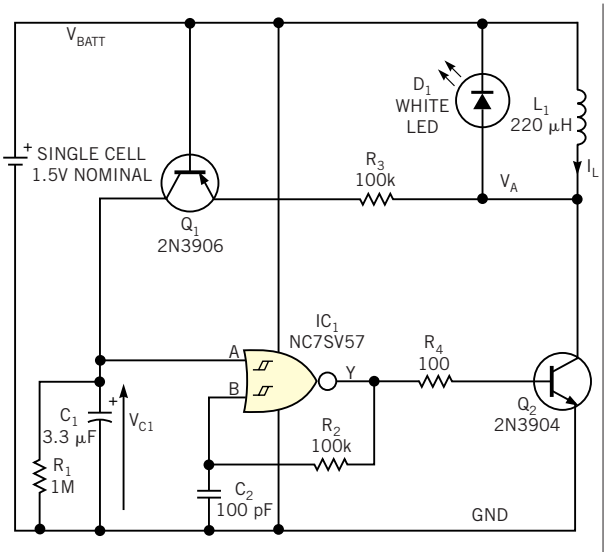
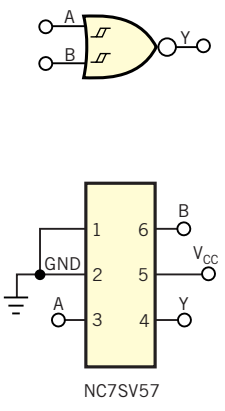


Figure 1 A few inexpensive components can light a white LED from a single primary cell.

Figure 2



Connecting pins 1 and 2 to ground configures the NC7SV57 as a two-input NOR gate.

Available in a six-lead SC70 package, this IC features Schmitt-trigger inputs. You can configure the device to implement AND, NAND, NOR, Exclusive-NOR, and invert logic functions. Connecting the pins as in **Figure 2** produces a two-input NOR gate. Upon initial power application, capacitor C_1 is uncharged, and its voltage, V_{C1}, is 0V. With C_1 holding Input A low, IC_1 temporarily becomes an inverter and forms a simple astable relaxation oscillator at a frequency that C_2 and R_2 determine. The square-wave signal at IC_1's output drives switching transistor Q_2.

When IC_1's output pulses high, Q_2 turns on and saturates, sinking current, I_L, through inductor L_1. The inductor current ramps up at a rate determined mainly by V_{BATT}; L_1's inductance; and Q_2's on-time, t_{ON}. During this interval, LED D_1 and Q_1's base-emitter junction are reverse-biased. Provided that the inductor does not saturate, current I_L ramps up linearly and reaches a peak value, $I_{L(PEAK)}$ at the end of the on-time.

When IC_1's output goes low and Q_2 turns off, L_1 generates back EMF to forward-bias D_1 and raises its anode voltage, V_A, to a value greater than V_{BATT}. Current circulates through L_1 and D_1 and ramps down to zero as L_1's stored energy decays. Values of 100 pF for C_2 and 220 kΩ for R_2 set the astable oscillator's frequency at approximately 20 to 30 kHz. On each cycle, a current pulse with a peak value, $I_{L(PEAK)}$, flows through the LED. Due to the high repetition frequency and persistence of vision, the LED appears to be continually on.

Without Q_1 and R_3, the astable circuit would oscillate without interruption and continuously illuminate the LED. However, Q_1 and R_3 provide a charging path for C_1. On any cycle of the astable square wave during which V_A rises above V_{BATT}, Q_1's base-emitter junction becomes forward-biased via R_3, allowing a pulse of current to flow through Q_1 into C_1. The magnitude of this current pulse depends largely on D_1's forward-voltage drop and R_3's resistance. Each current pulse applied to C_1 slightly increases the capacitor's charged voltage. When the charged voltage eventually exceeds IC_1's upper input-threshold voltage, V_{TU}, at Input A, the astable oscillator shuts off, and IC_1's output goes low. In response, Q_2 and the LED turn off, and current pulses cease to flow through Q_1.

Next, C_1 discharges through R_1, and

V_{C1} decays at a rate that only the R_1-C_1 time constant determines. D_1 remains off until V_{C1} falls below the Schmitt trigger's lower threshold voltage, V_{TL}; astable oscillations recommence; and the LED again turns on and repeats the illumination cycle.

For the values of C_1 and R_1 in **Figure 1**, the LED's on-time is roughly proportional to R_3's resistance. A relatively small value produces a short "blink," whereas a higher resistance leads to an on-time of several seconds. The LED's off-time depends only on the values of C_1 and R_1. To ensure that V_{C1} can exceed IC_1's upper input-threshold voltage, R_1's resistance must exceed R_3's resistance.

You can use a small-signal pnp transistor with good current gain for Q_1, because its specifications aren't critical. However, to ensure that most of the battery voltage appears across L_1 when Q_2 conducts, use a switching transistor with low collector-emitter saturation voltage for Q_2. If the saturation voltage is low enough to neglect, you can calculate the peak current in L_1 using $V_{BATT} \times t_{ON}/L_1$. The LED's intensity is proportional to its average forward current and thus determined in part by $I_{L(PEAK)}$. For optimum LED brightness, select the on-time and L_1 to maximize $I_{L(PEAK)}$ but not to exceed D_1's and L_1's maximum current ratings. The actual value of L_1 isn't critical, but values of 100 to 330 µH provide good performance and reasonable efficiency.

For large values of C_1, R_1, and R_3, the LED flashes at a fairly slow rate. With values of 3.3 µF for C_1, 1 MΩ for R_1, and 100 kΩ for R_3, the circuit produces a flash rate of approximately 0.4 Hz with V_{BATT} of 1.6V. Reducing V_{BATT} to 0.8V results in little flash-rate variation. At V_{BATT} of 1.6V, the LED delivers brightness that remains even when battery voltage decreases to 0.8V. The circuit continues to operate when V_{BATT} decreases to 0.65V, although the LED dims considerably at that level.

The NC7SV57's guaranteed operating voltage ranges from 0.9 to 3.6V, which allows operation from one or two alkaline or rechargeable nickel-cadmium cells or from a single 3V lithium cell. Texas Instruments' SN74LVC1G57 offers the same logic functions but operates over a slightly higher supply voltage range of 1.65 to 5.5V. To eliminate flashing operation, simply omit C_1, R_1, R_3, and Q_1. To turn the LED on or off, you can apply a gating signal to IC_1's Input A.□

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Low power voltage-to-frequency converter makes a wireless probe for testing an inductive power supply

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POWERING PORTABLE telemetry systems for long-term monitoring presents interesting design challenges. Batteries are unsuitable for certain critical applications, and, in these circumstances, designers typically use wireless inductive links to transmit both power and data. An inductive link comprises an RF transmitter that drives a fixed primary coil, and a loosely coupled secondary coil that supplies power to the portable circuitry. For design engineers, measuring transmitted power takes on considerable importance because it imposes limits on the amount of circuitry that designers can include in the portable circuitry. Unfortunately, classical test equipment is poorly suited to the task. Standard voltage probes pick up noise that the primary coil induces, and, in some applications, the portable circuits are hermetically encapsulated in small enclosures that prevent entry of a cable or a probe.

The circuit in **Figure 1** reduces noise effects because its VFC (voltage-to-frequency converter) produces a PPM (pulse-position-modulated) output signal, V_{OUT}, that integrates, or averages, noise. In addition, the design uses "load modulation" to eliminate wired connections. When the PPM signal drives on MOSFET switch Q_1, the switch connects an additional loading network comprising D_2 and the series combination of R_{SF} and R_{SV} across the secondary coil, L_S. A load-modulation receiver connects to the primary coil and recovers the PPM signal. When you build it with surface-mounted components, the VFC circuit occupies a board area of only 238 mm^2.

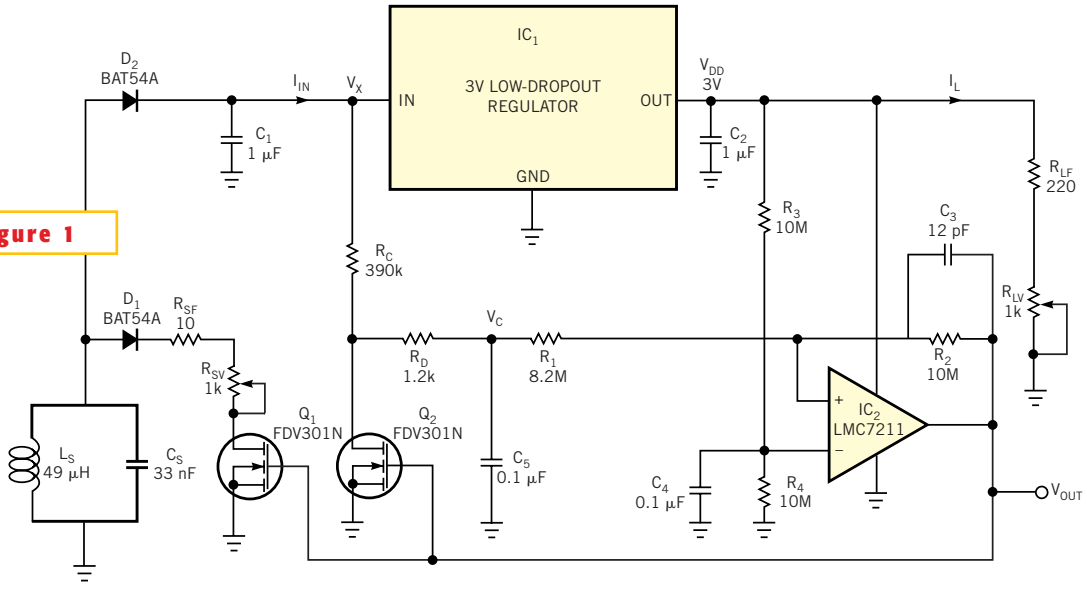
To understand the circuit's operation, assume that a 125-kHz sinusoidal magnetic field induces approximately 4 to 16V in secondary coil L_S. To improve power-transfer efficiency, L_S and C_S form a tuned, 125-kHz tank circuit having a loaded Q factor, Q_L, of approximately 8. Schottky diode D_1 rectifies the voltage induced in L_S, and C_1 provides lowpass filtering. The resultant dc voltage, V_X, powers low-dropout regulator IC_1, which supplies a constant 3V to VFC IC_2 and the load resistors, R_{LF} and R_{LV}. Trimmer potentiometer R_{LV} sets the output current at 2.5 to 13.5 mA.

The combined total current drain of the low-dropout regulator and the VFC measures a few tens of microamperes and is negligible compared with the output current. Hence, I_{IN} approximately equals I_L. **Equation 1** expresses the dc output power that the inductive power supply produces:

$$P_X \approx V_X \times I_L = V_X \frac{3V}{R_{LF} + R_{LV}}. \qquad (1)$$

This **equation** shows that the output current is constant and therefore the dc output power, P_X, is proportional to the dc voltage, V_X. After setting a known initial output current adjustment via R_{LV}, you can test the inductive power supply's

Figure 1



A low-power VFC and load modulator measure power generated by a wireless-telemetry power source.

output ability by measuring the transmitted dc voltage that the VFC digitizes. To minimize power consumption, component count, and pc-board area, a simple passive integrating network comprising R_C, R_D, and C_5 replaces the classical op-amp integrator that constitutes a typical VFC's input stage.

The VFC generates a constant-amplitude sawtooth voltage whose rising slope is proportional to V_X across integrating capacitor C_5. When the capacitor's voltage reaches a high reference voltage, switch Q_2 rapidly discharges the capacitor to a low reference voltage. This action produces a free-running waveform whose frequency is proportional to the input voltage, V_X. A noninverting Schmitt trigger comprising comparator IC_2; its positive-feedback network, R_1, R_2, and C_3; and supply-voltage splitter R_3, R_4, and C_4 defines the high- and low-level reference voltages, as **equations 2** and **3** calculate.

$$V_{TH} = \frac{V_{DD}}{2}\left(1+\frac{R_1}{R_2}\right), \quad (2)$$

$$V_{TL} = \frac{V_{DD}}{2}\left(1-\frac{R_1}{R_2}\right). \quad (3)$$

Equation 3 shows that, to reset the integrated voltage almost to 0V, the value of R_1 must be slightly lower than that of R_2. Using standard values of E12-series resistors and taking into account power-consumption constraints, select a value of 8.2 MΩ for R_1 and 10 MΩ for R_2. Replacing these values in **equations 2** and **3** yields, respectively:

$$V_{TH} = 2.73V \approx V_{DD};\ V_{TL} = 0.27V \approx 0V. \quad (4)$$

To understand the VFC's operation, assume that, at start-up, capacitor C_5 is fully discharged. Consequently, comparator IC_2's output, V_{OUT}, is low and MOSFET switches Q_1 and Q_2 are off. Under these conditions, current through R_C and R_D begins to charge C_5 toward V_X with a time constant of $\tau_C=(R_C+R_D)\times C_5$. When capacitor C_5's voltage reaches the Schmitt trigger's upper threshold voltage at time t_X, the comparator's output, V_{OUT}, rises to V_{DD} and turns on MOSFET switches Q_1 and Q_2. Switch Q_2

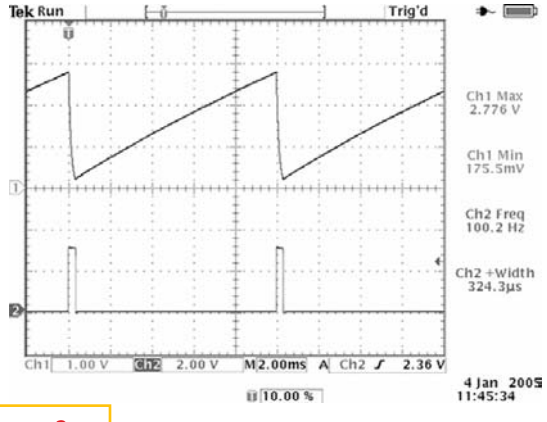
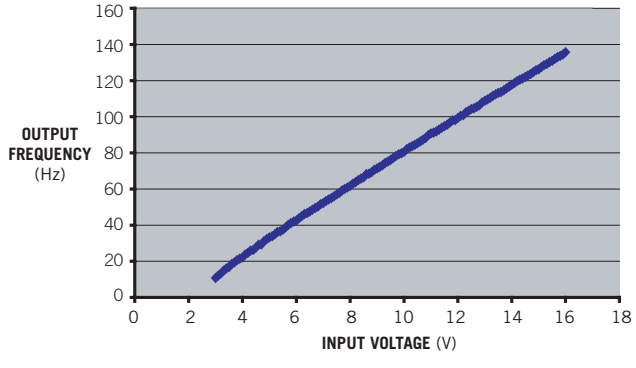


Figure 2

Oscilloscope measurements of the VFC show voltage across capacitor C_5 (upper trace) and comparator IC_2's output voltage, V_{OUT} (lower trace), for a nominal input voltage of 12V.

Figure 3



The measured transfer function of the VFC exhibits excellent linearity over a wide range of inductively coupled input voltages.

discharges C_5 through R_D at time constant of $\tau_D \simeq R_D \times C_5$. Simultaneously, Q_1 generates a load-modulation pulse.

When $V_C = V_{TL}$, the comparator's output drops to zero, restores the initial state, and repeats the sequence. As Trace 1 in **Figure 2** shows, the circuit behaves as a free-running oscillator in which the voltage across C_5 ramps up and down between the Schmitt trigger's threshold voltages. Given that the discharge-time constant, τ_D, is much less than the charging-time constant, τ_C, the discharge time, t_{ON}, is considerably shorter than the integrating time, t_X. As Trace 2 in **Figure 2** shows, the comparator's output delivers a PPM signal having a relatively short pulse of approximately 320 µsec.

Equations 5 and **6**, respectively, describe the complete expressions for calculating the pulse widths of waveforms t_X and t_{ON}:

$$t_X = (R_C + R_D) \times C_5 \times \log\left(\frac{V_X - \frac{V_{DD}}{2}\left(1 - \frac{R_1}{R_2}\right)}{V_X - \frac{V_{DD}}{2}\left(1 + \frac{R_1}{R_2}\right)}\right), \quad (5)$$

$$t_{ON} = R_D \times C_5 \times \log\left(\frac{R_2 + R_1}{R_2 - R_1}\right). \quad (6)$$

These formulas are useful for designing the VFC in **Figure 1** but yield little insight into the circuit's global-transfer function. You can apply the following approximations to simplify the calculations: Because $t_X >> t_{ON}$, the PPM output frequency is approximately $f_X \simeq 1/t_X$. In normal operation, V_X reaches relatively high values when compared with the Schmitt trigger's threshold voltages, and you can linearize the charging law of capacitor C_5 to a ramp having a constant slope (**Equation 7**).

$$\frac{dV_C}{dt} \approx \frac{V_X}{(R_C + R_D)C_5}. \quad (7)$$

According to **Equation 4**, the Schmitt trigger's high and low threshold voltages are, respectively, $V_{TH} \simeq V_{DD}$ and $V_{TL} \simeq 0V$. Using these approximations, the PPM output frequency simplifies to:

$$f_X \approx \frac{1}{(R_C + R_D) \times C_5} \times \frac{V_X}{V_{DD}}. \quad (8)$$

Equation 8 shows that the circuit in **Figure 1** exhibits a voltage-to-frequency transfer function, as **Figure 3** experimentally confirms. The VFC's power consumption is low; for example, at a dc voltage of 12V, the VFC's current drain is about 36 µA.□

Simple circuit converts 5V to −10V

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A typical switched-capacitor charge pump requires no inductors, is easy to design, and can double a positive voltage or convert a positive voltage to an equivalent negative voltage. However, in some applications, only a positive supply is available, and the power-supply system must generate a negative voltage of larger magnitude than the positive supply rail's voltage. The circuit in **Figure 1** simultaneously inverts its input voltage and doubles the resulting negative output.

Normally, the MAX889T voltage inverter, IC_1, converts a positive input to a negative output voltage with an absolute magnitude lower than that of its input. But, in this circuit, Schottky diodes D_1 and D_2 and capacitors C_4 and C_5 help produce a higher output voltage. The circuit's nominal output is $V_{OUT} = -(2 \times V_{IN} - 2V_D - I_{OUT} \times R_O)$, where V_{IN} is the input voltage, V_D is a diode's forward-voltage drop, I_{OUT} is the output current, and R_O is IC_1's output resistance in free-running mode. For a 300-µA load current, the circuit's output voltage is −10V. Parasitic inductances inherent in the capacitors and pc-board traces produce a voltage overshoot that charges the output capacitors, delivering more than −11V at no load (**Figure 2**).□

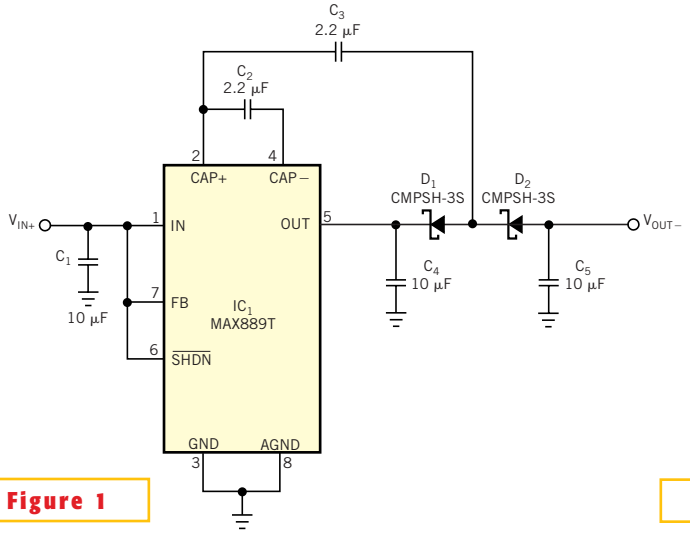

Figure 1

This switched-capacitor inverter derives −10V from 5V.

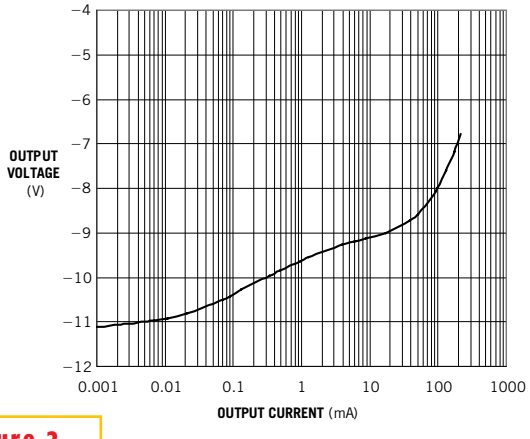

Figure 2

At light loads, the circuit in Figure 1 delivers more than −10V; at higher currents, the magnitude of the negative output voltage exceeds its positive input voltage of 5V.

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

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DIs Inside

Inrush limiter also provides short-circuit protection

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For containing large amounts of bulk capacitance, controlling inrush currents poses problems. The simplest approach involves placing an inrush-limiting resistor in series with the capacitor bank, but a resistor wastes power and adds a voltage drop. The circuit in **Figure 1** addresses these problems and provides an additional benefit. At start-up, bipolar PNP transistor Q_2 holds N-channel power MOSFET transistor Q_1 off until the voltage across capacitor C_1 reaches a high enough level to turn off Q_2. During this interval, resistor R_1 supplies C_1 and the rest of the circuit with start-up current. When Q_2 turns off, Q_1 turns on and provides a low-resistance path across R_1. When you shut off external power, the circuit resets as C_1 discharges.

As an additional benefit, this circuit provides protection against short-circuited loads. As current through Q_1 increases, the voltage drop across Q_1 increases due to Q_1's internal on-resistance. When the voltage drop across Q_1 reaches approximately 0.6V (Q_2's $V_{BE(ON)}$ voltage), Q_2 turns on, turning off Q_1 and forcing load current through R_1. Removing the short circuit restores normal operation, allowing Q_2 to turn off and Q_1 to turn on. Note that, because Q_1's on-resistance acts as a current-sense resistor for this function, the short-circuit trip point may vary depending on ambient temperature and Q_1's characteristics. You can adjust Q_1's turn-on and -off threshold by selecting R_1 and Q_1's on-resistance characteristic. Adding a conventional or zener diode in series with Q_2's emitter increases the short-circuit trip current.

The components and values for constructing this circuit depend on the application. Depending on the design requirements, you may need to select a high-power resistor for R_1 or add a heat dissipater to Q_1, but, for many applications, the circuit saves power over a conventional approach. EDN

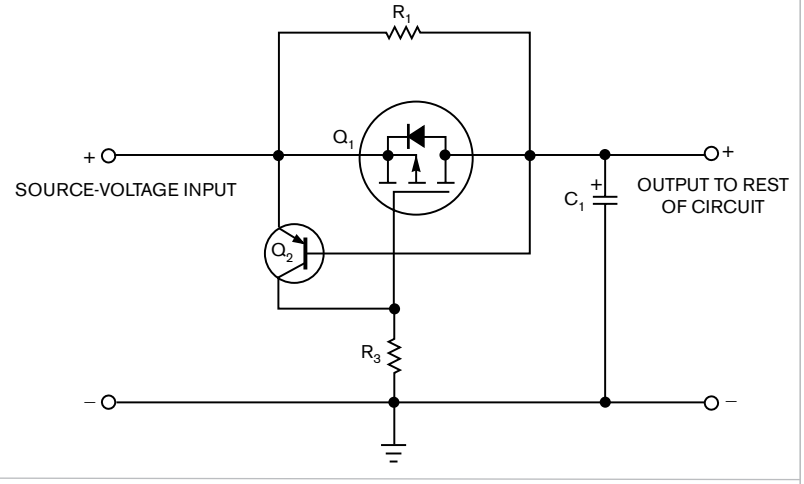

Figure 1 A power-MOSFET-limiting circuit restricts inrush current and protects against output short circuits.

Microprocessor-based dual timer features four outputs

Tito Smailagich, ENIC,
Belgrade, Yugoslavia

Based on Freescale Semiconductor's MCC908QY 8-bit flash-memory microcomputer, the circuit in **Figure 1** provides a low-cost, general-purpose dual timer that offers an alternative to one-shot circuits. You can modify the assembly-language software available from the online version of this Design Idea at www.edn.com/050609di2 to meet specific applications. The circuit uses microprocessor IC_1's internal 12.8-MHz clock oscillator. Internal division by four yields 3.2 MHz, which further divides by 64 with a timer prescaler to produce 50 kHz. A timer modulo counter divides by 50,000 to produce a 1-Hz timebase that generates a once-per-second real-time interrupt and master timing interval.

Two groups of four switches, S_3 through S_6 and S_7 through S_{10}, set time intervals t_1 and t_2, respectively, in increments of 1 to 16 sec. Although the **figure** shows individual DIP switches, you can also use hexadecimal-encoded rotary switches to set the

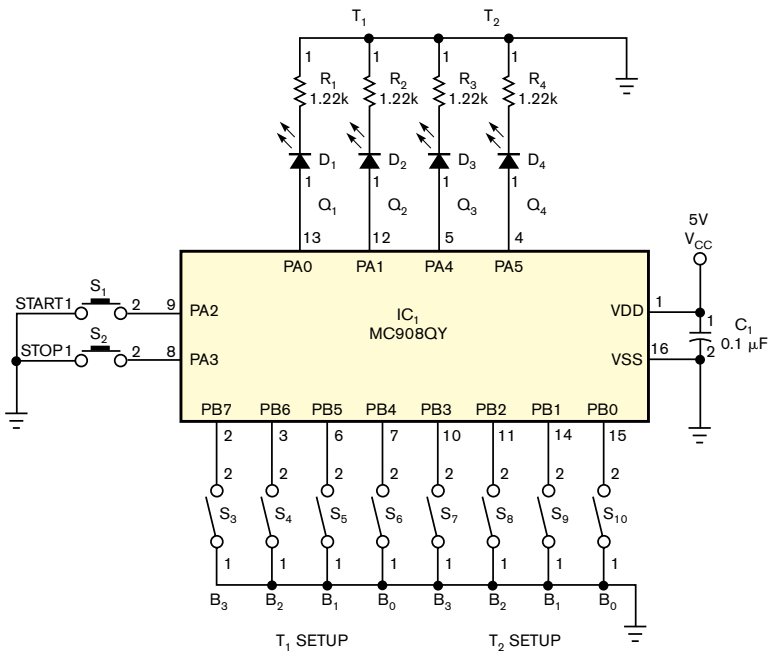

Figure 1 This dual timer comprises only a few switches and a microprocessor whose internal clock sets the time intervals.

time intervals. For demonstration purposes, LEDs D_1 through D_4 show the outputs' states during the timing cycle. Normally open pushbutton switches S_1 and S_2 start and stop the timers' operating cycles. The start function initiates the main timer and operates only when the timer stops. After activation, output Q_1 goes to logic one during interval t_1 (**Figure 2**). Output Q_2 complements Q_1 and remains at logic one until the next cycle starts. On Q_1's trailing edge, output Q_3 goes to logic one for time interval t_2. After t_2 elapses, output Q_4 goes to logic one and remains there until the next cycle starts. You can use the stop switch, S_2, at any time to terminate a cycle and reset all four outputs to logic one. EDN

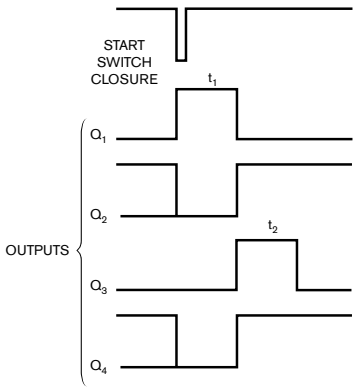

Figure 2 This timing diagram illustrates outputs available from the timer's two sections.

Wide-range voltage regulator automatically selects operating mode

Joel Setton, Crolles, France

The circuit in **Figure 1** delivers programming voltages to an EEPROM under the control of an external DAC (not shown). You can replace the DAC with a potentiometer to create a general-purpose power supply operating from 12V and able to deliver a variable output voltage of 0 to 32V. As **Figure 1** shows, a Linear Technology LT1072HV variable-boost switching regulator, IC_1, drives a Class A amplifier comprising operational amplifier IC_2, voltage-boost-stage Q_3, and emitter-follower Darlington transistor Q_2. Resistors R_9 and R_{10} set the amplifier's noninverting loop gain to a value of $1+(R_9/R_{10})$.

For output voltages below 8V, switching regulator IC_1 remains in shutdown mode, and the output stage draws current through L_1 and D_1. Q_1's collector voltage, V_C, measures approximately 11.4V—that is, 12V minus D_1's forward-voltage drop. Transistor Q_1 monitors the voltage drop across R_7, which measures a fraction of Q_2's collector-base voltage, V_{CB}. As long as V_{CB} exceeds 1V, Q_1's collector current remains high enough to drive IC_1's feedback input higher than 1.25V, which in turn keeps IC_1 shut down.

As the output voltage increases, the voltage differential across R_7 decreases, and, when it drops below 0.9V, Q_1's collector current decreases, lowering the feedback voltage applied to IC_1 and switching it on. The boost regulator's output voltage increases, and the Q_1-IC_1 feedback loop regulates the collector-emitter voltage differential across Q_2 to a constant 3V for all outputs exceeding 8V. If IC_2's output goes to ground, cutting off Q_3 and forcing Q_2 into saturation, the feedback loop around Q_1 opens and allows the circuit's output voltage to increase. Diode D_5 and associated components form an overvoltage-protection clamp that limits IC_1's output to 37V.

Resistive divider R_9 and R_{10} and IC_2 determine the output voltage's range.

Apart from selecting the V_{CE} ratings of Q_1 and Q_3 to withstand the highest desired output voltage, values of other components are not critical. If you substitute appropriate components for D_5, Q_1, and Q_3, the circuit can deliver output voltages as high as IC_1's maximum output-switch rating—75V for the LT1072HV variant—minus 3V. EDN

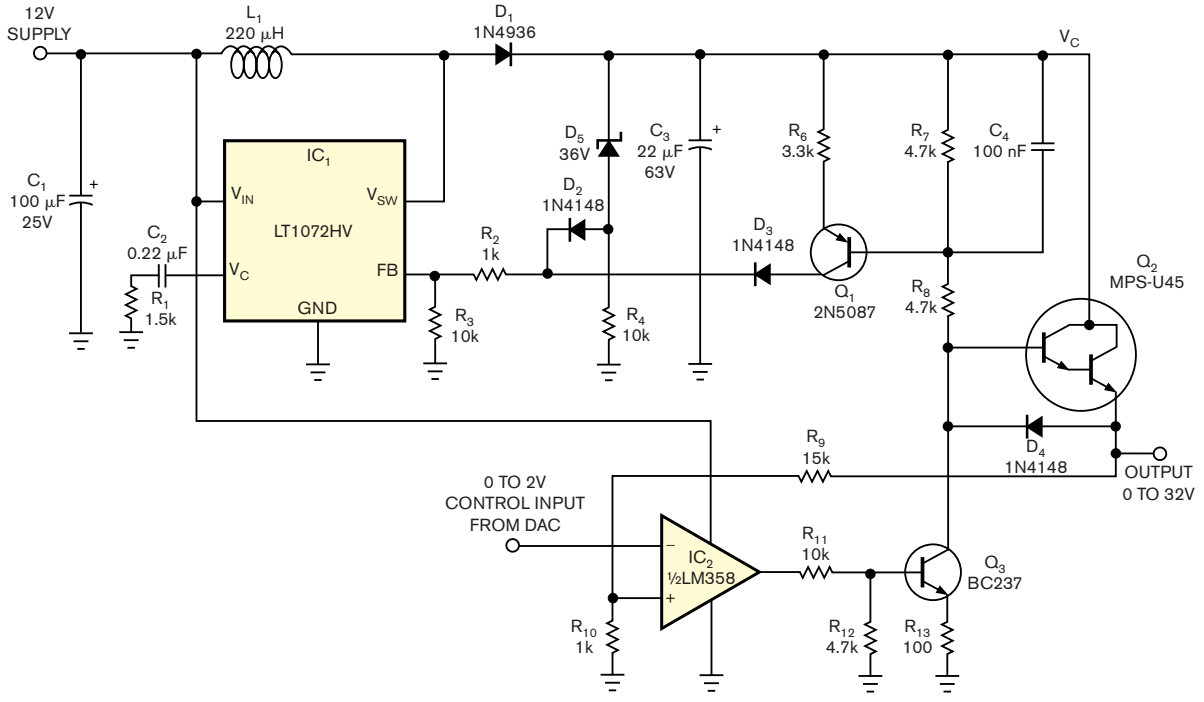

Figure 1 Able to deliver a wide range of output voltages, this regulator circuit automatically selects a linear or a switched mode as required.

CMOS hex inverter generates low-distortion sine waves

Al Dutcher, West Deptford, NJ

This Design Idea provides a simple, inexpensive, portable circuit as an alternative to a microcontroller to provide a wide-range source of low-distortion sine waves for audio-circuit design and debugging. Although sine waves from DDS (direct digital synthesis) offer greater stability and fewer harmonics and other spurious-frequency components, this more "retro" approach lets designers use Linear Technology Corp's LTSpice freeware and hone their circuit-simulation skills. An oscillator comprises a frequency-determining network and a method of limiting oscillation amplitude to prevent circuit saturation, waveform clipping, and the generation of harmonics. Many audio-oscillator designs use classic Wien-bridge bandpass-filter topology and include incandescent lamps, thermistors, or JFET circuits as amplitude-sensitive resistors to automatically vary feedback and limit amplitude.

However, amplitude-sensitive resistors introduce a small delay that can cause amplitude ringing while the oscillator stabilizes. In addition, the limiter's "soft" characteristics require frequency-determining components that track closely and maintain a level amplitude response over the oscillation range. Diode limiters present a softer characteristic than allowing an amplifier to go into "hard" limiting, and a diode limiter introduces no envelope delay. A Wien-bridge filter's frequency response rolls off relatively slowly and thus inadequately rejects clipping-induced harmonic frequencies. As a consequence, designers of most high-quality oscillators eschew the use of hard-clipping limiters.

Figure 1 shows a sine-wave-oscilla-

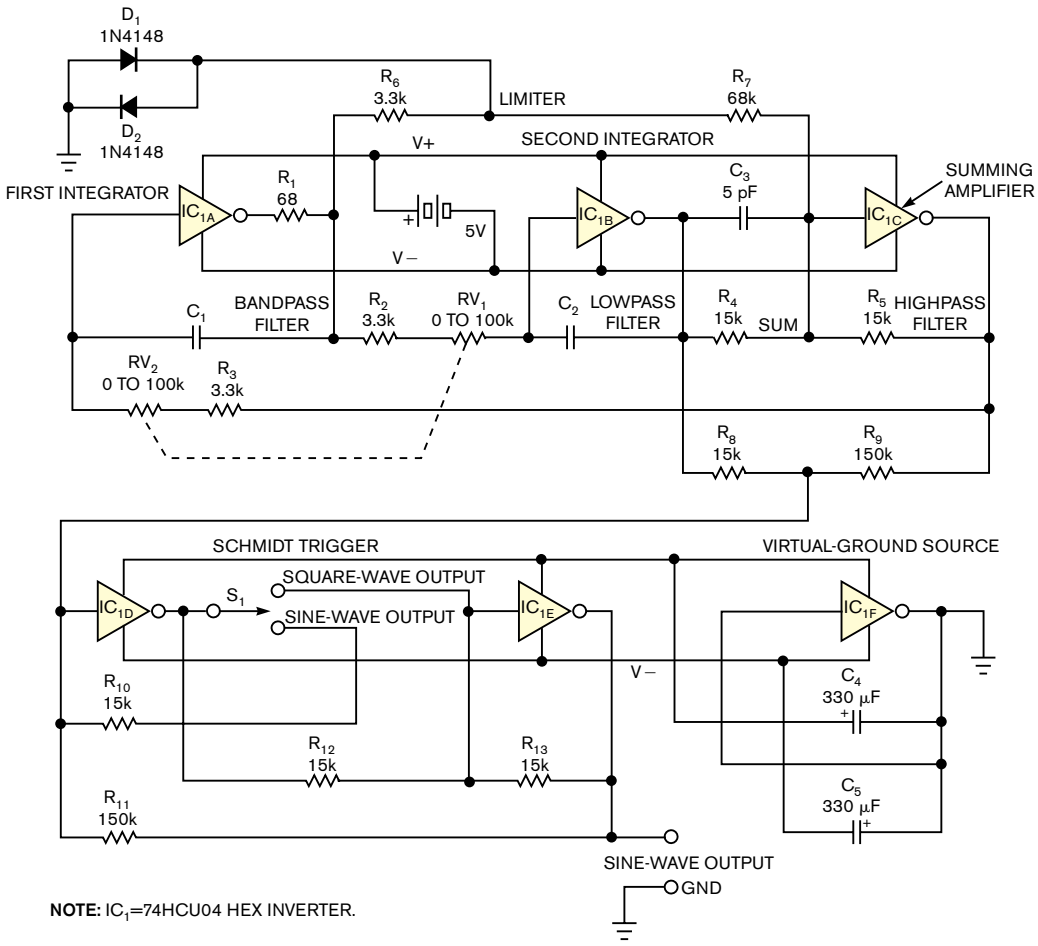

Figure 1 Build a sine-wave source around a single high-speed CMOS hex inverter and a handful of components.

tor design that makes unconventional use of a logic circuit. Based on state-variable topology that provides buffered highpass-, bandpass-, and lowpass-filtering nodes in one circuit, this oscillator relies on the peaking characteristics of an underdamped, two-pole lowpass filter that significantly boosts response at the fundamental frequency. In addition, the filter's lowpass node provides −12-dB-per-octave attenuation for harmonics. The state-variable loop comprises two integrators and a summing amplifier that provides 180° of phase shift. The two integrators each add almost −90° of additional phase shift, and the whole loop thus presents slightly less than 360 or 0° of phase shift and unity gain for oscillation.

The loop's gain blocks comprise unbuffered 74HCU04 CMOS inverters that emphasize circuit simplicity, wide bandwidth, and self-referencing logic thresholds. Individual inverters each provide relatively low-voltage gains of approximately 15 per stage. Operating in Class A linear mode, the inverters produce no crossover distortion and thus produce harmonic amplitudes that decrease rapidly with harmonic order. In addition, a 74HCU04 package contains six inverters, making possible a one-device oscillator circuit.

To understand how the circuit operates, use the summing node at IC_{1C}'s input as a phase reference. Summing amplifier IC_{1C} provides the first 180° of phase shift (inversion). Inverter/integrators IC_{1A} and IC_{1B} each present a quality factor, Q, equal to a gain of approximately 15, contributing a phase shift of −86° for a total of 180−86=94° each. The total phase margin for the three stages is 180+94+94=8° degrees. The circuit's phase shift now amounts to 8° away from the "perfect" 0° phase required for oscillation. The total circuit Q of approximately 7.5 provides a boosted fundamental-frequency-filtering action of approximately 17 dB, but, at 8° phase shift, the circuit does not oscillate.

To obtain the exact 360° phase shift for oscillation, apply a small amount of signal from the filter's bandpass tap, which operates at a phase angle of 180+180−86=−86°. Combine the circuit's Q of 7.5 and attenuate the bandpass intermediate output's signal at the bandpass filter by a factor of four,

and the circuit oscillates with adequate gain and phase margins. Due to its symmetric internal configuration, a CMOS-inverter circuit attempts to maintain a logic threshold of one-half of its supply voltage. However, an N-channel MOS transistor conducts more than its P-channel counterpart, and the logic threshold shifts slightly toward the negative supply rail. Because an imbalance would lead to asymmetry if you use it as is for limiting the oscillation's amplitude, a pair of back-to-back 1N4148 diodes, D_1 and D_2, serves as a symmetrical limiter, preventing the gates from clipping the bandpass filter's output.

Soft clipping eases the filter's performance requirements by producing a third-harmonic level of −17 dB at the clipper's output. The filter's response peaks at 17 dB at the oscillation frequency, and the lowpass node provides 20 dB of third-harmonic attenuation for a theoretical third-harmonic total rejection of −54 dB. In practice, the CMOS devices' gain and threshold characteristics depart from ideal performance, and, as a result, the circuit produces sine waves that approach 1% distortion at the lowpass node, an acceptable level for the intended application. Replacing the CMOS inverters with operational amplifiers would further enhance performance.

The filter's highpass node provides the first integrator's input signal, and the two cascaded integrators approach a 180° phase shift for all frequency components and also attenuate harmonic frequencies by a factor of $1/N^2$, where N represents the harmonic number. Subtracting some of the highpass signal, which contains harmonics produced by the diode limiter, from the lowpass signal further reduces the output's harmonic components. Resistors R_8 and R_9 form a 10-to-1 cancellation circuit that provides an additional 6-dB harmonic reduction for a 0.5% distortion figure at the signal output. **Figure 2** shows harmonic levels for a 500-Hz fundamental output frequency.

Oscillation occurs at unity gain at which the integrator's capacitive reactance equals the integrator's resistance, and at a frequency of $1/(2\times\pi\times R\times C)$, where $R = (RV_1+R_2)=(RV_2+R_3)$, and $C=C_1=C_2$. For C=10 nF and values of R of 8 to 80 kΩ, the circuit produces frequencies of 200 Hz to 2 kHz. You can use a 100-kΩ, dual-section ganged stereo-audio potentiometer as a frequency control. The control's ganged sections ensure that the integrators' resistance elements adequately track each other. To cover the audio spectrum of 2 Hz to 200 kHz, add a two-section band switch (not shown) to select pairs of capacitors with values of 1 µF, 100 nF, 10 nF, 1 nF, and 100 pF. You can use matched pairs of temperature-stable ceramic capacitors, but film-dielectric capacitors improve frequency stability. Compensation capacitor C_3 improves output flatness at higher frequencies. Over a typical frequency band, the output amplitude remains flat within 1 dB.

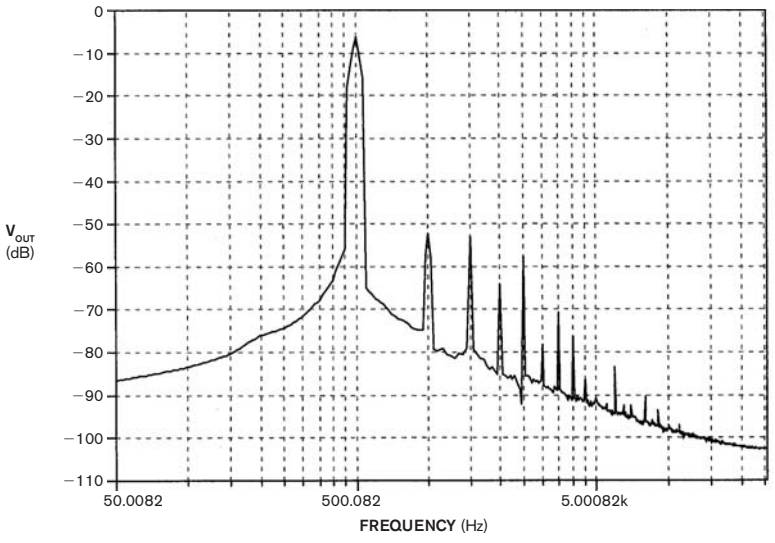

Figure 2 The oscillator's output spectrum contains second- and third-harmonic levels of at least 250 dB below the fundamental.

One of IC_1's three remaining inverters, IC_{1F}, serves as a virtual-ground generator by dividing the 5V power supply, a floating four-cell stack of AA-sized nickel-cadmium or nickel-metal-hydride batteries. Current drain from the batteries averages 50 to 60 mA. Switch S_1 connects the remaining inverters, IC_{1D} and IC_{1E}, to form a unity-gain buffer amplifier for sine-wave outputs or as a Schmidt trigger to produce a square-wave output. Resistor R_{11} sets the Schmidt trigger's hysteresis level. For ease of construction, use a perforated prototype board and the DIP version of the 74HCU04.

When you construct the circuit, note that the 74HCU04 can deliver appreciable gain at high frequencies, and excessively long leads can provoke parasitic oscillations that resistor R_1 helps suppress by reducing gain at frequencies in the very-high-frequency range. If you reduce circuit values, this oscillator easily operates in the high-frequency range, and, although its stability doesn't approach that of an LC-based oscillator, the circuit offers easy adjustment over a wide frequency range. EDN

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DIs Inside

Digital countdown timer may never need battery replacement

Mark E Buccini, Texas Instruments, Houston, TX

Comprising a microprocessor, an LCD, a 32.768-kHz crystal, and little else, the basic countdown-timer circuit in **Figure 1** operates from a commonly available CR2032 lithium-coin-cell battery. Based on the circuit's calculated current drain, the battery may never need replacement over a projected 10-year operational life. Careful selection of the battery and diligent exploitation of the microprocessor's low-power modes help minimize power consumption and thus maximize battery life. The coin-cell battery's size and flat form factor encourage miniaturization for portable-system applications. In addition, the lithium cell presents a flat voltage-versus-time discharge curve that allows direct drive of the LCD's segments to produce high contrast without additional compensation circuitry.

A typical CR2032 cell delivers approximately 200 mAhr of rated energy capacity. To achieve the design goal of 10 years of continuous operation, the system's average current consumption must not exceed 2.28 μA, which you calculate by dividing the battery's energy capacity by the system's operational life: 200 mAhr/10 years/365 days/24 hours=2.28 μA. A microprocessor from Texas Instruments' MSP430 family presents a low-standby-current demand of only 0.8 μA, which includes current drawn by its crystal oscillator, integrated LCD driver, and interrupt-driven wake-up timer. The 3½-digit LCD, a Varitronix model VI-302-DP, consumes an additional 1 μA. The total standby-current consumption for all active countdown-timer components is thus 1.80 μA.

In normal (standby) operation, the microprocessor's 32-kHz external-crystal clock drives an internal counter that generates an interrupt once per second. The interrupt awakens the processor, which executes an active main-software loop that decrements a countdown register via direct BCD (binary-coded-decimal) subtraction. Adding a value of 99 (decimal) to the countdown register and discarding the leftmost digit perform a one-digit subtraction. For example, 21+99=120; dropping the one in the 100s place yields a value of 20. As a bonus, this method directly displays the countdown register's contents on the LCD without requiring current-hungry binary-to-BCD conversions. (You can download the timer software's assembly-language listing from the online version of this Design Idea at www.edn.com/050623di1.)

As a final step, the main loop compares the countdown register's contents with zero to determine whether the preprogrammed time interval has expired. If so, the display flashes the time-out message. The main loop activates the CPU and its on-chip high-speed oscillator, which consume a total of 250 μA. Writing the software to execute 100 or fewer clock cycles—equivalent to 100 μsec at the default 1-MHz CPU clock frequency—reduces current demand. With such a short active period, the main loop's total current consumption is virtually negligible: Main loop=250 mA×(100/1 million)=0.025 μA.

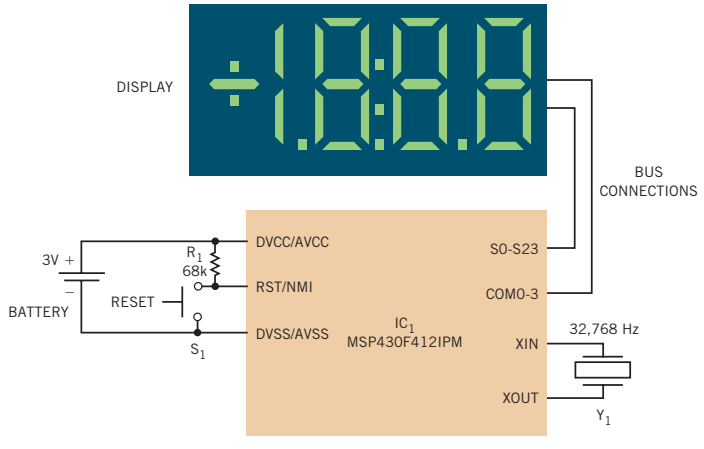

Figure 1 A half-dozen components are all it takes to build a battery-thrifty countdown timer.

Thus, total current consumption for the digital countdown timer is the sum of the standby- and main-loop currents: 1.8+0.025≃1.8 µA.

At approximately 1.8-µA average current consumption, the countdown timer easily meets the 2.28-µA design goal and ensures more than 10 years of continuous operation. Given the device's low current drain, a designer could reduce the timer's cost and complexity by packaging the circuitry along with a nonreplaceable battery. Many of the microprocessor's functions and I/O pins remain unused and available for additional features, and the compact firmware for implementing the counter occupies less than 250 bytes of 8 kbytes of available flash memory.

Applications for the circuit range from exercise-routine timing to a restaurant-service-guarantee timer. In such an application, the restaurant's greeter presses the timer's reset switch to reset the processor and start a preprogrammed countdown interval. If the time interval expires without the customer's being seated, the timer's display flashes to indicate that a guarantee of service went unmet. EDN

Wide-range regulator delivers 12V, 3A output from 16 to 100V source

Wayne Rewinkel, National Semiconductor, Schaumburg, IL

Synchronous buck regulators offer high efficiency and are popular in applications in which available input voltages are 12V or less. However, as input voltage approaches 100V, wide-range-regulator design becomes more difficult, and the choice of suitable ICs narrows considerably. This Design Idea combines a current-mode PWM IC for flyback-regulator circuits with a 100V gate-driver IC to produce a relatively high-performance synchronous buck regulator that can operate at inputs as high as 100V.

The circuit in **Figure 1** uses National Semiconductor's LM5020 current-mode PWM, IC_1, to drive an LM5104 gate driver, IC_2, forming a synchronous controller. The LM5020 contains an internal linear regulator that accepts input as high as 100V and can also deliver an output that can supply drive current to the LM5104. To reduce power dissipation at high input voltages, after initial power application, diode D_2, a 1N4148, supplies an 11.5V bootstrap voltage to the remainder of the circuit. Transformer T_1, a 100-to-1 current transformer from Pulse Engineering, provides current feedback during MOSFET Q_1's on-time. Q_1 and Q_2 are Siliconix Dpak devices, which have low gate-charge requirements and low on-resistances to minimize total switching losses at the circuit's 200-kHz operating frequency. All capacitors are of ceramic-dielectric construction to withstand high temperature and to meet packaging-size constraints.

For sustained operation at high input voltage, maximum current, and elevated-temperature conditions, transistor Q_1 requires an adequate heat sink or cooling airflow to maintain its junction temperature below the 175°C maximum specification. Q_1 has a low junction-to-case thermal resistance, and thus its case temperature must not exceed 160°C. L_1, the model DO5010 unshielded ferrite-core inductor from Coilcraft, presents a small pc-board footprint and offers a high saturation-current rating but represents this design's dom-

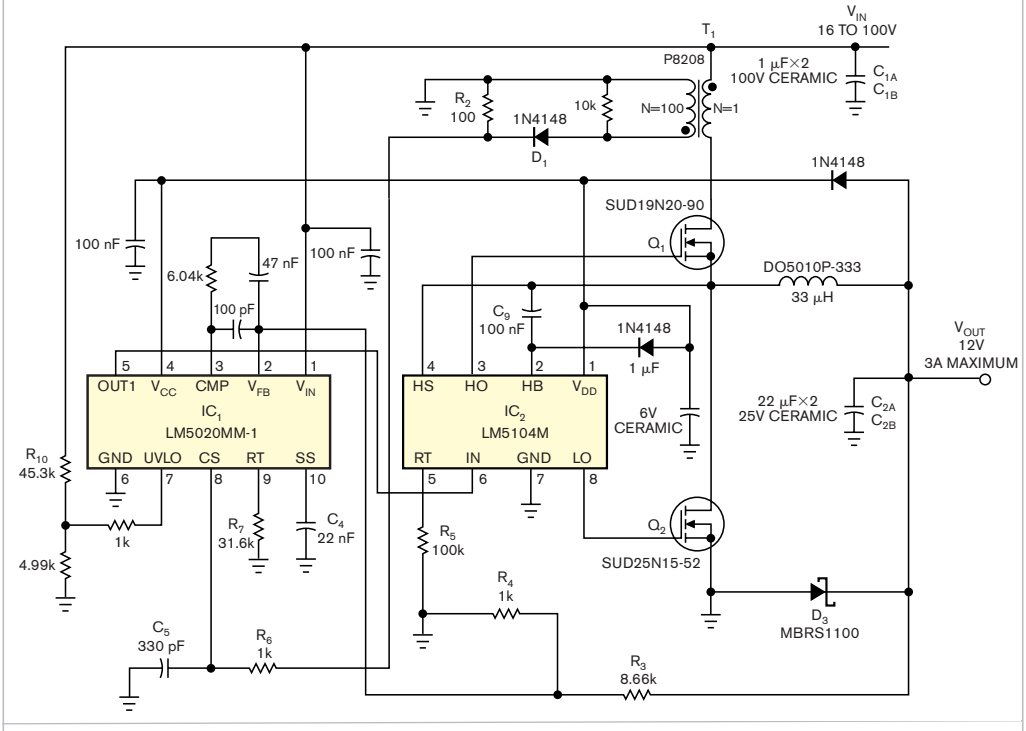

Figure 1 Two ICs and two MOSFETs form the heart of this high-efficiency, wide-range voltage regulator.

inant loss component. For applications with less critical space requirements, you can improve circuit efficiency by increasing L_1's inductance and size, thus reducing ripple current and enabling use of a larger core and increased winding-wire gauge. Reducing the output voltage improves efficiency, but, as output voltage drops below the circuit's 8V bootstrap voltage, IC_1 dissipates additional power and requires caution to avoid exceeding its ratings. **Figure 2** shows the circuit's measured efficiency versus output current for three input voltages.

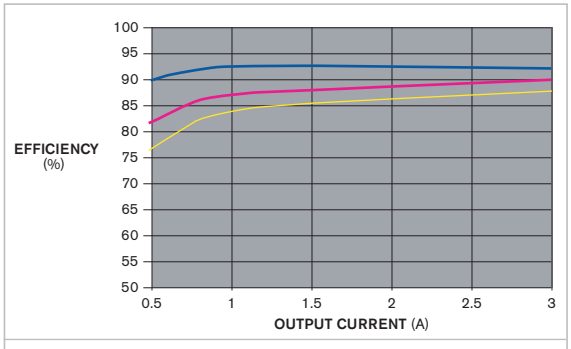

Figure 2 Circuit efficiency varies as functions of power-supply input voltage and load current.

One practical application for the circuit met a customer's requirement for a dc/dc converter that would operate from a 24V source and deliver 12V output at currents as high as 3A. This routine-sounding specification also requires operation in a physically and electrically harsh environment in which the packaged circuit resides on an engine block that reaches a temperature of 125°C, and ambient-air temperature reaches 100°C. In addition, the power source comprises two series-connected 12V batteries that provide a nominal voltage of 24V, which in practice varies from 18 to 40V and includes inductively induced load-dump voltage spikes that reach 100V. EDN

Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output

Jim McLucas, Longmont, CO

A recent Design Idea described a method for designing simple, high-frequency LC oscillators with few passive components (**Reference 1**). However, for best results, practical hardware design of a stable oscillator requires more parts and greater complexity. **Figure 1** shows a stable, 18-MHz oscillator with automatically leveled output amplitude control and an output buffer that delivers a sine wave with low harmonic content (**Reference 2**). In addition, this Design Idea replaces the original JFET oscillator with an inexpensive dual-gate MOSFET: an Infineon Technologies BF998, available from DigiKey and other sources.

The heart of the circuit comprises a Hartley oscillator, Q_1. To minimize loading, a 10-kΩ resistor couples the output from Q_1's source to the high-input-impedance gate of source follower JFET Q_2. In turn, Q_2 drives Q_3, a BJT (bipolar-junction-transistor) emitter follower, which in turn drives BJT amplifier Q_4. Toroidal-core transformer T_1 couples Q_4's output to a 50Ω load, delivering 2.61V p-p or 12.3 dBm. A Spice-circuit simulation predicts a second-harmonic amplitude of 35 dB below the fundamental. The second harmonic exceeds the amplitudes of all higher order harmonics, and an oscilloscope measurement displays a clean-looking sine wave across the 50Ω load.

To provide a good termination for the amplifier and still obtain 7.3 dBm (1.47 V p-p)—for example, to drive a diode-ring mixer—you can insert a 50Ω, 5-dB pad between output transformer T_1 and the load. Potentiometer R_2 adjusts the RF output level, and, for increased stability, you can replace R_2 with a fixed resistive divider built with low-temperature-coefficient, metal-film, fixed resistors. Part of the signal at Q_4's collector drives the gate of JFET source follower Q_5 through C_7 and R_9. Diode D_1 rectifies the signal, which, after filtering, feeds operational amplifier IC_1's inverting input. Resistor R_1 and low-temperature-coefficient potentiometer R_2 divide the 12V supply to produce a dc reference voltage for IC_1's noninverting input and set the output signal's level. After filtering, IC_1's dc output drives Q_1's Gate 2 to set the device's gain and thus control RF output.

Connected to the center tap of coil L_1, trimmer capacitor C_{18} allows fine adjustment of the oscillator's frequency. If decreased frequency stability is acceptable, you can replace C_{18} with a low-cost ceramic trimmer. Piston-type trimmers are rather expensive and less available than ceramic trimmers, but a typical ceramic trimmer exhibits a temperature coefficient that's at least an order of magnitude worse than a piston trimmer's. To operate the oscillator at a frequency other than 18 MHz, multiply the inductance of L_1 and the capacitances of C_{12}, C_{13}, C_{16}, C_{17}, and C_{18} by $18/f_{OSC2}$, where f_{OSC2} is the new frequency in megahertz. Adjust the tap for Q_1's source connection so that it remains at about 20% of the winding's total number of turns as counted from the inductor's grounded end.

You can replace the series combinations of C_{12} and C_{13} with a 13-pF capacitor, and you can replace C_{14} and C_{15} with a 2.5-pF capacitor. If you redesign the circuit for a different frequency, adjust the values of C_{14} and C_{15} or their single-capacitor replacement for just enough capacitance to ensure reliable start-up under all anticipated operating conditions. Also, note that using two capacitors for C_{16} and C_{17} helps reduce start-up drift, as does

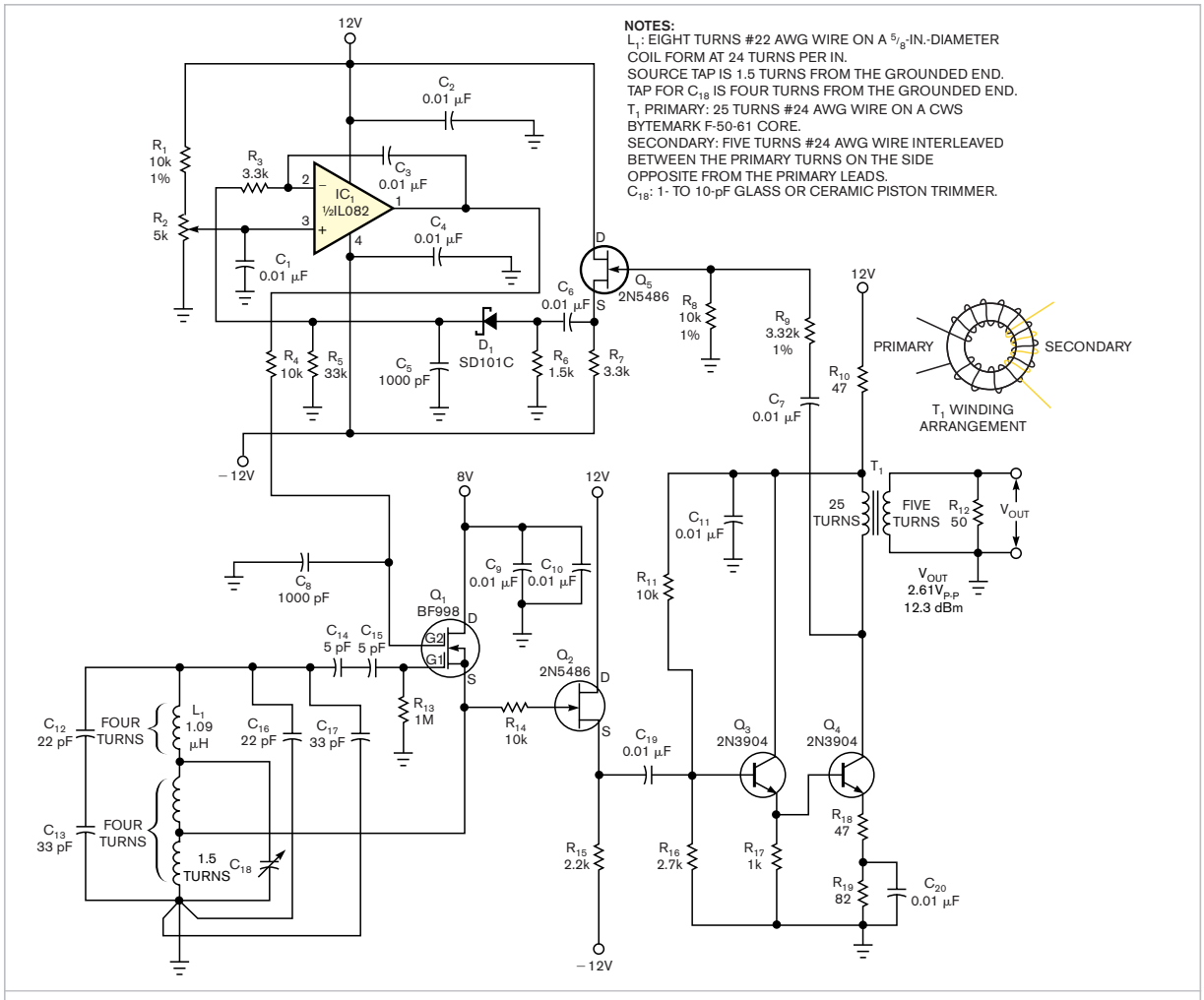

Figure 1 This low-distortion, 18-MHz oscillator offers high stability and automatic output-level control.

using temperature-stable (NP0-characteristic) ceramic-dielectric capacitors for C_{12} through C_{17}. The buffer amplifier, Q_2 through Q_4, requires modifications for operation at frequencies above approximately 25 MHz.

A well-regulated external dc source (not shown) provides 12, −12, and 8V to the circuit. To maintain high stability and remain within Q_1's 12V maximum drain-to-source-voltage rating, the 8V supply powers only the oscillator. Using the specified components and at a constant ambient temperature of 22°C, after an initial 10-minute warmup period, the oscillator's frequency drifts at an average rate of −2 to −3 Hz per minute over one hour. EDN

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Ultra-low-noise low-dropout regulator achieves 6-nV/√Hz noise floor

Ken Yang, Maxim Integrated Products Inc, Sunnyvale, CA

Many low-dropout-voltage regulators see service in electronic systems, but relatively few are designed for low-noise operation. (For example, Maxim's MAX8887 achieves a noise voltage of approximately 42 µV rms. However, certain applications, such as ultra-low-noise instrumentation oscillators, demand even lower levels of power-supply noise. To reach this level, the circuit in **Figure 1** combines low-noise components and extra filtering to achieve an output noise floor of only 6 nV/√Hz.

Voltage reference IC_1, a Maxim MAX6126, features low output noise. Lowpass filter R_1-C_1 further reduces this noise by attenuating noise frequencies

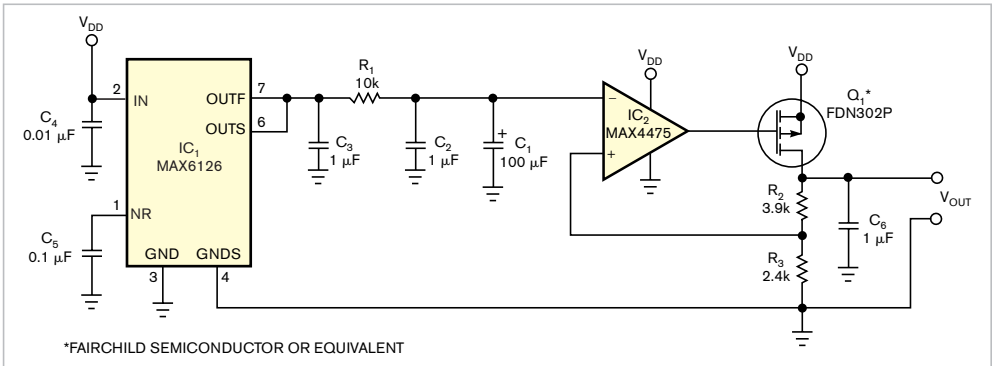

Figure 1 This low-dropout-voltage regulator features a noise floor of only 6 nV/$\sqrt{\text{Hz}}$, making it an ideal power source for low-noise oscillators.

above IC_1's 0.16-Hz cutoff frequency. The filtered reference voltage drives the inverting terminal of error amplifier IC_2, a Maxim MAX4475, which regulates the output voltage by means of Q_1, a P-channel power FET source follower. Feedback resistors R_2 and R_3 determine the output voltage as follows: $R_2=R_3[(V_{OUT}/2.048V)-1]$.

The simplified noise-analysis diagram illustrates the components' noise contributions (**Figure 2**). Lowpass filter R_1-C_1 attenuates high-frequency noise on the voltage reference's output. The op amp's noise current, 0.5 fA/$\sqrt{\text{Hz}}$, is negligible with respect to its voltage noise, 4.5 nV/$\sqrt{\text{Hz}}$. The reference-noise source adds to the op-amp voltage noise because they effectively connect in series. The MOSFET's noise contribution appears at Q_1's input.

The noise at IC_2's inverting terminal equals the noise at its noninverting terminal:

$$V_{N\_REF}H(f)+V_{N\_OPAMP}=V_{N\_OUT}\left(\frac{R_3}{R_2+R_3}\right),$$

and

$$V_{N\_OUT}=\left(V_{N\_REF}H(f)+V_{N\_OPAMP}\right)\left(\frac{R_2+R_3}{R_3}\right),$$

where V_{N_OUT} represents the low-dropout circuit's output noise, V_{N_REF} represents the reference noise, V_{N_OPAMP} represents the op amp's input-referred noise, and H(f) represents the R_1-C_1 lowpass filter's transfer function. If a noise frequency of interest falls well below the filter's cutoff frequency, the reference noise is negligible, and the low-dropout circuit's output noise comprises only the op amp's noise multiplied by the closed-loop gain. The feedback loop suppresses V_{N_FET}, the MOSFET's noise contribution, which therefore can't contribute to the output noise. For frequencies within the loop's bandwidth, the low-dropout circuit also rejects ripple and noise voltages that the power supply introduces.

Figure 3 shows a plot of noise density versus frequency for the circuit of **Figure 1**, which exhibits a noise floor of about 6 nV/$\sqrt{\text{Hz}}$ at 1 kHz. For comparison, the plot shows the noise-measurement instrument's noise floor and a typical low-dropout circuit's much higher noise density—for example, 500 nV/$\sqrt{\text{Hz}}$ at 1 kHz for the MAX8887 low-noise, low-dropout circuit. EDN

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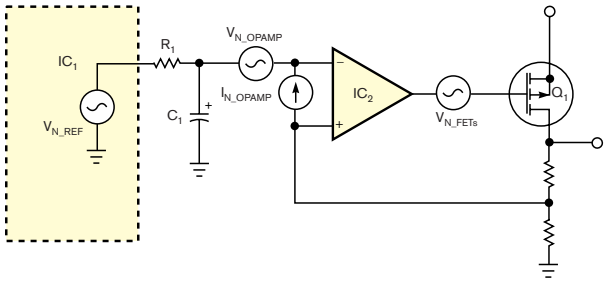

Figure 2 This simplified version of Figure 1 highlights noise sources for analysis.

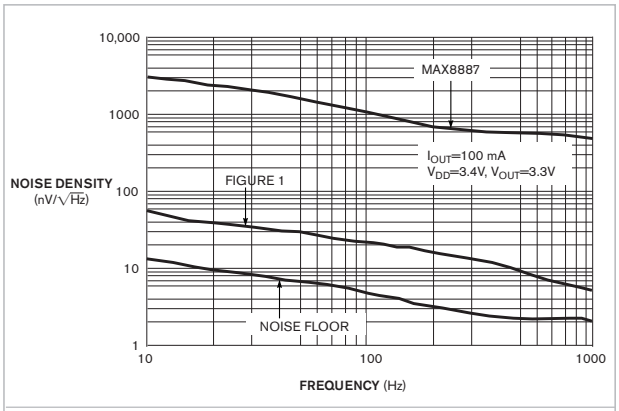

Figure 3 A noise-density-versus-frequency plot for the low-dropout circuit in Figure 1 is 38 dB lower than that of a conventional low-noise, low-dropout-voltage regulator—in this case, a Maxim MAX8887.

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READERS SOLVE DESIGN PROBLEMS

Contact-debouncing algorithm emulates Schmitt trigger

Elio Mazzocca, Technical Consultant, Adelaide, South Australia

Among other interface problems, contact bounce complicates the connection of mechanical contacts or any noisy digital input signal to a microcontroller. Although designers have proposed a variety of hardware and software approaches that address the problems that contact bounce poses, no one has yet claimed a definitive and predictably stable approach. (For a sampling of approaches, see **references 1** through **10**.) The usual hardware approach to eliminating contact bounce comprises an RC filter followed by a Schmitt trigger (**Figure 1**). You can extend the filter's effectiveness simply by increasing the RC time constant at the expense of increased response time.

Software-debouncing methods usually include 1-bit processing, which involves twice reading the contact's input state with a fixed delay between the two readings. You can also implement a state machine or launch an input signal through a shift register and wait for three or four register-output states that haven't changed. The low efficacy of 1-bit processing approaches stems from designers' erroneous assumptions that seemingly simple debouncing tasks can tolerate equally simple software. However, a detailed study of many types of contacts reveals a range of complex and sometimes unexpected behaviors. This Design Idea documents a more comprehensive method that can easily handle all mechanical contact interfacing to microcomputers.

The debouncing method applies full 8-bit-processing and digital-filtering techniques to digital inputs. Using as few as 20 assembly-language instructions that execute in 19 machine cycles on an ATmega8 microcontroller, the method produces a robust debouncing action (see **Listing 1** at the Web version of this Design Idea at www.edn.com/edn050707di1).

The software closely simulates the hardware circuit in **Figure 1** by using a first-order, recursive, digital lowpass filter followed by a software Schmitt trigger. In contrast to 1-bit software debouncers that generally do not apply processing to inputs, this debouncing algorithm is effective because it "remembers" past input transitions and assigns a "weight" to each transition depending on how long ago it occurred. Furthermore, you can alter the filter's settings on the fly to meet changing conditions by modifying its thresholds and hence its execution time, or time constant, from the main program. The basic recursion algorithm comprises present output value=(1/4)×input value+(3/4)×previous output value, or, $Y_{NEW}=(1/4)\times X_{NEW}+(3/4)\times Y_{OLD}$.

To avoid register overflow and instability, the value of Y_{OLD} and X_{NEW} must be less than 1, which for an 8-bit microprocessor translates to values of less than 256 for X_{NEW} and Y_{OLD}. Consequently, the input $(1/4\times X_{NEW})$ to the filter is either 0 or 63. You then apply the output value, Y_{NEW}, to the software Schmitt trigger. The trigger uses the following algorithm: If Y_{NEW}>hi, and flag=0, then flag=1, and out=1. If (Y_{NEW}<lo, and flag=1, then flag=0, and out=0.

Hardware Schmitt triggers typically have fixed thresholds of one-third and two-thirds of the power-supply voltage. However, the software allows widening these thresholds and thus increasing the filter's time constant. In operation, a timer-interrupt routine should execute the debouncing program every 4 to 5 msec. Becausee one time constant equals the period of one interrupt, using thresholds of 15 and 240 causes the routine's output to "trigger" after 11 interrupts, or 44 to 55 msec, which ade-

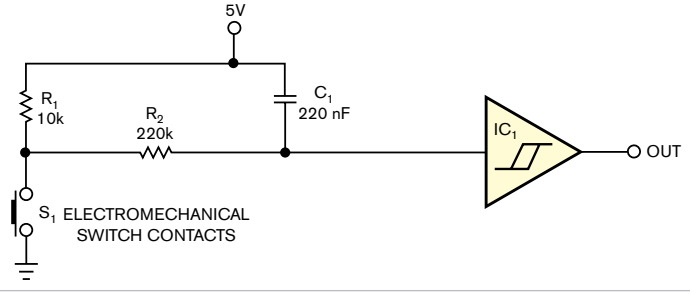

Figure 1 A basic switch-contact debouncer consists of an RC network followed by a Schmitt-trigger circuit.

DIs Inside

quately processes most switches' contact bounce.

You can easily modify the main filter coefficient to provide different filtering-time constants. For particularly troublesome contact bounce, you can use the following recursion formula, which requires 16 time constants to trigger the software Schmitt routine. $Y_{NEW}=(1/16)\times X_{NEW}+(15/16)\times Y_{OLD}$. You can implement this algorithm with only eight assembly-language instructions, whereas the Schmitt-trigger routine requires 12 instructions. When you combine both of these routines, the software Schmitt trigger updates bit 0 of a register, which the main program loop should continuously check to ascertain the contact's status. As an alternative, you can activate a software interrupt to signal a contact's status change. To do so in the AVR architecture, you write to that port bit that functions as an external interrupt input.

Always avoid connection of mechanical contacts to interrupt inputs unless the contacts undergo hardware debouncing. Otherwise, the contacts may bounce dozens of times, unnecessarily consuming processor-machine cycles. The software routine reads the inputs only every 4 msec and thus imposes additional filtering on the inputs. Simulation and practical testing have confirmed that the debouncing algorithm behaves as expected, producing clean output transitions when enduring noisy contacts. When you program the assembly-language source code accompanying this Design Idea into an Atmel Atmega8, the code turns on an output LED connected to Port_B bit 0 when Port_D bit 0 of the microcontroller goes to ground.

A simulated input waveform (pind0) and its corresponding output log file (portb0.log, both available at the Web version of this Design Idea at www.edn.com/050707di1,) illustrate the filter's excellent debouncing capabilities. Beginning with a key closure at 10 msec, the stimulus loads into the AVR Studio integrated development environment. After multiple input transitions, the output-log file shows a single output transition occurring at 55.333 msec. The software effectively filters out the three input pulses starting at 56.1 msec (**figures 2** and **3**). EDN

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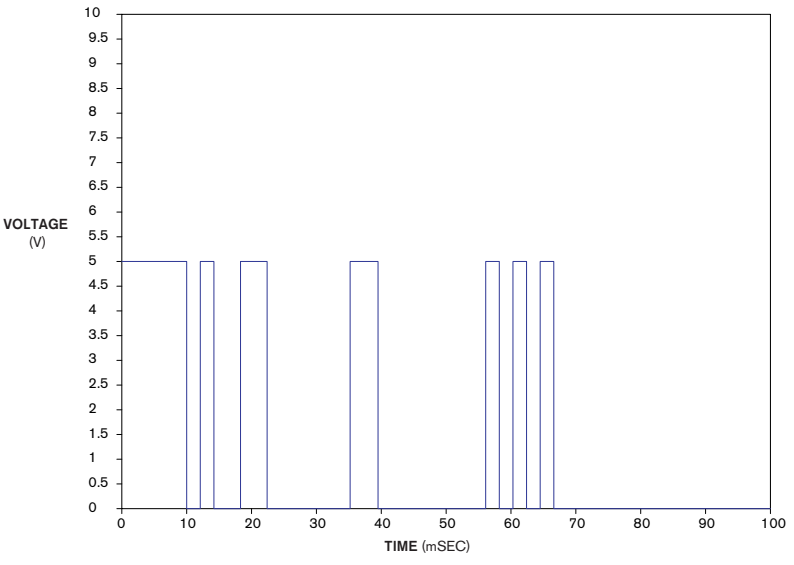

Figure 2 Switch contacts first close at 10 msec and then bounce erratically for more than 50 msec before reaching a stable closed condition.

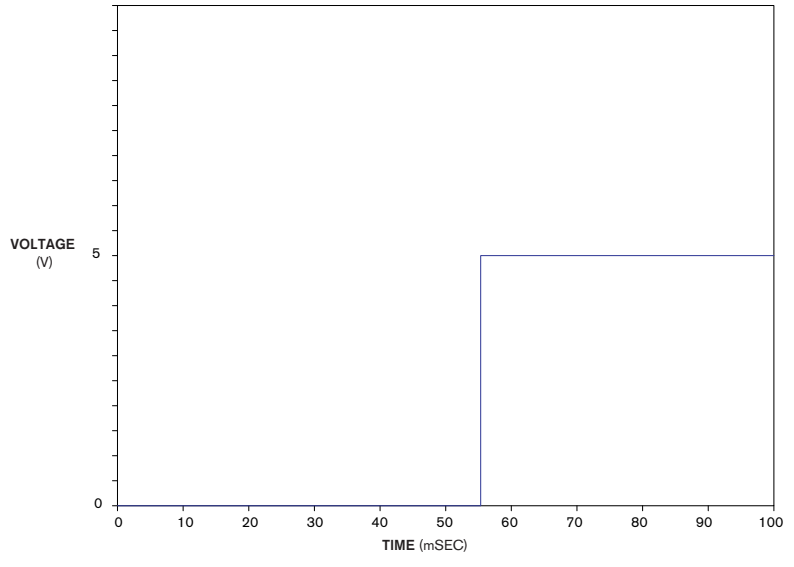

Figure 3 The debouncing-software routine signals that the contacts have closed only after bouncing ceases.

```
/*********************************************************************
**                                                                  **
**                     THE ULTIMATE SOFTWARE DEBOUNCER              **
**                                                                  **
** Program: debounce.asm                                            **
** Version: 1.0                                                     **
** Date:    5/5/2005                                                **
** Author:  Elio Mazzocca                                           **
** E-mail:  jnz9876@adam.co.uk                                      **
**                                                                  **
** micro used: ATmega8 with internal 4 MHz oscillator               **
** assembled with: AVR Studio 4.0                                   **
** Timer0 interrupt period: 4 mSEC                                  **
**                                                                  **
** Description: This is a 1st order recursive digital filter        **
**              with Schmitt trigger output that filters noisy      **
**              digital inputs to ATmega8 microcontroller.          **
**              The formula employed for the recursive filter:      **
**                                                                  **
**              ynew = 1/4 xnew + 3/4 yold                          **
**                                                                  **
**              Formula for an inverting Schmitt trigger:           **
**                                                                  **
**              if(ynew>hi) and (flag=0) then flag=1; vout=1;       **
**              if(ynew<lo) and (flag=1) then flag=0; vout=0;       **
**                                                                  **
** Use:         The code is placed in Timer0 interrupt routine      **
**              with a 4 mSEC period. The output of the trigger     **
**              is continuously checked in the main program loop    **
**              The interrupt routine checks the PORT bit and       **
**              applies either 0 (keypress) or $3F to the digital   **
**              filter, the output value is then applied to a       **
**              Schmitt trigger with thresholds of 15, 240 for      **
**              an effective "time constant" of 11 interrupts.      **
**              Program requires 11 ints, 19/18 machine cycles,     **
**              6 ints if schmitt threshold is $3C instead of $0F   **
**                                                                  **
** Input stimuli: pind0.sti                                         **
** Output log:    portb.log                                         **
*********************************************************************/
;
.NOLIST
.INCLUDE "AvrAssembler2\appnotes\m8def.inc"
.LIST

; Register defines

.DEF    yold = R17                      ; old/new filter output value, share same reg
.DEF    tmp  = R18                      ; new input to filter value/threshold reg
.DEF    flag = R19
.DEF    VOUT = R20

.CSEG
.ORG $0000
        rjmp    Reset

.ORG OVF0addr
        rjmp    tim0_ovf                ; Timer0 overflow handler

Reset:
        ldi     R16,    LOW(RAMEND)     ; Initiate Stackpointer
        out     SPL,    R16             ; for use by interrupts
        ldi     R16,    HIGH(RAMEND)
        out     SPH,    R16
```

```
        ldi     R16,    (1<<CS01)|(1<<CS00)  ; Fosc = 4 MHz
        out     TCCR0,  R16             ; set Timer/Counter0 Prescaler=64, int = 16x256
uSEC

        ldi     R16,    (1<<TOIE0)      ; set timer0 interrupt enable
        out     TIMSK,  R16             ; in the Timer Interrupt Mask Register
        ldi     R16,    (1<<TOV0)       ; clr pending interrupts
        out     TIFR,   R16

        ser     tmp
        out     DDRB,   tmp             ; set PORTB = output
        clr     tmp
        out     DDRD,   tmp             ; set PORTD = input
        ser     tmp
        out     PORTD,  tmp             ; turn on PORTD pull-ups

        ldi     yold,   $FF             ;optional
        sei                             ; enable interrupts
loop:                                   ; main program loop
        sbrs    VOUT,   0               ; if schmitt out = 1
        rjmp    a1
        sbi     PORTB,  0               ; then set PORTB, bit 0 - LED on
        rjmp    loop
a1:
        cbi     PORTB,  0               ; else clear PORTB, bit 0 - LED off
        rjmp    loop
;-----------------------------------------------------------------------
tim0_ovf:
        mov     tmp,    yold
        lsr     tmp
        lsr     tmp                     ; tmp = 1/4 yold
        sub     yold,   tmp             ; 3/4 yold is in left in reg yold
        ldi     tmp,    $3F             ; re-use tmp register for xnew
        sbis    PIND,   0               ; if PIND bit 0 = 0, then input = 1/4 xnew
        clr     tmp
        add     yold,   tmp             ; yold same as ynew, saves 1
instruction/register !

.UNDEF tmp                              ; re-use tmp register as threshold reg.
.DEF   thresh = R18
                                        ; now apply filter output to schmitt trigger
        ldi     thresh, $0F             ; load lo thresh into threshold register
        sbrc    flag,   0               ; test bit 0 of flag register
        rjmp    s1
        cp      yold,   thresh
        brsh    s1
        sbr     flag,   (1<<0)          ; set bit 0 of register flag
        sbr     VOUT,   (1<<0)
s1:
        swap    thresh                  ; to test hi thresh, swap nibbles
        cp      yold,   thresh
        brlo    s2
        cbr     flag,   (1<<0)
        cbr     VOUT,   (1<<0)          ; clear bit 0 of register VOUT
s2:
        reti                            ; 19/18 (nokeypress/keypress) machine cycles
;-----------------------------------------------------------------------
.EXIT
```

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Inexpensive peak detector requires few components

Anthony H Smith, Scitech, Bedfordshire, England

Requiring no rectifier diodes, the positive peak-detector circuits in **figures 1** and **2** exploit the open-drain output of a Texas Instruments TLC372 fast comparator, IC_1. Both versions of the detector are simple and inexpensive and provide a buffered, low-impedance output at V_{OUT}. In addition, the TLC372's high typical input impedance of $10^{12}\Omega$ eliminates any need for an input buffer stage. As **Figure 1** shows, the detector's output voltage at the output of op amp IC_{2A} applies a feedback signal for the comparator and acts as a reference level for comparison with the input signal's amplitude. Upon first application of input signal V_{IN}, the voltage on the hold capacitor, C_1, is 0V, and V_{OUT} is also 0V.

When the input signal goes more positive than the output voltage, the comparator's internal output MOSFET turns on and sinks current through R_1. Provided that R_2 is relatively large, charging current flows into C_1 from IC_{2A}'s output. Over several cycles of the input signal, the charge on C_1 builds up, and V_{OUT} rises to the point at which it slightly exceeds the peak level of V_{IN}. For as long as V_{OUT} is slightly greater than V_{IN}, IC_1's output MOSFET remains off, and C_1 receives no additional packets of charge.

As a consequence, the charge stored on C_1 starts to dissipate as the capacitor discharges through R_2 and through the bias-current path into IC_{2A}'s inverting input. V_{OUT} gradually falls until it is just below the peak level of V_{IN}. The next positive peak of V_{IN} trips comparator IC_1, which pulls current through R_1, "topping up" the charge on C_1. This process produces a dc level at V_{OUT} that closely approximates the positive peak level of the input waveform. The values of R_1, R_2, and C_1 determine the ripple voltage present on V_{OUT}.

IC_{2A}'s inverting input is held at virtual ground potential, so whenever IC_1's output MOSFET turns on, the voltage across R_1 approximately equals the negative-supply-rail voltage, $-V_S$. Therefore, using a small value of R_1 injects a relatively large pulse of current into C_1, thus allowing the circuit to respond quickly to a sudden increase in input-signal amplitude—that is, a "fast-attack" response. However, if the value of R_1 is too small, the positive-going ripple on V_{OUT} becomes excessive and can lead to bursts of oscillation around peak values of V_{IN}.

For a given value of R_2, the value of C_1 determines the circuit's "delay time."

(continued on pg 92)

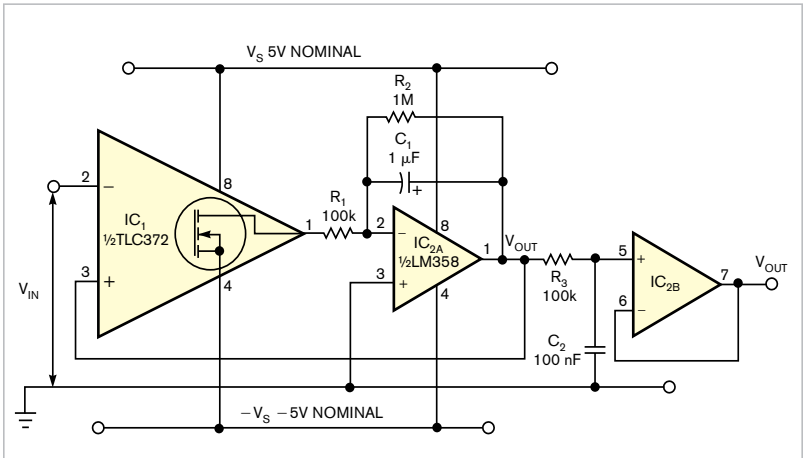

Figure 1 The dual-power-supply-voltage version of this positive peak detector requires only two active devices: a comparator and a dual operational amplifier.

A relatively large value of capacitance minimizes the negative-going ripple on V_{OUT}, which can be useful when dealing with low frequencies, low-duty-cycle pulse trains, or both. However, making C_1 too large renders the detector sluggish when responding to a sudden decrease in input-signal amplitude. Note that C_1 also affects the attack time; for example, doubling the capacitance doubles the time the circuit takes to acquire the peak level of V_{IN}.

Because the comparator's feedback path includes op amp IC_{2A}, offsets and errors that IC_{2A} presents have no effect on the circuit's accuracy. At low to moderate frequencies, only the comparator's input offset errors contribute to the detector's overall accuracy. At high frequencies, the comparator's response time becomes a significant factor, leading to a reduction in V_{OUT} that worsens as the frequency increases. Despite these limitations, the circuit performs well over several decades of frequency from approximately 50 Hz to 500 kHz. **Figure 2** and **Table 1** show the test circuit's sine-wave-frequency response by plotting the error in V_{OUT} for three peak levels of V_{IN}.

The oscilloscope photo shows the circuit's response to a 500-mV peak sine wave at 400 kHz, in which the output voltage, at 488 mV, lies just below the positive peaks (**Figure 3**). In addition to exhibiting good sine-wave response, the test circuit produces good results with rectangular signals of duty cycles as low as 5%. Note that the virtual ground at IC_{2A}'s inverting input restricts V_{OUT} to positive voltages only. Therefore, the circuit can respond only to true positive peaks—that is, peaks that go above 0V. If the input signal goes entirely below 0V, V_{OUT} simply levels off at 0V.

Although not essential to the circuit's operation, the lowpass filter and buffer formed by R_3, C_2, and IC_{2B} can minimize any switching noise that appears on V_{OUT}. However, offset errors inherent to op amp IC_{2B} affect the filter's output voltage.

Figure 4 shows a single-supply version of the circuit, in which R_A and R_B set a reference voltage, V_{REF}, at IC_{2A}'s

TABLE 1 SINE-WAVE-FREQUENCY RESPONSE

Frequency (Hz)	Error V_{IN}=2.5V peak (%)	Error V_{IN}=250 mV peak (%)	Error V_{IN}=25 mV peak (%)
200	−0.4	0.8	10
2000	−0.4	1.2	10
20,000	0	0.4	6.4
200,000	0	−2.4	−7.6
400,000	0	−4	−22
500,000	−2.4	−4.8	−28.4
600,000	−12	−6	−34

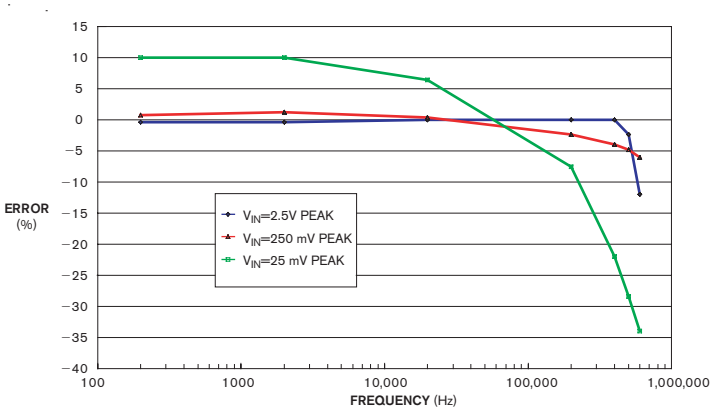

Figure 2 Plotting the difference between peak signal levels and output voltage for three peak levels illustrates the detector's frequency response.

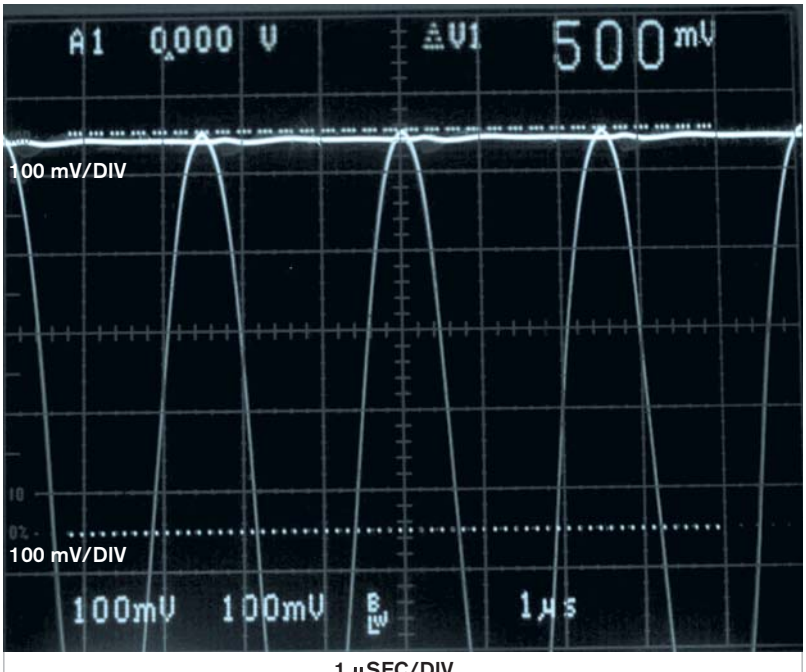

Figure 3 An oscilloscope photo displays input versus output voltages for a 400-kHz, 500-mV sine wave.

noninverting input, such that IC_{2A} maintains a virtual potential equal to V_{REF} at the inverting input. Thus, when V_{IN} goes more positive than V_{OUT}, the comparator's output MOSFET turns on, pulling the output down to 0V and impressing a potential equal to V_{REF} across R_1. This action, in turn, injects a current pulse equal to V_{REF}/R_1 into C_1. In most respects, the circuit behaves in the same manner as the circuit in **Figure 1**. As in the dual-rail version, V_{OUT} cannot go below the potential at the op amp's noninverting input. Therefore, even though V_{IN} need not center on a potential equal to V_{REF}, V_{IN}'s positive peaks must exceed V_{REF} for the circuit to work properly.

To select a value for V_{REF}, examine the input and output common-mode-voltage ranges of both op amp IC_{2A} and comparator IC_1 and the maximum peak-to-peak swing of the input signal. For example, setting the positive power-supply voltage, V_S, to 10V and setting $R_A=R_B$ sets $V_{REF}=5V$. The detector accommodates an input signal that swings from 0V to approximately 8V and thus detects positive peak voltages of 5 to 8V. Remember to select R_1 according to the value chosen for V_{REF}.EDN

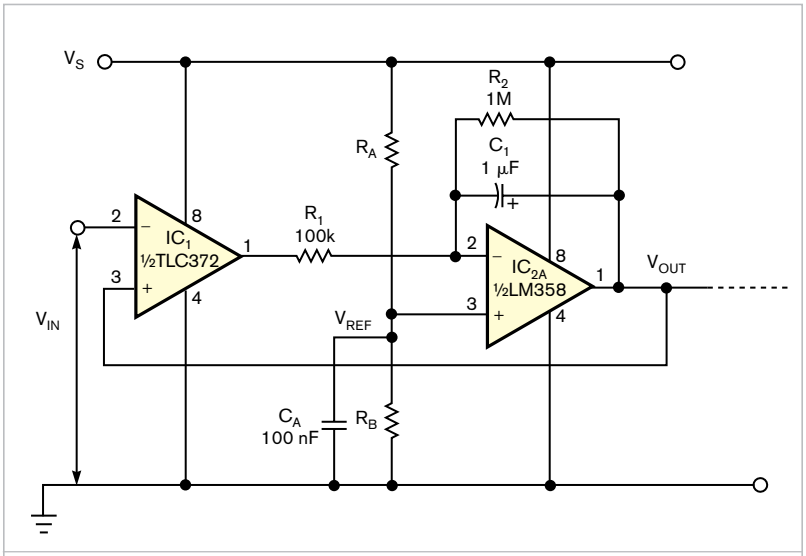

Figure 4 For operation from a single power supply, this version of the peak detector sets a reference voltage via resistors R_A and R_B.

Free program designs and analyzes passive and active filters

James Squire, Virginia Military Institute, Lexington, VA

At one time or another, most electrical engineers encounter a requirement to design or analyze an analog filter. Despite an abundance of graphical-user-interface-based digital-filter-design tools, such as The MathWorks (www.mathworks.com) Matlab Signals toolbox, which includes the FDATool filter-analysis package, few general-purpose, intuitive, and free GUI tools exist for synthesis of arbitrary active analog filters. To fill the need for a powerful and intuitive filter-design tool, this Design Idea describes an active-filter-design tool that bioengineering students at the Massachusetts Institute of Technology and at least four other universities use. Although originally implemented to run under Matlab, you can download a free copy of the program's stand-alone version at www.jamessquire.net. Select the "Research" menu and scroll to the software section at the bottom of the page. From the program list, select "Active Filter Design for Matlab" to download a copy of Filter Free 4.0.

Filter Free's functions include third-order analog and IIR (infinite-impulse-response) filters and 10-tap FIR (finite-impulse-response) filters. The program synthesizes filter designs and analyzes the frequency, time, and reflection responses of the ideal, unmodified filters. You can also view transfer functions in standard formats and pole-zero patterns. Using Filter Free, you can select any of 11 filter topologies ranging from gaussian to delay in bandstop, bandpass, highpass, and lowpass responses in five passive, transmission-line, active, switched-capacitor, and digital implementations.

As a design tool, Filter Free simulates a filter's frequency and time-domain responses as assembled using idealized component values. For component-approximation purposes, a round-off option reduces the number of significant figures in components' values. Data-display options include time or frequency response, pole-zero plots, transfer function, and reflection coefficient. You can select graphical plots' axis format, scale factors, and units of measurement.

As a teaching tool, Filter Free can load a user-supplied data file containing a stimulus waveform and simulate a filter's time- and frequency-domain responses. You can download 2000-point data files containing sample waveforms from www.nuhertz.com/filter/sampledata.html. Although the program's user interface is self-explanatory and includes built-in help menus, you can obtain a copy of the program's user's manual in Adobe's pdf format from the download site.EDN

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READERS SOLVE DESIGN PROBLEMS

Power-supply interrupter fights ESD-induced device latch-up

Emerson Segura, Lifescale Global Diagnostics Inc, Toronto, ON, Canada

Under certain conditions, ESD events can damage digital circuits by causing latch-up. For example, when ESD triggers them, parasitic transistors normally formed as parts of a CMOS device can behave as an SCR (silicon-controlled rectifier). Once ESD triggers, the SCR presents a low-resistance path between portions of the CMOS device and conducts heavily. Damage to the device can result unless you immediately remove power from the circuit. ESD from human interaction presents a significant problem for mobile industrial and medical devices. For adequate ESD protection, most medical and industrial devices require a grounded return path for ESD currents. In the real world, mobile devices may serve in environments in which properly grounded power outlets are unavailable.

To protect expensive equipment from latch-up failures even when no ESD ground is present, you can add the power-interruption circuit shown in **Figure 1** to prevent damage when ESD-induced latch-up occurs. Under normal conditions, current drawn by ESD-susceptible devices develops a small voltage across sense resistor R_6. A voltage divider formed by R_4 and R_5 defines a reset-current threshold for the LED portion of optoisolator IC_1, and, under normal operational current consumption, the LED remains dark.

The output of IC_1 controls the gate bias applied to MOSFET Q_1, which is normally on. When latch-up occurs, power-supply current drain rapidly increases by an order of magnitude or more. The large voltage drop developed across R_6 forward-biases IC_1's LED, which in turn drives IC_1's phototransistor into conduction and shuts off Q_1, interrupting dc power to ESD-susceptible devices for several milliseconds. In addition, the system's firmware design must allow for automatic recovery from a power interruption.

The following describes the relationship between the reset-current threshold and the values of R_4 and R_5: $(R_4+R_5)/R_4=(I_T\times R_6)/V_{LED}$, in which $I_T\geq(V_{LED})/R_6$, and $V_{CC}>V_{LED}$.

The ESD-induced fault threshold current, I_T, is greater than or equal to the optoisolator LED's conducting forward-voltage drop divided by the value of sense resistor R_6. Also, the raw power-supply voltage must exceed the LED's forward-voltage drop. Resistor R_1 provides a path for IC_1's base-leakage current, and resistors R_3 and R_2 determine Q_1's gate-shutoff bias.

In **Figure 1**, the optoisolator presents an LED forward-voltage drop of 1.2V. For the component values shown, the circuit momentarily interrupts V_{CC} when ESD-induced power-supply current exceeds approximately 300 mA. Total cost of the six resistors, one MOSFET, and one optoisolator is approximately $1 (production quantities). EDN

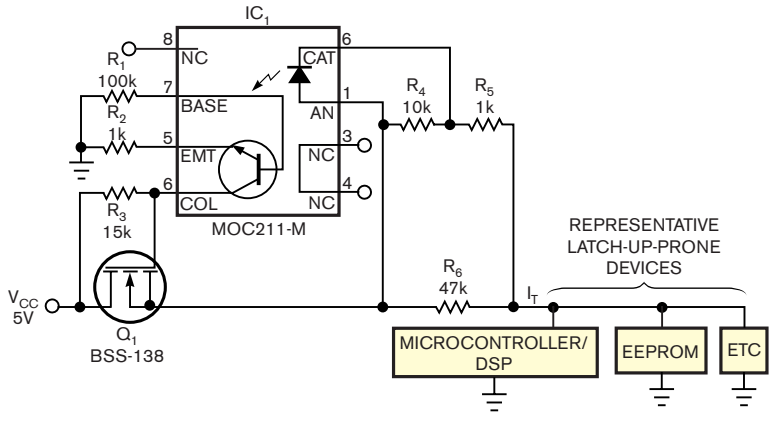

Figure 1 Upon sensing an overcurrent spike, this circuit interrupts power and enables the circuit's recovery from ESD-induced latch-up.

DIs Inside

High-impedance FET probe extends RF-spectrum analyzer's usable range

Steve Hageman, Windsor, CA

Current models of spectrum analyzers routinely offer frequency responses that begin as low as 10 Hz. When you combine them with 1-Hz or narrower band FFT software, expanded low-frequency performance makes the modern spectrum analyzer an invaluable tool for designing and debugging high-performance analog circuits. Unfortunately, a spectrum analyzer that's primarily for RF typically presents an input impedance of 50Ω, a heavy load when you apply it to most high-impedance analog circuits. You can improvise a somewhat higher impedance probe by adding a 953Ω resistor in series with the 50Ω input, but this approach provides only a 1-kΩ input impedance and reduces the measured signal by 26 dB.

In addition, most RF-spectrum analyzers lack ac coupling, and, thus, any dc-input component directly reaches either the internal terminating resistor or the front-end mixer. To maintain a 10-Hz, low-frequency response, you must connect a coupling capacitor with a value of at least 2 µF in series with the 953Ω input probe. Although oscilloscopes' input circuits can withstand accidental probe contacts and capacitive-transient overloads, using a low-impedance, ac-coupled probe with a spectrum analyzer can lead to destruction of the analyzer's expensive and possibly hard-to-replace front-end mixer.

Although high-impedance probes are commercially available, they're expensive to purchase and repair. This Design Idea offers an alternative: an inexpensive and well-protected unity-gain probe that presents the same input impedance as a basic bench oscilloscope and can drive the spectrum analyzer's 50Ω input impedance. The probe has a gain of 0±0.2 dB at 100 kHz. Input impedance is 1 MΩ, 15 pF, and maximum input is 0.8V p-p. Load impedance is 50Ω, and frequency response is 10 Hz to 200 MHz at −3 dB. Passband ripple is less than 1 dB p-p. Input noise at 1 MHz is less than 10 nV/√Hz. Distortion for 0.5V p-p input at 10 MHz is less than −75 dBc for second-order distortion and less than −85 dBc for third order. Power requirements are ±5V at 16 mA.

You can assemble the circuit in **Figure 1** in an afternoon from readily available and inexpensive components. The circuit's input presents the same characteristics as a bench oscilloscope—a 1-MΩ resistance in parallel with 15 pF of capacitance. You can also use this active probe in place of standard 1-to-1 or 10-to-1 oscilloscope probes, thus extending the design's applicability. The back-to-back silicon diodes in the D_1 clamp the input signal to plus or minus one forward-voltage drop, which limits signal excursions you apply to the spectrum analyzer's front end, thus protecting the input mixer from damage due to overloads and ESD. Because most users employ the probe and spectrum analyzer to measure small-amplitude signals and noise,

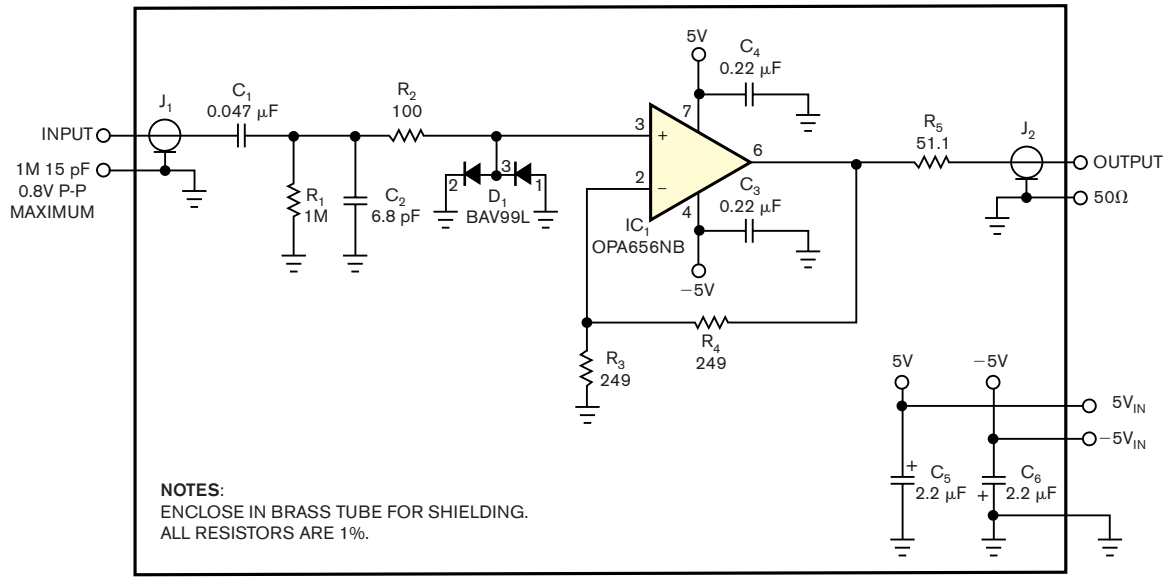

Figure 1 Just a handful of parts can help extend a spectrum analyzer's performance. This unity-gain probe emulates a standard oscilloscope probe's 1-MΩ and 15-pF input characteristics and easily drives 50Ω loads.

the limited large-signal response does not affect most applications.

High-performance FET input operational amplifier IC_1, a Texas Instruments OPA656, provides a voltage gain of two. This configuration yields a bandwidth of approximately 200 MHz (**Figure 2**). The OPA656 can drive 50Ω back-matched loads for a total load of 100Ω, which results in a 6-dB gain loss for which IC_1's gain of two compensates for a net gain of unity. The OPA656 also introduces lower noise and distortion than that of most commercially available, active FET-based probes.

The probe in **Figure 3** fits into a small section of brass hobby tubing. The input connector comprises a small SMA edge-launch connector that you can easily adapt to other connectors, including the BNC and its many accessories. The probe requires 5 and −5V at approximately 18 mA each, which you can obtain from an instrument's probe-power connector if available or from a linear supply designed around an ac wall transformer. For best results, use 78L05 and 79L05 voltage regulators to stabilize the supply voltages.

Standard miniature 50Ω coaxial cable connects the probe to the measuring instrument. For the flattest frequency response and uniform gain, terminate the probe's output with 50Ω; the circuit requires no dc-output-blocking capacitor. EDN

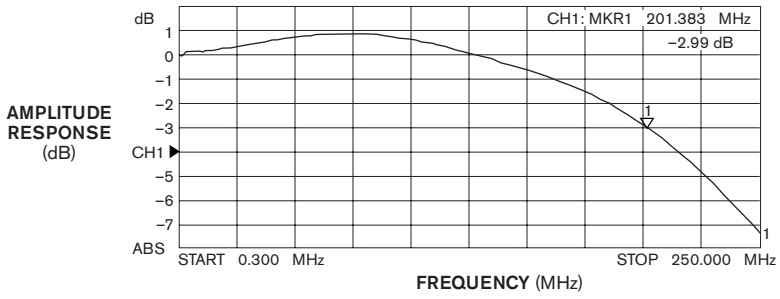

Figure 2 The probe's measured −3-dB frequency response extends from 10 Hz to 200 MHz with slightly less than 1-dB passband ripple, which compares favorably with the ±2-dB response of many commercial active-FET probes.

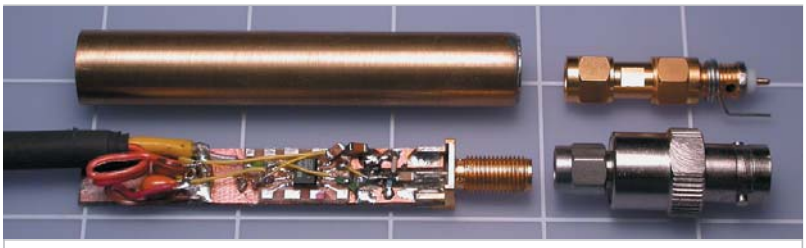

Figure 3 You can assemble the probe on a piece of breadboard that fits into a section of brass tubing from model and hobby shops. An SMA input connector matches a multitude of adapters and probe tips, a few of which are shown. Use a rubber grommet to close the probe's output end.

Watchdog circuit protects against loss of battery charger's control signals

Andy Fewster, Maxim Integrated Products Inc, Hampshire, UK

Recharging a mobile phone's internal battery usually occurs under control of a proprietary charging algorithm that resides in the baseband controller. The charger connects to the internal battery through a P-channel-MOSFET switch of low on-resistance (**Figure 1**). A baseband controller supplies a PWM signal that drives the switch. To minimize power dissipation and consequent thermal problems in the phone, the charging supply—usually a plug-in transformer assembly—features internal current limiting and has specifications that correspond to the battery's chemistry and charge-recovery requirements.

However, if the baseband processor stalls for any reason, the nearly direct charger-to-battery connection could damage the battery. To circumvent the problem, another circuit monitors the charger's PWM input and disables the series power switch after a predetermined delay interval (**Figure 2**). The circuit operates independently of the baseband unit's processor and allows charging to resume when the PWM signal returns.

In this circuit, microprocessor supervisor IC_1, a Maxim MAX6321 that includes a watchdog circuit that can monitor software execution, drives IC_2, a normally open SPST analog switch. Components R_4, D_2, and C_1 protect IC_1 and IC_2 by limiting V_{CC} to a maximum of 5.1V. Resistor R_4's value isn't critical because the protection circuit's quiescent current is low at approximately 30 µA. Select R_4 to provide just enough current—for example, 0.5 mA—to bias zener diode D_1 into the "knee" of its characteristic V-I curve.

(continued on pg 76)

The protection circuit consumes no power except when the battery undergoes charging and therefore doesn't burden the battery. Supervisor IC_1 provides a $\overline{\text{RESET}}$ output that can serve as a charger-ready interrupt input to the baseband-controller CPU. The $\overline{\text{RESET}}$ output's open-drain structure allows its connection to other circuits that operate from different supply voltages. Supplying power to the watchdog and PWM circuits only during charging also prevents reverse current from flowing into the IC_1's $\overline{\text{RESET}}$ output and discharging the battery via a sneak path.

The timing diagram illustrates the circuit's operation when an active

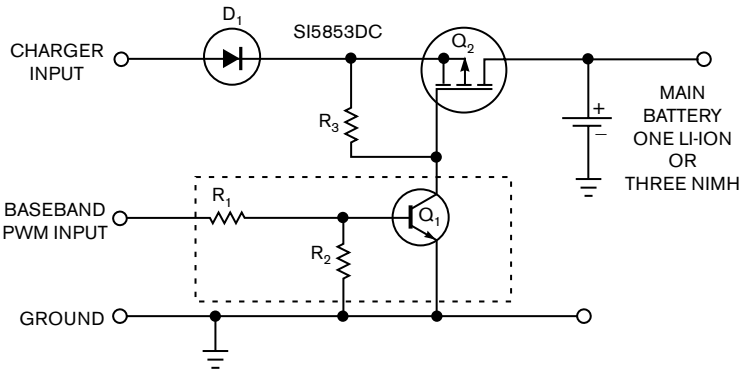

Figure 1 A typical mobile phone's battery-charger input circuit comprises a series switch controlled by a PWM signal.

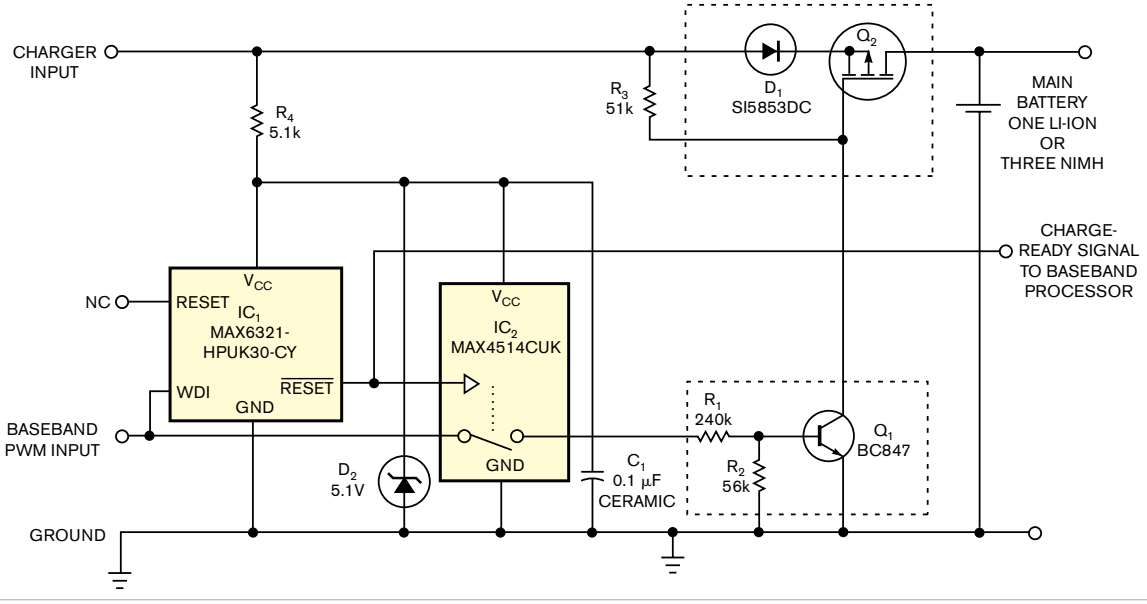

Figure 2 Adding watchdog protection to the circuit of Figure 1 guards against battery damage when the baseband processor stalls or ceases software execution.

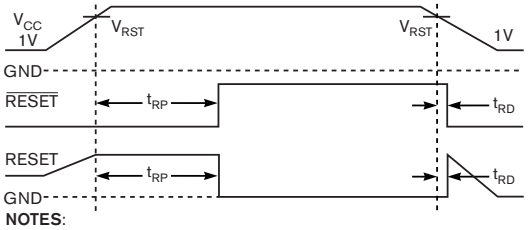

Figure 3 Reset-timing relationships for the circuit of Figure 2 illustrates its power-on behavior.

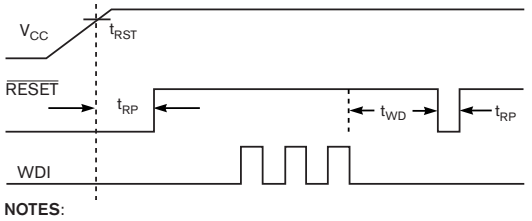

Figure 4 When PWM pulses cease, the watchdog circuit disables the charger after a 1.6-sec interval.

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

AGC amplifier features 60-dB dynamic range

Julius Foit, Department of Microelectronics, CTU Prague, Czech Republic

When processing signals from analog sensors, you frequently encounter wide variations in attenuation among communication channels or sensors. Or, you face situations in which several identical sensors within a supervised system return signals of roughly similar spectral composition and dynamic range but with considerably different maximum amplitudes. Sometimes, it's possible to predict these and other variations and adjust the gain of preprocessing amplifiers. More frequently, you encounter unpredictable signals and thus lose data associated with nonrepeatable events. In these circumstances, an adaptive preamplifier with AGC (automatic gain control) can prevent measurement-channel saturation and data loss.

AGC preprocessing suppresses the absolute amplitude of a sensed signal while preserving the best possible resolution of individual spectral components' relative amplitudes. The circuit in this Design Idea offers one relatively simple and efficient approach to per-channel AGC. The circuit uses a method of direct low-level signal control using a short-circuited bipolar transistor. In **Figure 1**, a variable voltage divider comprising a fixed resistance, R_1, and a variable resistance controls the signal's ac amplitude. The variable resistance comprises the differential resistance of a bipolar transistor, Q_1, short-circuited from base to collector. To vary Q_1's resistance, you force direct current into the shorted transistor from a current source comprising voltage source V_{REG} and a high-value resistor, R_2. To prevent R_2 from affecting the circuit's ac-voltage-transfer characteristic, R_2's resistance must greatly exceed R_1's.

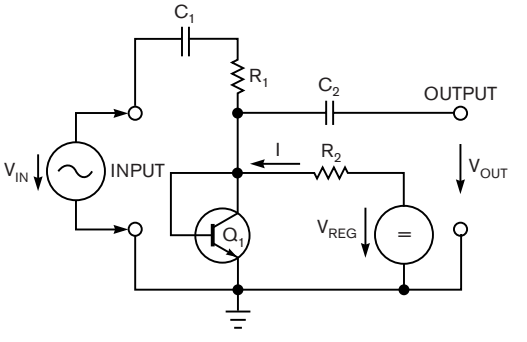

Figure 1 A short-circuited bipolar transistor forms one element of a basic attenuator circuit.

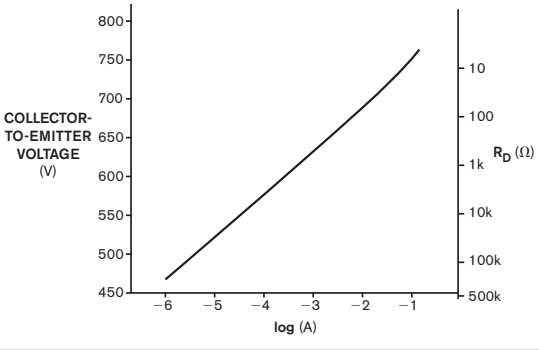

Figure 2 A VI characteristic shows the corresponding differential-resistance graph for a short-circuited BC337-16 transistor. (Note: The -16 denotes a sorted h_{FE} range of $100<h_{FE}<250$.)

DIs Inside

For all reasonable values of positive current I—generally, less than the transistor's maximum rated emitter current (I_E)—transistor Q_1's collector-to-emitter saturation voltage is less than its base-emitter threshold voltage, and the transistor operates in the active state. The shorted transistor's VI (voltage-versus-current) characteristic curve strongly resembles that of a PN diode and follows Shockley's Equation except for slightly higher dc-voltage values. That is, the device's voltage variation is proportional to the logarithm of the dc-current variation.

Therefore, the shorted transistor's differential resistance at every dc operating point along the VI curve is inversely proportional to the passing dc current; in other words, the device's differential conductance is directly proportional to the current. Because, in its active state, a common-emitter-connected bipolar transistor's current-amplification factor is typically 100 or more, the differential resistance accurately follows this rule over a broad range of currents.

Thus, varying V_{REG} in **Figure 1** varies the current, I, and controls the R_1-Q_1 voltage-division ratio. Coupling capacitors C_1 and C_2 separate the

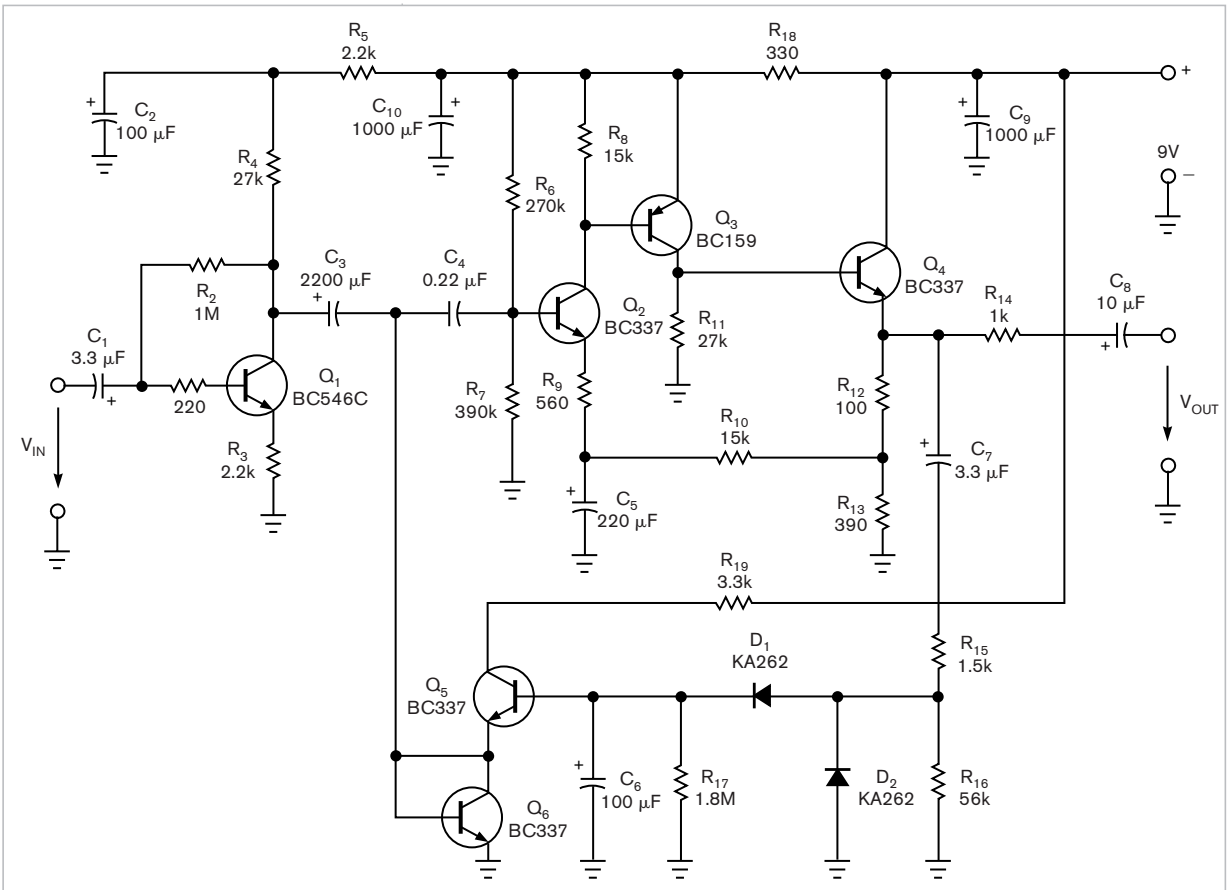

Figure 3 You can assemble this AGC circuit entirely from discrete components.

circuit's attenuator from the input-signal source and output load. **Figure 2** illustrates a typical small-signal bipolar transistor's short-circuited VI characteristic, showing that you can control differential resistance over at least five decades of range—that is, more than 100 dB.

In a practical circuit, the finite values of R_1 and R_2 limit the control range. For proper operation and to keep the signal's THD (total-harmonic-distortion) factor, k, below 5%, the output-voltage amplitude, V_{OUT}, should be just a few millivolts. Even with these limitations, this attenuator circuit appears to offer one of the best and simplest AGC circuits.

Figure 3 shows the completed circuit design. The input signal, V_{IN}, drives buffer stage Q_1, whose unbypassed emitter resistor, R_3, serves four purposes. First, it increases Q_1's differential output resistance to the approximate value shown in **Equation 1**:

$$R_{D1} \approx \frac{h_{11E} + h_{21E}R_3}{h_{11E}h_{22E}}. \quad (1)$$

The increase in the circuit's differential output resistance is so large that the value of R_4, 27 kΩ, almost exclusively determines the overall output resistance. Second, leaving R_3 unbypassed reduces Q_1's voltage gain to:

$$A_{IC1} = (h_{22E}R_3 - h_{21E})R_4 / (R_3 + R_4)D_{hE} + [h_{21E} + 1 - h_{12E} + (R_3 + R_4)]R_3 + h_{11E} \approx -R_4/R_3. \quad (2)$$

This **equation** simplifies to $A_{IC1} \approx R_4/R_3$. (Note that D_{hE} denotes the determinant $(h_{11E} \times h_{22E} - h_{12E} \times h_{21E})$, which this Design Idea includes for theoretical accuracy. However, you can neglect the numerical value of D_{hE} for modern silicon transistors without significantly affecting the calculation's accuracy.) Third, as **Equation 2** shows, leaving R_3 unbypassed helps linearize the response of Q_1's collector current-to-voltage drive. Fourth, Q_1's differential base input resistance rises to: $R_{dBASE} = h_{11E} + h_{21E} \times R_3$, which is larger and less dependent on Q_1's instantaneous operating point than h_{11E} alone.

In **Figure 3**, resistor R_4 forms the variable attenuator's fixed resistance, analogous to the upper resistor, R_1, in **Figure 1**, and Q_6 forms the attenuator's variable-resistance element. Transistor Q_5 supplies Q_6's collector-drive current, and Q_5's common-emitter configura-

(continued on pg 92)

tion draws little base current. This approach enables use of a high value for AGC-release time-determining resistor R_{17}, thus permitting a long AGC-release time. Resistor R_{19} limits the maximum dc control current through Q_5 and Q_6.

The large value of C_3, when you compare it with Q_6's minimum differential resistance—that is, its maximum signal amplitude—at full control, presents negligible reactance to the lowest frequency-signal-spectrum component. A voltage-doubler rectifier comprising D_1 and D_2 extracts a portion of the signal from output stage Q_4 and produces the control voltage for Q_5. This arrangement accommodates both polarities of large peak amplitudes of nonsymmetrical signal waveforms. Resistor R_{15} determines the AGC's "attack" time. Too small values of R_{15} in combination with C_6 can lead to instability by creating a pole in the feedback-transfer function. Resistor R_{17} determines the AGC-release time.

To secure good response to high-frequency-signal components, use either Schottky or fast PN silicon diodes for D_1 and D_2. The dc-coupled complementary cascade comprising Q_2 and Q_3 supplies most of the circuit's voltage gain. A 1-kΩ resistor, R_{14}, isolates Q_4, the output-emitter follower, from the signal-output terminal. If necessary, you can use a lower resistance at R_{14}, but a large-capacitance connecting cable can provoke Q_4 into parasitic oscillation if R_{14} is too low.

Figure 4 shows the circuit's input-versus-output characteristics as measured with a sine-wave signal. The effective AGC range extends from 100-μV- to 100-mV-rms input voltage, a 60-dB dynamic range. Output voltage varies less than 2 dB over this input range, reaching a nominal level of 775 mV rms at a −20-dB- (100-μV-rms) input level. The input's 0-dB point is set arbitrarily at 1-mV-rms input, which corresponds to an 803-mV-rms output. The AGC attack time for a sinusoidal-input-signal step from 0 to 100 mV rms is approximately 0.3 sec, and the AGC release from 100-mV-rms input to −20 dB (100 μV rms) is approximately 100 sec. **Figure 4** also includes a graph of THD versus input voltage. The distortion is well below a 5% THD limit throughout the input-voltage range.

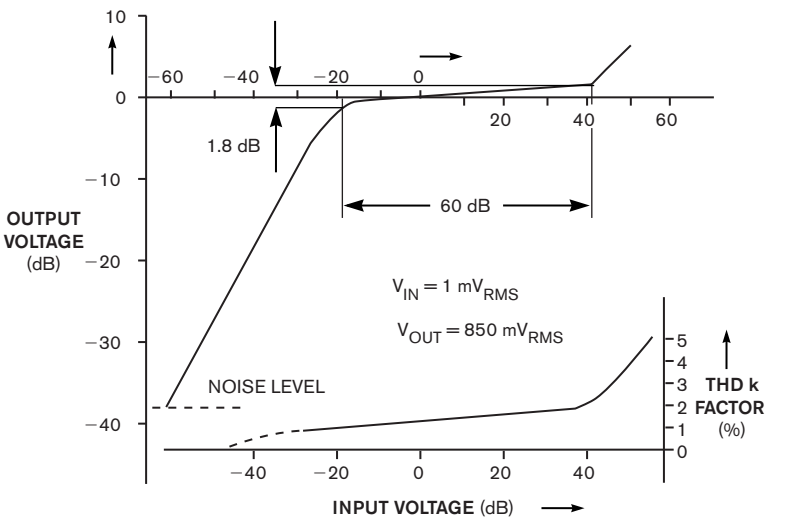

Figure 4 The circuit's input-versus-output characteristic shows a 60-dB control range (upper trace) and total harmonic distortion well below 5% over the control range (lower trace).

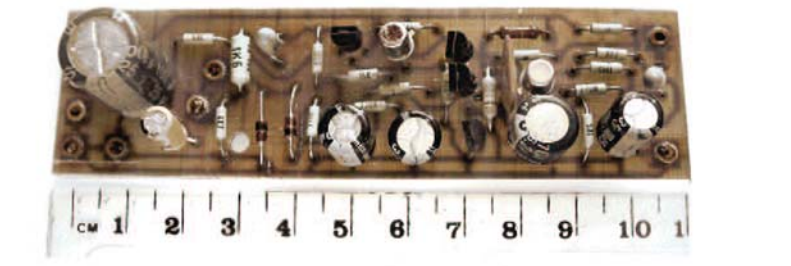

Figure 5 A single-sided pc board accommodates the assembled AGC amplifier.

To measure the attenuator's baseline input noise, terminate the input with its nominal 1-kΩ source resistance. At low input voltages, input stage Q_1's noise limits the processed signal's usable dynamic range. The rms noise level is about −38 dB relative to the nominal output for input signals below the AGC threshold. When the AGC becomes active, the SNR increases in proportion to the AGC reduction. For example, with a 0-dB- (1-mV-rms) input signal, the SNR increases to approximately 60-to-1.

If you assemble the circuit using the passive-component values in **Figure 3**, the amplifier's −3-dB bandwidth spans 45 Hz to 35 kHz. At a power-supply voltage of 9V, no-signal current consumption is approximately 12 mA. **Figure 5** shows a photograph of the assembled pc board. EDN

Precision active load operates as low as 2V

By Joel Setton, Crolles, France

This Design Idea presents a self-powered, precision-active-load circuit that improves on a previously published design (**Reference 1**). Added features include a wider operating-voltage range of 2 to 50V or higher and several flexible current-setting modes. The circuit in **Figure 1** uses National Semiconductor's LM10, which suits this application. The LM10's reference section, IC_{1A}, generates a precision 1.2V reference voltage, V_S. Resistive divider R_1 and R_2 applies a fraction of V_S to IC_{1A}'s reference amplifier, which drives shunt regulator Q_1.

Transistor Q_3 acts as a current mirror of transistor Q_2's collector current and supplies power to shunt regulator Q_1. Resistors R_9 and R_7 set the current-mirror ratio, and the current through resistor R_9 depends on the current through R_6, which V_S establishes. As a result, Q_3, which mirrors the collector current of Q_2, provides power to the shunt regulator. V_S sets R_6, which determines the current through R_9. Thus, the LM10's reference section regulates both its own power-supply voltage and the current that Q_3 provides.

At power-on, Q_2, Q_3, and Q_4 are all off. Resistor R_{10} draws a small amount of start-up current, which Q_3 amplifies to start the current-mirror process. When sufficient current flows through R_7, Q_4 saturates, and R_9 and R_7 then set the current-mirror ratio. The active load's power-handling section comprises the LM10's operational-amplifier section, IC_{1B}, and power transistors Q_6 and Q_8. A 10-turn precision potentiometer, P_1, and range-selection switch, S_1, set the load current as follows:

On Range A, the load current varies at 1A per turn of P_1—that is, 10A maximum with P_1 set fully clockwise. On Range B, the load current varies at 100 mA per turn of P_1—that is, 1A maximum with P_1 set fully clockwise. On Range C, an external voltage source that connects to R_{13} controls the load current at a rate of 1A per volt with P_1 set fully clockwise. You can drive the external input with a function generator to test a power supply's transient response. On Range D, the load circuit emulates an adjustable power resistor with load current proportional to the voltage across the load's terminals. The equivalent resistance varies with P_1's setting—that is, $R_{LOAD}=100\Omega/N_{TURNS}$. Range E is similar to D, with a resistance of $10\Omega/N_{TURNS}$.

To calibrate the circuit, connect it to a suitable power supply delivering any voltage from 2 to 50V. First, set P_1 to one turn—that is, one-tenth of full-scale—and S_1 to Range B. Adjust R_{17} for a 100-mA output current. Then, rotate P_1 fully clockwise and adjust R_{20} to set the output current to 1A. Repeat these two adjustments in sequence because they interact slightly. Current that IC_1 draws through Q_3 sets the minimum current through the load circuit at slightly less than 1 mA.

Because the circuit operates at 2 to 50V, it is suitable for testing the low-voltage outputs of a PC's power supply. You can extend the maximum voltage by selecting suitable transistors for Q_2, Q_3, and Q_5 through Q_8; the LM10's regulated power-supply voltage does not link to the external voltage. Note that when dissipating large amounts of power, transistors Q_6 and Q_8 require adequate cooling to maintain safe junction temperatures. EDN

REFERENCE

1 Toffoli, Tommaso, "Self-powered dummy load checks out multiple power supplies," *Electronic Design*, April 17, 2000, pg 118.

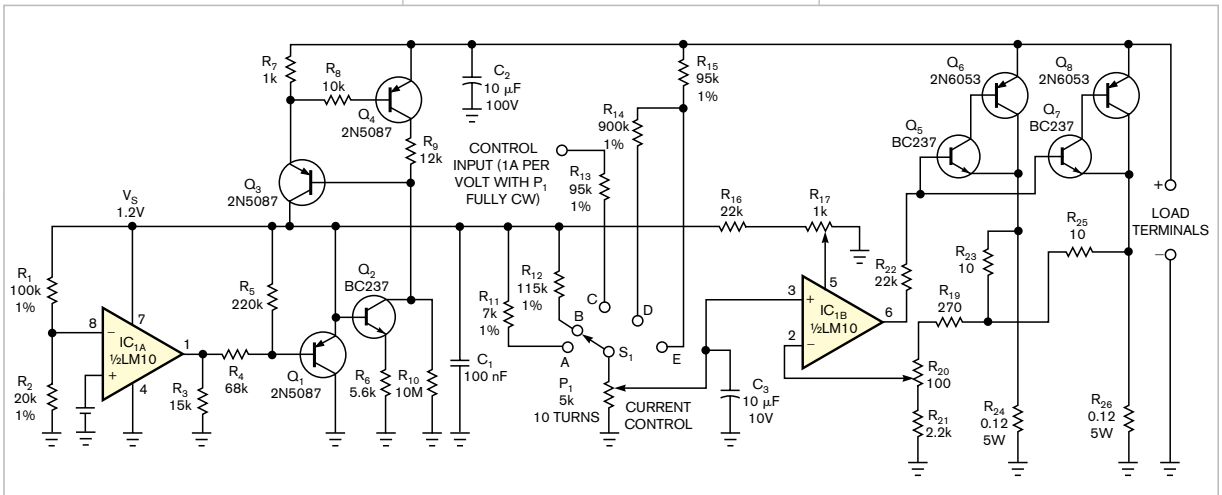

Figure 1 This versatile precision load circuit draws constant current or emulates an adjustable power resistor.

charger connects to the phone's charger-input socket (**Figure 3**). In this example, the MAX6321-HPUK30-CY that IC_1 uses is factory-trimmed for a 3V reset threshold, and the -CY suffix indicates complementary reset outputs and a 1.6-sec delay interval. The reset interval begins when V_{CC} reaches 3V±45 mV. After 200 msec, RESET goes low, and $\overline{RESET}$ goes high.

The $\overline{RESET}$ output releases the SPST analog switch, IC_2, which enables the PWM input. Meanwhile, the active WDI (watchdog input) monitors the PWM input signal. If no signal transitions occur within 1.6 sec, the RESET and $\overline{RESET}$ outputs become active, disabling the PWM input and pausing the charger algorithm using a CPU interrupt that the charger-ready signal conveys (**Figure 4**). All active and passive components for the circuit are available in surface-mount packages. Pass transistor Q_2, a Siliconix-Vishay SiS5853, includes an integrated Schottky diode, D_1.EDN

Circuit adds foldback-current protection

Rafael García-Gil and JM Espí, Electronic Engineering Department, University of Valencia, Spain

For many applications that require power-supply currents of a few amperes or less, three-terminal adjustable-output linear voltage regulators, such as National Semiconductor's LM317, offer ease of use, low cost, and full on-chip overload protection. The addition of a few components can provide a three-terminal regulator with high-speed short-circuit current limiting for improved reliability. The current limiter protects the regulator from damage by holding the maximum output current at a constant level, I_{MAX}, that doesn't damage the regulator (**Reference 1**). When a fault condition occurs, the power dissipated in the pass transistor equals approximately $V_{IN}\times I_{MAX}$. Designing a regulator to survive an overload requires conservatively rated—and often overdesigned—components unless you can reduce, or fold back, the output current when a fault occurs (**Reference 2**).

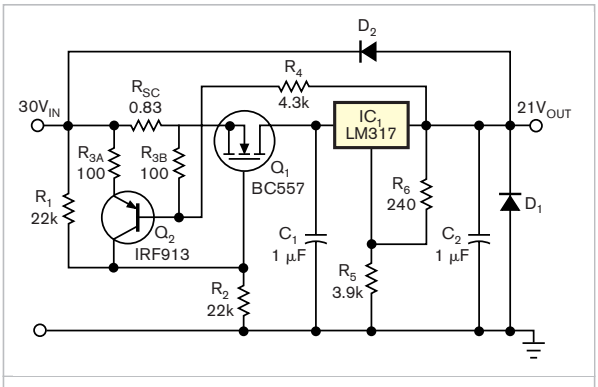

Figure 1 This circuit adds foldback-overcurrent protection to a linear regulator.

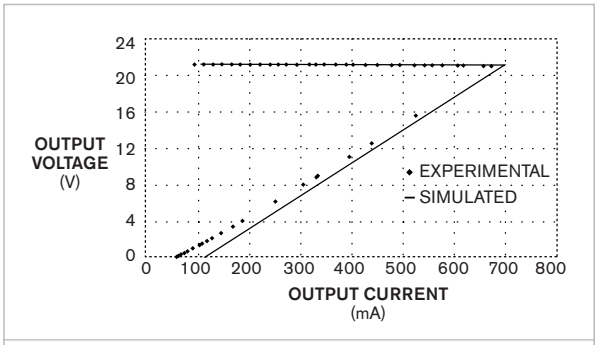

Figure 2 Simulated and measured foldback-current responses to a load resistance that varies from 200 to 0.01Ω show close agreement.

The circuit in **Figure 1** incorporates foldback-current limiting to protect the pass transistor by adding feedback resistor R_4. Under normal conditions, transistor Q_2 doesn't conduct, and resistors R_1 and R_2 bias MOSFET Q_1 into conduction. When an output overload occurs, Q_2 conducts, reducing the on-state bias applied to Q_1 and thus increasing its drain-source resistance and limiting the current flowing into regulator IC_1, an LM317. Adding R_4 makes Q_2's bias current dependent on the output voltage, V_{OUT}, which decreases under overload conditions.

For the circuit in **Figure 1**, you can calculate the maximum foldover and short-circuit currents, I_{KNEE} and I_{SC}, respectively, as follows:

$$I_{KNEE}=\frac{(R_3+R_4)\times V_{SENSE}}{R_{SC}\times R_4}-(V_{IN}-V_{OUT})\times\frac{R_3}{R_{SC}\times R_4}. \quad (1)$$

$$I_{SC}=\frac{(R_3+R_4)\times V_{SENSE}}{R_{SC}\times R_4}-V_{IN}\times\frac{R_3}{R_{SC}\times R_4}. \quad (2)$$

In a practical design, you select values for I_{KNEE} and I_{SC} and equal values for R_{3A} and R_{3B} and then use **equations 1** and **2** to calculate resistors R_{SC} and R_4. For the circuit in **Figure 1**, the output's maximum and short-circuit currents are fixed at 0.7 and 0.05A, respectively. With R_{3A} and R_{3B} set to 100Ω, solving the equations yields values of 0.73Ω for R_{SC} and 4.3 kΩ for R_4. You can demonstrate the circuit's performance by applying a variable-load resistor that's adjustable from 0 to 200Ω. As **Figure 2** shows, the output's simulated and measured voltage-versus-current characteristics, V_{OUT} and I_{OUT}, respectively, are in close agreement.EDN

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Squeeze extra outputs from a pin-limited microcontroller

Abel Raynus, Armatron International Inc, Malden, MA

Many of today's designs use low-cost microcontrollers from Freescale and Microchip, but during the last decade, device packages have resorted to ever-smaller footprints featuring as few as eight or even six pins. Although these packages minimize pc-board area, they also reduce the number of available I/O pins and pose problems for designers who need to add one more function without migrating to a device that occupies a larger package.

To overcome a shortage of inputs, a designer can increase a small microcontroller's inputs by writing a program that multiplexes and polls the input pins. However, this approach doesn't lend itself to extending outputs, because most designs require simultaneously driving multiple pins. **Figure 1** shows how to solve the problem by adding a shift register.

For example, you can add an eight-LED bar graph to a design based on IC_1, Freescale Semiconductor's 9-bit, flash-memory MC68HC908QT1 microcontroller, which has only eight pins. The device includes only four general-purpose outputs and thus by default cannot drive eight discrete LEDs. To solve the problem, you can add IC_2, a 74HC595 serial-input/serial-output/parallel-output latching shift register available from On Semiconductor and other vendors. The register's latching function allows selective drive of only those LEDs associated with specific data bits.

According to its data sheet, the 74HC595 accepts signals through the SPI protocol. Unfortunately, low-end microcontrollers, such as the MC68HC908QT1, lack SPI hardware, but you can simulate the SPI in software by following these steps:

1. Unlatch the shift register's outputs by deasserting microprocessor IC_1's PA4 pin.
2. Starting with the MSB, copy a bit from the processor's internal data register and transfer the bit to the processor's PA0 (SD) output.
3. Generate a clock pulse at Pin PA1.
4. Repeat steps 2 and 3 for all eight data bits.
5. Assert the microprocessor's PA4 output to latch the data into IC_2, the 74HC595.

Figure 2 shows the timing diagram for transmitting data byte $F0 from IC_1 to IC_2.

Available from the online version of this Design Idea at www.edn.com/050804di1, **Listing 1** illuminates the LEDs by sending five consecutive bytes to IC_2 and the LEDs: $03, $0c, $30, $c0, and $55. The first four bytes progressively illuminate two LEDs along the bar-graph display at one step per second. The last byte illuminates and latches all odd-numbered LEDs. The **listing** contains only commonly used instructions that easily translate into other microcontrollers' assembly languages.

The SPI requires only three output pins, which frees the microcontroller's remaining I/O pins for other functions and allows remote installation of the shift register/LED driver—for example, on a separate display board with the LEDs. Also, when suitably buffered, the register's outputs can drive other loads, such as motors, relays, and incandescent lamps. EDN

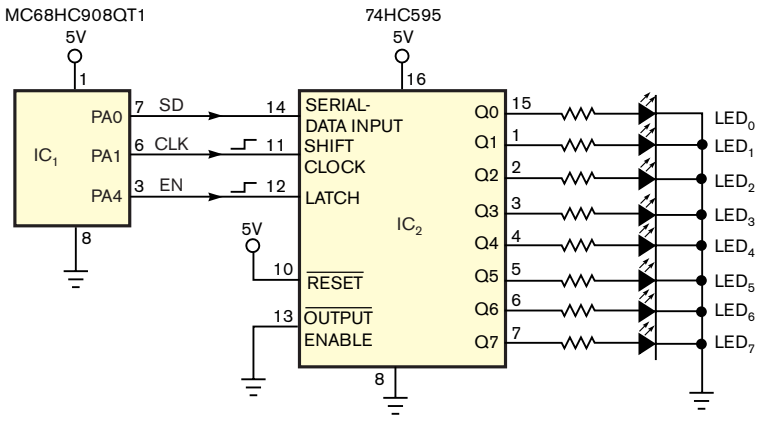

Figure 1 Do you need more outputs? You can emulate an SPI in software to add a shift register to a pin-limited microcontroller.

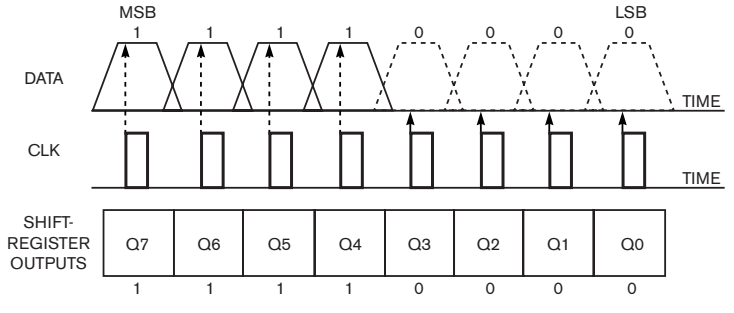

Figure 2 The sample timing diagram illustrates the loading of $F0 byte into an external shift register.

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READERS SOLVE DESIGN PROBLEMS

Build a precise dc floating-current source

D Ramírez, S Casans, C Reig, AE Navarro, and J Sánchez,
University of Valencia, Burjassot, Spain

Although well-known to active-filter theorists and designers, GICs (generalized impedance converters) may be less familiar to analog generalists. Comprising a one-port active circuit typically comprising low-cost operational amplifiers, resistors, and capacitors, a GIC transforms capacitive reactance into inductive reactance and thus can substitute for an inductor in a filter that an RLC-transfer function describes. In addition, the flexibility of a GIC's input-impedance equation permits the design of virtual impedances that don't exist as physical components—for example, frequency-dependent resistance (**Reference 1**). The GIC, which its developers introduced 30 years ago, has seen its greatest application in ac-circuit and active-filter applications.

Figure 1 shows a classic GIC circuit in which the input impedance, Z_{IN}, depends on the nature of impedances Z_1 through Z_5. The following equation describes the circuit's input impedance:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{Z_1 \times Z_3 \times Z_5}{Z_2 \times Z_4}.$$

For example, if Z_1, Z_2, Z_3, and Z_5 comprise resistors R_1, R_2, R_3, and R_5, and Z_4 comprises capacitor C_4, then the input impedance, Z_{IN}, appears as a virtual inductor of value L_{IN}:

$$L_{IN} = \frac{R_1 \times R_3 \times R_5 \times C_4}{R_2}.$$

Figure 2 shows the GIC circuit in its dc configuration. When you consider the GIC circuit in a purely dc environment, you can envision new applications. For example, you could replace impedances Z_1 through Z_5 with pure resistances R_1 through R_5. Instead of an ac input-voltage source, connect a precision temperature- and time-stable dc reference voltage to the input port. A simple circuit analysis using ideal op amps for IC_1 and IC_2 shows that the reference input voltage, V_{REF}, appears across resistor R_5, and, as the following equation shows, a constant current, I_O, flows through R_5.

$$I_O = \frac{V_{REF}}{R_5}.$$

However, op amp IC_2's noninverting input diverts a small amount of current from the junction of R_4 and R_5, and I_O thus also flows through R_4. Selecting

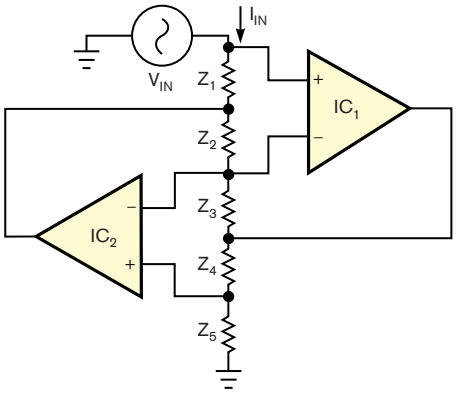

Figure 1 A classic generalized impedance converter provides a single-port impedance that appears at V_{IN}. The schematic omits power connections for clarity.

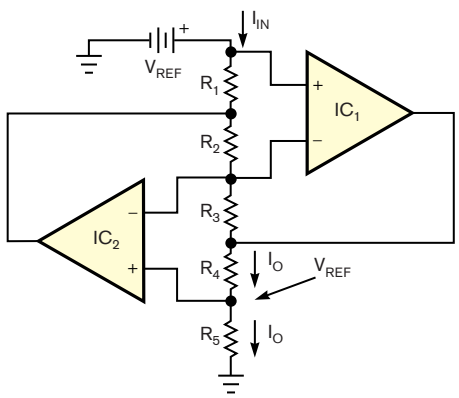

Figure 2 Replacing all of a GIC's impedances with resistors creates a constant-current source.

large values for R_1, R_2, and R_3 helps minimize current drawn from the reference voltage. For example, the circuit can supply 2 to 10 mA to R_4 and draw only a few tenths of a microampere from the reference source. Using tight-tolerance and low-drift components for V_{REF} and R_5 ensures the stability of I_O. Applications include providing constant-current drive for Wheatstone-bridge and platinum-element sensors (**Reference 2**). In addition, you can replace R_4 with a series of resistive sensors as in an Anderson loop (**Reference 3**). EDN

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Frequency dithering enhances high-performance ADCs

Steve Hageman, Windsor, CA

Since the late 1970s, designers have successfully improved the effective resolution and spurious performance of A/D converters by adding dither—uncorrelated noise—to a converter's input and then using DSP techniques to average out noise from the converted data. The most common dithering method adds random-amplitude noise to an A/D converter's input signal. Although this method works, the added noise includes large random peak values. To keep the A/D converter's input out of the saturation region, a designer must know both the peak signal and the peak dither levels. Even briefly saturating the A/D converter adds more nonlinearities than dither can remove.

Another approach adds a dithered-frequency, constant-amplitude signal. **Figure 1** shows one possible implementation featuring a Linear LTC1799 programmable oscillator, IC_2, that's operated in a VCO (voltage-controlled-oscillator) mode in which an applied voltage modulates the center frequency. You can set the LTC1799's center frequency at 1 kHz to 33 MHz, making it a suitable dither generator for many currently available A/D converters. Because the LTC1799's output comprises a square wave, its peak output amplitude is well-defined.

You can set the random-dither center frequency either below or above the signal frequency of interest. For conversion of a narrowband intermediate frequency, either location may work well. For an A/D converter that must operate to dc, the only useful location is above the signal frequency of interest. One approach places the dither frequency at one-half of the sampling or the Nyquist frequency. When you place it there, the random noise typically doesn't interfere with the desired signal, and any aliasing that occurs only folds the random frequency noise around itself and not into the desired signal band.

The circuit in **Figure 1** operates with a 20-MHz sampling A/D converter and generates random noise around a center frequency of 10 MHz. You can use any of a number of techniques to generate the random noise, including dig-

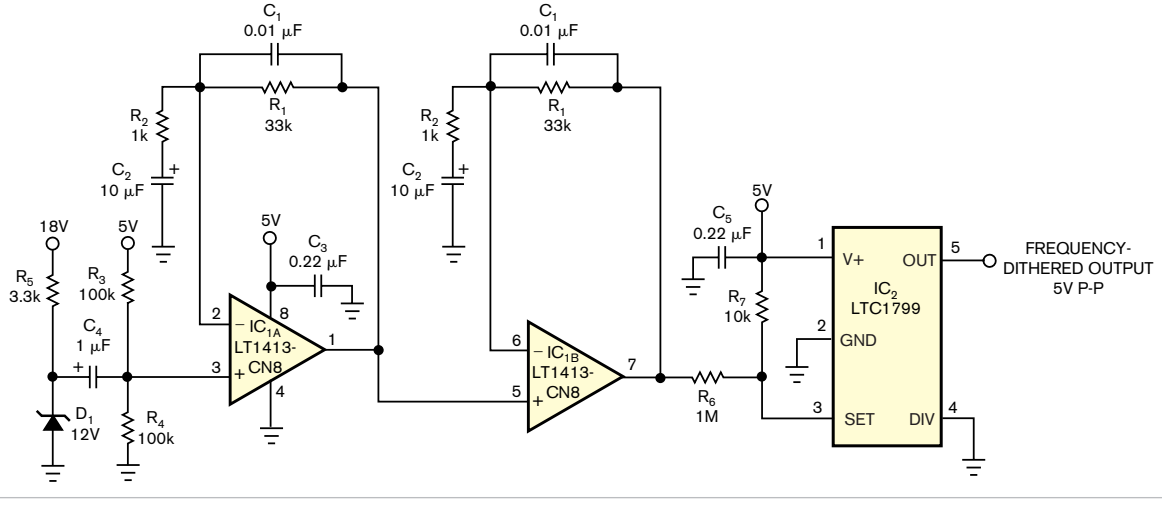


Figure 1 A zener diode, two stages of amplification, and an FM voltage-controlled oscillator form a constant-amplitude dither generator.

ital shift registers and semiconductor junctions biased into the breakdown range. In this design, a 12V zener diode, D_1, generates the noise, which a two-stage amplifier amplifies and frequency-shapes. If necessary, you can further shape the noise distribution by using more complex active-filter sections, IC_{1A} and IC_{1B}. After filtering, the noise modulates the LTC1799. Make sure that the LTC1799's power-supply voltage is pure dc and free of ripple, because power-supply noise produces nonrandom AM sidebands.

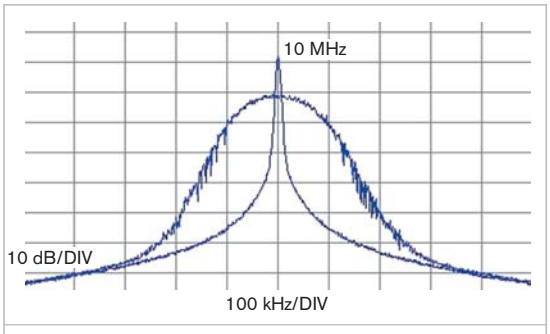


Figure 2 The broad bell-shaped curve shows a random-frequency-dithered spectrum superimposed onto the LTC1799's unmodulated, 10-MHz output.

Figure 2 shows an amplitude-versus-frequency plot of the frequency-limited spectrum that the design in **Figure 1** produces. Depending on the circuit's configuration, you can apply the dither to the A/D converter using a small coupling capacitor or a more complex active summing circuit. Although zener-diode noise generators offer theoretical simplicity, they behave poorly in production environments because their noise outputs can vary greatly. Even among diodes from the same manufacturing batch, you can observe popcorn noise, unevenly distributed noise histograms, amplitude shifts, and frequency-weighted noise. In a high-volume application, well-specified noise diodes, such as those from Micronetics (www.micronetics.com), may prove more cost-effective than zener diodes.

Once you select a noise diode, you can select amplification-stage gains such that clipping of noise peaks isn't evident at the circuit's output. If your application requires it, you can alter the amplifiers' frequency responses to alter the noise spectrum. Finally, adjust the LTC1799's frequency-setting resistors, R_6 and R_7, so that the noise-spectrum display resembles that in **Figure 2**. Any clipping along the amplifier path tends to add peaks to the edges of the spectrum, which indicates amplitude clipping and reduction of the noise's random characteristics.

You can add a filter between the noise output and the A/D converter's summing input to limit inband noise or remove any periodic modulation that power-supply ripple introduces. In a modern, high-performance A/D converter, even a small amount of periodic noise can manifest itself as a −80-dBc (decibels-below-carrier) spurious response. EDN

Memory-termination IC balances charges on series capacitors

Clayton B Grantham, National Semiconductor, Tucson, AZ

As one of today's most interesting component families, high-value capacitors offer ratings ranging from tenths to tens of farads but suffer from relatively low working voltages. For example, Maxwell's (www.maxwell.com) PC10 ultracapacitor occupies an area about the size of a large postage stamp and the thickness of four stacked US 25-cent coins. The PC10 provides 10F capacitance, a 2.5A maximum discharge-current rating, and an 18Ω ESR (equivalent-series resistance). However, its rated working voltage is only 2.5V.

To accommodate a supply voltage greater than 2.5V, you can connect two capacitors in series, halving the available capacitance and doubling the overall voltage rating. However, due to differences in leakage current and capacitance, the voltage at the capacitor's common connection can vary, and your design must ensure that you do not exceed either capacitor's maximum voltage rating. If the series-connected capacitors' charge and discharge currents are relatively small, you can connect equal-valued charge-balancing resistors across both capacitors. But for farad-range capacitors that can deliver amperes of current, you need a more efficient approach.

The theoretical voltage across a capacitor comprises its initial voltage, $V_C(0)$, plus the integral of the capacitance, C, multiplied by the capacitor's current over time: $V_C(t)=V_C(0)+C\times\int I(t)dt$. In a two-capacitor divider, the current through both capacitors is

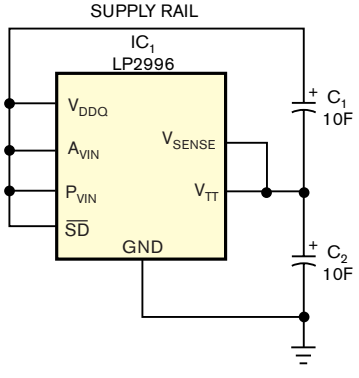


Figure 1 This simple circuit requires only a single IC to balance the charges on two series-connected, low-voltage, high-value capacitors and maintain their common junction at one-half of the supply voltage.

identical, and the loop equation, including the supply voltage, becomes: $V_{SUPPLY}=V_{C1}(0)+V_{C2}(0)+(C_1\times C_2)/(C_1+C_2)\times\int I(t)dt$. During charging to a 5V-supply level, differences in tolerances between C_1 and C_2 or residual voltages on either capacitor cause the voltage across one capacitor's terminals to exceed 2.5V and cause the other to fall below 2.5V.

To overcome this undesirable mismatch, the LP2996 DDR termination regulator, IC_1, sinks or sources current from both capacitors and actively maintains their voltages at one-half of the supply voltage (**Figure 1**). The LP2996 provides an active termination for DDR-SDRAM devices and can sink or source large amounts of current; its data sheet's nomenclature and labels reflect its intended memory-support role. The LP2996's Class B output, V_{TT}, drives the capacitors' common connection, actively maintaining the junction at $V_{DDQ}/2$ and becoming active only when the capacitors get out of balance. At balance, the LP2996 wastes no charging current and thus operates efficiently. The device's data sheet specifies that the LP2996's out-of-balance error amounts to a V_{TT} offset of ±20 mV around the $V_{DDQ}/2$ setpoint. **Figure 2** shows charge and discharge waveforms for 1A current steps.

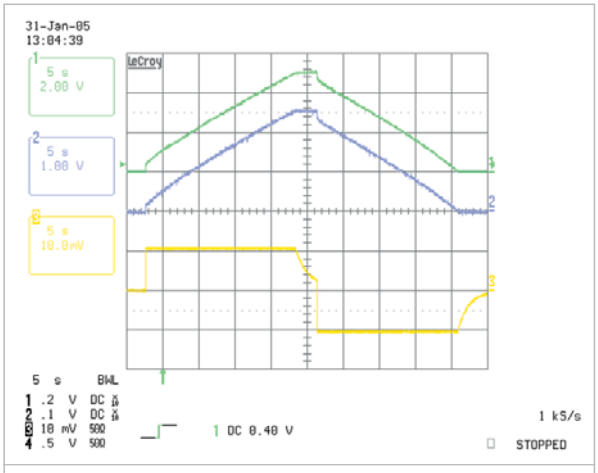


Figure 2 The oscilloscope waveforms within the active-balance circuit show the power-supply rail voltage (top trace), the midpoint voltage at the junction between the two capacitors (middle trace), and the charge/discharge current (lower trace, scaled to 1A per division). The traces reflect a 1A charge interval to 5V, followed by a 1A discharge to 0V. The waveform steps at the start of the charge and discharge intervals are due to the capacitor's internal ESRs.

This active balancing circuit does impose some limitations. Using a power supply rated at 5V and 1A, the two capacitors achieve charge balance in a maximum of 25 sec: Charge time=5F×5V/1A. The initial charging interval overcomes any initial prebias charge on either C_1 or C_2. The steady-state current flow into and out of the LP2996 amounts to a fraction of the high current flowing through the capacitors and is just sufficient to overcome any tolerance mismatch in the two. The LP2996 includes thermal-shutdown protection, but an instantaneous short circuit across either capacitor may occur too quickly to activate the protection circuitry.

Thermal considerations determine the capacitor's maximum current-handling capability, and the PC10's data sheet derates the current downward from 2.5A. You can connect 1Ω current-limiting resistors in series with both capacitors if the power supply provides charging current in excess of 2A.

Upon interruption of the power supplied to the circuit, the LP2996 imposes a self-discharge current of less than 1 mA, which represents a capacitor-"battery" discharge rate of 5000 sec per volt into an open circuit. You can reduce the LP2996's self-discharge current by applying an external control signal to its shutdown input. Upon power interruption, the two-capacitor string can supply a constant-current load of 1A for 15 sec over a voltage change from 5 to 2V. You can connect additional pairs of capacitors in parallel to provide additional current, but, depending on capacitance mismatches, initial bias voltages, and current demand, you may need additional LP2996s to maintain charge balance.EDN

Voltage reference is software-programmable

Reza Moghimi, Analog Devices, San Jose, CA

For a variety of reasons, designers often discover that their creations need yet more power-supply voltages. For example, a system powered by ±2.5V power supplies suddenly needs a precision −1.4V reference for a signal-level-shifting circuit and needs a 2.1V reference to drive an ADC. Your options include adding a couple of operational amplifiers and resistors to level-shift and buffer the system's voltage reference or adding a couple of DACs. Op-amp circuits lack programmability to accommodate design changes, and, although the DACs offer programmability, their settings are volatile, and the outputs are typically unipolar and lacking in drive capability.

The circuit in **Figure 1** offers an easy way to generate extra reference voltages and provides a few additional benefits. It allows you to easily generate positive or negative buffered references under software control. Its output buffer sinks and sources as much as 10 mA. You can read and adjust programmed voltages. On-chip storage restores the reference

voltages after a power interruption, and a parity bit can indicate a malfunction if an internal device failure accidentally causes the programmed voltage to change.

The programmable voltage reference comprises IC_1, an Analog Devices AD8555 high-precision auto-zero instrumentation amplifier, which contains an 8-bit DAC as part of its offset-adjustment circuit. In a change from its intended role, the monotonic DAC generates the output voltage, which can swing from V_{SS} (input code 0) to $V_{DD}-1$ LSB (input code 255). The DAC's 8-bit resolution provides voltage steps of 0.39% of the difference between V_{DD} and V_{SS}—for example, steps of 19.5 mV with a 5V supply. The output-voltage, V_{DAC}, temperature coefficient is less than 15 ppm/°C.

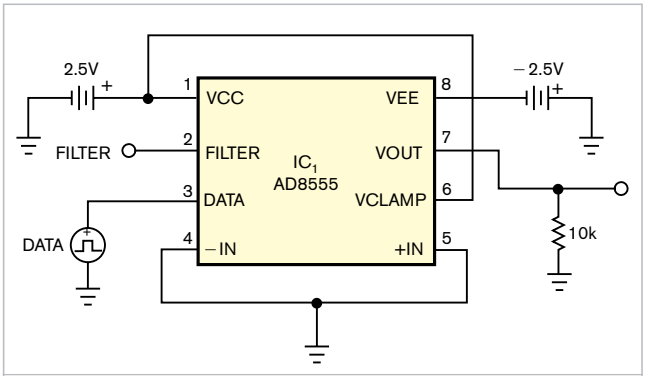


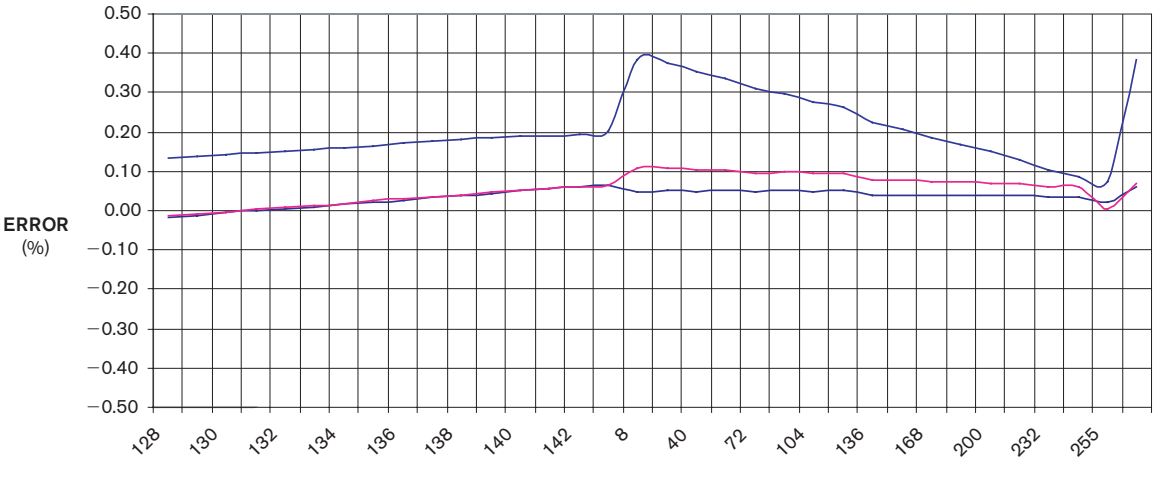
Figure 1 Occupying a tiny, eight-lead LFCSP footprint, a programmable instrumentation amplifier doubles as a last-minute adjustable-voltage bipolar-reference source.

The following equation describes the DAC's approximate internal reference voltage, V_{DAC}:

$$V_{DAC} \approx \left(\frac{CODE + 0.5}{256}\right)(V_{DD} - V_{SS}) + V_{SS},$$

and the following equation yields the circuit's output voltage, V_{OUT}: $V_{OUT} = GAIN(V_{POS} - V_{NEG}) + V_{DAC}$, in which GAIN represents the circuit's default internal gain of 70 for the differential input. Both inputs connect to ground, and the first term is thus close to 0V, or 10 µV maximum due to input-amplifier errors, and the circuit's output voltage, V_{OUT}, is equal to V_{DAC}.

Until you permanently program the internal registers, they allow you to alter the output voltage and explore the circuit's behavior as a fixed-voltage reference and reprogrammable 8-bit DAC. To program the output voltage, you apply the appropriate pattern according to the first equation and instructions from the device's data sheet. After verification, you can permanently set the output voltage by blowing certain of the device's internal polysilicon-fuse resistors. As **Figure 2** shows, for a given output-voltage level, the device's absolute error is less than 0.4% across a −40 to +140°C temperature range. EDN



NOTE: PERCENTAGE ERROR = $100 \times \frac{V_{OUT(ACTUAL)} - V_{OUT(CALCULATED)}}{5V\ FULL\text{-}SCALE}$.

Figure 2 Output-voltage error for the reference circuit reaches a maximum of 0.4% at a temperature of −40°C and a 5V power supply.

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Precision full-wave signal rectifier needs no diodes

José M Blanes and José A Carrasco,
University Miguel Hernández, Elche, Spain

Rectifier circuits based on semiconductor diodes typically handle voltage levels that greatly exceed the diodes' forward-voltage drops, which generally don't affect the accuracy of the rectification process. However, the rectified signal's accuracy suffers when the diode's voltage drop exceeds the applied voltage. Precision rectifier circuits combine diodes and operational amplifiers to eliminate the effects of diode voltage drops and enable high-accuracy, small-signal rectification. By taking advantage of modern operational amplifiers that can handle rail-to-rail inputs and outputs, the circuit in Figure 1 dispenses with diodes altogether, provides full-wave rectification, and operates from a single power supply.

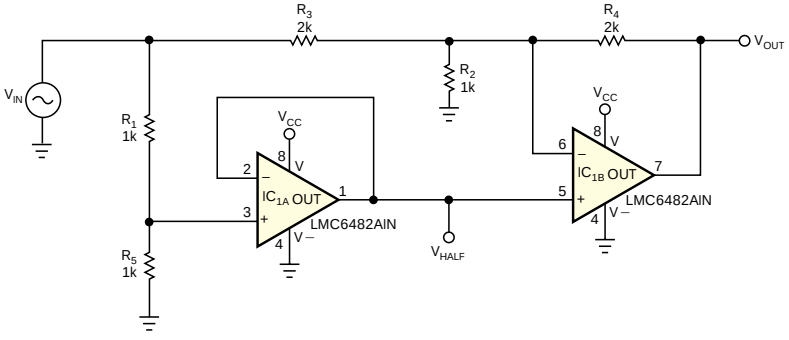


Figure 1 This precision full-wave-rectifier circuit uses two op amps and no diodes. When altering the basic design, note that resistors R_3 and R_4 are both twice the value of R_2 and that R_1 and R_5 are equal.

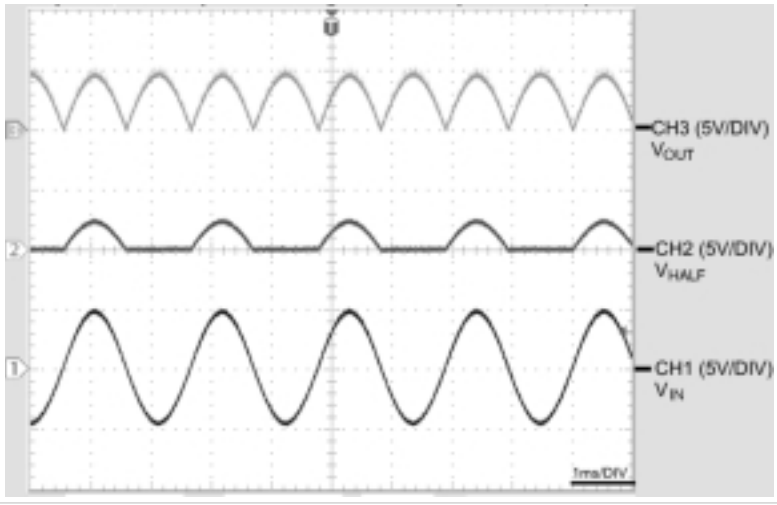


Figure 2 From bottom to top, the waveforms show V_{IN} (CH1), V_{HALF} (CH2), and V_{OUT} (CH3).

The circuit operates as follows: If $V_{IN}>0V$, then IC_{1A}'s output, V_{HALF}, equals $V_{IN}/2$, and IC_{1B} operates as a subtracter, delivering an output voltage, V_{OUT}, equals V_{IN}. In effect, the circuit operates as a unity-gain follower. If $V_{IN}<0V$, then $V_{HALF}=0V$, and the circuit behaves as a unity-gain inverter and delivers an output of $V_{OUT}=-V_{IN}$. Figure 2 shows the circuit's input signal at V_{IN}; its intermediate voltage, V_{HALF}; and its output voltage, V_{OUT}.

The circuit uses a single National Semiconductor LMC6482 chip and operates in the linear regions of both operational amplifiers. Suggested applications include low-cost rectification for automatic gain control, signal demodulation, and process instrumentation. The circuit relies on only one device-dependent property: The amplifiers must not introduce phase inversion when the input voltage exceeds the negative power supply; the LMC6482 meets this requirement. EDN

DIs Inside

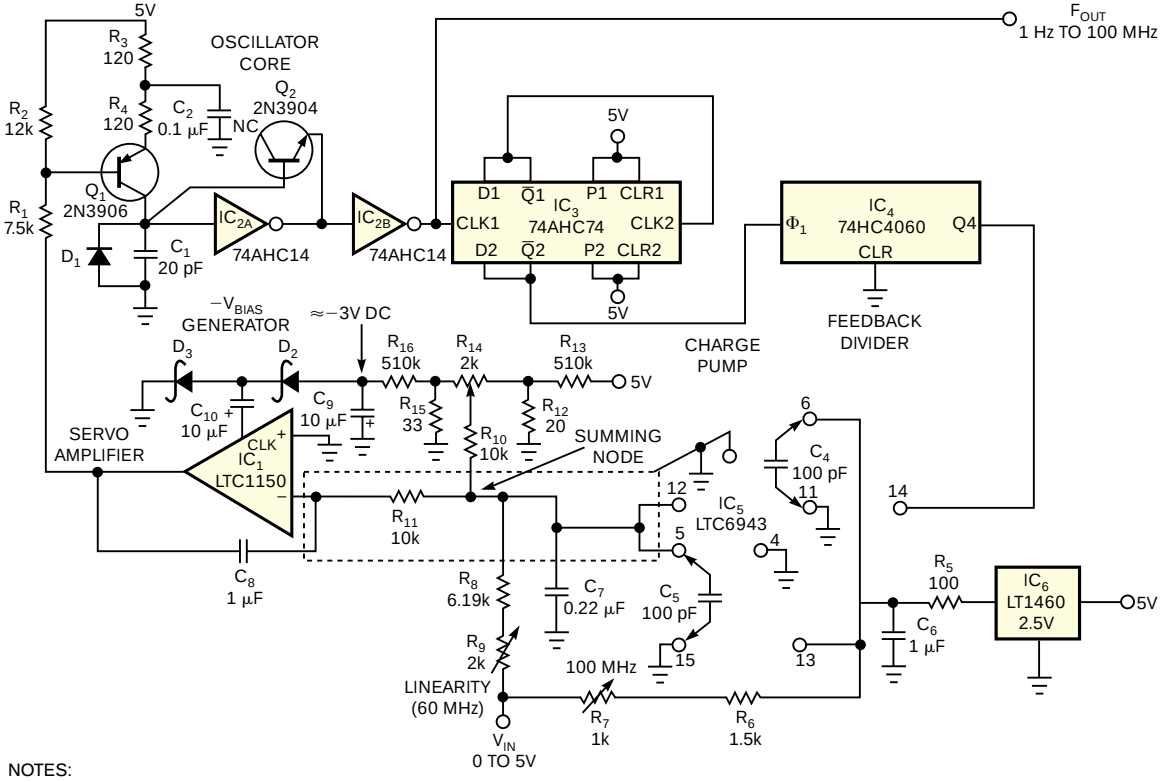
1-Hz to 100-MHz VFC features 160-dB dynamic range

Jim Williams, Linear Technology Corp

The VFC (voltage-to-frequency-converter) circuit in Figure 1 achieves a wider dynamic range and a higher full-scale output frequency—100 MHz with 10% overrange to 110 MHz—by a factor of 10 over any commercially available converter. The circuit's 160-dB dynamic range spans eight decades for a 0 to 5V input range and allows continuous operation down to 1 Hz. Additional specifications include 0.1% linearity, a 250-ppm/°C gain/temperature coefficient, a 1-Hz/°C zero-point shift, and a 0.1% frequency shift for a 10% power-supply-voltage variation. A single 5V supply powers the circuit.

Chopper-stabilized amplifier IC_1, an LTC-1150, controls a crude but wide-range oscillator core comprising bipolar transistors Q_1 and Q_2 and inverters IC_{2A} and IC_{2B}. In addition to delivering a logic-level output, the oscillator core clocks divide-by-four counter IC_3, which in turn drives IC_4, a 74HC4060 configured as a divide-by-16 counter.

After undergoing a total division by 64 in IC_3 and IC_4, the oscillator core's output drives a charge pump comprising IC_5, an LTC6943, and its associated components. The averaged difference between the charge pump's output and the applied input voltage appears at the summing node and biases IC_1, thereby closing the control loop around the wide-range oscillator core.



NOTES:
1. D_1: JPAD-500, D_2, D_3: BAT-85, R_5, R_6, R_8: TRW-IRC TYPE MAR-6, 1% METAL-FILM, C_4, C_5: WIMA TYPE FKP-2 CAPACITORS, AND C_7, C_8: WIMA TYPE MKS-2 CAPACITORS.
2. CONNECT ALL COMPONENTS AT Q_1'S COLLECTOR WITH A MINIMUM-AREA AIR-INSULATED "FLOATING" JUNCTION OVER A RELIEVED AREA OF GROUND TO MINIMIZE STRAY CAPACITANCE.
3. ENCLOSE R_{11} AND ITS CONNECTIONS TO R_9, R_{10}, IC_1'S INVERTING INPUT, C_7, AND PINS 5 AND 12 OF IC_5 WITHIN SOLDER- AND COMPONENT-SIDE GUARD TRACES TO INTERCEPT ANY BOARD-SURFACE LEAKAGE CURRENTS. (NOTE THAT THE DASHED LINE DEFINES THE GUARD TRACE.)
4. CONNECT IC_2'S UNUSED INPUTS TO GROUND. THE SCHEMATIC OMITS POWER-SUPPLY CONNECTIONS TO MOST ICS FOR CLARITY

Figure 1 Featuring a 160-dB dynamic range corresponding to a 1-Hz- to 100-MHz-frequency span, this voltage-to-frequency converter operates from a single 5V power supply.

The circuit's extraordinary dynamic range and high speed derive from the oscillator core's characteristics, the divider/charge-pump-based feedback loop, and IC_1's low dc input errors. Both IC_1 and IC_5 help stabilize the circuit's operating point by contributing to overall linearity and stability. In addition, IC_1's low offset drift ensures the circuit's 50-nV/Hz gain-versus-frequency characteristic slope and permits operation as low as 1 Hz at 25°C.

Applying a positive input voltage causes IC_1's output to go negative and alter Q_1's bias. In turn, Q_1's collector current produces a voltage ramp on C_1 (upper trace in Figure 2). The ramp's amplitude increases until Schmitt trigger inverter IC_{2A}'s output (lower trace in Figure 2) goes low, discharging C_1 through Q_2 (connected as a low-leakage diode). Discharging C_1 resets IC_{1A}'s output to its high state, and the ramp-and-reset action continues.

The leakage current of diode D_1, a Linear Systems JPAD-500, dominates all other parasitic currents in the oscillator core, but its 500-pA maximum leakage ensures operation as low as 1 Hz. The two sections of charge pump IC_5 operate out of phase and transfer charge at each clock transition. Components critical to the charge pump's stability include a 2.5V LT-1460 voltage reference, IC_6; two Wima FKP-2 polypropylene film/foils; 100-pF capacitors, C_4 and C_5; and the low charge-injection characteristics of IC_5's internal switches.

The 0.22-µF capacitor, C_7, averages the difference signal between the input-derived current and the charge pump's output and applies the smoothed dc signal to amplifier IC_1, which in turn controls the bias applied to Q_1 and thus the circuit's operating point. As noted, the circuit's closed-loop-servo action reduces the oscillator's drift and enhances its high linearity. A 1-µF Wima MKS-2 metallized-film-construction capacitor, C_8, compensates the servo loop's frequency response and ensures stability. Figure 3 illustrates the loop's well-behaved response (lower trace) to an input-voltage step (upper trace).

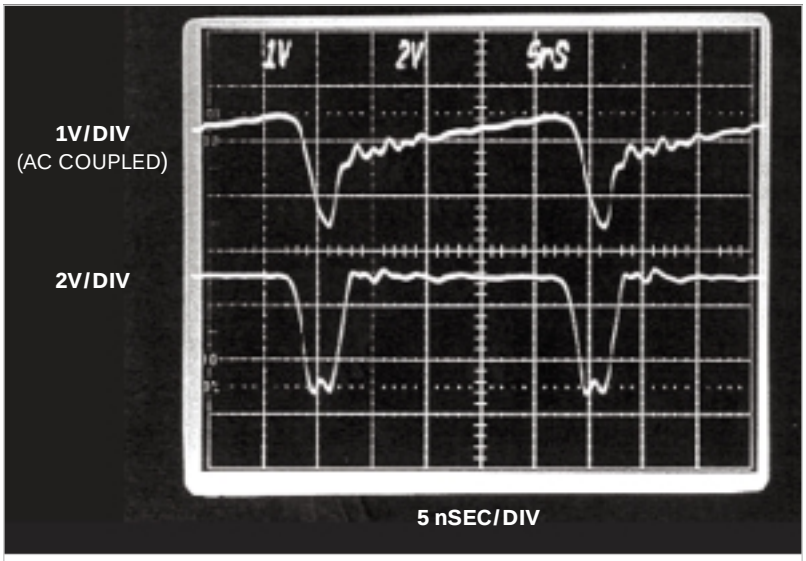


Figure 2 On a 700-MHz real-time oscilloscope, the oscillator-core waveforms at a 40-MHz operating frequency show the ramp-and-reset waveform at Q_1's collector (upper trace) and Q_2's emitter (lower trace).

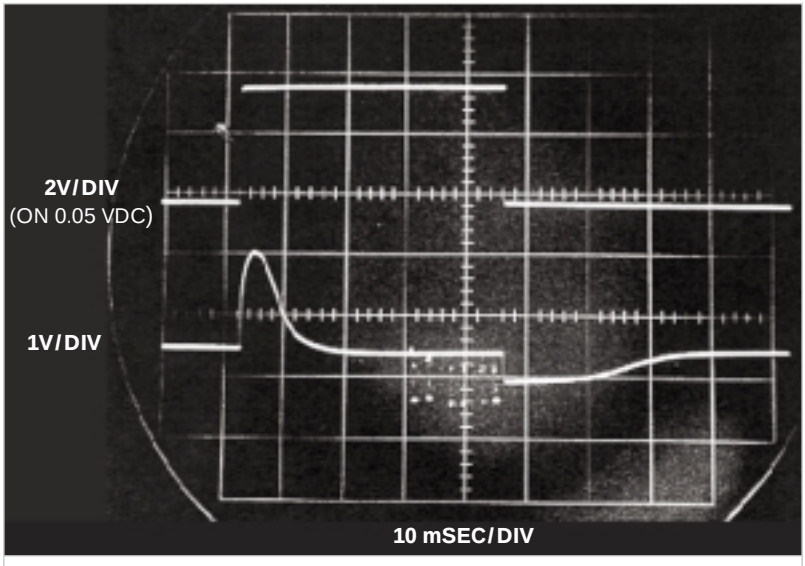


Figure 3 In response to an input-voltage step (upper trace), the voltage at the circuit's summing junction shows a 30-msec settling time.

For the circuit to achieve its design goals, certain special techniques and considerations apply. Diode D_1's leakage current dominates all other parasitic leakage currents at IC_{2A}'s input, and thus Q_1 must always supply sufficient source current to sustain oscillation and ensure operation as low as 1 Hz.

The circuit's 100-MHz full-scale upper frequency limit forces stringent restrictions on the oscillator core's cycle time, and only 10 nsec is available for a complete ramp-and-reset sequence. The reset interval imposes an ultimate speed limit on the circuit, but the upper trace in Figure 2 shows a 6-nsec reset interval that falls comfortably within the 10-nsec limit. A path from the cir-

cuit's input to the charge pump's output allows for correction of small nonlinearities due to residual charge injection. This input-derived correction is effective because the charge injection's effects vary directly with the oscillation frequency, which the input voltage determines.

Although you can use the component values given in Figure 1 to assemble prototypes and small production quantities of the circuit, you need to consider component selection for optimum manufacturability and high-volume production. Table 1 lists certain components' target values and estimated selection yields. The notes in Figure 1 list the key components that the design uses.

To calibrate the circuit, apply 5V to the input and adjust the 100-MHz trimmer, R_7 for a 100-MHz output. Next, connect the input to ground and adjust trimmer R_{13} for a 1-Hz output. Allow for an extended settling interval because, at this frequency, the charge-pump update occurs once every 32 sec. Note that R_{13}'s adjustment range accommodates either a positive or a negative offset voltage because IC_1's clock output generates a negative bias voltage for R_{13}. Next, apply 3V to the input and adjust R_9 for a 60-MHz output. A certain amount of interaction occurs among the adjustments, so repeat the process until you arrive at optimum values for the three calibration frequencies. EDN

TABLE 1 SELECTION CRITERIA FOR COMPONENTS

Component	Selection parameter at 25°C	Typical yield (%)
Q_1	I_{CER}<20 pA at 3V	90
Q_2	I_{EBO}<20 pA at 3V	90
D_1	75 pA at 3V; I_{REV}<500 pA	80
IC_{2A}	I_{IN}<25 pA	80
IC_1	I_B<5 pA at V_{CC}=5V	90
IC_{2A}, IC_{2B}	Must toggle with 3.6-nsec-wide (at-50%-level) input pulse	80

Cascode MOSFET increases boost regulator's input- and output-voltage ranges

Scot Lester, Texas Instruments, Dallas, TX

Targeting use in portable-system applications that require raising a battery's voltage to a higher level, IC boost regulators often include output transistors that can drive storage inductors. However, most boost regulators' absolute-maximum input-voltage rating typically doesn't exceed 6V, an adequate level for battery operation. In addition, breakdown voltage of the regulator's output transistor limits the regulator's absolute-maximum output voltage to 25 to 30V, which may be too low for some applications.

You can extend a boost regulator's output-voltage range by adding an external transistor that has a higher breakdown voltage than the regulator. However, the internal design of a typical boost regulator's control circuitry often prevents direct drive of an external transistor's base or gate. As an alternative, you can add an external higher voltage transistor by connecting it in a cascode configuration.

Most boost regulators feature a peak-current-control method that reduces the number of external components and thus shrinks the overall pc-board area of the converter circuit. Figure 1 shows a boost regulator based on a TPS61040 boost controller, IC_1, which uses peak-current control.

Applying input voltage V_{IN} to IC_1's V_{CC} pin and to one leg of inductor L_1 turns on IC_1's internal MOSFET switch, Q_1, allowing a gradually increasing amount of current to flow from V_{IN} through L_1, Q_1, and internal current-sense resistor R_1. The circuit's internal controller monitors the volt-

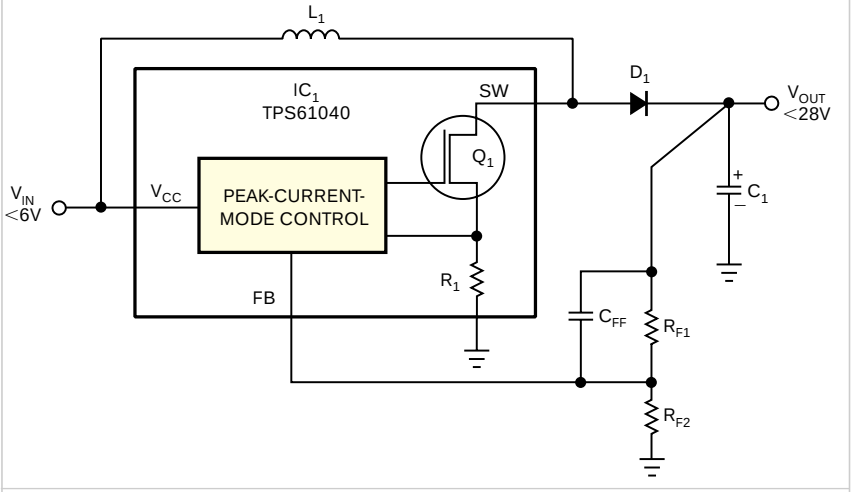


Figure 1 Based on the "barefoot" TPS61040, this dc/dc boost converter delivers output voltages only within IC_1's ratings.

age across sense resistor R_1 and, upon reaching a predetermined current limit, turns off Q_1.

Interrupting the current through L_1 raises the voltage across the inductor and applies forward bias to diode D_1, which conducts and charges output capacitor C_1 to a higher voltage than would be available from the input voltage alone. The input voltage, L_1's inductance, and the preset peak current through R_1 all affect Q_1's on-time, and the output voltage sensed by IC_1's FB (feedback) pin and its external components determines Q_1's off-time. To maintain operation and set Q_1's off-time, IC_1's internal controller must monitor current through L_1 using Q_1 and R_1.

You can add a higher voltage MOSFET transistor, Q_2 (Figure 2), for applications that require an output voltage higher than the internal transistor's breakdown voltage. To maintain the circuit's current-flow path through L_1 and IC_1's SW pin, you connect the external transistor in a cascode, or common-gate, configuration.

Q_2 comprises a low-on-resistance, low-gate-voltage-threshold MOSFET with the addition of diode D_2 between Q_2's gate and source. To ensure the circuit's proper operation, V_{CC}—5V in this example—must exceed Q_2's gate-threshold turn-on voltage. In operation, IC_1's internal control circuit turns on Q_1, which pulls Q_2's source close to ground level and turns on Q_2 with almost 5V of gate-to-source potential.

Current flows through inductor L_1, external transistor Q_2, internal transistor Q_1, and sense resistor R_1, and IC_1's control circuit "sees" no difference with the installation of Q_2. Once the inductor current reaches its preset limit, Q_1 turns off, leaving Q_2 with no path for current to flow from its source. The voltage on Q_2's drain rises rapidly to the desired output voltage plus the voltage drop across D_1. As the drain voltage rises, Q_2's drain-to-source capacitance attempts to pull the MOSFET's floating source above 5V, which forward-biases D_2, connects IC_1's SW pin voltage to 5V plus one diode drop, and clamps Q_2's source to the same voltage.

A boost converter delivers a 180V output at 4 mA (V_{OUT}) to bias a laser circuit from a 9V power supply (V+). In this application, the 5V input supply need provide only enough current—typically, a few milliamperes—to drive IC_1's internal logic and the gate of cascode MOSFET Q_2. You can use a dropping resistor and zener-diode voltage regulator (not shown) to supply the 5V requirement from the 9V supply. You can drive the inductor and IC_1 from a common power supply or from a separate source that's within Q_2's breakdown-voltage rating. The cascode circuit also can produce any output voltage that's within Q_2's drain-to-source breakdown-voltage rating. Specify other components with an appropriate voltage rating—for example, breakdown-voltage ratings of inductor L_1 and capacitor C_1 should safely exceed the desired output voltage. EDN

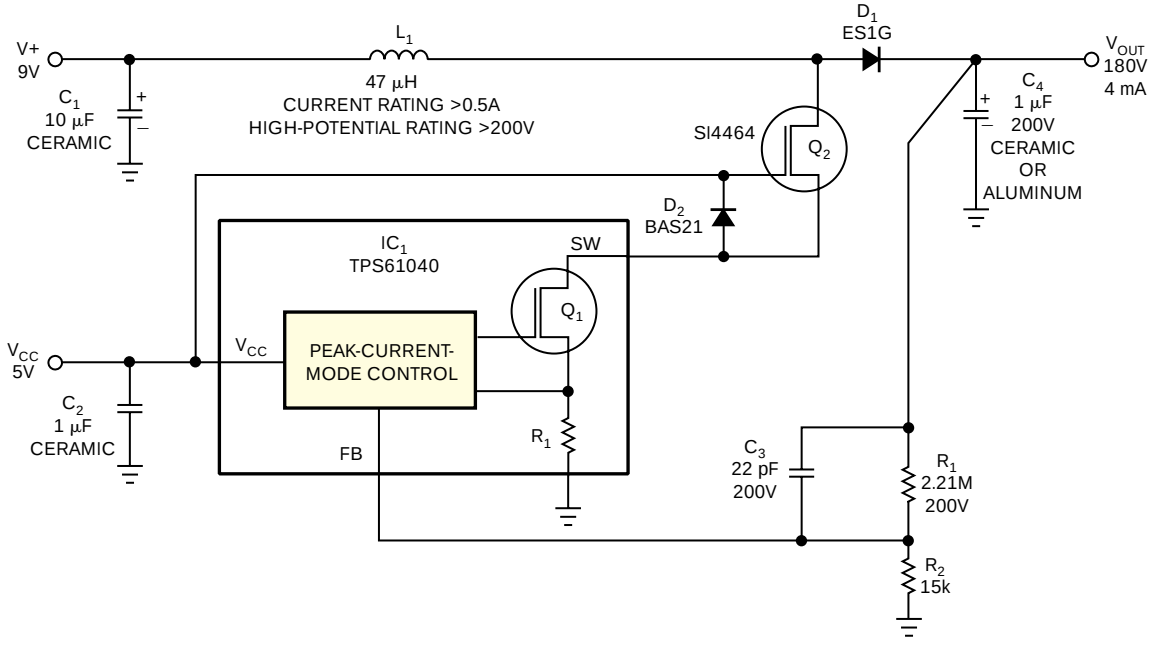


Figure 2 Adding an external cascode-connected MOSFET transistor, Q_2, with higher breakdown-voltage ratings, enables the circuit to produce higher output voltages.

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Buffer amplifier and LED improve PWM power controller's low-load operation

Gregory Mirsky, LaMarche Manufacturing Co, Des Plaines, IL

Texas Instruments' UCC3895 offers a good base for building a high-efficiency, pulse-width-modulated, switched-mode power supply that suits either current- or voltage-mode control. Designed for driving a full-bridge power inverter using two sets of complementary outputs, Out A through D, the circuit controls power by phase-shifting outputs C and D with respect to A and B. The manufacturer's data sheet provides a detailed description (**Reference 1**). However, when lightly loaded and configured for current-mode control, the controller can produce asymmetric-width pulses on its lagging outputs, C and D, under start-up conditions. **Reference 2** provides a complete description of the problem and a workaround.

Unfortunately, the workaround evokes other problems when you use the IC in other circuit implementations. **Figure 1**, from **Reference 2**, shows a partial schematic featuring the UCC3895 in a peak-current-mode-control circuit in which R_1 serves as a pullup resistor, providing a dc offset for the voltage ramp. However, for a significant portion of the ramp waveform, diode D_1 doesn't conduct and therefore narrows the power supply's dynamic range by cutting off a portion of the ramp voltage at IC_1's Pin 3.

Figure 2 shows another approach that requires additional components but delivers the full magnitude of the voltage ramp to Pin 3 of IC_1 and provides the approximately 1V-dc offset that **Reference 1** requires. Transistors Q_1 and Q_2, resistors R_1 and R_2, and LED D_3 form an emitter-follower amplifier for the ramp voltage available at IC_1, Pin 7 across timing capacitor C_1. This arrangement provides reliable current-mode operation over the full range from no-load to full-load output current by delivering a

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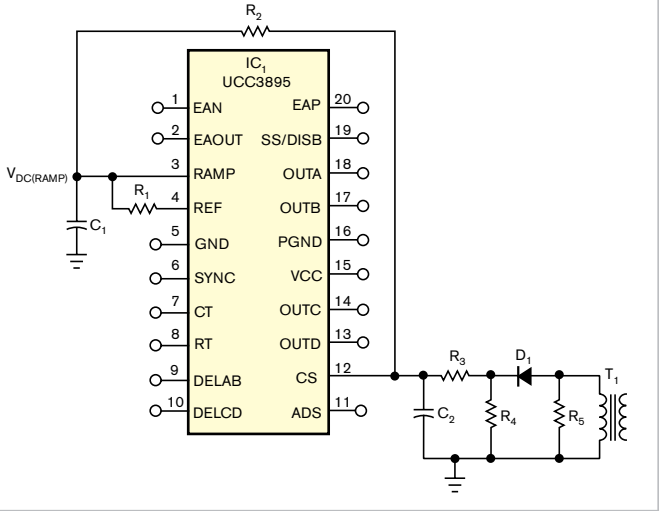


Figure 1 An added resistor, R_1, helps improve light-load operation of a popular switched-mode power-supply controller by eliminating output asymmetry.

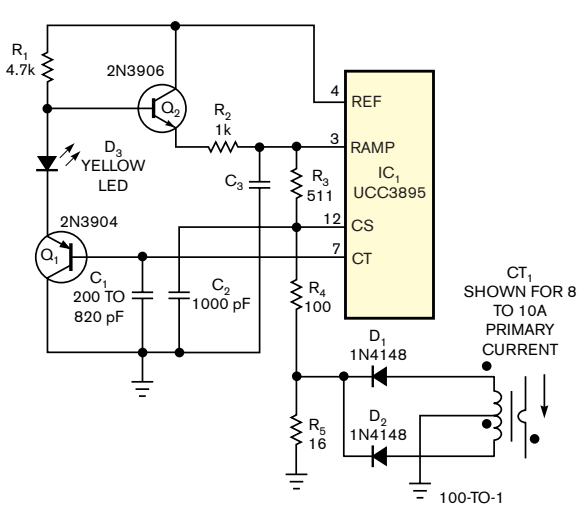


Figure 2 For even better performance, add a level-shifting amplifier to the ramp-voltage path.

sawtooth drive with a dc offset to IC_1's ramp input. Diode D_3, a yellow LED, performs a 1.7V level translation without introducing any substantial signal loss. The component values not shown depend on the application. EDN

REFERENCES

1 "UCC3895 BICMOS Advanced Phase Shift PWM Controller," Texas Instruments data sheet, http://focus.ti.com/docs/prod/folders/print/ucc3895.html.

2 Mappus, S, "UCC3895 OUTC/OUTD Asymmetric Duty Cycle Operation," Texas Instruments Application Report, SLUA275, September 2002.

Temperature controller has "take-back-half" convergence algorithm

W Stephen Woodward, University of North Carolina, Chapel Hill, NC

"The unfortunate relationship between servo systems and oscillators is very apparent in thermal-control systems," says Linear Technology's Jim Williams (**Reference 1**). Although high-performance temperature control looks simple in theory, it proves to be anything but simple in practice. Over the years, designers have devised a long laundry list of feedback techniques and control strategies to tame the dynamic-stability gremlins that inhabit temperature-control servo loops. Many of these designs integrate the temperature-control error term T_S-T in an attempt to force the control-loop error to converge toward zero (**Reference 2**).

One tempting and "simple" alternative approach makes the heater power proportional to the integrated temperature error alone. This "straight-integration" algorithm samples the temperature, T, and subtracts it from the setpoint, T_S. Then, on each cycle through the loop, the loop gain, F, multiplies the difference, T_S-T, and adds it as a cumulative adjustment to the heater-power setting, H. Consequently, $H=H+F\times(T_S-T)$.

The resulting servo loop offers many desirable properties that include simplicity and zero steady-state error. Unfortunately, as **Figure 1** shows, it also exhibits an undesirable property: an oscillation that never allows final convergence to T_S. Persistent oscillation is all but inevitable because, by the time that the system's temperature corrects from a deviation and struggles back to $T=T_S$, the heater power inevitably gets grossly overcorrected. In fact, the resulting overshoot of H is likely to grow as large as the original perturbation. Later in the cycle, H's opposite undershoot grows as large as the initial overshoot, and so on.

Acting on intuition, you might attempt to fix the problem by adopting a better estimate of H whenever the system's temperature crosses the setpoint, $T=T_S$). This Design Idea outlines a TBH (take-back-half) method that takes deliberate advantage of the approximate equality of straight-integration's undamped overshoots and undershoots. To do so, you introduce variable H_O and run the modified servo loop, except for the instant when the sampled temperature, T, passes through the setpoint, $T=T_S$. Whenever a setpoint crossing occurs, the bisecting value $(H+H_O)/2$ replaces both H and H_O. As a result, at each setpoint crossing, H and H_O are midway between the values corresponding to

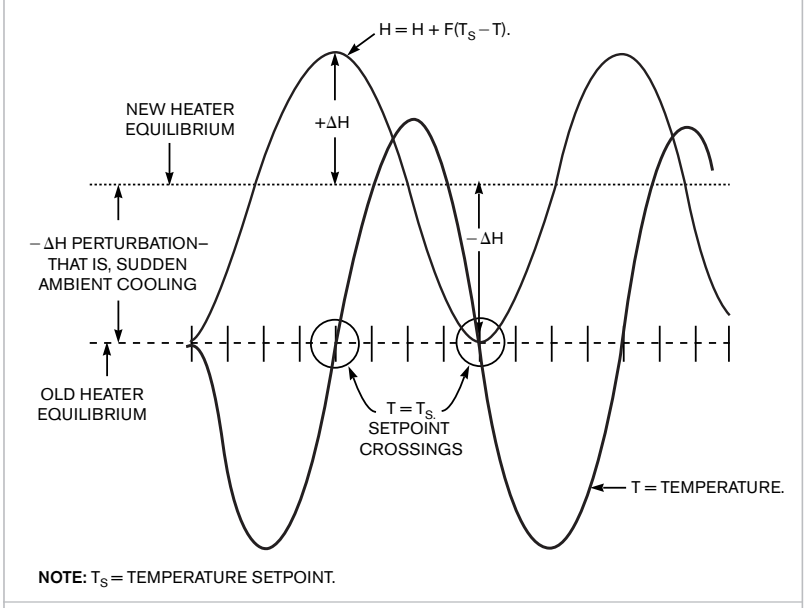


Figure 1 A simple integrating control algorithm virtually guarantees that the system's temperature oscillates and never converges to the setpoint temperature, T_S.

the current (H) and previous (H_O) crossings. This action takes back half of the adjustment applied to the heater setting between crossings. **Figure 2** shows how a simulated TBH algorithm forces rapid half-cycle convergence.

Successful applications of the TBH algorithm range from precision temperature control of miniaturized scientific instrumentation to managing HVAC (heating/ventilation/air-conditioning) settings for crew rest areas in Boeing's 777 airliner. Experience with TBH applications shows that, with a reasonable choice for loop gain, F, the algorithm exhibits robust stability.

In general, a TBH system's natural cycle time is proportional to the square root of the ratio of the thermal time constant to F. Based on both simulations and experiments, a cycle time that's at least eight times longer than

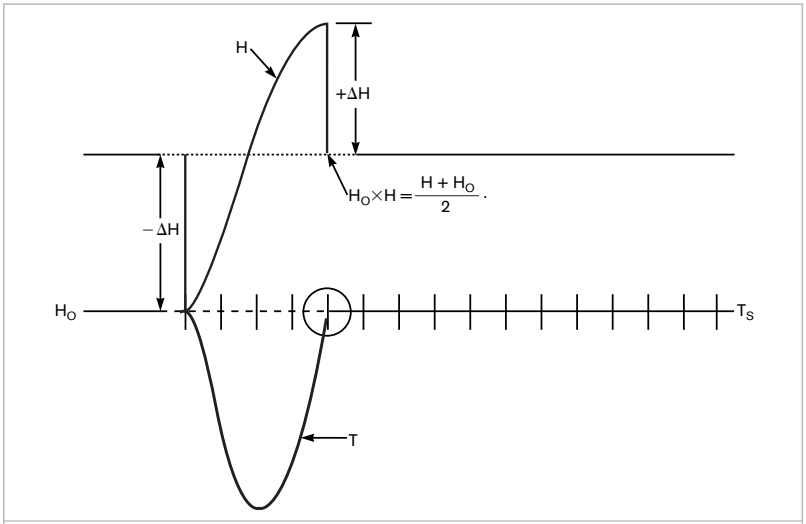
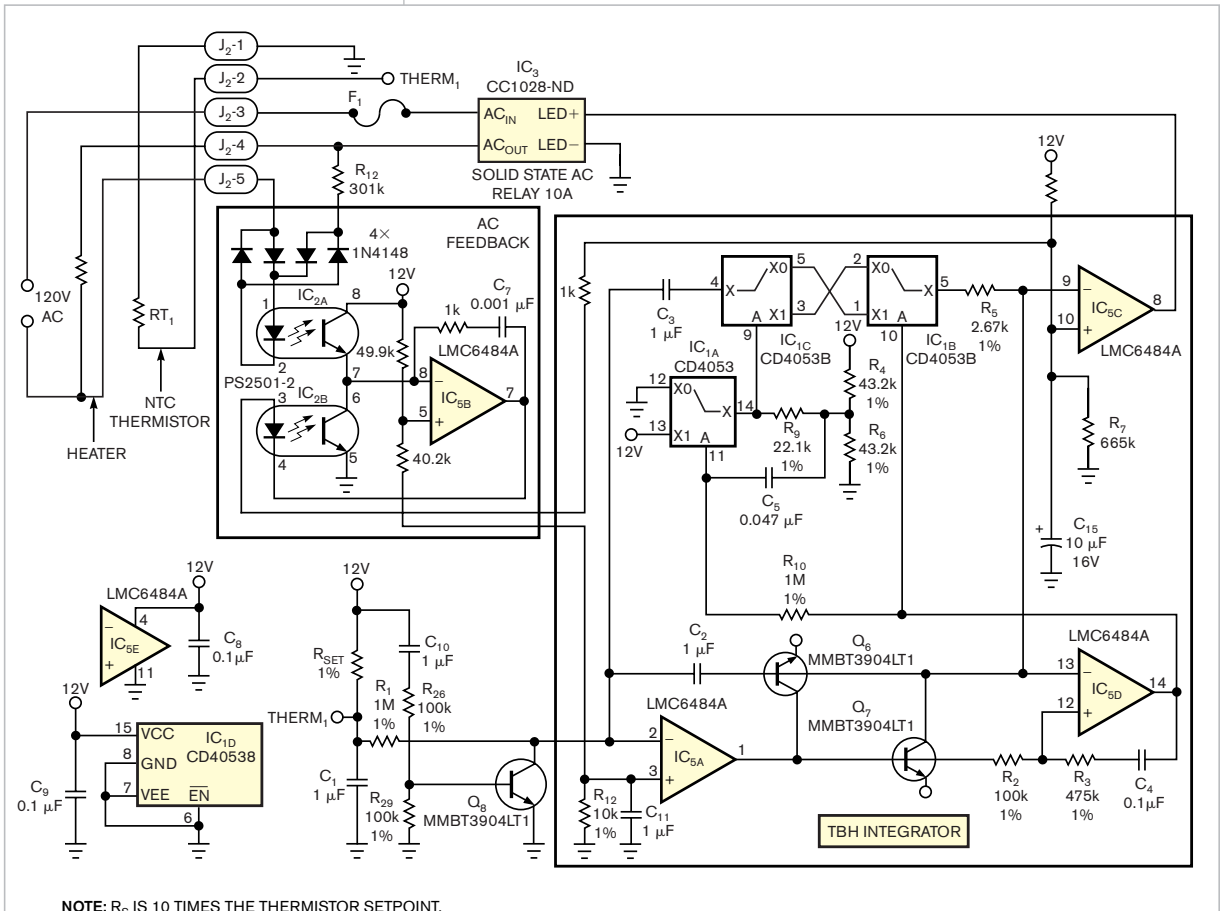


Figure 2 In this simulation, applying the "take-back-half" algorithm forces convergence to the setpoint value in a single half-cycle.



NOTE: R_S IS 10 TIMES THE THERMISTOR SETPOINT.

Figure 3 For safety, this version of a TBH heater controller features full isolation of the ac-line and control circuits.

the heater-sensor time delay ensures convergence. Therefore, setting loop gain F low always achieves convergence, and the steady-state error, $T_S - T$, remains equal to zero.

Figure 3 shows a practical example of a TBH controller that's suitable for managing large thermal loads. Thermistor RT_1 senses heater temperature. The output of error-signal integrator IC_{5A} ramps negative when $T<T_S$ and ramps positive when $T_S>T$, producing a control signal that's applied to comparator IC_{5C}, which in turn drives a solid-state relay, IC_3, which is rated for 10A loads.

Comparator IC_{5D} and the reverse-parallel diodes formed by the collector-base junctions of Q_6 and Q_7, and the CMOS switches of IC_1 perform the TBH zero-crossing convergence function.

In most temperature-control circuits, it's advantageous to apply a reasonably linear feedforward term that represents the actual ac voltage applied to the heater; the need for complete galvanic isolation between the control and the power-handling circuits complicates this requirement. In this example, a linear isolation circuit comprising a PS2501-2 dual-LED/phototransistor optoisolator (IC_{2A} and IC_{2B}) and op-amp IC_{5B} delivers feedback current to C_{15} and IC_{5C} that's proportional to the averaged ac heater current. As a bonus, the feedback circuit provides partial instantaneous compensation for ac-line voltage fluctuations. EDN

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1 Williams, Jim, *Linear Applications Handbook*, Linear Technology, 1990.
2 "Hybrid Digital-Analog Proportional-Integral Temperature Controller," www.discovercircuits.com/C/control3.htm.

MOSFET enhances low-current measurements using moving-coil meter

Stefan Strózecki, Institute of Telecommunications ATR, Kaliskiego, Poland

A previous Design Idea describes an interesting and useful method for using a moving-coil analog meter to measure currents in the less-than-1A range (**Reference 1**). The design offers considerable flexibility in the choice of meter-movement sensitivity and measurement range and simplifies selection of shunt resistors. Although the design uses a bipolar meter-driver transistor, under some circumstances, a MOSFET transistor represents a better choice. The original circuit comprises a voltage-controller current sink that measures the bipolar transistor's emitter current, but the transistor's collector current drives the analog meter. A bipolar transistor's emitter and collector currents, I_E and I_C, respectively, are not identical because base current, I_R, adds to the emitter current.

You can express these current components as $I_E=I_C+I_B$ and then as $I_C=I_E-I_B$. Whether base current adversely affects the measurement accuracy depends on the magnitude of I_B and the magnitude of the common-emitter current gain, β, because base current $I_B=I_C/\beta$. When β is greater than 100, the base current's contribution to emitter current is generally negligible. However, β is sometimes smaller. For example, the general-purpose BC182, an NPN silicon transistor, has a low-current β of only 40 at room temperature. If you were to use a 15-mA-full-scale meter in the transistor's collector, full-scale base current I_B at minimum β would amount to 0.375 mA. Subtracting base current from collector current introduces a 2.5% error.

But if you use a moving-coil meter that requires 150 µA for full-scale deflection, the measurement error increases considerably because β decreases as collector current decreases. For the BC182, reducing collector current from a few milliamps to 200 µA, current gain decreases β by a factor of 0.6 and adversely affects the meter reading's accuracy.

To solve the problem and improve the circuit's accuracy, you can replace the

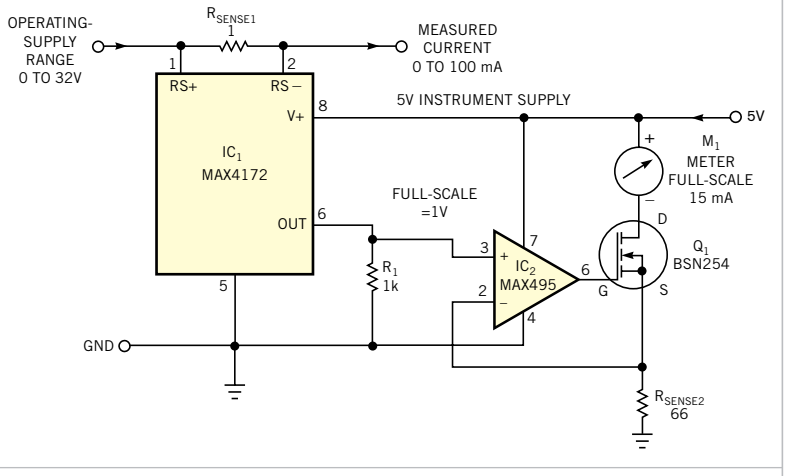

Figure 1 This updated version of an earlier Design Idea uses a MOSFET to drive an analog meter display, offering great flexibility in power-supply-current measurement.

BC182 with an N-channel MOSFET, such as the BSN254 (**Figure 1**). Because a MOSFET draws no gate current, its drain current, I_D, equals its source current, I_S. When you select a MOSFET for the circuit, note that the device's gate-source threshold voltage should be as low as possible. For example, the BSN254 has a room-temperature gate-source threshold-voltage range of 0.8 to 2V. The remainder of the circuit design proceeds as in the original Design Idea; that is, for a maximum voltage drop of 1V across R_1, you calculate R_{SENSE2} as follows: $R_{SENSE2}=(1V/I_{METER})$, where R_{SENSE} is in ohms, 1V represents the voltage drop across R_1, and I_{METER} is the full-scale meter reading in amps. Note that a 1-kΩ resistor at R_1 develops 10V/1A output across sense resistor R_{SENSE1}. In this application, 100 mA produces 0.1V across R_{SENSE1}, and the voltage across R_1 thus corresponds to 1V for full-scale deflection of the meter. EDN

REFERENCE

1 Bilke, Kevin, "Moving-coil meter measures low-level currents," *EDN*, March 3, 2005, pg 72, www.edn.com/article/CA505070.

Shunt regulator serves as inexpensive op amp in power supplies

Michael O'Loughlin, Texas Instruments, Nashua, NH

Developed as a three-terminal shunt regulator, the popular and multiple-sourced TL431 IC offers designers many intriguing possibilities beyond its intended application. Internally, the TL431 comprises a precision voltage reference, an operational amplifier, and a shunt transistor (**Figure 1a**). In a typical voltage-regulator application, adding two external resistors, R_A and R_B, sets the shunt-regulated output voltage at the lower end of load resistor R_S (**Figure 1b**).

In today's power-supply market, cost reduction drives most designs, as evidenced by Asian manufacturers that have resorted to shaving pennies off their power-supply products by using single-sided pc boards. This Design Idea shows how a three-terminal shunt regulator can replace a more expensive conventional operational amplifier in a power-converter design.

A switched-mode power supply uses a galvanically isolated feedback portion of a PWM circuit (**Figure 2**). In designs that omit a voltage amplifier, a shunt regulator can serve as an inexpensive op amp. Resistors R_1 and R set the power supply's dc output voltage, and optocoupler IC_2 provides galvanic isolation. Resistor R_1 provides bias for the optocoupler and the TL431, IC_1. Resistor R_3 and zener diode D_1 establish a fixed bias voltage to ensure that bias resistor R_1 does not form a feedback path. Resistors R_1 and R_2 control the gain across the optocoupler. In most designs, the ratio of R_2 to R_1 is roughly 10-to-1.

Components C_P, C_Z, and R_Z provide frequency compensation for the control loop. The optocoupler includes a high-frequency pole, f_P, in its frequency response, an item that most optocouplers' data sheets omit. You can use a network analyzer to determine the location of the high-frequency pole or estimate that the pole occurs at approximately 10 kHz. The following **equation** describes the compensation network's small-signal transfer function:

$$G_C(s)=\frac{\Delta V_{ERR}}{\Delta V_{OUT}}=\frac{(s\times R_Z\times C_Z+1)}{s\times R_1(C_Z+C_P)\left(\frac{s\times R_Z\times C_P\times C_Z}{C_P+C_Z}+1\right)}\times\frac{R_2}{R_1}\times\left(\frac{1}{\left(\frac{s}{2\times\pi\times f_P}+1\right)}\right).$$

Note that, under some circumstances, adding a bypass capacitor across diode D_1 may be necessary for output-noise reduction. EDN

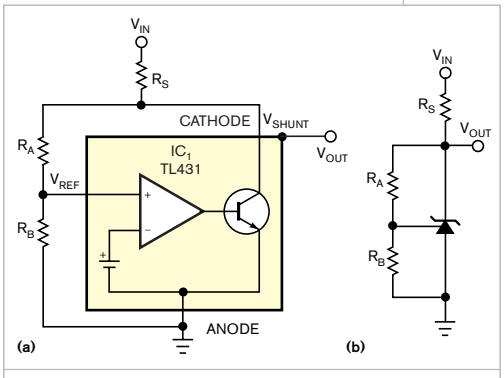

Figure 1 Despite the block diagram, the TL431 is internally complex (a), but you need only three external resistors to use the TL431 in a basic shunt-regulator circuit (b).

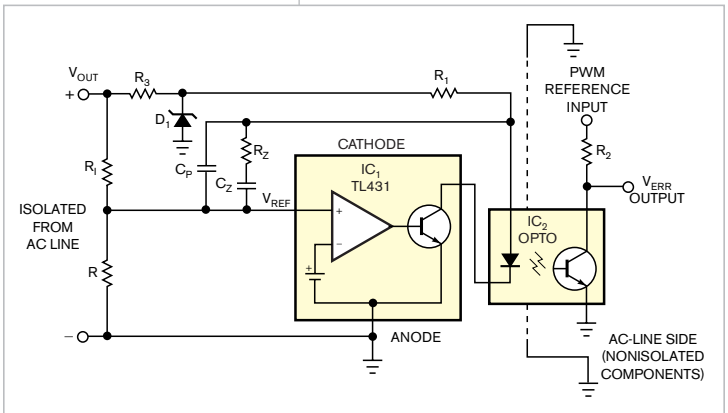

Figure 2 A TL431 replaces a more expensive operational amplifier in this power supply's PWM feedback-regulator circuit.

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Keyboard links to microcomputer through one-wire interface

Israel Schleicher, Prescott Valley, AZ

A previous Design Idea described a single-wire-plus-ground-return, keypad-to-microcontroller interface in which a single pulse represents each keystroke (**Reference 1**). The pulse's width is proportional to the key's numerical value, and the microcontroller identifies the pressed key by measuring the pulse width. Component tolerances and the accuracy of the microcontroller's internal oscillator limit the original design to keypads with 16 or fewer keys—that is, four rows by four columns or smaller cross-point-key matrix. This Design Idea illustrates how a relatively simple modification applies the method to much larger keypads. (The following description omits a few details from the original Design Idea, which you can find online at www.edn.com/article/CA512131.)

You can divide a large keypad or keyboard into sections of 12 keys each (**Figure 1**). Each section connects to a separate comparator circuit, which detects a keystroke and generates a trigger pulse using the monostable circuit of IC_4, and you can add more sections in the same manner. Diodes D_1, D_2, and D_3 couple and isolate the comparators' outputs to Pin 2 of IC_4. Each keypad section connects the same selection of timing-resistor values to the monostable. Therefore, each keypad section's output pulse widths occupy the same range: 110 to 1320 µsec.

For the microcontroller to identify an active keypad section, the circuit generates a single, double, or triple pulse, depending on whether the pressed key

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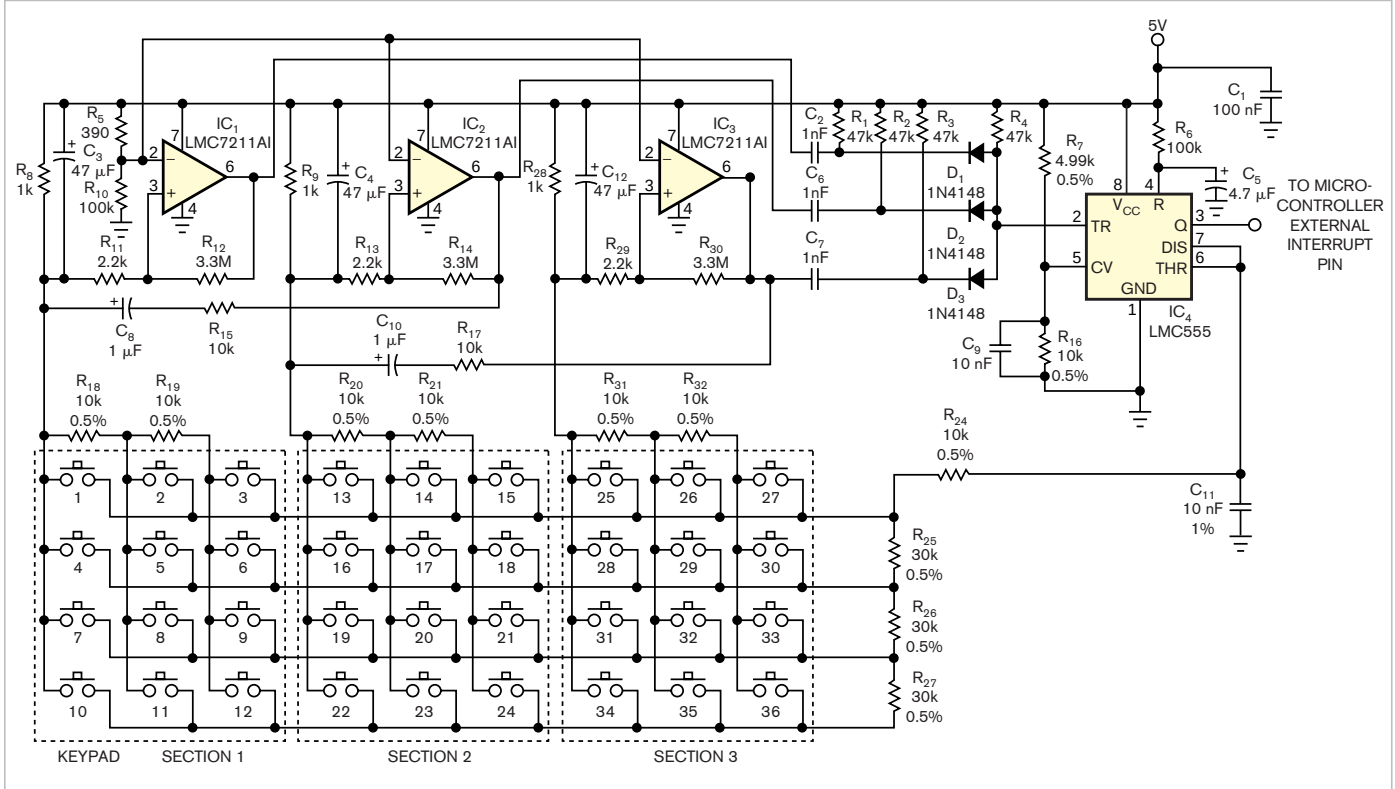

Figure 1 A keyboard encoder uses multiple variable-width pulses to communicate keys' addresses to a microcontroller using a single-wire interface.

resides in section 1, 2, or 3, respectively. The microcontroller identifies the pressed key by measuring the width of the first pulse and identifies the keypad section by counting the number of pulses. Implementing the multiple-pulse-encoding scheme requires no additional active components. Pressing a key in Section 1 generates a single pulse. Pressing a key in Section 2 causes comparator IC_2's output to go low and triggers IC_4 to generate the first pulse. At the same time, R_{15} and C_8 apply IC_2's output transition to comparator IC_1's input. As IC_2's output, Pin 6, goes low, C_3 starts to charge, and, after a delay of about 2 msec, IC_1 triggers IC_4 to generate the required second pulse. Because the time-constant product of $R_{15} \times C_8$ is much longer than 2 msec, C_8 does not charge significantly during the 2-msec interval. However, C_8 does charge to a full 5V during the interval in which the key is pressed, which allows comparator IC_1 to recover to its steady state.

In a three-section keypad, pressing a key in the third section activates comparator IC_3 which in turn triggers IC_4 to produce the first pulse. After feedback through R_{17} and C_{10} produces a 2-msec delay, IC_2 triggers IC_4 to produce a second pulse. After yet another 2-msec delay, IC_1 triggers IC_4 to produce the third and final pulse. Although somewhat arbitrary, a 2-msec delay provides sufficient margin over the maximum key-pressed pulse width of 1.32 msec. The interrupt routine provides additional timing margin by allowing as much as 3 msec between pulses.

Listing 1, available in the online version of this Design Idea at www.edn.com/050929di1, represents a modified version of the interrupt routine in **Reference 1** and supports the circuit in **Figure 1** for any number of keypad sections. For a three-section-keyboard implementation, the routine returns a key number from 1 to 36. EDN

REFERENCE

1 Schleicher, Israel, "Single-wire keypad interface frees microcontroller-I/O pins," *EDN*, March 31, 2005, pg 75, www.edn.com/article/CA512131.

Added components improve switching-regulator stability

Wayne Rewinkel, National Semiconductor, Schaumburg, IL

This Design Idea shows how adding one or two passive parts can reduce a hysteretic constant-on-time switched-mode voltage regulator's output voltage ripple and reduce its susceptibility to variations in external load capacitance and ESR (equivalent series resistance). The regulator operates much like a pure hysteretic switcher. The device's internal one-shot sets its pass transistor's on-time, making it less prone to frequency runaway but still susceptible to noise injected at the regulator's FB (feedback) pin. To switch cleanly with predictable frequency and duty cycle, the switcher requires application of approximately 50 to 100 mV of ripple voltage to the feedback pin. This Design Idea shows how four circuit implementations using National's LM5007 and LM5008 regulators satisfy the important feedback-ripple requirements by adjusting on-resistance and maintaining a nearly constant switching frequency as input voltage varies.

Figure 1 shows a basic buck regulator whose output capacitor, C_5, presents a high internal ESR, R_5. Note that the designer cannot access R_5 and V_{OUT2}. Inductor L_1's ripple current flows through R_5 and C_5 and produces a certain amount of ripple voltage at V_{OUT1}. Although common, this simple design presents two problems: First, feedback resistors R_4 and R_3 form a voltage divider that reduces the output ripple presented to IC_5's FB pin. Thus, 50 mV of ripple at the pin may correspond to excessive ripple voltage at V_{OUT1}. Adding a compensation capacitor, C_4, forces the output-ripple voltage to appear at the feedback pin. Second, a typical pc board may include many low-ESR ceramic bypass capacitors that attenuate ripple voltage to a level that destabilizes the circuit.

Suppose that you replace C_5 in **Figure 1** with a low-ESR capacitor and add R_5 as a discrete resistor. You can connect the external load to V_{OUT2} to reduce output-ripple voltage at the load

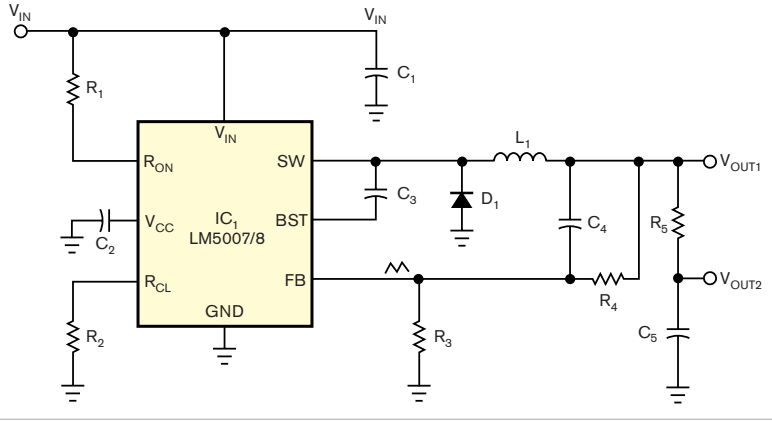

Figure 1 This basic switched-mode voltage regulator reduces its input voltage to a lower value.

and increase the circuit's immunity to added load capacitance. The regulator's feedback voltage derives from V_{OUT1}, and C_4 reduces output-ripple losses in the feedback divider, R_4 and R_3. Unfortunately, this frequently used design introduces new problems: As output current increases, V_{OUT2} falls below V_{OUT1} and degrades load-voltage regulation. Second, R_5 carries full load current and dissipates power, reducing overall efficiency. Using a large, high-wattage fractional-ohm resistor at R_5 increases product cost and regulator-package dimensions.

Figure 2 shows a rearranged buck-mode-switching regulator with two additional components. Assume that C_5's ESR is negligible and that R_6 is open. Now, R_5 remains inside the feedback loop, and C_4 couples voltage ripple from the inductor side of R_5 to feedback. This action stabilizes the regulator's operation and requires almost no output-ripple voltage, and R_5 introduces only a small reduction in efficiency. Taking dc feedback at the load preserves the circuit's excellent load regulation.

In another scenario, suppose that you replace R_5 with a short circuit and select values for R_6 and C_4 that provide the desired amount of ripple voltage at the feedback pin. This configuration produces almost no output-voltage ripple and eliminates R_5's power losses. Load regulation suffers because, as load current increases, inductor L_1's ESR introduces voltage droop at V_{OUT1} and forces the voltage at switching node SW slightly higher. However, designers can select L_1 for a low ESR that minimizes its effects on load regulation and can make R_6's resistance larger than that of R_4.

The following examples compare output ripple, circuit losses, and component count for the design scenarios. Assume that input voltage is 50V, output voltage is 5V, output current is 400 mA, switching frequency is 480 kHz, and desired minimum feedback ripple is 50 mV p-p. Select L_1 to operate at a ripple current of 200 mA. Solving for L_1, you obtain:

$$L_1 = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}} = \frac{(50-5) \times t_{ON}}{0.2}.$$

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} = \frac{5}{50 \times 480\ k\Omega} = 0.21\ \mu SEC.$$

Substituting on-time into the above **equation** yields

$$L_1 = \frac{45 \times 0.21}{0.2} = 47\ \mu H.$$

Select a Coilcraft DO1813P-473HC with ESR of 0.47Ω based on its small pc-board footprint. For C_5, choose a ceramic capacitor that's large enough to limit the ripple voltage on V_{OUT} to less than 10 mV p-p. Given the maximum ripple voltage and a known triangle-wave current drive, calculate a value for C_5:

$$C_5 = \frac{I_{RIPPLE}}{(8 \times V_{RIPPLE} \times f_S)} = \frac{0.2}{(8 \times 0.010 \times 480\ kHz)} = 5.2\ \mu F.$$

For C_5, you can use TDK's 10-µF C3216X7R0J106 ceramic capacitor that presents an ESR of 3 mΩ or less. Because the internal reference voltage for the LM5007 or LM5008 is 2.5V, set feedback resistors R_3 and R_4 to 1 kΩ to divide the regulator's 5V output to 2.5V. Next, select values for R_5, C_4, and R_6 to compare results for each design. In the first scenario, to provide 100 mV of ripple at V_{OUT1} and 50-mV ripple at the feedback pin in the circuit of **Figure 1**, the design requires a value of 0.25Ω for R_5. Adding C_4 changes the value of R_5 to 0.125Ω to provide 50-mV ripple at V_{OUT1} and the feedback pin. You calculate a value for C_4 that passes the ripple current:

$$C_4 = \frac{10}{(2\pi(R_4 \| R_3) \times f_S} = \frac{10}{(2 \times 3.14159 \times 500 \times 480\ k\Omega)} = 6.6\ nF,$$

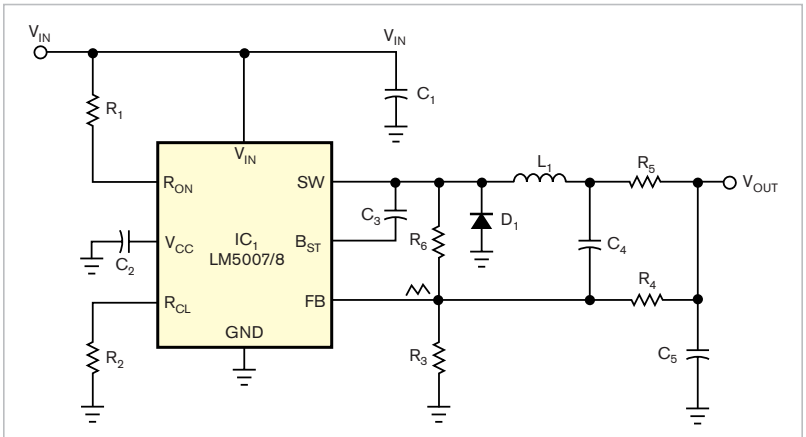

Figure 2 Adding two components, R_6 and C_4, helps reduce output-ripple voltage and improve output-voltage regulation.

TABLE 1 CIRCUIT OPTIONS

Scenario	Figure	R_5 (Ω)	R_6 (Ω)	C_4 (nF)	V_{OUT}, R_6 (mV)	Voltage droop (mV)	Power dissipation (mW)	Issues
1	1	0.25	0	0	100	0	0	Load capacitance and stability
1	1	0.125	0	6.6	50	0	0	Load capacitance and stability
2	1	0.25	0	0	6	100	40	Voltage droop and power dissipation
2	1	0.125	0	6.6	6	50	20	Power dissipation
3	2	0.125	0	6.6	6	0	20	Power dissipation
4	2	0	30k	6.6	6	7	0	Voltage droop

where $R_4 || R_3$ represents the value of the parallel combination of R_4 and R_3.

In the second scenario, V_{OUT2} droops to 100 mV at full load but exhibits only 6 mV of ripple without C_4 in the circuit. Losses in R_5 amount to 40 mW. Adding C_4 delivers 50 mV of ripple to the feedback pin and V_{OUT1}; setting R_5 to 0.125Ω reduces R_5's power loss to 20 mW. In the third scenario, R_6 is an open circuit, and the design in **Figure 2** requires an R_5 value of 0.125Ω to provide 50-mV ripple at FB. V_{OUT1} exhibits no voltage droop at full load current and has only 6 mV of ripple voltage. R_5's power loss is 20 mW.

In the fourth case, a short circuit replaces R_5, and the design in **Figure 2** requires a value for R_6 that increases the voltage across C_4 to provide 50 mV of ripple voltage at FB. Use the following **equations** to calculate the value:

$$R_6 = \frac{(V_{IN} - 2.5)}{C_4 \times 50\ mV \times V_{IN} \times ((f_S / V_{OUT}))} = 30\ k\Omega.$$

$$R_{RIPPLE} = (V_{IN} - 2.5)/(C_{RIPPLE} \times 50\ mV \times V_{IN} \times f_S / V_{OUT}) = 30\ k\Omega.$$

With R_6 in the circuit, V_{OUT} drops slightly because R_6 and R_4 effectively connect in parallel. To compensate, you can slightly increase R_4 so that the new value of R_4 in parallel with R_6 equals R_4's original value. Thus,

$$R_{4(NEW)} = \frac{R_{4(OLD)} \times R_6}{R_6 - R_{4(OLD)}} = \frac{1000 \times 30}{29} = 1.034\ k\Omega.$$

In this instance, you may decide not to use the new value of R_4 because adding R_6 raises V_{OUT} by only 85 mV. Adding R_6 produces 6 mV of ripple at V_{OUT} and little or no loss in R_5, but load regulation will not be perfect.

Inductor L_1's ESR of 0.47Ω introduces a voltage drop of about 200 mV at full load, which increases the voltage at the junction of L_1 and R_6 and also reduces V_{OUT} to maintain 2.5V at FB. You can calculate the magnitude of the change by multiplying L_1's voltage drop of 200 mV by the ratio of R_4 to R_6:

$$V_{OUT(DROOP)} = \frac{200\ mV \times R_4}{R_6} = \frac{0.2 \times 1}{30} = 0.0067V.$$

Note that output-voltage droop and power dissipation become more significant in designs that deliver higher output current or lower output voltage (**Table 1**).EDN

Electromechanical damping stabilizes analog-meter readings

Alexander Bell, Infosoft International Inc, Rego Park, NY

Before shipping moving-coil meters, manufacturers may short-circuit the meters' terminals with a length of wire, which provides effective electromagnetic damping and results in better immunity to external mechanical vibration and shocks that can occur during transportation. This Design Idea applies essentially the same principle to analog meters under normal operating conditions. Connecting a meter to a voltage source with low internal resistance applies electromagnetic damping and makes the meter's readings more stable. Increased immunity to external vibration and shock takes on importance in mobile- or portable-system applications and especially in automotive devices.

For example, suppose that your application requires measurement of a 0 to 10V power supply (**Figure 1**). You have available a typical electromechanical meter that presents a full-scale voltage rating, V_{FS}, of 50 mV and a full-scale current rating of 1 mA. To obtain the 10V full-scale voltage range, you add a series resistance, R_S. First, calculate the meter's internal resistance, R_{COIL}:

$$R_{COIL} = \frac{V_{FS}}{I_{FS}} = \frac{50\ mV}{1\ mA} = 50\Omega.$$

Next, calculate the multiplier resistor, R_S, as follows:

$$R_S = \frac{(V_{IN} - V_{FS})}{I_{FS}} = \frac{(10V - 0.05V)}{1\ mA} = 9950\Omega.$$

The resistance of R_S typically great-

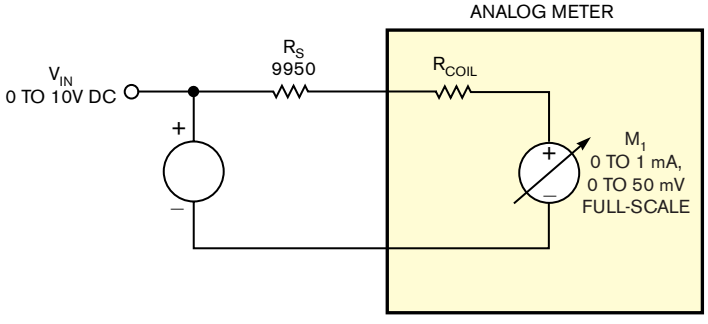

Figure 1 A typical analog moving-coil voltmeter employs a high-value series resistor, R_S, to establish the full-scale range but doesn't contribute to electromagnetic damping of the meter movement.

ly exceeds that of R_{COIL} and therefore significantly reduces the electromagnetic damping action on the meter movement. Although you can improve damping by shunting the meter with a capacitor, this approach also increases the meter's settling time.

Figure 2 illustrates a better approach, in which a moving-coil meter connects to the output of an operational amplifier, IC_1, embedded in a deep negative-voltage-feedback loop. Because the op amp presents an extremely low equivalent output resistance, the meter's terminals are "virtually shorted," providing effective electromechanical damping that results in more stable readings and increased shock and vibration resistance. In **Figure 2**, the resistive voltage divider comprising R_1 and R_2 connected to the op amp's noninverting input determines the meter's full-scale reading. You can add R_F and C_F to form an optional highpass filter to further improve the meter's settling time. Transistors Q_1 and Q_2 are also optional and added as overvoltage protection. Note that, for normal operation, the transistors' forward base-emitter voltage, V_{BE}, should be several times larger than the meter's full-scale voltage, V_{FS}, which is typically 50 to 100 mV.

A rail-to-rail-capable, single-supply micropower op amp makes a good choice for this application. If the input voltage, V_{IN}, exceeds the op amp's minimum power-supply-voltage requirement, you can connect the op amp's V_{CC} pin directly to the input terminal, as the dashed line in **Figure 2** shows. In effect, the circuit combines the advantages of meter buffering and improved shock and vibration resistance with a traditional moving-coil meter's advantage of requiring no external power supply. You can choose from among many commercially available off-the-shelf, rail-to-rail output-micropower op amps that draw supply currents well below the full-scale current drain, I_{FS}, of typical moving-coil meters. For example, Maxim's MAX4289 requires as little as 1V and 9 µA of power, and the MAX4470 requires a minimum of 1.8V but only 750 nA of supply current.

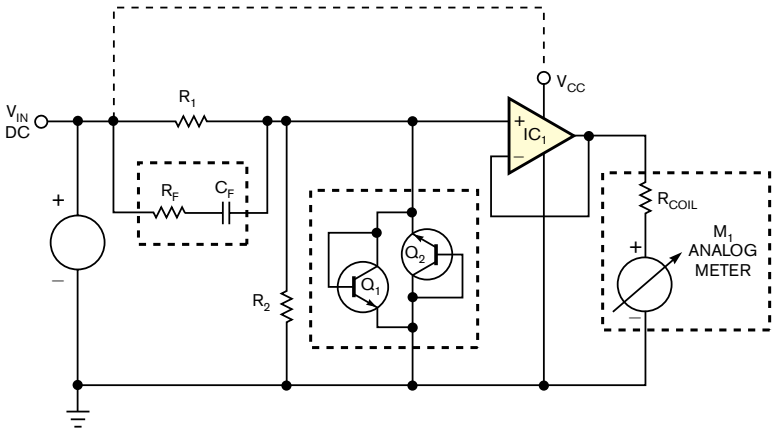

Figure 2 An operational amplifier's low output resistance provides electromechanical damping for a moving-coil meter for stable readings and enhanced resistance to mechanical shock and vibration. Connect V_{CC} to either an external power supply or the circuit's input terminal if V_{IN} exceeds IC_1's minimum power-supply-voltage rating.

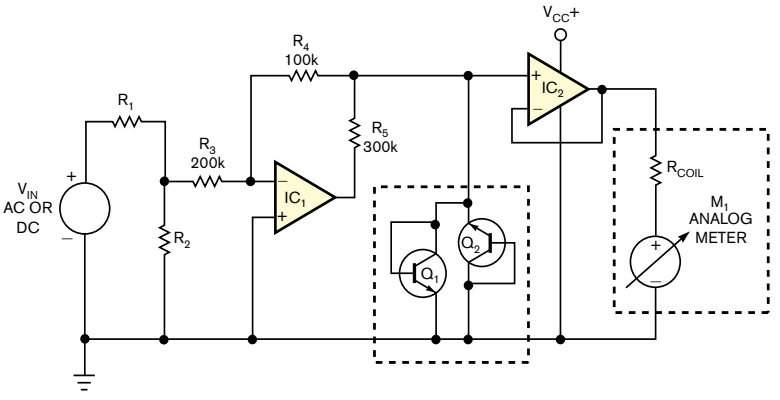

Figure 3 Based on rail-to-rail operational amplifier IC_1, this circuit's input stage forms a diodeless, precision full-wave rectifier and enables the circuit of Figure 2 to display ac- or dc-voltage measurements on a dc meter.

Although this Design Idea has so far related only to dc-voltage measurements, you can expand the circuit to include ac- and dc-voltage measurements (**Figure 3**). In this approach, you add a precision diodeless, full-wave-rectifier stage based on a single rail-to-rail operational amplifier and resistors R_3, R_4, and R_5 (**Reference 1**). Resistors R_1 and R_2 determine the full-scale reading. This circuit requires an external dc power supply to drive op amps IC_1 and IC_2; voltage-limiting transistors Q_1 and Q_2 are optional. EDN

REFERENCE

1 Bell, Alexander, "Simple Full-Wave Rectifier," *Electronic Design*, April 4, 1994, pg 78.

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Dither a power converter's operating frequency to reduce peak emissions

Bob Bell and Grant Smith, National Semiconductor, Phoenix, AZ

Designers of dc/dc switching power converters face the challenge of controlling EMI (electromagnetic-interference) emissions produced during normal operation. If large enough, these emissions conduct through power lines or radiate to other assemblies within a system and can compromise a system's performance. Emission peaks typically occur at the converter's fundamental switching frequency and gradually reduce in amplitude at each higher order harmonic, with most of the emitted energy confining itself to the fundamental and lower order harmonics. Modulating, or dithering, the power converter's operating frequency can reduce the peak emissions by spreading EMI over a band of frequencies.

Most modern PWM controllers use an external resistor to set the operating frequency, which typically increases with decreasing resistor values. For example, the LM5020's internal oscillator delivers a regulated 2V at its programming pin (RT), and a programming resistor connected to RT sets the current that RT delivers. The oscillator also delivers a proportional current into an internal timing capacitor (**Reference 1**). The period of the timing capacitor's ramping voltage determines the oscillator's frequency.

The external dithering circuit in **Figure 1** comprises a simple stand-alone comparator-based oscillator configured to operate at approximately 800 Hz. The output state of comparator IC_2 goes high upon power-up. R_1, R_2, and R_3 set the comparator's positive input, which initially rests at 2.9V. The voltage at capacitor C_3 ramps up toward the positive threshold.

When the voltage at the comparator's negative input reaches the positive-threshold voltage, the comparator's output switches low, which also lowers the threshold at the comparator's positive input to 2.1V. The voltage at capacitor C_3 then ramps down toward the new threshold, and, when it reaches the lower threshold voltage, the cycle repeats. The voltage across C_3 approximates a triangular wave with a minimum voltage of 2.1V and a maximum of 2.9V.

To dither the LM5020 controller's PWM-oscillator base frequency, the triangular wave generated by IC_2 modulates the current from the controller's RT pin. Resistor R_5 sets the percentage of modulation dither. The right side of R_5 is fixed at the RT pin's regulated potential of 2V, and the low-frequency triangle wave coupled from IC_2 through capacitor C_2 drives R_5's left side. For R_5 with a value of 64.9 kΩ, the peak-to-peak current through resistor R_5 is approximately 12 µA. With the dither circuit disconnected, the steady-state current that RT sources is approximately 121 µA, and the 12-µA p-p dither current thus represents 10% total modulation.

An LM5020-controlled PWM flyback dc/dc converter, IC_1, evaluates the dither circuit's effectiveness. The circuit's fundamental operating frequency is 250 kHz, which the controller's R_T

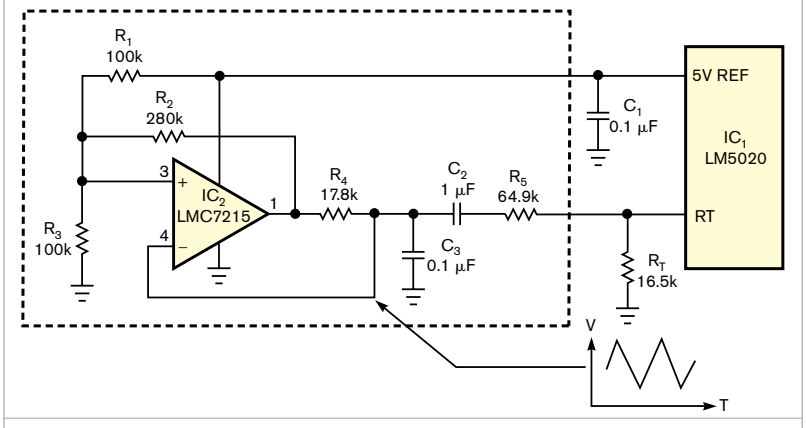

Figure 1 A low-frequency triangular-wave oscillator modulates a PWM controller's oscillator frequency.

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resistor sets. The red trace of **Figure 2** shows the conducted emissions on the circuit's positive input-power line without the dither circuit in operation. The peak emissions are narrowly confined around the fundamental oscillator frequency of 250 kHz with a measured amplitude at the fundamental frequency of −24 dB.

Connecting the dither circuit to the controller's RT input produces the blue trace of **Figure 2**. Conducted emissions around the fundamental frequency now disperse around the fundamental frequency with maximum amplitude reduced by −34 to +10 dB. EDN

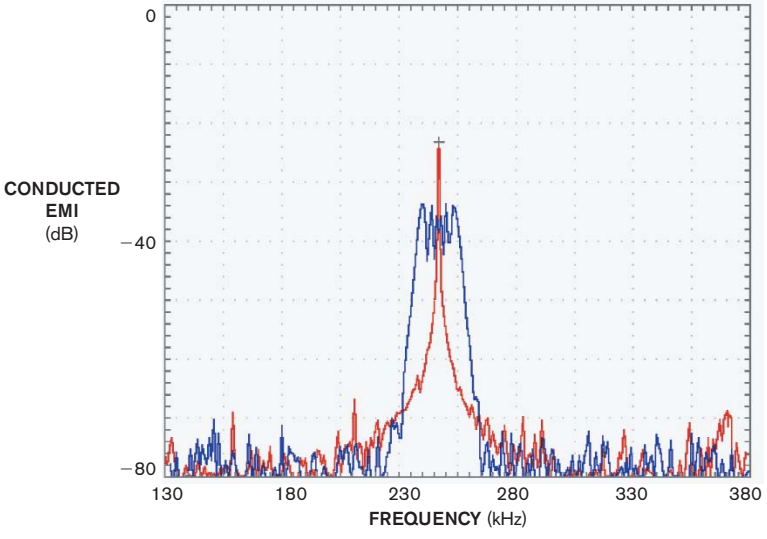

Figure 2 Measured at the dc/dc converter's input, peak conducted emissions without dither (red trace) decrease by 10 dB with dithering applied (blue trace).

REFERENCE

1 LM5020 data sheet, National Semiconductor, www.national.com/pf/LM/LM5020.html#Datasheet.

Single-port pin drives dual LED

Tom Gay, Dornstadt, Germany

Most current microcontrollers offer I/O ports that can change their functions during program execution. As outputs, the circuits can sink and source reasonably large amounts of current. This Design Idea shows three alternative methods for driving a two-pin, two-color LED from a single I/O pin. **Figure 1** illustrates one possible approach that uses external inverter IC_1 to drive D_1, a red/green bidirectional LED. A logic-high output on the port pin forces current through the green (upper) LED and pulls the inverter's input high, which drives the inverter's output low and sinks current from the green LED. A logic-low output on the port pin raises the inverter's output high, delivering current to the red (lower) LED; the microcontroller's output sinks current from the red LED.

To turn off both LEDs, you reconfigure the microcontroller's port pin from output to input or switch the pin to tri-state mode, either of which prevents the microcontroller's port pin from sourcing or sinking current. This circuit's primary disadvantage is that it yields no control over each LED's brightness; instead, resistor R_5 determines forward current for both LEDs.

Figure 2 presents an approach that also involves a major disadvantage. Zener diodes D_3 and D_4 and resistors R_3 and R_4 form a low-impedance voltage divider that applies $V_{CC}/2V$ to one end of LED D_5. The value of V_{CC} drives the selection of the zener diodes' voltage, V_Z, with lower voltage zener diodes allowing more LED current and higher voltage ones limiting maximum LED current. Given that the microcontroller's outputs can deliver rail-to-rail voltages, the difference between V_{CC} and V_Z limits maximum forward current for both LEDs. For example, if V_{CC} is 5V and V_Z is 3V, the forward voltage across either LED is less than 2V. Once a designer selects the zener-diode voltage, only small variations in V_{CC} can occur; otherwise, the LEDs' brightness would fluctuate.

Using discrete components, another circuit offers an inexpensive approach that avoids the other circuits' disadvantages (**Figure 3**). When the microcontroller's output port goes high, current flows through the green (upper) LED, R_2, D_2, and FET Q_2, which the port's high level turns on. When the microcontroller's output port goes low, transistor Q_1 turns on and delivers current to the port pin through R_2 and the red (lower) LED. The circuit operates symmetrically because silicon diode D_2's forward-voltage drop is present

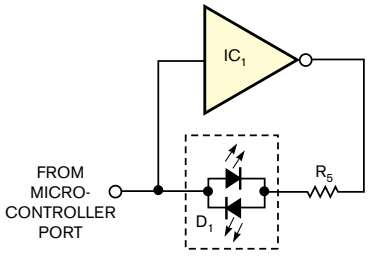

Figure 1 An inverter can drive a bidirectional, two-color LED but applies the same amount of current to both LEDs.

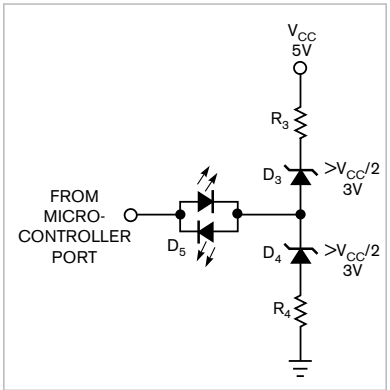

Figure 2 A zener-diode and resistor-voltage divider exhibits sensitivity to supply-voltage variations and allows LED brightness to vary.

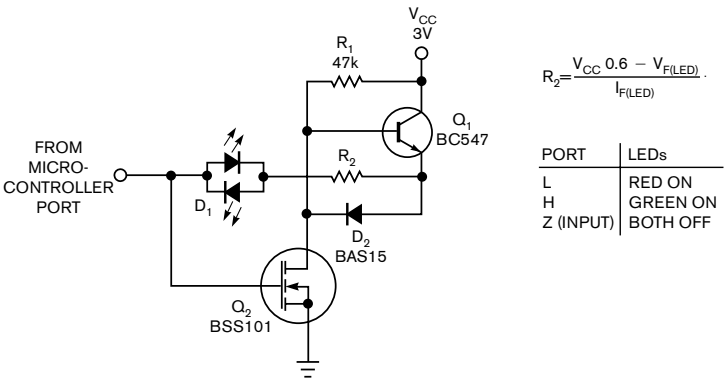

Figure 3 This circuit provides immunity to supply-voltage fluctuations and more uniform LED brightness.

regardless of whether the microcontroller's port pin goes high or low. V_{CC} may vary during operation but must remain higher than 3V.

You can individually adjust the LEDs' currents to equalize brightness or compensate for a difference between the microcontroller's power-supply voltage and the LED-driver circuit's V_{CC}. Replace R_2 with two resistors connected in series between Q_1's emitter and D_2's anode. Connect the midpoint of the two resistors to the LEDs.

With the microcontroller's port pin configured as an "input with pullup," the port delivers a small current to the green LED. However, pullup-resistor values of 22 kΩ or higher do not cause misleading light output from LEDs in the off-state. When the input signal from the port pin floats—that is, with V_{CC} at 5V and the port configured as an input with no pullup resistor—the circuit draws no additional current, and the quiescent current, which R_1 determines, averages less than 100 µA. EDN

Network linearizes dc/dc converter's current-limit characteristics

John Guy and Lance Yang, Maxim Integrated Products Inc, Sunnyvale, CA

Recently announced versions of integrated step-down dc/dc converters have eliminated the requirement for a high-side current-sense resistor by sampling the voltage drop across an external, low-side, MOSFET synchronous rectifier. This topology eliminates the sense resistor's cost and pc-board-space requirement and also provides a modest increase in circuit efficiency. However, the MOSFET's highly temperature-dependent on-resistance dominates the current-limit value. Fortunately, certain newer dc/dc converters, such as Maxim's MAX1714, allow external adjustment of the current-limit threshold. The circuit in **Figure 1** shows how a thermistor applies temperature compensation to the circuit's output-current limit.

The MAX1714's linear current-limit (I_{LIM}) input range at Pin 6 of IC_1 spans 0.5 to 2V, which corresponds to current-limit thresholds of 50 to 200 mV, respectively. For the default current-limit setting, 100 mV, the circuit imposes a 7.5A current limit at 25°C. However, **Figure 2** shows that the current limit varies from 9A at −40°C to 6A at 85°C. To design the temperature-compensation network, begin by breadboarding the circuit and using an external power supply to vary the MAX1714's current-limit input voltage such that the output-current-limit value remains constant. You repeat the

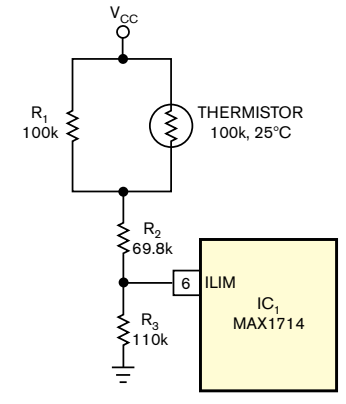

Figure 1 A thermistor-resistor network provides temperature compensation for a dc/dc converter's current-limit input, I_{LIM}.

measurements at 10°C intervals over the circuit's operating-temperature range.

To compensate for IC_1's temperature variation, you can select from among several possible resistor-thermistor-network topologies. First, you need to select a suitable thermistor and characterize its resistance-versus-temperature variation. Because the MAX1714's current-limit input pin feeds a relatively high input-impedance voltage-follower stage, this thermistor requires a high nominal resistance of 100 kΩ. Resistance-versus-temperature characteristics of inexpensive thermistors exhibit considerable nonlinearity, but one relatively simple approach to linearization involves paralleling the thermistor with a fixed resistor equal to the thermistor's nominal resistance (**Reference 1**). In the network of **Figure 1**, R_1 linearizes the thermistor, and R_2 and R_3, respectively, set the slope and intercept of the current-limit-voltage-versus-temperature-characteristic curve.

To arrive at optimal values for R_2 and R_3, we prepared a spreadsheet incorporating the original current-limit-voltage-versus-temperature data and added columns for each of the network's resistors, plus the thermistor specification sheet's resistance-versus-temperature data. While observing the circuit's temperature-versus-voltage transfer function, we varied the spreadsheet's values for R_2 and R_3 until the transfer function best approximated the measured current-limit-voltage-versus-temperature data. Finally, we constructed the circuit and tested it over the temperature range and noted that it yielded a reasonably flat response.

The curvature of the corrected output characteristic of **Figure 2** (red trace) is intrinsic to the thermistor. Though not perfectly flat, the corrected curve represents a great improvement over the original (black trace) and is sufficient to meet the original design goal. You can achieve more precise compensation by selecting a different thermistor or by incorporating multiple thermistors. EDN

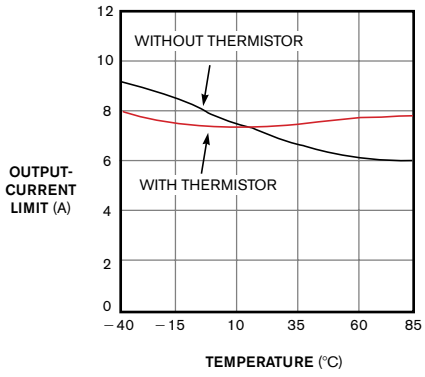

Figure 2 Before (black trace) and after (red trace) current-limit-versus-temperature characteristics show the performance enhancement that the circuit in Figure 1 provides.

REFERENCE

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Add a Schmitt-trigger function to CPLDs, FPGAs, and applications

Stephan Roche, Santa Rosa, CA

Thanks to its internal hysteresis, the highly useful Schmitt-trigger circuit accepts a low-slew-rate input signal and produces a clean, glitch-free output transition. Unfortunately, user-programmable logic devices, such as CPLDs and FPGAs, generally offer no direct method of synthesizing Schmitt-trigger gates and buffers. This Design Idea shows how a few external components and some VHDL code can implement a Schmitt trigger and put it to work in several useful applications.

To create an equivalent of the basic Schmitt-trigger buffer, you use two external resistors to create positive feedback around a buffer (**Figure 1a** and **b**). You can also use four external resistors to set two threshold levels around an R-S flip-flop (**Figure 1c**). The following equations, respectively, describe the basic Schmitt trigger's positive- and negative-threshold levels:

$$V_+ = \frac{R_1}{R_2} V_{CC} + V_{TH}\left(1 - \frac{R_1}{R_2}\right);$$

$$V_- = V_{TH}\left(1 - \frac{R_1}{R_2}\right).$$

In these **equations**, V_{TH} represents the input-voltage threshold of the CPLD/FPGA device, and V_{CC} is its power-supply voltage.

Based on the equivalent Schmitt-trigger circuit in **Figure 1b**, the low-cost resistance-capacitance oscillator in **Figure 2** requires four external passive components. Resistor R and capacitor C set the circuit's oscillation frequency. Note that the resistance values of R_1

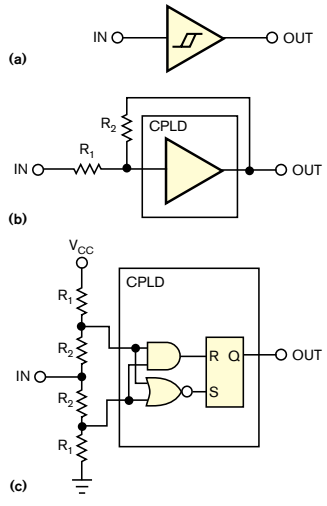

Figure 1 Use a portion of a programmable-logic device or gate array to implement a Schmitt-trigger buffer (a) by adding either two (b) or four external resistors (c).

and R_2 must be larger than that of R. **Listings 1** and **2** contain the circuit's VHDL implementation and RTL architecture, respectively.

In **Figure 3**, an open-collector buffer provides the trigger for the basic Schmitt-trigger-retriggerable monostable circuit by discharging timing capacitor C. The circuit's output pulse width approximately equals the time constant RC. **Listing 3** shows the VHDL implementation and RTL architecture, respectively.

You can convert the retriggerable monostable into the nonretriggerable monostable in **Figure 4** by using an open-collector NAND gate to discharge timing capacitor C. As long as the circuit's output remains high during the timing interval, the system locks out external triggers. As in the previous circuit, the output pulse width approximately equals the time constant RC. **Listing 4** contains the VHDL and RTL codes.

You can use the basic CPLD buffer-with-feedback circuit to provide hysteresis for a contact-debouncing circuit. In **Figure 5**, resistor R_4 provides contact-cleaning current, and R_3 and C form a low-pass filter to reduce noise that contact bounce generates. Component values vary depending on the application. EDN

```
Entity Oscillator is
   Port (
         A : in std_logic;
         B : in std_logic;
         OUT : out std_logic
   );
end Oscillator;



architecture RTL of Oscillator is
begin
   A <= B;
   OUT <= not A;
end RTL;



Entity Monostable is
   Port (
         A : in std_logic;
         B : in std_logic;
         Trigger : in std_logic;
         C : out std_logic;
         OUT : out std_logic
   );
end Monostable;
architecture RTL of Monostable is
begin
   A <= B;
   OUT <= not A;
   C <= '0' when Trigger= '1' else 'Z';
end RTL;



   Port (
         A : in std_logic;
         B : in std_logic;
         Trigger : in std_logic;
         C : out std_logic;

           OUT : out std_logic
    );
  end Monostable;
  architecture RTL of Monostable is
  begin
     A <= B;
     OUT <= not A;
     C <= '0' when Trigger= '1' and A='0' else 'Z';
  end RTL;
```

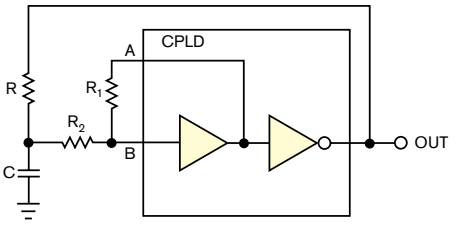

Figure 2 Add a resistor and capacitor to a basic Schmitt-trigger buffer to form a low-cost oscillator.

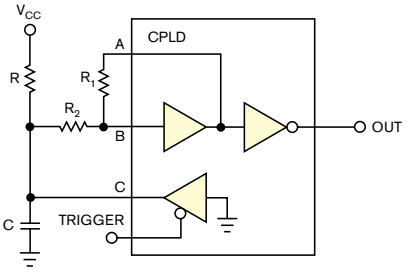

Figure 3 An active-low buffer holds timing capacitor C discharged in this version of a retriggerable monostable multivibrator based on the Schmitt-trigger buffer.

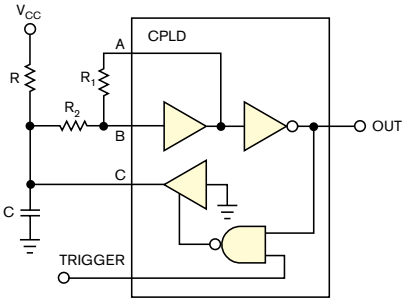

Figure 4 A NAND gate locks out trigger pulses, forming a nonretriggerable, monostable circuit.

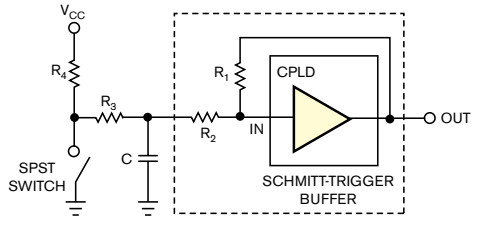

Figure 5 Use a Schmitt trigger to debounce switch contacts.

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READERS SOLVE DESIGN PROBLEMS

LC oscillator has stable amplitude

Julius Foit, Czech Technical University, Prague, Czech Republic

Many applications call for wide-range-tunable LC oscillators that can deliver a nearly constant-frequency, nearly harmonic-free output even when the circuit's output load changes. From a design viewpoint, eliminating either inductive or capacitive LC circuit taps and transformer couplings within the frequency-determining circuit simplifies fabrication and production, as does the option of grounding one side of the tuned LC circuit. These requirements suggest a circuit that can automatically and efficiently internally adjust loop gain, the basic criterion for oscillation. In addition, the circuit must provide sufficient gain to oscillate with low-impedance LC circuits and regulate the oscillation's amplitude to improve frequency stability and minimize THD (total harmonic distortion).

Designers have exploited many circuit topologies—some highly complex—in their attempts to achieve these design goals, but certain active devices' basic properties can help designers obtain acceptable behavior from a simple oscillator circuit. **Figure 1** shows a basic LC-oscillator arrangement. The amplifier operates as a noninverting voltage-controlled current source. The LC circuit converts the amplifier's output current, I_{OUT}, to voltage, V_{IN}, and applies it as input to the amplifier. **Equation 1** shows the formal condition for oscillation:

$$A_O = \frac{I_{OUT}R_D}{V_{IN}} \geq 1. \qquad (1)$$

In this **equation**, A_O is the overall voltage amplification and R_D is the LC circuit's dynamic resistance at its resonant frequency. In practical circuits, the value of R_D depends on the LC circuit's properties and thus can fall anywhere within a wide range. Also, **Equation 1** assumes an ideal amplifier—that is, one having characteristics that are independent of frequency.

Figure 1 and **Equation 1** yield a simple insight into the basic design problem: If the operation over a wide frequency range demands the use of several LC circuits with widely varying values of R_D, the amplifier's properties must be adjustable over a wide range. You can adjust the amplification to fulfill the gain-limitation condition for the worst-case LC circuit and then rely on device nonlinearities to reduce amplification under overdrive conditions. However, a heavily overdriven amplifier's input- and output-differential resistances can drop to a fraction of their optimum, high-resistance values. Second, large amounts of nonlinear distortion can impair frequency stability. Moreover, these effects depend

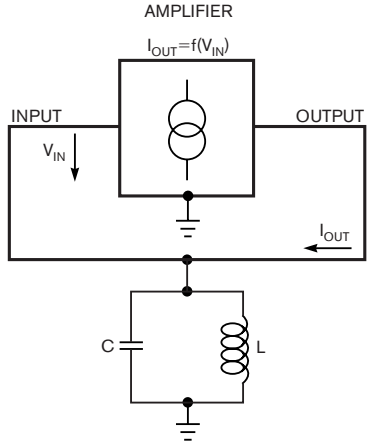

Figure 1 A parallel LC circuit and an amplifying voltage-to-current converter form a basic oscillator.

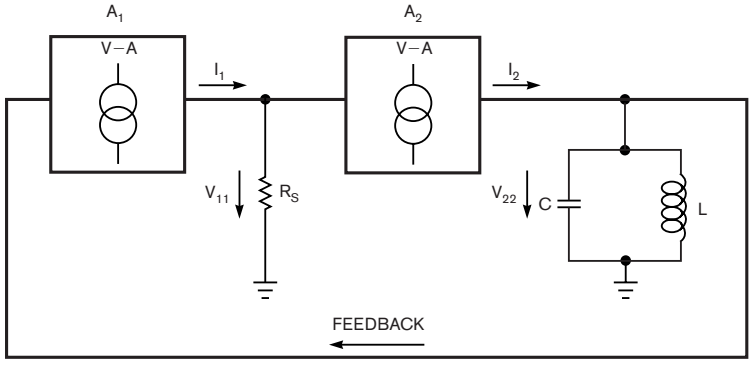

Figure 2 Adding a second voltage-to-current converter isolates the tuned circuit.

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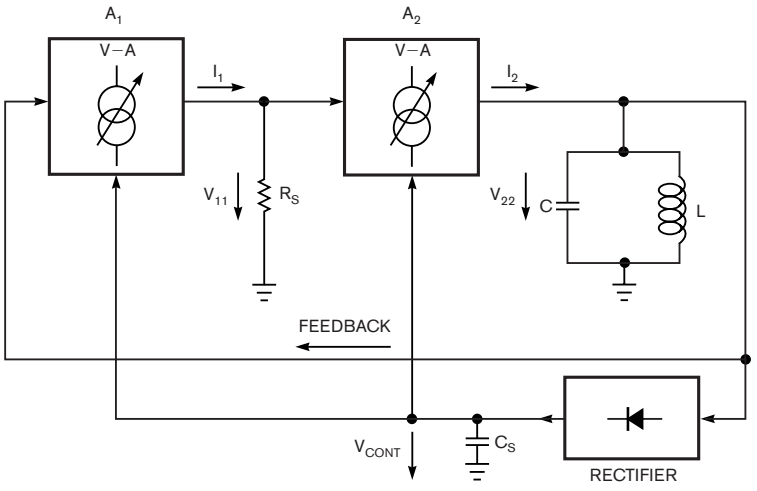

Figure 3 Rectifying a portion of the signal provides a gain-control voltage for the amplifiers.

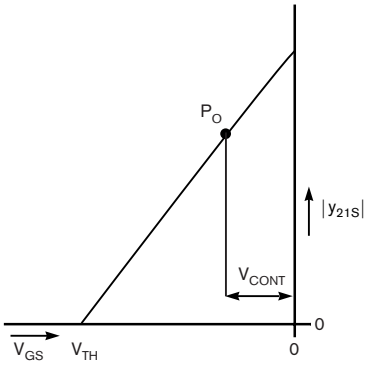

Figure 4 Control characteristics of an idealized JFET exhibit linear variation of forward transconductance versus gate-to-source voltage.

heavily on the amplifier's power-supply voltage, causing frequency stability to deteriorate if the supply voltage varies with load.

Various oscillator circuits use different designs within the amplifier block in **Figure 1**. The popular common-emitter or common-source transistor stage presents two important drawbacks: First, it's an inverting amplifier, and, second, its output does not behave as a good current source, especially when heavily overdriven. Attempts to avoid these problems include transformer coupling or providing impedance-matching taps on the LC circuit, both of which complicate the design and only partially solve the problems.

As **Figure 2** shows, another oscillator topology features two cascaded noninverting amplifiers, A_1 and A_2, as voltage-to-current converters (voltage-controlled current sources). In the circuit, coupling resistor R_S converts amplifier A_1's output current, I_{IN}, to voltage V_{IN}, and drives the second stage, A_2. The tuned circuit's dynamic resistance converts A_2's output current to output voltage, V_{22}, which feeds back to A_1's input to complete the positive-feedback loop. The overall loop amplification, A_{TOTAL}, appears in **Equation 2**:

$$A_{TOTAL} = A_1 \times A_2 = R_S R_D |y_{21S1}| \times |y_{21S2}|. \quad (2)$$

In this **equation**, $R_D = Q\omega L$ is the dynamic resistance of the LC circuit at resonance at the ω frequency, Q is the quality factor of the LC circuit, A_1 and A_2 are the equivalent voltage amplifications of both amplifier stages, and $|y_{21S1}|$ and $|y_{21S2}|$ are the real parts of differential-forward-transfer admittances of both amplifying stages. For self-sustained oscillations, the basic condition $A_{TOTAL} > 1$ in **Equation 1** must apply for all values of the LC circuit's dynamic resistance, R_D. In theory, this condition presents no problem; however, in practice, a situation arises in which the circuit must operate as an LC oscillator with a broad range of tuning inductances and capacitances; a wide range of tuned-circuit quality-factor Q, which the inductor primarily determines; a constant-amplitude output at any combination of conditions A and B; and the best possible frequency stability versus supply voltage and load.

Most LC oscillator circuits cannot simultaneously fulfill all of these requirements. Some oscillator circuits can sequentially fulfill some requirements, but none can fulfill all of them without complicating the circuit beyond reasonable limits. **Figure 3** shows a circuit deriving an external dc control signal from V_{22} to control the voltage-to-current-conversion coefficients—that is, amplification factors—of A_1 and A_2. Applying amplification control to both stages considerably increases the control's effectiveness. In addition to the original positive feedback for starting and sustaining oscillation, you can add an indirect negative-feedback path to the oscillator circuit to limit V_{22}'s amplitude. To meet the original design goals, amplifier blocks A_1 and A_2 should exhibit voltage-controlled input-versus-output characteristics, should possess linear-control amplification characteristics (**Figure 4**), should not invert the signal's phase, and should draw nearly no input current. Also, to emulate a current source, A_2 should present the highest possible differential internal output resistance.

The best active devices for both amplifier stages are the selected N-channel, medium-grade BF245Bs JFETs with a drain current of 5 mA at a gate-to-source voltage of 0V and a drain-to-source voltage of 15V. **Figure 5** shows the final circuit, in which Q_2 operates as a common-drain amplifier, A_2, and Q_1 operates as a common-gate amplifier, A_1.

The gate-source junction of Q_1 rectifies the ac voltage, V_{22}, across the tuned circuit. Coupling capacitor C_4

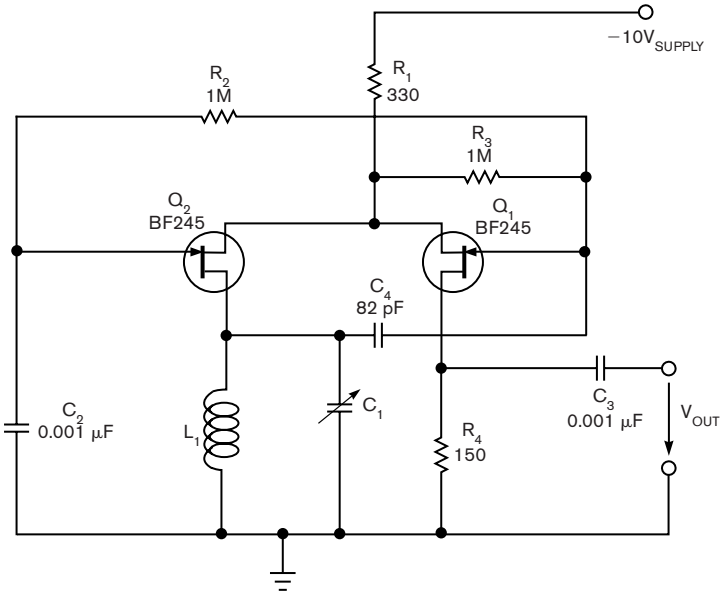

Figure 5 The completed oscillator circuit features a minimal component count.

in **Figure 5** doubles as dc-voltage-smoothing capacitor C_S in **Figure 3** because its bottom electrode connects to ground through the low dc resistance of tuning coil L. The dc-control voltage drives the gate of Q_2 through resistor R_2. Capacitor C_2 connects Q_2's gate to ground for ac signals, and Q_2 operates in common-gate connection because Q_1's source drives Q_2's source. To minimize frequency variations due to changing loads, a relatively low-value resistor, R_4, in series with Q_1's drain, isolates the output from the circuit's frequency-determining components. In addition, one lead each of L and C connects to ground.

The waveforms in **Figure 6a** and **6b** show no substantial change in the voltage across the tuned circuit even for widely different values of L and C. The voltage across the tuned circuit remains constant within 3% over a supply-voltage range of 8 to 30V. The same or better amplitude stability holds for the output voltage (**Figure 6c**), even at frequencies as low as 5 kHz and as high as 50 MHz with no adjustment of any passive-component values, except for L and C. Reducing the value of R_4 yields a smaller output voltage, further diminishing the effects of load variations on the operating frequency.

The dc level of the top, flat part of V_{OUT} rests at ground potential, and the waveform goes negative due to the negative power-supply voltage. Because of automatic-gain-control action, the waveshape remains remarkably consistent, regardless of frequency, exhibiting slightly rounded corners, mostly due to stray capacitances, at frequencies higher than 25 MHz. Only the LC circuit's ungrounded end provides a perfect sine wave. Other voltage and current waveforms exhibit cutoff distortion because both transistors operate roughly in Class B mode, shifting toward Class C at increasing power-supply voltages. You can extract a sine wave directly from the LC circuit, but variations in load impedance will influence the operating frequency.

On the other hand, the negative dc feedback controlling the gain of both transistors prevents even relatively large-load-impedance variations across the tuned circuit from greatly affecting the generated amplitude until the LC circuit's Q factor drops very low. At the expense of added complexity and a larger component count, you can include a buffer stage and extract a true sine wave from the LC circuit, but, in the circuit's original application as a radar-marker generator, the constant output amplitude ranked as of greater importance than the waveshape. EDN

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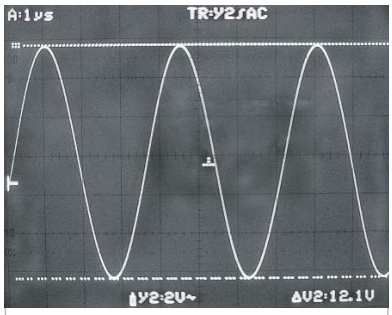
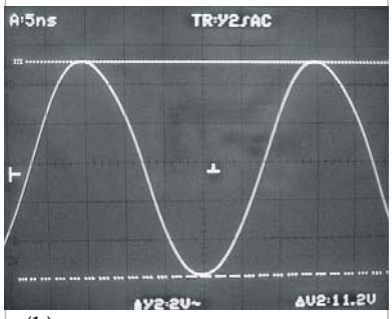
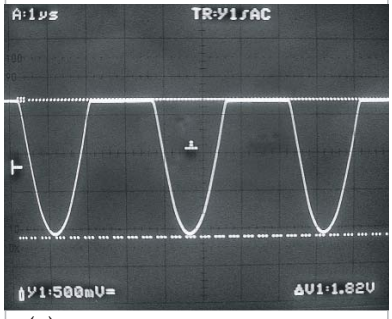


(a)



(b)



(c)

Figure 6 A clean sine wave (V_{22} in Figure 3) appears across the tuned circuit at 280 kHz for values of 147 µH and 2200 pF for L_1 and C_1, respectively (a). The sine wave with respective values of 56 µH and 60 pF differ (b). The output waveform at 280 kHz, for values of 147 µH for L_1 and 2200 pF for C_1, exhibits a flat top (c).

Use a system's real-time clock to "hide" a code sequence

Mihaela Costin, Delmhorst Instruments, Towaco, NJ

Although the concept of a totally accessible system represents an ideal situation for users, designers now must limit access to—and conceal code sequences for—software routines for calibration, diagnostics, memory erasure, system reset, and more. In a system that includes a computer-compatible interface, such as an RS-232, a GPIB, or an infrared-I/O port, the system's software can detect unique input patterns and execute the "secret" code sequences. But if a system lacks a data port, any attempt to implement a secret-access feature in a publicly accessible user interface makes it transparent to the user, even if the feature includes password protection. This Design Idea offers an efficient way to activate a code sequence without making the customer aware that such a feature exists and without requiring any hardware modifications.

If a system includes an RTC (real-time clock), you can define a date and time stamp that invokes the hidden code. The date acts as a password, and, if you choose a date far in the past, a casual user would be unlikely to stumble across it. To implement the routine, you can modify the system software by inserting a date- and time-check routine at the location in which the hidden code executes. Under normal conditions, the program skips the hidden code and executes the routine only if the system's date matches the one that the routine specifies.

For example, the following pseudocode illustrates the use of Aug 12, 1980, as a system "password":

```
Check_date:
  if (Read_RTC(year) ==1980 and
  Read_RTC(month) ==8 and
  Read_RTC(day) ==12)
                run_hidden_sequence();
  Continue_the_Code();
```

After completing the procedure, you must remember to reset the system's clock to the current date and time. Otherwise, the system executes the special code for the remainder of the day until the clock rolls over to the next day. EDN

Shunt regulator eases power-supply-start-up woes

Michael O'Loughlin, Texas Instruments, Nashua, NH

The popular and multiply sourced TL431 three-terminal shunt regulator offers designers considerable versatility in its applications. **Figure 1a** illustrates the TL431's internal circuitry, which comprises a precision voltage reference, an operational amplifier, and a shunt transistor (**Reference 1**). In a typical voltage-regulator application, two external resistors, R_A and R_B, determine the shunt-regulated output voltage at the lower end of load resistor R_S (**Figure 1b**). By way of illustration, the TL431 and a few external active and passive components can serve as a low-power auxiliary power supply for an SMPS (switched-mode-power-supply) PWM (pulse-width-modulated) controller. In some power-supply designs, an auxiliary winding on the step-down transformer supplies power to the PWM controller. Under light output loads, the auxiliary winding may supply inadequate power to the PWM controller. For example, the converter circuit in **Figure 2** derives power for PWM controller IC_1 through an auxiliary bias winding, W_{AUX}, which is part of transformer T_1. Resistor R_T and capacitor C_{HOLD} form a trickle-charge circuit that supplies start-up power to IC_1. To conserve energy, resistor R_T supplies just enough current to trickle-charge C_{HOLD} to voltage V_{AUX}. Once the circuit starts, it

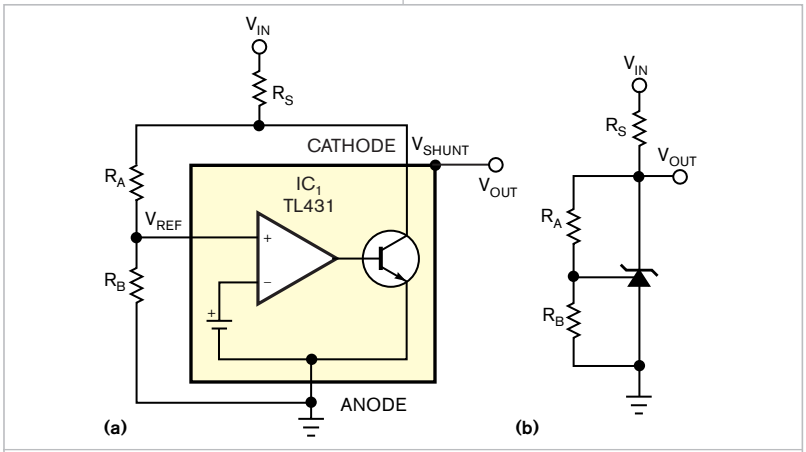


Figure 1 An uncomplicated block diagram (a) conceals the TL431's internal complexity, but you need only three external resistors to use the TL431 in a basic shunt-regulator circuit (b).

operates as you would expect and delivers output power to the load, and the auxiliary winding and its components power the PWM controller.

However, removing the output load reduces the energy supplied to the auxiliary bias winding, depleting the charge on C_{HOLD} and causing IC_1 to turn off, which in turn upsets output-voltage regulation and causes the power supply to operate erratically. A low-power bias-supply circuit supplies light-load start-up power and then switches off to conserve power whenever the auxiliary winding can supply enough energy to PWM controller IC_1 (**Figure 3**). In this circuit, a series-pass regulator turns on under light-load conditions and turns off when the bias winding can supply the energy to the PWM controller, thus conserving energy under load and improving converter efficiency.

Resistors R_A through R_D, shunt regulator IC_1, diode D_1, and transistor Q_1 form the low-load series-pass-regulated bias supply. You select these components to produce a voltage at Q_1's emitter that falls between IC_1's turn-off voltage and the nominal voltage produced by rectifying the auxiliary bias winding's output, V_{AUX_NOM}. In effect, the voltage at IC_1's V_{CC} pin follows in wired-OR fashion whichever is higher: V_{AUX_NOM} or the voltage at transistor Q_1's emitter. When the auxiliary bias winding and its components deliver sufficient power, Q_1's emitter sees a reverse bias, and Q_1 shuts off to conserve energy. Conversely, Q_1 supplies power when V_{AUX} decreases below V_{AUX_NOM} due to a light output load. Note that the circuit still must include trickle-charge resistor R_T because most PWM controllers incorporate undervoltage lockout, the ability to start at a higher than nominal supply voltage.

To design the series-pass regulator, select resistor R_C to supply sufficient operating current to IC_2, and select resistor R_D to maintain Q_1's collector voltage and current within its safe operating area. Select resistors R_A and R_B to set the series regulator's output voltage above IC_1's start-up voltage and below the nominal voltage supplied by the auxiliary winding's rectified output. Choose bypass capacitor C_A to minimize ripple voltage across IC_2.

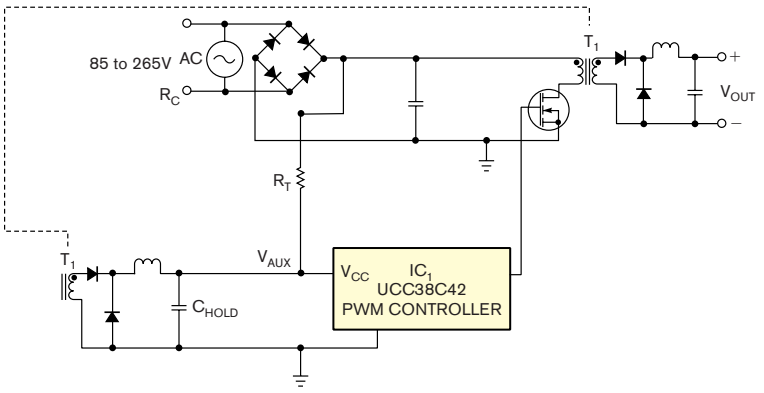


Figure 2 An auxiliary winding supplies power to the supply's PWM controller.

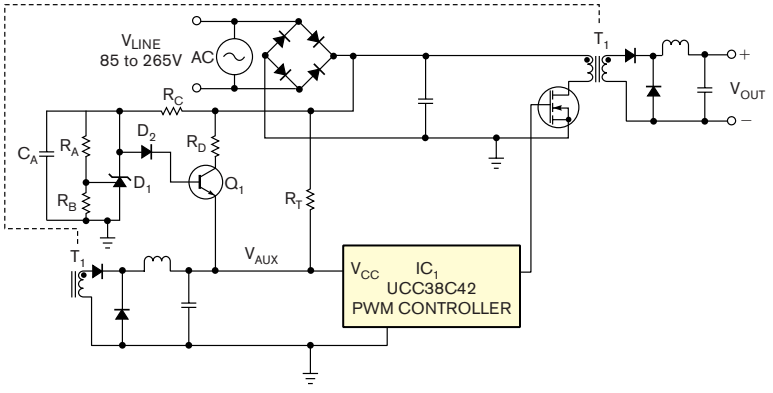


Figure 3 In this improved design, pulse-width-controller IC_1 derives its power from R_T for start-up, auxiliary winding W_{AUX} for normal operation, and shunt-regulator circuit IC_2 and Q_1 for low-load operation.

You can use the following **equation** to adjust the voltage divider formed by resistors R_A and R_B:

$$\frac{V_{REF}}{R_B} = \frac{V_{AUX\_NOM} - V_{DI} - V_{BE(Q_1)} - V_{REF} - 1V}{R_A}.$$

The voltage at Q_1's emitter must fall below the nominal auxiliary voltage, which the auxiliary bias winding supplies. V_{REF} represents shunt regulator IC_2's internal nominal reference voltage of 2.495V, and V_{DI} and $V_{BE(Q1)}$ represent D_1's voltage drop and Q_1's forward base-emitter voltage, respectively. EDN

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1 O'Loughlin, Michael, "Shunt regulator serves as inexpensive op amp in power supplies," *EDN*, Sept 15, 2005, pg 96, www.edn.com/article/CA6255051.

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READERS SOLVE DESIGN PROBLEMS

Temperature-to-period circuit provides linearization of thermistor response

S Kaliyugavaradan, Anna University,
Madras Institute of Technology, Chennai, India

Designers often use thermistors rather than other temperature sensors because thermistors offer high sensitivity, compactness, low cost, and small time constants. But most thermistors' resistance-versus-temperature characteristics are highly nonlinear and need correction for applications that require a linear response. Using a thermistor as a sensor, the simple circuit in **Figure 1** provides a time period varying linearly with temperature with a nonlinearity error of less than 0.1K over a range as high as 30K. You can use a frequency counter to convert the period into a digital output. An approximation derived from Bosson's Law for thermistor resistance, R_T, as a function of temperature, θ, comprises $R_T=AB^{-\theta}$ (see **sidebar** "Exploring Bosson's Law and its equation" on the Web version of this article at www.edn.com/051110di1). This relationship closely represents an actual thermistor's behavior over a narrow temperature range.

You can connect a parallel resistance, R_P, of appropriate value across the thermistor and obtain an effective resistance that tracks fairly close to $AB^{-\theta}\simeq$ 30K. In **Figure 1**, the network connected between terminals A and B provides an effective resistance of $R_{AB}\simeq AB^{-\theta}$. JFET Q_1 and resistance R_S form a current regulator that supplies a constant current sink, I_S, between terminals D and E.

Through buffer-amplifier IC_1, the voltage across R_4 excites the RC circuit comprising R_1 and C_1 in series, producing an exponentially decaying voltage across R_1 when R_2 is greater than R_{AB}. At the instant when the decaying voltage across R_1 falls below the voltage across thermistor R_T, the output of comparator IC_2 changes its state. The circuit oscillates, producing the voltage waveforms in **Figure 2** at IC_2's output. The period of oscillation, T, is $T=2R_1C_1\ln(R_2/R_{AB})\simeq 2R_1C_1[\ln(R_2/A)+\theta\ln B]$. This equation indicates that T varies linearly with thermistor temperature θ.

You can easily vary the conversion sensitivity, $\Delta T/\Delta\theta$, by varying resistor R_1's value. The current source comprising Q_1 and R_1 renders the output period, T, largely insensitive to variations in supply voltage and output load. You can vary the period, T, without affecting conversion sensitivity by

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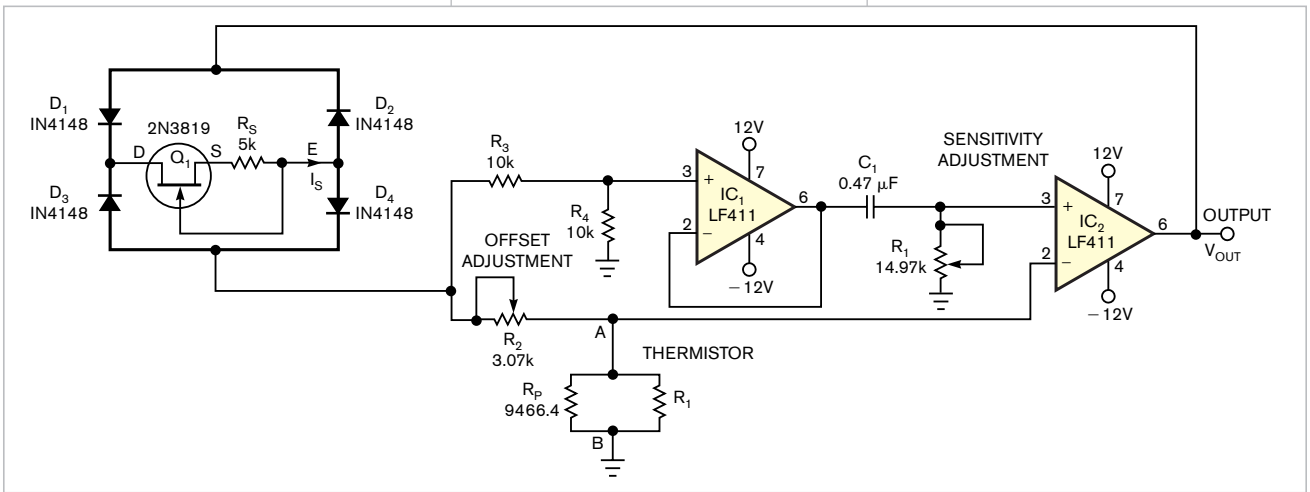

Figure 1 This simple circuit linearizes a thermistor's response and produces an output period that's proportional to temperature.

varying R_2. For a given temperature range, θ_L to θ_H, and conversion sensitivity, S_C, you can design the circuit as follows: Let θ_C represent the center temperature of the range. Measure the thermistor's resistance at temperatures θ_L, θ_C, and θ_H. Using the three resistance values R_L, R_C, and R_H, determine R_P, for which R_{AB} at θ_C represents the geometric mean of R_{AB} at θ_L and θ_H. For this value of R_P, you get R_{AB} exactly equal to $AB^{-\theta}$ at the three temperatures, θ_L, θ_C, and θ_H.

At other temperatures in the range, R_{AB} deviates from $AB^{-\theta}$, causing a nonlinearity error that is appreciably less than 0.1K for most thermistors when the temperature range is 30K or less. You can easily compute R_P using: $R_P=R_C[R_C(R_L+R_H)-2R_LR_H]/(R_LR_H-R_C^2)$. Because temperature-to-period-conversion sensitivity, S_C, is $2R_1C_1\ln b$, you can choose R_1 and C_1 such that $R_1C_1=S_C[\theta_H-\theta_C]/\ln(R_{AB}$ at θ_L/R_{AB} at $\theta_H)$ to obtain the required value of S_C. To get a specific output period, T_L, for the low temperature, θ_L, R_2 should equal (R_{AB} at $\theta_L)e^Y$, in which Y represents $(T_L/2R_1C_1)$. In practice, use a lower value for R_2 because the nonzero response delay of IC_2 causes an increase in the output period.

Next, set potentiometers R_1 and R_2 close to their calculated values. After you adjust R_1 for the correct S_C, adjust R_2 until T equals T_L for temperature θ_L. The two voltage-divider resistances, R_3 and R_4, should be equal in value and of close tolerances. As a practical example, use a standard thermistor, such as a Yellow Springs Instruments 46004, to convert a temperature span of 20 to 50°C into periods of 5 to 20 msec. This thermistor exhibits resistances for R_L, R_C, and R_H of 2814, 1471, and 811.3Ω, respectively, at the low, midpoint, and high temperatures. Other parameters for the design include S_C=0.5 msec/K, θ_L=20°C, θ_H=50°C, θ_C=35°C, and T_L=5 msec.

Because only a fraction of current I_S is through the thermistor, I_S should be low to avoid self-heating effects. This design uses an I_S of approximately 0.48 mA, which introduces a self-heating error of less than 0.03K for a thermistor's dissipation constant of 10 mW/K. **Figure 1** illustrates the values of the components in the example. All resistors are of 1% tolerance and 0.25W rating; use a polycarbonate-dielectric capacitor for C_1.

Simulating various temperatures from 20 to 50°C by replacing the thermistor with standard, 2814 to 811.3Ω, 0.01%-tolerance resistors produces T values of 5 to 20 msec with a maximum deviation from correct readings of less than 32 µsec, which corresponds to a maximum temperature error of less than 0.07K. Using an actual thermistor produces a maximum error of less than 0.1K for a thermistor dissipation constant of 10 mW/K or less. EDN

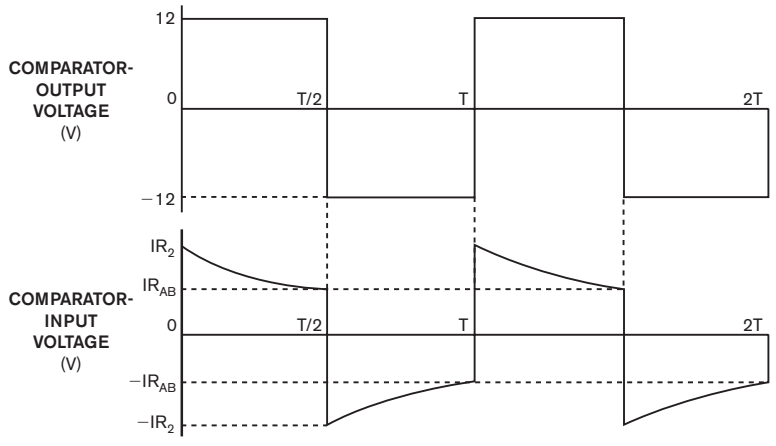

Figure 2 Waveforms show input to comparator IC_2 (lower trace) and its output (upper trace). In the lower trace, IR_2 represents the voltage across R_2.

Two wires control SPI high-speed ADC

Dan Meeks, Texas Instruments Inc, Austin, TX

Most current microprocessors, DSPs, and field-programmable gate arrays integrate hardware and software resources that support either or both of two common interface standards—SPI (serial-peripheral interface) and I^2C (inter-IC)/SMBus. Both two-wire-interface standards suffer from a few crucial disadvantages. For example, I^2C's throughput rates are 100 kbps, 400 kbps, or 3.4 Mbps in standard-, fast-, and high-speed modes, respectively, and can thus restrain a fast peripheral data converter's sample rate. Excluding framing and overhead bits, a 100k-sample/sec, 12-bit ADC must transfer at least 1.2 Mbps over the interface, a rate that only I^2C's high-speed mode supports. Many processors and controllers currently offer no I^2C high-speed mode and thus would be unable to support a fast data converter.

One of I^2C's major benefits reduces the number of host-to-target interconnections. Using only two wires plus ground, the host controller can address the target device and exchange data, whereas SPI requires three wires—data, clock, and chip-selection—plus ground. Multiple SPI-target devices can share data and clock lines, but each device requires its own

dedicated chip-selection line.

Given the perpetual demand for higher sample rates and resolution, I²C's limited speed may restrict its use in some applications and instead force designers to select SPI. However, SPI requires an additional I/O pin on the host controller. In situations in which extra pins are unavailable but the application requires a fast SPI-bus converter, you can apply the technique in **Figure 1**.

For example, Texas Instruments' ADS7816 comprises a 200k-sample/sec, 12-bit-sampling ADC that requires a bit rate of 3M samples/sec to sample continuously at a 200k-sample/sec rate (**Reference 1**). Selecting the ADS7816's active-low $\overline{CS}$ (chip-select) pin initiates a conversion cycle. After toggling and holding $\overline{CS}$ low during the data transfer, $\overline{CS}$ returns high after transferring the data completes the process.

When the clock line initially goes low, it also asserts $\overline{CS}$ to a low state. The time constant of the peak detector comprising D_1, R_1, and C_1 ensures that $\overline{CS}$ does not go high until the clock line remains high for more than one clock cycle (**Figure 2**). Although the clock line toggles and retrieves data from IC_2, $\overline{CS}$ remains asserted low, and, upon completion of retrieval, the clock line goes high, and $\overline{CS}$ follows, readying the circuit for another conversion cycle.

Because C_1 must discharge at the end of a conversion cycle, the controller should delay the start of the next conversion cycle until C_1 fully discharges. Careful choice of R_1 and C_1 minimizes the delay to a minimum of three clock cycles. In addition, the voltage across C_1 must not fall below inverter IC_{1B}'s input threshold before the next clock pulse arrives to refresh the capacitor's voltage. Inverter IC_{1A}'s output voltage and current capabilities affect C_1's recharge time, and R_1 and IC_{1B}'s input impedance affect the discharge time. To ensure a robust design, include components' tolerances and temperature coefficients along with variations of logic-input and -output thresholds. EDN

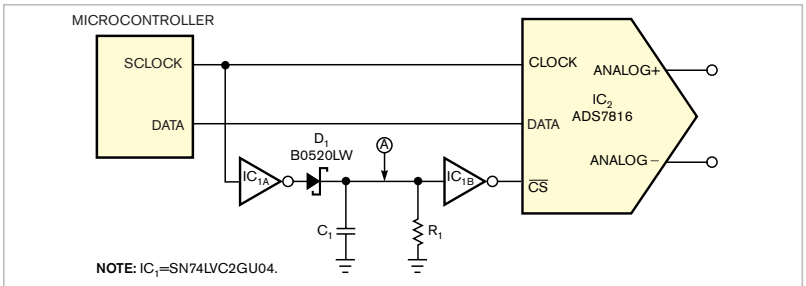

Figure 1 Two inverters and a few components can substitute for an SPI ADC's chip-select line.

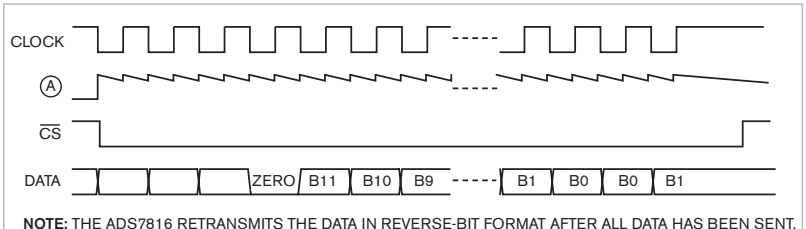

Figure 2 An SPI-clock waveform (top trace) evokes data (bottom trace), and peak detection of the clock (the waveform at Point A in Figure 1) yields a signal (next-to-bottom trace) that mimics the chip-selection line's behavior.

REFERENCE

1 ADS7816 data sheet, http://focus.ti.com/docs/prod/folders/print/ads7816.html, Texas Instruments.

Volume-unit meter spans 60-dB dynamic range

Jon Munson, Linear Technology Corp, Sunnyvale, CA

An audio volume-unit meter displays peak-related audio amplitudes to aid in accurately setting recording levels or for displaying an amplifier's operating conditions. A simple diode and capacitor network provides a classic volume-unit meter's peak-weighted response, but the circuit typically limits response to about 23 dB of displayable dynamic range, and the meter suffers from errors that its pointer's inertia and mechanical "ballistics" introduce. Contemporary displays eliminate the inertia problem by using arrays of lighted elements to form bar graphs, but any shortcomings in response and accuracy characteristics now shift to the signal-processing domain. You can use DSP techniques and applied mathematics to replicate a meter's functions in firmware, but this approach gets relatively expensive if the device doesn't already include DSP functions to spare.

An inexpensive analog meter's weakness remains its peak-hold element, a capacitor that must charge quickly to accommodate large signals and accurately for small signals—two mutually exclusive goals. In addition, the nonideal characteristics of the diodes for

(continued on pg 88)

full-wave rectification and peak-hold functions also limit an analog volume-unit meter's dynamic range. Preserving 20 dB of display dynamics and monitoring signal levels that can vary over a 40-dB range, which is typical in consumer electronics, call for a circuit with a dynamic range on the order of 60 dB.

In most instances, traditional circuits fail to simultaneously provide the intended accuracy and slew rate, particularly at low signal levels over a wide dynamic range. The circuit in **Figure 1** offers a simple configuration that delivers high accuracy over a dynamic range that exceeds 60 dB and provides the rapid-attack/slow-decay characteristics that a high-quality display requires.

The heart of the circuit is a Linear Technology LT1011 comparator, IC_2, which monitors the difference between the incoming signal's amplitude and the peak-detected output. It also delivers charging current to a 4.7-µF hold capacitor, C_6, whenever the state of its charge is too low. Unfortunately, the input-to-output delay inherent in comparators and nonlinear amplifiers determines the minimum output-pulse width. If the hold capacitor charges quickly to track large input bursts, the minimum charge step must greatly exceed the level of small signals and thus limits the dynamic range.

Inductor L_1 solves the capacitor-response problem by providing an adaptively variable source of charging current. Adding a 10-mH inductor limits the maximum current rate when the comparator generates narrow pulses, thus reducing the minimum charging amplitude step to a smaller level of 1 mV or less. For wider charging pulses, the current automatically ramps up to higher levels to provide the desired high slewing rate. The minimum charge step is essentially proportional to the signal-step size, ensuring a constant relative accuracy of better than 1 dB over a 60-dB signal range. A signal level of −59 dB corresponds to a 13-mV input, and a meter-scale factor of 0 dB of 2V peak corresponds to the input level necessary for a typical gain-of-20 audio power amplifier to deliver 100W rms into an 8Ω load, or approximately 40V peak output.

The circuit also includes two operational-amplifier stages based on Linear Technology's high-accuracy LT1469 dual op amp. The first stage, IC_{1A}, provides gain of a factor of six in this example, so that a 2V input peak provides a 12V output. The second op-amp stage, IC_{1B}, forms a precision inverting half-wave rectifier. The outputs from IC_{1A} and IC_{1B} and the positive-peak-detected voltage across C_6 combine at IC_2's input to provide a zero-crossing threshold to the comparator. When its input falls below 0V, IC_2's output switches on Q_1 and delivers charge to C_6 until the voltage across C_6 reaches or slightly exceeds the amplified audio voltage. The feedback network comprising R_8 and C_4 provides an optimal volume-unit-metering discharge. EDN

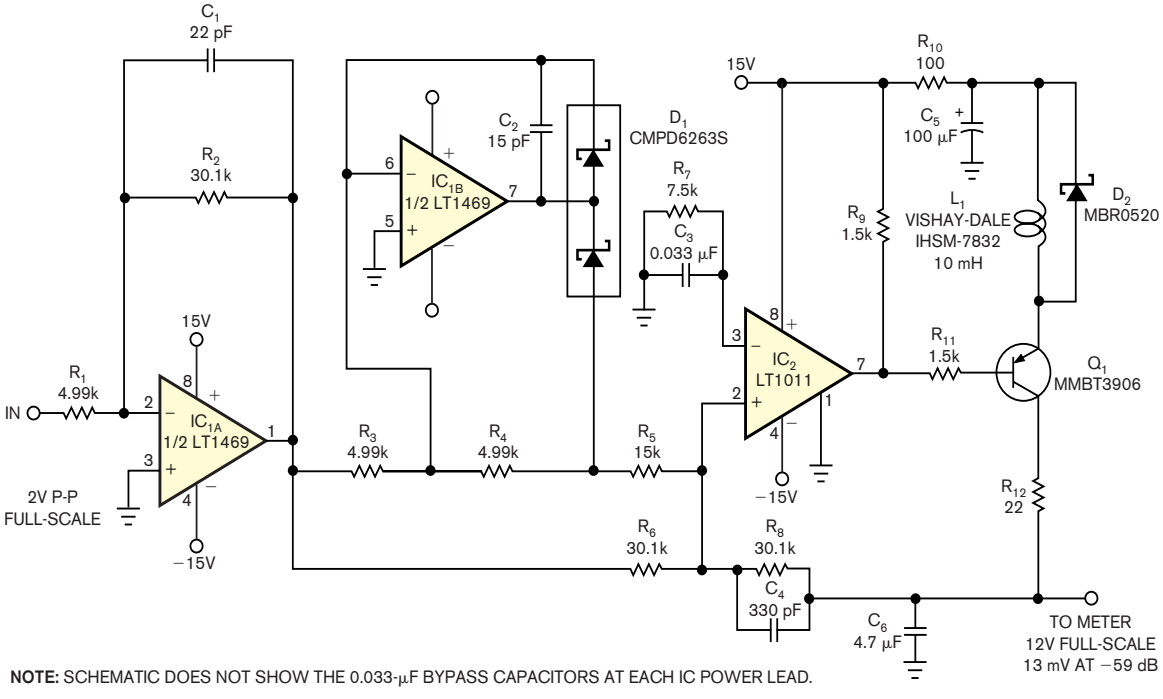

Figure 1 This inductor-compensated voltage-unit meter displays a 60-dB dynamic range.

Pacer clock saves subroutine calls

Enver Torlakovic, Willmot, New South Wales, Australia

This Design Idea outlines an easy-to-implement time-delay routine that requires no subroutine calls and thus avoids possible stack-overflow problems (**Listing 1**). This method also saves RAM space by requiring in most cases only two variables: the PACER_CLOCK as a free-running counter and another variable introduced at a particular instance (for example, TIME_VAR). The routine dedicates the microcontroller's Timer 0 to generate an interrupt-on-overflow instruction every 10 msec or at any other desired interval. You assign the Timer 0 interrupt a low priority in the initialization code and then enable the Timer 0 any convenient time. After assignment, do not alter the interval because many services likely depend on the pacer-clock routine. Note that the routine can achieve delays of as much as 255 times the Timer 0 overflow period.

Listing 1 is written for Microchip's PIC18F242 flash-memory controller, but porting the routine to another microcontroller should pose few problems. When copying the code to paste it into routines, note that you must change the labels—in this example, "wait_loop100"—at each application of the code between the rows of asterisks in the **listing.** EDN

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You can download the listing from the Web version of this Design Idea at www.edn.com/051110di2.

LISTING 1—TIME-DELAY ROUTINE

```
int_test_timer0

        btfss       INTCON,     TMR0IF      ; test if Timer0 IRQ was active
        goto        int_test_INT1                       ;if not, check
next INT source
        bcf         INTCON,     TMR0IE              ;disable Timer0 int.
        bcf         INTCON,     TMR0IF      ; clear Timer1 H/W flag

        ;Jobs to do here:    INC the PACER_CLOCK variable

        incf        PACER_CLOCK         ;This variable is a free running
counter

        ;RELOAD TIMER0 now: (Timer0 set for 10 milliseconds pacer clock)
        ;Note: Rollover occurs after the Timer reaches 0xFFFF
        ;Required number of ticks is calculated as: 0xFFFF-(TMR0H:TMR0L)

        movlw       0x0D                        ; High byte
        movwf       TMR0H               ; Reload Timer0 high
        movlw       0x61                        ; LOW byte
        movwf       TMR0L               ; Reload Timer0 low.

        ;Note: for an internal clock period of 0.161002 microseconds, count 62111 clocks
        ;to make up  the 10 millisecond interval.

        bcf         INTCON,     TMR0IF      ; clear Timer1 H/W flag
        bsf         INTCON,     TMR0IE              ;Re-enable the Timer0
interrupt
        bsf         T0CON,          TMR0ON          ; turn ON Timer0
module

int_test_INT1
        ;code for INT1 starts from here…
        .
        .
retfie          ;return from interrupt
```

```
Somewhere in the code:

                ;*******************
        movf            PACER_CLOCK, w      ;get the current Pacer_Clock
state
        addlw       D'10'                                   ; to
count up to 10  Timer0 overflow periods
        movwf       TIME_VAR                    ;load the time variable
with the contents of …

            ;…PACER_CLOCK plus 10
wait_loop100
        ;do some jobs here…
        ;….
        ;…
        movf            PACER_CLOCK, w
        xorwf           TIME_VAR, w                         ;check
if PACER_CLOCK was incremented 10 times
        tstfsz          WREG
        ;if zero, files are equal = Timed Out !
        goto            wait_loop100
        ;otherwise wait longer

            ;*******************
```

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Stereo-amplifier IC's outputs drive multiple loads

Jean-Jacques Avenel, Maxim Integrated Products, Lesigny, France

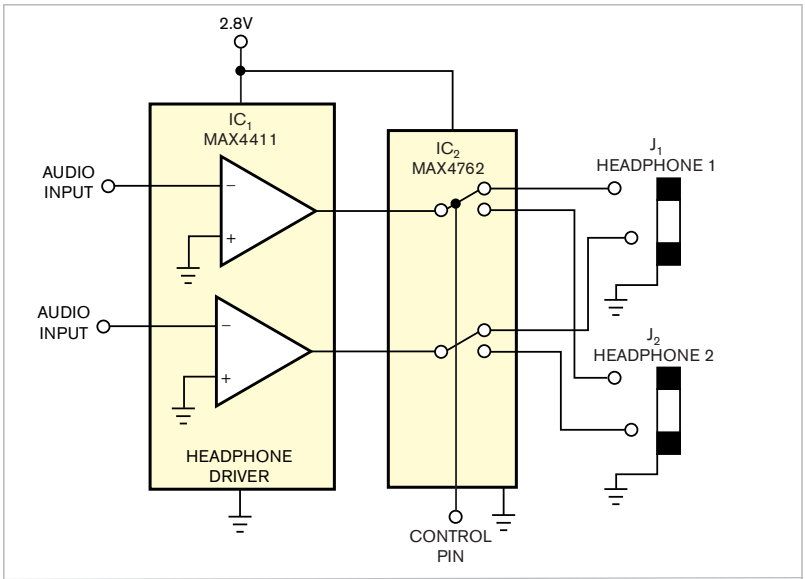

Figure 1 For low values of power-supply voltage, 2.8V maximum, use an analog switch at IC_2 that handles signal amplitudes to $V_{DD}-5.5V$ to direct IC_1's bipolar outputs to the headphone loads.

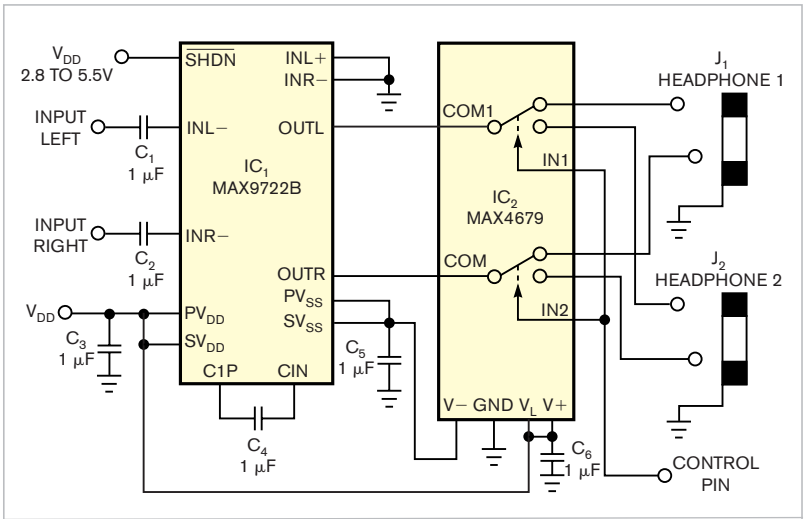

Figure 2 Higher values of V_{DD}, 2.8 to 5.5V, require a different amplifier and a dual-supply-voltage switch at IC_2.

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Newer generation, directly coupled stereo-amplifier ICs can directly drive headphones and speakers and thus eliminate bulky and expensive output-coupling capacitors. Many of these amplifiers also include a charge pump for generating an internal negative-supply-voltage rail to produce a bipolar-output swing while operating from one positive-supply voltage. However, if your applications require switching the amplifier's output between two or more headphones or other loads, you cannot necessarily use a simple electronic analog switch. Many analog switches can't handle a signal that makes excursions above the positive-power-supply voltage, V_{DD}, or below ground. Depending on V_{DD}'s maximum value, you can apply one of two approaches.

If V_{DD} falls below 2.8V (**Figure 1**), choose a switch for IC_2 such as Maxim's MAX4762, which handles negative signals down to V_{SS} of −5.5V, where V_{DD} can range from 1.8 to 5.5V with a typical on-resistance of 0.6Ω. If V_{DD} falls between 2.8 and 5V, use a dual-supply, low-on-resistance switch, such as Maxim's MAX4679 at IC_2 (**Figure 2**), along with a different stereo amplifier, such as the MAX9722B, IC_1, to handle the higher V_{DD}. For the switch's negative supply, you can use the nega-

tive voltage generated within the MAX9722B to eliminate the need for an additional charge-pump-power-supply circuit.

To enhance a mobile-telephone design, you can use a stereo-headphone jack to accommodate a hands-free combination earphone and microphone. You use the stereo jack's tip connection as the headphone contact, the ring contact for the microphone, and the shell contact as the common connection to ground (**Figure 3**). When you connect the hands-free combination, you must also turn off one channel of headphone amplifier IC_1. Although the MAX4411 amplifier offers an individual-channel-shutdown feature, the device's outputs present an impedance of 2 kΩ to ground when you switch it off.

An electret microphone capsule typically includes an open-drain JFET-output circuit that typically requires a 2-kΩ resistor, R_1, which connects to a low-noise, positive-supply voltage of approximately 2V. The resistor provides dc bias to the JFET and allows the microphone capsule's audio-output signal to appear on the output terminal. In most applications, the microphone's output connects directly to a high-impedance, low-noise amplifier, IC_3, by ac coupling of capacitor C_1.

The amplifier's 2-kΩ-to-ground off-impedance would heavily load the microphone and halve its dc bias, moving it out of its optimum operating range and reducing its output and SNR. Adding analog switch IC_2 between the microphone and the headphone amplifier's output maintains the microphone's bias and resistive load. EDN

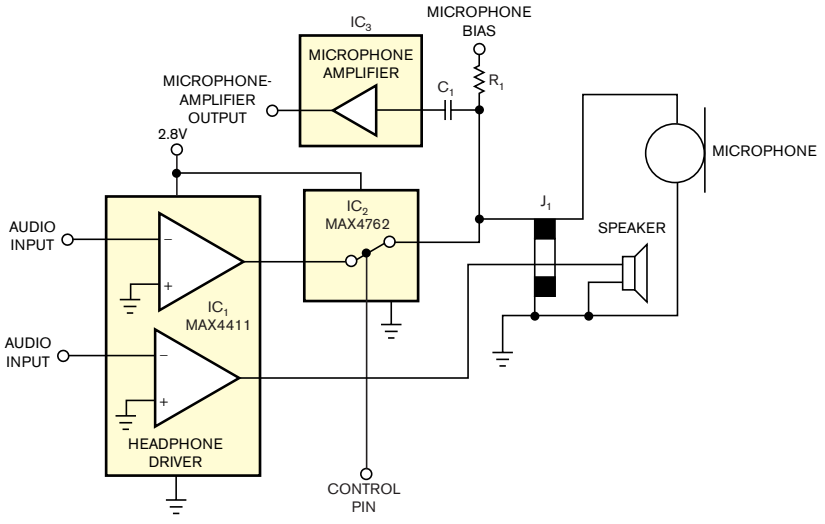

Figure 3 When using a hands-free microphone/earphone kit as an alternative to stereo headphones, add the circuitry shown to avoid loading the microphone's output with the headphone-driver amplifier's output.

Muscle power drives battery-free electronics

Alexander Bell, Infosoft International Inc, Rego Park, NY

Recent developments in electric-double-layer-capacitor technology have made it possible to replace rechargeable batteries in certain secondary-power-storage applications (**Reference 1**). Capacitors offer significant advantages over rechargeable batteries, including a practically unlimited number of charge/discharge cycles, survival of short circuits, and simple charging circuits that require only overvoltage protection. In addition, storage capacitors recharge quickly and pose no toxic-waste-disposal problems when the product reaches the end of its service life.

This Design Idea extends an earlier one by describing a muscle-power-driven capacitor charger. The combination of a muscle-powered electrical generator and a high-value capacitor provides a highly autonomous and environmentally clean power approach for emergency equipment and survival kits. Applications of such an alternative "renewable" energy source span a range of modern portable electrical and electronic devices, including cellular phones, MP3 players, AM/FM radios, PDAs, handheld PCs, and flashlights.

A muscle-powered capacitor charger contains only a few components: a storage capacitor, a bridge rectifier, and a voltage-limiting zener diode that protects the capacitor from excessive voltages (**Figure 1**). For practical energy-storage experiments, you can use 1 or 0.47F capacitors with 5.5V maximum ratings, such as those available from NEC-Tokin America (www.nec-tokin.com, **Figure 2**). For more storage, you can use higher capacitance capacitors, such as Elna's (www.elna.co.jp) 100F, 2.5V Dynacaps (**Figure 3**).

You can remove the lamp from an

inexpensive, hand-powered flashlight and use its generator as a capacitor charger (**Figure 4**). Also, a variety of manually powered products now appearing on the market offer possibilities for experimentation. For higher outputs, you can use a stationary-bicycle-powered generator. Depending on the individual providing pedaling power, these generators can deliver average powers ranging from 20 to 100W. The hand-cranked flashlight in **Figure 4** originally lit a 2.5V, 0.15A, filament-type bulb, which consumes approximately 0.4W at full brightness. However, measurements show that the generator could deliver more power and could charge a 1F capacitor to 5V in approximately 10 sec. Thus, the following equation calculates the energy, E, stored in the capacitor of value C: $E=\frac{1}{2}C\times V_{MAX2}=12.5J$, and the following equation calculates the average maximum muscle-generated electrical power over time, T: $T_{MAX}=E/T=12.5/10=1.25W$.

You can use the following equation to calculate the effective energy, E_{EFF}, that the capacitor can deliver during its discharge cycle while its terminal voltage changes from maximum to minimum voltage: $E_{EFF}=\frac{1}{2}C(V_{MAX2}-V_{MIN2})$, where V_{MAX2} and V_{MIN2} represent the maximum and minimum operating voltages, respectively, applied to the powered devices. You can connect storage capacitors in parallel or in series. In both cases, make sure that the circuit includes proper overvoltage protection for the capacitors. To obtain additional voltages, you can add a dc/dc switched regulator to produce stable output voltages.

Important design considerations relate to the maximum voltage and current ratings of the diode-bridge rectifier and the zener diode, D_Z. Experimental measurements on the hand-cranked generator yield the following approximate values for its open-circuit voltage: maximum voltage of 10V rms, peak voltage of 14V, and maximum short-circuit current of 200 mA rms. For this application, an inexpensive bridge rectifier with 20V minimum peak-inverse voltage and 0.5A minimum forward current provide adequate margins. D_Z's breakdown-voltage rating should be slightly lower than the storage capacitor's maximum working voltage, and the diode's power rating—2W in this application—should exceed the product of the generator's maximum output current and the zener's conduction voltage. EDN

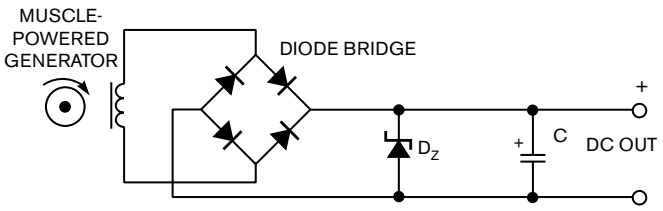

Figure 1 This charger circuit for storage capacitor C requires few additional components: a diode-bridge rectifier and an overvoltage-limiting zener diode.

Figure 2 Supercapacitors from NEC America provide 1F (left) and 0.5F of storage at 5.5V maximum and occupy little pc-board area.

Figure 3 These 100F, 2.5V Dynacaps from Elna approximate standard electrolytic capacitors in volume.

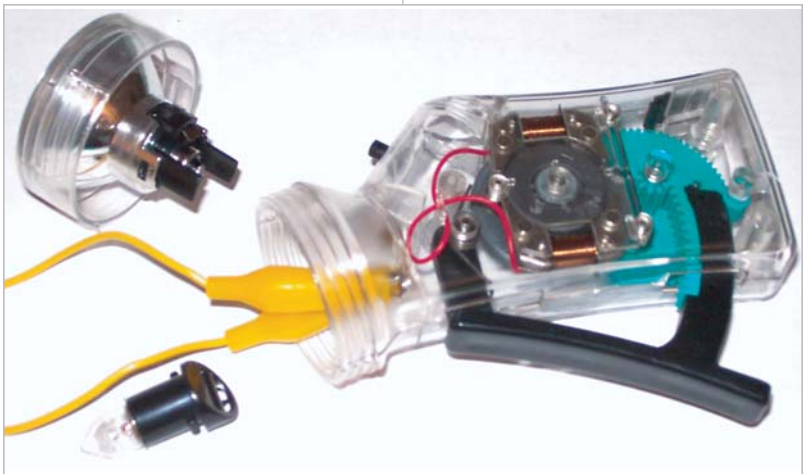

Figure 4 A hand-cranked flashlight's electrical generator serves as a muscle-powered charger for a high-capacity storage capacitor (lower left).

REFERENCE

1 Bell, Alexander, "Single capacitor powers audio mixer," *EDN*, March 14, 1997, pg 80, www.edn.com/archives/1997/031497/06DI_04.htm.

FET biasing targets battery-powered PWM applications

Steve Franks, Franks Development LLC, Tucson, AZ

Many PWM (pulse-width-modulated) applications, such as Class D audio amplifiers, require symmetric drive circuitry. Comprising complementary N- and P-channel FET devices with gates and sources connected, the textbook CMOS pair in **Figure 1** provides a low-impedance path to either the positive or the negative power supply and can directly drive a logic-level N-channel FET. Direct coupling of the CMOS pair to the logic driver works well in PWM systems in which the controlled devices operate at the same voltage as the logic circuits. However, raising the output FETs' power-supply voltage while driving the gates from lower voltage logic results in the P-channel device's remaining in conduction because of the difference between supply voltages.

To achieve an off-state, an amplifier's P-channel FET's gate must go to the positive-supply rail. Complementary-CMOS logic-level drivers can't accommodate the amplifier's high positive-supply voltage, and alternatives, such as using commercial FET drivers and operational-amplifier level-shift circuits, add cost and complexity. You can add an external high-voltage N-channel FET to drive the P-channel-amplifier FET's gate (**Figure 2**). However, capacitive loading imposes an exponential-rise characteristic on the drive waveform, leaving the P-channel FET in its linear operating region for an extended period and thus limiting switching frequency and causing significant power losses in the cascaded FETs.

Current-generation PWM systems can operate at relatively high switching frequencies and, as **Figure 3** shows, allow you to use a dc-blocking coupling capacitor, C_B, between the logic-level driver's output and the P-channel output FET's gate. Resistive divider R_1 and

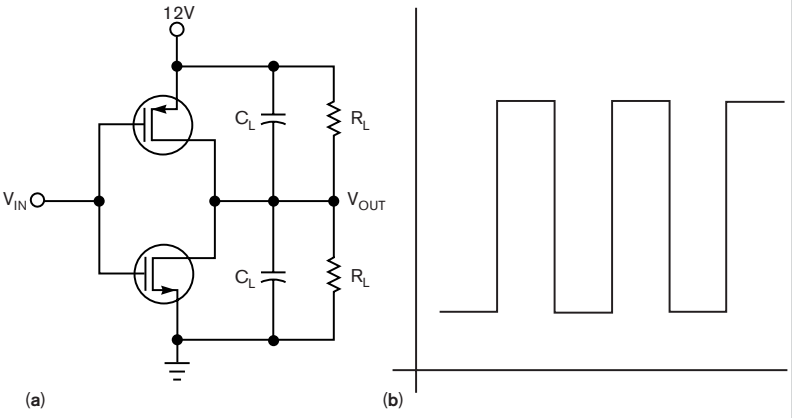

Figure 1 The textbook complementary-CMOS pair (a) produces a clean output waveform with fast on/off transitions (b).

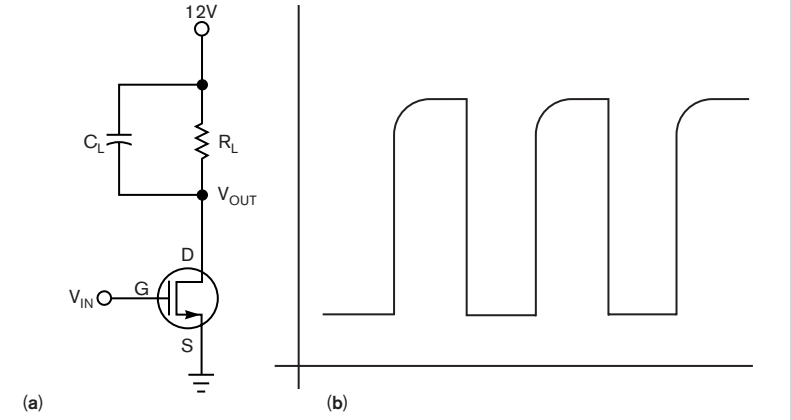

Figure 2 An N-channel FET driver (a) has output that exhibits an exponential rising edge on shutoff.

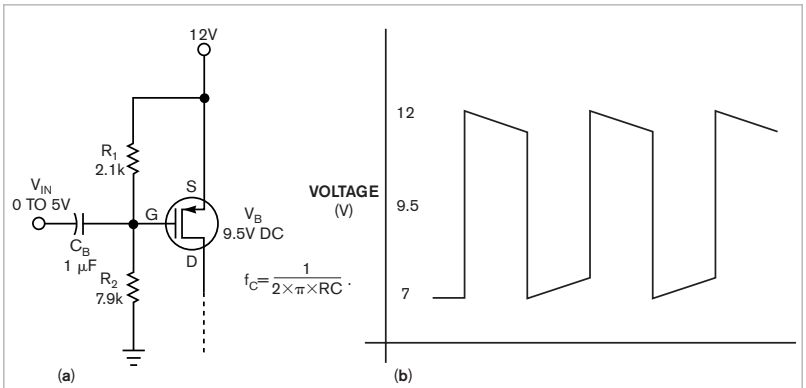

Figure 3 Adding resistive bias and capacitive coupling to an N-channel MOSFET (a) improves transition times but introduces waveform droop during on or off intervals (b).

R_2 applies a dc bias to the output FET's gate that's equal to the difference between the output power-supply voltage and the midrail logic voltage. For example, in a 12V Class D PWM audio amplifier driven from a 5V microcontroller, bias the P-channel FET's gate at 9.5V (12V−5V/2). Use the specified FETs for logic-level gate drive as output devices because other FETs don't exhibit nominal I_{DS} characteristics at gate drives of 5V or lower.

Battery-powered amplifiers with resistive-divider output-stage bias introduce an additional complication. As battery voltage decreases, so does bias. Instead, you can use a voltage-reference IC or a zener diode, D_1, to provide a constant bias voltage regardless of supply-voltage variations (**Figure 4**). This technique consumes less power than a purely resistive divider and offers more flexibility in coupling-capacitor selection to reduce waveform droop. Based on Texas Instruments' TPA2010 PWM power-amplifier IC (**Reference 1**), a Class D audio power amplifier boosts the TPA2010's 2.5W differential output to more than 200W rms into an 8Ω load (**Figure 5**).EDN

REFERENCE

1 TPA2101D1 data sheet, http://focus.ti.com/lit/ds/symlink/tpa2010d1.pdf.

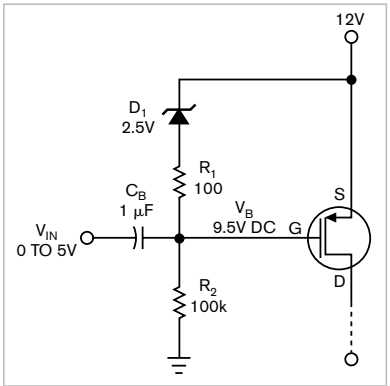

Figure 4 Inserting a zener diode into the bias divider allows optimization of the coupling capacitor's value and the P-channel device's bias voltage for logic-level drive.

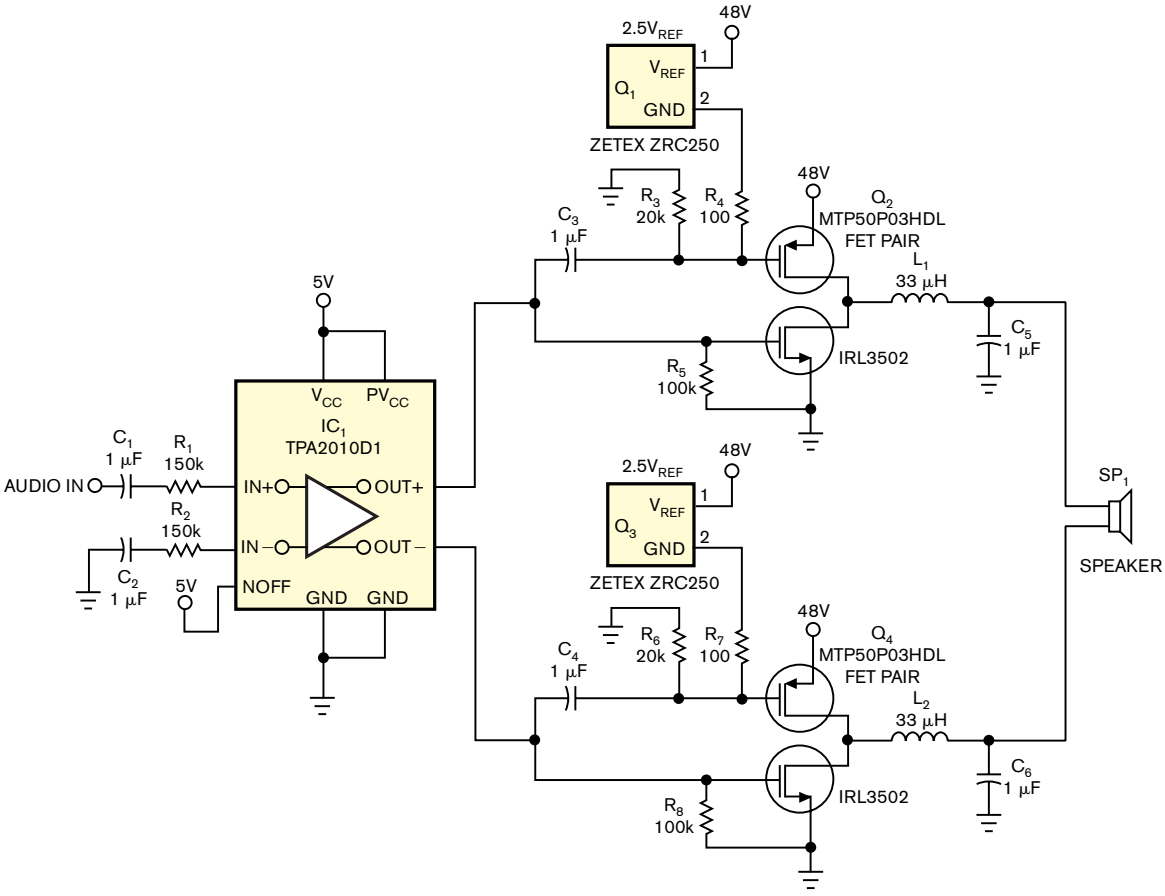

Figure 5 This Class D audio amplifier boosts its driver's output to 200W rms for a 48V power supply.

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designideas

READERS SOLVE DESIGN PROBLEMS

Low-cost BER tester measures errors in low-data-rate applications

Cedric Mélange, Johan Bauwelinck, Jo Pletinckx, and Jan Vandewege,
Ghent University, Ghent, Belgium

You don't need an expensive pattern generator to produce a PRBS (pseudorandom-bit-sequence) signal for making elementary BER (bit-error-rate) measurements in low-data-rate continuous-transmission systems (**Reference 1**). You also need not spend time programming on a computer to compare sent and received data patterns. Moreover, most professional BER-measurement equipment doesn't cover lower bit rates. This Design Idea offers a simple, low-cost alternative that can accommodate data rates as high as 20 kbps. The system tests a 10-kbps transceiver in low-power sensor networks. The pattern generator, a Hewlett-Packard (www.hp.com) E1401B, can produce PRBS streams of only 150 kbps and higher.

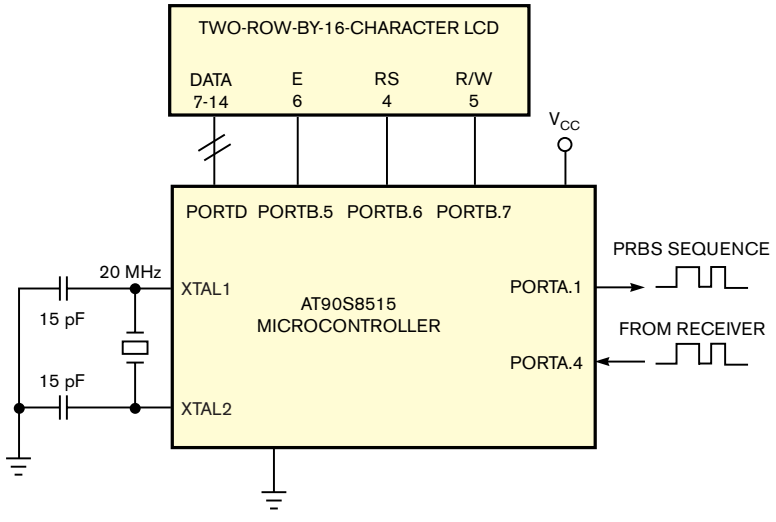

Figure 1 You can assemble a bit-error-rate-measurement circuit from only a few components.

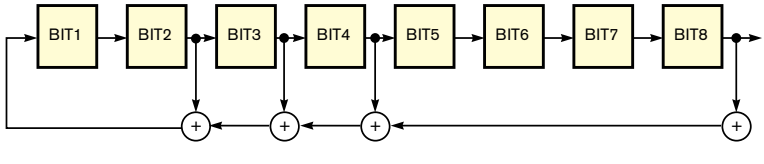

Figure 2 A linear-feedback-shift register generates a pseudorandom bit sequence.

An Atmel (www.atmel.com) AVR microcontroller creates a PRBS signal and compares the generated output stream with received data bits (**Figure 1**). After sending 1 million bits, the system displays the number of badly received bits on a two-row-by-16-character LCD. You can program the unit to transmit longer sequences of bits; however, doing so significantly increases the measurement time. Many low-cost or free development tools are available for AVR microcontrollers. This Design Idea uses an assembler and a serial programmer (**references 2** and **3**).

The design uses an 8-bit Fibonacci-type LFSR (linear-feedback-shift register) to produce the PRBS stream. The basic design includes a serial-shift register with modulo-2 addition using XOR instructions (**Figure 2**). You select the feedback taps' position to obtain a maximal-length sequence that has a period of 2^8-1 bits. Additional LFSR designs of different lengths and optimal feedback taps are also available (**Reference 4**). You can easily adapt the software in **Listing 1**, which is available for downloading at www.edn.com/

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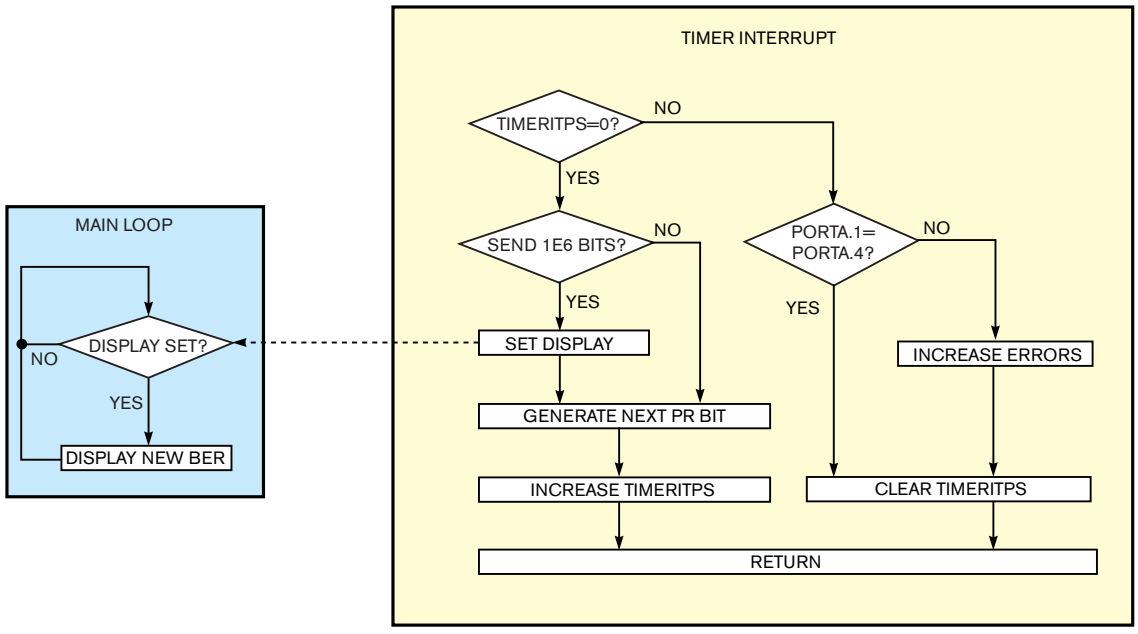

Figure 3 A simplified flow chart illustrates a BER tester's program subroutines.

051205di1 to produce PRBS signals with longer periods. A simplified flow chart of the assembler program is written for the AVR microcontroller (**Figure 3**).

The generated bit sequence appears at Pin Port A1, which you connect to a transmitter that's suitable for the system under test. Connect the digital output of a convenient receiver to Pin Port A4. The processor compares the received input with the output at Port A1 between two "send" bits. When the bits sent and received don't match, the number of displayed errors increases. If the system exhibits throughput delay, you need to modify the software to cope with the delay. EDN

REFERENCES

1 http://intec.ugent.be/design/.
2 AVRStudio 4, www.atmel.com.
3 SP12, www.xs4all.nl/~sbolt/e-spider_prog.html.
4 www.newwaveinstruments.com/resources/articles/m_sequence_linear_feedback_shift_register_lfsr.htm.

DMA eases CPU's workload for waveform generation

Mike Mitchell, Texas Instruments, Houston, TX

To generate analog voltages and waveforms, embedded systems often require one or more embedded or external DACs. To produce an analog voltage, the CPU must write the desired output value to the DAC at the appropriate time, a task that a timer-generated interrupt applied to the CPU usually initiates. In applications in which the DAC generates a periodic waveform, the CPU reads the next value from the table, sends it to the DAC, increments a table pointer, and checks for table boundaries to determine when to reset the table pointer.

Writing the periodic values to the DAC to maintain the output waveform requires CPU overhead, which varies depending on the data table's length, the output waveform's frequency, and the CPU's operating frequency. For example, using 32 data points per period to generate a 1-kHz sine wave requires the CPU to service 32,000 interrupts/sec. If the application requires a second analog output waveform, the CPU's loading increases, and updating both DACs within the required interrupt-service time may be impossible.

To calculate CPU loading, you need to know the length and the context-switching overhead of the ISR (interrupt-service routine). For the MSP430 processor, the ISR's overhead consumes 11 cycles, but the ISR's length depends upon how it is written. The assembly code in **Listing 1**, available at the Web version of this Design Idea at www.edn.com/051205di2, uses the fewest cycles to implement periodic waveform generation using one or two DACs. For a typical 1-MHz MSP430 CPU-instruction rate, serving 32,000 interrupts/sec leaves 1 million/32,000=

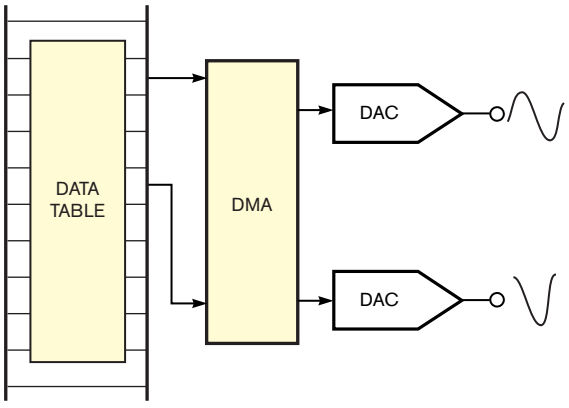

Figure 1 Using DMA, tabulated data values on their way to waveform-generating DACs avoid handling by a system's processor.

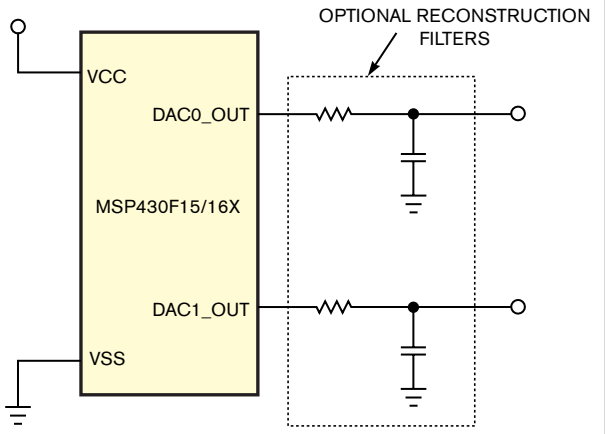

Figure 2 Optional lowpass filters on the DACs' outputs remove switching artifacts from the sine and the cosine waveforms.

31.25 CPU-instruction cycles between interrupts. An ISR requiring 18 cycles—that is, 18/31.25=57.6—represents a 57.6% CPU load. Supporting two DACs requires 23 cycles—that is, 23/31.25=73.6—and imposes a 73.6% CPU load. Increasing the MSP430's clock rate to its maximum 8 MHz reduces the CPU loading to 7.2 and 9.2%, respectively.

The required CPU load imposes limits not only on other tasks that the application may demand, but also on the waveform's maximum frequency. For example, a CPU operating at 100% CPU loading and an instruction rate of 1 MHz can generate a single waveform with a maximum frequency of approximately 1.73 kHz or two waveforms with a maximum frequency of approximately 1.35 kHz each. Raising the instruction rate to 8 MHz increases the respective maximum frequencies to approximately 13.9 and 10.9 kHz.

However, the MSP430F15x/16x family of devices includes a multichannel-DMA controller that can move data from one location to another without CPU intervention (**Figure 1**). In a waveform-generation application, the DMA controller moves data from the data table to the two DACs, significantly reducing the necessary CPU overhead to produce the waveforms. You can configure each of the DMA controller's three separate and independent channels to move a value from any address to any other address. In this example, one data table contains values for both the sine and the cosine waves, and two of the DMA channels simply access different parts of the table to form the sine and the cosine outputs. In addition, each DMA channel can independently increment its source or destination address. For this application, each DMA channel increments its source address, but the destination addresses of the respective DAC data registers always remain the same.

You can reconfigure each controller's preset number of DMA transfers. When either DMA channel has transferred its programmed number of data values, it begins the next data transfer from its originally programmed source address. In effect, each DMA channel treats its portion of the data table as a circular buffer to gener-

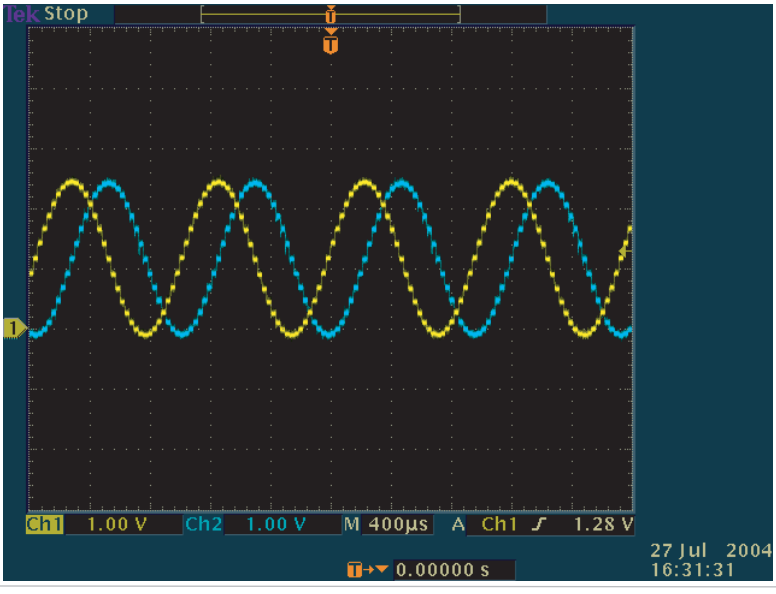

Figure 3 A phase shift occurs between the sine and the cosine output waveforms; removing the lowpass filters in Figure 2 reveals switching artifacts.

ate a periodic waveform. Although DMA transfers do not involve the CPU, each transfer does consume two CPU clock cycles, which delays CPU code execution and thus introduces overhead. For the single-waveform example, using DMA transfers consumes two clock cycles for each DAC update instead of the 18 cycles necessary when using only the CPU. Thus, for a CPU clock rate of 1 MHz, using DMA reduces the effective CPU loading from 57.6% to 6.4% and increases the possible maximum output frequency from approximately 1.73 kHz to approximately 15.6 kHz. For an 8-MHz clock rate, using DMA reduces single-waveform CPU loading from 7.2% to 0.8%.

Generating two waveforms requires two DMA transfers or four clock cycles. For the two-waveform example, DMA reduces loading from 73.6% to 12.8% for a 1-MHz instruction rate, and from 9.2% to 1.6% for an 8-MHz rate. For the 1-MHz instruction rate, using DMA increases the possible maximum frequency for two waveforms from approximately 1.35 kHz to approximately 7.8 kHz.

After initialization, each DMA controller simply performs its duties with no further intervention other than receiving a trigger to move the data value. In this example, each DAC's interrupt flag serves as a trigger for its respective DMA channel. When you use dual DACs, you can load each DAC with the next value of waveshape data before it's required and then simultaneously trigger both DACs using a timer to avoid introducing delays that manifest themselves as output harmonic distortion. **Listing 2**, also available at www.edn.com/051205di2, contains software that generates sine and cosine waves and illustrates the DMA channels' independent operation apart from the CPU. Note that, after initialization of DMA channels and other device-specific peripherals, no further CPU activity occurs.

Figure 2 shows a partial schematic of the DACs' outputs. Depending on the application, you may need to add optional resistance-capacitance lowpass filters at the DACs' outputs. Select values for the resistor and capacitor in each filter to produce a pole in the filter response at the desired output frequencies. Note that the oscilloscope photo in **Figure 3** was taken with filters removed to show the DAC outputs' unfiltered waveforms. EDN

Bipolar current source maintains high output impedance at high frequencies

Alex Birkett, University College London, Hospital National Health Service, London, UK

Traditional current sources and voltage-to-current converters based on instrumentation and operational amplifiers offer high output impedances at low frequencies because of the amplifiers' good low-frequency CMRR (common-mode-rejection ratios). At higher frequencies, decreasing CMRR, inherent output capacitances, and slew-rate limitations prevent realization of high-quality current sources. Two 200-MHz line-receiver/amplifier ICs from Analog Devices, the AD8129 and AD8130, offer differential inputs and outstanding CMRR, making them strong candidates for building high-frequency constant-current sources. Al-

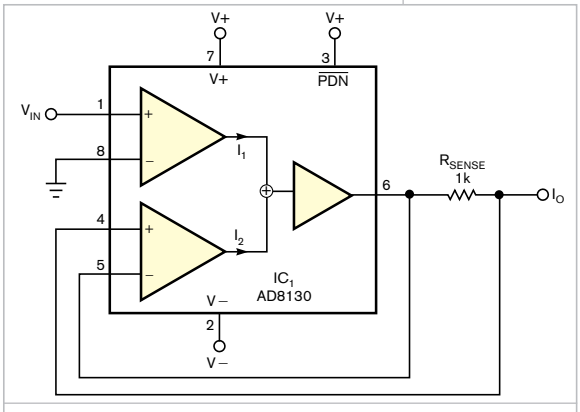

Figure 1 The 200-MHz AD8130 differential-input line receiver/amplifier can serve as a basic building block in a high-frequency-capable current source.

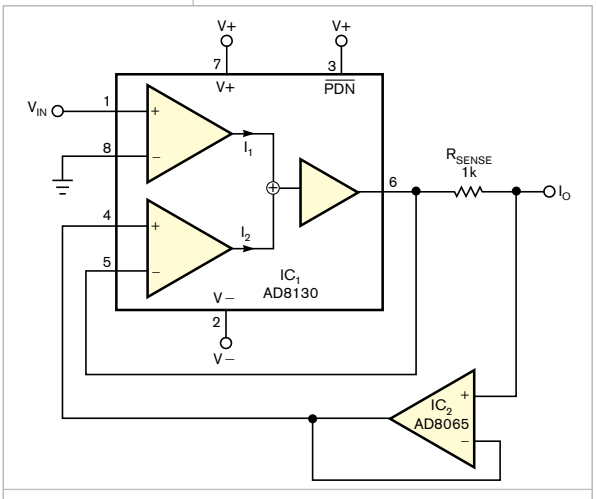

Figure 2 Adding an Analog Devices AD8065 buffer amplifier, IC_2, isolates the current-sampling resistor R_{SENSE} and reduces errors that IC_1's input-bias current contributes.

though the circuit in **Figure 1** provides a good starting point, the AD8130's relatively high input bias current can affect output-current accuracy at low current levels.

To overcome the problem, you can add a unity-gain buffer, IC_2, to isolate the current-sense resistor (**Figure 2**). In addition, you can use the buffer amplifier to measure the load voltage and bootstrap the output cable's capacitance. The circuit presents an output impedance of about 500 kΩ at 1 MHz and a current-compliance range of 0 to ±3V using ±5V power supplies.

Current sources that have capacitance-coupled loads benefit from a dc servo loop to stabilize the circuit's operating point (**Figure 3**). The value of output-coupling capacitor C_O depends on the desired low-frequency roll-off characteristic. Further improvements of the basic circuit enable compensation of output capacitance and increase the circuit's output impedance. A small, adjustable feedback capacitor, C_{COMP}, that's approximately one-half of the output's stray capacitances provides feedforward compensation and further reduces the effects of stray capacitance at the output (**Figure 4**). To prevent oscillation, the cable's shield-driver circuit's gain should be slightly less than unity. Note that reducing the output-current-sense resistor, R_9, to 100Ω compensates for the input attenuator formed by R_1 and R_2 and maintains a 1-mA/V characteristic. This voltage-to-current source's frequency range spans 20 Hz to 10 MHz. For best results, use high-frequency circuit-layout and power-supply-bypassing methods. EDN

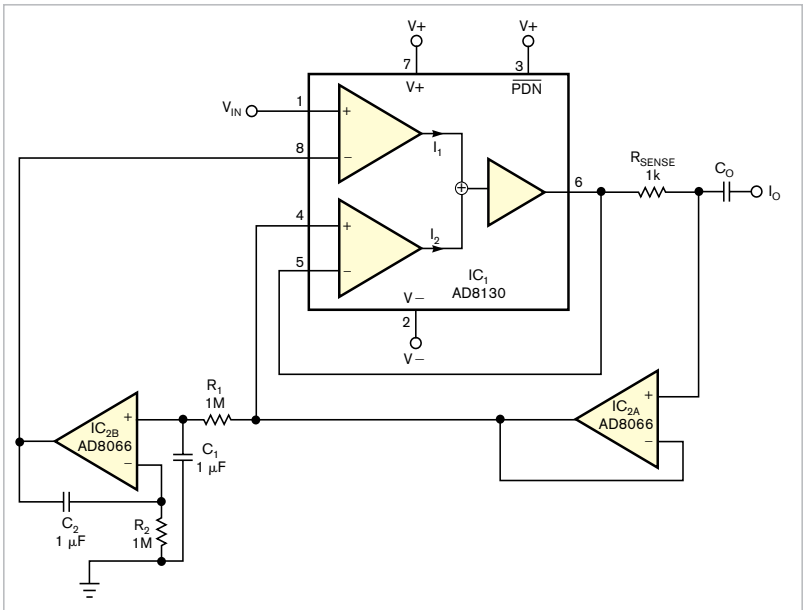

Figure 3 For an ac-coupled current output, add a dc-stabilization loop, IC_{2A} and IC_{2B}.

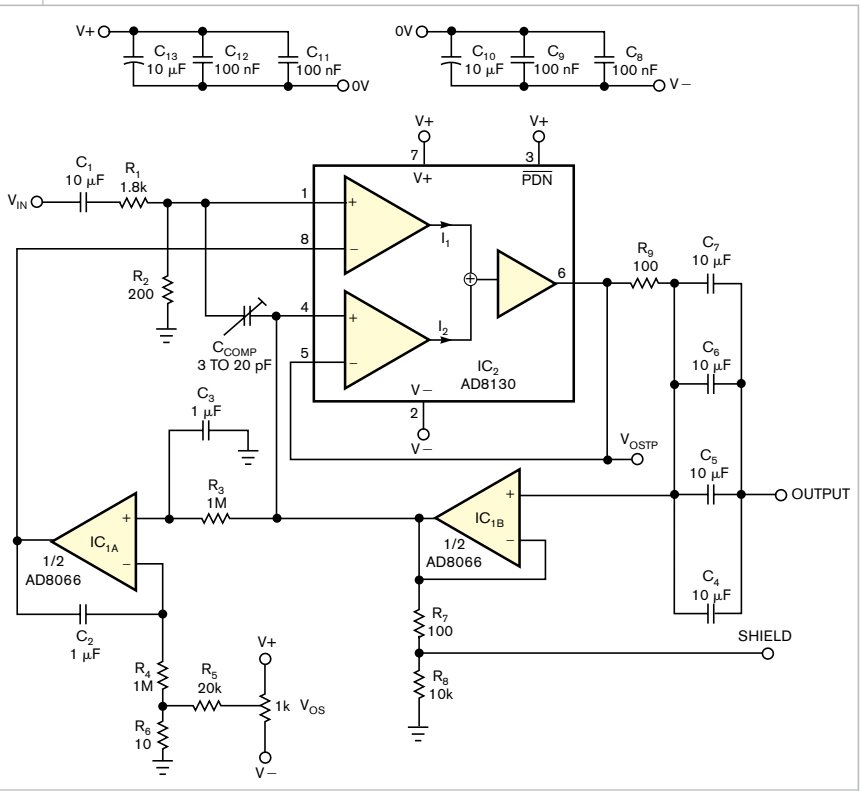

Figure 4 The complete circuit includes trimmer capacitor C_{COMP}, which compensates for stray capacitances in the circuit's packaged layout. Also, note wideband treatment of power-supply bypass capacitors.

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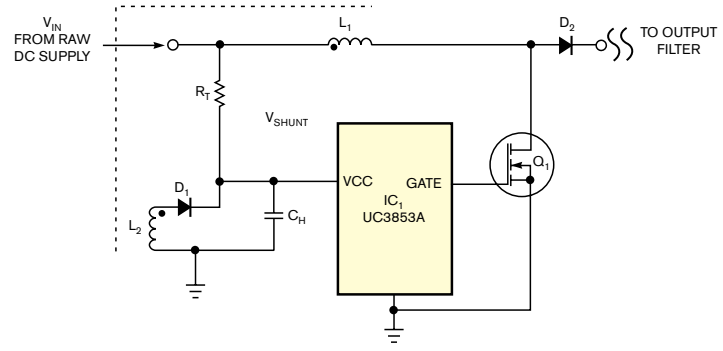
READERS SOLVE DESIGN PROBLEMS

Shunt regulator speeds power supply's start-up

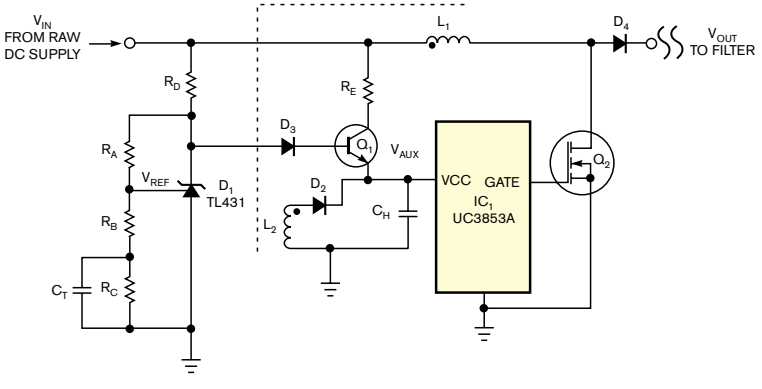
Michael O'Loughlin, Texas Instruments, Nashua, NH

In certain applications, design requirements may call upon a system's switched-mode power supply to more promptly deliver its output than would the garden-variety power supply. **Figure 1** shows such a supply's bootstrap, or start-up, circuit. In a switched-mode power supply's PFC (power-factor-corrected) preregulator, the circuit's PWM (pulse-width modulator), IC_1, draws its normal operating power from auxiliary winding L_1, wound on boost inductor L_2's magnetic core and diode D_1.



NOTE: DASHED LINE SHOWS MAGNETIC COUPLING BETWEEN WINDINGS L_1 AND L_2.

Figure 1 In a conventional switched-mode power supply's bootstrap circuit, trickle-charge resistor R_T and capacitor C_H supply start-up power to the pulse-width modulator and controller, IC_1.



NOTE: DASHED LINE SHOWS MAGNETIC COUPLING BETWEEN WINDINGS L_1 AND L_2.

Figure 2 In this augmented bootstrap circuit, transistor Q_1 delivers a robust initial pulse of current to capacitor C_H, ensuring faster start-up and power delivery.

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Resistor R_T and capacitor C_H form a trickle-charge circuit that supplies power for bootstrapping IC_1 into normal operation. In conventional designs, R_T comprises a high resistance that delivers just enough current to overcome the standby current and supply a trickle charge to holdup capacitor C_H, which stores enough energy to power the PWM circuit until the power converter begins operation. Under normal circumstances, the circuit's slow start-up response poses no problems.

When faster power-on response becomes important, you can reduce the bootstrap time by reconfiguring the start-up shunt regulator (**Figure 2**). Capacitor C_T; shunt-regulator IC D_1, a TL431; diode D_3; transistor Q_1; and resistors R_A through R_D form the bootstrap circuit. At power application, capacitor C_T holds no charge, and the series-pass regulator that Q_1 and D_1 form determines the voltage at the PWM's power input, V_{AUX}.

At turn-on, the V_{AUX} voltage reaches its peak voltage, V_{AUX_PEAK}, which the ratio of resistors R_A and R_B determines.

Capacitor C_T and resistor R_C conserve energy by setting the bootstrap circuit's turn-off time and voltage. Resistor R_D supplies bias current to D_1, the TL431 shunt-regulator IC, and resistor R_E keeps transistor Q_1 within its safe operating area by limiting its collector current.

To design the circuit, begin by selecting resistors R_A and R_B to establish the peak charging voltage, as the following equation shows:

$$\frac{V_{REF}}{R_B} = \frac{V_{AUX\_PEAK} + V_{D3} + V_{BE} - V_{REF}}{R_A + R_B},$$

where V_{REF} represents the TL431's internal reference voltage. Next, select resistor R_C to reduce the shunt-regulated voltage below the nominal V_{AUX} voltage, $V_{VAUX\_NOMINAL}$, which the auxiliary winding supplies:

$$RC_T = \frac{V_{REF} \times R_A + (V_{REF} - V_{AUX\_NOMINAL})R_B}{V_{AUX\_NOMINAL} - V_{REF} - 1V}.$$

Choose capacitor C_T's value to set the bootstrap time, T_{BOOT}, as follows:

$$C_T = \frac{2 \times T_{BOOT}}{R_C}.$$

As in **Figure 1**, diode D_2 and auxiliary winding L_2 provide normal operating power to IC_1. EDN

Build a USB-based GPIB controller

Boštjan Gla ar, Marko Jankovec, and Marko Topic,
Laboratory of Semiconductor Devices, Ljubljana, Slovenia

Contemporary research laboratories include a variety of instruments that connect using any of several interface methods to a PC for automating procedures and collecting data. Although different communication interfaces exist, the GPIB (general-purpose-interface bus) still enjoys wide popularity. The host PC must include a suitable GPIB controller—an internal interface card or an external device. Newer PC designs are phasing out traditional internal buses, such as PCI, ISA, and EISA, in favor of other standards, so using an external controller offers a more appropriate approach because external I/O ports, such as RS-232 and USB, tend to maintain backward compatibility.

This Design Idea covers the development of a GPIB controller, which turned out to be easier and cheaper than commercially available alternatives. The design uses easy-to-obtain components with a total component cost of approximately $50. For comparison, a commercial controller costs at least 10 times more: $500 to $1000. The USB 2.0-compliant controller, an external device, draws its operating power from the bus and provides plug-and-play operation and high-speed data transfer. In addition, a USB-controller design extends its applications to notebooks and other computers that lack available I/O slots. The controller resides on a double-sided pc board and fits into a 123×30×70-mm enclosure (**Figure 1**). To simplify controller use, the design uses National Instruments' (www.ni.com) LabView graphical programming language to develop the appropriate driver.

The design uses the FT245BM USB-controller IC from Future Technology Devices International Ltd (www.ftdichip.com), which features an 8-bit parallel connection to the host microcontroller and a virtual-communications port to the PC-interface side. The circuit operates at a full speed of 12 Mbps. Targeting use in GPIB applications, the 75160 and 75161 ICs drive GPIB I/O lines. An Atmel (www.atmel.com) AVR AT90S8515 microcontroller provides firmware-resident sequence control and in-circuit-programmable flash memory that simplifies firmware design and upgrades. The USB also can supply 5V of power at as much as 500 mA, which eliminates the requirement for an external power supply. The controller also supports the required low-power mode to reduce consumption to less than 1 mA.

The designers used the Protel (www.altium.com) schematic-capture and pc-board-layout software to design the circuit. They used a milling machine to produce the prototype pc board and partially assembled the board with a manual SMD placer. You can also use a commercial prototype pc-board-fabrication service to prepare a double-sided pc board with plated through holes and manually assemble the circuit. **Figure 2** shows an internal view, and **Figure 3** shows the completely assembled controller, which is easy and fast to build.

The controller communicates with the host computer through a logical serial interface that enables use of the

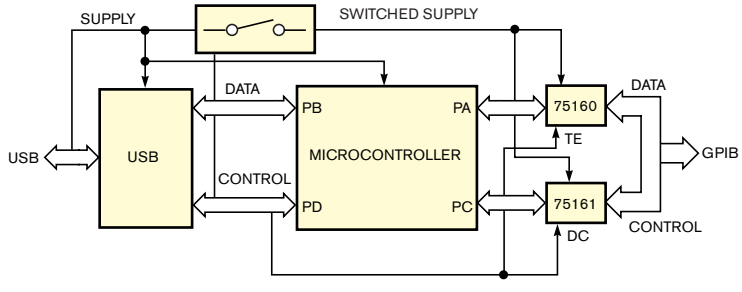

Figure 1 This USB-based GPIB controller requires only four ICs.

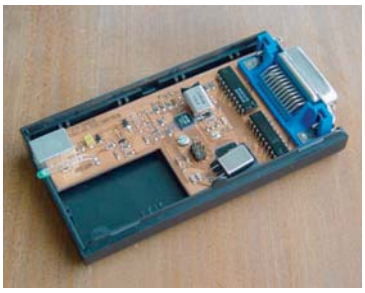

Figure 2 A top view of the controller's pc board shows the USB connector (left) and the GPIB connector (right).

Figure 3 The controller in its housing presents a profile that's not much larger than a GPIB cable connector.

controller with any programming language that supports serial-port communications. The LabView driver is compatible with LabView's built-in GPIB driver, thus simplifying adaptation of programs to the new interface. The driver is a collection of virtual instruments, which require only one more input—that is, a serial-port number—than a built-in GPIB driver.

Thanks to its open-source design, the controller provides a highly cost-effective approach to controlling GPIB instruments that's adaptable to many computational platforms. You can obtain the microcontroller's firmware; descriptions of the protocols; and all other necessary files, including a pc-board layout, at http://lsd.fe.uni-lj.si/gpib/. With that information, you can write a driver for whatever operating system or programming language you choose. In addition, the Web page includes firmware for the Atmel AVR microprocessor, a user's manual for the assembled interface, and additional notes on GPIB and LabView. To download a 1505-kbyte, zip-formatted archive containing the entire project, go to: http://lsd.fe.unilj.si/gpib/complete.zip.EDN

Programs calculate 1% and ratio-resistor pairs

Carl Rutschow, Upland, CA

If you perform analog-circuit design, you'll occasionally need to use a resistor with a nonstandard value to produce a particular gain, ratio, or attenuation factor. You can create resistors of unusual values by connecting two standard-value resistors of 1% tolerance in parallel. Because it is impossible to readily predict which resistor pairs will fall closest to the desired value, a computer program can help by calculating all combinations of standard 1% resistors to determine the best values for your application.

The Visual Basic, compiled, executable file Rratio2.exe checks all standard 1%-resistor values in a given range for a desired ratio, attenuation factor, or noninverting operational-amplifier gain (**Figure 1**). You can download the program from www.edn.com/051216di1. You select the calculation mode via the program's window buttons. As an option, you can choose whether the program displays all possible values or only the values closest to the target value.

Using standard 1%-resistor values, a second program, RPar2a.exe, also available at www.edn.com/051216di1, checks and displays all appropriate combinations that generate a desired parallel resistor's value. The program generally calculates several parallel combination values that fall well within 0.1% of the desired value. By comparison, a single 1% resistor's nominal value may differ by as much as 1.45% from the desired value. Note that, for both programs, the calculated resistance values depend on the paired resistors' tolerances.EDN

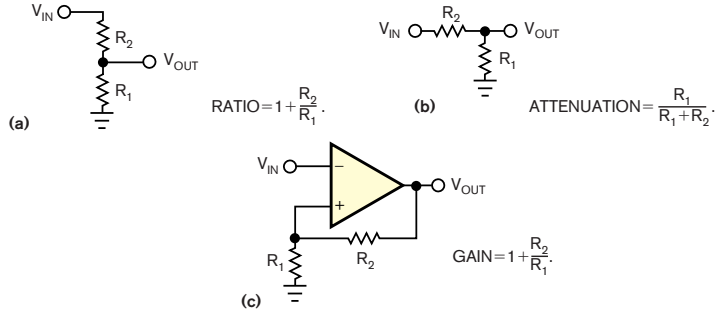

Figure 1 You can use the program Rratio2.exe to calculate ratio (a), attenuation (b), or gain (c).

Simplify worst-case PSpice simulations with customized measurement expressions

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During IC design, worst-case simulations help designers account for variations in characteristics of PNP and NPN transistors and base and polysilicon resistors. These four classes of devices alone produce more than 16 combinations of simulation conditions. To accommodate temperature variations, each combination undergoes simulation at −40, +27 (room temperature), and +125°C, producing at least 48 series of data to analyze when simulations are complete. To help an IC designer evaluate simulated waveforms' characteristics, PSpice provides a library of ready-to-use, predefined measurements, including bandwidth, gain/phase margins, and more. PSpice also allows a designer to use predefined YatX and XatNthY measurements to measure a waveform's y value at a given x value—usually, time—and to find an x value that corresponds to the nth instance of a given y value (**Reference 1**).

However, when a designer must measure the value of Waveform 1 when Waveform 2 crosses a certain y value, predefined measurements do not apply because, unlike many programming languages, PSpice allows no embedment. This Design Idea describes how to create a customized PSpice measurement expression that solves the problem. As **Listing 1** shows, the measurement expression itself is straightforward. Line 1 finds the X_value (x1) when Trace 1 crosses the y1_value for the nth positive slope. Line 2, denoted by braces { } at the bottom of the **listing**, searches for the value of Trace 2 (y2) at x1. Similarly, **Listing 2** shows how a designer can create a measurement expression to find a y2 value when Trace 1 crosses a y1_value for the nth negative slope or when Trace 1 crosses a given percentage of its full y-axis range.

Figure 1 shows a simulation example in which the input and the output voltages represent a comparator's input and output, respectively. When the input voltage is greater than the positive threshold voltage, then the output voltage is high; when the input voltage is less than the negative threshold voltage, the output voltage is low. Using customized measurement expressions, a designer can easily find the rising and falling thresholds and the comparator's hysteresis voltage for all conditions immediately after the probe data becomes available. If any condition exists in which the threshold doesn't meet the design specification, the designer can then go directly to that condition and spend time on further analysis.

The simulation example describes an input-voltage monitor comprising a comparator that acts as a "power-good" block in a power-management IC. When the input voltage rises above a 13V enable threshold, the output voltage goes high and enables other circuit blocks. When the input voltage falls below a 10V disable threshold, the output voltage goes low and disables other circuits. The difference between the enable and the disable thresholds—that is, 3V—defines the hysteresis voltage. A worst-case simulation of the circuit must account for variations in characteristics of NPN and PNP transistors, base resistors, and polysilicon resistors in the circuit. Each device's characteristics can fall at either the low or the high end of the process specifications and thus produce 16 combinations.

The toolbar lists a few of the 16 possible combinations. For example, LLLL refers to the case in which characteristics of NPN and PNP transistors and base and polysilicon resistors all fall at their low values. In addition, one pass of the simulation uses nominal values; that is, the components' specifications fall in the centers of their nominal characteristics. For each combination, PSpice simulates the circuit's behavior at low, room, and high temperatures, respectively, producing 51 data traces for the block's input and output voltages for a total of 102 displayed traces. After PSpice assembles the data, the circuit's designer must extract the actual threshold voltages for each condition for comparison with the circuit's specifications. Given the large number of displayed traces, using the display's cursor to measure each threshold consumes much of a designer's time. Using a customized PSpice measurement extracts the threshold voltages in a fraction of the time and presents the data in tabular form. The table immediately below the waveform plot contains simulation results for all 51 traces. Columns 1, 2, and 3 list results for nominal characteris-

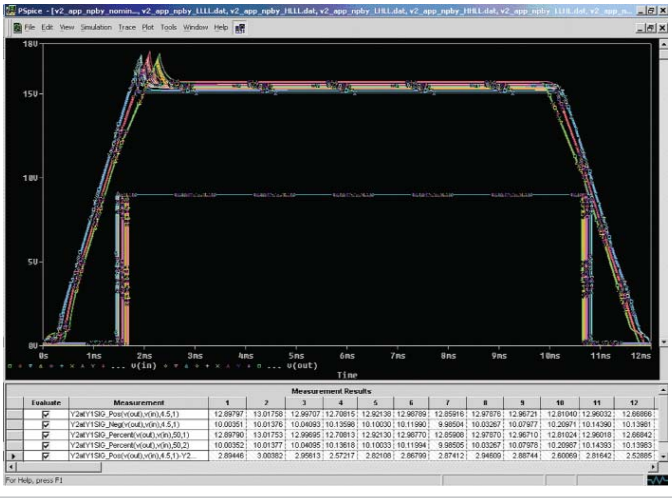
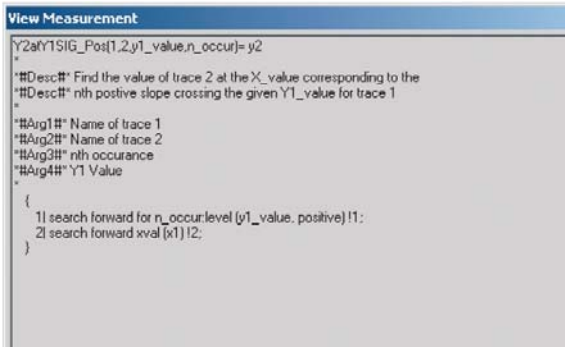


Figure 1 On-screen waveforms represent inputs and outputs for multiple simulation passes.

LISTING 1 MEASUREMENT EXPRESSION FOR x1



LISTING 2 MEASUREMENT EXPRESSION FOR y2

```
Y2atY1SIG_Neg(1,2,y1_value,n_occur)=y2
  {
    1| search forward for n_occur:level (y1_value, negative) !1;
    2| search forward Xvalue (x1) !2;
  }

Y2atY1SIG_Percent(1,2,y1_pct,n_occur)= y2
  {
    1| search forward for n_occur:level (y1_pct%  ) !1;
    2| search forward xval (x1) !2;
  }
```

tics, and columns 4, 5, and 6 list results for low, room, and high temperatures when all devices' specifications reside at their lower extremes.

Row 1 of the table displays the measurement expression and results for the enable-voltage threshold. When the output voltage first crosses 4.5V (one-half the simulated circuit's 9V power-supply bus voltage) on the positive slope, the simulation records the value of the input voltage as the enable-threshold voltage, and row 2 measures the disable-threshold voltage. Rows 3 and 4 measure the enable- and disable-threshold voltages by another method: When the output voltage passes 50% of the full-scale value for the first and second times, PSpice measures the value of the input voltage. Row 5 calculates the hysteresis voltage. EDN

REFERENCE

1 *PSpice User's Guide*, Cadence Design Systems Inc, June 2003, www.cadence.com.

Tiny twisted-pair transmission line solves test-fixture woes

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Engineers often construct test fixtures that include high-speed differential signals. Although miniature coaxial cable is widely available, there's no commercial off-the-shelf source for small-gauge twisted-pair cable that's suitable for differential signals. Although Category 5 Ethernet cable contains four twisted pairs, it's too large for crowded fixtures and for attachment to the Amp Z-Pack connectors some fixtures require. Many engineers are unaware that they can twist together two lengths of AWG #30 Kynar-insulated wire—garden-variety wire-wrap and prototype cut-and-jumper wire—to make a 102Ω differential-transmission line. If you use Kynar's dielectric constant and the insulation's thickness to compute its properties, the line's calculated differential impedance works out to 110Ω. In practice, differential TDR (time-domain-reflectometer) measurements show that the line's actual impedance consistently measures 102Ω—only 2% away from the target impedance and thus close enough for most practical purposes.

To make your own twisted pair, start with a long AWG #30 Kynar-insulated wire and fold it in half. Enlist a coworker to hold the cable's closed end by slipping the loop around a screwdriver's blade. If you're working alone, slip the loop around a doorknob. Tightly twist the two wires' free ends together and insert the twisted ends into the chuck of a Dremel (www.dremel.com) rotary tool. Tighten the chuck and hold the Dremel tool so that the wires are stretched tightly, are of the same length, and lie parallel with each other.

Apply a slight amount of tension to the wires and start the tool. As the wires twist together, the pair shortens and pulls the tool's operator toward the loop support. A variable-speed Dremel tool works best when you operate it at its slowest setting. If you have only a fixed-speed Dremel tool, avoid overtwisting the wires by preparing a length of 10 to 20 ft of cable at a time. The extra length allows time to switch the tool off and avoid overtwisting the wires. Cut off and discard the cable's nonuniformly twisted end sections.

The amount of twist in the wires is not critical, but the wires should be firmly twisted together. Using approximately eight to 10 twists/in. works well. To count the twists, hold a portion of the cable against a ruler or measuring scale under a magnifier and count 16 to 20 "bumps," or half-twists, per inch. Using too many twists per inch uses excess wire and increases losses and propagation delay. For the lengths in a test fixture, losses are insignificant except at extremely high frequencies.

You can also use a variable-speed hand drill with a 1/4- or 3/8-in. chuck to twist the wires, but you need to fold the wires' free ends several times and wrap them in duct tape to ensure a snug fit in the drill's chuck. When using any power tool, wear safety glasses or other eye protection during the procedure. EDN