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CMOS inverters convert RF to digital signal

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Applications ranging from frequency counting and synthesis to sensor signal conditioning require conversion of RF signals to digital-logic levels. In such situations, designers typically use a high-speed voltage comparator to perform the RF-to-digital conversion. Due to their high gain, voltage comparators typically exhibit good sensitivity but also present some drawbacks. High-speed comparators are expensive, difficult to find off the shelf, and prone to rapid obsolescence.

For frequencies as high as 180 MHz, the circuit in **Figure 1** offers an attractive approach. The IC in the design, a 74LVCU04 very-high-speed CMOS hex inverter, is available off the shelf and from many sources. Furthermore, many applications may already include three unused inverters. A single inverter, IC_{1A}, operating as a linear preamplifier, forms the converter's input stage. Biasing resistor R_3 forces the inverter into its linear region by equalizing its input and output voltages at one-half of the power-supply voltage, $V_{O1}=V_{I1}=(V_{DD}/2)$. Because the ac gain of a very-high-speed CMOS inverter is relatively low at RF $(V_{O1}/V_{I1})\approx 7$, additional gain stages follow the preamplifier. One self-evident approach—a cascade of additional inverters—presents poor stability at low frequencies and at dc when no RF source is present.

The circuit in **Figure 1** eliminates this drawback thanks to a topology based on a Schmitt trigger and amplifier circuit, IC_{1B} and IC_{1C}, that includes a frequency-dependent positive-feedback network comprising R_1, R_2, C_{D1}, and C_{D2}. Depending on the input frequency, the network exhibits two behaviors: At high frequencies, the decoupling-capacitor pair, C_{DC1} and C_{DC2}, short-circuits feedback resistor R_1, canceling the time constant introduced by the positive-feedback network, R_1 and R_2, and the input capacitance of inverter IC_{1B}. Consequently, at high frequencies, the three inverters, IC_{1A}, IC_{1B}, and IC_{1C}, behave as three cascaded, high-speed amplifiers that allow the best performance in input-signal bandwidth. At dc and low frequencies, the influence of coupling-capacitor pairs C_{D1} and C_{D2} is negligible, and inverters IC_{1B} and IC_{1C} and the positive-feedback network, R_1 and R_2, act as a Schmitt-trigger circuit. The choice of the high- and low-threshold voltages, V_{TH} and V_{TL}, at the Schmitt

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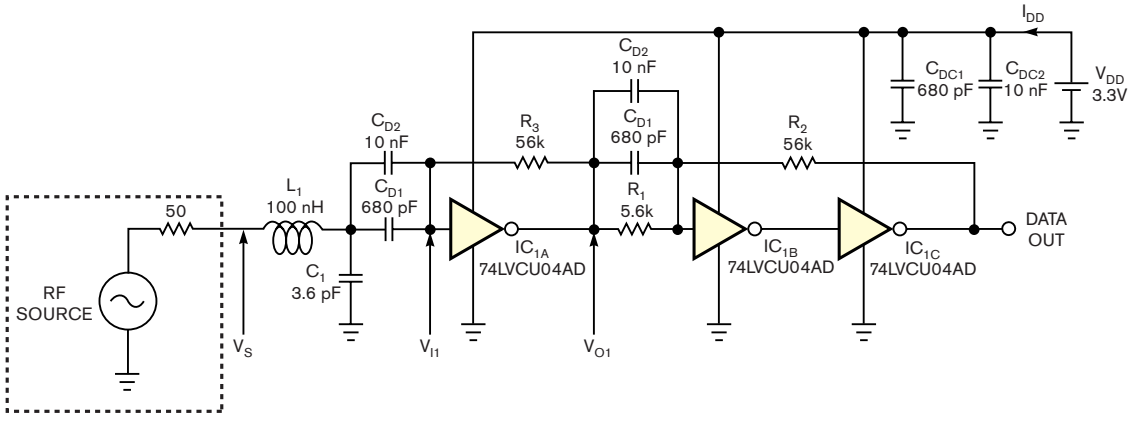

NOTE:
ALL COMPONENTS ARE SURFACE-MOUNTED DEVICES.

Figure 1 Three high-speed CMOS inverters and a few passive components form an RF-to-logic converter.

trigger's input, V_{OI}, stems from a compromise between input sensitivity at V_S and ensuring unconditional stability of the comparator's output. **Equations 1** and **2** set the high and low threshold voltages, respectively:

$$V_{TH} = \frac{V_{DD}}{2}\left(1+\frac{R_1}{R_2}\right) \approx 1.8V. \quad (1)$$

$$V_{TL} = \frac{V_{DD}}{2}\left(1-\frac{R_1}{R_2}\right) \approx 1.5V. \quad (2)$$

To counteract a roll-off of sensitivity at higher frequencies, add a low-Q impedance-matching network comprising L_1 and C_1 at the comparator's input. Given the design objective of obtaining acceptable sensitivity at frequencies as high as 160 MHz, the network matches the 50Ω RF source and IC_{1A}'s input impedance, Z_{I1}, at 150 MHz. Unfortunately, manufacturers of digital ICs typically do not specify logic devices' input impedances. When designing the matching network, the first task involves using an Agilent (www.agilent.com) vector-network analyzer to measure the first inverter's input scattering parameter, S_{11}, at IC_{1A}'s input, V_{I1}. **Figure 2** shows a Smith-chart plot of the inverter's S_{11} parameter.

Knowing that

$$S_{11} = \frac{Z_{I1}-Z_C}{Z_{I1}+Z_C}, \quad (3)$$

with Z_C=50Ω, you can use the data in **Figure 2** to extract the first inverter's input impedance at the frequency of interest. At 150 MHz, this yields Z_{I1}= 106.1Ω − j 116.7Ω (at Marker 4 in **Figure 2**). To determine values for the matching network's components, you can use any of several software tools (**references 1** and **2**). If you are unfamiliar with Smith-chart computations, you can also proceed analytically with the following method:

1. Use series-to-parallel transformation formulas (**equations 4** and **5**) to transform the first inverter's input impedance into a parallel form:

$$R_P = \frac{R_S^2 + X_S^2}{R_S}. \quad (4)$$

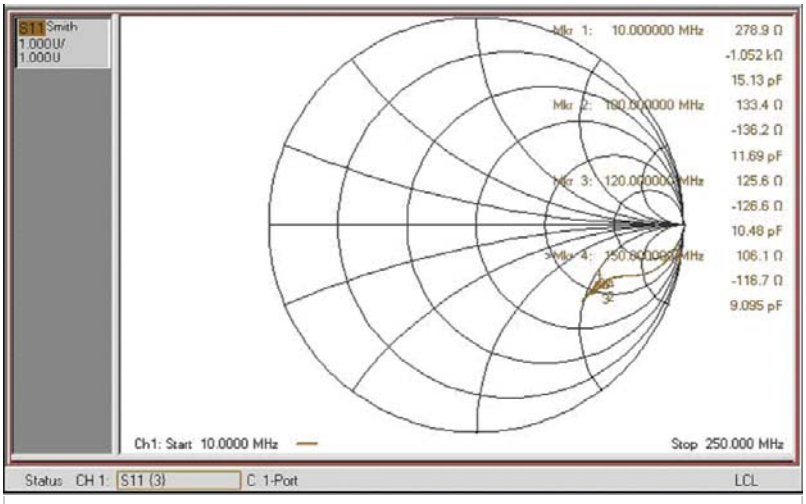

Figure 2 An Agilent N3382A vector-network analyzer obtained this S-parameter plot, which shows S_{11} measured at the first inverter's input for a source power level of −6 dBm.

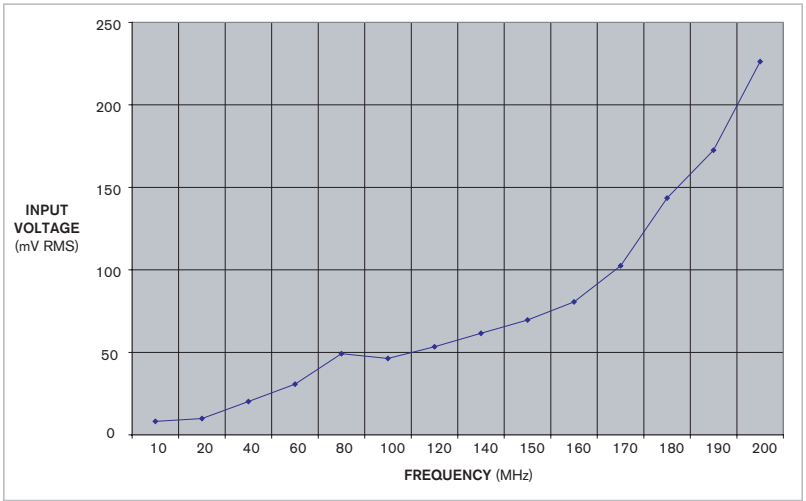

Figure 3 An input-level-versus-frequency plot of the RF-to-digital comparator measured from the RF source's reference plane to a clean logic output reveals less-than-100-mV sensitivity at 160 MHz and usable output to 200 MHz.

$$X_P = \frac{R_S^2 + X_S^2}{X_S}. \quad (5)$$

Applying these formulas at 150 MHz yields: R_p=233Ω, and X_p=−213Ω. (At 150 MHz, X_p represents an input capacitance, C_p=5 pF.)

2. Compute an initial version of the matching network to perform a match between the real part of the first inverter's input impedance, R_p, and the 50Ω RF source. Solving **equations 6** and **7** yields values for the matching network's elements (**Reference 3**):

$$L_1 = \frac{R_S}{\omega}\sqrt{\frac{R_P}{R_S}-1}. \quad (6)$$

$$C_1 + C_P = \frac{1}{R_P\omega}\sqrt{\frac{R_P}{R_S}-1}. \quad (7)$$

Applying these formulas at 150 MHz yields $L_1 \approx 100$ nH, and $C_1 + C_P \approx 8.7$ pF.

3. Subtract the inverter's input capacitance, $C_P = 5$ pF, from **Equation 7** to calculate a value for C_1:

$$C_1 = \frac{1}{R_P \omega \sqrt{\frac{R_P}{R_S} - 1}} - C_P \approx 3.7 \text{ pF}. \quad (8)$$

To build the circuit, use standard component values that fall closest to the computed values: $L_1 = 100$ nH, and $C_1 = 3.6$ pF. As the plot of input frequency versus sensitivity in **Figure 3** shows, the circuit's increased sensitivity for 100- to 170-MHz frequencies clearly demonstrates the impedance-matching network's effectiveness. You can optimize the circuit's sensitivity in any other frequency band of interest by applying this method at the chosen frequency. The RF-to-digital-logic converter's power consumption does not change significantly for input signals of 10 to 180 MHz. Under worst-case conditions, the current drain does not exceed 58 mA for a supply voltage of 3.3V. EDN

REFERENCES

1. Smith tool, Ansoft Corp, www.ansoft.com.
2. *Ansoft Designer: Student Version*, Ansoft Corp, www.ansoft.com.
3. Bowick, Chris, *RF Circuit Design*, HW Sams & Co, Indianapolis, IN, 1988.

Instrumentation amplifier extends DSO

Bob Perrin, Sacramento, CA

To determine the specifications of a solar-generating plant, I needed to accurately measure the load current a product consumed. The product switched several internal devices on and off during an interval of several seconds. An ammeter showed that the current transitions occurred too quickly for visual logging, and my managers had requested an oscilloscope photo of the current waveform's peaks. I rolled out our company's cart-mounted DSO (digital-storage oscilloscope), inserted a low-value resistor in series with the product's positive-power-supply input, and attempted to make a differential-voltage measurement (Channel A minus Channel B) across the current-sampling resistor.

Unfortunately, RF noise from a local FM-broadcast station swamped the small-load-induced fluctuations in the voltage developed across the sampling resistor, and increasing its resistance

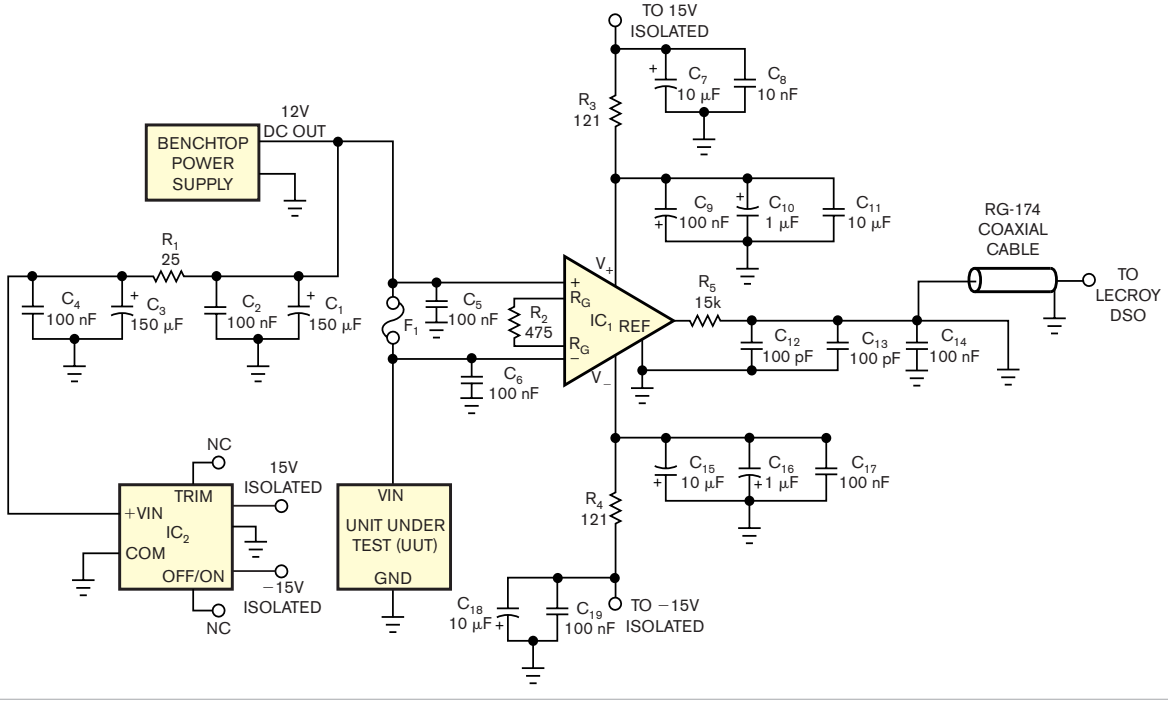

Figure 1 Improve your oscilloscope's performance in high-RF-noise environments by adding an instrumentation-amplifier front end. For best results, package the circuitry in a metal enclosure.

introduced an unwanted voltage drop on the product's power-supply rail. Finally, the 12V supply rail introduced a voltage offset that limited the oscilloscope's ability to accurately resolve the small differential signal that I was attempting to measure. I disconnected the oscilloscope's ac ground to "float" the scope with respect to the sampling resistor, but the RF noise visible on the trace increased significantly. I briefly considered using an older analog (nonstorage) scope, but the DSO's storage feature would allow me to capture and print the waveforms required for my report.

In frustration, I scoured the workbench for stray parts and assembled a circuit that solved the problem. By chance, the parts collection included an instrumentation amplifier, IC_1, which does an excellent job of extracting small signals from high-frequency background noise. The amplifier's inherently slow response attenuates RF noise but doesn't affect amplification of lower frequency signals. Adding RC lowpass filters to the amplifier's inputs and output further attenuates lower frequency noise induced by nearby switched-mode power supplies and digital logic or microprocessors.

Normally, I avoid using noise-emitting dc/dc converters as power supplies for analog circuits. However, in this case, IC_2, a dc/dc converter, provided an expedient and technically sound approach (**Figure 1**). In general, dc/dc converters produce more noise as their load currents increase, but, in this circuit, the sole load comprises the instrumentation amplifier that draws only a few milliamperes. Adding a few filtering components provided additional noise suppression.

Under normal operation, the current that the product draws fluctuates from approximately 300 to 800 mA. To minimize the voltage drop induced in the power-supply loop, I used a 5×20-mm, 10A, 250V fuse, F_1, as a current-sampling resistor. Voltage drop across the fuse is approximately 1 mV per 100 mA of current, and operating the fuse at a small fraction of its nominal rating avoids introducing nonlinearities in the measurement.

With a 475Ω gain-setting resistor, R_2, the instrumentation amplifier, an Analog Devices (www.analog.com) AD620, provides a gain of 105V/V and delivers an output of approximately 1V, which corresponds to 1A of current flowing through the shunt. Capacitors C_{12} and C_{13} provide low-impedance paths for high-frequency noise. EDN

Virtual instrument determines magnetic core's B-H-loop characteristics

Michael Nasab, Circuit Mentor, Boulder Creek, CA

To design an inductive component that contains a magnetic-core material, an engineer must accurately measure the material's characteristics. A magnetic core's dynamic hysteresis loop, or "B-H curve," contains valuable information about core losses and other magnetic parameters. Unfortunately, commercially available magnetic-loop-analysis instruments are expensive and thus impractical for small-scale research labs and manufacturers. This Design Idea describes a virtual instrument that uses a desktop or notebook computer with an analog data-acquisition card and National Instruments' (www.ni.com) LabView software (Version 7.1 or above). In operation, the software extracts B-H-loop information, core losses, and other magnetic parameters at a reasonable cost per measurement.

Figure 1 shows the test fixture for a magnetic-core-based device. The device, T_1, comprises a sample of core material and two windings with equal numbers of turns. A precision current-sensing resistor, R_1, samples the excitation current that induces a magnetic field in the core. The voltage drop across R_1 is proportional to the excitation current and the magnetic field, H. A network comprising resistor R_2 and capacitor C_1 integrates the voltage induced in the secondary winding. The voltage across C_1 is directly proportional to the flux density, B, in the core. In practice, R_2's value should be much larger than capacitor C_1's impedance at the operating frequency. (Textbook descriptions of the circuit suggest a ratio of 100-to-1.)

Components' tolerances and characteristics affect measurement accuracy. Use a noninductive, 1Ω, 1%-tolerance resistor of appropriate wattage rating for R_1, and select a low-leakage, low-dielectric-absorption, polyester- or polypropylene-film capacitor with tight tolerance for C_1. To acquire and view the data, you can use a dedicated virtual instrument using a National Instruments PCI-6024E data-acquisition card and LabView. The software features NI's Express VI (virtual-instrument) technology that greatly simplifies the creation of user-designed data-acquisition and -manipulation features. This application uses only two

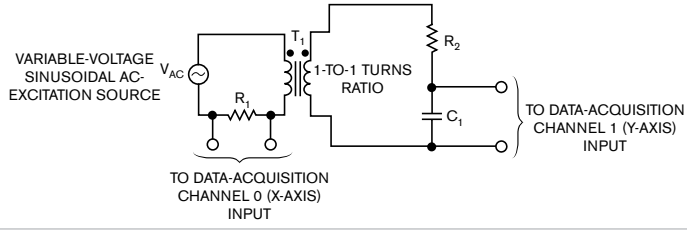

Figure 1 The test fixture for a basic hysteresis-loop analyzer requires few components.

data-acquisition analog-input channels: Channel 0 acquires magnetic-field readings (H) for display on an x-y chart's x axis in units of ampere-turns per meter, and Channel 1 captures flux density (B) in tesla units for the y-axis display.

At low frequencies, the core's hysteresis losses predominate, whereas eddy-current losses become more apparent at higher frequencies. A wattmeter-style algorithm calculates core losses, but you can easily substitute your own mathematical expression into the VI block diagram's formula node. LabView also can save the data and export results in Microsoft's (www.microsoft.com) Excel-spreadsheet format or into other programs for further analysis.

You can use another of the data-acquisition card's eight differential analog-input channels to determine inductance. To do so, measure the voltage across the device's primary winding and calculate its rms value. The ratio of the voltage to the rms current as measured through R_1 determines the magnitude of the winding's scalar impedance, X_L. Then, you can calculate the inductance from the following equation: $L=X_L/2\pi f$, where f denotes the frequency of the applied excitation voltage.

Figure 2 shows a hysteresis curve for a 3B7-mixture ferrite-pot core prepared with 100-turn primary and secondary windings and measured at 60 Hz. For comparison, **Figure 3** displays the 60-Hz hysteresis curve for a 100W power transformer wound on a toroidal core composed of grain-oriented steel. The toroidal core's wider loop indicates greater hysteresis, a characteristic that saturable-core power inverters exploit. To apply 60-Hz excitation, you can drive the device's primary winding from a stepdown (isolation) transformer powered by an adjustable-output autotransformer, such as a GenRad (www.ietlabs.com) Variac. While observing the B-H curve display, gradually increase the primary voltage until the flattening of the hysteresis loop's upper and lower portions indicates core saturation. No calibration is necessary if you use precision. However, when evaluating core materials, you may need to experiment with different numbers of turns to obtain the windings' ampere-turns value for optimum results.

For tests at 60 Hz, use a 267-kΩ, 1%-tolerance resistor for R_2 and a 1-μF polyester-dielectric capacitor for C_1 in the integrator network. Depending on the number of turns and the current necessary to obtain a usable output voltage, a few volts of ac excitation is usually sufficient to run the test. For core measurements at higher frequencies, use a signal generator connected to a power amplifier and alter the RC integrator's component values for proper operation at the frequency of interest. Although the application does not use an analog output from the data-acquisition card, this output can serve as a sinusoidal-signal source for the power amplifier.

Review the electrical specifications of the card you plan to use and avoid exceeding the card's peak-to-peak differential- and common-mode input voltages. If the excitation voltage approaches or exceeds the card's ratings, add a 10-to-1 resistive-voltage divider to limit the applied voltage and compensate for the attenuator's losses by adding a factor-of-10 gain multiplier in the software.

You can download a copy of the VI that this Design Idea describes from www.circuitmentor.com/services.htm. You can also obtain a trial version of LabView from NI's Web site at www.ni.com. EDN

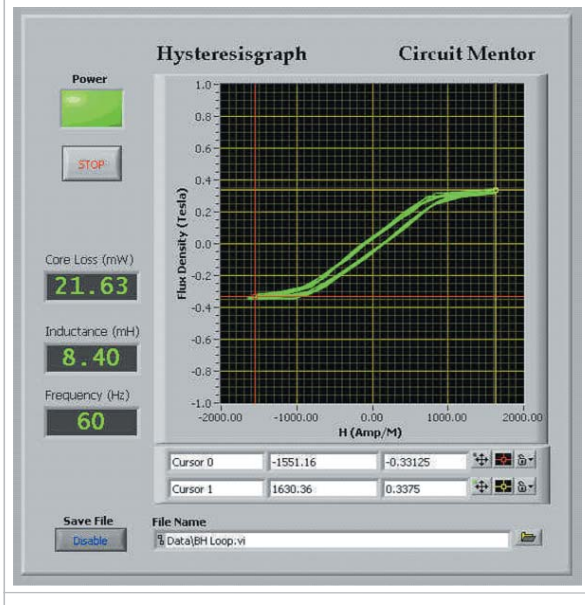

Figure 2 The virtual instrument's display shows a 3B7-mixture ferrite-pot core's B-H loop.

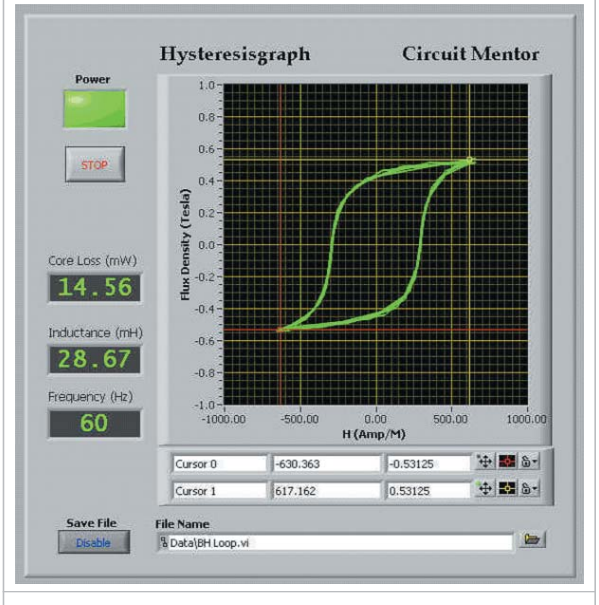

Figure 3 This grain-oriented-steel toroidal core's B-H loop exhibits saturation at a lower excitation value than the core in Figure 2.

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Programmable analog circuits yield single-chip sinusoidal oscillators

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Programmable-logic devices provide a popular method of implementing complex functions in digital designs. Although manufacturers don't yet offer analog circuits whose complexity compares to VLSI digital circuits, field-programmable analog circuits are enjoying extensive use in signal-conditioning and filtering applications. Based on CMOS-operational-transconductance and switched-capacitor amplifiers, these devices offer a convenient approach to relatively complex design problems. Lattice Semiconductor's (www.latticesemi.com) ispPAC10 in-system-programmable analog circuit and its accompanying PAC Designer software offer a convenient method of circuit design and verification (**Reference 1**). This Design Idea presents two simple sinusoidal oscillators based on the ispPAC10.

Resistors within the ispPAC10 are fixed at a nominal 250 kΩ, and all capacitors are user-selectable from 1.07 to 61.59 pF. **Figure 1** shows an ispPAC10 with its internal blocks 1, 2, and 4 connected as a cascade of three first-order lowpass filters to form a classic phase-shift RC oscillator. Altering the capacitors' values produces oscillation frequencies over a range of 18 to 130 kHz. Each PAC block's gain is fixed at a factor of two to obtain a loop gain of −8, which Barkhausen's condition for oscillation requires (**Reference 2**). Configured from Block 3, a first-order lowpass filter reduces the THD (total harmonic distortion) on the oscillator's output. The values of capacitors in Block 3 are optimized for filtering performance and thus differ from those of the phase-shift stages.

The circuit in **Figure 2** describes a two-integrator loop that forms a classic quadrature-RC oscillator. The circuit's oscillation frequency spans 12 to 126 kHz and depends on the time con-

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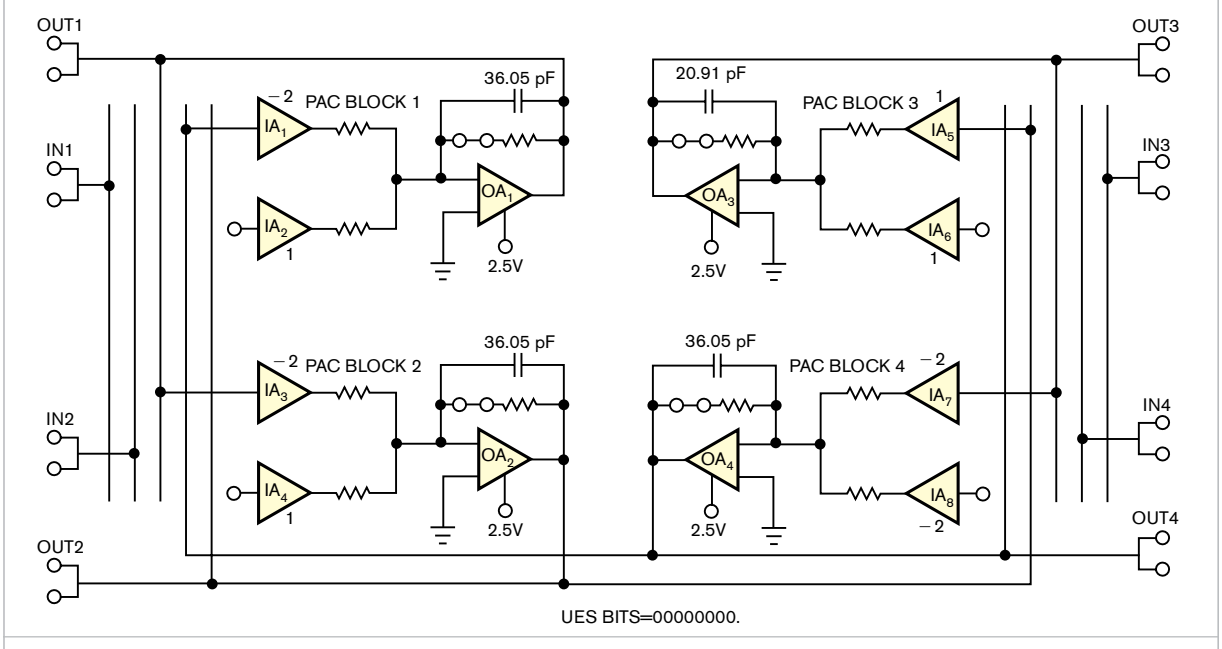

Figure 1 Based on a Lattice Semiconductor ispPAC10 programmable analog circuit, this phase-shift sine-wave oscillator and lowpass filter require no external components. The values are for a 30.4-kHz oscillator.

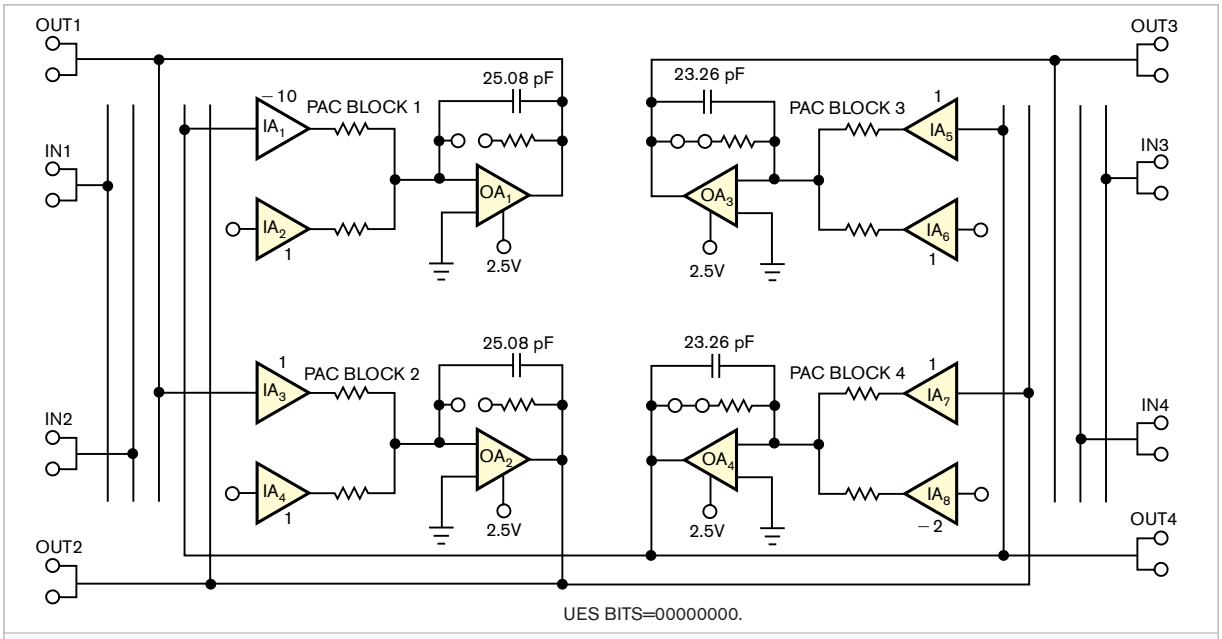

Figure 2 Cascaded dual integrators implement a quadrature sine-wave oscillator, with blocks 3 and 4 forming a low-pass filter. Again, the circuit design uses no external components. The values shown are for a 27.2-kHz oscillator.

stants of the integrators that blocks 1 and 2 form. In theory, each integrator's gain should have an absolute value of unity, but, in practice, ispPAC allows specification only of inverting integrators, and producing a stable sinusoidal signal requires a gain of at least −4 in Block 1. The circuit uses a gain of −10. Two additional blocks of the ispPAC10 device form a second-order lowpass filter that decreases the output's THD. In both oscillator circuits, you can alter the lowpass filters' gain so that the circuit's outputs deliver specific voltages, such as 1V p-p, at all frequencies.

Tables 1 and **2**, respectively, contain summaries of the phase-shift and quadrature oscillators' components and output characteristics. C_N refers to the value of the capacitor used in the

TABLE 1 PHASE-SHIFT OSCILLATOR

C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	f_0 (kHz)	Δf (kHz) at −20 dB	THD (dB)
5.46	5.46	5.06	5.46	130.1	6	−25
6.92	6.92	5.92	6.92	115.4	6	−30
7.77	7.77	6.92	7.77	109.9	6	−30
9.19	9.19	6.92	9.19	97.8	2.5	−32
14.62	14.62	9.19	14.62	67.9	2.5	−39
20.91	20.91	12.78	20.91	50.1	2.5	−40
36.05	36.05	20.91	36.05	30.4	1.2	−40
61.59	61.59	35.25	61.59	17.7	0.6	−41

TABLE 2 QUADRATURE OSCILLATOR

C_1 (pF)	C_2 (pF)	C_3 (pF)	C_4 (pF)	f_0 (kHz)	Δf (kHz) at −20 dB	THD (dB)
1.07	1.07	5.06	5.06	125.9	6	−27
3.56	3.56	5.92	5.92	105.1	6	−25
5.92	5.92	7.77	7.77	80.4	2.5	−30
7.77	7.77	9.62	9.62	66.3	2.5	−34
14.22	14.22	15.45	15.45	41.7	2.5	−40
25.08	25.08	23.26	23.26	27.2	1.2	−40
40.08	40.08	26.29	26.29	18.6	1.2	−42
50.01	50.01	35.25	35.25	15	0.6	−42
61.59	61.59	40.98	40.98	12.3	0.6	−41

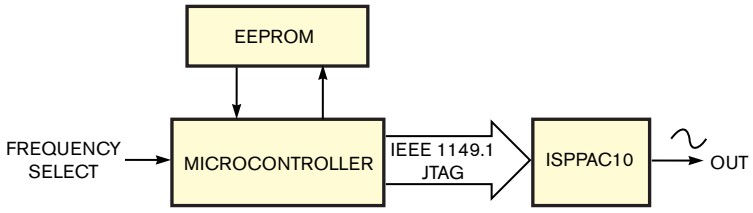

Figure 3 Either ispPAC10 circuit's implementation can serve as a foundation for a programmable oscillator by adding a microcontroller and nonvolatile storage.

nth PAC block for oscillation at frequency f_0. The design uses a Tektronix TDS1002 digital oscilloscope's FFT function to measure THD and the spectral line width of each output frequency at a level of −20 dB with respect to the central frequency, f_0.

Figure 3 illustrates the application of a microcontroller to dynamically reconfigure an ispPAC-based oscillator for specific frequencies. The nonvolatile memory stores frequency-specific capacitance and gain values for each of the ispPAC10's circuit blocks. Data transfers occur using the IEEE 1149.1 JTAG-standard protocol through the ispPAC10's serial test-access-port interface. EDN

REFERENCES

1 PAC Designer software, www.latticesemi.com.
2 http://jlnlabs.imars.com/spgen/barkhausen.htm.

Enhanced, three-phase VCO features ground-referenced outputs

Harry Bissell Jr, Welding Technology Corp, Farmington Hills, MI

Three-phase VCOs (voltage-controlled oscillators) see service in many applications, including power inverters and in electronic-music synthesis as control and modulation sources. A previous Design Idea describes a basis for a simple, three-phase VCO (**Reference 1**). However, adding a few components enhances the circuit's performance. The original circuit delivers an output of only 600 mV p-p and cannot tolerate substantial loading, especially at low operating frequencies at which the circuit draws the least operating current. Providing ac coupling for the output signals doesn't work well at low frequencies and worsens the loading problem. Finally, the circuit's dc operating point varies with frequency.

The circuit in **Figure 1** elegantly overcomes these limitations. The original circuit uses three of six of a CD4069UB hex inverter's subcircuits. One of the spares, IC_{1A}, senses the complete circuit's dc operating point. Resistor R_2 provides linear feedback around IC_{1A}, forcing the input voltage at Pin 9 to equal the output transition threshold voltage over a range of operating currents. In other words, the voltage is proportional to the average dc value of the sinusoidal output waveforms.

A voltage follower, IC_{2A}, buffers the averaged voltage at IC_{1A}'s Pin 8. The remaining sections of IC_2 buffer the oscillator's three outputs, equalizing the loading on the oscillator and providing low-impedance drive to three differential amplifiers: IC_{3A}, IC_{3B}, and IC_{3C}. The differential stages subtract the dc offset voltage from IC_{2A} from the buffered three-phase outputs. You can alter the voltage gain of the three differential amplifiers from its nominal factor of five to suit other applications.

Zener diode D_1 limits the voltage to 10V at IC_1's Pin 14. At low frequencies and currents, the oscillator's dc operating point can easily exceed the linear range of IC_2's inputs. You can use rail-to-rail-capable operational amplifiers instead of LM324-family devices. Note that the inputs of IC_1's remaining unused inverters connect to IC_1's Pin 7 and not to circuit ground per normal practice.

Adding an exponential current source eases the task of adjusting the circuit over a wide frequency range. Transistors Q_1 and Q_2 and their associated components form a simple exponential voltage-to-current converter. For best results, the base-emitter voltages of Q_1 and Q_2 should match at the circuit's nominal operating current—100 μA—and you should thermally couple both transistors. If your application requires precise thermal tracking, replace R_6 with a 2-kΩ temperature-compensating resistor with a coefficient of 3500 ppm/°C, such as a Tel Labs Q81, which is available from such companies as Precision Resistor (www.precisionresistor.com). Place this resistor in thermal contact with Q_1 and Q_2. Temperature-compensating resistors are also available from Micro-Ohm (www.micro-ohm.com), Vishay (www.vishay.com), Ultronix (www.ultronix.com), and KRL Bantry (www.krlbantry.com).

Using the component values in **Figure 1**, the circuit's operating frequency spans 0.1 to 26 Hz. Adding the components in this Design Idea reduces the circuit's dc operating-point shift from 5.5V to less than 25 mV over the frequency range. Most of the frequency

(continued on pg 84)

error occurs at the low end of the frequency range, at which it's the least objectionable. EDN

REFERENCE

1 Dutcher, Al, "Inverters form three-phase VCO," *EDN*, Aug 2, 2001, pg 102, www.edn.com/article/CA149120.

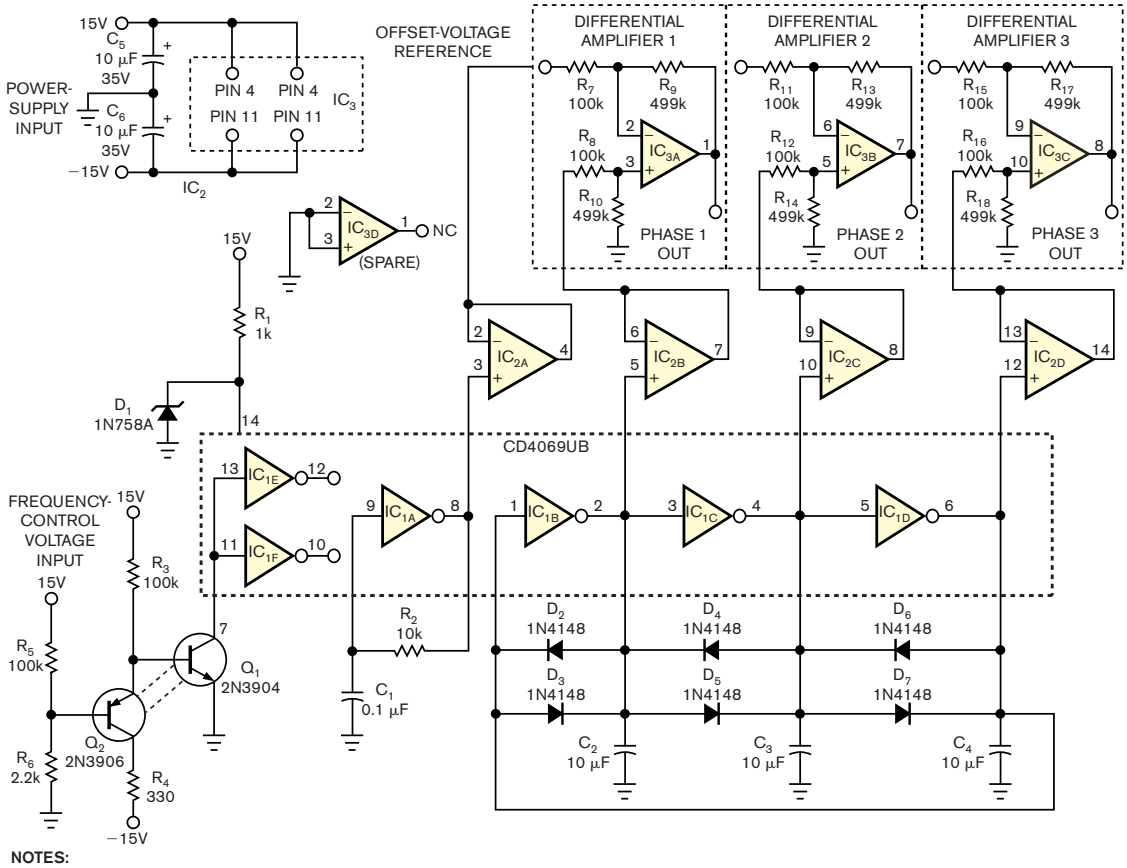

Figure 1 Adding differential and buffer amplifiers and an exponential voltage-to-current converter enhances the performance of a low-frequency, three-phase voltage-controlled oscillator.

Improved current monitor delivers proportional-voltage output

Susanne Nell, Breitenfurt, Austria

This Design Idea expands the capabilities of a previously published one (**Reference 1**). The original version featured a current transformer whose secondary winding formed part of an oscillator's tank circuit. Under normal conditions, direct current flowing through the current transformer's single-turn primary winding kept the circuit from oscillating until primary current flow ceased. Although the circuit acted as a power-interruption detector, when you add a few components, the operating principle lends itself to measurement applications. This revised circuit delivers an accurate linear-voltage output that's proportional to direct current flow through current-sense transformer T_1's primary winding (**Figure 1**). In addition, the circuit also offers possibilities as an ac current sensor.

To achieve improved performance, the design retains the original oscillat-

ing-circuit concept and adds a PLL circuit and one additional winding to the current transformer whose secondary forms an LC oscillator's resonant circuit. Integrating a 74HC4046, IC_1, the PLL measures the frequency of an LC oscillator comprising Q_1 and its associated components and compares it with a fixed-frequency internal VCO (voltage-controlled oscillator). The PLL's phase-comparator output drives a current source comprising Q_2 and Q_3, which in turn feeds current to an additional winding on the current-sense transformer's core.

Sources of T_1's ferrite core include Epcos (www.epcos.com), which offers the B642-90L 632×87-toroid 20×10×7 material N87; Pramet (wwwpramet.com), which offers Fonox Type T20 material H60; Vacuumschmelze (www.vacuumschmelze.com), with the VAC T60006L2020-W409-52; and other manufacturers. Depending on the ferrite material you use, the circuit will operate to some degree with virtually any ferrite toroidal core. (It is difficult to simulate this circuit using PSpice or other simulators; for accurate results, you need a complex model that accurately portrays the core's nonlinear behavior at various current levels.)

The added winding induces magnetic flux in the core, decreasing its permeability and inductance and raising the LC oscillator's frequency. When the oscillator's frequency matches the VCO (reference) frequency, the circuit reaches an equilibrium state. An increasing or decreasing current through the compensation coil balances any additional magnetic flux that dc current flowing through the measurement coil produces.

Within the PLL's frequency-tracking range, the current waveform through the compensation coil has the same shape as fluctuations of the measured current. The turns ratio of 1-to-250, which also represents the ratio of currents in transformer T_1, establishes a secondary current of 10 mA for a primary current of 2.5A. If the PLL circuit's gain is sufficient and the ferrite core's region of operation avoids saturation, the circuit's closed-loop configuration maintains the core's magnetic flux at a constant value and thus minimizes the effects of core-material nonlinearities.

Measuring the voltage difference across resistor R_5 shows that the circuit's output voltage is linearly proportional to the compensation current, and R_5's resistance scales the voltage output. For 100Ω at R_5, a 1V output corresponds to a primary-side current of 2.5A. With zero current flowing in the single-turn primary winding, calibrate the circuit's range by adjusting potentiometer R_{11} to a set operating point. A voltage drop of 2V across R_5 sets a measurement range of +5 to −5A. To accommodate other measurement ranges, you can alter T_1's turns ratio or vary the compensation current by using different values for R_5 and R_{11}. Use a well-regulated power supply to provide power for the circuit. You may be able to replace the 74HC4046 with a software PLL-emulation routine that uses a microcontroller's spare processing resources. EDN

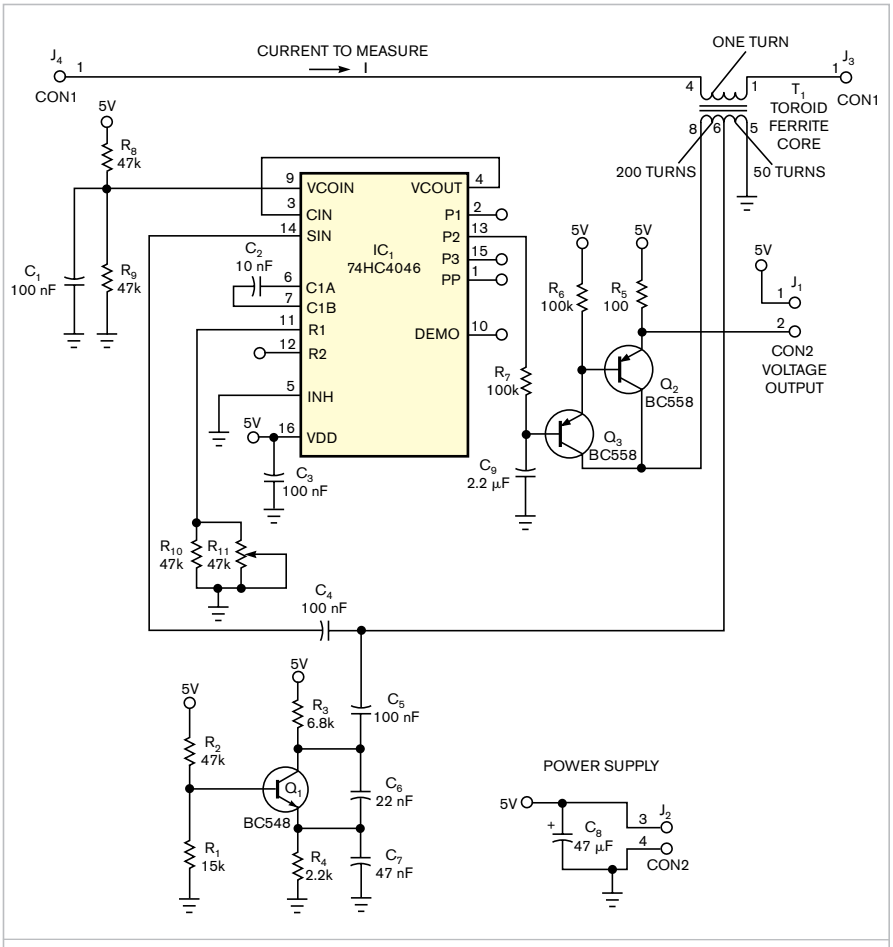

Figure 1 This current sensor uses a variable-frequency oscillator, Q_1, and a PLL, IC_1, to measure current in an isolated circuit.

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Hardened Ethernet cable goes underground

Philip Freidin, Fliptronics, Sunnyvale, CA

An application required the extension of Ethernet (IEEE 802.3u-1995) service from a home to a garage, a distance of approximately 300 ft. Wireless communication using IEEE 802.11a/b/g equipment had proved unreliable due to the buildings' construction, which comprises stucco over embedded wire mesh. In effect, the buildings' walls form Faraday cages that attenuate radiated signals. Straight-line aerial deployment of the Ethernet cable between buildings would have required installation of support poles, and simply laying the cable on the surface of the ground would expose the cable to damage from automobiles, hungry pets, and inquisitive children. At first glance, burial of the cable appeared impractical due to the presence of a large concrete surface between the buildings. However, an alternate route through an adjacent garden would avoid tunneling beneath the concrete slab but would expose the cable to environmental hazards, such as spade work and burrowing animals.

This Design Idea describes how to environmentally "harden" a Category 5 UTP (unshielded-twisted-pair) cable conforming to EIA/TIA 568B and ISO/IEC 11801:1995 that's terminated with RJ-45 connectors (ISO 8877). Without adding repeaters, a Category 5 Ethernet cable can extend to 100m, or a little more than 300 ft. In this application, the cable run comprises 100 ft of exposed cable, 100 ft of "garden-grade" protected cable, and 100 ft more of exposed cable. To apply the idea, you have to find a way to protect and handle the exposed 200 ft of cable.

Depending on your installation's requirements, you will need various numbers and lengths of the following parts: a 100-ft-long garden hose whose fittings conform to the ANSI/ASME B1.20.7-1991.75-11.5 NH thread-form standard; a 4-Gbyte SCSI disk drive, which need not be functional; a continuous, 300-ft-long Category 5 Ethernet cable terminated in RJ-45 connectors; a 120-ft-long, nylon twine; a 5-in.-long, electrical-grade, adhesive-backed tape; a 2-in.-steel, socket-head-cap, 1/4-20-thread machine screw (ANSI/ASME B1.1-1989); and two bricks.

To construct the design, uncoil and stretch the garden hose as straight as possible, perhaps using a driveway as a work surface. Place a brick on each end of the hose to prevent it from curling. If you use only one length of garden hose, cut off and discard the hose fittings. Using Torx or Philips screwdrivers as appropriate, dismantle the 4-Gbyte SCSI disk drive by removing all of the screws that retain the drive's cover. If the cover resists removal, look for screws beneath labels. Remove the drive's head-positioning magnets, which can exert a strong pull on nearby ferrous objects. Use caution to avoid pinching your fingers between the magnets and the steel surfaces. Discard the remainder of the SCSI drive.

Securely tie the nylon twine to the 1/4-20 steel machine screw and insert the screw into one end of the hose. Apply the magnet to the hose's exterior to attract the machine screw. Slide the magnet along the hose to pull the nylon twine through the hose. When the screw reaches the hose's far end, untie the twine and save the screw for future use. To ease manipulation of the Category 5 cable, deploy it from either its original dispenser box or a spool mounted on a suitable axle so that the cable can easily unwind. Securely attach the twine to one end of the Category 5 cable. Walk to the far end of the hose and gently pull the cable through the hose. If you encounter excessive resistance, investigate the cause and remove any cable kinks or feeder-end snags.

When the cable appears at the pulling end, stop for a moment. Go to the other end of the hose and wrap an inch or two of electrical tape around the cable where it's just about to enter the hose. Return to the far end of the hose and continue pulling the cable through the hose. Stop pulling when you see the electrical-tape marker. You now have a 300-ft-long Category 5 cable whose central 100 feet the garden hose protects. If you decide to protect more of the cable, repeat the process by feeding the twine through a second length of hose. Use the hoses' couplings to make a watertight joint between lengths. If you take this approach, make sure that you properly orient the hose segments before you spend too much time threading the twine through the hose. EDN

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Shunt regulator improves power amplifier's current-limit accuracy

John Guy, Maxim Integrated Products Inc, Sunnyvale, CA

Adding current-limiting circuitry to a power amplifier's or a linear voltage regulator's emitter-follower output stage protects both the output transistor and the downstream circuitry from excessive-current damage. **Figure 1** shows the classic current-limiter circuit: Transistor Q_2 senses the output-current-induced voltage drop across ballast resistor R_2 and diverts base current from Darlington-connected transistors Q_1 and Q_3. Transistor Q_2's base-emitter voltage, V_{BE}, sets the circuit's current-limit threshold. Unfortunately, a small-signal transistor's V_{BE} exhibits a temperature coefficient of −2 mV/°C, which causes a substantial variation in the current-limiting threshold over the circuit's operating-temperature range.

You can improve the circuit's performance by replacing Q_2 with IC_1, an adjustable shunt regulator (**Figure 2**). With an input threshold voltage of 0.6V, the MAX8515 allows use of a lower value for current-sense resistor R_2 and thus helps minimize R_2's power and thermal losses. Alternative commonly available shunt regulators present input voltages of 1.25 to 2.5V. In addition, a separate power-supply input connection allows the MAX8515 to maintain accuracy when its internal output transistor approaches saturation.

Figure 3 compares current-limit accuracy for the circuits of **Figure 1** and **Figure 2** over an operating-temperature range of −40 to +85°C. Neglecting the temperature coefficient of sense resistor R_2, the shunt-regulator version maintains its output current to an accuracy of better than 2%, and the small-signal-transistor version exhibits a 25% current variation over the operating-temperature range. EDN

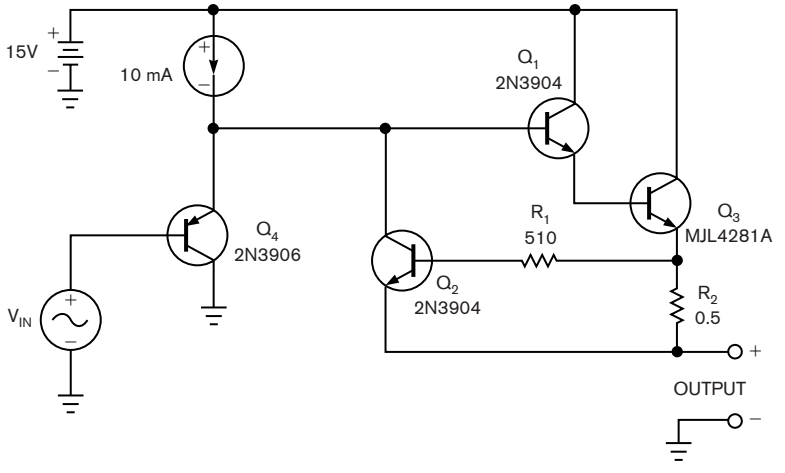

Figure 1 A small-signal transistor, Q_2, provides an output-current limit for this emitter-follower power amplifier.

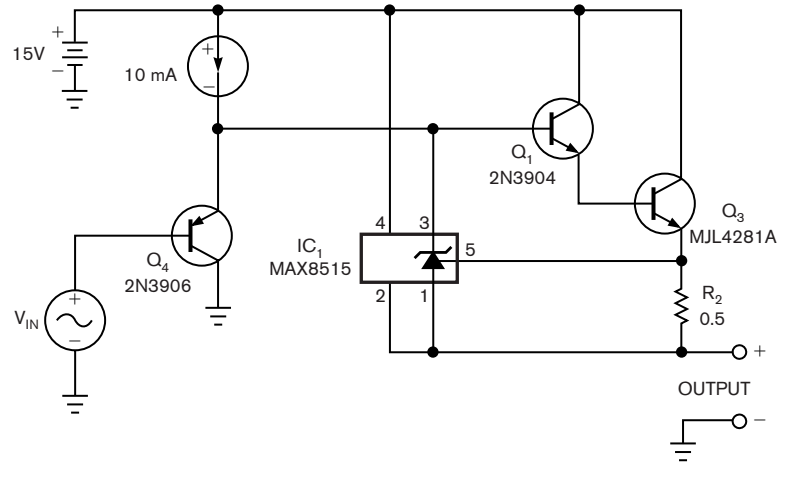

Figure 2 Substituting a shunt regulator, IC_1, for Q_2 in Figure 1 improves the output-current-limit accuracy.

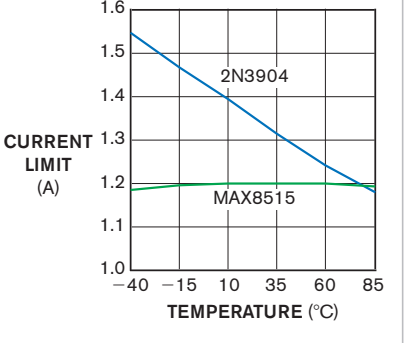

Figure 3 Output-current-versus-temperature plots for the circuits of figures 1 and 2 show improved accuracy for the shunt-regulated circuit (bottom trace) over the discrete-transistor version (top trace).

Low-power, super-regenerative receiver targets 433-MHz ISM band

Cedric Mélange, Johan Bauwelinck, and Jan Vandewege,
Ghent University, Ghent, Belgium

Designers often choose a super-regenerative receiver—despite its frequency instability and poor selectivity—for battery-powered, short-range, wireless applications in which power consumption is a major issue. Examples include remote-keyless-access systems, automobile alarms, biomedical monitors, sensor networks, and computer peripherals (**Reference 1**). A super-regenerative detector can also demodulate frequency-modulated signals through slope detection. Tune the detector so that the signal falls on the slope of the detector circuit's selectivity curve. This Design Idea presents a super-regenerative receiver that consumes less than 1 mW and operates in the license-free, 433-MHz ISM (industrial/scientific/medical) band.

In its simplest form, a super-regenerative receiver comprises an RF oscillator that a "quench signal," or lower frequency waveform, periodically switches on and off. When the quench signal switches on the oscillator, oscillations start to build up with an exponentially growing envelope. Applying an external signal at the oscillator's nominal frequency speeds the growth of the envelope of these oscillations. Thus, the duty cycle of the quenched oscillator's amplitude changes in proportion to the amplitude of the applied RF signal (**Figure 1**).

A super-regenerative detector can receive AM signals and is well-suited for detecting OOK (on/off-keyed) data signals. The super-regenerative detector constitutes a sampled-data system; that is, each quench period samples and amplifies the RF signal. To accurately reconstruct the original modulation, the quench generator must operate at a frequency a few times higher than the highest frequency in the original modulating signal. Adding an envelope detector followed by a lowpass filter improves AM demodulation (**Reference 2**).

IN ITS SIMPLEST FORM, A SUPER-REGENERATIVE RECEIVER COMPRISES AN RF OSCILLATOR THAT A "QUENCH SIGNAL," OR LOWER FREQUENCY WAVEFORM, PERIODICALLY SWITCHES ON AND OFF.

Figure 2 is a block diagram of the super-regenerative receiver circuit in **Figure 3**. The heart of the receiver comprises an ordinary Colpitts-configured LC oscillator operating at a frequency that the series resonance of L_1, L_2, C_1, C_2, and C_3 determines. Switching off transistor Q_1's bias current quenches the oscillator. (Note that increasing C_1 and C_2 improves the oscillator's frequency stability at the expense of increased power consumption.) Cascode-connected transistors Q_2 and Q_3 form an antenna amplifier that improves the receiver's noise figure and provides some RF isolation between the oscillator and the antenna. To conserve power, the amplifier operates only during oscillation growth.

Based on a Schmitt-trigger circuit, the quench generator switches the oscillator and RF-amplifier stage. To improve sensitivity, the triangular waveform across C_5 quenches the oscillator, and the square wave at the output of IC_1 switches the RF amplifier. The quench generator's two outputs are phased in quadrature so that the RF amplifier has received power when the detector's oscillations start to grow. The quench frequency of this circuit is 100 kHz to allow data transfers at rates as high as 20 kbps.

The envelope detector comprises a common-source amplifier that's nominally biased to operate in Class B mode. To increase this stage's gain, you apply a small amount of bias current to make it operate in Class AB mode. To reduce the load on the oscillator's LC tank circuit, C_{10} connects to a tap on inductor L_1, as inductor L_2 shows.

The first stage in the data-recovery circuit comprises buffer IC_{2A}; amplifier IC_{2B}; and a third-order, lowpass filter for suppressing quench-frequency components in the envelope detector's output. A dc-coupled Schmitt-trigger circuit, IC_3, extracts the transmitted data from the demodulated signal. A lowpass filter comprising C_{12} and R_{16} extracts the demodulated signal's dc

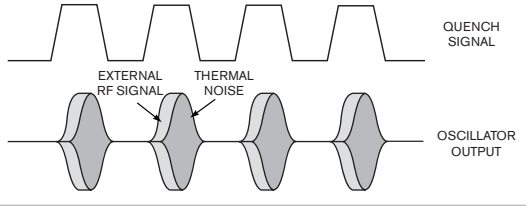

Figure 1 In a super-regenerative detector, the arrival of a signal starts RF oscillations sooner than under no-signal conditions.

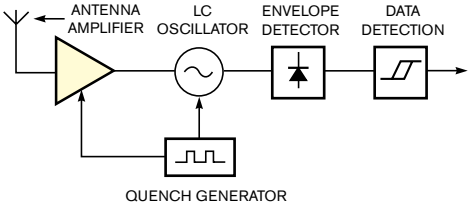

Figure 2 The super-regenerative receiver is considerably simpler than a superheterodyne circuit.

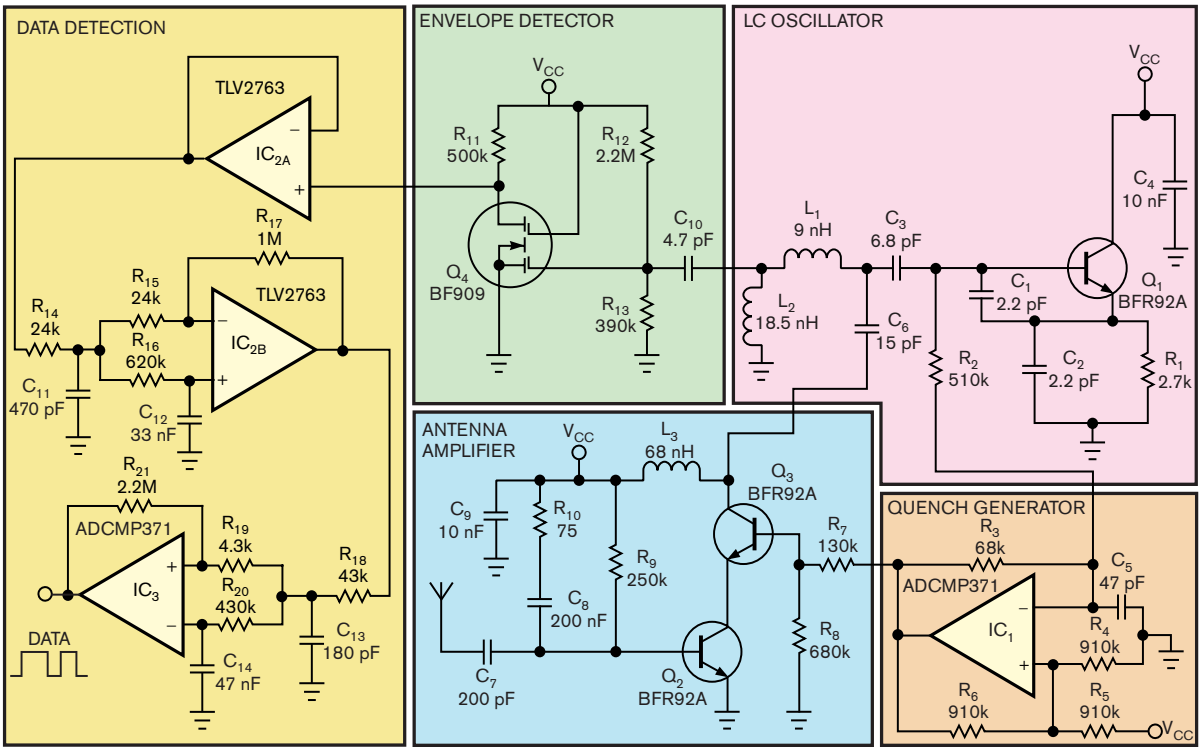

Figure 3 The super-regenerative receiver features relatively few components.

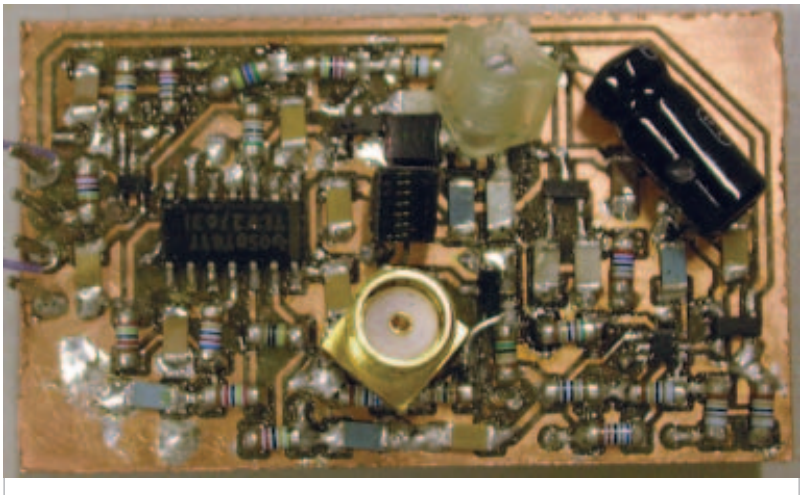

Figure 4 A prototype version of a super-regenerative receiver uses mostly surface-mount components. The large, black, leaded component in the upper right corner is a power-supply-decoupling capacitor. Note the RF-input connector in the center of the pc board.

component and sets the Schmitt trigger's decision threshold. As a consequence, the data transmitter must use a dc-balanced coding scheme, such as Manchester coding, for modulation. On the receiving end, no additional active components are necessary for extracting the data-recovery circuit's decision threshold, which helps minimize the receiver's power consumption.

The prototype occupies a compact pc board measuring approximately 5×3 cm (**Figure 4**). Using a simple, homemade PRBS (pseudorandom-binary-sequence) generator that uses Manchester coding with a 28-to-1-bit sequence (**Reference 3**), BER (bit-error-rate) measurements yield the results in **Figure 5**. These results demonstrate a sensitivity of less than −100 dBm for a 10-to-4 BER at 1 kbps. The receiver consumes 270 µA at 3V for a power consumption of 810 µW. As a further

enhancement to the design, it includes a transmitter circuit based on Maxim's MAX1472, creating a simple, compact, low-cost, and low-power transceiver for the 433-MHz ISM band. You can easily adapt the receiver circuit for recovery of AM audio or other analog signals by replacing the Schmitt trigger, IC_3, with a conventional audio-output amplifier. Retune the RF oscillator to cover the frequency range of interest. EDN

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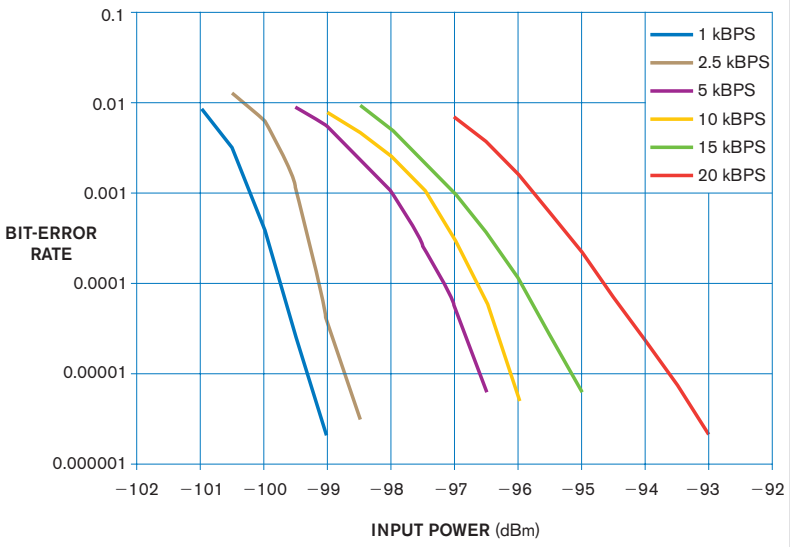

Figure 5 Measurements of bit-error rate versus input RF power highlight the prototype receiver's sensitivity. The frequency is 433.92 MHz.

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Lowpass, 30-kHz Bessel filter offers high performance for audio applications

Troy Murphy, Analog Devices, San Jose, CA

Thanks to its property of applying an equal amount of delay to all frequencies below its cutoff frequency, the Bessel linear-phase filter sees service in audio applications in which it's necessary to remove out-of-band noise without degrading the phase relationships of a multifrequency in-band signal. In addition, the Bessel filter's fast step response and freedom from overshoot or ringing make it an excellent choice as a smoothing filter for an audio DAC's output or as an antialiasing filter for an audio ADC's input. Bessel filters are also useful for analyzing the outputs of Class D amplifiers and for eliminating switching noise in other applications to improve accuracy of distortion and oscilloscope-waveform measurements.

Although the Bessel filter provides flat magnitude and linear-phase—that is, uniform group-delay—responses within its passband, it has worse selectivity than Butterworth or Chebyshev filters of the same order, or number of poles. Thus, to achieve a given level of stopband attenuation, you need to design a higher order Bessel filter, which, in turn, requires careful selection of amplifiers and components to achieve the lowest levels of noise and distortion.

Figure 1 shows a schematic for a high-performance, eighth-order, 30-kHz, lowpass Bessel filter. This design uses standard values for 1%-tolerance resistors and 5%-tolerance ceramic capacitors. As an alternative, you can use 10%-tolerance capacitors at the expense of increased group-delay variance within the passband. For best results, use temperature-stable capacitors.

In this application, the filter processes audio signals that swing above and below ground, and its amplifiers draw power from positive and negative ±2.5V supplies. Rail-to-rail output capability helps achieve maximum output-voltage swing at these low supply voltages. To achieve a high SNR in high-quality audio service, the amplifiers must exhibit unity-gain stability and low inherent noise. For example, Analog Devices' AD8656 low-noise, precision-CMOS dual op amp meets all of these requirements.

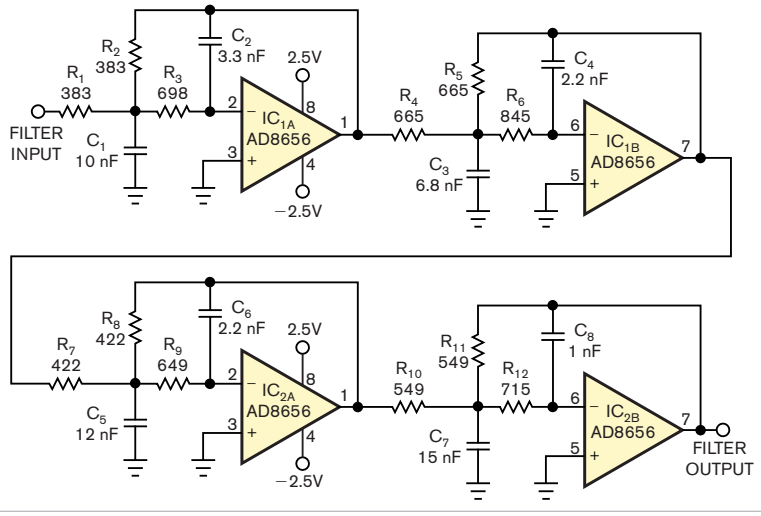

Figure 1 Two dual op amps and a handful of passive parts implement a high-performance, eighth-order, 30-kHz, lowpass Bessel filter.

Connecting the amplifiers as inverting-gain stages maintains constant input-common-mode voltage and helps minimize distortion. Using less-than-1-kΩ resistors throughout the circuit reduces the resistors' thermal-noise contributions. Each AD8656 amplifier contributes less than 3 nV/$\sqrt{\text{Hz}}$ of noise across a 30-kHz bandwidth, and the total noise over a 30-kHz bandwidth measures less than 3.5 μV rms. For a 1V-rms input signal, the circuit yields an SNR of better than 109 dB, and, for a 1-kHz, 1V-rms input signal, the circuit yields a THD+N (total-harmonic-distortion-plus-noise) factor of better than 0.0006%.

Figure 2 shows the filter's measured magnitude response for a 1V-rms input signal. The filter's passband gain of 0 dB is flat within 1.2 dB for frequencies as

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high as 20 kHz. With its −3-dB point at 30 kHz, an eighth-order Bessel presents a theoretical attenuation of −110 dB at 300 kHz, decreasing at −160 dB/decade at higher frequencies. This characteristic provides sufficient attenuation of repetitive noise that switched-mode power supplies and other sources induce, which typically occurs at frequencies of 300 kHz and higher.

Figure 3 illustrates the filter's phase shift and its group delay, which remains relatively constant at roughly 17 µsec, even for frequencies as high as 40 kHz. Note the linear scale on **Figure 3**'s frequency axis, which clearly illustrates the filter's linear-phase behavior within the passband. The following **equation** defines group delay as the negative partial derivative of phase shift with respect to frequency:

$$\text{Group delay} = -\delta\phi/\delta f.$$

At dc, resistor R_1 sets the filter's input resistance at 383Ω. If your application requires higher input impedance, you can insert a unity-gain buffer ahead of the filter at the expense of increased distortion and noise. For applications that require operation from ±15V power supplies, replace the AD8656 with a higher voltage amplifier, such as Analog Devices' AD8672 low-distortion, low-noise (3.8-nV/$\sqrt{\text{Hz}}$), dual operational amplifier. EDN

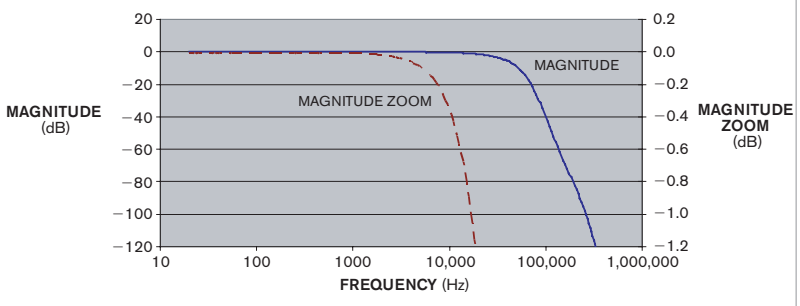

Figure 2 The measured amplitude-versus-frequency response of the circuit in Figure 1 shows a change of scale on the right vertical axis.

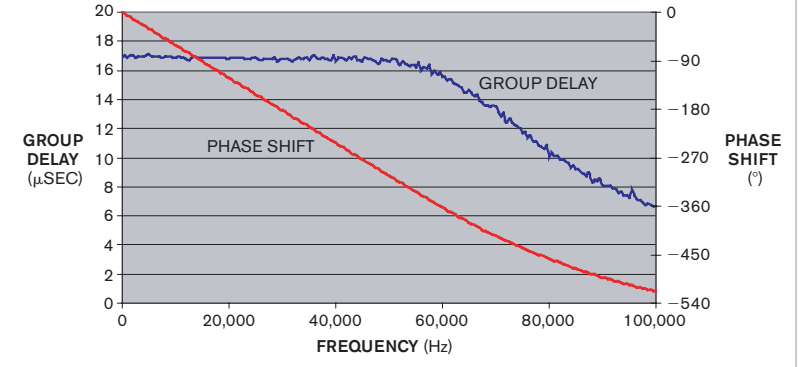

Figure 3 Measured within the passband of dc to 30 kHz, the Bessel filter's phase-shift and group-delay characteristics display excellent uniformity and linearity.

Use a PWM fan controller in an EMI-susceptible circuit

Dimitri Danyuk, Niles Audio Corp

Microchip Technology (www.microchip.com) offers a family of cooling-fan speed controllers that operate in PWM mode for use with brushless dc fans (**Reference 1**). To control fan speed using the PWM waveform's duty cycle, you can use either an external NTC (negative-temperature-coefficient) thermistor or one of Microchip's PIC microcontrollers and its SMBus serial-data bus. **Figure 1** illustrates a typical application that the data sheet describes for the TC664 and TC665 controllers (**Reference 2**). Using a frequency-control capacitor, C_F, with a value of 1 µF, fan-controller IC_1 generates a PWM pulse train with a nominal frequency of 30 Hz and a temperature- or command-dependent duty cycle that varies from 30 to 100%.

Although using the controller in PWM mode reduces power dissipation in transistor Q_A, which drives the fan, the 100-mA, square-wave motor-drive current can cause unwanted interference in a nearby high-sensitivity audio circuit. The circuit in **Figure 2** solves the problem. An additional driver transistor, Q_1, and an RC network comprising C_3 and R_3 form a simple PWM-to-linear converter. You can also use another PWM-to-linear-conversion circuit, such as an integrator based on an operational amplifier.

Figure 3 shows a graph of the dc voltage at Q_2's collector versus IC_1's PWM

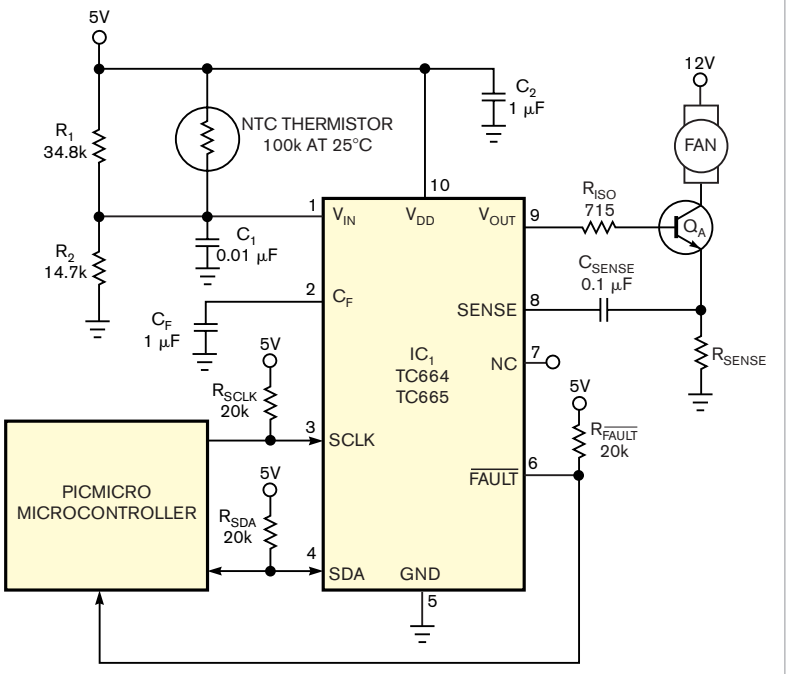

Figure 1 In a typical application, fan-controller IC_1 and transistor Q_A apply pulse-width-modulated current to vary a fan's speed as a function of temperature.

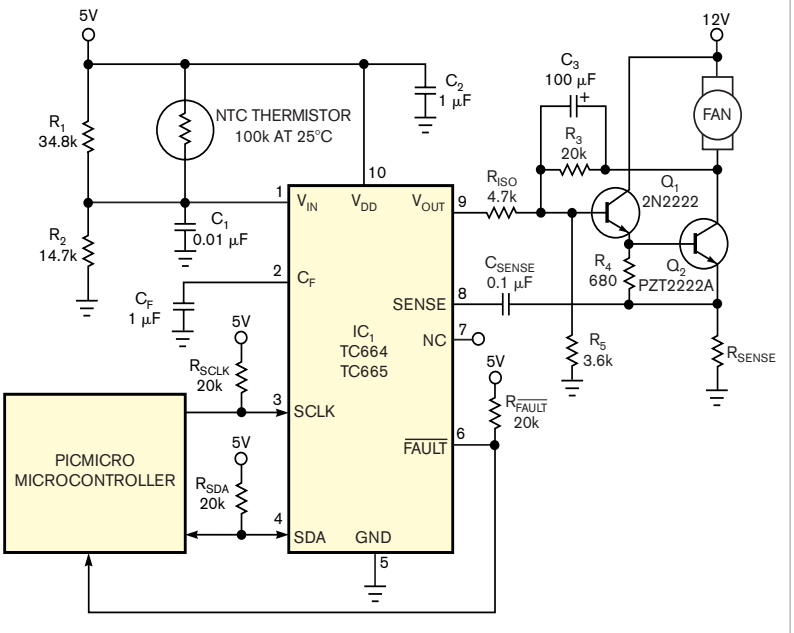

Figure 2 To minimize the effects of high-frequency noise on sensitive analog circuits, you can convert the high-current PWM waveform applied to the fan to a continuous analog voltage.

drive-output waveform's duty cycle. The voltage applied to the fan corresponds to the difference between Q_2's collector voltage and the 12V supply voltage. Even though a steady voltage appears across the fan, current pulses that the fan motor's commutation produces still develop a voltage across current-sense resistor R_{SENSE} that connect to Q_2's emitter, and all of IC_1's protective and advisory features remain available.

The listed component values are valid for a 100-mA, 12V, brushless fan. Use a general-purpose NPN transistor such as the 2N2222 for driver-transistor Q_1 and an NPN transistor, such as Fairchild Semiconductor's PZT2222A, that can dissipate one-third of the fan's maximum power consumption for Q_2. Note that you can vary the PWM's nominal frequency over a range of 15 to 35 Hz by altering the value of C_F. EDN

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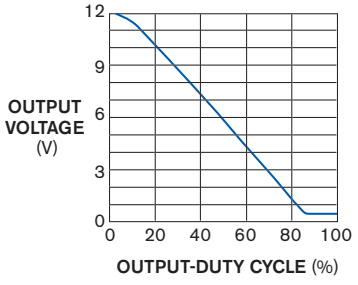

Figure 3 Output voltage at Q_2's collector shows a linear relationship versus the controller's pulse-width-modulated output-duty cycle. (The pulse width increases as the temperature increases.) The fan's operating voltage corresponds to the difference between Q_2's output voltage and the 12V supply rail.

PC's parallel port and a PLD host multiple stepper motors and switches

Eduardo Pérez-Lobato, Universidad de Antofagasta, Antofagasta, Chile

Robotic applications frequently include multiple stepper motors and switches. The stepper motors produce motion in several directions, and the switches identify home positions and detect proximity to obstacles. This Design Idea describes the development and implementation of a PLD (programmable-logic-device)-based interface that can connect a PC's parallel port to as many as eight switches and four stepper motors (**Figure 1**). This interface design serves many applications, and using IC_1, a 22V10 PLD, to minimize the circuit's component count reduces complexity, weight, and overall dimensions. Drivers IC_3 through IC_6 for the stepper motors comprise three L293 quad half-H-bridge ICs (**Figure 2**).

Each rotation of the two-winding stepper motors in this design requires a sequence of four mechanical steps that you produce by applying a pair of 7V, 500-mA, 120-msec-long pulses to the motor's windings (**Figure 3**). To make a stepper motor rotate either CW (clockwise) or CCW (counterclockwise), you apply either of two pulse sequences (**tables 1** and **2**).

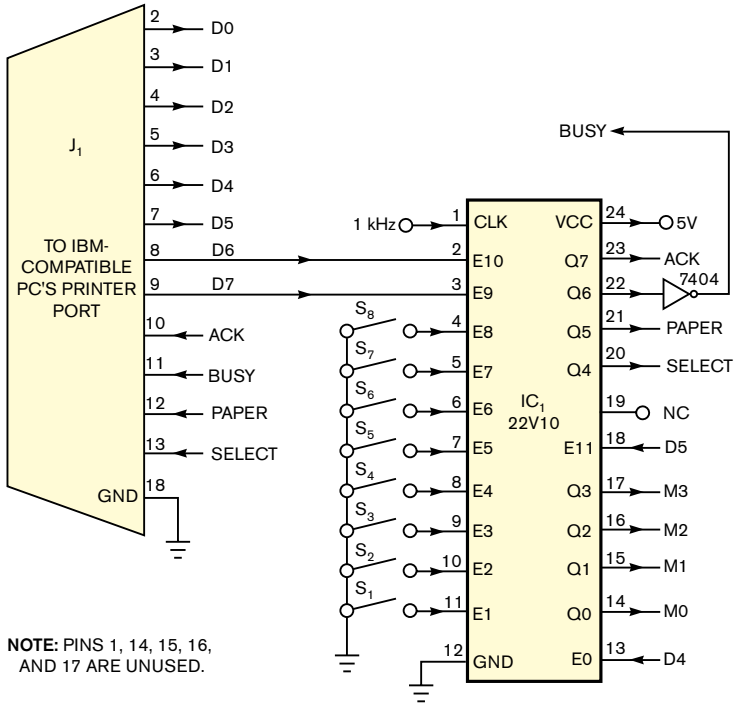

Figure 1 A programmable-logic device, IC_1, and a few additional components allow an IBM-compatible PC's parallel printer port to drive as many as four external stepper motors and to sense the states of as many as eight range-of-motion limit switches.

The following sections specify the functions of the input and output registers' bits that control the parallel-port interface and the PLD. The PLD output-register bits are 7, 6, 5, 4, 3, 2, and 1. Q7 signals the PC that one or more switches are active. Bit 0 means that a switch is active; bit 1 means that no switches are active. With Q6, Q5, and Q4, the BSS (buffered-status switch) tells the PC which of n switches is active: $000=S_1$, $100=S_5$, $001=S_2$, $101=S_6$, $010=S_3$, $110=S_7$, $011=S_4$, and $111=S_8$. For Q3, Q2, Q1, and Q0, the PLD's outputs enable one of the four motor-driver ICs to drive its associated stepper motor, with $1000=M_3$, $0010=M_1$, $0100=M_2$, and $0001=M_0$.

The PLD input register's bits are E11, E10, E9, and E0. For E11, the host PC controls the PLD, 0 disables the PLD, and 1 enables the PLD. For E10 and E9, the PLD reads these lines to determine which of the four motors in **Figure 2** receives drive pulses: 00 for Motor 0, 10 for Motor 2, 01 for Motor 1, and 11 for Motor 3. For bit E0, the PLD reads this bit to determine what to do with the BSS settings: 0=hold, and 1=clear. For E8 through E1, the PLD reads the status of one switch and stores it in the BSS register:

$00000001=S_1$, $00010000=S_5$,
$00000010=S_2$, $00100000=S_6$,
$00000100=S_3$, $01000000=S_7$,
$00001000=S_4$, $10000000=S_8$.

The PLD ignores any unlisted bits.

For the parallel-port output register, address 888_{10}, D7, and D6, the PC tells

TABLE 1 CLOCKWISE-ROTATION SEQUENCE

Step	A	B	C	D
0	1	1	0	0
1	0	1	1	0
2	0	0	1	1
3	1	0	0	1

TABLE 2 COUNTERCLOCKWISE-ROTATION SEQUENCE

Step	A	B	C	D
0	1	0	0	1
1	0	0	1	1
2	0	1	1	0
3	1	1	0	0

the PLD which motor should run, with 00 for Motor 0, 10 for Motor 2, 01 for Motor 1, and 11 for Motor 3. For D5, the PC takes control of the PLD chip: 0 disables the PLD, and 1 enables the PLD. For D4, the PC commands the PLD to control the BSS register's contents, with 0 for hold and 1 for clear. For D3 through D0, the PC selects which pair of motor windings get energized: 1001=A and D, 1100=C and D, 0011=A and B, and 0110=C and B. Parallel-port input-register, address $888_{10}+1$ indicates acknowledge, busy, paper, or select. The PC reads acknowledge to determine whether a switch is active: 0 means that any switch is active, and 1 means that no switch is active. The PC reads the busy, paper, or select register to determine which of the switches is active:

$000=S_1$, $011=S_4$,
$110=S_7$, $001=S_2$,
$100=S_5$, $111=S_8$,
$010=S_3$, $101=S_6$.

You can download **Listing 1** for this Design Idea from www.edn.com/060216di3. Note that the PC's portion of the software is written in Pascal, and the PLD's internal software is written in an emulated version of Basic. EDN

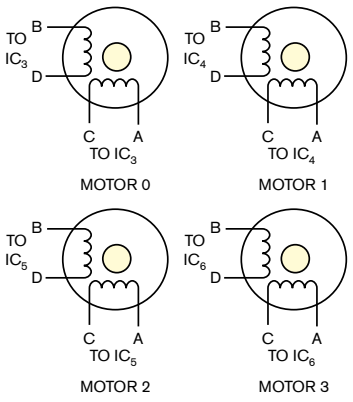

Figure 3 To control a stepper motor's direction of rotation, energize the windings as shown in tables 1 and 2.

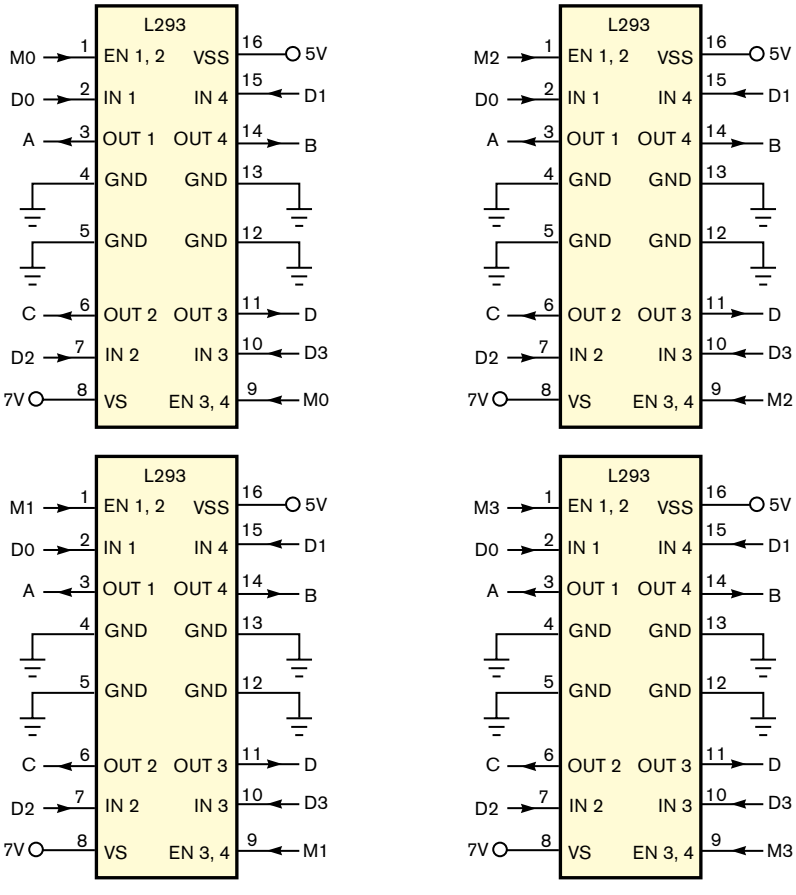

Figure 2 Each half-bridge-driver circuit, IC_3 through IC_6, controls a single two-winding stepper motor.

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READERS SOLVE DESIGN PROBLEMS

Op amp can source or sink current

Alfredo H Saab and Steve Logan,
Maxim Integrated Products Inc, Sunnyvale, CA

When you design for electronics applications, such as sensor or amplifier bias supplies or special waveform generators, a controlled constant-current source or sink circuit can serve as a useful building block. These circuits exhibit high dynamic-output impedance and deliver relatively large currents within an allowed range of compliance voltage. You can implement a constant-current circuit with an op amp and a discrete external transistor, but you can also design a bipolar version of a current source or sink around a single op amp and a few resistors (**Figure 1**). The constant-current sink circuits in **Figure 1a** through **Figure 1c** offer various compromises between precision, dynamic impedance, and compliance range.

The circuit in **Figure 1d** describes a bipolar current source with a simpler feedback configuration than that of the usual Howland-current pump, which requires positive feedback and presents variable input impedance. **Figure 1e** shows a constant-current source. All of these circuits exhibit excellent linearity of output current with respect to input voltage.

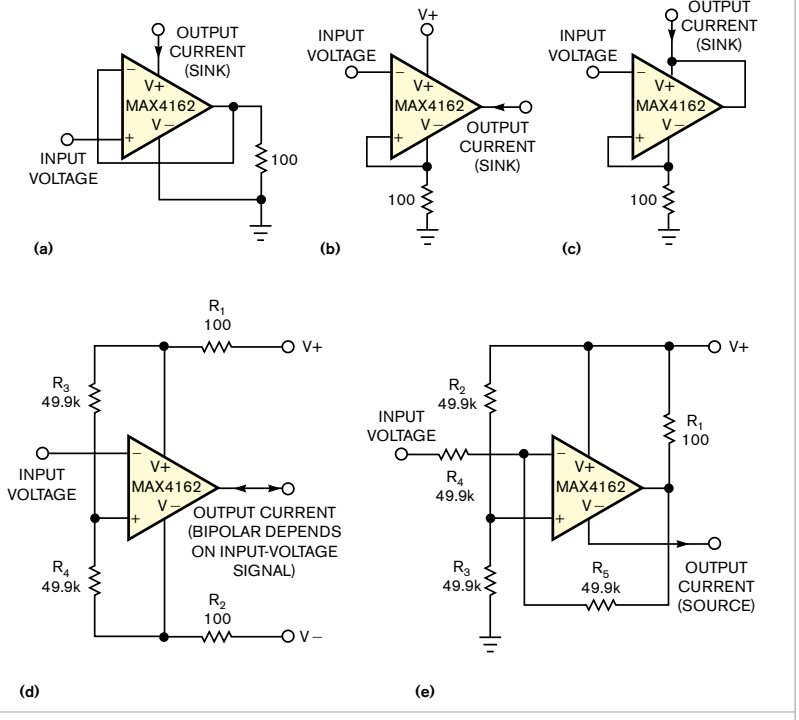

Figure 1 This compendium of constant-current circuits includes current sinks (a, b, and c), a bipolar sink or source (d), and a current source (e).

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The output from the circuit in **Figure 1a** includes an uncertainty due to the op amp's quiescent current, which adds to the calculated output current. For example, in most applications, you can neglect the MAX4162 op amp's quiescent current of approximately 25 µA. The circuit in **Figure 1b** behaves similarly, but its quiescent current subtracts from the ideal output-current value. The circuit in **Figure 1c** provides a current sink with no quiescent-current error, and the circuit in **Figure 1d** presents a bipolar output—that is, it sinks or sources current—depending on the polarity of the input voltage. Its performance depends on close matching for the resistor pairs R_1 and R_2 and R_3 and R_4 and good tracking of the positive- and negative-power-supply voltages. Any difference between the absolute values of the supply voltages appears as an offset current at 0V input voltage. To achieve insensitivity to power-supply-voltage variations, the current-source circuit in **Figure 1e** requires close matching of resistor pairs R_2 and R_3 and R_4 and R_5.

You can use the following equations to calculate output currents for the cir-

cuits in **Figure 1**. Note that R_{LOAD}= 100Ω in these examples. In **Figure 1a**, $I_{OUT}=-V_{IN}/R_{LOAD}+25\ \mu A$; in **Figure 1b**, $I_{OUT}=-V_{IN}/R_{LOAD}-25\ \mu A$; in **Figure 1c**, $I_{OUT}=-V_{IN}/R_{LOAD}$; in **Figure 1d**, $I_{OUT}=-2\times V_{IN}/R_{LOAD}$; and, in **Figure 1e**, $I_{OUT}=V_{IN}/R_{LOAD}$. The equation for circuit **1d** assumes perfect matches—that is, $R_3=R_4$, $R_1=R_2$, and V+ = V−. It also assumes that R_4 is much greater than R_1.

For a fixed value of output current in each of the five circuits in **Figure 1**, the graphs of **Figure 2** show the circuits' dynamic impedance and range of useful output voltage (current compliance). The graphs show a high nominal output current of 5 mA to better display the higher end of the current-amplitude range. Depending on your application, you can optimize each circuit's dynamic impedance and current range through a judicious choice of op amps and resistor values. EDN

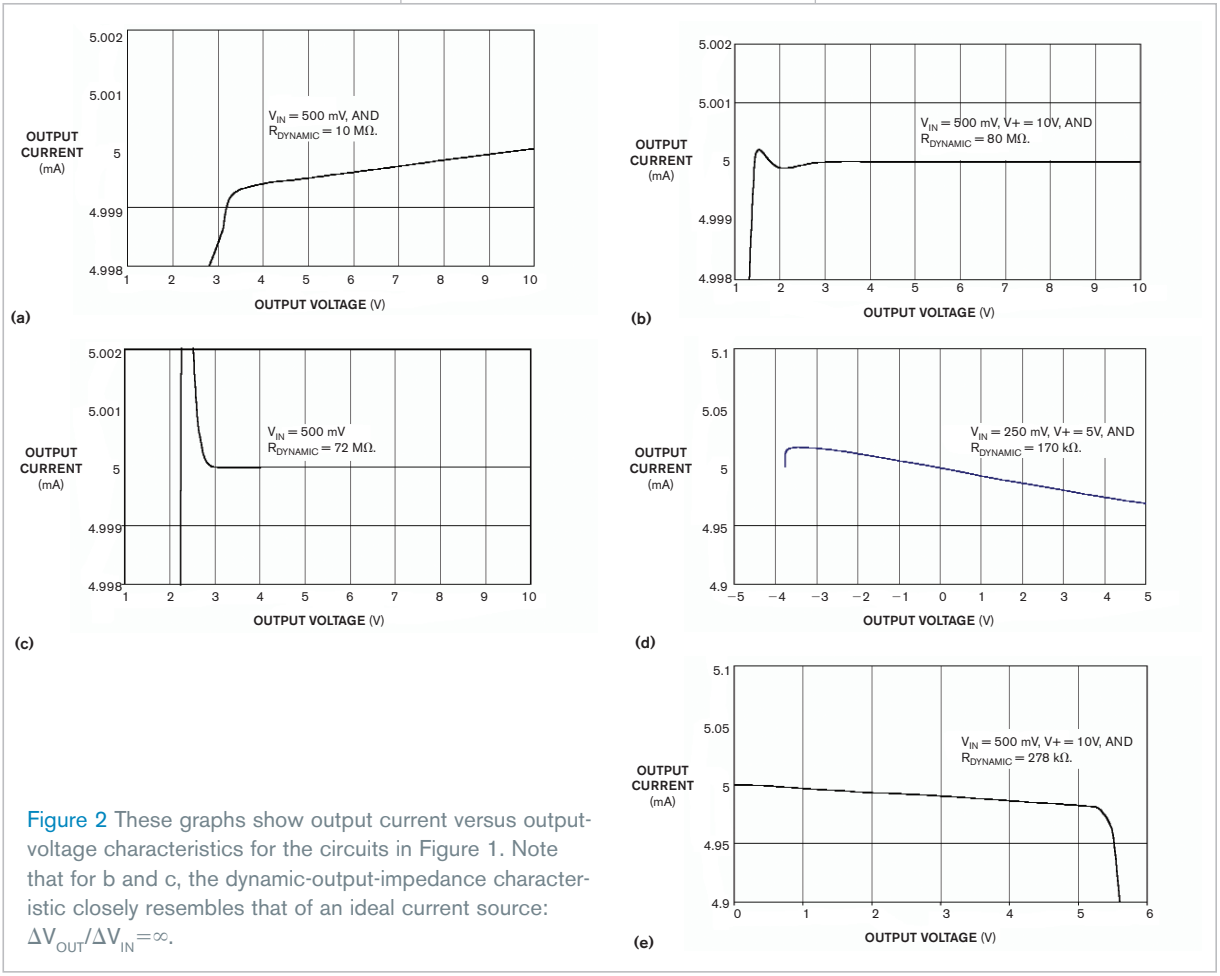


Figure 2 These graphs show output current versus output-voltage characteristics for the circuits in Figure 1. Note that for b and c, the dynamic-output-impedance characteristic closely resembles that of an ideal current source: $\Delta V_{OUT}/\Delta V_{IN}=\infty$.

Simple digital filter cleans up noisy data

Richard Rice, Oconomowoc, WI

Many systems use an ADC to sample analog data that temperature and pressure sensors produce. Sometimes, system noise or other factors cause the otherwise slowly fluctuating data to "jump around." To reduce higher frequency noise, designers often install an analog RC (resistor-capacitor) lowpass filter between the sensor and the analog-to-digital-conversion stage. However, this approach is not always ideal or practical. For example, a long time constant of minutes would require very large values for R and C.

Figure 1 shows an analog RC lowpass filter and its design equations. As an alternative, you can clean up noisy signals that remain within the ADC's lin-

ear range by using the digital equivalent of an analog RC lowpass filter. The filter's software comprises only two lines of C code: $LP_{OUT}=LP_{ACC}/K$, where the output value of the filter is LP_{ACC} divided by a constant, and $LP_{ACC}=LP_{ACC}+LP_{IN}-LP_{OUT}$, where you add the difference between input and output to update LP_{ACC}. You specify all variables as integers.

Each time the analog-to-digital conversion acquires a new input sample, LP_{IN}, the software produces an output value, LP_{OUT}, which comprises a lowpass-filtered version of the input samples. Calculate the value of the constant, K, based on the sampling rate of the system and the desired time constant for the filter as follows: $K=T\times SPS$, where $K>1$, and SPS is the system's sampling rate. For example, for a system-sampling rate of 200 samples/sec and a desired time constant of 30 sec, the constant K would equal 6000 samples. Applying a step change to the routine's input requires 6000 samples to reach approximately 63% of its final value at the output.

The lowpass accumulator, LP_{ACC}, can grow large for large time constants and large input values. It can grow as large as K times the largest possible LP_{IN} value. Under these conditions, you need to make sure that LP_{ACC} does not overflow, and you may need to specify a larger data type to contain LP_{ACC}. To avoid a long settling time during start-up, before the start of the sampling loop, you can initialize LP_{ACC} to a value of K times the current input value.

You can extend the basic filter concept presented to accommodate higher order filters with greater high-frequency rejection by executing multiple filter code segments in sequence. Also, you can use an array of variables for LP_{ACC} and an array of values of the constant K to filter signals that multiple data channels acquire. EDN

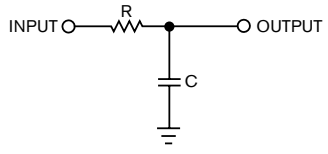


Figure 1 In some circumstances, a classic RC lowpass filter does an adequate job of removing noise from signals.

Single switch selects one of three signals

Felix Matro, JL Audio Corp, Phoenix, AZ

This Design Idea shows how you can use a single-pole momentary-contact switch to select one of three signal sources by scrolling through three output states. The circuit in **Figure 1** comprises commonly available components from the CD4000 CMOS-logic series, along with a general-purpose NPN transistor. The total cost of the components doesn't exceed $1. Only one of circuit's three outputs, CH_1, CH_2, or CH_3, goes low at any given time, and you can use these outputs to control analog switches, relays, or the gates of JFET switches. As long as you apply power, the

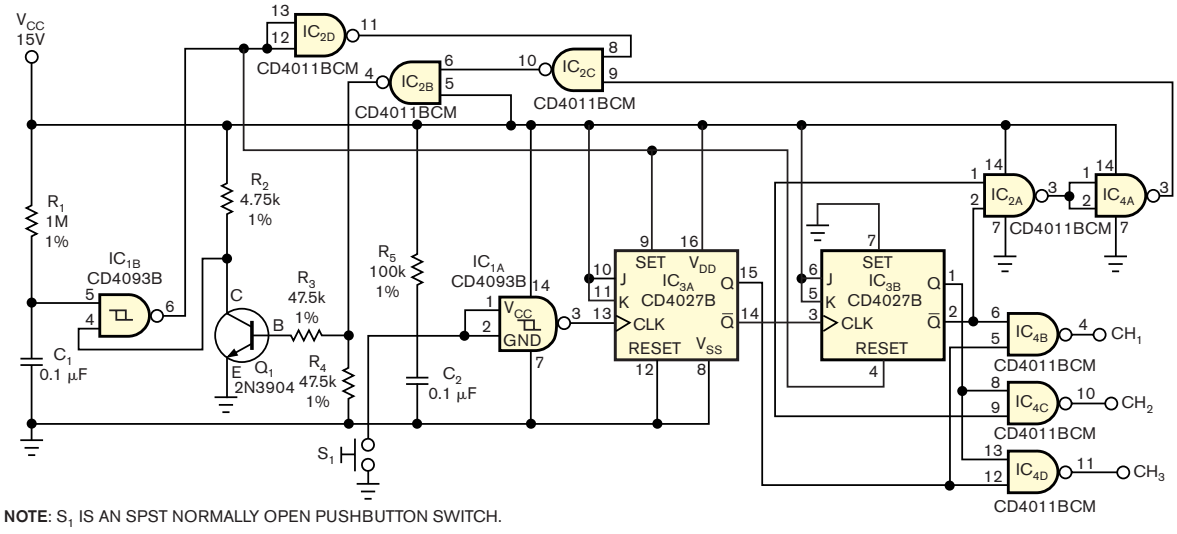


Figure 1 A handful of active and passive components form a one-of-three selector switch. Press switch S_1 once to advance to the next channel and twice more to revert to Channel 1.

selected output does not change, making the circuit a good choice for applications requiring nonvolatile operation. Quiescent-current consumption averages only about 15 µA at room temperature, 25°C, a low value even for battery-powered applications.

The heart of the circuit comprises a dual JK flip-flop, IC_3, that's configured as a 2-bit ripple counter. Without additional circuitry, the counter would allow selection of four signal sources. Upon initial application of power, a reset circuit comprising R_1, C_1, and IC_{1B} always sets the CH_1 output to a logic-low level.

When the $\overline{Q}$ outputs of IC_3, pins 2 and 14, both go to logic zeros, the feedback chain comprising IC_{2A}, IC_{2B}, IC_{2C}, and IC_{4A} pulls Q_1's base to a logic-high level, which in turn pulls one input of IC_{1B} to a logic low. This action causes the counter to skip the 00 state and advances the count to the 01 state. Components R_5, C_2, IC_{1A}, and normally open momentary-contact switch S_1 constitute a debounced switch that provides clock pulses for both sections of the counter, IC_3. When a user pushes S_1, the counter advances to the 10 state, and a subsequent push advances the counter to the 11 state. A third push restarts the cycle. To summarize, IC_{4B} decodes the counter's 01 state and pulls CH_1 low, IC_{4C} decodes the counter's 10 state and pulls CH_2 low, and IC_{4D} decodes the counter's 11 state and pulls CH_3 low. The layout of the circuit should be noncritical, but use a low-leakage capacitor for C_1. Connect unused logic inputs to ground or V_{CC} as appropriate. EDN

R_5, C_2, IC_{1A}, AND NORMALLY OPEN MOMENTARY-CONTACT SWITCH S_1 CONSTITUTE A DEBOUNCED SWITCH THAT PROVIDES CLOCK PULSES FOR BOTH SECTIONS OF THE COUNTER.

Low-cost audio filter suppresses noise and hum

Richard M Kurzrok, RMK Consultants, Queens Village, NY

The low-cost composite passive filter in this Design Idea requires no dc power and can enhance the performance of audio equipment and instrumentation by rejecting power-supply hum and spurious pickup from AM, FM, and low-band VHF transmissions (**Figure 1**). The composite filter comprises a cascade of three simple filters: a T-section highpass filter to reject power-source hum and two π-section lowpass filters to reject spurious RF signals. As a starting point, the three filter sections present a lossless 0.01-dB Chebyshev response at a 50Ω impedance level, but you can scale the components' values to meet other impedance requirements.

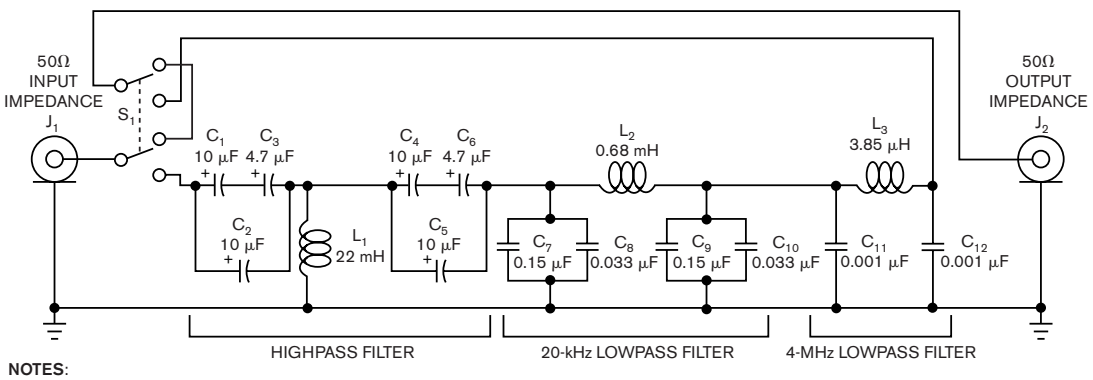
Table 1 lists the components the prototype filter uses. With the exception of inductor L_3, all the components are standard values that are available off the shelf. Switch S_1 provides a bypass mode that permits rapid frequency-response measurements without connection and disconnection of the prototype's BNC connectors. To construct the prototype, wire all components to a section of perforated breadboard stock supported by metal spacers that mount inside a die-cast aluminum enclosure. This method of shielded construction has proved its worth in other laboratory-accessory applications (**Reference 1**). **Table 2** lists the filter's measured insertion loss over a range of 40 Hz to 200 MHz.

Low-cost polarized electrolytic capacitors C_1 through C_6 provide reasonable performance, but observe input polarity for signals with a dc component. For a modest increase in cost and assembly time, you can enhance filter performance and reproducibility by selecting the values of these capacitors to meet a 10% or better tolerance. For best results, use nonpolarized film-dielectric capacitors for C_1 through C_6. For noncritical applications, you can relax the tolerances for the remaining capacitors and use off-the-shelf inductors for 22-mH L_1, 0.68-mH L_2, and 3.9-µH L_3.

Redesigning the filter to match the 600Ω impedance that you find in classic audio circuits would increase the

TABLE 1 COMPONENTS IN THE PROTOTYPE FILTER

Reference designators	Values	Description
C_1, C_2, C_4, C_5	10 µF	50V electrolytic capacitor, ±20% tolerance
C_3, C_6	4.7 µF	50V electrolytic capacitor, ±20% tolerance
C_7, C_9	0.15 µF	Polypropylene capacitor, ±2% tolerance
C_8, C_{10}	0.033 µF	Polypropylene capacitor, ±2% tolerance
C_{11}, C_{12}	0.001 µF	Polypropylene capacitor, ±2% tolerance
L_1	22 mH	Inductor, ±5% tolerance
L_2	0.68 mH	Inductor, ±10% tolerance
L_3	3.85 µH	Inductor, 27 turns of AWG #28 magnet wire hand-wound on T37-2 mixture (Carbonyl E) toroidal core
S_1	NA	DPDT panel-mounted toggle switch
J_1, J_2	NA	50Ω BNC panel jack
NA	NA	Hammond 1590H-BK die-cast aluminum enclosure



NOTES:
BOTH GROUNDS CONNECT TO CHASSIS.
WHEN S_1 IS IN THE UP POSITION, IT BYPASSES THE FILTER; WHEN IT IS IN THE DOWN POSITION, IT INSERTS THE FILTER.

Figure 1 A highpass filter and two lowpass filters help reduce or eliminate low-frequency hum and high-frequency noise from audio signals.

inductors' values by an order of magnitude, which would increase the inductors' dimensions and costs. An alternative design approach could use cascaded active-RC filters, which would pave the way for their inclusion into completely integrated composite-audio filters. EDN

REFERENCE

1 Kurzrok, Richard M, "Simple Lab-Built Test Accessories for RF, IF, Baseband, and Audio," *High Frequency Electronics*, May 2003, pg 60.

TABLE 2 FILTER INSERTION LOSS

Frequency (kHz)	Insertion loss (dB)	Frequency (MHz)	Insertion loss (dB)
0.04	45.2	0.1	42.3
0.07	35.4	0.3	60
0.1	29.4	0.5	60
0.2	17.3	1	55.5
0.3	10.9	2	52.2
0.5	5.5	3	51.1
1	2.7	4	56.2
2	2	5	60
5	1.9	10	46.5
10	2.1	25	44
15	2.7	50	40.5
20	4.5	100	39.5
30	11.7	150	45
50	24.5	200	44

Microprocessor's single-interrupt input processes multiple external interrupts

Abel Raynus, Armatron International Inc, Malden, MA

On the lower end of the performance spectrum, many widely available and inexpensive microcontrollers pay for their small pc-board footprints by omitting functions. For example, most low-end processors provide only one external-interrupt input pin and only one address vector in memory for the service routine that processes external IRQs (interrupt requests). However, a project occasionally requires that several interrupt-service programs must process multiple external interrupts from various sources. Cost and inventory constraints may make it undesirable to choose another microcontroller whose only advantage is the availability of a few more interrupt pins.

For example, Freescale Semiconductor's (www.freescale.com) popular Nitron family of flash-memory microcontrollers, such as the MC68HC908QT and QY, offer only one IRQ input pin. You can use one-time-programmable versions of the family, such as the MC68HC705KJ1 or MC68HC705J1A, that offer five external-interrupt inputs but omit some of the family's valuable functions, such as flash memory, built-in analog-to-digital conversion, and an advanced instruction set. You could also select a larger microcontroller, such as the MC68HC908JL3, from the same product family to gain eight external-interrupt inputs at the expense of sig-

nificant increases in cost and pc-board area.

This Design Idea offers an alternative that retains the small processor and adds extra interrupt inputs. The technique involves applying the interrupt signals to an AND gate to generate an IRQ signal and using the microcontroller's inputs to recognize the interrupt's source. For example, consider the four external-interrupt sources in **Figure 1**. If you apply no interrupt signals and if all of the AND gate's inputs rest at logic ones, the IRQ level also remains at logic one. Applying an interrupt signal (a logic-zero level) to any one of four inputs, INT1 through INT4, drives the gate's output to a low level and triggers the interrupt. The interrupt-service routine recognizes the interrupt's source by testing the levels of input pins PA0, PA1, PA4, and PA5 and executing the corresponding interrupt-service routine.

The MC68HC908QY2 microcontroller, IC_1, includes built-in pullup resistors that eliminate the need for external resistors, and you can use an inexpensive and readily available 74LS21 for IC_2. For demonstration purposes, this circuit displays the address of an incoming interrupt by lighting one of four corresponding LED indicators for 3 sec. The software routine in **Listing 1** that assigns a priority to each interrupt uses the standard set of assembler instructions and can apply to any microcontroller. You can download **Listing 1**, as well as the sample's assembler code and its accompanying table of equations (**Listing 2**), from www.edn.com/060302di1. EDN

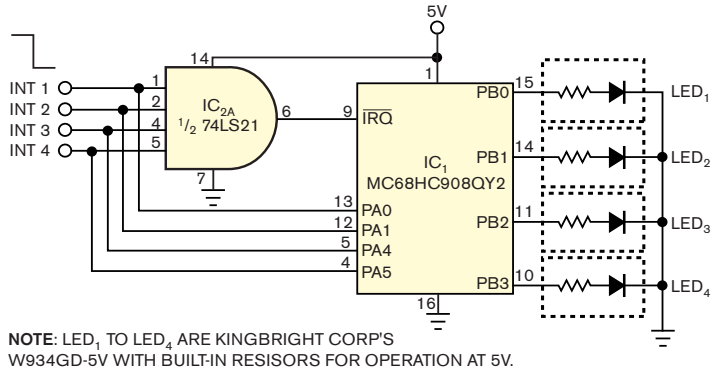


Figure 1 An external AND gate plus a software routine expand a microcontroller's single interrupt input into four inputs.

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READERS SOLVE DESIGN PROBLEMS

Audio-test accessory isolates and matches loads

Richard M Kurzrok, RMK Consultants, Queens Village, NY

Connecting a 600Ω audio circuit to a 50 or 75Ω circuit or test instrument requires an impedance-matching circuit or, when isolation of the circuits is necessary, a transformer. Both approaches offer advantages and disadvantages. A conventional transformer can match impedances with low typical losses of 1.5 dB, provide dc isolation, and operate from either a balanced or an unbalanced, 600Ω primary circuit. A high-quality transformer's passband can accommodate an audio-frequency range of 300 Hz to 15 kHz with minimal amplitude variation. However, transformers that can match 600 to 50 or 75Ω may not be readily available or may command a cost premium.

A minimum-loss, fixed-value impedance-matching circuit, or pad, provides frequency-invariant audio-impedance transformation and can comprise as few as two resistors. Although a pad can provide useful impedance matching, it introduces a significant insertion loss of 14.8 dB for a 600-to-75Ω transformation or 16.6 dB for a 600-to-50Ω transformation, either of which might impose an unacceptable loss of dynamic range.

Part of a suite of test accessories, this low-cost, switchable, dual-impedance transformation circuit comprises a single conventional transformer and two minimum-loss pads (**Reference 1**). A single inexpensive, conventional transformer steps down the 600Ω primary input impedance to an intermediate impedance level of 100Ω (**Figure 1**). Switch S_1 selects a 100 to 50Ω or a 100 to 75Ω minimum-loss pad. Construction of the unit involves noncritical point-to-point wiring, although this design uses a Hammond 1590LB die-cast-aluminum box to provide shielding and a rugged enclosure to support three Amphenol (www.amphenolrf.com) RFX series BNC panel-mounted, insulated-frame input and output jacks. T_1 is a Mouser Electronics (www.mouser.com) 42TM031 audio transformer, and the resistors are 0.5W, metal-film units with ±1% tolerances. With quantity discounts, the overall bill-of-materials cost is less than $20.

To verify frequency response and

TABLE 1 INSERTION LOSS VERSUS FREQUENCY

Frequency (kHz)	Insertion loss (dB) 600 to 50Ω	Insertion loss (dB) 600 to 75Ω
0.1	11.7	8.7
0.3	10	7
0.5	9.5	6.7
1	9.2	6.5
2	9	6.3
5	8.9	6.1
10	8.8	6.1
20	8.8	6
50	8.9	6.1
100	9.5	6.7

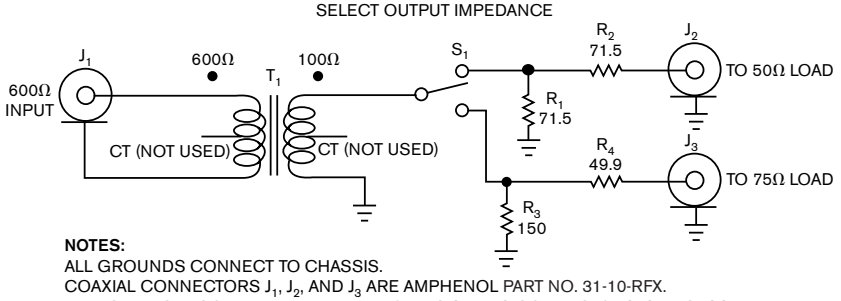

Figure 1 A handful of passive components creates a handy test fixture for matching impedances in audio-test circuits.

DIs Inside

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attenuation in a 600Ω test setup, connect two identical units back to back through their 50 or 75Ω terminals. You obtain the measured data (**Table 1**) for a single unit by halving the 600-to-600Ω transmission-loss measurements.

Calculated insertion loss for the 100 to 50Ω minimum-loss pad is 7.7 dB, and insertion loss for the 100 to 75Ω minimum-loss pad is 4.8 dB. Subtracting these values from the measured losses indicates that the transformer contributes a midband loss of 1.3 to 1.5 dB. Insertion loss due to stray coupling from the selected output port to an unused output exceeds 40 dB. Combining a conventional transformer with two minimum-loss pads takes advantage of the best of both techniques.

The low-cost transformer contributes moderate insertion losses and provides dc isolation and good frequency response. In addition, the transformer's low-frequency roll-off helps reduce 60-Hz hum and low-frequency noise. The electrically isolated input jack allows connection of the transformer's input to balanced or grounded 600Ω sources. EDN

REFERENCE

1 Kurzrok, Richard M, "Simple Lab-Built Test Accessories for RF, IF, Baseband, and Audio," *High Frequency Electronics*, May 2003, pg 60.

One oscillator drives multiple solid-state relays

Juan Ramón Vadillo Pastor, SOR Internacional SA, Saint Quirze Del Valles, Barcelona, Spain

Thanks to a combination of low initial cost and low on-resistance, a conventional electromechanical relay often makes sense for switching large amounts of load current on and off and when proportional control of the load's current or voltage is unnecessary. Low cost and low on-resistance represent the main reasons that relays still enjoy widespread use in the industry. In addition, a relay remains useful for switching high-voltage ac under the control of low-voltage electronics, due to the high degree of isolation between the control and the load circuits.

However, although relay technology has matured and offers proven performance, the relay remains a mechanical device that suffers from wearing out and other failure modes. Electrical endurance of the relay's contacts imposes a limit on the number of switching cycles. When a relay's contact opens, interruption of the current in an inductive load causes a spark that deteriorates the contact's performance. When switching high currents, a relay may reach the end of its operating lifetime in as few as 100,000 actuation cycles.

As an alternative to a conventional relay, a series-connected pair of MOSFETs can replace a contact in an ac circuit (**Figure 1**). A pair of IRF530 devices switches loads in circuits with peak maximum voltages as high as ±100V. Based on the well-known 555 timer, an astable oscillator, IC_1, provides a source of square-wave voltage to drive the MOSFET pairs' gate. Resistors R_1 and R_2 provide charge and discharge paths for timing capacitor C_1. The 555's output stage can sink and source several tens of milliamperes and provide enough current to drive as many as 10 stages' simultaneously operating switch gates, each consuming 5 mA of peak current; the 555's output sinks a maximum of 50 mA at an on-state maximum voltage of 0.75V. The 555's output drives a distribution bus that provides power to an array of pulse transformers, T_1 and T_2. Capacitor C_3 in series with the transformers' primary removes the dc offset voltage that would otherwise appear across the winding.

Selection of the transformer is not critical, and any ferrite-core pulse transformer that can provide gate voltage to the MOSFETs and maintain a safe level of voltage isolation can function in the circuit. For example, you can use C&D Technologies' (www.cdtech.com) 76601/3, which provides a 1-to-1 turns ratio at a primary inductance of 219 µH with 500V-dc interwinding isolation.

Applying a control signal to the base of general-purpose NPN switching transistor Q_3 allows collector current to flow through the primary of its associated transformer. Diode D_2 provides a reverse-current path through the winding. On the secondary side, diode D_1 rectifies the secondary voltage and charges capacitor C_4, which filters the rectified voltage to improve noise immunity and reduce voltage ripple at the MOSFETs' gates. Removing the control signal switches off Q_1 and Q_2. Resistor R_3 provides a discharge path for C_4, allowing the MOSFETs to switch off in approximately 3 msec. For faster turn-off, you can reduce the value of either C_4 or R_3 at the expense of increased ripple on the rectified gate voltage.

Using two series-connected MOSFETs allows bidirectional ac conduction through the pair. When the MOSFETs are off, their parasitic diodes connect in series opposition and thus block conduction. You can select from among a range of MOSFETs to match your application's requirements, but make sure that the voltage you apply to the gates of Q_1 and Q_2 is sufficient to fully switch

both devices into full conduction. The IRF530 has a gate threshold voltage of 3V, but applying a gate-source voltage of 10V ensures low on-resistance. You can adjust the gate-source voltage by altering the transformer's turns ratio or IC_1's power-supply voltage within its 4.5 to 16V rating (**references 1** and **2**). EDN

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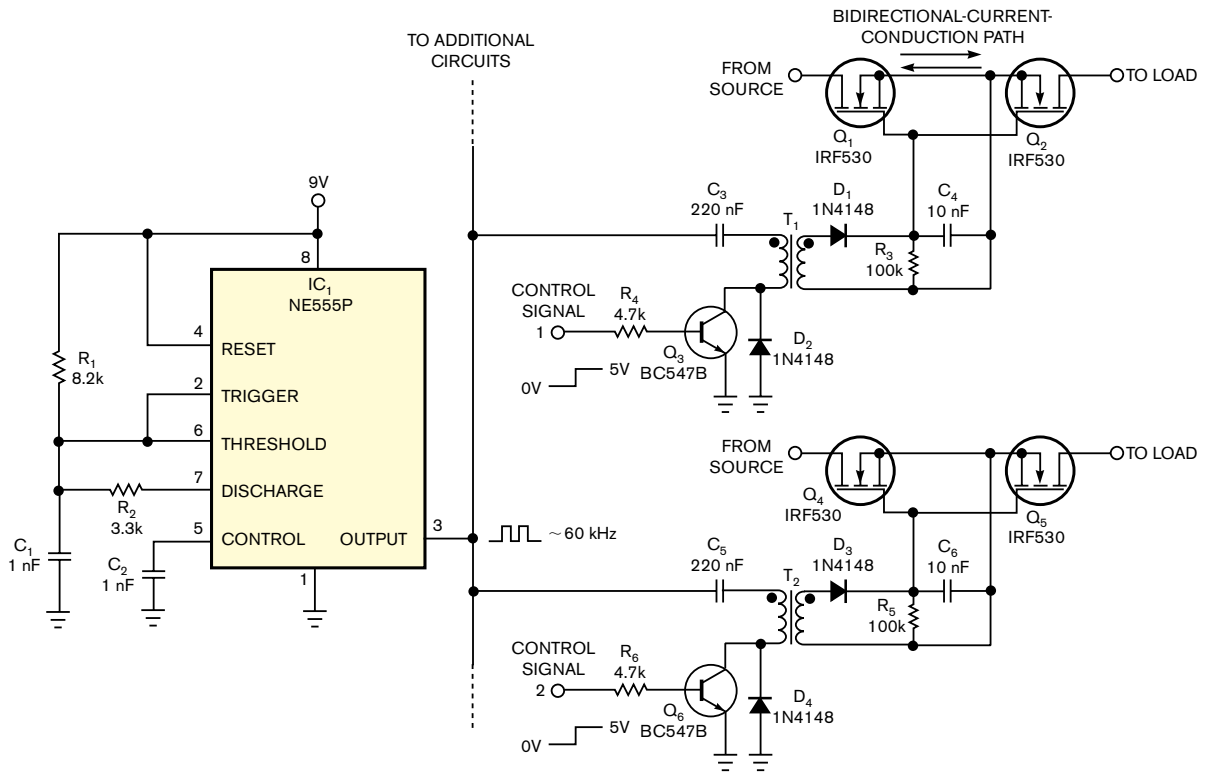

Figure 1 A single 555 oscillator provides square-wave ac gate drive to an array of as many as 15 MOSFET-based solid-state relays.

Low-dropout linear regulators double as voltage-supervisor circuits

William Lepkowski, On Semiconductor, Tucson, AZ

Many low-dropout voltage regulators include an enable-input pin that can also serve as an inexpensive alternative to a voltage-supervisor IC. Although the enable pin normally serves as a means of shutting down the regulator's output to save power, a few discrete components ensure that the regulator's output will turn on and off at appropriate input voltages. Thus, you can use the circuit as a voltage supervisor or as a controlled-characteristic linear-voltage regulator.

A typical low-dropout regulator's internal enable circuit comprises a voltage comparator that determines whether the voltage at the enable pin is either larger or smaller than an internal reference voltage, V_{REF}. Although you can create a low-dropout voltage supervisor by directly connecting the enable pin to the unregulated input voltage, this circuit's turn-on and turn-off voltages equal the reference voltage, which typically falls below the minimum operating voltage that most ICs powered by the regulator's output require.

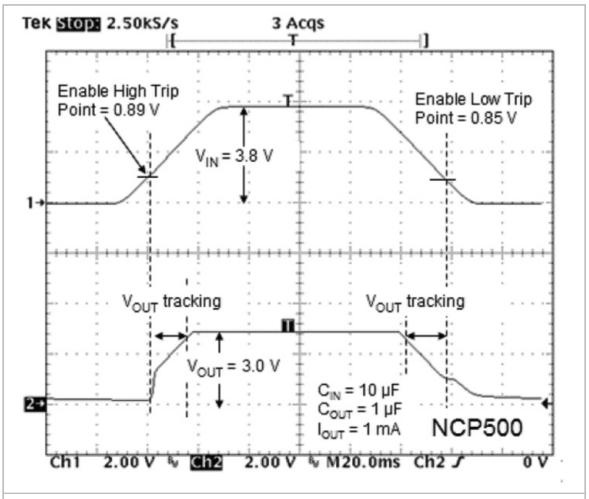

Figure 1 Connecting a low-dropout regulator's enable pin directly to the unregulated voltage input forces the output voltage to track the input voltage during the regulator's turn-on and turn-off intervals.

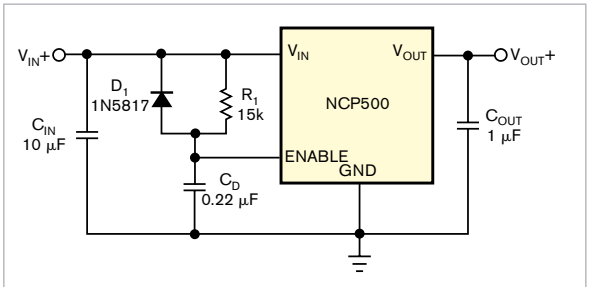

Figure 2 An alternative to directly connecting the regulator's input and enable pins, this "conventional" modification uses a resistor and a capacitor to delay the regulator's turn-on time. The diode eliminates the power-down delay interval.

In addition, directly connecting the enable pin to the unregulated input doesn't provide a turn-on delay to ensure that the input voltage has reached a value higher than the low-dropout regulator's dropout voltage. The directly connected circuit has unsatisfactory power-up and power-down characteristics (**Figure 1**). As a first-order improvement, you can enhance the circuit's performance by adding R_1, C_{IN}, and D_1 to provide a start-up delay for the voltage regulator's enable pin (**Figure 2**). Unfortunately, the external delay network improves the output's rising-edge characteristic, but its falling edge continues to track the input voltage (**Figure 3**).

You can solve the circuit's shutdown problem by replacing the single resistor with a voltage-divider network (**Figure 4**). Resistor R_2 raises the switching threshold of the regulator's enable pin and "tricks" the enable comparator into turning on at a higher voltage. The regulator's output then exhibits an adequate start-up delay and

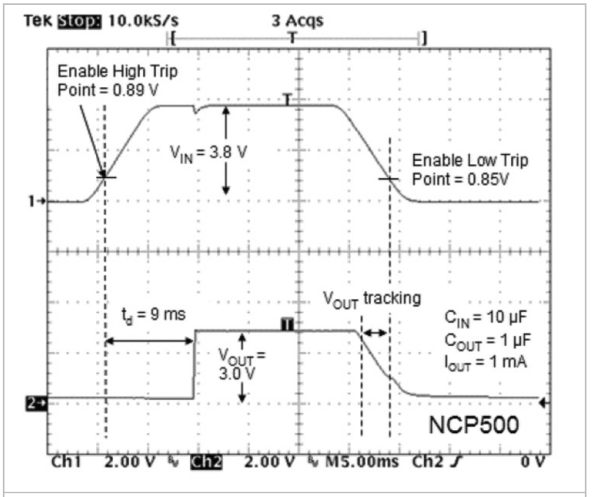

Figure 3 The added components in Figure 2 eliminate the problem of rising-edge output-voltage tracking. However, the falling-edge output voltage still tracks the input voltage.

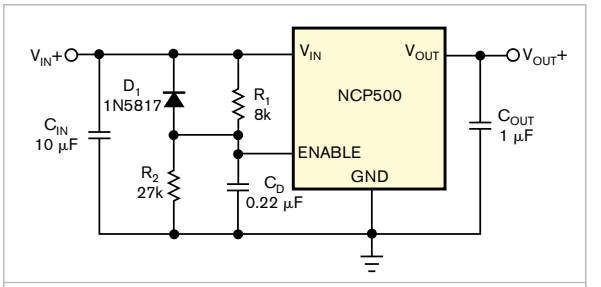

Figure 4 Resistor R_2 increases the enable pin's switching threshold voltage.

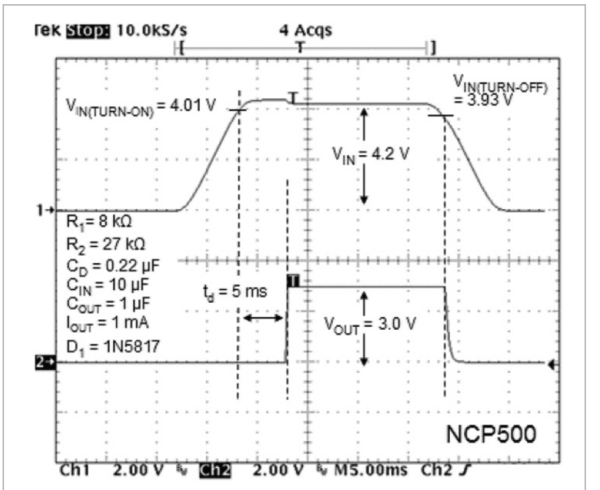

Figure 5 The addition of R_2 in Figure 3 solves the falling-edge problem, and shutdown occurs immediately after the input voltage drops too low. The regulator's output switches on only after sufficient voltage is present at its input.

cleanly switches on and off (**Figure 5**).

You can use **Equation 1** to calculate the values of resistors R_1 and R_2 to alter the enable pin's threshold voltage in the circuit in **Figure 4**.

$$V_{IN(TURN-ON)} \simeq \left[\left(2 \times V_{EN(RISING)}\right) - V_{EN(FALLING)}\right] \times \left(1 + \frac{R_1}{R_2}\right), \quad (1)$$

where $V_{IN(TURN-ON)}$ is the user-defined turn-on voltage, $V_{EN(RISING)}$ is the enable pin's rising-edge trip-point voltage, and $V_{EN(FALLING)}$ is the enable pin's falling-edge trip-point voltage. For example, $V_{IN(TURN-ON)}=4V$, $V_{EN(RISING)}=0.89V$, and $V_{EN(FALLING)}=0.85V$. To prevent the regulated output voltage from tracking the input, set the minimum value of $V_{IN(TURN-ON)}$ to $V_{OUT}+V_{DROPOUT}$, where $V_{DROPOUT}$ is the dropout voltage.

$$\frac{R_1}{R_2} \simeq \frac{V_{IN(TURN-ON)}}{\left[\left(2 \times V_{EN(RISING)}\right) - V_{EN(FALLING)}\right]}^{-1} \simeq \frac{4}{\left[\left(2 \times 0.89\right) - 0.85\right]}^{-1} \simeq 3.3. \quad (2)$$

If you select a value of 8 kΩ for R_2, then $R_1=3.3\times R_2$, or approximately 27 kΩ.

Equation 1 calculates only approximate values for the voltage-divider resistors, which may vary slightly depending on the voltage regulator's characteristics. If the resistors' values are too low, the regulated output tracks the input, a problem that you can easily solve by increasing the value of R_1. Also, R_1 and C_D determine the regulator's turn-on delay time, and C_D's capacitance should ideally be 0.01 to 0.47 µF. Too large a value increases the discharge time and reduces the circuit's effectiveness as a voltage supervisor. EDN

External components provide true shutdown for boost converter

Navid Mostafavi, Maxim Integrated Products Inc, Sunnyvale, CA

The step-up switching-converter circuit in **Figure 1** presents a familiar problem: If you shut down boost converter IC_1 by pulling its $\overline{SHDN}$ input low, external inductor L_1 and forward-biased Schottky diode D_1 allow the load to continue drawing current. For battery-powered applications that present a heavy load—300 mA, for example—this unwanted dc-current path may quickly drain the battery. Adding an N-channel MOSFET, Q_1, and a 100-kΩ resistor, R_1, solves the problem by opening the unwanted current path during shutdown. The resulting circuit is suitable for battery-powered-system applications in which a microcontroller handles the power management.

Asserting a low logic level on the $\overline{SHDN}$ input simultaneously shuts down the switching converter, a MAX756, and turns off the MOSFET, thereby blocking load current by removing the load's ground connection. When the $\overline{SHDN}$ signal deasserts, the 100-kΩ pullup resistor turns on the MOSFET by pulling the MOSFET's gate high. With its ground reconnected, the load then draws current from the activated boost-converter circuit.

For optimum results at high load currents, select a logic-level MOSFET for Q_1 that presents a reasonably low on-resistance. The MOSFET's drain-to-source breakdown voltage should also be able to withstand at least twice the maximum output voltage you expect from the boost converter. If necessary, you can reduce the MOSFET's effective on-resistance by connecting two or more MOSFETs in parallel. EDN

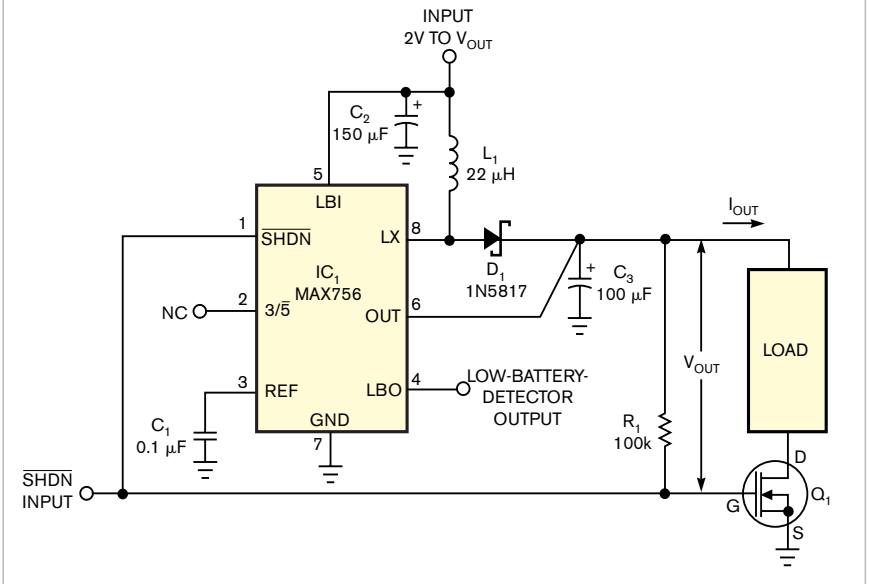

Figure 1 Adding R_1 and MOSFET Q_1 to this step-up-converter circuit enables the $\overline{SHDN}$ control to impose a "true" shutdown that blocks load current when boost converter IC_1 switches off.

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

On/off buffer switches analog or digital signals

Liviu Pascu, Kepco, Flushing, NY

Many applications require a method of switching an analog or a digital signal on or off under digital control. A "wish list" of specifications for such a switch might include attenuation of less than 90 dB when the switch is in its off-state, distortion of no more than 0.002% when the switch is in its on-state, and the ability to respond to an on or an off command in 10 µsec or less. In addition, the circuit should accommodate positive- or negative-going signals, and no turn-on or turn-off overshoot should occur for either signal polarity. The list might also require that the circuit's control input must accept digital signals from most logic families and that the circuit's SNR should exceed 90 dB.

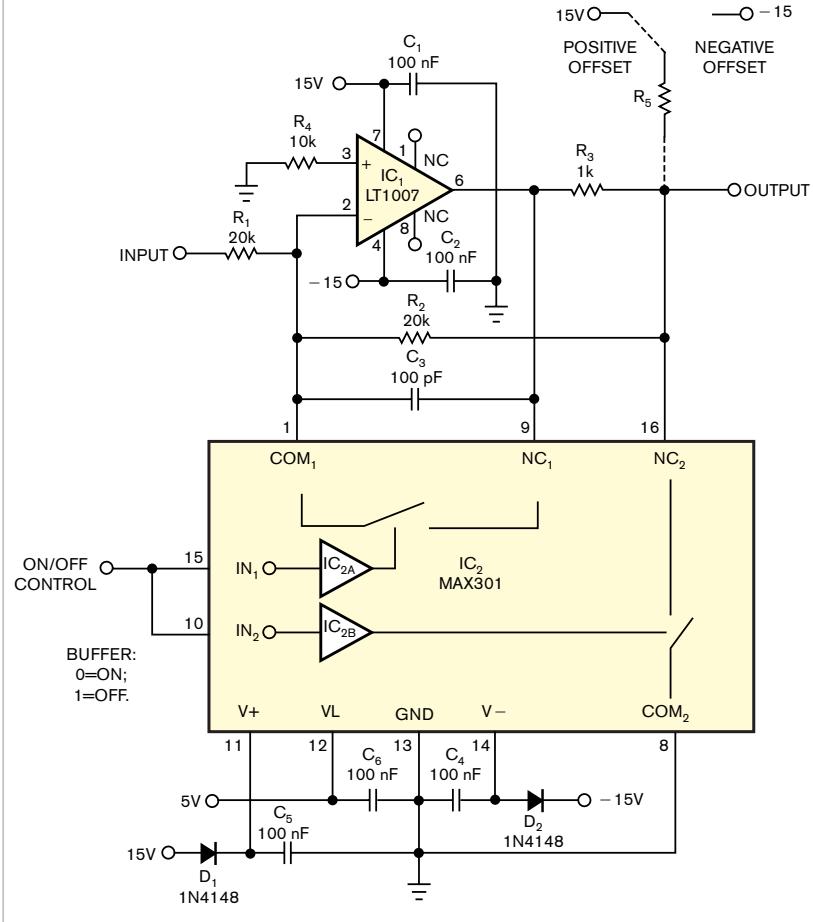

Figure 1 This buffered switch can accommodate either analog or digital signals.

The circuit in **Figure 1,** comprising IC_1, a low-noise, high-speed, precision Linear Technology LT1007 operational amplifier and IC_2, a Maxim MAX301 dual SPST, normally open analog switch, fulfills these requirements. In the circuit, V_{IN} is the input voltage, and V_{OS} and I_{OS} represent operational amplifier IC_1's voltage and current offsets of either polarity. I_{OFF} represents the off-state leakage current of either section of analog switch IC_2. In the buffer circuit, $R=R_1=R_2$, and $R_4=R/2$. Hence, $\Delta R=(R_1\times R_2)/(R_1+R_2)-R_4$.

If all resistors were identical in value, ΔR would equal zero. However, each resistor exhibits its own tolerance error, and the equation for ΔR expands to:

$$\Delta R = \frac{(R_1(1+e_1))\times((R_2)(1+e_2))}{(R_1(1+e_1))+((R_2)(1+e_2))} - \left(R_4(1+e_4)\right),$$

where e_1 through e_4 are maximum tolerance errors of ±1%. Worst-case values for ΔR occur when the tolerance values e_1 and e_2 for R_1 and R_2 are of the same sign and e_4 for R_4 has the opposite sign:

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$$\Delta R = \pm\left[\frac{R(1+|e|)}{2} - \frac{R(1-|e|)}{2}\right].$$

Simplifying further, $\Delta R = \pm R\,|e|\} = \pm\{(0.01)R\}$ when you use 1%-tolerance resistors for R_1, R_2, and R_4. The combination of the resistors' tolerances with the operational amplifier's internal errors and leakage effects from switches IC_{2A} and IC_{2B} determines the buffer's accuracy. When the circuit is on, both IC_{2A} and IC_{2B} are open. The following **equation** defines the circuit's output voltage:

$$V_{OUT(ON)} = -\left\{\left[\frac{V_{IN} - V_{OS} - (I_{OS} \times \Delta R)}{R_1}\right]\right\} - (I_{OFF}) \times R_2.$$

Simplifying further, you can calculate $V_{OUT(ON)}$ as: $V_{OUT(ON)} = -(V_{IN}) + V_{OS} + ((I_{OS}) \times (\Delta R)) + ((I_{OFF}) \times (R))$.

Most of today's solid-state switches present an I_{OFF} of less than 1 nA, and you can select an op amp for IC_1 whose V_{OS} is less than 50 µV and whose I_{OS} is less than 50 nA. Thus, for the resistor values in **Figure 1**, the maximum error for the amplifier's on-state is approximately 80 µV, or 0.0008%, when referred to a 10V nominal output. You can determine the minimum allowable value of the amplifier's load resistance by solving the following **equation**:

$$R_{LOAD} > \left(\frac{R_3}{\frac{V_{SAT}}{V_{OUT(MAX)}} - \frac{R_3}{R_2} - 1}\right),$$

where V_{SAT} represents the op amp's maximum saturated output voltage—usually, 13.5V for ±15V power-supply voltages. For example, using the resistor values in **Figure 1** and assuming a maximum output voltage of 10V, you can calculate a minimum allowable load resistance of 3.3 kΩ.

Also, I_{AMP}, the current from IC_1, should be less than the device's specified maximum current output: $I_{AMP} = (V_{OUTMAX}) \times [(1/R_2) + (1/R_{LOAD})]$.

Using these values, you can determine that I_{AMP} is 3.5 mA, which is less current than most op amps as sources deliver. When the amplifier is off, switches IC_{2A} and IC_{2B} are closed. In this state, the worst-case output occurs for V_{INMAX}. IC_1's offset errors are negligible with respect to the full-scale input voltage. Therefore, for the real case in which the on-resistance of IC_{2A} and IC_{2B} is much less than the load resistance, the following **equation** defines the circuit's output voltage: $V_{OUTOFF} = -[(V_{IN} \times R_2 \times R_{ON} \times R_{ON})/(K_1 + K_2 + K_3 - K_4)]$, where $K_1 = R_1 \times R_2 \times R_3$, $K_2 = R_1 \times R_3 \times R_{ON}$, $K_3 = R_1 \times R_{ON} \times R_{ON}$, and $K_4 = R_1 \times R_2 \times R_{ON}$. For $R_1 = R_2 = R$ and $R_{ON} << R$, and $R_{ON} << R_3$, the **equation** simplifies to: $V_{OUTOFF} = -[(V_{IN} \times R_{ON} \times R_{ON})/(R \times R_3)]$.

Many of today's analog switches present a maximum 20Ω on-resistance, and, using the resistor values in **Figure 1** and an input voltage of 10V, you can calculate that output voltage to be approximately 200 µV, or 0.002%, when referred to a 10V nominal output. Amplifier IC_1's slew rate limits the circuit's dynamic behavior, because analog switch IC_2 generally switches in much less than 1 µsec. Using an operational amplifier with a slew rate of 1.5V/µsec yields a circuit-response time of 10 µsec.

For applications that require unipolar outputs when the amplifier is in its off-state, you can add a known output-offset voltage by connecting resistor R_5 between the buffer's output and the power-supply voltage of the same polarity as the desired offset voltage. Note that IC_1's output must be able to sink current. Adding resistor R_5 doesn't affect the circuit's output voltage in its on-state because the closed-loop gain lowers the amplifier's output impedance.

To analyze the circuit's offset output voltage, assume that IC_{2A} and IC_{2B} present an on-resistance that's much less than R_{LOAD}, R_2, and R_5. The following **equations** define the circuit's positive and negative offset-output voltages, $V_{OUT(OS)}$ and $-V_{OUT(OS)}$, respectively:

$$V_{OUT(OS)} = \left[+|V_S| \times \left(\frac{R_{ON}}{R_5}\right)\right] + \left[|V_{IN}| \times \left(\frac{R_{ON}}{R_2}\right) \times \frac{R_{ON}}{R_3}\right].$$

$$-V_{OUT(OS)} = \left[-|V_S| \times \left(\frac{R_{ON}}{R_5}\right)\right] - \left[|V_{IN}| \times \left(\frac{R_{ON}}{R_2}\right) \times \frac{R_{ON}}{R_3}\right].$$

To make the offset voltage less dependent on the input signal, calculate the maximum value for R_5 as:

$$R_5 < \frac{I}{10} \times \frac{V_S}{V_{IN}} \times \frac{R_2}{R_{ON}} \times R_3.$$

Using the resistor values in **Figure 1**, solving this **equation** produces a minimum reliable offset voltage of 2 mV; the value of R_5 must be 150 kΩ or less. The maximum current-sinking ability of IC_1 determines the minimum value of R_5. EDN

Single switch serves dual duty in small, microprocessor-based system

Steve Hageman, Windsor, CA

Traditional control-system designs use separate switches to control power and various system functions, but adding a few components to a small, microprocessor-based system can combine a control function with the system's on/off switch. For example, you can design a system to display relative humidity and temperature (**Reference 1**). This small, battery-powered system requires a microprocessor-controlled on/off power switch, which you implement with a pushbutton, and a function switch to change the display from degrees Celsius to degrees Fah-

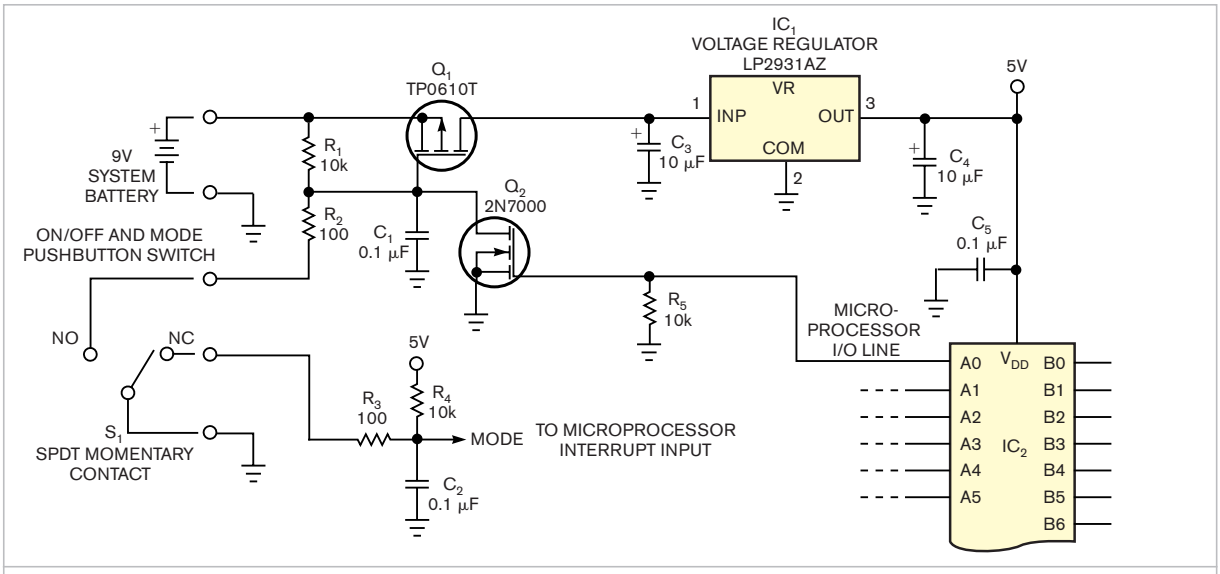

Figure 1 A single pushbutton switch can control power and select among operating modes in a simple microprocessor-based system.

renheit, which you implement as a toggle switch. From ease-of-use and total-cost perspectives, combining these two functions in a single switch makes sense.

Figure 1 shows a circuit for this application. Initially, Q_1, a P-channel MOSFET, is off because R_1 holds Q_1's gate-to-source voltage at 0V. No input reaches voltage regulator IC_1, and, thus, the system's microprocessor, IC_2, also remains off. When the operator presses the normally closed momentary-contact pushbutton switch, S_1, current flows through R_1 and R_2 to ground, developing sufficient gate-to-source voltage to turn on Q_1 and apply power to voltage regulator IC_1 and the microprocessor. Capacitor C_1 debounces the switch contact and ensures that Q_1 remains on long enough to start the microprocessor, regardless of how quickly the user presses and releases the switch. In addition, as its final task, the start-up firmware initializes the system's LCD, thus reinforcing the operator's tendency to hold the power switch in its on position long enough to ensure full start-up.

Immediately after the microprocessor powers up, it begins executing its firmware and turns on Q_2, an N-channel MOSFET, by delivering a logic one of more than 3V to Q_2's gate. In turn, Q_2 keeps Q_1 switched on, and the system runs under software control. If the operator again presses the on/off button, Q_1 remains on, and the microprocessor continues to run but pulls its mode line high. The mode line drives an interrupt input pin, and the software can use the interrupt as a toggling function or to access a wraparound, multiple-choice menu. After a suitable preprogrammed time interval, the microprocessor system turns itself off by placing a logic zero on Q_2's gate. In turn, Q_2 switches off Q_1 to remove power from the system. EDN

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Isolated-FET pulse driver reduces size, power consumption

José M Espí, Rafael García-Gil, and Jaime Castelló,
Electronic Engineering Department, University of Valencia, Spain

Three-phase controlled rectifiers and inverters, matrix cycloconverters, and cascaded power stages typically comprise large numbers of power transistors, each with its own driver circuit. The circuit in **Figure 1** drives a capacitive-input power device, such as a MOSFET or an IGBT (insulated-gate bipolar transistor) with pulses of all duty cycles at frequencies of 1 to 200 kHz. A single transformer provides galvanic isolation, and the circuit consumes little power from its 15V primary-side power supply. Tested satisfactorily using several MOSFETs and IGBTs with input capacitances as high as 5 nF, the driver can accommodate higher current power transistors by resizing the driver's transistors and coupling transformer and a few passive components.

Transistors Q_1 and Q_2 transmit pulses of approximately 1-µsec duration through coupling transformer T_1 to transistors Q_3 and Q_4, which respectively charge and discharge power transistor Q_5's gate-source input capacitance. The charging pulse that Q_1 produces begins on the rising edge of the drive-control signal, and the discharge

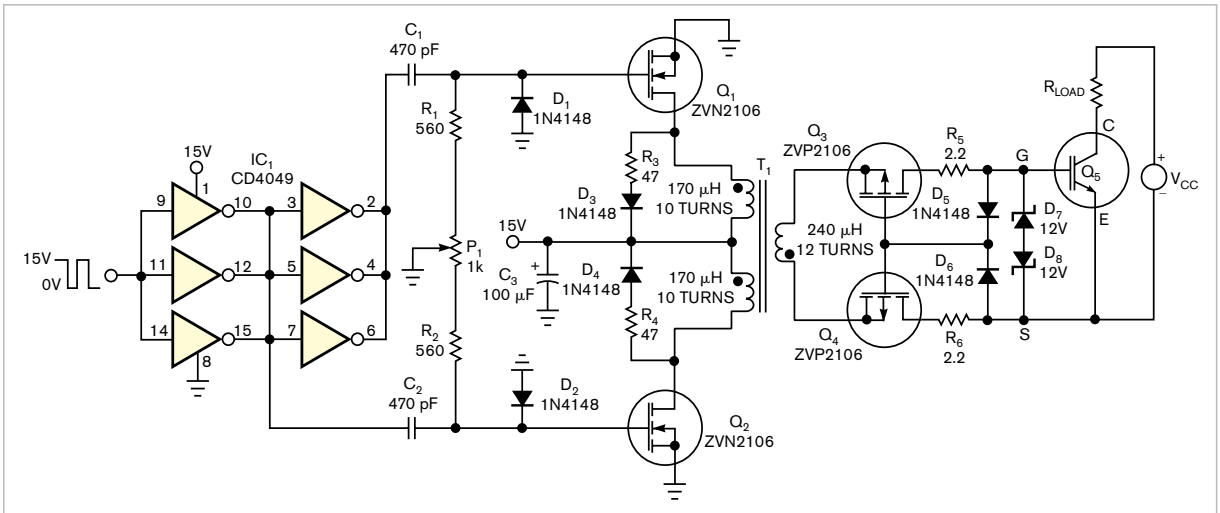

Figure 1 The isolated pulse driver transmits all duty cycles and consumes energy only during the gate charge and discharge processes.

pulse that Q_2 produces begins on the falling edge of the control signal. Differentiator circuits comprising C_1, R_1, a portion of potentiometer P_1, C_2, R_2, and the remaining portion of P_1 set the durations of the charge and discharge pulses. If necessary, adjusting P_1's setting alters the balance of the positive and negative charge and discharge voltages that Q_5's gate receives.

Transistors Q_3 and Q_4, respectively, transmit pulses to charge or discharge Q_5's input capacitance and then switch off, producing a high impedance across Q_5's input capacitance so that Q_5's gate voltage doesn't change, except for discharging slowly due to small leakage currents. Thus, the driver circuit consumes power only during the short intervals of the gate-to-source charge and discharge processes.

When transistors Q_1 through Q_4 switch off, resistor and diode pairs R_3, D_3, R_4, and D_4 form a path for transformer T_1's demagnetization current. Although they're reverse-biased most of the time, diodes D_5 and D_6 form a peak-amplitude discriminator, configured as a logical-OR circuit, to ensure that gate voltages at Q_3 and Q_4 always equal or exceed the voltage at the positive terminal of Q_5's gate-to-source capacitance.

Resistors R_5 and R_6 limit charge and discharge rates for Q_5's gate-to-source capacitance and can vary depending on Q_5's drive characteristics. Transformer T_1 comprises a Philips RM5/I core of 3E5 ferrite material with a center-

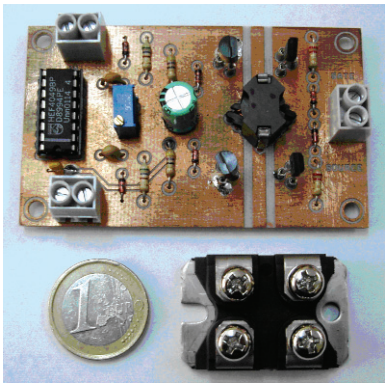

Figure 2 A top view of the isolated gate driver's prototype version shows that an isolation barrier interrupts the ground plane beneath transformer T_1 (upper right center).

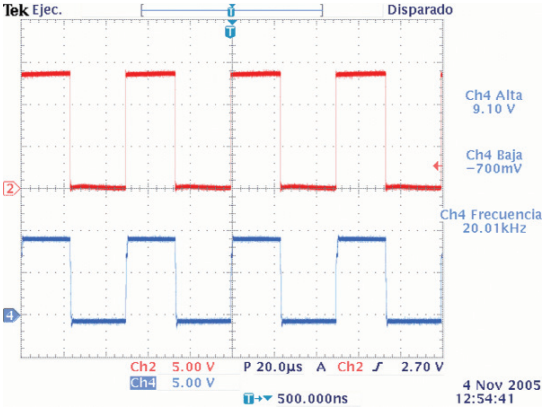

Figure 3 The top trace shows the driver-control voltage, and the bottom trace shows the gate-source voltage of an APT40GF120JRD IGBT, Q_5, at 20 kHz. You can use potentiometer P_1 to adjust the 9.1 and 20.7V high and low gate-to-source levels, respectively.

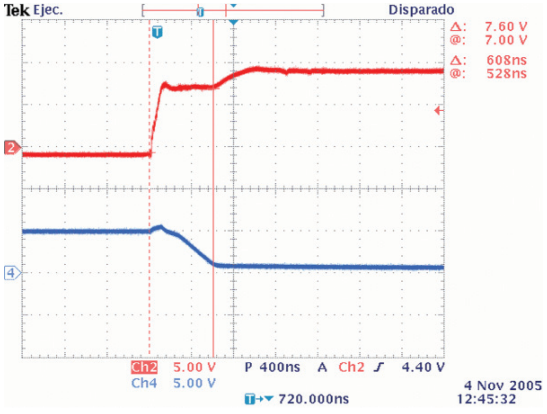

Figure 4 The top trace shows the driven transistor's gate-to-source voltage, and the bottom trace shows its collector-emitter voltage, which a probe attenuates. The transistor's load comprises a resistor that connects to a power supply.

tapped, 20-turn primary winding and a 12-turn secondary winding, both fabricated from 0.2-mm-diameter, 0.008-in, AWG #32 magnet wire.

When transistor Q_1 switches on, it induces a positive voltage in T_1's secondary winding that switches on P-channel MOSFET Q_3 and drives Q_4's internal body diode into conduction to begin charging Q_5's gate-to-source capacitance. Q_3's on-channel resistance primarily determines the charging rate. Charging ends either when the pulse terminates or when Q_5's gate-to-source voltage approximates T_1's secondary voltage minus Q_3's gate-threshold voltage.

Next, Q_3 switches off, allowing the charging current to decay to zero and the capacitance to reach its maximum positive charge. When Q_1 switches off, transformer T_1's magnetizing current resets through R_3 and D_3. The voltage at T_1's secondary winding goes slightly negative to balance the core's volt-second characteristic, which forward-biases Q_3's body diode without current, and Q_4's body diode blocks the discharge of Q_5's gate-to-source voltage.

The negative voltage you apply to Q_4's gate cannot switch on Q_4 because diode D_5's forward-voltage drop sets Q_4's gate voltage higher than the voltage at Q_5's gate. Thus, Q_5's input capacitance remains charged, and the reset path presents high impedance to this capacitance. When Q_2 switches on, the negative voltage that appears on T_1's secondary turns on Q_4 and starts the discharge process, which ends when Q_4's source-to-gate voltage equals its threshold level or when the pulse terminates. Then, Q_4 turns off, and Q_5's gate-to-source capacitance reaches its minimum negative voltage. When Q_2 turns off, T_1's magnetizing current resets through D_4 and R_4, Q_4's body diode conducts, and Q_3's body diode blocks Q_5's gate-to-source voltage. Diode D_6 applies a high voltage to Q_3's and Q_4's gates to ensure that the reset voltage at T_1's secondary doesn't drive Q_3 into conduction. Thus, all transistors remain off, and Q_5's gate-to-source capacitance remains discharged. When Q_1 next switches on, the sequence repeats.

Figure 2 shows the driver prototype compared with a €1 coin and a power transistor. The transistor, an Advanced Power Technology APT40GF-120JRD, combines an IGBT and a FRED (fast-recovery epitaxial diode) that operates at a maximum of 1200V and 60A with a gate-to-source capacitance of 4 nF. The transistor comes in a JEDEC SOT-227 package measuring approximately 1.5×1 in. (38×25 mm). **Figures 3** and **4** show experimental waveforms for the circuit of **Figure 1** to drive IGBT Q_5 at 20 kHz. The turn-on delay is approximately 600 nsec, and the total current consumption is 22 mA for a power consumption of 0.33W. When driving transistors that present a lower gate-to-source capacitance, the circuit's turn-on delay and power consumption both decrease. EDN

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CPLD automatically powers itself off

Rafael Camarota, Altera Corp, San Jose, CA

Most of today's CPLDs (complex programmable-logic devices) feature reduced-power operating modes, but, when the system is not in use, a complete shutdown that conserves battery power remains the ultimate power-reduction goal of many designers. Figure 1 shows how you can add a few discrete components to a CPLD—in this example, an Altera EPM570-T100—to implement a battery-powered system's power-down circuit. An external P-channel MOSFET, Q_1, an International Rectifier (www.irf.com) IRLML6302 or equivalent, serves as a power-control switch for the CPLD, IC_1, and other components in the system. The CPLD and an array of switches control the MOSFET's gate, applying bias that switches on Q_1 whenever a user presses a switch. The CPLD includes an embedded timer that monitors switches and system activity. After a specified period of inactivity, the timer disables the MOSFET's gate drive, powering down the CPLD and other components connected to the MOSFET.

Q_1's source connects to the battery's positive terminal, and its drain connects to IC_1's $V_{CC(INT)}$, $V_{CC(IO1)}$, and $V_{CC(IO2)}$ power pins and other components that require power-down control. When power switches off, a 1-kΩ pullup resistor, R_3, keeps Q_1 off by maintaining its gate at a gate-to-source voltage of 0V. When you turn off IC_1, it presents a leakage path to ground through the CPLD's power-down pin. The EPM570-T100 includes hot-socket protection that limits the current available from any user-accessible device-I/O pin to less than 300 µA. Thus, even in the worst case, the voltage that the I/O pin develops across R_3 doesn't reach the FET's minimum gate-threshold turn-on voltage of 0.7V.

Pressing any switch creates a current path through the switch's contacts and its associated diode, which in turn develops approximately 2.3V of gate-source bias across R_3—more than enough to turn on Q_1 and to power up IC_1 in approximately 100 µsec. When you actuate the mechanical switches, they exhibit a minimum on-time of at least 3 msec, whereas a typical human operator's minimum press-and-release operation consumes at least 30 msec. During these relatively slow response times, the CPLD can turn on, resetting its internal circuitry and asserting its power-down pin to a logic zero that turns on Q_1 before the operator can release the switch.

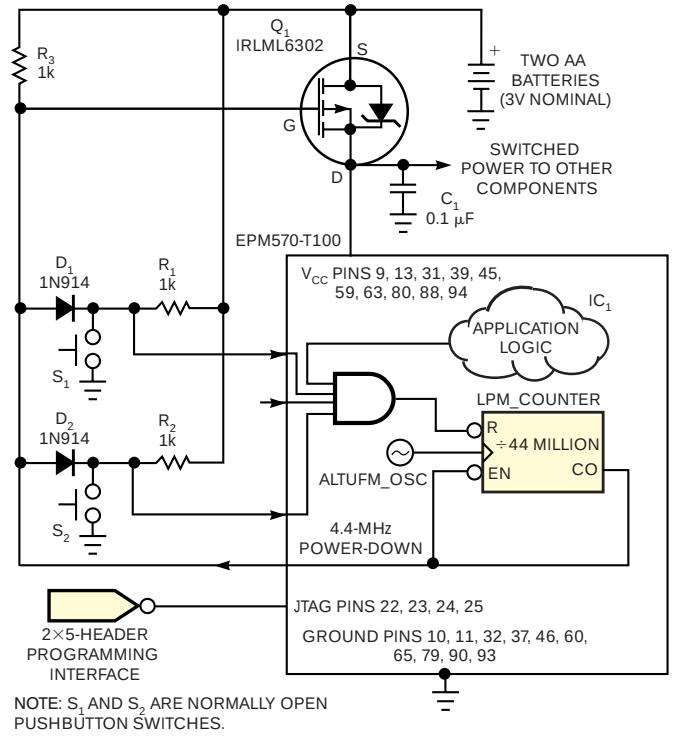

Figure 1 A few external components and internal logic blocks enable a CPLD circuit to switch itself off after a predetermined interval.

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In addition to user-specified application logic (not shown), the CPLD's power-control logic adds a pair of standard parameterized, library-macro circuits that Altera's (www.altera.com) Quartus II development tools generate. An internal 4.4-MHz±25% oscillator, Altufm_osc, drives a modulo-44-million LPM (library-parameterized-module) counter. A logic-low signal that the CPLD's application logic produces or closing any switch resets the counter. When you reset the counter, its carry-out signal goes low and drives the external power-down pin. An inverted version of the carry-out signal re-enables the LPM counter once you remove the reset.

If you leave all switches open and the application logic becomes inactive, the counter counts to 44 million in approximately 10 sec, and the internal carry-out signal goes high, disabling the counter and holding the carry-out signal high. In turn, the power-down pin rises toward V_{CC}, turning off Q_1 when the voltage on the power-down pin reaches 2.3V. Removing power from the CPLD places the power-down pin in the tristate, or disconnected, mode, and R_3 keeps Q_1 off.

You can use JTAG-compliant commands to configure the EPM570-T100 with a download cable you connect to a manufacturer-defined 10-pin header. The process requires that you press an external switch before, during, and shortly after configuration to ensure that the CPLD receives power throughout the configuration process. You can set the inactivity time-out to any desired value by changing the counter's modulus. Although power, ground, and JTAG signals use specific device pins, you can assign any general-purpose CPLD I/O pins as inputs for switches and as the power-down output.

If your application requires a matrix of pushbutton switches, you can use only n diodes to configure an n×m switch matrix for efficient power-up detection (Figure 2). In this example, rows of switches connect to the MOSFET's gate through diodes D_1 through D_4. Resistors R_8 through R_{11} provide a ground path for each column of switches and carry current only during key closures, holding the column inputs low while waiting to minimize power-supply current drain.

When a user presses any switch, Q_1's gate goes low, turning on the CPLD. A fast CPLD-power-up routine allows the application to scan the switch matrix's rows and columns and determine which switch a user pressed before the user can release the switch. In this application, the row signals reset the LPM counter's inactivity timer. EDN

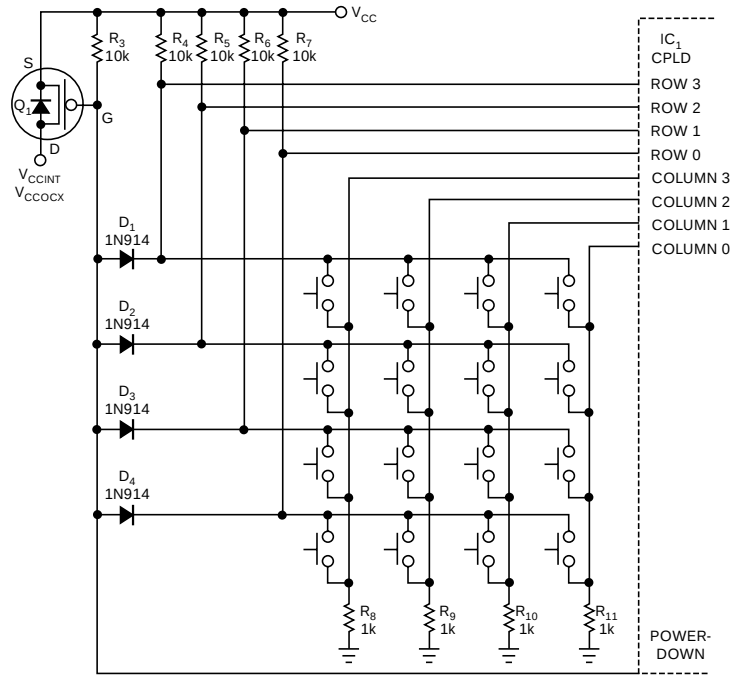

Figure 2 A keypad matrix expands the CPLD circuit's control capabilities and retains the circuit's automatic power-off function.

Amplifier removes common-mode noise on RGB differential-video-transmission line

Tamara Papalias and Mike Wong, Intersil Corp

Comprising four twisted pairs within a durable external sheath, Category 5 network cable offers a common and cost-effective choice for transmitting component-video signals. Three of the pairs can carry RGB video signals, and the fourth pair carries audio, synchronization, and other transmissions. Unfortunately, Category 5 cable lacks shielding, and thus it's somewhat vulnerable to common-mode coupling that induces equal voltages in each of the cable's conductors. As a first line of defense against common-mode problems, you can configure RGB signals as differential voltages, but any voltage difference between the ground references of the twisted-pairs' drivers and receivers results in a common-mode signal on each of the received lines.

Common-mode-noise voltages limit transmission quality of video signals. This Design Idea shows how you can use a single operational amplifier to

minimize common-mode signals' effects on differential-component-video receivers. In Figure 1, the receiver circuits' ground terminals (in red) show that the ground-reference voltages of each of the RGB differential signals differ from those present at the drivers. To maintain signal quality and minimize reflections, each video-signal twisted-pair transmission line terminates in 100Ω. For example, resistors R_{35} and R_{37} terminate the R+ line, and R_{36} and R_{38} terminate the R− line. Meanwhile, the G and B termination circuits are identical. Any common-mode voltage on the R-signal pair appears at the junction of R_{37} and R_{38} and across R_{39}.

To create a common-mode cancellation voltage, operational amplifier IC_1 sums and inverts the signals on all three or four signal-line pairs. For example, adding the R+ and R− signals cancels their differential-voltage components and doubles the common-mode voltage that each line contributes. Capacitors C_1 and C_2 provide ac coupling for the circuit's input and output, respectively. The output from IC_1 applies a common-mode bias voltage through a matched pair of 30-kΩ resistors, R_{42} and R_{43}, to the R+ and R− receiver network. Close tolerances for R_{42} and R_{43} ensure that the differential voltages delivered at R_{OUT+} and R_{OUT-} closely balance with respect to the inputs' common-mode

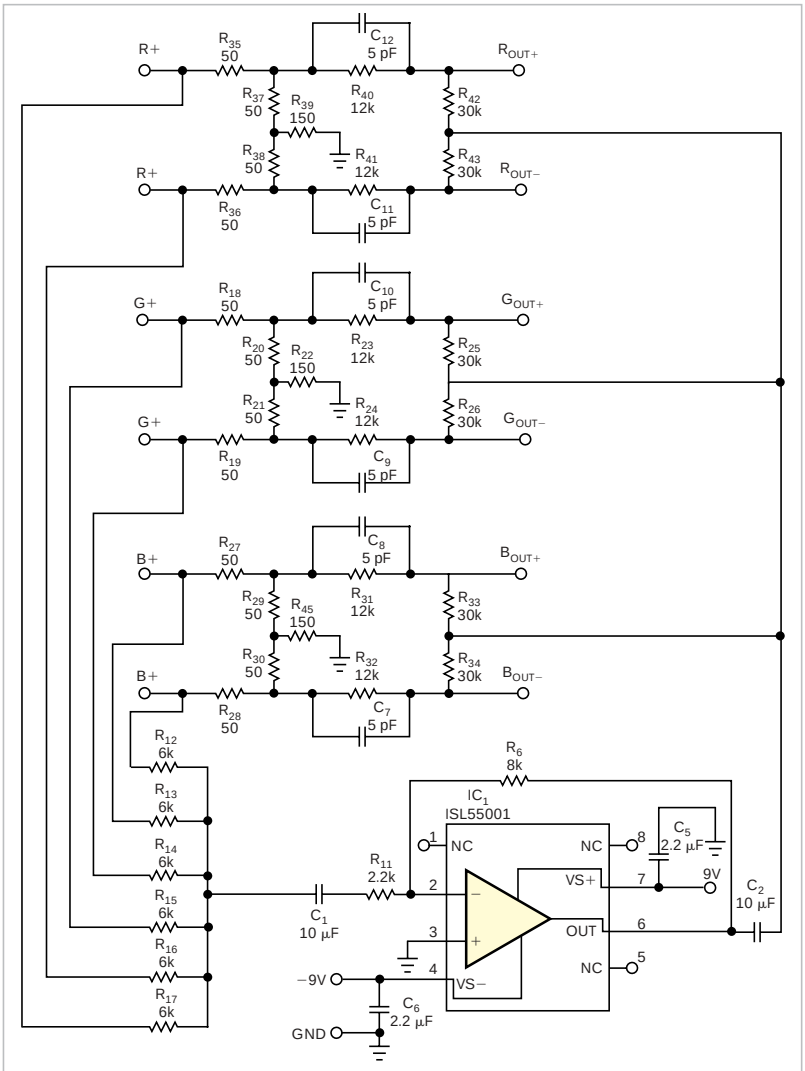

Figure 1 A common-mode-cleanup circuit reduces noise pickup on unshielded Category 5 differential-video signals.

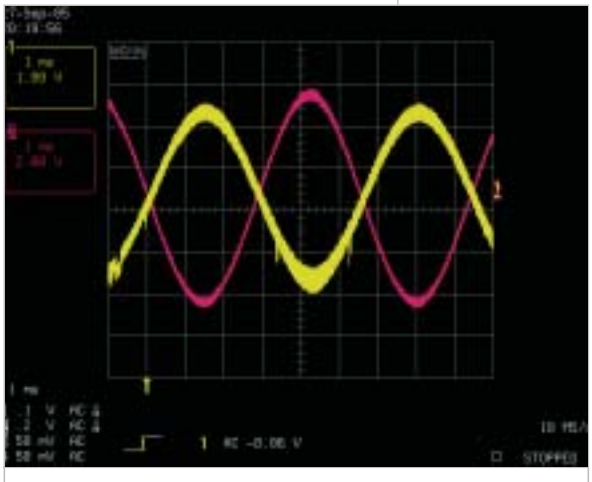

Figure 2 The common-mode signal (yellow trace) heavily influences the video signal (pink trace).

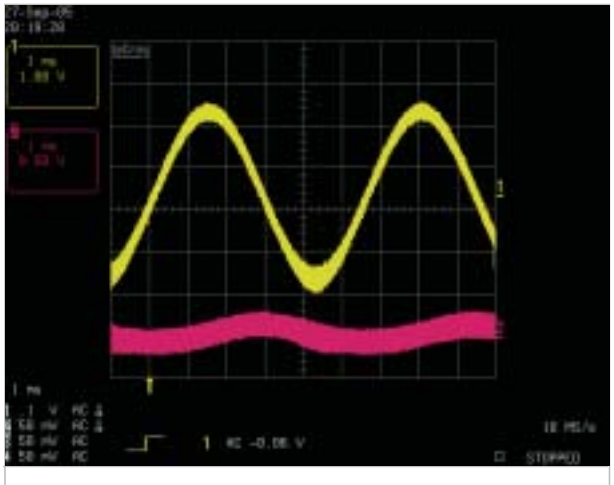

Figure 3 Adding the common-mode-reduction circuit in Figure 1 significantly reduces the amount of common-mode voltage on the video signal.

voltage. Capacitors C_{11} and C_{12} provide equalization to boost the differential-video signal's higher frequency components.

Before applying cancellation, the signals at the circuit's outputs R_{OUT+} and R_{OUT-} would appear as: $R_{OUT+}=V_{DIFF}/2+V_{CM}$, and $R_{OUT-}=-V_{DIFF}/2+V_{CM}$, where V_{DIFF} represents the desired differential signal, and V_{CM} exists with respect to the circuit's local ground. After applying cancellation, the output signals appear as: $R_{OUT+}=+V_{DIFF}/2+V_{CM}-V_{CMS}=+V_{DIFF}/2$, and $R_{OUT}-=-V_{DIFF}/2+V_{CM}-V_{CMS}=-V_{DIF}/2$, where V_{CMS} represents the summed and inverted common-mode voltage at IC_1's output.

Figure 2 shows a representative 1V peak received signal that's on the R+ line (yellow trace) and an accompanying 2V peak common-mode signal (pink trace). Figure 3 shows the circuit's common-mode-cancellation abilities. Although the differential signal (yellow) remains unchanged, the common-mode signal (pink) exhibits an 80%, 14-dB reduction. Any mismatch between the time delay and the summed analog signal, which the passive input network and IC_1, respectively, produce, prevents complete cancellation. Also, for best performance, the common-mode signal must not exceed IC_1's common-mode input-voltage rating. In addition, IC_1, an Intersil ISL55001, must exhibit unity-gain stability over a wide bandwidth and an excellent slew-rate response and, for best results, must operate at relatively high-power-supply voltages for good linearity. Use 10-µF, nonpolarized input- and output-coupling capacitors to accommodate extremely low-frequency common-mode voltages. Ensure adequate bypassing for IC_1's power-supply terminals for all frequencies of interest. EDN

Use a switching-regulator controller to generate fast pulses

Mitchell Lee, Linear Technology Corp

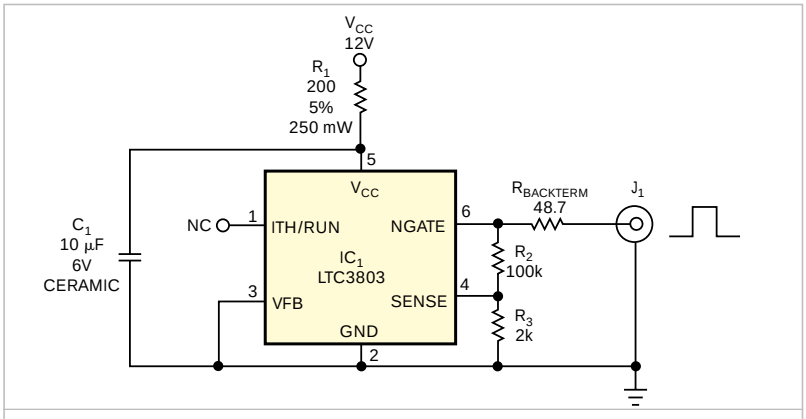

Figure 1 Switching-regulator-controller IC_1 delivers pulses with 1.5-nsec rise and fall times into a 50Ω load.

A source of pulses with fast-rising edges that approximate the step function can help you perform many useful laboratory measurements, including characterization of coaxial cables' rise times and location of cable faults using time-domain-reflectometry methods. For example, evaluating the rise time of a 10- to 20-ft-long RG-58/U cable requires edge-transition times of 1 to 2 nsec. Agilent's (www.agilent.com) HP8012B, a workhorse pulse generator that finds use in many electronics labs, can deliver pulses with rise times of 5 nsec that are adequate for many applications but not for cable characterization.

As an alternative, switching-regulator-controller ICs can deliver gate-drive pulses with rise and fall times of less than 2 nsec, making them ideal candidates for laboratory pulse-generation service. A simple implementation uses Linear Technology's (www.linear.com) LTC3803 constant-frequency flyback controller, IC_1 (Figure 1). The controller self-clocks at 200 kHz, and applying a sample of its output to its Sense pin causes the controller to operate at its minimum duty cycle and produce a 300-nsec-wide output pulse.

The LTC3803's output can deliver more than 180 mA into a 50Ω load, so use a low-series-inductance bypass capacitor that connects as directly as possible between IC_1's power and ground (pins 5 and 2). The decoupling components, C_1, a 10-µF ceramic capacitor, and R_1, a 200Ω resistor, minimize pulse-top aberrations without introducing amplitude droop. The circuit's output directly drives a 50Ω termination at amplitudes as high as 9V. For applications that require maximum pulse fidelity, use a back-termination resistor, $R_{BACKTERM}$, to suppress triple-transit echos and absorb reflections from the cable and any mismatch in the cable's far-end termination impedance. Back-termination also helps when driving passive filters, which expect to see a specific generator impedance. The LTC-3803's output impedance is approximately 1.5Ω, which affects the value of the back-termination resistor. The back-termination technique

(continued on pg 106)

works well with load impedances of at least 2 kΩ. At impedances higher than that value, parasitic impedances associated with the terminating resistor and IC_1 degrade bandwidth and pulse fidelity.

In a back-terminated, 50Ω system, the circuit delivers a 4.5V output pulse with symmetric rise and fall times of 1.5 nsec, pulse-top-amplitude aberrations of less than 10%, and amplitude droop of less than 5%. Directly driving a 50Ω load doesn't degrade the output's rise and fall times. For best pulse fidelity, use stripline techniques to route IC_1's output directly to the termination resistor and output connector J_1. Using a 100-mil-wide trace on a 1/16-in., double-sided, glass-epoxy pc board approximates a 50Ω surge impedance. EDN

Shift registers and resistors deliver multiphase sine waves

Gary Steinbaugh, 4 E A Transform, Loveland, OH

Sine waves with fixed phase relationships find application in communications equipment, instrumentation, and power sources. Although you can use any of several traditional analog techniques to generate basic sine-wave signals, this Design Idea offers a simple method that uses only digital logic and fixed-value resistors (Figure 1a). A common clock pulse drives three of four sections of a pair of CD4015 4-bit shift registers that recirculate a pattern comprising 12 zeros and 12 ones—that is, 000000000000111111111111. Each of the registers' outputs drives a resistor, R_1 through R_{12}, that connects to a summing node. If all of the resistors were of equal value, their summed output would comprise a stepped linear triangular waveform at a repetition frequency one-twenty-fourth that of the clock frequency.

To produce a stepped sinusoidal output waveform, you replace the equal-value resistors with the weighted values in Figure 1a. If you use resistors of 1% tolerance, the output's amplitude will approximate that of a true sine wave to better than 1°. To produce a cleaner sine wave, a lowpass filter helps remove clock-pulse feedthrough and stepped-edge transients (Figure 1b). For many applications, a simple one-pole lowpass filter/buffer provides adequate filtering, but a more elaborate multipole filter further increases output purity.

You can add a second set of registers and resistors, R_{13} through R_{24}, to produce cosine and sine waves offset by a 90° phase shift—that is, two sine waves in quadrature (Figure 2). Register IC_{2A}'s inverted and recirculated output from Q4 generates the 0000000000-00111111111111 bit pattern that the first set of shift registers uses. IC_{1B}'s Q2 output produces the D input that you apply to the second set of shift registers—IC_{2B}, IC_{3A}, and IC_{3B}—which in turn generate a 90° phase-shifted version of the bit pattern to form a cosine wave. The cosine bit pattern requires no recirculation and simply propagates

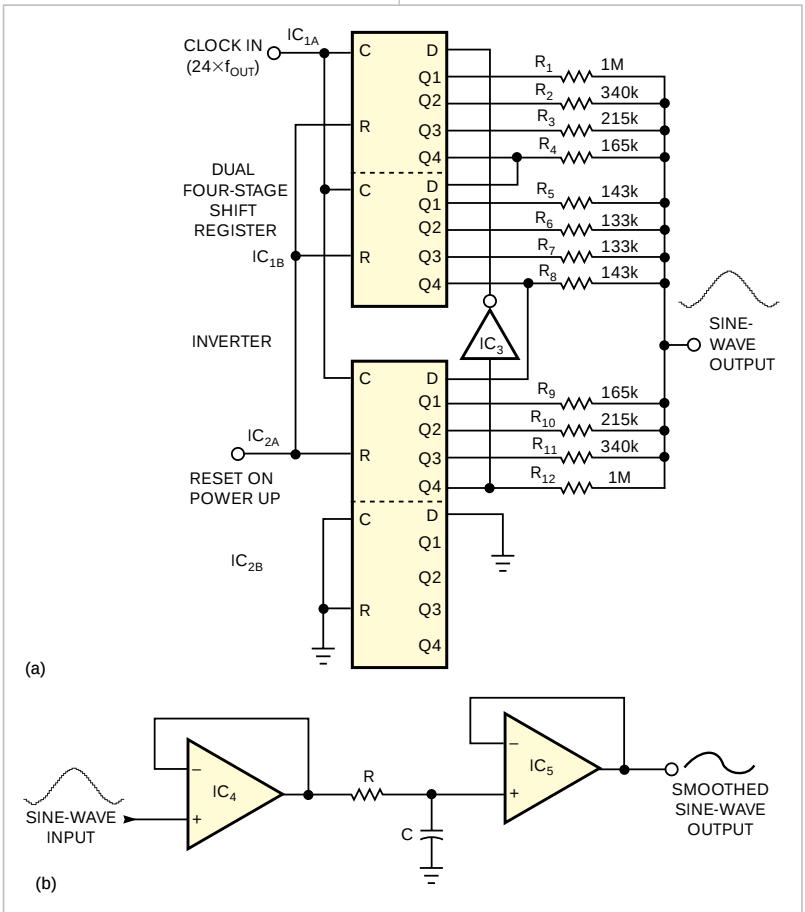

Figure 1 A pair of shift registers, an inverter, and a handful of precision resistors form a sine-wave generator (a). Two operational amplifiers form a resistance-capacitance lowpass filter that removes clock-signal artifacts from the output (b).

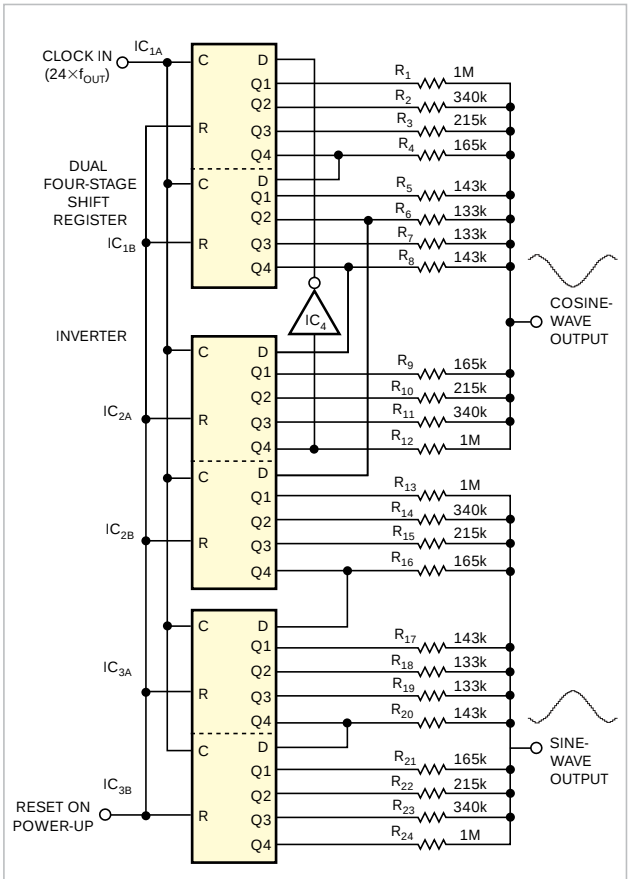

Figure 2 Add a second set of shift registers to generate a cosine wave.

through the second set of shift registers and "falls off the end." To adjust the second output's phase shift with respect to the first output from 15 to 180° in 15° increments, you can connect IC_{2B}'s D input to any one of IC_1's or IC_{2A}'s Q outputs.

Figure 3 illustrates a three-phase sine-wave-generator circuit. The Q4 output from IC_{1B} supplies the D input to the second set of shift registers, IC_{2A} and IC_{2B}, to produce the recirculated bit pattern. In similar fashion, the Q4 output from IC_{3A} supplies the D input to the third set of shift registers, IC_{4A}, to transfer a duplicate bit pattern that's phase-shifted by 240° with respect to the output from the first set of shift registers.

Register IC_{2B}'s D input connects to IC_{1B}'s Q4 output to produce a signal—Phase 2's output—that lags behind the Phase 1 output by 120°. In similar fashion, register IC_{4A}'s D input connects to IC_{3A}'s Q4 output to produce a signal—Phase 3's output—that lags behind Phase 2's output by 120°, or 240° with respect to Phase 1.

You can expand the basic circuit to accommodate additional signal phases. The weighted resistors' values are adequate for low-frequency sine waves and 4000-series CMOS-logic devices. However, you can scale the resistors' values to accommodate other output frequencies and logic families. EDN

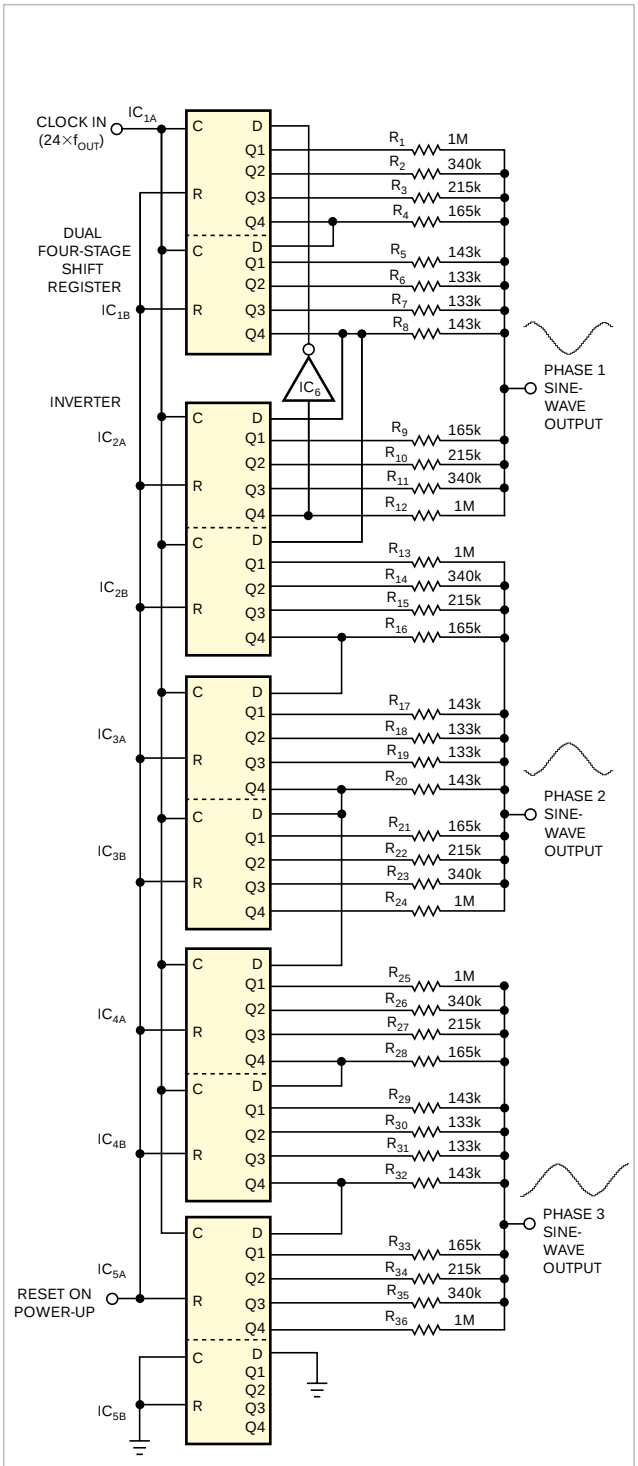

Figure 3 Adding a third set of shift registers yields a three-phase sine-wave output.

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Thermal considerations matter for Class D amplifiers

John Guy, Maxim Integrated Products, San Jose, CA

A Class D amplifier provides better efficiency and thermal performance than a comparable Class AB amplifier, but implementing a Class D amplifier still requires attention to good electrical- and thermal-design practices. Most engineers use a continuous-sine-wave-input signal to evaluate a Class D amplifier's performance in the lab. Although convenient for measurement purposes, a sine wave represents a worst-case scenario for the amplifier's thermal load. If you drive a Class D amplifier near maximum output power with a continuous sine wave, it's not uncommon for the amplifier to enter thermal shutdown.

Typical audio-program material comprising music and voice has a much lower rms value than its peak output power. The ratio of peak-to-rms power, or "crest factor," typically averages about 12 dB for voice and 18 to 20 dB for musical instruments. **Figure 1** shows time-domain-oscilloscope, rms-voltage measurements of an audio signal and a sine wave. Although the audio signal corresponds to a burst of music, it presents a slightly higher peak value than the sine wave, and its rms value approaches only half and may average even less than that of the sine wave. An audio signal's thermal effects on a Class D amplifier are considerably lower than a sine wave's, and, thus, it's important to test performance with actual audio signals instead of sine waves.

In an industry-standard TQFN package, a bottom-side-exposed pad provides the primary path for heat transfer from the IC and into copper areas of the amplifier's pc board that serves as a heat sink. Soldering the IC to a large copper pad helps minimize thermal resistance, as do multiple vias that transfer heat to the pc board's opposite side, on which an additional copper area further reduces thermal resistance. In addition, you can connect any of the device's pins to the thermal transfer area, provided that the pins and thermal pad are at the same electrical potential, such as the upper- and lower-right pins in **Figure 2**.

Although an IC's pins don't provide the primary heat-transfer path, they do dissipate a small amount of heat, and it's helpful to maximize the widths of all pc traces that connect to the IC. **Figure 3** shows how wide traces connect the IC's outputs to two inductors. In this case, the inductor's copper windings provide an additional thermal path away from the Class D amplifier. Improving heat dissipation by even a few percentage points may make the difference between achieving acceptable performance and encountering thermal problems. To further reduce thermal resistance, you can specify a heat sink

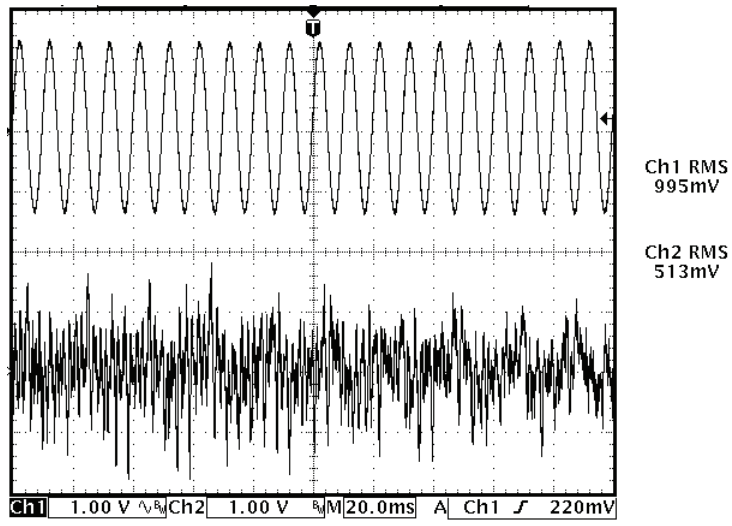

Figure 1 A sine wave's higher rms level than that of an audio signal predicts the additional thermal burden on a Class D amplifier that's tested with a sine wave.

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that solders to the pc board adjacent to the IC. For example, a Wakefield Engineering (www.wakefield.com) 218-series sink has lower edges that form the conduction path.

A few basic calculations can help you estimate a Class D-amplifier IC's die temperature. For example, consider an amplifier that operates at an ambient temperature of 40°C, has output power of 16W, and has 87% efficiency. Specified thermal resistance from the IC's junction to ambient air is 21°C/W. First, calculate the Class D amplifier's power dissipation: $P_{DISS}=[(P_{OUT}/\eta)-P_{OUT}]=(16W/87\%)-16W=2.4W$, where P_{DISS} is the dissipated power, P_{OUT} is the output power, and η is the efficiency. Use the power dissipation to calculate the die temperature, T_C, as follows: $T_C=T_A+P_{DISS}\times\Theta_{JA}=40°C+2.4W\times21°C=90.4°C$, which is within the device's maximum junction temperature of 150°C. A system seldom enjoys the luxury of operation at a 25°C ambient temperature, and it's important to base these calculations on a reasonable estimate of the system's actual internal ambient temperature.

The on-resistance of a Class D amplifier's MOSFET output stage affects both its efficiency and its peak-current capability. Reducing the peak load current reduces the infinite-impulse-response losses and increases efficiency in the MOSFETs. To further lower peak currents, choose the highest impedance speaker that delivers the desired output power within the voltage-swing limits of the Class D amplifier and its supply voltage. In **Figure 4**, a Class D amplifier with an output-current capability of 2A and a supply-voltage range of 5 to 24V goes into current limiting with a 4Ω load and a supply voltage of 8V for a corresponding maximum continuous output of 8W.

If 8W represents an acceptable output power, consider using a 12Ω speaker and a 15V supply voltage. The peak current limit then occurs at 1.25A, with a corresponding maximum continuous output power of 9.4W. Furthermore, the 12Ω load operates at 10 to 15% higher efficiency than the 4Ω load and thus lowers the IC's power dissipation. Actual efficiency improvements vary among Class D-amplifier ICs.

To complicate matters for the designer, a loudspeaker behaves as a complex electromechanical system that presents a variety of resonances across its frequency range and exhibits its nominal impedance only within a narrow frequency band (**Figure 5**). Over much of its audio bandwidth, this loudspeaker's impedance exceeds its nominal value of 8Ω; adding a crossover network and a tweeter may reduce the total load impedance below the nominal value. Keep the load impedance's behavior in mind when you consider the amplifier's power-supply current and thermal-dissipation capability. EDN

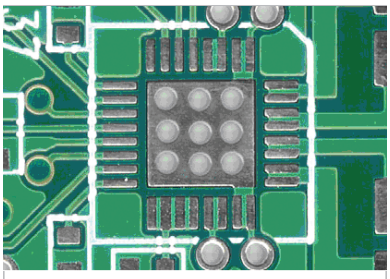

Figure 2 The exposed tinned-copper pad in the center provides the primary thermal path for a Class D-amplifier IC in a TQFN or TQFP package.

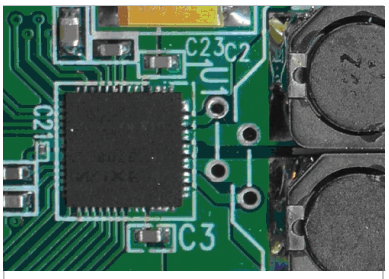

Figure 3 The wide traces to the right of this Class D-amplifier IC help conduct heat away from the device and into the adjacent components.

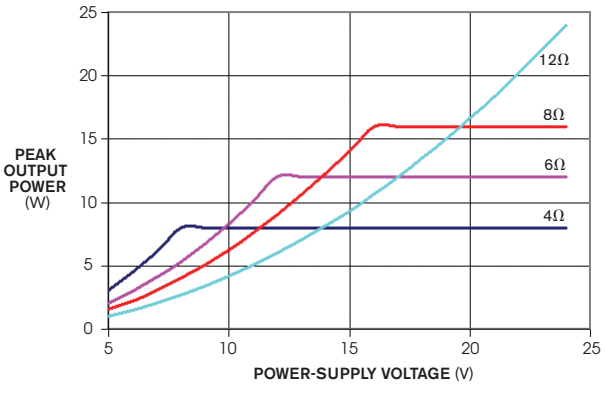

Figure 4 Selecting an optimal impedance, such as 12Ω, and supply voltage, such as 15V, maximizes output power and prevents current-limiting-induced distortion.

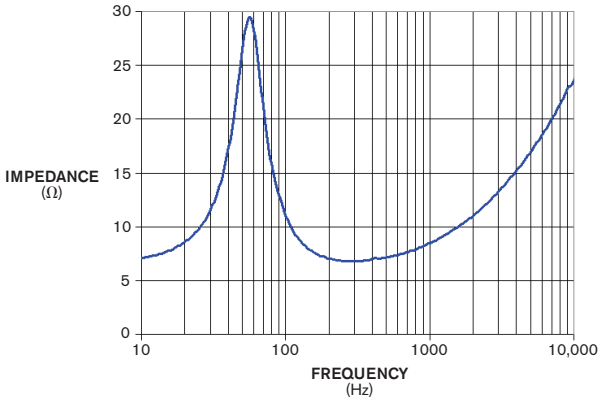

Figure 5 The electrical impedance of this nominally 8Ω, 13-cm-diameter, wide-range loudspeaker varies significantly with frequency.

Microcontroller simplifies battery-state-of-charge measurement

Abel Raynus and Evgueni Freidline, Armatron International, Malden, MA

A system that receives its power from a renewable-energy source, such as a photovoltaic panel or a wind-driven generator, typically accumulates power in a rechargeable battery and delivers it to a load. Often, both processes occur simultaneously. Periodic evaluation of the battery's remaining charge ensures extended performance and battery life, as does control of the battery current that goes to the load. A battery's residual charge comprises its previously calculated charge plus the amount of newly accumulated charge or minus the amount of charge it expends. According to Coulomb's Law, you can calculate the accumulated charge as follows:

$$Q_{ACC} = \int_0^{\Delta t} i \times dt,$$

where Q_{ACC} is the amount of a battery's newly accumulated charge, and i represents the amount of current integrated over time interval Δt.

In its discrete form, the equation becomes

$$Q_{ACC} = \left(\frac{1}{n}\sum_{k=1}^{k=n} Ik\right) \times \Delta t,$$

where n represents the number of current measurements, I_k, taken during the time interval, Δt. Although you can select any value for Δt, it's convenient to choose a value equal to one hour, because battery manufacturers specify capacity in units of ampere-hours.

To simplify the microcontroller's firmware and reduce the amount of memory necessary for arithmetic operations, you can divide one hour into 128 measurement cycles and use register shifting to perform the division required in the equation. You calculate each charge measurement as an average value from 32 current samples, which the microprocessor's internal ADC converts. One of the ADC's multiplexed input channels converts charging current, and another converts discharging current. Thus, the equation for remaining battery-charge capacity reduces to $Q_{REM} = Q_{PREV} \pm Q_{ACC}$, where Q_{REM} is the remaining battery charge, Q_{PREV} is its previously calculated charge, a plus sign indicates a net charge, and a minus sign indicates a net discharge.

As **Figure 1** shows, the circuit comprises an eight-pin version Freescale's (www.freescale.com) low-cost MC68HC908QT2 microcontroller, IC_3. The voltage across current-sampling resistor R_1 reverses polarity depending on whether the battery charges or discharges. Connected as identical-gain noninverting and inverting amplifiers, respectively, IC_{2A} and IC_{2B} sense the voltage developed across R_1. Noninverting amplifier IC_{2A} responds only to a positive voltage developed by a charging current and delivers zero output for a negative input voltage developed by a discharge current. Inverting amplifier IC_{2B} responds only to a negative input and delivers 0V for a positive-charging current. The outputs of both op amps are positive and range from 0 to approximately 5V and simplify design of the interface with the ADC's multiplexed inputs. Using Texas Instruments' (www.ti.com) TLC277 for IC_2 offers the benefits of a small-pc-board footprint and a low input-offset voltage.

You calculate the sense resistor R_1's value and the amplifiers' gain, G, by determining the lowest and highest expected charge and discharge currents and applying the following equation:

$$R_1 \times G = \frac{V_{IN(MAX)}}{I_{MAX}},$$

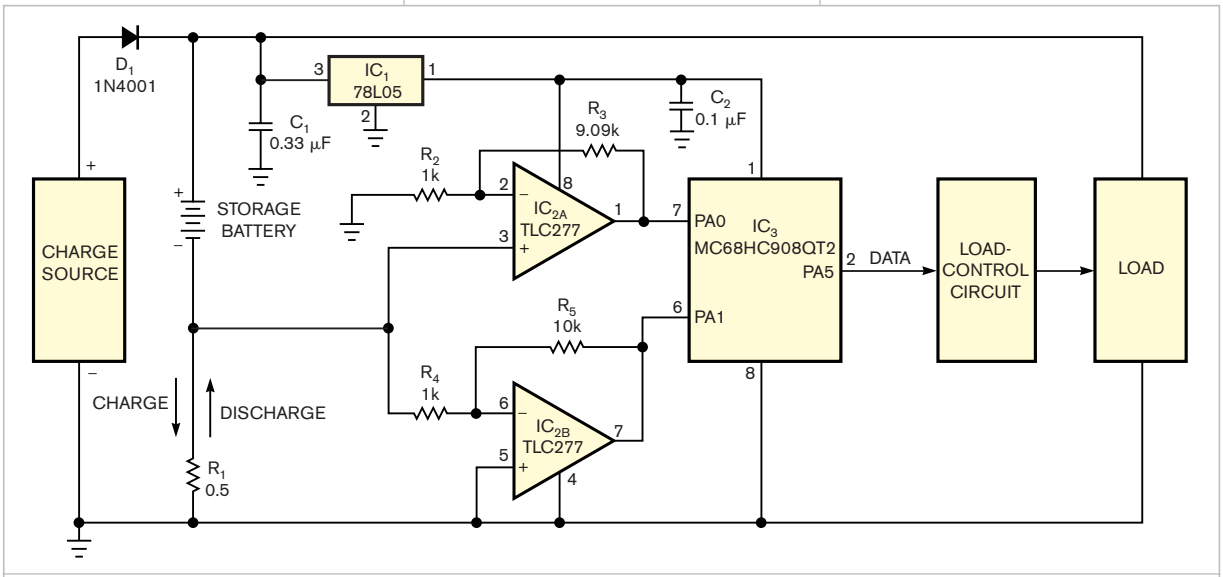

Figure 1 Measure a storage battery's state of charge using only a few components.

where I_{MAX} is the maximum discharge current and $V_{IN(MAX)}$ is the maximum ADC input. In this example, the maximum charge and discharge currents are approximately 1A.

Thus, for a 1A charge or discharge current and a maximum ADC input of 5V, you can choose a value of 0.5Ω for R_1 and a gain of 10 or 100. Once you calculate the battery's charge capability, you can send the data to a host processor or another destination through a single-wire interface, SPI, I^2C, CAN (controller-area-network), or another industry-standard method (**Reference 1**). To maximize battery life, you can use the microprocessor's output to control current that an external load draws.

Manufacturers generally ship lead-acid batteries fully charged to avoid sulfation, and this design assumes that a battery starts in a fully charged state. To accommodate battery chemistries other than lead acid, you must modify the value of the battery's maximum charge capability that's stored in a specialized firmware register. You can download the microprocessor's firmware from www.edn.com/060427di1.EDN

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1 Raynus, Abel, "Single wire connects microcontrollers," *EDN*, Oct 22, 1998, pg 102, www.edn.com/archives/1998/102298/22di.htm #single.

Switching regulator efficiently controls white-LED current

Clayton B Grantham, Agtech, Tucson, AZ

A few years ago, manufacturers specified their white, but dim, LEDs for a maximum forward-current rating of 20 mA. Today's white LEDs deliver more light and thus must operate at ever-higher bias currents. Maintaining control of an LED's bias point while operating at high current near its maximum rating requires a new approach.

The simplest and most common method of biasing an LED involves connecting a resistor in series with the LED to limit the LED's maximum current, but this method directly impacts power efficiency, which you define as the ratio of power to the LED to the total input power. For a white LED operating at 350 mA, the corresponding forward-voltage drop across the diode is approximately 3.2V. A series resistor and LED connected to a 5V power source operates at 64% efficiency—that is, 3.2V for a 5V source. The power dissipates as heat, causing an average power loss in the series resistor of 36 mW at a forward current of 20 mA, which is acceptable, but this figure balloons to 630 mW at a forward current of 350 mA.

In addition, using a series resistor allows the diode's bias point and thus its brightness to fluctuate as the power-supply voltage and the ambient temperature vary. Based on National Semiconductor's (www.natsemi.com) LM2852 switched-mode bucking regulator, which features internal compensation and synchronous-MOSFET switches that can drive loads as large as 2A, the circuit efficiently provides constant-current drive to a high-current LED and minimizes the effects of supply-voltage and temperature variations on the LED's brightness (**Figure 1**).

In this circuit, the LM2852 operates at efficiency of approximately 93% and directly controls a step-down-regulator topology that maintains a constant current flow through LED_1, which potentiometer R_1 adjusts. Current-to-voltage conversion taking place within the circuit's control loop effectively regulates the circuit's output current. In operation, the LM2852 compares its internal reference voltage with the voltage from the divider formed by D_1, R_1, and R_2 and drives the control loop to maintain a constant 1.2V at its voltage-sense pin. Current through the voltage divider is proportional to the current through LED_1, and the ratio of the currents tracks over the circuit's operating-temperature range because D_1 and LED_1 exhibit approximately the same forward-voltage temperature coefficient of −2 mV/°C. Mounting D_1 and LED_1 next to each other on the pc board provides sufficiently close thermal coupling for temperature compensation.

With R_1's wiper fully clockwise, the

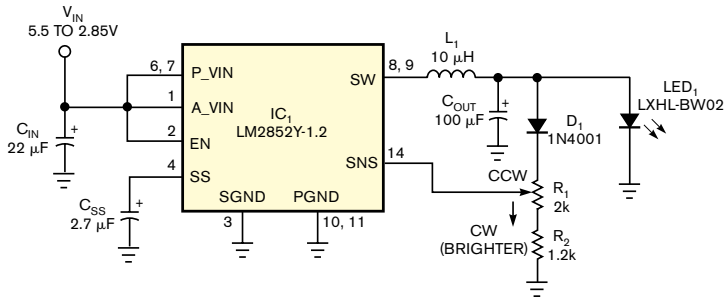

Figure 1 This circuit drives a high-current, white LED at 93% efficiency over input voltage and temperature. Potentiometer R_1 controls current through LED_1 and allows brightness adjustment. Diode D_1 provides temperature compensation for LED_1's forward-voltage drop.

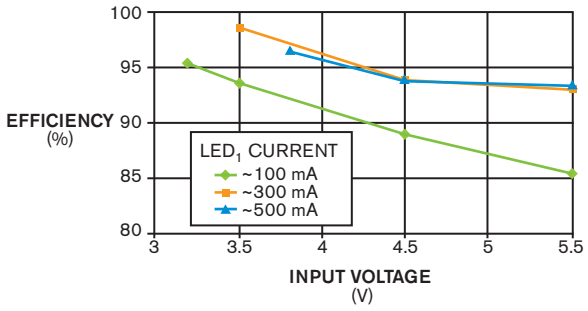

Figure 2 Circuit efficiency versus input voltage shows an increase in efficiency for increasing LED current and decreasing input voltage.

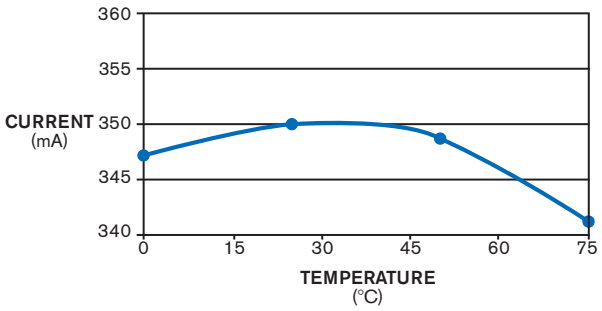

Figure 3 Current through the LED varies less than 3% over an operating-temperature range of 0 to 75°C.

current through D_1 approaches 1 mA, and the current through LED_1 averages approximately 500 mA. Adjusting R_1 counterclockwise reduces LED_1's forward current from 500 mA to 0A.

When scaling the values of R_1 and R_2 for a different current-loop gain, decreasing the gain impacts the circuit's conversion efficiency, and increasing the gain makes the loop more sensitive to component tolerances. To provide a remote brightness control, you can replace mechanical potentiometer R_1 with a digitally programmed potentiometer. Luxeon (www.luxeon.com), the manufacturer of LED_1, an LXHL-BW02, specifies limits of 350-mA continuous current and 500-mA peak-pulsed current. **Figure 2** shows the circuit's efficiency versus variations in input voltage. Note that the circuit's efficiency increases as input voltage decreases, which helps extend operating time in battery-powered-system applications.

As temperature fluctuates, the current through LED_1 varies less than 3% over the temperature range, a factor-of-three improvement over a series-resistor current-limiting circuit (**Figure 3**). Although more complex than a single resistor, the circuit in **Figure 1** requires only a few components. For L_1, this prototype uses Coilcraft's (www.coilcraft.com) MSS5131-103 surface-mount inductor rated for 10 µH.

National Semiconductor's data sheet for the LM2852 outlines criteria for selecting capacitors C_{IN}, C_{SS}, and C_{OUT}. For efficient heat removal, the circuit's pc board should include generous copper-mounting pads and traces for IC_1 and LED_1. At a forward current of 350 mA, LED_1 dissipates 1.1W, so consult the manufacturer's data sheet to review its thermal-design recommendations. EDN

Programmed reference oscillator generates nonstandard clock frequencies

William Grill, Honeywell BRGA, Lenexa, KS

Although manufacturers offer crystal and ceramic resonators and packaged oscillators for many frequencies, nonstandard frequencies may not be readily available. When a unique integrator application required a 2021-Hz fixed-frequency clock, the circuit in **Figure 1** solved the problem and required only a few extra and inexpensive components. The heart of the oscillator comprises a small assembly-language process that exploits equalized, fixed-length branch loops with only 12 instructions. A simple Visual Basic program, available at www.edn.com/060427di2, provides a user-input window that calculates the number of loops necessary to create the desired frequency and also determines the required number of individual instruction periods needed to "top off" the duration of the output period (**Figure 2**).

Including Microchip's (www.microchip.com) PIC12F508 8-bit microcontroller, IC_1, the circuit in **Figure 1** uses only four components. The microcontroller operates at clock-crystal frequencies as high as 4 MHz and includes a configuration option that uses the IC's internal 4-MHz oscillator, which is accurate to ±1% as the controller's base frequency. Another version of the microcontroller, the PIC16F505, can operate at clock-crystal frequencies as high as 20 MHz.

To calculate the constants to program the microcontroller for the desired out-

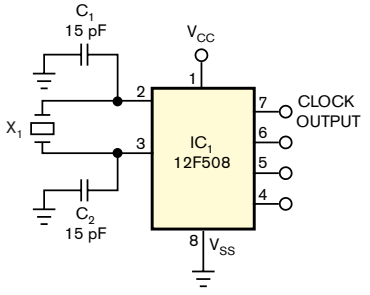

Figure 1 Delivering a fixed clock frequency, this preprogrammed oscillator uses few components.

put frequency, you use the Visual Basic program, editing the clock frequency of 4 MHz in this example if necessary. Next, you enter the clock's frequency error in percentage points or parts per million and the desired output frequency in hertz. When you click on the "Evaluate" control, the program computes the high- and low-state coefficients, the number of appended instructions, and the output's duty cycle. The program also calculates the maximum initial percentage error of the output frequency. The controller's instruction-execution times and clock frequency impose constraints on the desired output frequency, duty cycle, and frequency error. For the 2021-Hz clock in this application and a 4-MHz clock frequency, the program calculates the coefficients and number of discrete instructions as 20, 21, and three, respectively. Before compiling the code and writing the results to the microcontroller's internal flash memory, you transcribe the coefficients into the microcontroller's assembly-language program.

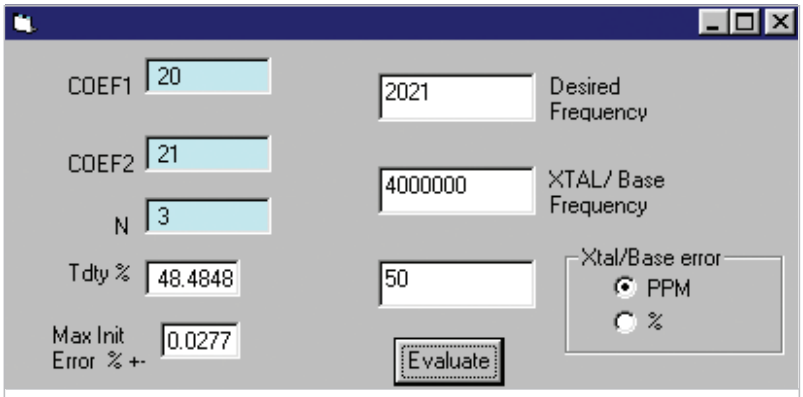

Figure 2 Use this Visual Basic program to calculate programming coefficients for the clock circuit.

The controller's assembly-language listing, at www.edn.com/060427di2, uses only 40 instructions, and its implementation leaves three of the controller's pins unused but available for a user-defined enable input or for selecting one of several preset output frequencies or coefficients. You can reduce the pc-board area the basic design uses if you select a microcontroller that occupies a smaller package, such as six-lead SOT-23 versions of the PIC10F200 or PIC10F220, and use its internal 4-MHz clock oscillator instead of an external crystal. EDN

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READERS SOLVE DESIGN PROBLEMS

JFET cascode boosts current-source performance

Clayton B Grantham, Tucson, AZ

Many process-control sensors, such as thermistors and strain-gauge bridges, require accurate bias currents. By adding a single current-setting resistor, R_1, you can configure voltage-reference circuit IC_1 to produce a constant and accurate current source (Figure 1). However, the source's errors depend on the accuracy of both R_1 and IC_1 and affect measurement accuracy and resolution. Although you can specify high-precision resistors whose accuracy exceeds that of most commonly available voltage-reference ICs, the voltage reference's error dominates this current source's accuracy. Although the manufacturer minimizes the voltage reference's temperature sensitivity and output-voltage error, sensitivity to power-supply variations can affect its accuracy, especially in process-control applications that must operate over a wide range of supply voltages.

A cascode-connected pair of JFETs, Q_1 and Q_2, form a constant-current source that minimizes the reference circuit's sensitivity to supply-voltage fluctuations and extends IC_1's operating voltage beyond its 5.5V maximum rating. In addition, Q_1 and Q_2 effectively increase the current source's equivalent resistance from a few megohms almost into the gigohm range. In the circuit's Norton model, equivalent resistance represents the parallel resistance across an ideal current source.

An N-channel JFET operates as a depletion-mode device at its maximum saturated drain current when its gate-to-source bias voltage is 0V. In contrast to a depletion-mode MOSFET that requires a gate-bias voltage to conduct, the JFET operates in a default on-state and requires gate-bias voltage to cut off conduction. As its gate-to-source voltage becomes more negative with respect to the source, a JFET's drain current goes to zero at the pinch-off voltage. The JFET's drain current varies approximately with its gate bias: $I_D \approx I_{DSS} \times (1+V_{GS}/V_P)^2$, where I_D is drain current, I_{DSS} is the sat-

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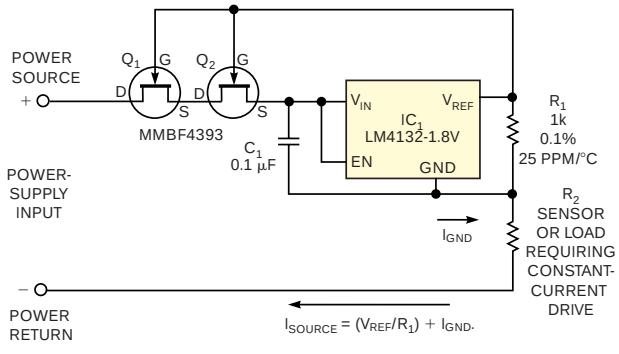

Figure 1 A pair of cascode-connected JFETs reduces the effects of power-supply-voltage fluctuations on a current source's accuracy.

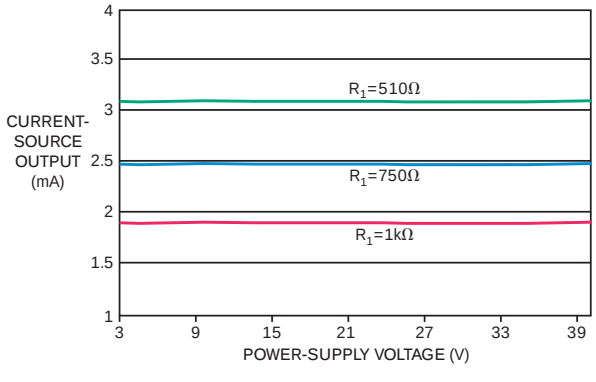

Figure 2 Setting R_1 to values of 1 kΩ, 750Ω, and 510Ω delivers output currents of approximately 1.8, 2.5, and 3.6 mA that are insensitive to a wide range of power-supply voltages.

urated drain current, V_{GS} is the gate-to-source voltage, and V_P is the pinch-off voltage.

Assume that IC_1's output voltage, V_{REF}, remains constant at 1.8V. Because the output voltage drives Q_2's gate, IC_1's input voltage, V_{IN}, equals $V_{REF}-V_{GS(Q2)}$, or $1.8V-(-1.2V)=3V$. Thus, Q_2's gate-to-source voltage rests at its nominal pinch-off voltage of 1.2V and varies in step with small changes in current source. As the power-supply voltage varies from 3V to more than 30V, then the input voltage remains almost constant, as you would expect, because V_{REF} also remains constant. The cascoded-FET configuration increases the current source's Norton equivalent resistance beyond that of the voltage reference and R_1 alone. You can use a single JFET, but stacking two JFETs further enhances the circuit's effective impedance. Note that IC_1 doesn't degrade accuracy because the JFETs hold IC_1's input voltage virtually constant, and IC_1 effectively cancels initial gate-to-source-voltage variations and temperature effects that Q_1 and Q_2 introduce.

Negative feedback in the Kirchhoff-voltage loop that comprises V_{IN}, V_{REF}, and $V_{GS(Q2)}$ allows the drain current to reach an equilibrium bias point that satisfies Q_2's transfer equation. Comprising the sum of (V_{REF}/R_1) plus IC_1's internal "housekeeping" current, I_{GND}, Q_2's drain current remains constant. Adding Q_1 reduces the effects of Q_2's output impedance to insignificance. Adjusting the value of R_1 varies the circuit's output current over a useful range of 200 µA to 5 mA, with Q_2's saturated-drain-current specification imposing an upper limit. If you select a JFET with higher saturated drain current, make sure not to exceed Q_1's maximum power dissipation.

Note that the circuit's lower power-supply-voltage limit must exceed the circuit's compliance voltage, 3V, plus the voltage drop that the sensor introduces: $I_{SOURCE}\times R_2$. The circuit's upper power-supply voltage must not exceed $I_{SOURCE}\times R_2+30V$. For example, supplying a current of 2.5 mA to a 1-kΩ pressure-sensor bridge, R_2, limits the power-supply-voltage range to 5.5 to 32.5V. The circuit's output current varies less than 1 µA over a wide range of power-supply voltages (Figure 2). EDN

Microcontroller delivers voltage-multiplied dc power

Aaron Lager, Masterwork Electronics, Santa Rosa, CA

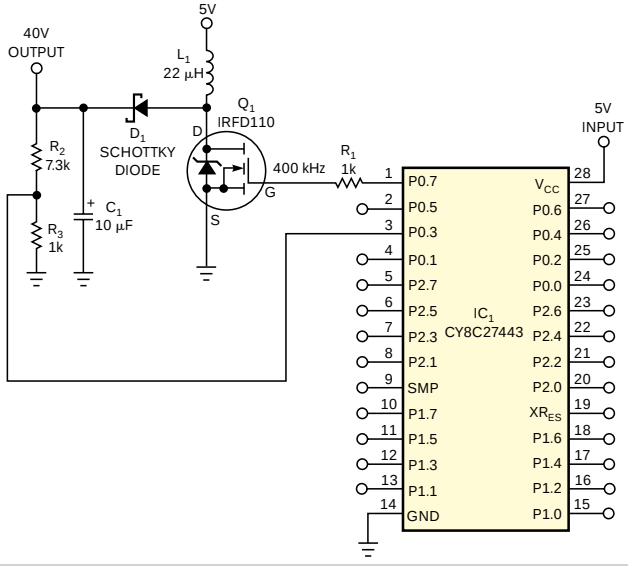

Figure 1 Use a pair of a PSOC microprocessor's internal blocks and a few external components to build a voltage-boost converter. Use a Schottky diode rated for a peak-inverse voltage of 100V for D_1. The PSOC's remaining pins are available for application support.

The combination of an external circuit and a low-voltage microcontroller occasionally requires a significantly higher power-supply voltage. You can use either an external boost converter to increase the logic supply or a buck converter to decrease an even higher voltage. However, you can alternatively use the microcontroller to create a higher voltage. For example, some of Cypress Semiconductor's (www.cypress.com) PSOC (programmable-system-on-chip) microcontrollers include a configurable comparator block that, with a PWM block, can form the heart of a simple inductor-based boost converter (Figure 1). A few external components implement a 40V power supply (Figure 2). When the feedback voltage you apply to Pin 3 (P0.3) exceeds the comparator's software-defined threshold voltage, the comparator shuts off the PWM stage. When the voltage drops below the threshold, the comparator re-enables the PWM block and thus regulates the output voltage. The voltage regulator uses only hardware blocks and

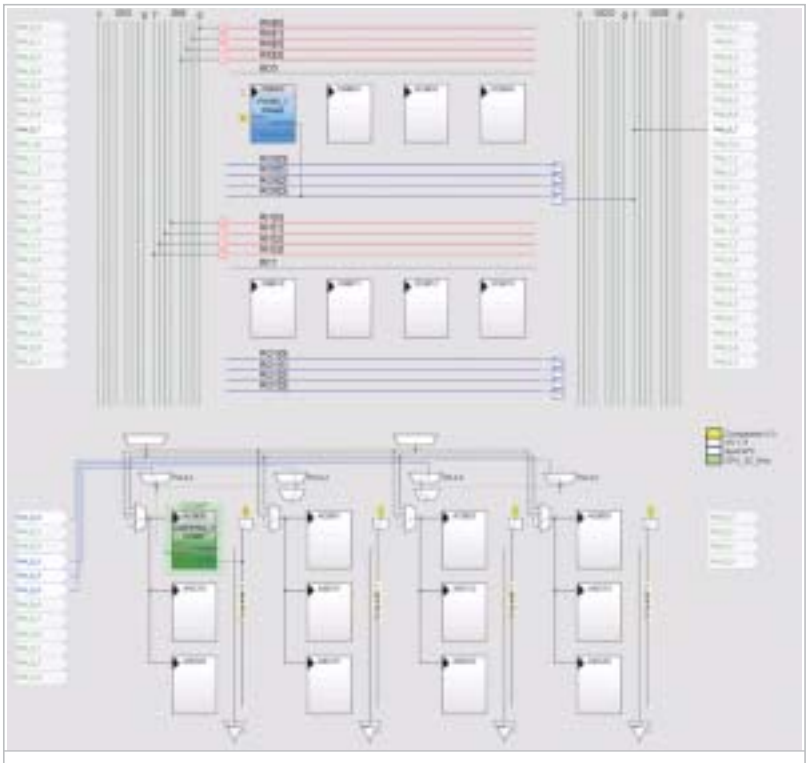

Figure 2 A pulse-width modulator (top) and a comparator (bottom) can operate independently of other PSOC functions. Unconnected pins are available for additional functions.

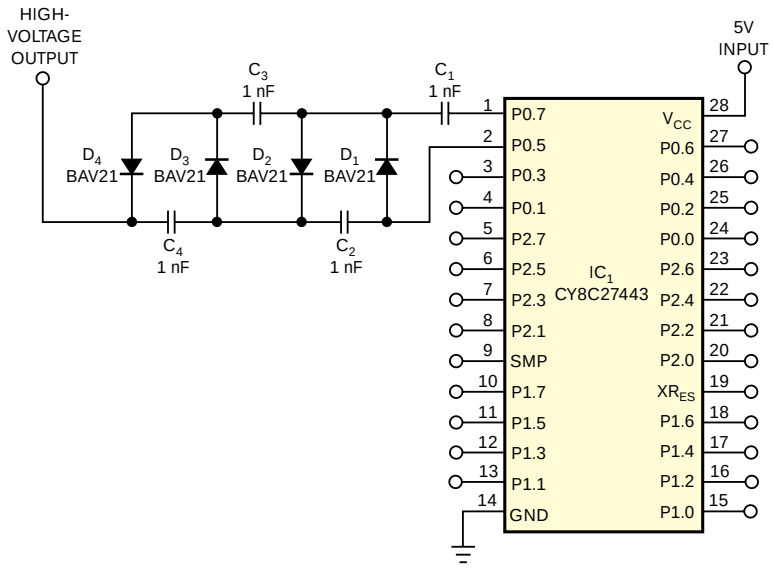

Figure 3 A few diodes and capacitors form a Villard Cascade voltage multiplier.

thus is immune to the effects of other activities taking place in the PSOC's CPU.

However, some microcontrollers lack a built-in comparator. For these devices, the Villard Cascade circuit offers a less expensive alternative to an external boost-voltage converter (Reference 1). Most engineers who are familiar with the Villard Cascade associate it with high-voltage applications and do not envision it as a low-voltage dc-supply technique. The circuit in Figure 3 requires an ac input source that you can easily simulate using a PSOC's internal PWM and inverter blocks. A square-wave output voltage appears on Pin 1, and an inverted version of the same square wave appears on Pin 2. The voltage difference between the two pins applies an ac square-wave voltage to the cascade.

Figure 4 shows how to configure a PSOC's internal blocks to drive the circuit in Figure 3. The PSOC's output multiplexer inverts the PWM's output and drives Port_0_5, and Port_0_6 receives the PWM's noninverted output signal. Again, the PSOC uses hardware blocks to drive a Villard Cascade voltage multiplier, and the circuit produces an output voltage without regard to CPU activity. For an input voltage, V_{IN}, a Villard Cascade of N stages delivers an output voltage of $V_{IN} \times 2N$. One stage comprises two diodes and two capacitors (Figure 5). However, the series-connected capacitors and diodes introduce voltage drops that limit the output current available from a Villard Cascade. In addition, the following equation imposes a practical limit that governs the cascade's output voltage:

$$\Delta V = \frac{I}{fC}\left(\frac{2}{3}N^3 + \frac{1}{2}N^2 - \frac{1}{6}N\right),$$

where ΔV is the output-voltage drop, f is the input frequency, C is the capacitance, I is the output current, and N is the number of stages.

Both boost circuits can supply only modest amounts of current, especial-

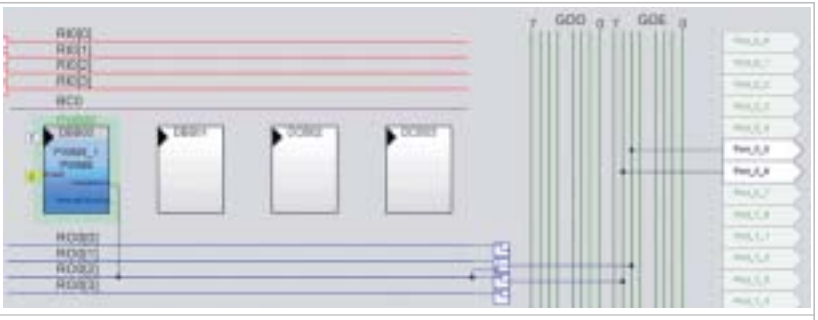

Figure 4 To drive a Villard Cascade multiplier, a PWM block and an inverter block deliver a balanced ac voltage with respect to ground.

ly when they receive power from a 5 or 3.3V source. However, you can charge a high-value storage capacitor from the boost circuit's output and drive a load that presents a low duty cycle (for example, solenoid actuation).EDN

REFERENCE

1 "Jochen's High Voltage Page," www.kronjaeger.com/hv/hv/src/mul/.

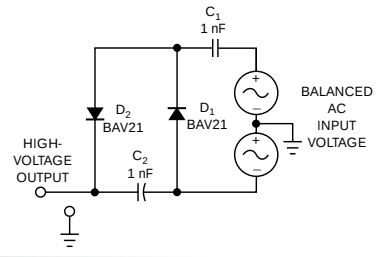

Figure 5 An isolated multiplier stage eases analysis.

Low-dropout linear regulators deliver constant currents

Budge Ing, Maxim Integrated Products Inc, Sunnyvale, CA

Linear voltage regulators offer a simple method of producing a constant current by connecting a fixed resistor between the regulator's output and ground nodes. The regulator's constant output voltage produces a constant current through the resistor. You can use the basic circuit as either a high-side or a low-side current source. The high-side current source uses a positive-output linear voltage regulator, IC_1, a Maxim MAX1818, to provide a constant current of 25 mA to the load resistance (Figure 1). The design imposes two conditions: First, the voltage between IC_1's V_{CC} and ground terminals must not exceed 5.5V. Second, the voltage between IC_1's input and ground terminals must meet or exceed 2.5V, the minimum voltage for proper operation. To satisfy these conditions, choose an output-resistance value that allows 2.5 to 5.5V between input and ground and provides a fixed output of 1.5V across the output resistance at the desired load current.

For example, if you use the circuit to drive a constant current through a 100Ω maximum load resistance while applying 5V V_{CC} between IC_1 and ground, the circuit functions properly when R_{OUT} equals or exceeds 60Ω. This value allows a maximum programmable current of 1.5V/60Ω, or 25 mA. The voltage across IC_1 then equals the allowed minimum: $5V-(25\,mA\times100\Omega)=2.5V$. Available in six-pin SOT-23 packages, the MAX1818 can source as much as 500 mA.

The low-side current-source circuit draws a constant current of 2.5V divided by the output resistance through the load resistance (Figure 2). In this example, IC_1, a MAX1735 linear negative-voltage regulator, provides a fixed output voltage of −2.5V. As in Figure 1, ensuring a voltage of 2.5 to 6.5V be-

tween IC_1's ground and input terminals represents the only precaution for its proper operation. To satisfy that condition, choose an output-resistance value that allows 2.5 to 6.5V between ground and the input. When using the circuit to draw current through a maximum load of 100Ω with V_{CC} at 5V, the output resistance should exceed 100Ω, which provides a maximum programmable current of 2.5V/100Ω=25 mA, which in turn produces a minimum recommended voltage across the device of 5V−(25 mA×100Ω)=2.5V. The MAX1735 can source as much as 200 mA and occupies a five-pin SOT-23 package.

In addition to the programmed load current, both configurations allow the regulator's quiescent current to flow through the load and introduce a source of error that varies with the voltage you apply between the regulator's input and ground connections. You can minimize the error by choosing a voltage regulator that draws low quiescent current or whose quiescent current remains constant through the operating range and allows you to compensate the error by adjusting the value of the output resistance. Quiescent currents for the devices in figures 1 and 2 typically average 130 µA and vary less than 40 µA for a regulator input-voltage range of 2.5 to 5V.EDN

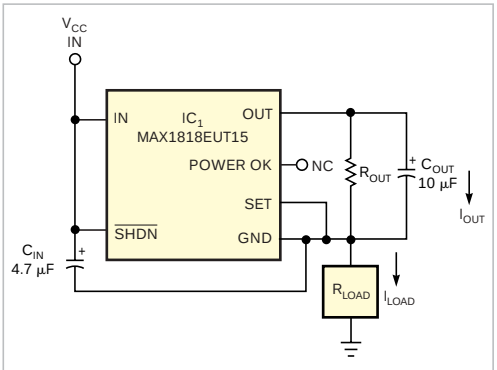

Figure 1 This high-side constant-current source delivers load current of 2.5V divided by the output resistance, provided that you choose the output resistance to ensure that the voltage between the regulator's input and ground terminals is at least 2.5V.

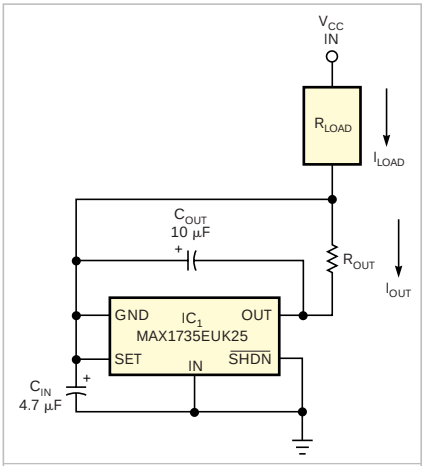

Figure 2 As in Figure 1, this low-side constant-current source draws a load current of 2.5V divided by the output resistance through the load resistance, provided that you select the output resistance to make the voltage difference between IC_1's input and ground terminals at least 2.5V.

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JFET-based dc/dc converter operates from 300-mV supply

Jim Williams, Linear Technology Corp, Milpitas, CA

You use a JFET's self-biasing characteristics to build a dc/dc converter that operates from power sources such as solar cells, thermopiles, and single-stage fuel cells, all of which deliver less than 600 mV and sometimes as little as 300 mV. Figure 1 shows the drain-to-source characteristics of an N-channel JFET under zero-bias conditions, which you can produce by connecting its gate and source together. Applying 100 mV causes a current of 10 mA to flow through the device, increasing to 30 mA at 350 mV. Exploiting the JFET's ability to conduct significant current at zero bias makes it possible to design a self-starting, low-input-voltage converter.

The circuit can supply 5V at currents as large as 2 mA—enough to serve many micropowered applications or to provide auxiliary bias for a higher power switched-mode voltage regulator. At 300-mV input, the circuit starts up at load currents of 300 µA. A load current of 2 mA requires an input of 475 mV.

In Figure 2, Q_1, a parallel-connected pair of Philips Semiconductor's (www.semiconductors.philips.com) BF862 JFETs, and Coiltronics' (www.coiltronics.com) Versa-Pac transformer, T_1, form an oscillator in which T_1's secondary winding provides feedback to Q_1's gate. When you first apply power, Q_1's gate rests at 0V, and drain current flows through T_1's primary winding. T_1's phase-inverted secondary winding responds by delivering a negative voltage to Q_1's gate, which turns off Q_1 and interrupts current flow through T_1's primary winding. In turn, T_1's secondary voltage collapses, and sustained oscillations begin. Although the BF862's published specifications do not cover the device's internal geometry, the device has a low on-resistance and maintains a low gate-turn-on threshold voltage. Using a pair of parallel-connected JFETs for Q_1 ensures the low saturation voltage for operation at low power-supply voltages.

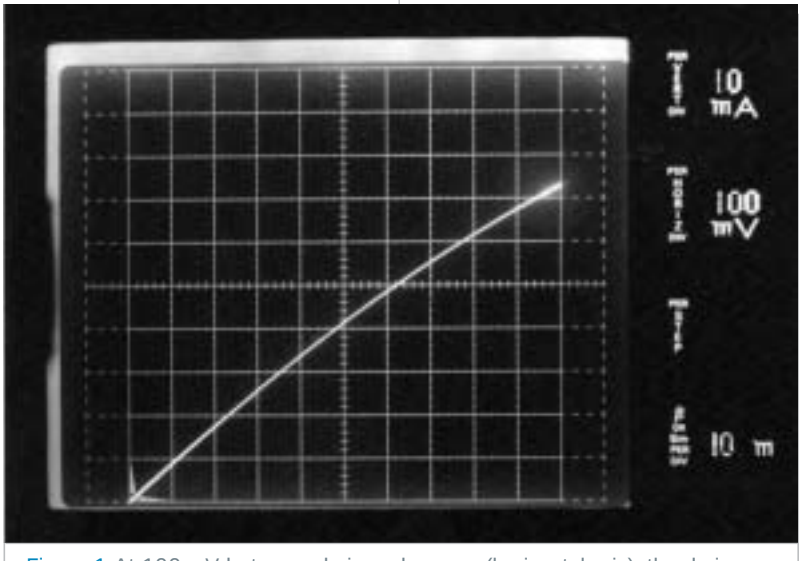

Figure 1 At 100 mV between drain and source (horizontal axis), the drain current reaches 10 mA (vertical axis) and increases to 30 mA at 300 mV.

Rectifying and filtering the positive-going flyback-voltage impulses on Q_1's drain produce a dc voltage across capacitor C_1. To assist the circuit's start-up, a P-channel MOSFET, Q_2, which requires a gate-to-source voltage of approximately 2V for conduction, initially isolates the output load from the rectifier. When Q_2 conducts, the output voltage increases toward 5V. Comparator IC_1, a Linear Technology (www.linear.com) LTC-1440, draws power from Q_2's source and imposes output-voltage regulation by comparing its internal voltage reference with a sample of the output voltage. The output

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from IC_1 varies Q_1's on-time through Q_3 to close the control loop and maintain output-voltage regulation. Figure 3 shows the ripple voltage present at the power supply's output. When the output voltage decays, comparator IC_1 switches (Trace B, middle) and allows Q_1 to oscillate. The resulting flyback events at Q_1's drain (Trace C, bottom) restore the output voltage.

Using Q_3 as a simple but effective shunt control for Q_1's gate voltage results in a 25-mA quiescent-current drain from the power source. A modification reduces the quiescent drain to 1 mA (Figure 4). Inserting switch Q_4 in series with T_1's secondary winding more efficiently controls Q_1's gate. Bootstrapping the voltage across T_1's secondary winding produces negative-turn-off-bias voltage for Q_4. Figure 5 illustrates how to connect T_1's wind-

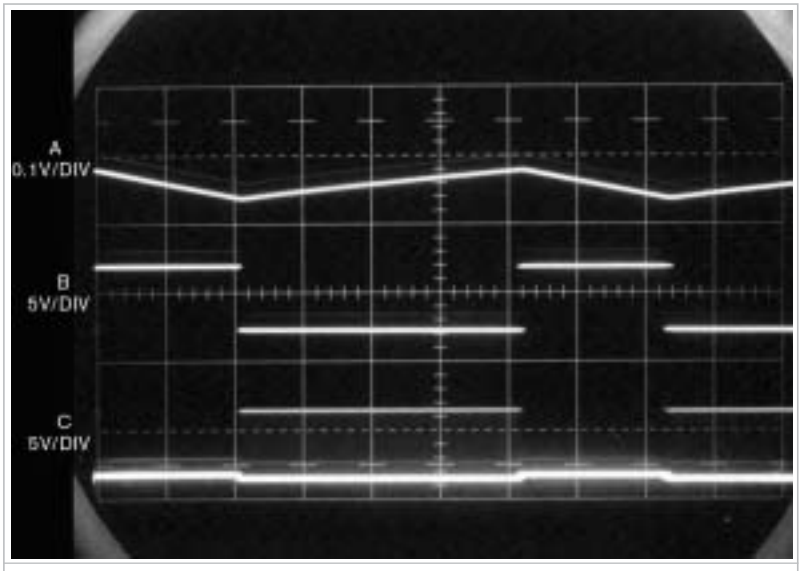
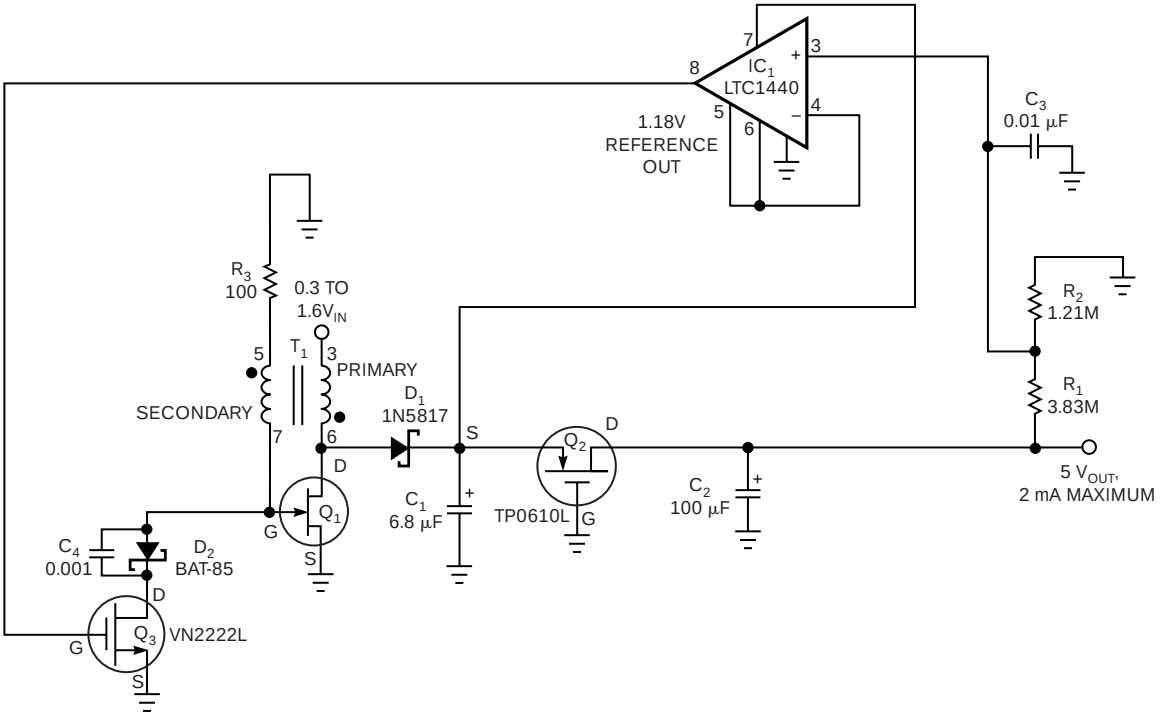


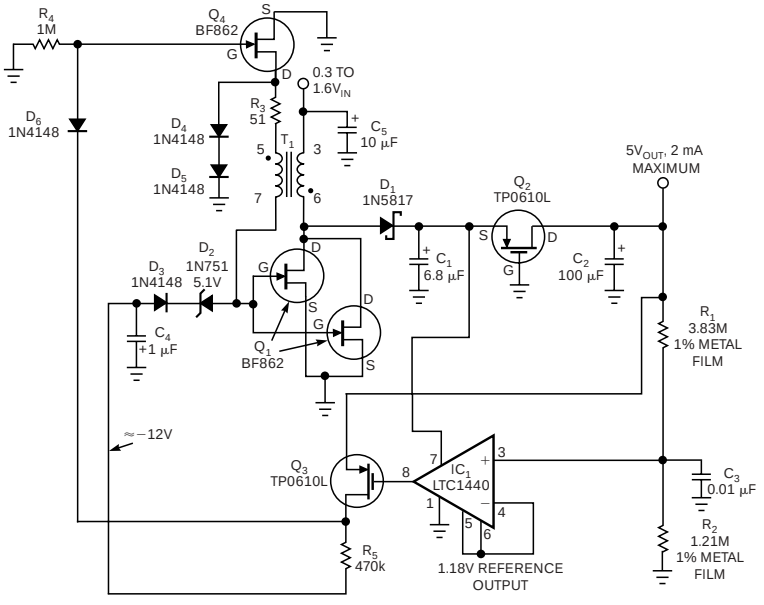
Figure 3 The dc output (Trace A), comparator IC_1's output, and the voltage at Q_1's drain (Trace C) have a horizontal-deflection factor of 5 msec.



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.

Figure 2 A pair of parallel-connected JFETs allows this dc/dc converter to operate from power sources that supply as little as 300 mV.

ings. When Q_4 switches off, it interrupts the current flowing in T_1's secondary winding and drives T_1's Pin 5 positive. Without diodes D_4 and D_5, the peak voltage would approach 15V and reverse-bias Q_4, an undesirable condition. Under normal operating conditions, excursions of approximately 0.8V appear at Pin 5, necessitating the use of two series-connected diodes to clamp the voltage at a safe level. Zener diode D_3 holds off bias-supply loading to aid start-up during initial power application. EDN



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.
4. T_1 = COILTRONICS VP1-1400.

Figure 4 Adding Q_3, Q_4, and the bootstrapped negative-bias generator comprising D_2, D_3, and C_4 reduces the circuit's quiescent current from 25 mA to 1 mA.

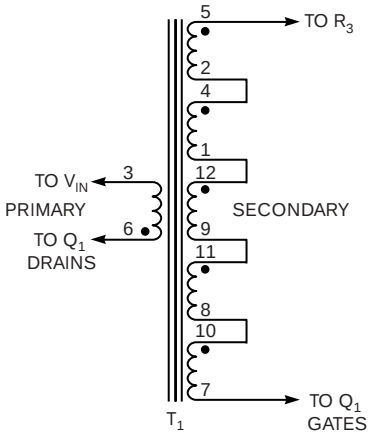


Figure 5 Comprising six independent windings that offer more than 500 configurations, Coiltronics' VP1-1400 serves as a combination feedback and flyback transformer in this application. Connect the windings as shown.

Configurable logic gates' Schmitt inputs make versatile monostables

Glenn Chenier, Allen, TX

You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (Reference 1) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (Reference 2) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

Texas Instruments (www.ti.com)

offers functional equivalents—the SN74LVC1G57 and SN74LVC1G58 (Reference 3). Both companies' devices offer upper- and lower-trip-point-voltage thresholds averaging 37 and 63%, respectively, of V_{CC}, or approximately one RC time constant on the rising or the falling edges. According to the published data sheets from the manufacturers' Web sites, Texas Instruments' versions impose somewhat tighter tolerances on the analog threshold levels and thus deliver tighter timing tolerances than do the Fairchild parts.

For digital-analysis purposes, any voltage below the upper trip point for a rising edge effectively represents a logic zero, and any voltage above the lower trip point for a falling edge represents a logic one. These conditions are true only after the input crosses a respective trip point, such as a rising edge that approaches but never crosses the upper trip point. This voltage remains a logic zero, even if the voltage then drops back to ground potential on its falling edge.

Figure 1a shows some typical circuit implementations. Note that these circuits lack some of the niceties of genuine monostables. For example, a circuit doesn't retrigger until after its RC network has stabilized or about five time constants have elapsed. The RC time constant must be five times shorter than the time between triggering events. Devices from the SN74LVC1G57 family produce the waveforms in Figure 1b, and circuits using the SN74LVC1G58-family devices produce the inverse of these waveforms. The circuits' operation is straightforward. The RC circuits delay one input, so that the inputs momentarily rest at opposite states. When one RC time constant elapses, the delayed voltage crosses the Schmitt upper- or lower-trip-point thresholds, and the delayed input catches up to the straight-through input.

Of unusual interest and unlike the usual variety of monostable that triggers only from a voltage transition in one direction, the XOR implementation functions as a monostable triggered by both the rising and the falling edges, enabling it to function as a frequency doubler for generating strobe pulses on rising and falling clock edges. You can make any inverting-gate configuration into an oscillator by feeding back its inverted output to an RC-delayed Schmitt input and enabling the gate's remaining input. However, once the XOR oscillator's remaining gate switches off the oscillation, the gate's output state hangs at either a one or a zero to produce a truly random state derived from the oscillation's nonsynchronous relationship to the timing of the disabling input. EDN

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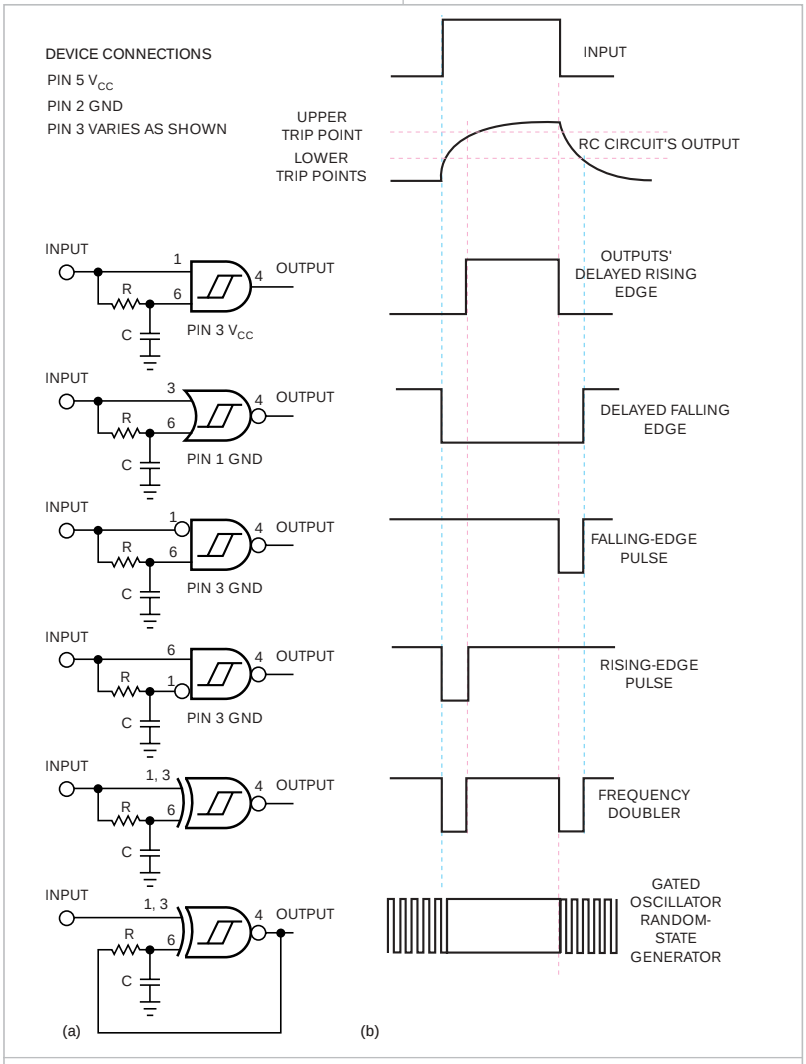

Figure 1 One gate plus an RC network (a) can deliver a range of useful timed outputs (b).

Stealth-mode LED controls itself

Howard Myers, Greensboro, NC

Since the LED's invention more than 30 years ago, its emission efficiency has steadily increased, and, although it may surprise you, the increased conversion efficiency works in two directions. Certain bright, efficient LEDs, such as Hewlett-Packard's (www.hp.com) HLMP-EG30-NR000, a red emitter molded in clear encapsulation, also exhibit significant photovoltaic action. The circuit in Figure 1 shows how you can put an LED's photovoltaic characteristics to work. Using the same components, older, red LEDs also function but with lower light output in this circuit. This Design Idea circuit describes an LED that controls itself by determining whether it's on or off without the assistance of any light sensor other than its own characteristics. When you darken the LED, it turns on, and, when you illuminate it, it turns off. The circuit's main components comprise LED D_1, micropower operational amplifier IC_1, one-shot IC_{2A}, and transistor switch Q_1 to control current through the LED.

When dark, the LED produces no photovoltaic current. When moderate lighting, such as that in an office or a lab, illuminates it, it generates 50 to 100 mV into a 4.7-MΩ load resistor. Comparator op amp IC_1 compares the voltage that the LED produces with a threshold reference voltage of approximately 50 mV. You can vary the circuit's sensitivity threshold by altering the values of resistors R_1 and R_2 in the voltage divider that connects to IC_1's Pin 2.

When ambient light decreases, the LED produces less voltage, and, when the voltage falls below the 50-mV threshold, the op amp's output goes low and triggers one-shot IC_{2A}. The one-shot turns on transistor Q_1 for an interval, lighting the LED for approximately 3 msec until the one-shot's output goes low. In a darkened room, the cycle repeats at a 200-Hz rate, and the LED blinks repeatedly with short off periods. At high flash rates, the LED appears to be continuously on.

The circuit's current drain in the daylight state mainly comprises the current driving the reference-bias network: 3.6V/162 kΩ=22 μA. In both day and night modes, with the LED drawing a few milliamperes when illuminated, a battery that can deliver 1 Ahr would power the circuit for a couple of months. You can reduce the current by increasing the values of R_1 and R_2. Given the circuit's low and intermittent current drain in a well-lighted environment, a 1-Ahr lithium cell's service life should approach its shelf life. EDN

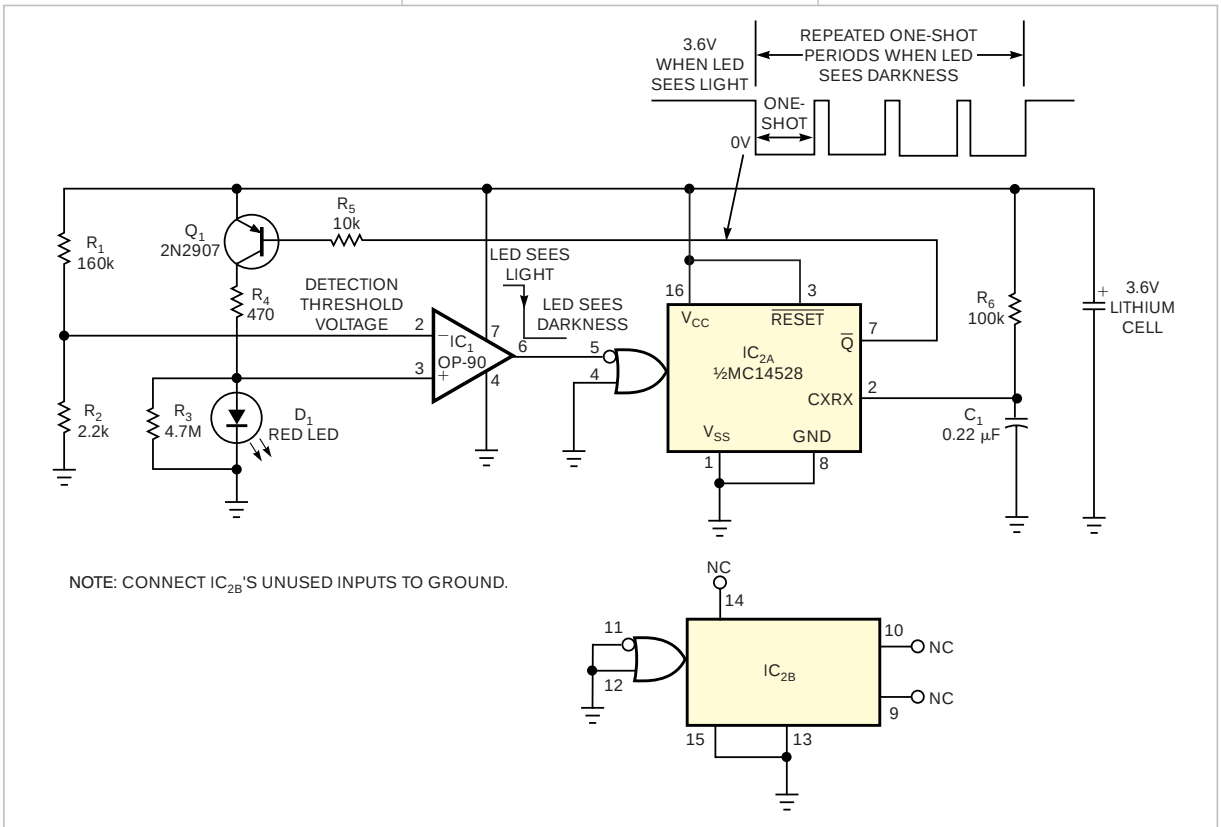

Figure 1 An efficient LED forms the heart of a light-sensitive "mystery lamp" that contains no apparent photodetector.

Data-acquisition system captures 16-bit voltage measurements using the USB

Terry Millward, Maxim Integrated Products Inc, Bionay, Switzerland

The USB has become the interface of choice for connecting to PCs. Available on all relatively modern PCs, the USB offers a standard connector and can supply power to peripherals at 5V and as much as 100 mA of current. The circuit in Figure 1 combines Maxim's (www.maxim-ic.com) MAX1168, a low-power, 16-bit ADC, with a small USB-interface module to make a simple, eight-channel, 16-bit measurement system. The MAX1168 includes eight input channels, an SPI (serial-peripheral-interface) port, a 4.096V reference, and a clock oscillator. The MAX1168 operates from a 5V supply and can convert individual channels, execute multiple conversions on one channel, or scan the channels sequentially and store measured data on-chip.

Based on a Cypress (www.cypress.com) CY7C63743 controller, USBmicro's (www.usbmicro.com) U421 USB-interface module provides as many as 16 I/O lines and an option to use some of those lines as an SPI port at selectable clock rates of 62.5 kHz, 500 kHz, 1 MHz, or 2 MHz. Firmware on the U421 allows generic access to SPI read-and-write devices, and the device's general-purpose I/O lines can serve as slave-select lines for addressing multiple SPI devices. One I/O line controls the MAX1168's chip-select input. When you use it with an

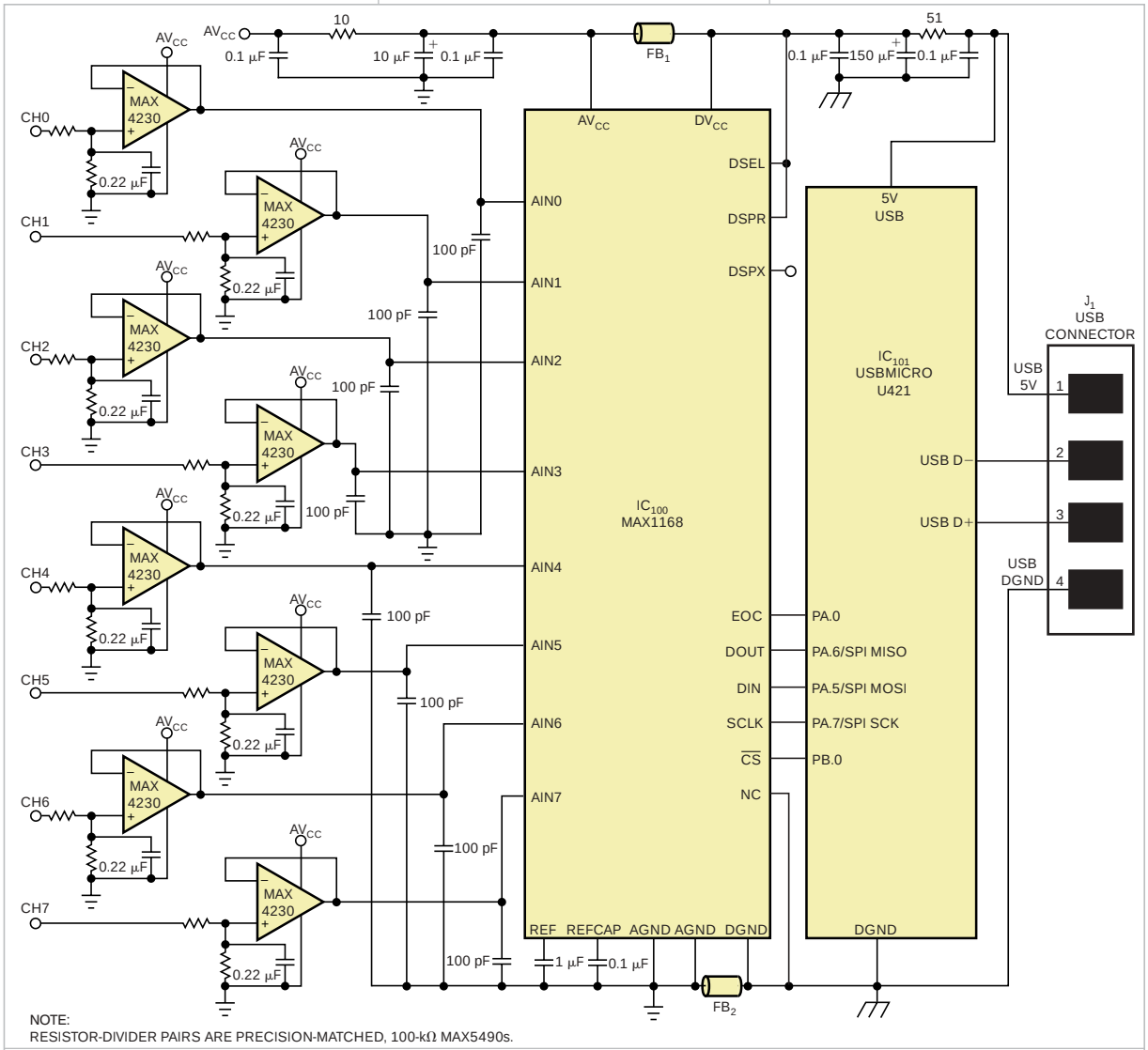

Figure 1 This simple data-acquisition system provides eight channels of 16-bit data to a host computer through a USB interface.

HID (human-interface device), the U421 USB controller can transfer data at rates as high as 800 bytes/sec. With additional filtering to reduce noise, the USB port provides 5V power to the circuit.

The MAX1168's sample-and-hold circuit must acquire the input voltage and charge its 45-pF holding capacitor in 3 μsec and thus requires a fast amplifier to minimize acquisition errors. Available in dual and quad versions, the MAX4230 provides a 10-MHz bandwidth, 2V/μsec slew rate, rail-to-rail inputs and outputs, and the ability to operate from a 5V rail or from voltages as low as 2.7V. The MAX4230's bias current—typically, 50 pA—allows significant input impedance without affecting accuracy.

To provide protection from overvoltages and apply input-voltage scaling, each buffer amplifier's input includes a 100-kΩ precision-matched resistive divider. This application uses Maxim's MAX5490VA10000 10-to-1 dividers, which provide a scaling factor of $^1/_{11}$, to allow maximum readable inputs of 45V at resolutions of 687.5 μV.

Figure 2 User-interface software for the data-acquisition system allows selection of operating parameters. In this image, the lower three channels are unselected and hence are not visible in the display.

Written in Microsoft's Visual Basic.Net, Standard Edition, the evaluation software provides commands to the U421 through the USBm.dll DLL (dynamic-linking-library) file. The demo program sets the MAX1168 to scan all eight channels and display the results. When you run the program, the Visual Basic form allows you to set the reference voltage to allow for the input divider, select the scan time, and enable any of the eight input channels for screen display (Figure 2). You can download the evaluation software at www.maxim-ic.com/MAX=1168DI. EDN

ACKNOWLEDGMENT

Thanks to Robert Severson of USBmicro for his help with the interface.

EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Obtain a lower dc voltage from a higher voltage power supply

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

You can use the circuit in Figure 1 to obtain a low regulated voltage, such as 5V dc, from a higher voltage, rectified, sinusoidal voltage source without resorting to an electrically noisy dc/dc converter or wasting watts in a dropping resistor. This application requires a regulated 5V-dc source, but a transformer supplies 18V rms to a full-wave bridge rectifier. During the charging phase, two equal-value electrolytic capacitors, C_1 and C_2, receive charging current when connected in series through forward-biased diodes D_1 and D_2. An enhancement P-channel MOSFET transistor, Q_1, an International Rectifier (www.irf.com) IRF-9530, remains off because its gate receives a slightly positive reverse-gate-bias voltage due to zener diode D_4's forward-voltage drop. Each capacitor charges to approximately one-half the peak value of the rectified voltage minus the forward-voltage drops that D_1 and D_2 present. The full-wave bridge rectifier, D_5, or Graetz bridge, produces these drops (Reference 1).

When the discharge phase begins, D_1 gets reverse-biased, and capacitor C_2 discharges through the load that voltage regulator IC_1 presents. Subsequently, the anode voltage of diode D_1 continues to decrease, Q_1's gate-to-source voltage becomes negative, and the transistor conducts, allowing C_1 to discharge into the load through forward-biased diode D_3. In effect, the two capacitors charge in series and discharge in parallel into the load, halv-

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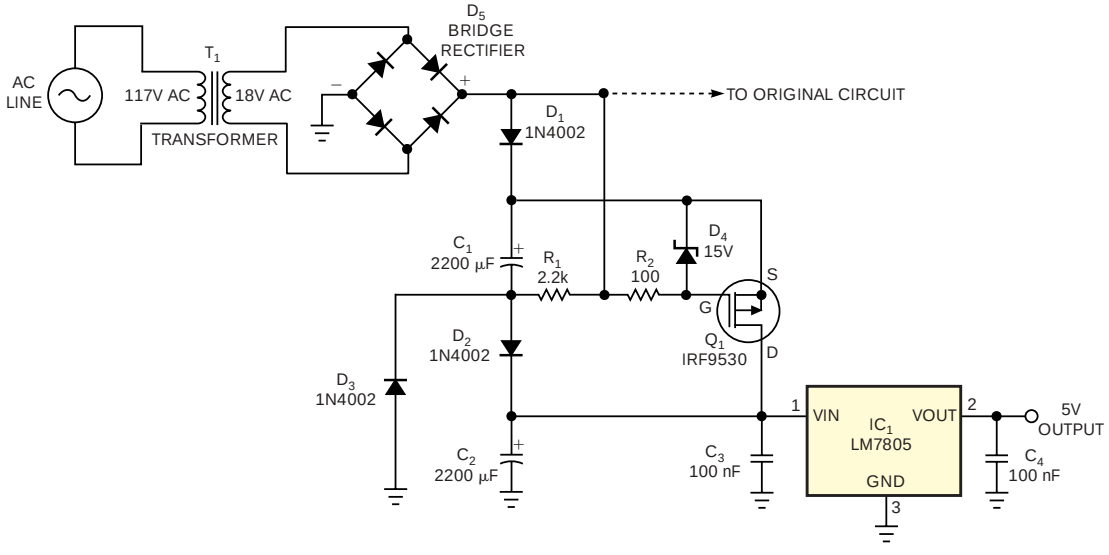

Figure 1 In this unconventional step-down circuit, capacitors C_1 and C_2 charge in series and discharge in parallel, reducing the voltage applied to regulator IC_1.

ing the raw rectified voltage and ripple voltage at IC_1's input. During C_1's discharge, zener diode D_4 protects Q_1 by clamping its gate-to-source voltage within its maximum rating.

To function properly, the circuit requires a minimum load current; the regulator's quiescent-current drain is usually enough. Otherwise, capacitor C_2 charges to the peak voltage available from D_5. The values of C_1 and C_2 and the ratings of the remaining components depend on the maximum load current required. The values of resistors R_1 and R_2 are not critical. Note that Q_1 functions as a switch; selecting a device with low on-resistance limits Q_1's power dissipation. EDN

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Line-powered driver lights up high-power LEDs

Aaron Lager, Masterwork Electronics, Rohnert Park, CA

Using LEDs has gained popularity as a method of saving power for general-purpose lighting, but an efficient method for driving them has also become a necessity. For example, Lumileds' (www.lumileds.com) Luxeon devices create lighting effects or room lighting. Providing power to a few LEDs may require only a current-limiting resistor, but illumination applications need a string of 20 or more LEDs to provide light over an area. Based on On Semiconductor's (www.onsemi.com) NCP1200A, a 100-kHz PWM current-mode controller for universal offline power supplies, the circuit in Figure 1 provides a low-cost, offline constant-current source for powering multiple LEDs. Although designers typically configure it to provide a voltage source, in this application, the NCP1200A provides a constant-current source. Figures 2 and 3 show close-ups of the circuit.

A full-wave bridge rectifier, D_2 to D_5, and filter capacitor C_1 provide approximately 160V dc to the conversion circuit, IC_1, and its associated components. Resistor R_3 alters the bias for IC_1's current-sense pin and, at 6.2 kΩ, allows the use of a 1.2Ω sense resistor for R_6. Decreasing R_6 not only reduces costs over a higher wattage sense resistor, but also improves the circuit's efficiency. Capacitor C_3 stabilizes the feedback network's current and carries a 400V rating in case of an open circuit in the LED string. An RC network comprising R_5 and C_4 provides a small amount of lowpass filtering to the CS pin.

Bleeder resistors R_1 and R_2 eliminate any shock hazard across the ac-line plug's prongs when you disconnect it. Although you can use a 1-MΩ through-hole-mounted resistor, two surface-mounted 500-kΩ series resistors cost less and provide the required track-

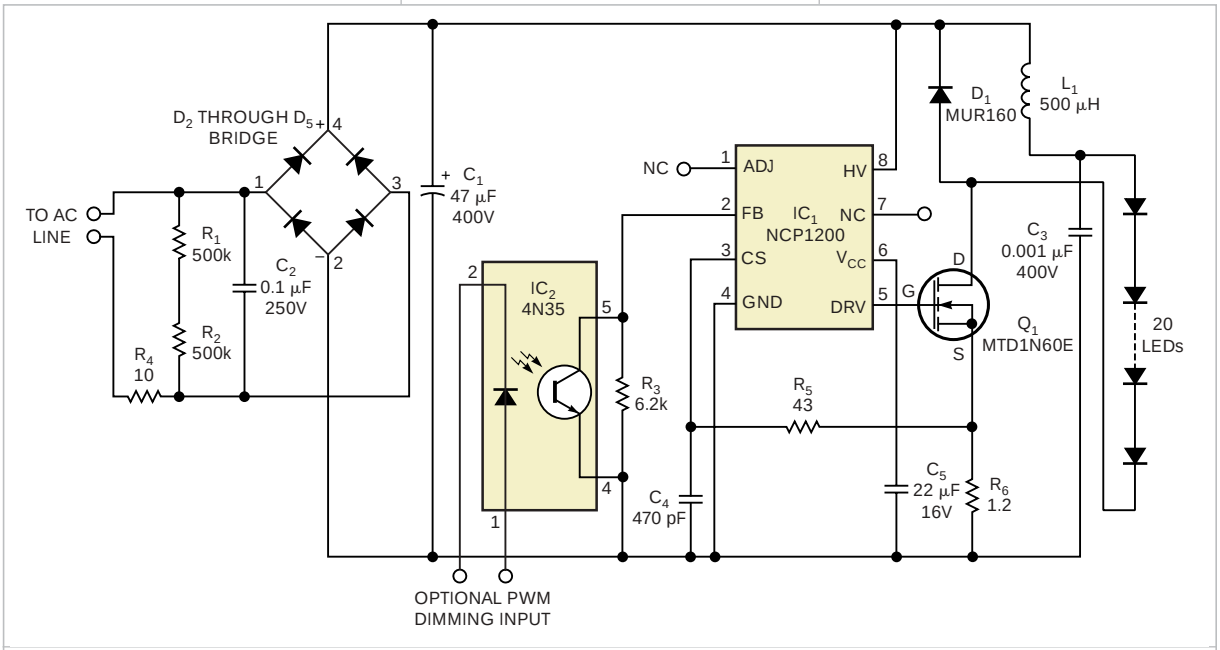

Figure 1 An offline constant-current source drives a string of high-output LEDs.

to-track pc-board spacing for line-voltage applications. Use a capacitor rated for line-bypass service for capacitor C_2. You can use any power MOSFET with a suitable breakdown voltage and a low on-resistance, such as an MTD1N60E or IRF820, for Q_1. Inductor L_1, a 500-μH device, should be able to operate at 100 kHz and handle more than 350 mA of continuous current. You can use an inductor from Coilcraft's (www.coilcraft.com) RFB1010 or DR0810 series of surface-mount inductors, or you can experiment with inductors manually wound on suitable core materials. As an option, adding optoisolator IC_2 allows microcomputer-controlled illumination dimming using pulse-width modulation of IC_1's feedback terminal, Pin 2.

To understand the economic motivation for using LEDs as illuminators, compare the light output of a string of 20 1W, white Luxeon emitters with a standard incandescent light bulb. Each LED provides 45 lumens, or 900 lumens for a string of 20 LEDs. The average forward voltage per LED is 3.42V for a power dissipation of 1.197W each at a forward current of 350 mA. Thus, the 20-LED string dissipates 23.94W. Factoring in a conservative 80% efficiency for the power supply, the power the system consumes becomes 28.73W for a light-emission-efficiency value of 900 lumens/29W or 31 lumens/W. The Luxeon emitters also carry a rating for 100,000 hours, or approximately 11 years, of operation.

Figure 2 A close-up view of the circuit of Figure 1 shows inductor L_1 in the upper right corner.

In contrast, a standard 60W Philips incandescent light bulb produces 860 lumens for 1000 hours, or just over a month, at an efficiency of only 14 lumens/W. From a power-consumption viewpoint, the LED-based design is twice as efficient as the incandescent-bulb-based design and thus reduces power consumption and cost. In addition, the LED design imposes no additional maintenance costs for replacement bulbs and labor. EDN

Figure 3 This version of the circuit comprises three constant-current driver channels. An LED light-bar assembly is above the pc board.

Rectifier tracks positive and negative peaks

Harry Bissell Jr, Welding Technology Corp, Farmington Hills, MI

Signals ranging from music to complex control-system waveforms may contain unequal positive and negative peak amplitudes. An "envelope-follower" circuit can track unequal peaks, but the ability to select a desired peak can enhance the circuit's performance (Reference 1). The circuit in Figure 1 applies a new twist to a classic absolute-value circuit. Applying an input signal to R_1 (full) produces an output equal to the input's absolute value. Applying an input signal to R_6 (positive) or R_7 (negative) produces outputs of positive or negative half-cycles, respectively. Figure 2 illustrates all three modes of operation.

Understanding the circuit is simple if you consider that op amp IC_{1A} strives to maintain its inverting input at virtual ground. For example, applying −1V to the negative input, R_7, drives the anode of D_1 to −333 mV. IC_{1A}'s output, Pin 1, drives D_2's cathode positive enough to force D_2's anode voltage to 333 mV. Because IC_{1A}'s inputs now rest at 0V, D_1 is effectively reverse-biased and out of the circuit. The 333 mV available at D_2's cathode also applies to IC_{1B}'s noninverting input, Pin 5, and IC_{1B} must balance its input voltages by driving its output, Pin 7, to 1V. IC_{1B}'s inverting input, Pin 6, goes to 333 mV. The voltage drop across R_4 thus equals 666 mV. One-third of the input current flows through the series connection of R_2 and R_3, and two-thirds flows in R_4. To achieve unity gain, R_7's value equals that of R_2+R_3 in parallel with R_4.

Applying a positive input to R_7 causes IC_{1A}'s output to go negative by a voltage equal to one forward-diode drop and thus holds D_1's anode at ground. D_2 is reverse-biased, and both of IC_{1B}'s inputs rest at 0V. The circuit's output is thus 0V. Applying an input voltage at R_6 yields similar operation. A positive input causes an equal-value positive output, and a negative input produces a 0V output. You can ignore the effects of IC_{1B}'s high input impedance, which are negligible. To maintain unity gain, the value of R_6 is twice that of R_3.

Resistors R_1, R_2, R_3, R_4, and R_5 are of equal value and close tolerance. Note that IC_1's power-supply connections require bypass capacitors (not shown). To minimize errors, use a low-impedance source or buffer amplifier to drive the circuit. You can use a three-posi-

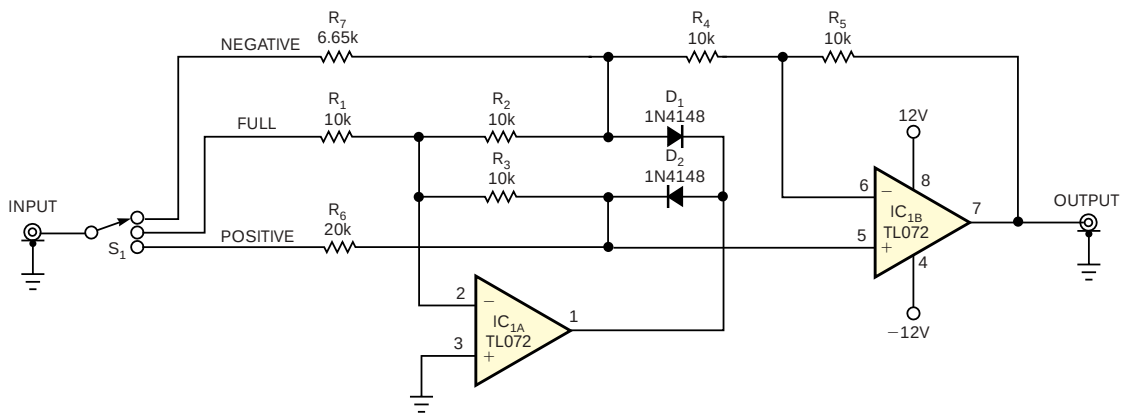

Figure 1 Use this versatile precision rectifier circuit to recover a signal's positive peaks, negative peaks, or both in full-wave mode.

tion rotary switch for input-mode selection, or an on/on/on toggle switch, such as C&K Components' 7211, available from Digi-Key Corp (www.digikey.com) and other sources, or a similar switch, wired as a three-way selector. (See the manufacturer's data sheet for a connection diagram.) You can also use separate connectors for the inputs, but connect no more than one input at a time.EDN

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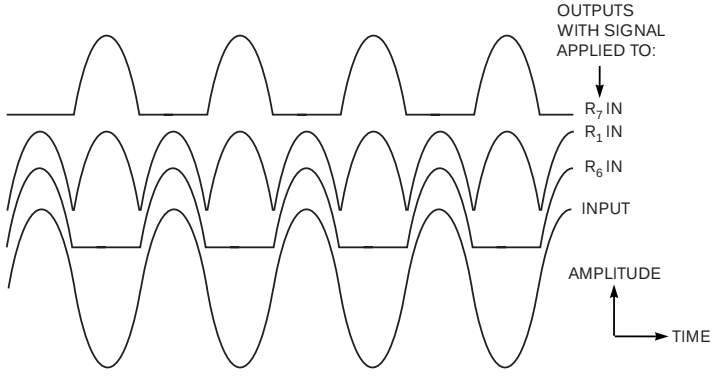

Figure 2 This waveform plot shows the circuit's outputs for a sine-wave input connected to the negative, full, and positive inputs, respectively. Traces are vertically offset for clarity.

Isolated indicator signals telephone line's status

Yongping Xia, Navcom Technology, Torrance, CA

Part 68 of the FCC's (Federal Communications Commission, www.fcc.gov) telecommunications regulations requires that certain signaling equipment connecting directly to the public-telephone network must present a line-to-line resistance of at least 5 MΩ. In addition, status signals that equipment derives from the phone lines must include electrical isolation to prevent interaction between earth grounds from the telephone network and attached control or communications equipment. Although a transformer can provide isolation for voice-frequency signals, the telephone-line-status-indicator circuit in Figure 1 meets FCC isolation requirements without incorporating a transformer (Reference 1). A diode bridge, D_1 through D_4, and R_1, a 5.6-MΩ resistor, supply a small amount of dc power from the phone line to a nanopowered combination comparator and a 1.2V voltage reference, IC_1. The Maxim (www.maxim-ic.com) MAX917 IC draws only 0.75 µA at $1.8V_{CC}$.

Resistors R_2 and R_3 form the detection-voltage divider, and R_4 provides hysteresis. When IC_1's output goes low, R_4 and R_3 form a parallel combination of 3.26-MΩ resistance. To reach the comparator's reference voltage of 1.245V, the voltage across C_1 must reach at least 5.06V. Once IC_1's output

goes high, R_4 and R_2 form a parallel resistance of 6.67 MΩ, and the voltage across C_1 must reach 3.37V to deliver a 1.245V input to the comparator. IC_1's output drives a photocoupler, IC_2, a Toshiba (www.semicon.toshiba.co.jp) TLP190B. Unlike other photocouplers, IC_2 includes an array of photodiodes that, when illuminated, delivers a voltage output. Although weak by power-conversion standards, the photocoupler's output can deliver several microamperes at an open-circuit voltage that exceeds 7V, or enough to drive a MOSFET's gate or a microprocessor's input pin. In addition, the TLP190B carries a 2500V-rms emitter-to-detector isolation-voltage rating.

When a telephone is not in use, the on-hook voltage across its line of approximately −48V produces a current of 7 to 8 µA through R_1, which imposes a low-leakage requirement on C_1. The prototype version of the circuit uses an X5R-characteristic ceramic capacitor. When the voltage across C_1 exceeds 5.06V, IC_1's output goes high and drives IC_2 through R_5, discharging C_1. When the voltage across C_1 decreases to 3.37V, IC_1's output goes low, and C_1 recharges. The output from IC_2 comprises a 1.4-msec-wide voltage pulse with a repetition period of approximately 240 msec. When the phone is off the hook, the voltage across its lines drops to a few volts, which don't sustain pulse generation. EDN

REFERENCE

1 www.fcc.gov/wcb/iatd/part_68.html.

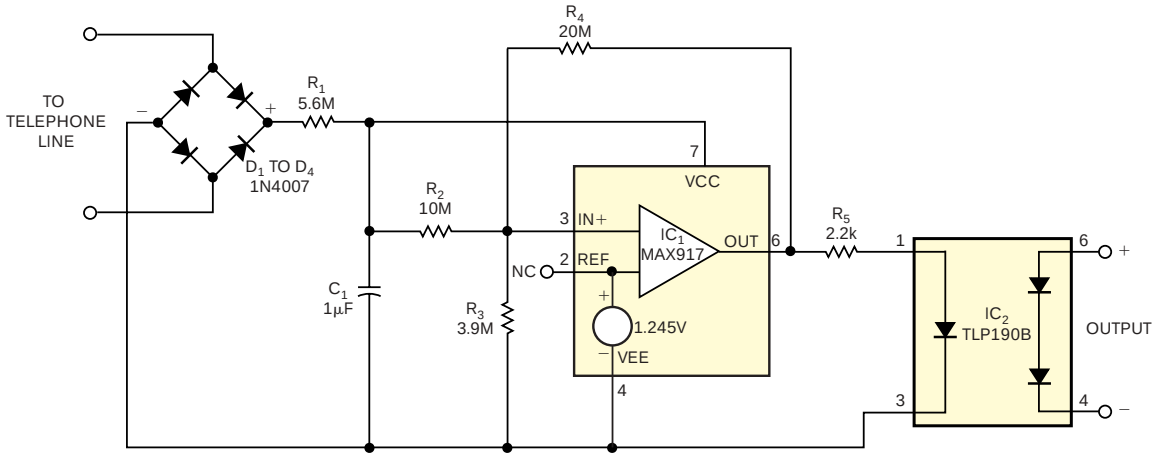

Figure 1 Drawing minuscule amounts of power from a telephone line, this isolated-output circuit indicates whether the line is in use.

Circuit converts DAC's outputs from single-ended to differential mode

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High-speed DACs, such as Analog Devices' AD9776/78/79 TxDAC family, offer differential outputs, but, for low-end ac applications or high-precision level-setting applications, a single-ended current-output DAC with a differential-conversion circuit provides a novel approach to generating differential-waveform-control functions. The basic circuit in Figure 1 combines a current-output DAC, IC_1, such as the 8-bit AD5424 DAC, with a single-ended-to-differential op-amp stage—IC_2, IC_{3A}, and IC_{3B}—to generate the desired outputs. For dual-power-supply applications, you select the DAC's unipolar mode of operation to achieve optimum performance from the DAC. Using a single op amp, the DAC provides two-quadrant multiplication or a unipolar output-voltage swing. The DAC's output requires a buffer because changing the code applied to the DAC's input varies its output impedance.

This equation defines the circuit's output voltage: $V_{OUT} = -V_{REF} \times (D/2^N)$, where N defines the number of input bits, V_{REF} is the reference voltage, and D is the decimal equivalent of the binary code. To generate a positive common-mode voltage, you use a negative voltage for the DAC's reference voltage. The DAC's internal design accommodates ac reference input signals of −10 to +10V. In this mode, the DAC provides a 5M-sample/sec maximum update rate for one-quarter full-scale code changes when you operate it from a 5V power supply. Use resistors R_1 and R_2 only if your application requires adjustable gain.

The single-ended-to-differential stage comprises two cross-coupled op amps, which resistors R_5 and R_6 configure as a unity-gain follower. To yield a symmetric circuit, the outputs also drive each other as unity-gain inverters through R_7 and R_8. The voltage you apply to the positive terminal of op amp IC_2 sets the circuit's common-mode voltage. Resistors R_3 and R_4 control the amplitude of the differential voltage. Review your application's output-load requirements and the op amps' input- and output-voltage capabilities.

For single-supply applications, you can use a current-output DAC in reverse mode, in which you apply the reference voltage, V_{IN}, to the DAC's I_{OUT1} pin and take the output voltage from the DAC's V_{REF} terminal (Figure 2). In this configuration, a positive reference voltage produces a positive output voltage. This circuit does not use the DAC's feedback resistor, R_{FB}, and its connection to I_{OUT1} prevents stray capacitance effects. The DAC's reference input "sees" an impedance that varies with the applied code and thus requires a low-impedance source.

Note that the switches in the DAC ladder no longer have the same source-to-drain drive voltage, which in turn limits the input voltage to low voltages. As a result, the switches' on-resistances differ and degrade the DAC's linearity. Also, this mode limits the max-

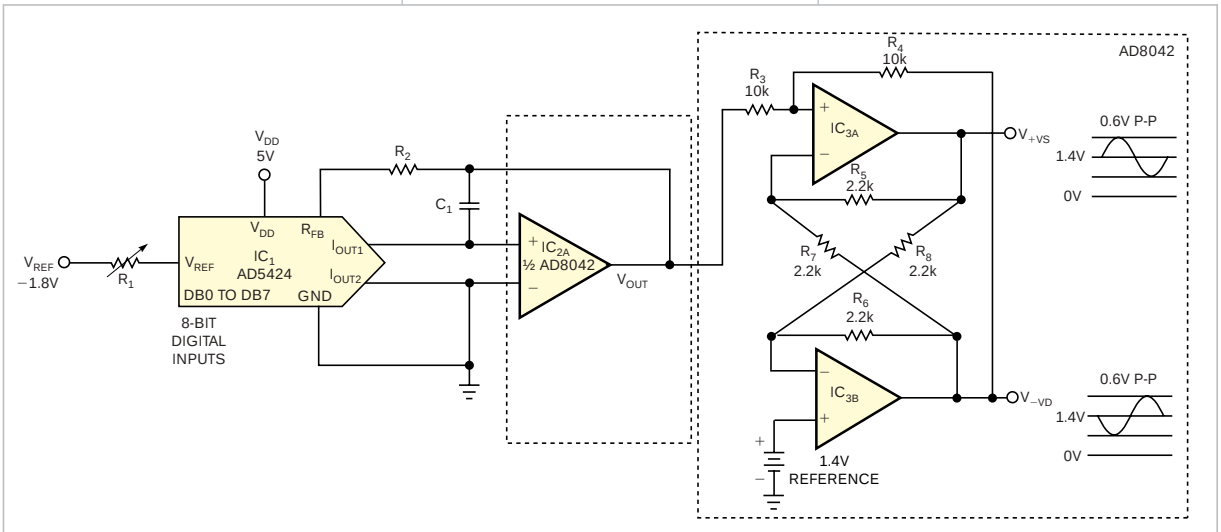

Figure 1 This basic circuit combines a current-output DAC, IC_1, with a single-ended-to-differential op-amp stage–IC_2, IC_{3A}, and IC_{3B}–to generate the desired outputs.

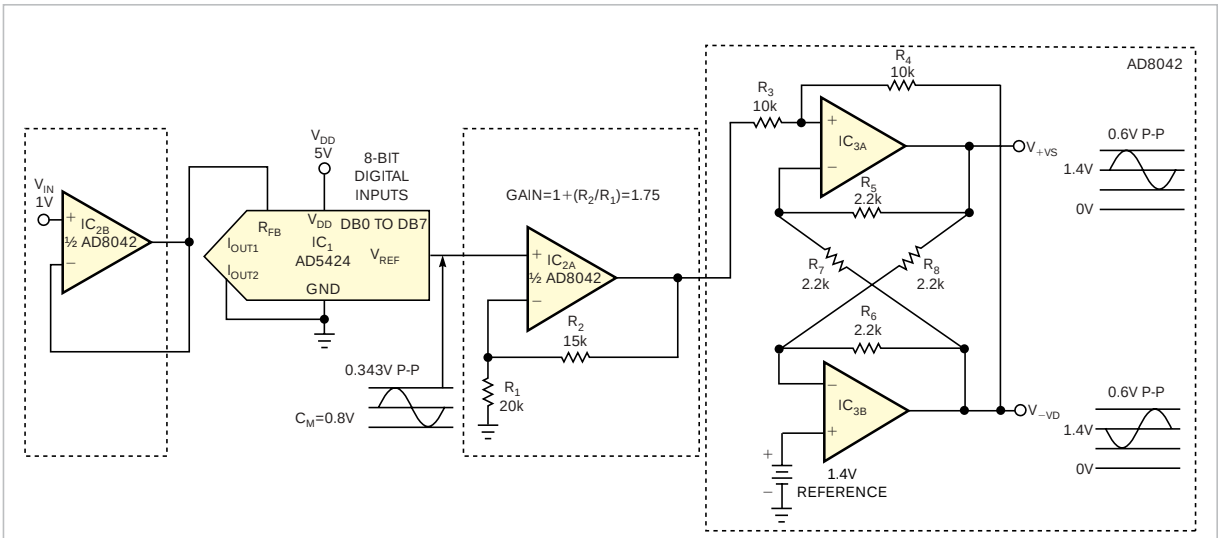

Figure 2 In this configuration, a positive reference voltage produces a positive output voltage.

imum update rate to 1.5M samples/sec. You can use sections of a dual op amp to buffer the DAC's input and to amplify the DAC's output voltage (Figure 3). The circuit's intended application determines your choice of supporting amplifiers. For lower speed, precision applications, the op amp requires low input-bias currents and low input-offset voltage to avoid degradation of the DAC's DNL (differential-nonlinearity) performance. For example, the AD8628 offers 100-pA maximum bias current at room temperature and 5-μV maximum input-offset voltage. The op amp's low-frequency noise is important in precision level-setting applications, and the AD8628 specifies 0.1- to 10-Hz noise of less than 0.5 μV p-p. Its rail-to-rail inputs and outputs make it ideal for use in single-supply circuits.

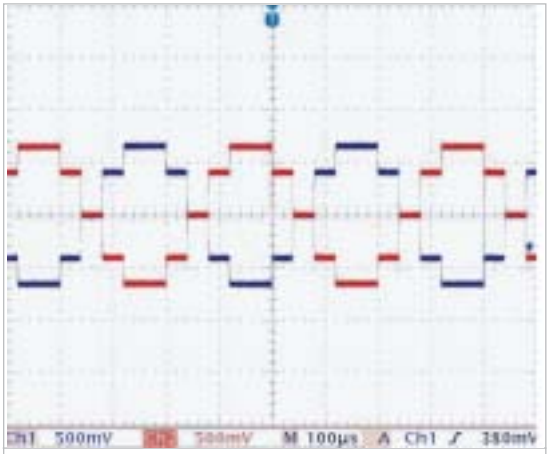

Figure 3 The single-ended-to-differential conversion of a digitized, eight-point sine wave produces differential outputs.

For high-speed-system applications, the op amp's slew rate must not dominate the DAC's slew rate. The op amp's bandwidth must be large enough to drive the feedback load and must not limit the circuit's overall bandwidth, and the DAC's output- voltage settling time should determine the circuit's maximum update rate. The AD8042 in figures 1 and 2 offers 170-MHz bandwidth and a 225V/μsec slew rate, allowing it to easily achieve these results. Other high-speed op amps, such as the AD8022, AD8023, and AD8066, also work well in this application.

The DAC consumes only 0.4 μA of power-supply current, and the op amps thus dominate the circuit's power consumption. To minimize the area for the circuit on a pc board, you can replace all four op amps in Figure 2 with a single AD8044 quad op amp. The single-ended-to-differential conversion of a digitized, eight-point sine wave in the presence of a 1.4V common-mode voltage and a 0.6V differential signal produces differential outputs (Figure 3). EDN

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READERS SOLVE DESIGN PROBLEMS

Microcontroller, JFET form low-cost, two-digit millivoltmeter

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The circuit in Figure 1 offers an inexpensive alternative to commercial digital voltmeters. Although it has only two digits, it provides considerable flexibility and thus lends itself to customization by means of a microcontroller and its software. As one of Microchip's (www.microchip.com) least expensive offerings, the PIC16F84A lacks an internal ADC. However, you can use a classic RC time-delay circuit to implement an analog-to-digital conversion by connecting capacitor C_3 between lines RB7 (output) and RA4 (input) and in series with an equivalent "unknown" resistor consisting of Q_3's drain-to-source on-resistance, plus R_4, plus R_5. Q_3, a BF245A JFET, presents the on-resistance. Q_3's "A" suffix is important because it corresponds to an on-resistance of 200Ω to 2 kΩ for a gate-to-source voltage of 0 to 1V (Figure 2). Other devices in the BF245 family exhibit a less pronounced change of resistance versus gate-to-source voltage. To correct the measurement nonlinearity inherent in Q_3's gate-to-source voltage versus drain-to-source on-resistance transfer, the microprocessor's software includes a 100-point look-up table that provides correction for a two-digit display.

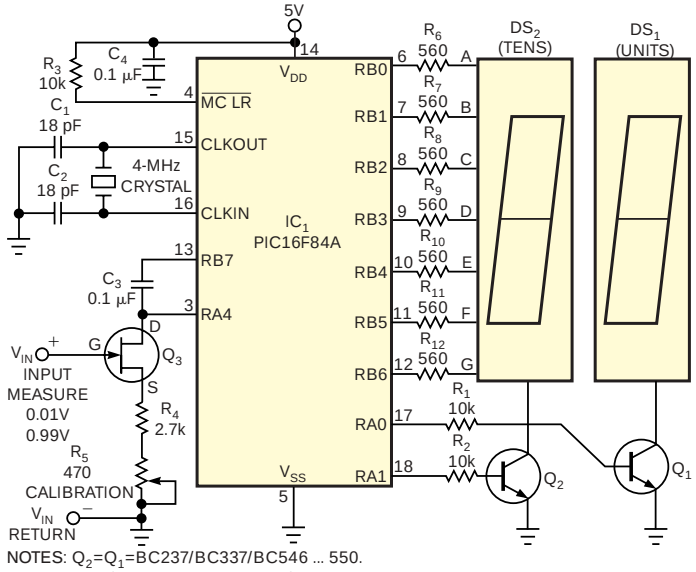

Figure 1 Build a low-cost, two-digit dc millivoltmeter from a microprocessor and a few components.

For an application requiring the display of readings of 0.01 to 0.99V, you can use a 4-MHz crystal and Microchip's PIC16F84A microprocessor for IC_1. To display the rightmost three digits of readings in the 0.001 to 0.999V range, use a 20-MHz crystal and a PIC16F84A-20 microprocessor. Choose 15- to 33-pF values for capacitors C_1 and C_2, which the PIC's data sheet describes. Listing 1, which is available online at www.edn.com/060622di1, includes the full assembler source code for the PIC16F84A. The most critical portion of the firmware comprises a subroutine that provides a precision time delay according to the following steps:

1. Configure RA4 as an input to sense the voltage across C_3 during the charging interval. When you configure RA4 as an input, it serves as a Schmitt trigger with 1.6V low-threshold and 3.2V high-threshold voltages when drain-to-drain voltage is 5V.
2. Configure RB7 as an output and set it high to begin charging C_3. Initialize a counter (register $0C_H$) to its maximum value of FF_H.
3. Decrement the counter in a loop

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until RA4 senses a low state. At that time, C_3 charges to nearly 66% of the power-supply voltage.

4. Use the time it takes to produce a low on the RA4 input as a jump value in the linearity-correction look-up table to extract a value for the two-digit LED readout.
5. Configure RB7 as an input and set it low to discharge capacitor C_3.
6. After a time delay, repeat Step 2.

To round out the design, another software subroutine solves the problem of driving a two-digit LED display at adequate visibility with a minimum amount of current. Although an LCD would use less current, LCDs aren't visible in darkness. The display subroutine examines the eight bits of the units and tens—registers 11_H and 12_H—and tests each one in sequence; if the subroutine sets a bit, then the subroutine puts a short-duration high state on its corresponding segment-driver line, RB. Doing so lights only one LED segment at a time, and, consequently, the maximum current consumption of the circuit remains relatively constant even if you add a third LED display to build a 999-count millivoltmeter.

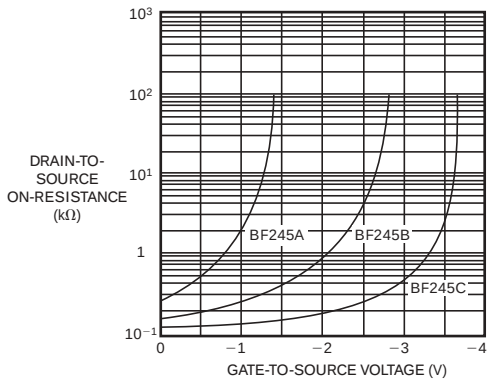

Figure 2 Gate-to-source-voltage-versus-drain-to-source-resistance-transfer curves for three selected grades of the BF245 JFET show maximum resistance variation for the "A" grade at low gate voltage.

Persistence of vision eliminates the need to keep the displayed digits continuously visible, and maintaining the segments on for approximately 33% of a 1-sec refresh interval allows a good and sufficient display effect. Transistors Q_1 and Q_2 are never simultaneously on, and only one display segment lights at a time. You can further optimize the hardware by removing current-limiting resistors R_6 through R_{12}, lifting the emitters of Q_1 and Q_2 from ground, and inserting a single 560Ω resistor between the emitters and ground. EDN

Inexpensive envelope tracker handles wide signal variations

Anthony H Smith, Scitech, Bedfordshire, England

Converting band-limited NRZ (non-return-to-zero) data to a digital format suitable for microprocessors and other digital systems poses problems when a signal's duty cycle or amplitude varies or when its average level unpredictably wanders within a given dc range. Transferring the signal to a fixed-reference comparator using ac coupling produces poor results because changes in duty cycle cause variations in average signal level that result in jitter or distortion of the output signal's timing.

Based on diodes and RC networks, an envelope tracker creates a voltage between the input signal's excursions (Reference 1). Using the midpoint voltage as a reference, the comparator generates a digital output signal that faithfully replicates the original signal's timing information. Although highly effective for relatively large signals, a diode-based circuit can introduce errors or even fail completely for inputs that are small relative to a diode forward-voltage drop or when the input's average level drifts toward either of the circuit's supply-voltage rails.

Requiring no diodes, the single-supply circuit in Figure 1 reconstructs a band-limited NRZ data stream whose duty cycle can vary from less than 5% to more than 95% and whose amplitude varies from less than 100 mV to the supply-rail voltage—5V, for example. Furthermore, the circuit tolerates an average signal level that falls between the two supply rails. The circuit comprises triple analog switch IC_1, dual comparator IC_2, and a few passive components.

The circuit functions as a self-clocking envelope tracker by sampling the input signal's upper and lower levels, V_U and V_L, and generating corresponding dc levels, V_{UC} and V_{LC}, on capacitors C_3 and C_4. Two equal-valued resistors, R_4 and R_5, between C_3 and C_4, produce a third voltage, V_{MID}, that's equivalent to the input signal's midlevel voltage, V_M. Capacitor C_2 smoothes and filters V_{MID}, which serves as a reference potential for output comparator IC_{2B}. R_2, R_3, and C_1 provide temporal hysteresis, ensuring clean switching of V_{OUT}, even for relatively small inputs.

To understand the circuit's operation, assume that C_4, C_2, and C_3 all discharge; that is, V_{LC}, V_{MID}, and V_{UC} are all 0V. Because input signal V_{IN} is greater than V_{MID} and the potential at IC_{2A}'s inverting input, both comparators' outputs go high and cause the three analog switches to assume the positions in Figure 1. Now, assume that V_{IN} is at its positive peak amplitude, V_U. Capacitor C_3 now charges through R_1 and the on-resistances of the three switches. Provided that C_3 is not too large, V_{UC} rapidly acquires a value roughly equal to V_U.

When V_{IN} falls below V_{UC}, comparator IC_{2A}'s output goes low and

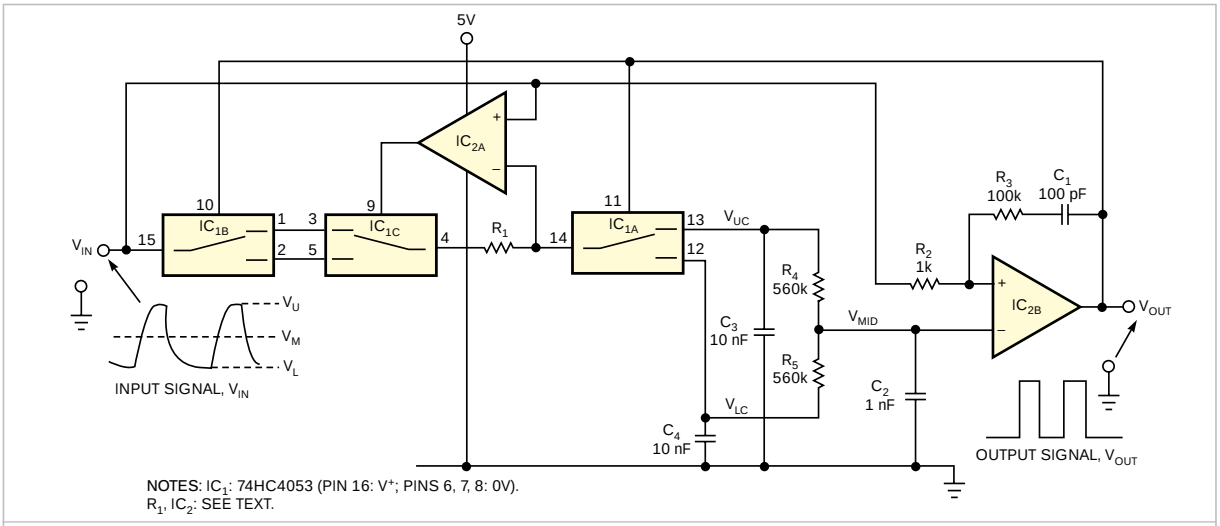

Figure 1 This circuit tracks an NRZ signal's envelope excursions and recovers the original waveform.

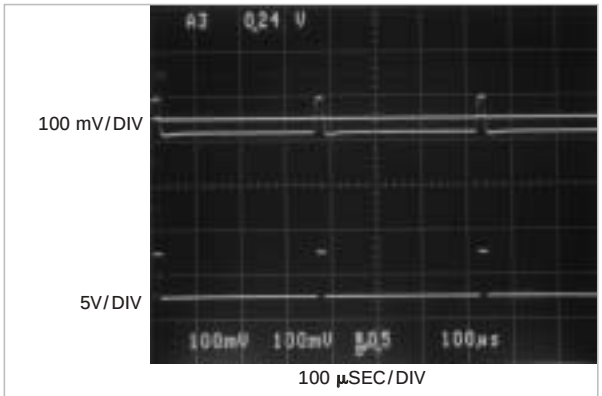

Figure 2 The lower trace shows the envelope tracker's response to a bandwidth-limited, low-duty-cycle, low-amplitude input signal. The horizontal line in the upper trace shows the signals' recovered midpoint voltage, V_{MID}.

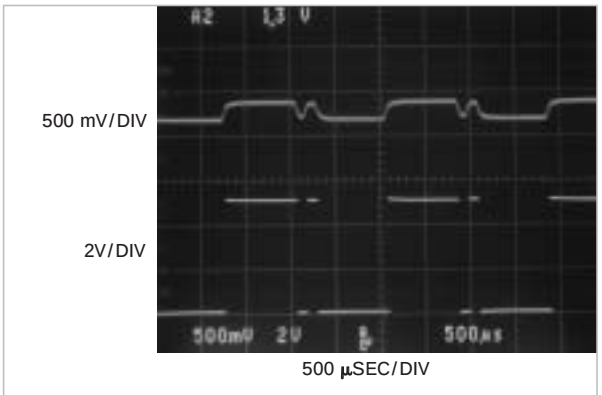

Figure 3 The lower trace shows the envelope tracker's output signal recovered from an inductively coupled data transceiver.

forces analog switch IC_{1C} to change state and disconnect C_3 from V_{IN}. Ignoring comparator input-bias currents and assuming negligible switch-leakage currents, C_3 can now discharge only through R_4. If R_4 is large enough, the relatively slow discharge rate allows V_{UC} to remain roughly equal to V_U.

During C_3's charging interval, C_2 also charges through R_4. Depending on the values of C_2 and R_4 and on the duration of the input signal's positive-going pulse, voltage V_{MID} may exceed the input signal's lower level, V_L. If V_{MID} exceeds V_L, comparator IC_{2B} trips when V_{IN} approaches V_L, and the resulting low level at V_{OUT} causes both IC_{1A} and IC_{1B} to change state. Capacitor C_4 now connects to V_{IN} through R_1 and the switches' on-resistances and quickly charges to a level at which V_{LC} approximately equals V_L.

Depending on component values and on the input signal's timing parameters, several cycles may elapse before the circuit's voltage levels stabilize at their quiescent values, at which $V_{UC} \approx V_U$, $V_{LC} \approx V_L$, and $V_{MID} \approx V_M$. However, careful selection of components ensures that the circuit rapidly reaches equilibrium. Ensuring that the comparator trips properly when V_{IN} goes below V_U or above V_L requires that R_1 provide a minimum amount of impedance of 100Ω to 1 kΩ between V_{IN} and IC_{2A}'s inverting input. Higher values result in sluggish charging of C_4 and C_3. In many designs, the combined on-resistances of IC_{1B} and IC_{1C} may allow omission of R_1.

The presence of IC_{1B}, IC_{1C}, and IC_{2A} ensures that C_3 can charge when V_{IN} is close or equal to V_U and that C_4 can charge only when V_{IN} is close or equal to V_L. Without IC_{1B}, IC_{1C}, and IC_{2A}—that is, with V_{IN} connected directly to R_1—C_3 would discharge on the downward slope of V_{IN} between V_U and V_M

and would thus pull down V_{UC}. Similarly, C_4 would continue to charge on the upward slope of V_{IN} between V_L and V_M and would thus pull up V_{LC}. Although V_{MID} might be roughly equal to V_M, such a minimal configuration performs relatively poorly, particularly for small signals and at extreme duty cycles.

The components in Figure 1 produce good results for input frequencies of 5 to 50 kHz. Frequencies lower than 5 kHz may require larger capacitor values, and operation higher than 50 kHz may require reduction of capacitors' values and selection of a comparator with minimal response time. With properly selected components, the circuit performs well at baud rates to or exceeding 128 kbps.

The values of R_5, R_4, C_2, and, to a lesser extent, the analog switches' on-resistance and R_1, C_4, and C_3 determine the circuit's response time to a sudden change in input-signal amplitude or average level. Making C_2 approximately 10 times smaller than C_4 and C_3 ensures a rapid "attack" time, but too small a value can result in excessive ripple and noise on V_{MID}. For reliable operation, use equal values of close-tolerance resistors of 100 kΩ to 1 MΩ for R_4 and R_5. If you use high-value resistors for R_4 and R_5, choose a comparator with low input-bias currents for IC_2. For detection of signals that might approach the positive-supply rail, the 0V rail, or both, make sure that IC_2 offers rail-to-rail input capability. Bypass each IC's power-supply connections with low-impedance ceramic capacitors.

Note that, with no input signal present (that is, when applying a dc level to V_{IN}) V_{OUT} may contain random pulses caused by noise and the comparators' attempts at maintaining V_{MID} equal to V_{IN}'s average dc level. To eliminate the pulses, remove C_1 to replace temporal hysteresis with "normal" hysteresis, but ensure that the hysteresis levels that R_2 and R_3 set are not excessively large relative to the minimum input-signal amplitude.

Figure 2 shows the circuit's response to a bandwidth-limited input signal of approximately 5% duty cycle and 75-mV amplitude. The horizontal trace, V_{MID}, neatly bisects the waveform. The bottom trace shows the reconstructed signal at V_{OUT}. In Figure 3, the circuit processes the real-world output of an inductively coupled transceiver (upper trace) of approximately 200 mV p-p. Again, the lower trace shows the reconstructed signal at V_{OUT}.EDN

REFERENCE

1 Whipple, Roger C, "Envelope tracker quells jitter," *EDN*, July 7, 1994, pg 102, www.edn.com/archives/1994/070794/14di8.htm.

Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

Examine a traditional Hartley-oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance for a given frequency, finding the coupling coefficient, k, may require experimental, or "cut-and-try," optimization. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

Figures 1a and b show the Hartley oscillator's equivalent tuned circuit, the equations that calculate its components, and component values for an 18-MHz oscillator. The mutual inductance is $L_M = k\sqrt{L_1 \times L_2}$. For the equivalent circuit, the equations are: $L_A = -L_M$, $L_B = L_2 - L_A = L_2 + L_M$, and $L_C = L_1 - L_A = L_1 + L_M$. The rest of the equations for the equivalent circuit are:

$$C_A = -\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O = \frac{1}{2\pi\sqrt{(L_B + L_C)C}},$$

and

$$C_A = \frac{1}{(2\pi f_O)^2 k\sqrt{L_1 \times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, L_A.

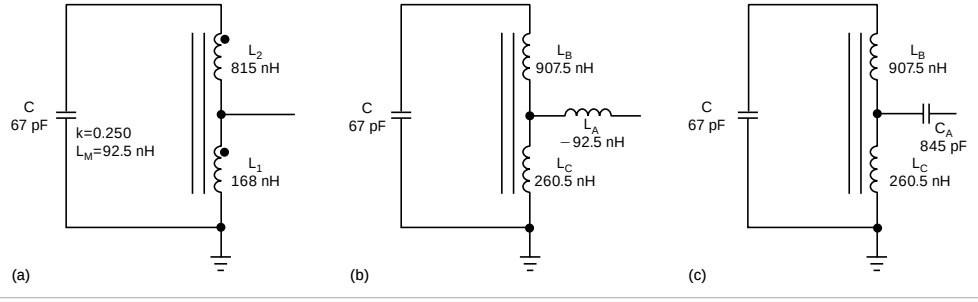

Figure 1 A traditional Hartley oscillator's resonant circuit comprises a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).

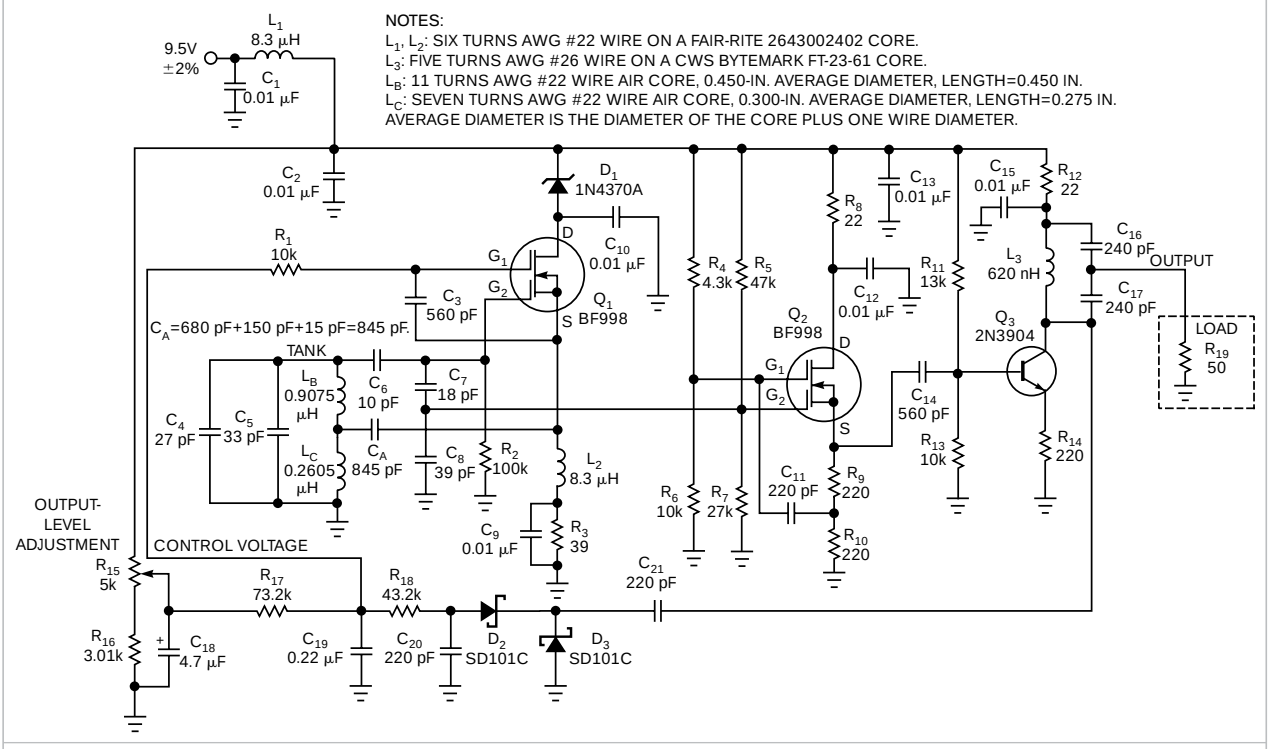

Figure 2 This buffered-output, 18-MHz oscillator has a resonant circuit that doesn't rely on mutual coupling for operation.

However, for frequencies near the resonant frequency, f_0, you can replace the negative inductor with a capacitor, in which C_A replaces L_A (Figure 1c). Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

Figure 2 illustrates an oscillator and output buffer using the equivalent circuit. The constructed circuit generally performs as you would expect from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design. The oscillator's tank circuit comprises L_B, L_C, C_4, and C_5, plus capacitance provided by voltage divider C_6, C_7, and C_8. This capacitance of approximately 6 pF includes Q_1's and Q_2's input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors L_B and L_C comprise air-core coils with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should comprise windings on dielectric or toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application. Reference 1 provides basic designs for both inductors, and adjusting the spacing of their turns tunes the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require readjusting the inductors' values.

The capacitive voltage divider comprising C_6, C_7, and C_8 applies the proper signal levels to Q_1 and Q_2. Because the divider "sees" the tank circuit's effective capacitance as only 6 pF, the remaining 60 pF can comprise a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage comprising Q_3 and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor C_3 bootstraps Q_1's Gate 2 to Q_1's source to provide additional gain from Q_1 and to reduce its Gate 1 input capacitance below its value of approximately 2.1 pF (Reference 2). An 8.3-µH inductor, L_2, connects to Q_1's source and presents relatively high impedance at 18 MHz and provides a dc path from Q_1's source to ground through R_3. The impedance of L_2 at 18 MHz comprises an inductive reactance of about 940Ω in parallel with a resistance of approximately 3.5 kΩ, which results in a choke with low resistive losses. You can substitute a smaller inductor for L_2 provided that its inductance and reactance approximate the original's values. You can use a standard-value 8.2-µH choke for L_2 provided that its resistive losses meet these low-loss criteria and that its inherent series resistance is 2Ω or lower to avoid upsetting Q_1's dc bias voltage. The inductance and resonance of the choke for L_1 are less critical than those for L_2, but using a choke with low resis-

tive losses at L_1 helps avoid spurious resonances.

Source follower Q_2 drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at Q_3's collector. Bootstrapping Q_2's Gate 2 by one-half of its output voltage increases the source follower's gain and dynamic range and reduces its input capacitance. Potentiometer R_5 adjusts the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. The circuit's frequency remains stable at a constant room temperature of about 23°C. Also, the output-level-control circuit remains stable even if you apply no load to the output. For a fixed-frequency oscillator, the output circuit's loaded resistive losses of approximately 4 provide adequate bandwidth without retuning L_3, C_{16}, and C_{17}.

To set the output level to a safe maximum, connect a 50Ω load to the output and adjust the output to 1.5V p-p. The drain-to-source voltage you apply to Q_1 remains at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding Q_1's specified maximum 12V drain-to-source voltage, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode D_1 reduces Q_1's drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit control the oscillator's gain by applying a variable voltage to Q_1's Gate 2 (Reference 3). In this design, a simple passive circuit serves the same purpose. A portion of the signal at Q_3's collector drives a voltage doubler comprising D_2, D_3, C_{20}, and C_{21}. The voltage doubler develops a negative voltage, part of which drives the junction of R_{18} and C_{19}, the control-voltage node. This control-voltage node also receives a positive voltage through R_{17} from variable resistor R_{15}, and the resultant voltage sets the output-signal level. At start-up, only a positive voltage is present at Q_1's Gate 2, and Q_1's maximum gain easily starts the oscillator. When the output reaches steady state, the control voltage decreases and maintains oscillation at a signal level that the output-level control determines. EDN

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READERS SOLVE DESIGN PROBLEMS

Error compensation improves bipolar-current sinks

Christian de Godzinsky, Planmeca Oy, Helsinki, Finland

You can improve a current sink's accuracy by at least two orders of magnitude by adding two standard 1%-tolerance resistors. As a bonus, you also compensate for errors that a low-current-gain pass transistor's base current introduces. To do so, you measure the transistor's base current and add a proportionally scaled error term to the source's reference voltage. When you design a current sink, you can use a MOSFET for the sink's pass transistor because of its nearly infinite power gain and low gate current. However, a high-power MOSFET presents high input and output capacitances that reduce the sink's high-frequency output impedance.

As an alternative, a low-current-gain, bipolar power transistor presents a much lower output capacitance than does a MOSFET of comparable power ratings. Figure 1 shows a design for a bipolar-transistor-based current sink that unfortunately suffers from accuracy errors due to Q_1's base current's flowing into the current-measurement resistor R_1. The base current varies with changes in Q_1's collector current and current gain, which in turn depend on Q_1's production tolerances, junction temperature, and collector-emitter voltage.

You can use a Darlington transistor to increase the circuit's current gain and reduce the output error, but few Darlington transistors offer good high-frequency parameters. Superbeta power transistors are rare, have typically lower unity-gain-bandwidth frequencies, and are more expensive. In other words, even though a bipolar transistor presents higher output impedance at high frequencies, the error from its base current makes it a poor choice for a high-precision current sink. You could compensate for base-current errors by measuring the output transistor's collector current and introducing a correction factor, but that approach increases circuit complexity and reduces the sink's output impedance.

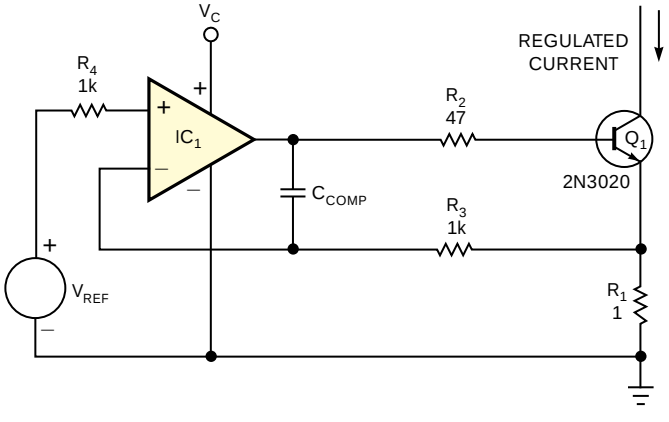

Figure 1 This typical quickly responding constant-current sink uses a bipolar transistor but suffers from base-current-induced error. Its nominal output current is $I_{OUT}=(V_{REF}/R_1)-I_B$.

Figure 2 shows a better approach, which adds a differential amplifier, IC_2, and resistors R_6 through R_9 to measure Q_1's base current by sampling the voltage across R_2. Resistors R_4 and R_5 scale and sum the error and reference voltages you apply to differential amplifier IC_1. Because IC_1's inverting input connects to current-shunt resistor R_1's upper end and not to ground, the reference voltage, V_{REF}, determines the error voltage applied to Q_1, preserving output scaling and allowing output-current calculation as V_{REF}/R_1. As a result, the regulated voltage across R_1 represents the sum of the desired output current plus the transistor's base current. Because the transistor inherently "subtracts" its base current, its collector current and, hence, the output current have no base-current error.

You can simplify the circuit and preserve its error-correction properties by combining IC_1 and IC_2; better yet, you can add two resistors to Figure 1 to

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achieve the same effect. Figure 3 shows the final circuit. To understand its operation, think of the circuit as a voltage regulator that delivers a voltage equal to V_{REF} across R_1. If you short-circuit base resistor R_2, note that any common-mode error that resistors R_5 and R_6 introduce cancels and thus has no effect on Q_1's base voltage. When you feed the voltage drop back to IC_1's input through R_5 and R_4, the voltage drop across R_2, representing Q_1's base current, increases the regulated voltage across R_1 by the ratio of R_5/R_4. If the ratio of R_5/R_4 equals that of R_2/R_1, the voltage across R_1 includes an error term that effectively cancels the base current. If $R_3=R_4$ and $R_5=R_6$, the following equation describes the output current, I_{OUT}:

$$I_{OUT}=\frac{V_{REF}+I_B\times R_2\times\frac{R_4}{R_5}}{R_1}-I_B.$$

Because the base current, I_B, appears twice with opposite signs and cancels, the equation simplifies to: $I_{OUT}=(V_{REF}/R_1)$.

To optimize the circuit's performance, use the following resistor ratios: $R_2/R_1=R_5/R_4$, $R_5=R_6$, $R_3=R_4$, $R_5>>R_4$, and $R_3>>R_1$. Using standard 1%-tolerance resistors in the circuit of Figure 3 reduces the error from Q_1's base current to about one-one-hundredth of its uncompensated level. Without compensation, a low-gain power transistor with a typical current gain of 25 at Q_1 would introduce a full-scale current error of 4%. The circuit corrects the error to 0.04% and raises Q_1's current gain to an effective current gain of 2500. Perfect matching would result in an immeasurably small base-current error. Note that IC_1's input common-mode-voltage range must include the negative-supply-voltage rail. Equal resistances at both of IC_1's inputs balance the op amp's input-bias currents. The minimum power-supply voltage depends on IC_1's maximum current-sourcing capability and on the sum of the worst-case voltage drops across Q_1's base-emitter junction, R_1 and R_2. The circuit's maximum output current depends on Q_1's worst-case minimum current gain times IC_1's worst-case minimum output current.

To ensure stable operation, use a unity-gain-stable op amp for IC_1. When the circuit operates within its nominal current range, an op amp whose response time is substantially

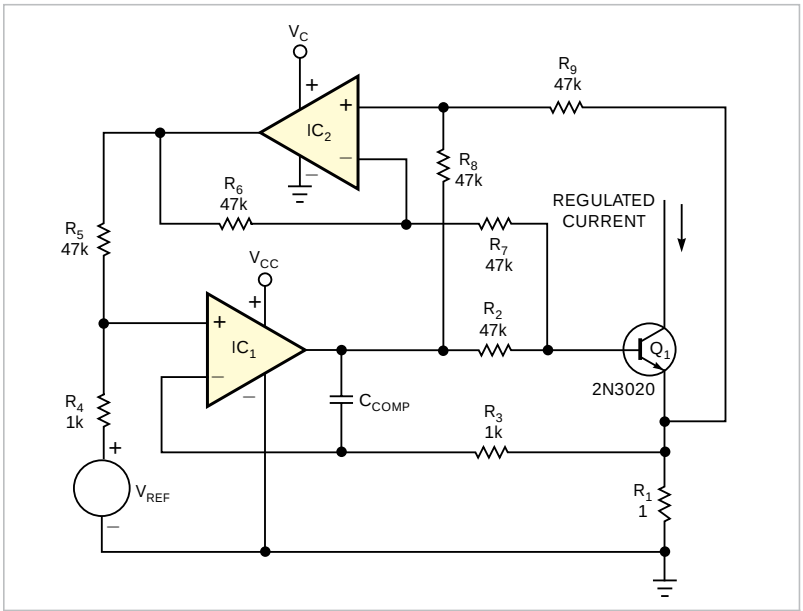

Figure 2 Adding base-current error compensation improves the circuit's performance. Using perfectly matched resistors simplifies the output-current equation to $I_{OUT}=(V_{REF}/R_1)$.

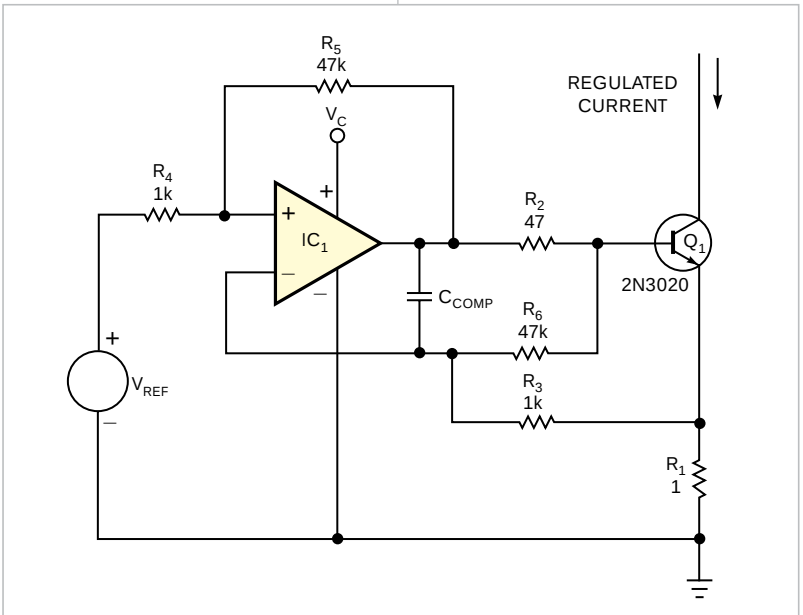

Figure 3 You can further simplify the current sink's design by adding only two resistors, R_5 and R_6, to the original in Figure 1. The output-current equation remains $I_{OUT}=(V_{REF}/R_1)$, as in Figure 2.

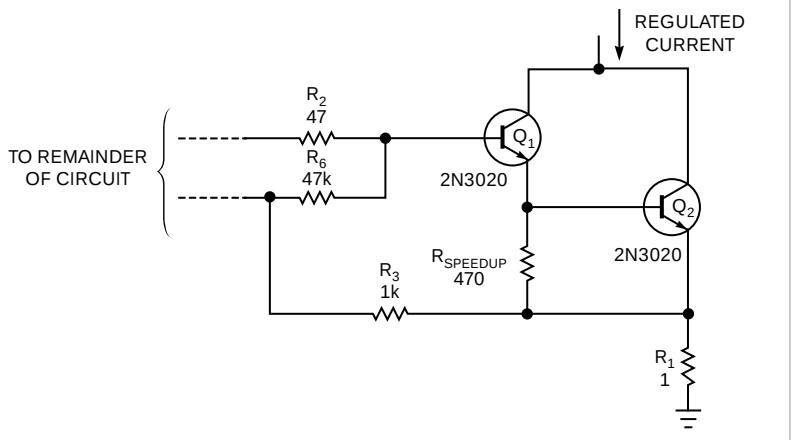

Figure 4 Adding $R_{SPEEDUP}$ improves the performance of a two-transistor Darlington output stage.

longer than Q_1's generally doesn't require installation of compensation capacitor C_{COMP}. However, a small capacitor of a few tens of picofarads guarantees stability under all conditions—for example, when the circuit's output current and the feedback voltage across R_1 approach zero.

The circuit in Figure 3 works equally well if you use a Darlington transistor for Q_1 because its higher current gain further improves the circuit's operation. If you use two discrete bipolar transistors, you can improve the composite Darlington transistor's turn-off time by connecting a resistor between the output transistor's base and emitter to remove its excess base charge (Figure 4).

You can use either a fixed or an adjustable reference-voltage source, but for the smallest possible error, the reference source's output impedance should be fairly low to sink feedback current from R_4. You can also proportionally increase the values of resistors R_3 through R_6 to reduce the amount of current that the reference source absorbs. It's amazing what you can achieve by adding only two resistors to an already-simple circuit. EDN

Phase-sequence indicator uses few passive components

Metodi Iliev, University of California—Berkeley

In a three-phase ac system, a power source with three wires delivers ac potentials of equal frequency and amplitudes with respect to a zero-potential wire, each shifted in phase by 120° from one wire to the next. Two possibilities exist for establishing a phase sequence. In the first, voltage on the second wire shifts by 120° relative to the first, and, in the second, a −120° shift occurs with respect to the first wire. Phase order determines the direction of rotation of three-phase ac motors and affects other equipment that requires the correct phase sequence: a positive 120° shift. You can use a few low-cost passive components to build a phase-sequence indicator.

Figure 1 shows a conceptual circuit that can detect both phase sequences. For certain component values, the following conditions apply: The voltages across R_1 and C_2 are equal—that is, their magnitudes and phases are the same—only when V_{S2} occurs exactly 120° ahead of V_{S1}, which indicates the correct phase sequence. In this case, the voltage between points A and B is zero. Conversely, the voltages across C_2 and R_3 are equal only when V_{S2} is ahead of V_{S3} by 120°, which corresponds to a reversed sequence.

Referring to the phasor diagram in Figure 2, when the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$. The following equations satisfy these conditions: $|V_{R1}|=|V_{C2}|=(1/2)|V_{S2}|=(1/2)|V_{S1}|$, and $|V_{C1}|=|V_{R2}|=\cos(30°)|V_{S1}|=\cos(30°)|V_{S2}|$. You calculate the component values by solving the following equations: $|X_{C1}|=\tan(60°)\times R_1=\sqrt{3}\times R_1$, and $R_2=\tan(60°)\times|X_{C2}|$, where $X_C=-j[1/(2\pi\times f\times C)]$, and f represents the frequency of the V_S voltages.

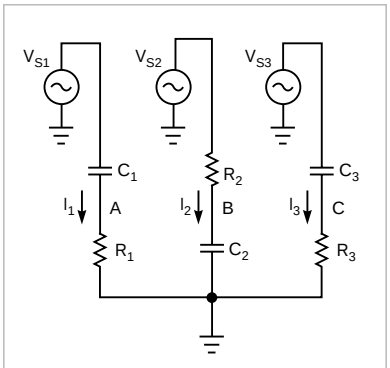

Figure 1 This conceptual circuit can detect both phase sequences.

Also, to ensure detection of a reversed phase sequence, $C_1=C_3$, and $R_1=R_3$; that is, the components in the

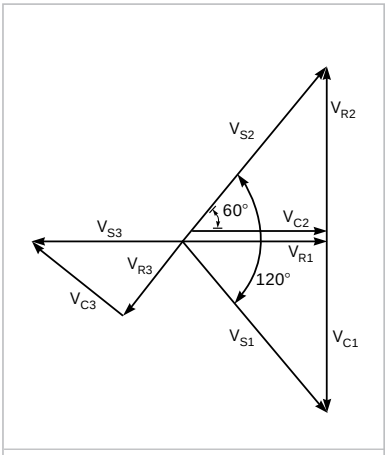

Figure 2 When the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$.

third branch are identical to those in the first branch. The phase-sequence-detection circuit in Figure 3 eliminates the requirement for an accessible ground wire by adding resistors R_4 and R_5 that connect in parallel with the first and third branches. Eliminating the ground-wire requirement also dictates a ratio between $|X_{C1}+R_1|$ and $|X_{C2}+R_2|$. For no current to flow to ground from Node G, the sum of currents in the branches must equal zero, and, if you disconnect Node G from ground, its potential with respect to ground is also zero.

As long as the proportions of X_{C1} to R_1, X_{C2} to R_2, and X_{C3} to R_3 remain as noted, the balance of voltage drops remains across R_1, C_2, and R_3. Multiplying the impedance of any branch by a constant influences only the magnitude of the currents through the respective branch. The current through any branch presents the same phase angle as the voltage across a resistor in the branch. The phasor diagram in Figure 4 shows the currents in Figure 3. From this diagram, if $|I_2|=\tan(60°)\times|I_1|$, then $I_1+I_2=-2\times I_3$. Thus, I_3 has half the magnitude of and an exactly opposite direction from (I_1+I_2).

A vector diagram of the currents shows that adding two currents, each with magnitudes equal to I_3 and the same phases as V_{S1} and V_{S3}, produces a summed current with the same magnitude and phase as I_3; therefore, the total current at Node G is zero: $I_1+I_2+I_3+I_1'+I_3'=I_1+I_2+2\times I_3=0$. To make the sum of the currents equal zero, $R_4=R_5=|R_1+X_{C1}|=|R_1-j[1/(2\pi\times f\times C_1)]|$. The two LEDs in Figure 3 indicate correct or reversed-phase sequence. When LED_2 lights and LED_1 remains dark, the voltage between nodes A and B is 0V, which corresponds to a correct phase sequence. A reversed-phase sequence lights LED_1 while LED_2 remains dark. The diodes connected in parallel with the LEDs protect against exceeding the LEDs' reverse-breakdown voltages, and resistors R_6 and R_7 limit forward currents through the LEDs. For greater sensitivity, you can replace the LEDs with high-input-impedance ac-detector circuits.

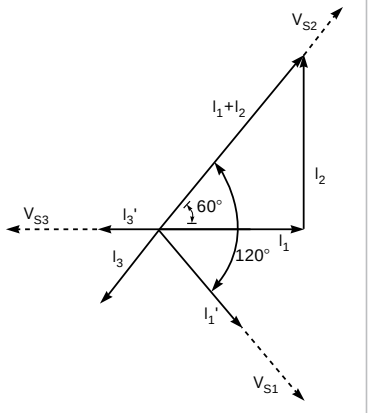

Figure 4 I_3 has half the magnitude and an exactly opposite direction to (I_1+I_2) in Figure 3.

The circuit's final version includes indicators that show whether all three phases carry voltage. In the circuit in Figure 3, a phase that carries 0V lights both LEDs. Depending on your application, you can connect voltage-detection circuits comprising LEDs and protection diodes in series with current-limiting resistors between V_{S1}, V_{S2}, and V_{S3} and Node G. You can also use low-wattage neon lamps with appropriate series-current-limiting resistors.

When selecting components, ensure that their values conform to the following proportions. For an arbitrarily chosen value for C_1, $R_1=R_2=R_3=1/(2\pi\times f\times C_1\times\tan(60°))$, $C_1=C_3$, $C_2=3C_1$, and $R_4=R_5=2\times R_1$. When you select a value for C_1, the currents through the detection circuitry should be significantly lower than the currents through the branches, which excludes arbitrarily low values for C_1.EDN

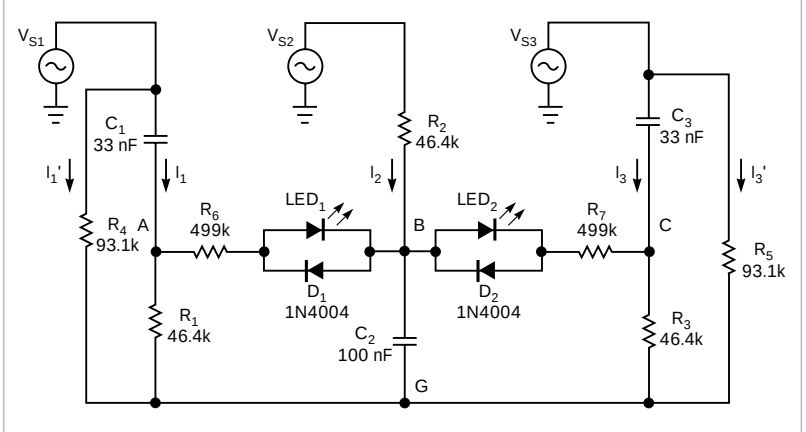

Figure 3 This phase-indicator circuit balances branch voltages and currents and requires no ground reference. These component values are for a 60-Hz line frequency.

Microcontroller's single I/O-port line drives a bar-graph display

R Jayapal, PhD, Bharat Heavy Electricals Ltd, Trichy, India

Instrument designs featuring a digital display may benefit from a secondary display that provides an analog version of the displayed parameter. A bar-graph display provides an easily interpreted graphical indicator that allows comparison with its full-scale value, but a conventional microcontroller-based design uses at least one eight-line I/O port to drive an eight-segment-bar-graph LED display.

As an alternative, some microcontrollers include a PWM (pulse-width-modulated) output. You can minimize the number of required I/O lines by using the PWM output to drive National Semiconductor's (www.national.com) LM3914 bar-graph-display-driver circuit or an equivalent. In operation, the microcontroller's program adjusts the PWM output's pulse width such that the average voltage that feeds to the LM3914 circuit illuminates the required number of bars in the display.

The design in Figure 1 obviates the shortcomings of these approaches and uses only one port line to drive an eight-segment bar graph. This design does not use a PWM output and hence can apply to any microcontroller. Referring to the timing diagram in Figure 2, whenever the bar-graph display requires an update, the microcontroller's software delivers a pulse train through its output port. The first pulse comprises a pulse of width T_1 that's longer than the width of the pulse T_2, which triggering monostable IC_1, a 74123 or equivalent, produces. You apply both pulses to IC_3, a 7400 or equivalent NAND gate, which together with IC_1 forms a long-pulse detector. Use the equation in IC_1's data sheet to select values for C_1 and R_1 that yield a value of approximately 1.5 msec for T_2's output pulse. Typical widths for T_1 and T_3 are 3 and 1 msec, respectively.

The output pulse from IC_3 goes low for a duration of T_1-T_2, and this pulse clears IC_2, an 8-bit serial-in parallel-out shift register, which forces all of IC_2's outputs to go low and lights all segments of the bar-graph array (LED_1 to LED_8).

To light N segments of the bar-graph array, the microcontroller immediately sends a serial train of (8−N) pulses of width T_3 through the output-port line. Because the width of these pulses is less than T_2, NAND gate IC_3's output always remains high and thus does not clear the shift register. The rising edge of each of the microcontroller's output pulses loads a high to one of IC_2's outputs.

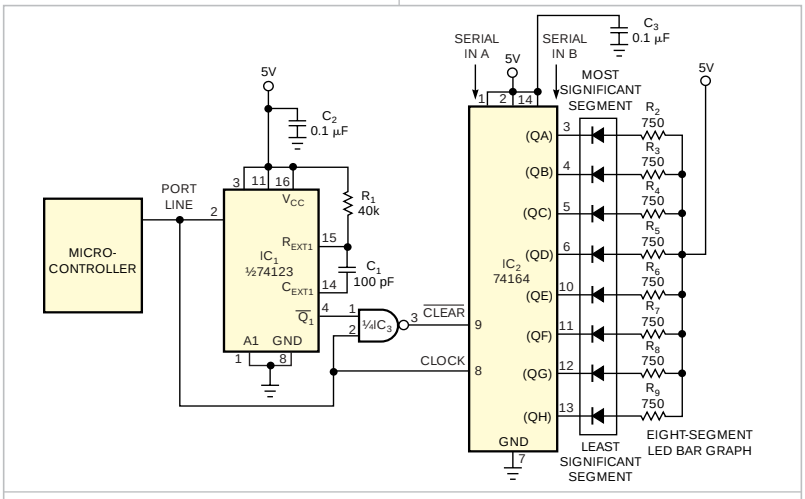

Figure 1 You can add a multisegment bar-graph display to a microcontroller that has only one output line.

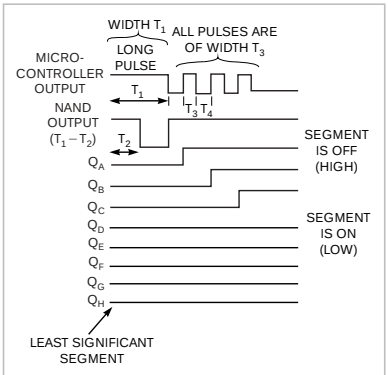

Figure 2 During the first pulse of the microcontroller's output-pulse sequence, the NAND gate's output clears the shift register and lights all of the display's segments.

Note that shift register IC_2's QA output connects to the bar graph's most significant segment. Hence, the first pulse switches off the most significant segment. Starting with the most significant segment, for (8−N) pulses, 8−N segments switch off, and N segments beginning with the least significant segment remain lighted. Using this reverse logic takes advantage of the shift register's outputs' ability to sink more current than they can source—8 versus 0.4 mA, respectively, and thus produce a brighter bar-graph display without adding output buffers. Figure 2 shows a sample timing diagram that lights five of eight display segments.

If a second output-port line is available, you can omit using monostable multivibrator IC_1 and NAND gate IC_3 and use the second port to clear the shift register by outputting a zero whenever the bar graph requires an update. To obtain finer resolution, you can add segments to the bar graph by cascading additional shift registers. To light N segments of a display that is M segments long, the first output port sends M−N pulses to the shift register's clock input.

This design lends itself well to situations in which unused I/O-port lines are at a premium, as is the case for microcontrollers with reduced pin counts, or if you need to retrofit a bar-graph display by adding a daughterboard to a design. EDN

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READERS SOLVE DESIGN PROBLEMS

Microprocessor generates programmable clock sequences

William Grill, Honeywell BRGA, Lenexa, KS

To produce trains of pulses suitable for keying transmitters, testing circuits, and debugging data links, designers requiring continuous or event-driven pulse sequences have traditionally relied on pulse generators or collections of simple circuits. Today's inexpensive microprocessors make it possible to design and build low-cost, dedicated pulse-sequence generators with a minimum of resources. In a small, SOT-23-packaged, 10F200 controller from Microchip (www.microchip.com), the design in Figure 1 uses a code-based embedded table algorithm to generate an application-settable period and table-based PWM (pulse-width-modulation) sequence. The application produces a continuously pulsed sequence and requires only three constants and a pulse-width profile table that it copies into the microprocessor's assembler-based code before compiling (Figure 2).

All code branches undergo equalization to produce a group of 29 constant instruction times. During software development, you can use coded constants and a table-based approach as a flexible method of modifying the pulse sequence. The three parameters that Figure 2 highlights include the number of PWM cycles that execute between tabled steps, which the algorithm passes as "temp_cntK." This parameter defines how many PWM periods of a range from one to 255 repeat within each tabled step. For three cycles per table step, you use #define temp_cntK .3. The next parameter is the number of 29-instruction loops that execute during each PWM period. All branches of the coded instructions equalize to constant 29-instruction periods. When you copy this parameter as "loopsK," it can range from one to 255. Using the 10F200's internal 4-MHz clock and an 8-bit counter to generate 1-µsec instruction periods, you can generate a PWM period range of 58 to 7395 µsec, which corresponds to a frequency range of 17,241 to 135 Hz. For a 1-msec PWM-cycle period and the sequence in Figure 2, you require 31 base loops per cycle, which you obtain by dividing 1 msec by the 29-µsec instruction period: #define loopsK .31.

You then equate the total number of table profile steps to "table_maxK." The total number of profile steps that a look-up table includes and that you copy into the code may vary from one to 252. In this application, five tabled steps correspond to pulse duty cycles of 25, 50, 87.5, 12.5, and 75%. These val-

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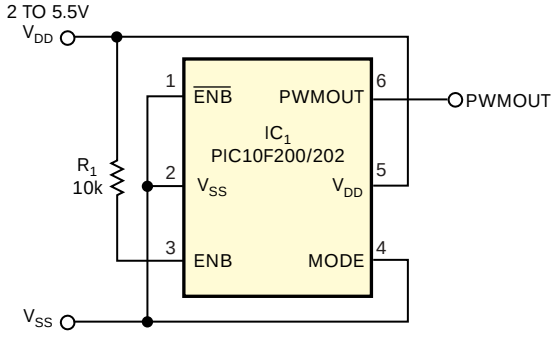

Figure 1 A microcontroller and a resistor can deliver a complex PWM output.

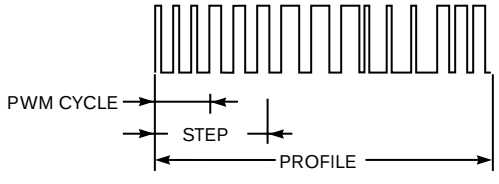

Figure 2 This waveform profile comprises five steps, each using one of three PWM cycles. In continuous mode, the circuit's output repeats indefinitely.

ues undergo scaling according to the following equation: Duty cycle=INT ($\%T_{DTY}$/100×loopsK+0.5), in which INT is the integer value and $\%T_{DTY}$ is the percentage of the total duty cycle. In this example, loopsK=31. The number of steps in the table passes to the program as #define loop_maxK .5.

The pulse-duty cycle can vary only in increments of a single 29-instruction base loop, and, as a consequence, the pulse duty cycle's resolution varies as the number of basic loops for the waveform's desired period, which you define as loopsK=31 loops. Thus, the duty-cycle resolution equals 1/(loopsK), or 1/(31)=3.22% for this application.

You can use a spreadsheet or manually calculate the translated and scaled duty-cycle values and store them in the data-profile table. For example, you calculate the value for a 25% duty cycle as INT(25/resolution+0.5)=INT(25/3.22+0.5), where INT represents extraction of the integer value of the computed quantity. For required duty cycles of 25, 50, 87.5, 12.5, and 75%, the values that pass to the data-profile table are retlw_8, 16, 27, 4, and 23, respectively. The assembly-language program available for downloading from the online version of this Design Idea at www.edn.com/060720di1 includes these duty-cycle values and the three other parameters.

The program includes two additional features: Connecting Pin 1 to ground enables a continuous-output mode. Connecting Pin 1 to $+V_{DD}$ evokes a single output waveform. Pin 3 serves as a high true-output enable when you connect it to $+V_{DD}$ or as a positive-edge trigger input when you pull the pin to ground and release it. Note that the program currently includes no contact-debounce routines for either input.

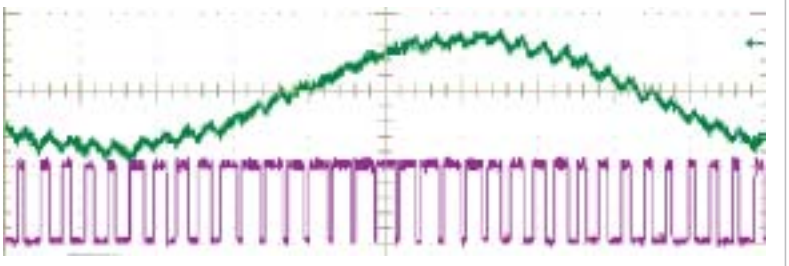

Figure 3 After undergoing lowpass-filtering, the controller's pulse-width-modulated output (lower trace) reveals its sine-wave origin.

In the example in Figure 3, the controller delivers a pulse-width-modulated output (lower trace), which, after processing by a single-pole lowpass filter, corresponds to a sine wave (upper trace). Using another version of the circuit, you can evaluate how a critical midword error affects a serial link's characteristics, system timing, and response latency.

The waveform in Figure 4 comprises 100 pulses, 99 of which exhibit a nominal duty cycle that varies from 48 to 51%, and a single error pulse with a 75% duty cycle. The waveform-table entries use values of loopsK=100, temp_cntK=1, and table_maxK=100 to produce a pulse sequence comprising 74 pulses with nominal duty cycles, a single pulse with a 75% duty cycle, and a final sequence of 25 clocks with nominal duty cycles. The entire sequence repeats at a 345-Hz rate.

Using a 4-MHz-clock-rate version of Microchip's 10F220 controller constrains the basic software-timing loop to a 29-μsec period. You can compile the program into an 8-MHz 10F220 to reduce the timing loop to 14.5 μsec and extend the output's usable bandwidth. You can modify the code in the listing to suit other compatible microprocessors to obtain greater bandwidth and integrate additional functions. As is, the circuit requires only 155 bytes of internal EEPROM and occupies an SOT-23 pc-board footprint—not bad for a processor that costs less than $1. EDN

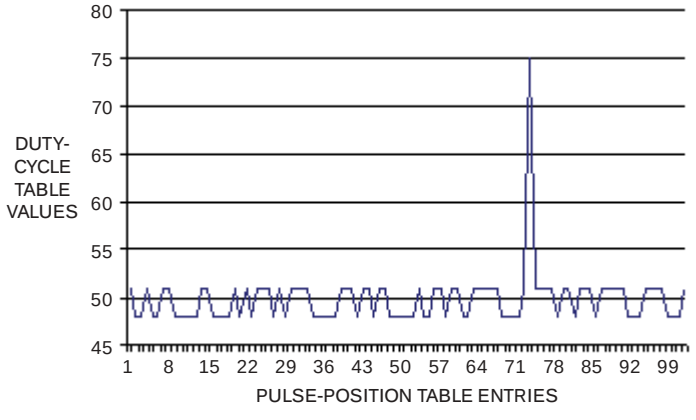

Figure 4 Devised for testing a serial link's error response, this waveform plot displays pulses' locations within the waveform (horizontal axis) versus the duty cycle for each pulse (vertical axis). The waveform cycle repeats after pulse 100 ends.

Ceramic output capacitors enhance internally compensated switchers

Robert Kollman, Texas Instruments, Dallas, TX

Integrating compensation components with a power-supply controller and buck regulator's power switches can minimize pc-board area, improve reliability, and eliminate assembly errors by reducing the number of components and solder joints. However, integration also limits a designer's range of choices in the selection of output-filter components. Figure 1a presents a typical switching regulator based on Texas Instruments' (www.ti.com) TPS5430. The boxed area in Figure 1b shows a simplified version of the IC's internal small-signal-equivalent circuit, which includes an error amplifier, E_1; passive-compensation components; and a voltage-controlled voltage-source, E_2, which represents the modulator and the power switches. Support components external to the IC include output-filter components and their parasitic resistances, a resistor representing an external load, and a divider comprising R_1 and R_2 that sets the output voltage. The compensation-circuit design accommodates a certain range of output-filter inductance and capacitance and their associated parasitics.

Figure 2 shows Bode diagrams for the error-amplifier and modulator-gain blocks (2a) and the entire regulator system (2b). Envisioning that end users would specify aluminum electrolytic capacitors for the output-filter circuit, the IC's designer includes a Type 3 compensation circuit to optimize the IC's performance for aluminum capacitors' characteristics. Note that a Type 3 compensation circuit includes a pole at the origin of the circuit's pole-zero plot to provide high gain at dc and an integratorlike high-frequency roll-off augmented with pairs of poles and zeros to provide phase and gain margins at certain frequencies (Reference 1).

The regulator's LC-output modulator/filter's amplitude-response curve peaks at the resonant frequency set by the filter's inductor and output capacitor, and then it decreases at a −40-dB/decade rate until it reaches a zero at a frequency set by the output capacitor and its ESR (equivalent series resistance). Beyond that frequency, the output inductor's and the capacitor's ESRs determine the attenuation curve's slope, resulting in a −20-dB/decade rate.

For good regulation, the error amplifier provides a high dc gain at low frequencies. However, to ensure stability, the loop gain must decrease as frequency increases. The goal is to approximate a −20-dB/decade roll-off at all frequencies. Placing two zeros at the output filter's resonant frequency helps cancel the two poles representing the resonance. Adding a pole to the error-amplifier response cancels the zero that the output capacitor and its ESR introduce. Adding a final pole above the power supply's crossover frequency helps further increase the regulator loop's stability. Figure 2b shows the sum of the gains of the error amplifier and modulator/filter gain. The power supply's characteristics show a 30-kHz bandwidth and a 60° phase margin that ensures stable operation.

The power-supply-control-

(continued on pg 90)

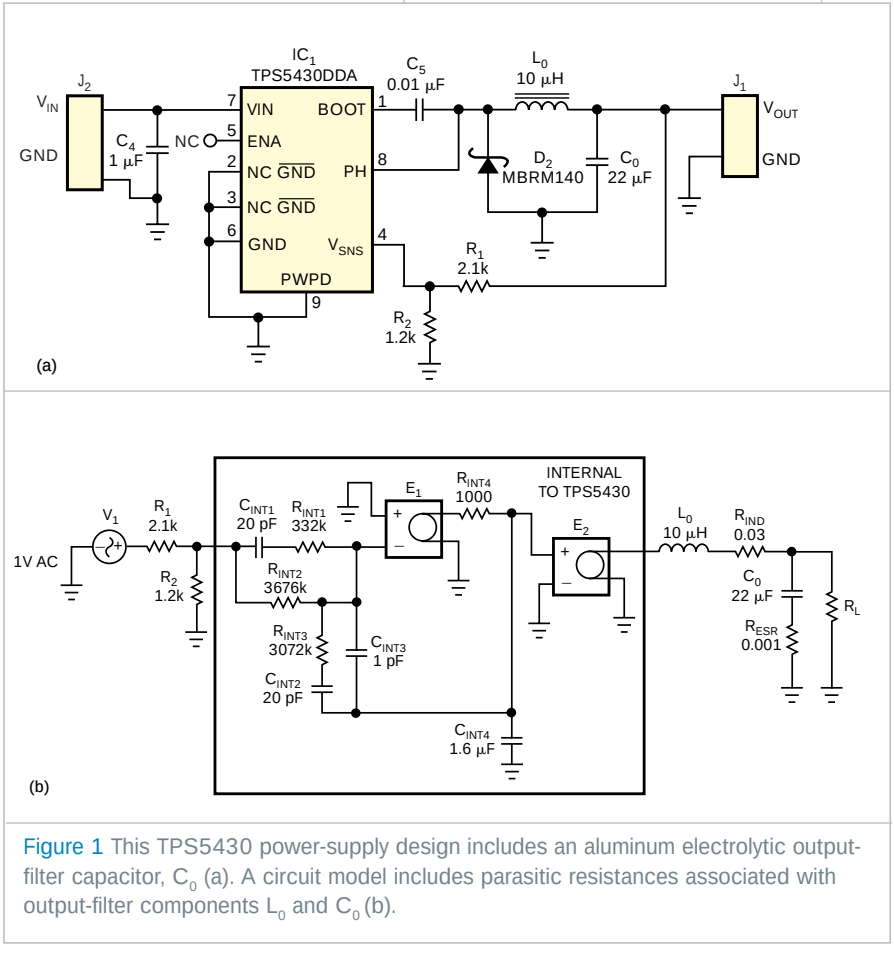

Figure 1 This TPS5430 power-supply design includes an aluminum electrolytic output-filter capacitor, C_0 (a). A circuit model includes parasitic resistances associated with output-filter components L_0 and C_0 (b).

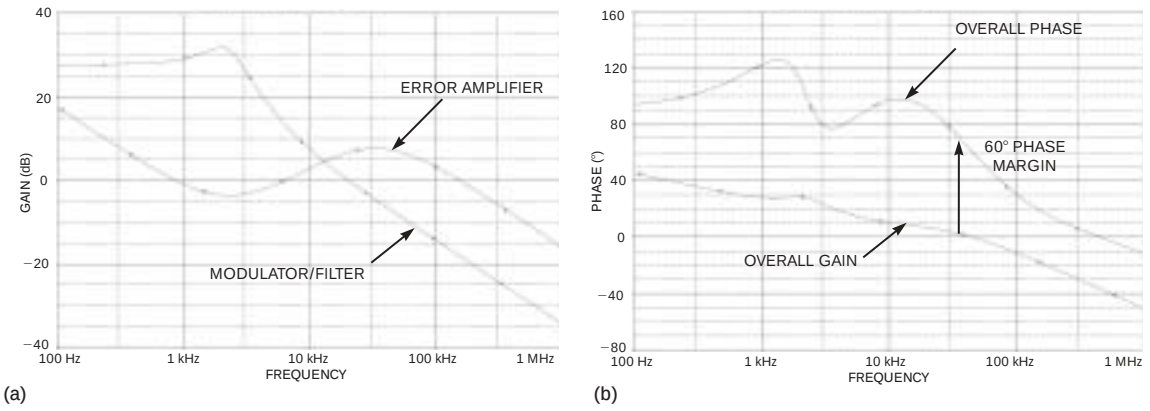

Figure 2 Gain (a) and phase (b) plots show that the circuit of Figure 1a includes adequate compensation and phase-angle margin for an aluminum electrolytic output-filter capacitor.

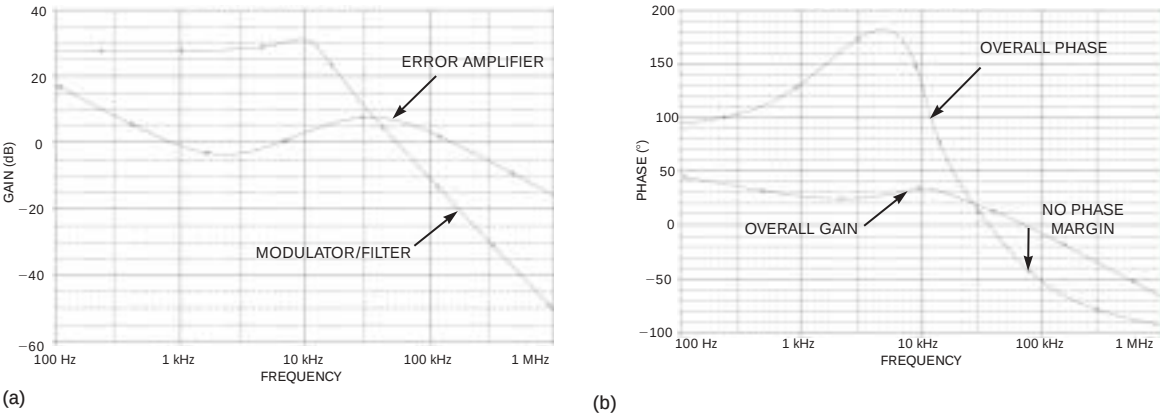

Figure 3 Gain (a) and phase (b) plots show that using a ceramic-dielectric output-filter capacitor erodes the phase-angle margin and pushes the circuit dangerously close to oscillation.

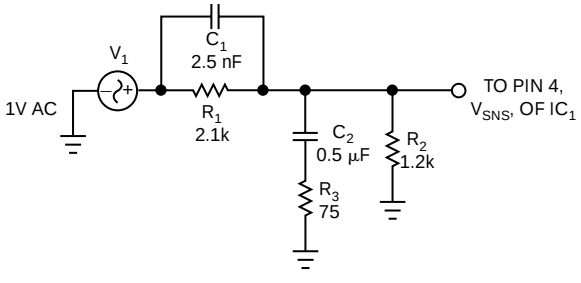

Figure 4 A few passive components supplement R_1 and R_2 and stabilize the circuit for use with a ceramic-dielectric output-filter capacitor.

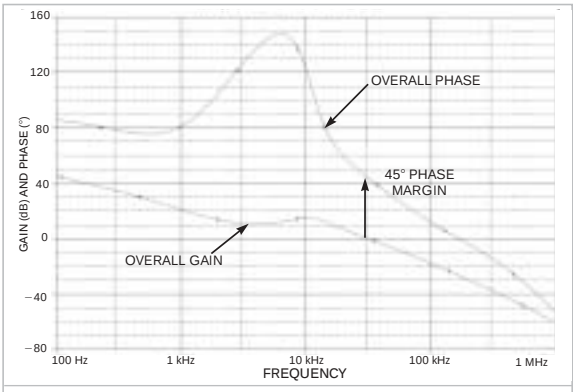

Figure 5 The phase-angle plot for the circuit of Figure 4 shows a sufficient phase-angle margin to allow stable operation with a ceramic output-filter capacitor.

loop response (Figure 3) illustrates the circuit's behavior when the design includes ceramic-dielectric output-filter capacitors and the same integrated-compensation components in Figure 1. Ceramic capacitors present a much lower ESR than do aluminum electrolytic capacitors, and their capacitance determines the filter's attenuation rather than their ESR. Consequently, at high frequencies, the LC filter's characteristics include a double pole and a steeper, −40-dB/decade slope. In addition, filter attenuation increases at the desired crossover frequency, degrading phase and gain margins. Figure 3b indicates that the power supply is unstable and, with no phase margin, will likely oscillate.

Replacing the divider network, R_1 and R_2 in Figure 1 with the passive network in Figure 4 stabilizes the regulation loop and allows an internally compensated controller to use ceramic output capacitors. The network's components add two sets of poles and zeros to the compensation network to cancel the consequences of using ceramic output capacitors. For example, C_2 and R_3 provide attenuation that reduces the crossover frequency. You select C_2 to provide attenuation at frequencies much lower than the crossover frequency. Unfortunately, C_2 adds a negative-phase shift that R_3 returns to nearly zero at the design's crossover frequency. Adding C_1 introduces a phase lead that compensates for the ceramic capacitors' negative effects. Without C_1, the filter's 180° phase shift would reduce the regulator's phase margin to nearly zero.

The phase angle starts increasing at a frequency that C_1 and R_1 determine, and they introduce a zero in the phase-plane plot at that frequency (Figure 5). At a frequency that C_1 and R_3 determine, a pole in the phase-plane plot terminates the phase angle's increase. The geometric mean of the pole and zero frequencies determines the maximum phase-angle boost.

As a starting point, you can place the first pole, which C_2 and the parallel combination of R_1 and R_2 determine, at a low frequency, such as 100 Hz. Next, adjust the values of C_2 and R_3 to set the first zero's frequency at 1 kHz, which is much less than the gain curve's 0-dB crossover frequency. Finally, set the zero that C_1 and R_1 introduce to a frequency that's at least a factor of two below the zero-gain crossover frequency to ensure a 45° phase margin at the crossover frequency. The Bode plot in Figure 5 features a 30-kHz regulation-loop bandwidth that provides good transient response and more than 45° of phase margin to ensure good stability. EDN

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Tapped inductor, boost regulator deliver high voltage

David Ng and Adam Huff, Linear Technology Corp, Milpitas, CA

When you face the task of generating a regulated voltage that's higher than the available power-supply voltage, you may consider a boost regulator. Although a boost converter can in theory generate almost any voltage that's higher than its input, practical considerations limit the output to approximately eight times its applied voltage. To generate an even higher voltage, consider using a tapped-inductor boost topology. Figure 1 shows an implementation of a converter that boosts a 3V input to 100V dc. The connections to the regulator chip are similar to those of a traditional boost converter, but, to achieve the high boost ratio, this design uses L_1, a 1-to-6-turns-ratio, tapped inductor.

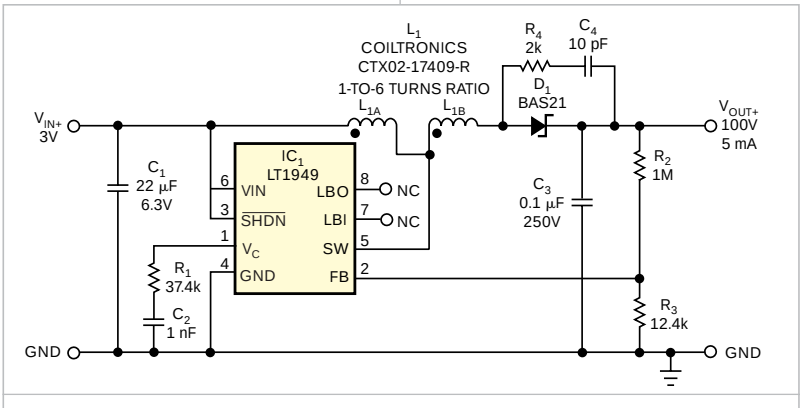

Figure 1 Using a tapped inductor extends a boost-topology switching regulator's practical output-voltage range.

The waveforms in Figure 2 show the input voltage, the voltage at power-switch IC_1's output, Pin 5, and rectifier diode D_1's anode voltage. As in any boost circuit, inductor L_1's core stores energy when IC_1's internal output switch conducts. When the switch turns off, the voltage across its terminals and L_{1A} goes higher than the input voltage. Due to inductive coupling and the larger number of turns that make up L_{1B}, the voltage at rectifier diode D_1's anode and hence the output voltage goes much higher. Resistors R_2 and R_3 form a feedback-voltage divider that closes the regulation loop. The R_4-C_4 network forms a snubber circuit that suppresses the impact of diode D_1's small parasitic capacitance. Without the network,

Figure 2 For a 3V-dc input (lower trace, horizontal line), the voltage at regulator IC_1's SW pin reaches a peak of approximately 18V (lower trace, pulsed waveform). The 1-to-6 step-up turns ratio of inductor L_1 further increases the peak output voltage to 160V (upper trace) to produce 100V dc. The upper trace's lower limit goes to $-6\times V_{IN}(-18V)$ due to the tapped inductor.

power switch IC_1 "sees" a capacitance that's 36 times larger due to the multiplicative effect of the tapped inductor's turns ratio.

Measuring only 5.6×6×3.4 mm, Coiltronics' (www.coiltronics.com) CTX02-17409 tapped inductor, L_1, and Linear Technology's (www.linear.com) LT1949 monolithic regulator, IC_1, available in an eight-lead MSOP package, present small pc-board footprints. When you implement the circuit on a single-layer pc board, the entire circuit occupies less than 1.9 cm^2 of board space (Figure 3). For best results, review the board-layout suggestions in the device's data sheet (Reference 1) and use multilayer-ceramic capacitors for C_1 and C_3.EDN

Figure 3 The entire boost-converter circuit occupies a footprint of less than 1.5×1.25 cm on a single-sided pc board.

REFERENCE

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EDITED BY BRAD THOMPSON
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Low-dropout regulator, SMPS cascade suppress ripple, maintain efficiency

Scot Lester, Texas Instruments, Dallas, TX

A step-down SMPS (switched-mode power supply) efficiently converts unregulated power to a regulated output voltage. However, unwanted switching-induced ripple and input transients may appear on the output. Applying noisy power to an RF power amplifier can inject spurious signals or modulated noise into the broadcast spectrum. Analog- and RF-system engineers favor traditional low-noise power-supply designs that comprise a transformer, rectifier, and filter followed by a linear voltage regulator. A low-dropout linear regulator's low output noise and high PSRR (power-supply rejection ratio) ensure clean power that imposes no interference on a power amplifier's output.

Unfortunately, a transformer-and-rectifier power supply delivers a fluctuating output voltage that depends on its input voltage. As the difference between its input and output voltage increases, a low-dropout regulator's efficiency decreases, and its power dissipation increases. To remain in regulation at low ac-line voltages, even a low-dropout regulator requires a certain amount of head-room input-to-output voltage.

To overcome the disadvantages inherent in both circuits, you can use an SMPS to maintain high efficiency and a low-dropout regulator to reduce the output noise and ripple voltage of the SMPS. Setting the output voltage of the SMPS slightly higher than the low-dropout regulator's minimum dropout voltage reduces the regulator's power dissipation, accommodates the voltage margin you need for good switching-noise rejection, and maintains high efficiency. The regulators' PSRRs add, and the combined circuits' PSRR exceeds that of either the regulator or the SMPS alone.

Figure 1 shows a cascade circuit comprising an SMPS followed by a linear regulator. This circuit's output voltage ranges from 1.5 to 5V at an output cur-

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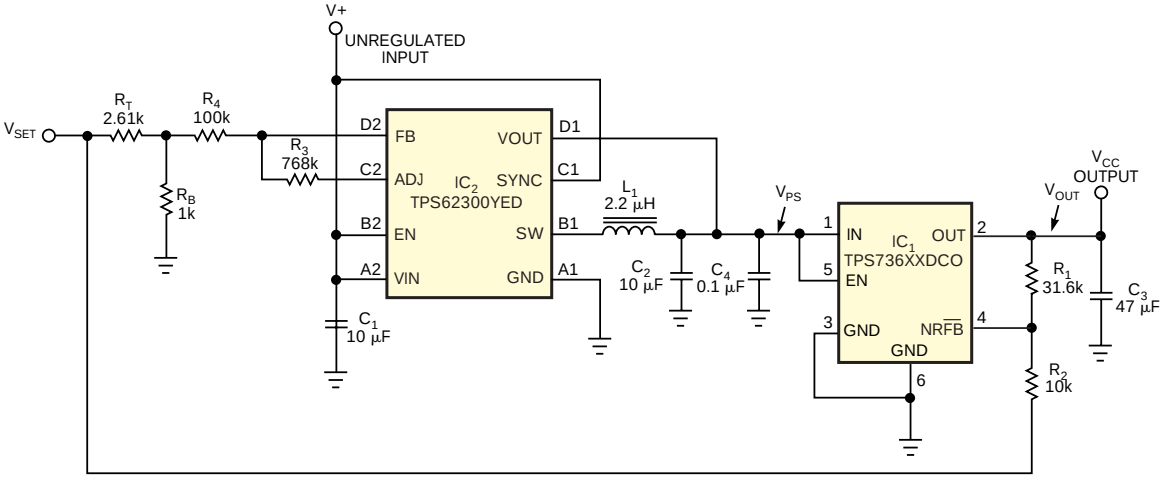

Figure 1 Connected in cascade, a low-dropout linear regulator and a switched-mode power supply improve output-voltage ripple and maintain overall efficiency. (Note: In IC_1's part designation, "XX" represents the regulator's output voltage.)

rent as high as 400 mA. Although a fixed 6V supply powers the cascaded circuit, its design accommodates any input voltage at least 0.5V higher than the cascaded pair's desired output voltage.

Adjusting the reference voltage, V_{SET}, over 0 to 1.105V linearly varies the circuit's output voltage. Resistors R_1 and R_2 and reference voltage V_{SET} determine the low-dropout regulator's output voltage and thus the cascaded pair's output voltage. Resistors R_T, R_B, R_3, and R_4 divide V_{SET} to maintain the SMPS' output voltage, V_{PS}, at a constant 0.2V higher than the regulator's output voltage, reducing the regulator's power dissipation to 80 mW at full output current and any output voltage.

At its maximum output current of 400 mA, the cascaded supply reaches a maximum efficiency of 89% with a 6V input and a 4.69V output (Figure 2). The overall efficiency decreases as the output voltage decreases. Figure 3 compares the PSRRs of the SMPS alone and of the SMPS cascaded with the regulator, which improves PSRR by 46 dB at 500 Hz—essentially that of the regulator alone at 500 Hz.

Over a frequency range of 100 Hz to 100 kHz, the low-dropout regulator improves PSRR by at least 25 dB (Figure 3). Circuit-layout and -measurement techniques compound the difficulty of making accurate small-signal measurements, and the graph's PSRR values may not appear additive. The linear regulator governs the circuit's switched-load transient response, which may represent an improvement over the response of the SMPS. However, the cascade circuit's low output ripple and high efficiency make the circuit well worth investigation. EDN

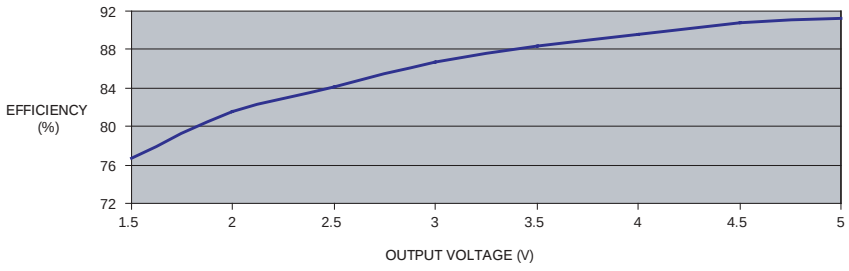

Figure 2 The regulator cascade's combined efficiency improves as the unregulated output voltage increases.

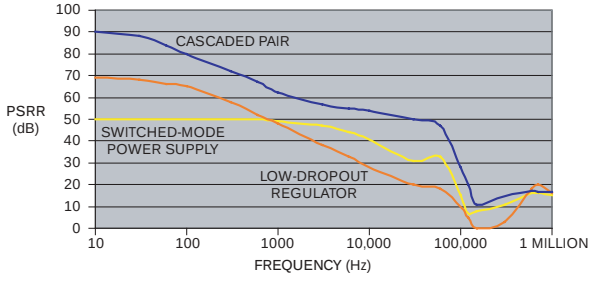

Figure 3 The power-supply rejection ratio improves significantly (blue trace) when you cascade switched-mode (yellow trace) and linear (red trace) voltage regulators.

Novel circuit isolates temperature sensor from its host

Alfredo H Saab and Tamer Mogannam,
Maxim Integrated Products Inc, Sunnyvale, CA

Temperature sensors must sometimes operate at locations whose return potentials differ considerably from that of the data-acquisition system's common—that is, equipotential—ground. In consequence, the temperature sensor's support circuitry must provide galvanic isolation between the sensor and its data-acquisition system. Also, the data-acquisition system seldom provides an isolated source of power for the sensor. The circuit in Figure 1 solves both problems by isolating the sensor's signal and power supply.

The complementary, fixed-frequency square-wave outputs of a power-transformer driver—IC_1, a Maxim (www.maxim-ic.com) MAX845—drive a Halo Electronics (www.haloelectronics.com) TGM-010P3 1-to-1-to-1 transformer with dual primary windings and a single untapped secondary winding (Reference 1). The secondary winding feeds a Graetz-bridge rectifier that generates approximately 4.5V to power IC_2, a Maxim MAX6576 sensor. Combining a temperature sensor, signal-processing electronics, and an easy-to-use digital-I/O interface in a low-cost package, the MAX6576 draws little current from a single supply source and maintains its specified accuracy over a 3 to 5V supply-voltage range.

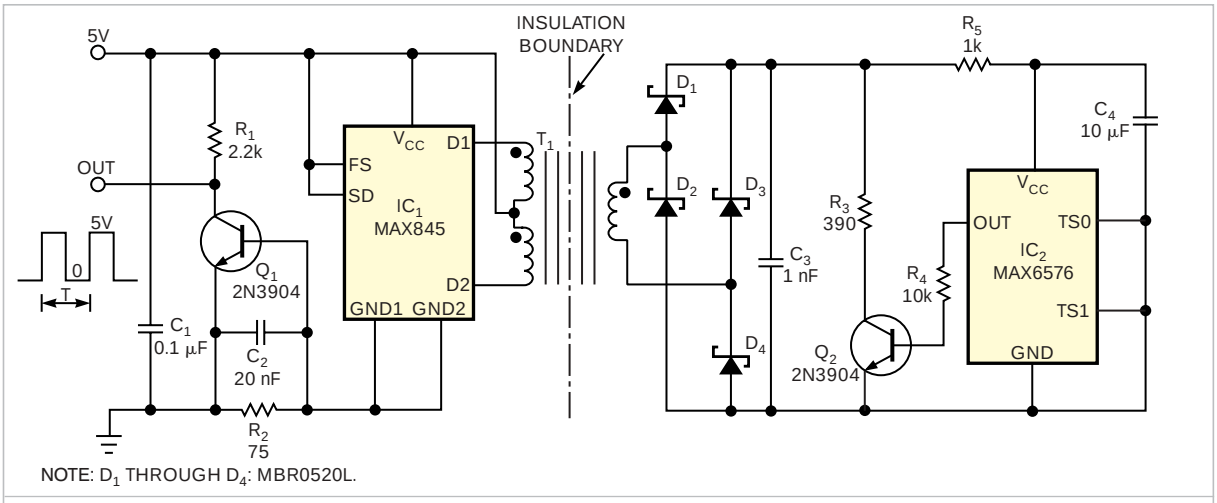

Figure 1 Transformer T_1 isolates the temperature sensor, IC_2, from the equipment under test. The period of IC_1's digital output varies as a function of temperature. The circuit's output period varies at a rate of 10 µsec/°K. User-selected scale factors range from 10 to 640 µsec/°K.

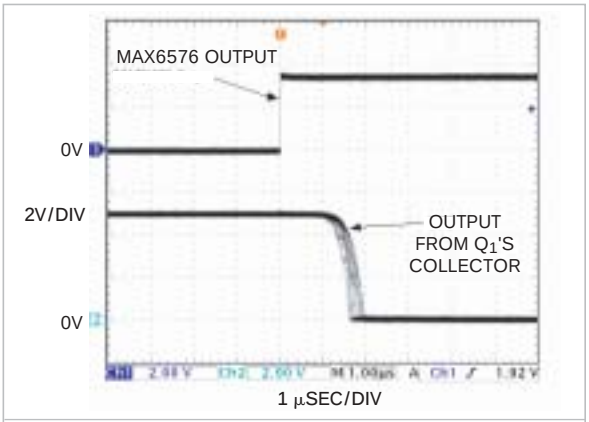

Figure 2 Measured from the positive-going edge of IC_2's output to the circuit's output at Q_1's collector, the relative jitter averages less than 1 µsec.

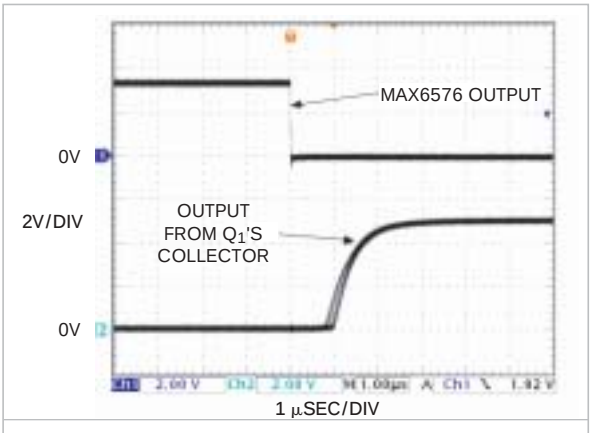

Figure 3 As in Figure 2, Q_1's average output jitter with respect to IC_1's negative-going output also averages less than 1 µsec.

If you connect the sensor as Figure 1 shows, it operates as an absolute temperature-to-period converter and provides a nominal conversion constant of 10 µsec/°K, which, at room temperature, yields a period of approximately 2.980 msec—a frequency of 335 Hz. You can adjust the conversion constant from 10 to 640 µsec/°K. Note that longer conversion constants allow more signal-integration time to minimize noise effects. The sensor's symmetrical square-wave output drives NPN transistor Q_2's base through R_4, a 10-kΩ resistor. A 390Ω resistor, R_3, serves as Q_2's collector load and connects to the same lines that deliver power to the temperature sensor. When Q_2 conducts, it draws an asymmetrical power-supply current that exceeds the supply current during the sensor output's positive half-cycle.

In IC_1's sensor output-to-ground return on the data-acquisition system's side, resistor R_2 and capacitor C_2 shunt Q_1's base-emitter junction. The values of R_2 and C_2 ensure that the sum of IC_2's current and transformer T_1's magnetizing current cannot drive Q_1 into conduction. When Q_2 conducts, it draws about 12 mA from the isolated 4.5V power-supply line. Reflecting to the primary, Q_2's conduction current flows from the 5V supply into IC_1, out through its ground terminals, and partly through R_2. The voltage drop across R_2 exceeds Q_1's base-emitter voltage threshold and supplies sufficient base current to turn on Q_1.

Thus, when Q_2 conducts, so does Q_1, which copies IC_1's isolated square-wave output to Q_1's collector circuit. As the waveforms of figures 2 and 3 show, Q_1's output rise and fall times, jitter, and propagation delay total about 2 µsec. The equivalent measurement error due to timing jitter amounts to less than 0.1°K at the fastest conversion constant of 10 µsec/°K. Varying the circuit's supply voltage through a range of 4.5 to 5.5V introduces an error of less than 0.1°K. The output at Q_1's collector can sink several milliamperes at a voltage excursion of 0 to 5V.

This design can accommodate temperature-to-frequency converters and other types of temperature sensors. For further information on IC_1 and IC_2, review the devices' data sheets and the data sheet for the MAX845 evaluation kit (references 2, 3, and 4). EDN

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Find resistor values for arbitrary programmable-amplifier gains

Sid Levingston, DML Engineering Inc, Aloha, OR

When available fixed-gain values match design requirements, a PGA (programmable-gain-amplifier) IC offers a drop-in choice, but what does a designer do when a suitable PGA is unavailable? Before the PGA's advent, a circuit designer who needed selectable, fixed amounts of gain chose a suitable operational amplifier and designed a switched-resistor gain-setting network. This Design Idea discusses two methods of designing the desired resistive network.

Figure 1 shows a series-ladder-resistor network comprising a string of resistors whose junctions connect to switch-selectable taps that determine the circuit's gain. Little current flows through the switch, and the resistance of the switch thus doesn't affect the design. A circuit with N discrete-gain values requires an N-position switch, usually an analog multiplexer, and N+1 resistors in its ladder. Equation 1 describes the circuit's gain in the general case:

$$GAIN[n] = \frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} + 1. \quad (1)$$

You can solve Equation 1 for the resistor summations and expand a few terms as follows:

$$\frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} = GAIN[n]-1. \quad (2)$$

$$\sum_{i=1}^{n} R_i = (GAIN[n]-1) \times \sum_{i=n+1}^{N+1} R_i. \quad (3)$$

$$R_1 = (GAIN[1]-1) \times (R_2 + R_3 + ... + R_{N+1}), \quad (4)$$

$$R_1 + R_2 = (GAIN[2]-1) \times (R_3 + ... + R_{N+1}), \quad (5)$$

and

$$R_1 + R_2 + R_3 + ... + R_N = (GAIN[N]-1) \times (R_{N+1}). \quad (6)$$

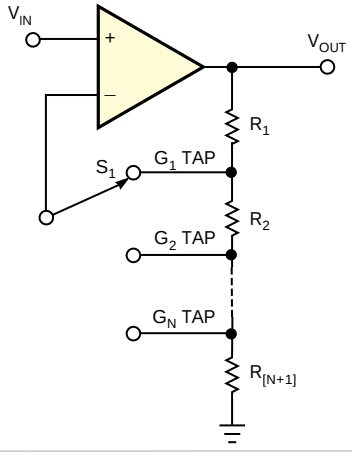

Figure 1 A series-resistor-ladder network and a single-pole, multiple-throw switch form a custom-value programmable-gain amplifier.

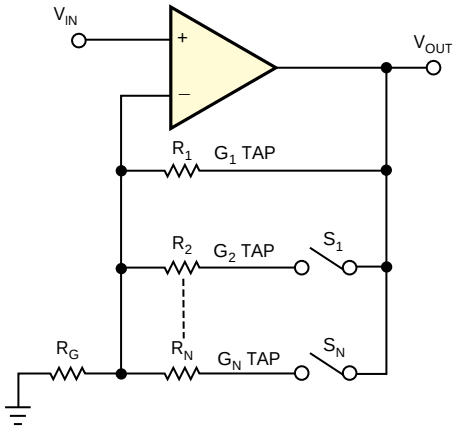

Figure 2 In a parallel-resistor-ladder network, connecting one resistor at a time in parallel with R_1 determines the circuit's gain.

Next, normalize R_1 to 1Ω and solve the equations for R_1:

$$1 = (GAIN[1]-1) \times (R_2 + R_3 + ... + R_{N+1}), \quad (7)$$

$$1 = -R_2 + (GAIN[2]-1) \times (R_3 + ... + R_{N+1}), \quad (8)$$

and

$$1 = -R_2 - R_3 - ... - R_N + (GAIN[N]-1) \times (... + R_{N+1}). \quad (9)$$

$$\begin{bmatrix} GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 \\ -1 & GAIN[2]-1 & GAIN[2]-1 & GAIN[2]-1 \\ ... & ... & ... & ... \\ -1 & -1 & -1 & GAIN[N]-1 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ ... \\ R_{N+1} \end{bmatrix} = 1. \quad (10)$$

A network that synthesizes N gain values results in an N×N matrix whose upper echelon equals the desired gains minus one, in ascending order, and its lower echelon equals negative one. To produce the resistor values for the desired gains, invert the matrix and calculate its dot product with a unity matrix. For example, a circuit requiring four gain values of three, five, 24, and 50 also requires five resistors. Stuffing and solving the matrix yields:

$$\begin{bmatrix} 2 & 2 & 2 & 2 \\ -1 & 4 & 4 & 4 \\ -1 & -1 & 23 & 23 \\ -1 & -1 & -1 & 49 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = 1. \quad (11)$$

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 0.2000 \\ 0.2375 \\ 0.0325 \\ 0.0300 \end{bmatrix}. \quad (12)$$

Scale the resistors' values to 1 kΩ and select the closest available standard resistor values to produce gains of:

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 200 \\ 237 \\ 32.4 \\ 30.1 \end{bmatrix}. \quad R_1 = 1\,k\Omega. \quad GAINS = \begin{bmatrix} 3.002 \\ 5.007 \\ 23.99 \\ 49.82 \end{bmatrix}. \quad (13)$$

Figure 2 shows a parallel-resistor-ladder network. To select a gain value, connect an additional resistor in parallel with the other resistors. A circuit with N discrete gains requires N resistors in the ladder; an additional gain resistor, R_G; and N−1 switches. Equation 14 describes the circuit's gain in the general case:

$$GAIN[n] = \frac{R_1 \| R_2 \| ... \| R_N}{R_G} + 1, \quad (14)$$

and Equation 15 describes the parallel-resistor combination for each gain:

$$R_P[n] = (GAIN[n]-1) \times R_G. \quad (15)$$

The nth value of R_p equals the nth−1 value of R_p in parallel with the ladder's nth resistor. Solve the following equations for the nth resistor value:

$$R_P[n] = R_P[n-1] \| R_n, \quad (16)$$

$$R_1 = (GAIN[1]-1) \times R_G, \quad (17)$$

and

$$R_n = \frac{R_P[n] \times R_P[n-1]}{R_P[n-1] - R_P[n]}. \quad (18)$$

To find the desired network's resistors, select the desired gain values and R_G and then use Equation 14 to calculate the parallel values. Use the resulting values to solve Equation 15 and find the required resistor values. As in the previous example, a circuit must produce gain values of three, five, 24, and 50. Four gain values require four resistors. Let $R_G = 1\Omega$. Solving Equation 14 for the parallel-values matrix yields:

$$\begin{bmatrix} R_P[1] \\ R_P[2] \\ R_P[3] \\ R_P[4] \end{bmatrix} = \begin{bmatrix} 49 \\ 23 \\ 4 \\ 2 \end{bmatrix}. \quad (19)$$

Substituting these values into Equation 15 yields the resistors' values:

$$R_1 = 49 \times 1 = 49\Omega, \quad (20)$$

$$R_2 = \frac{23 \times 49}{49-23} = 43.35\Omega, \quad (21)$$

$$R_3 = \frac{4 \times 23}{23-4} = 4.842\Omega, \quad (22)$$

and

$$R_4 = \frac{2 \times 4}{4-2} = 4\Omega. \quad (23)$$

Scaling to 1 kΩ and selecting the closest available standard-value resistors yields gains of:

$$\begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix} = \begin{bmatrix} 48{,}700 \\ 43{,}200 \\ 4870 \\ 4002 \end{bmatrix}. \quad R_G = 1\,k\Omega. \quad GAINS = \begin{bmatrix} 49.7 \\ 23.9 \\ 5.02 \\ 3 \end{bmatrix}. \quad (24)$$

Reference 1 provides a review of the matrix math. EDN

REFERENCE

1 Freeman, Larry, "Review of Matrices," Math Refresher, Dec 19, 2005, http://mathrefresher.blogspot.com/2005/12/review-of-matrices.html.

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READERS SOLVE DESIGN PROBLEMS

Ultralow-cost, two-digit counter features few components

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University of Sciences and Technology, Oran, Algeria

The ultralow-cost, two-digit-counter circuit in Figure 1 represents an attempt to reduce the number of components using a mostly software approach and a low-cost microcontroller, the PIC16F84A. The circuit lacks the current-limiting resistors that normally connect to a seven-segment LED display's pins because a software routine lights only one of the display's segments at a time, first in the 10s display and then in the units display. Doing so keeps the circuit's maximum current consumption at a nearly constant level, even if you add a third LED display to implement a three-digit counter. The circuit also lacks digit-selection switching transistors that classic multiplexed circuits' switching transistors typically use, and the circuit includes one common-cathode and one common-anode display. The reason for this approach is that each of the microprocessor's I/O Port A and Port B lines can assume one of three states: high, low, and floating—that is, high impedance. Programming a line as an input places it in a high-impedance state, which turns the display off.

In addition, the program drives only one segment at a time and executes the following sequence: To drive the 10s display, program the line RB0 output and drive it high to light the corresponding segment of the common-cathode display and then program RB0 as an input. Repeat this procedure for lines RB1 through RB6. To drive the units display, repeat the process while applying a low output from RB0 to drive the common-anode display. Figure 2 shows the circuit's timing diagram. The prototype display uses Kingbright's (www.kingbright.com) SC52-11EWA (DS_1) and SA52-11EWA (DS_2) high-efficiency, seven-segment displays that emit 2000 to 5600 µcd at a forward current of 10 mA. At a forward current of approximately 5 mA, the displays remain readable.

Early motion pictures displayed at an 18-Hz rate, which produces marginal flicker. The software executes at a rate of 180 Hz, or 10 times the minimum flicker rate. Each of the display's seven segments must illuminate for an interval of 1/(180×7) sec, or approximately 0.8 msec. To simplify the timing routine (section Delay3 of Listing 1, available at www.edn.com/060817di1), the software uses a refresh interval of 1 msec.

Although this approach provides adequate segment-drive current, the display's internal LEDs carry a 3V maximum reverse-voltage rating. Driving any I/O line high applies forward bias to one segment of the common-cathode digit but applies reverse bias to the

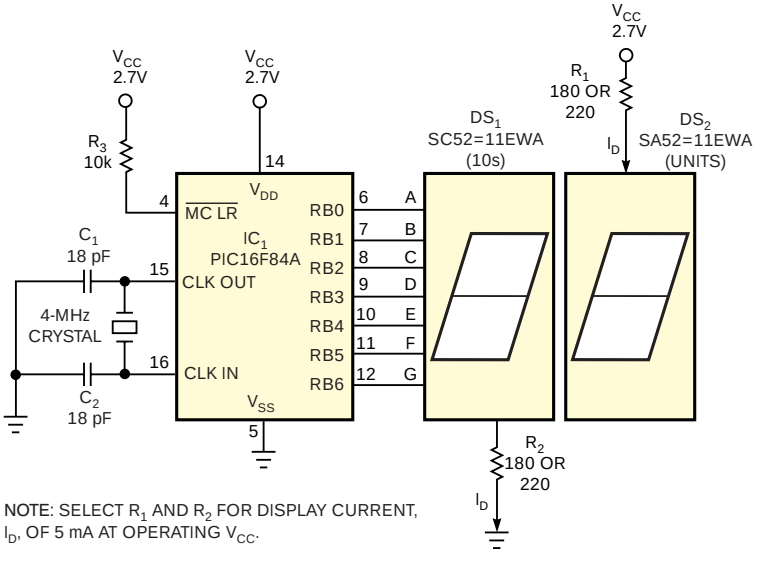

Figure 1 This low-cost, two-digit counter uses few components.

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corresponding segment of the common-anode display. The 16F84A requires a minimum of 2V for operation, and thus the circuit must operate in a 2 to 3V power-supply range. The assembler source code in Listing 1 counts from 0 to 99 sec and serves as an unoptimized proof-of-concept software test bed for the display.EDN

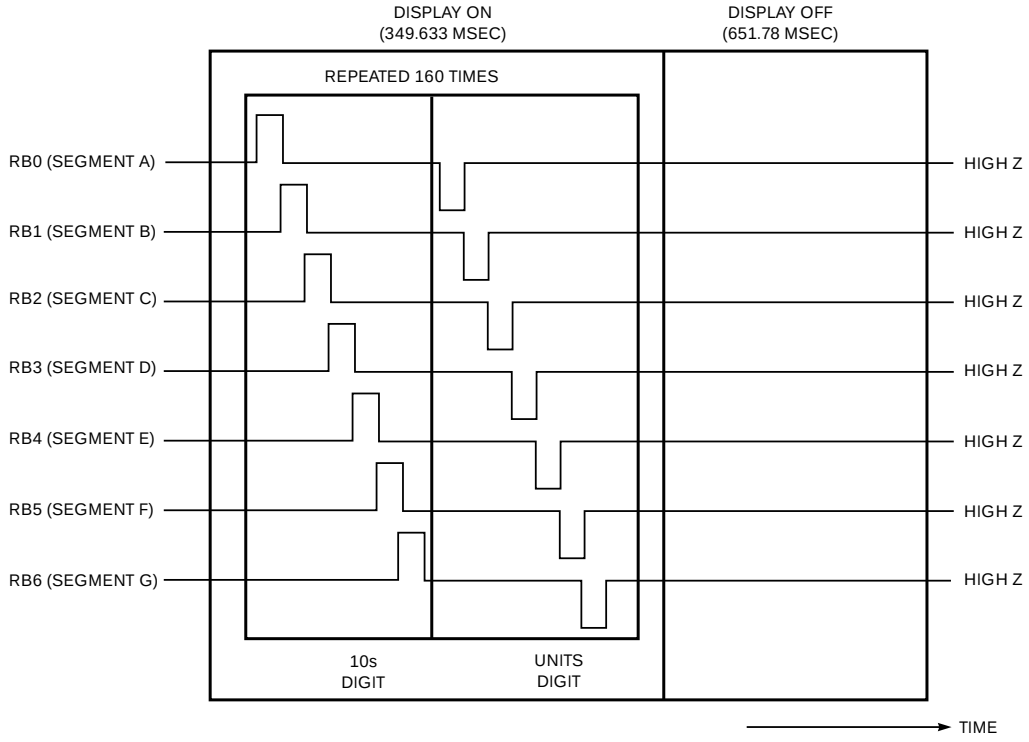

Figure 2 The timing diagram illustrates segment- and digit-drive intervals.

Two-wire, four-by-four-key keyboard interface saves power

Stefano Salvatori, University of Rome, Rome, Italy,
and Gabriele Di Nucci, EngSistemi, Rome, Italy

You can use a microcontroller that includes an ADC to design a two-wire-plus-ground keyboard interface. For example, you can use a resistive voltage divider to identify a pressed key (Reference 1). A microcontroller's integrated ADC typically presents an input resistance on the order of hundreds of kilohms, and, for adequate accuracy, its keypad divider should comprise relatively low-value resistors of 10s of kilohms. However, in battery-powered systems, a resistive divider can consume a few hundred microamperes, forcing a designer to choose an alternative classic digital-matrix array of switches and multiple I/O lines. Moreover, portable-equipment designs typically place constraints on the number of components.

To satisfy both requirements, the circuit in Figure 1 uses a matrix keypad and a resistor network divided into two row and column sections. For the four-by-four-key keypad, seven resistors are sufficient to encode any pressed key, and the circuit consumes power only while a key remains closed. Conversely, with no keys pressed, the standby current approaches zero. Using only two values of resistors, let $R_A=R_B=R_C=R_1$ and $R_D=R_E=R_F=R_G=R_2$. Assigning values from zero to three for the keys' x and y addresses, you can calculate the voltage across resistor R_G for any key closure by solving the following equation:

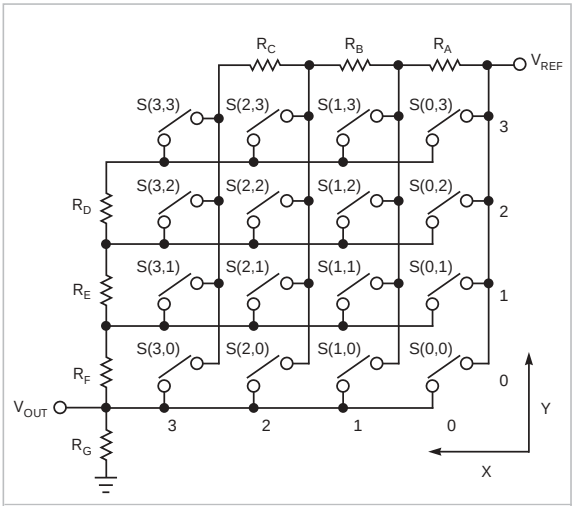

Figure 1 A two-wire resistive voltage-divider interface encodes a four-row-by-four-column keypad.

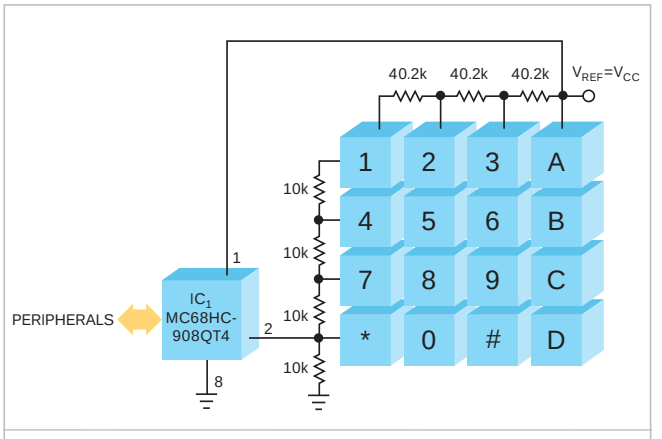

Figure 2 Using the microcontroller's analog reference-voltage output and ratiometric analog-to-digital conversion ensures correct encoding of the keypad.

TABLE 1 SINGLE-KEY OUTPUT CODES

Keys pressed/resistance (Ω)

Y \ X	3	2	1	0
3	1/ 15 to 16	2/ 21	3/ 32	A/ 63 to 64
2	4/ 17	5/ 23	6/ 36	B/ 85
1	7/ 18	8/ 25	9/ 42	C/ 127
0	*/ 19	8/ 28	#/ 51	D/ 255

Note: The figures preceding the slashes represent the keypad's key labels.

TABLE 2 TWO-KEY OUTPUT CODES

Keys pressed	Resistance (Ω)
C+#	141 to 142
C+0	134 to 135
C+*	132
B+#	109
B+0	98
B+9	91
B+8	88
A+8	76
A+7	70 to 71
A+6	68

$$V(x,y)=V_{REF}\times\frac{R_2}{x\times R_1+y\times R_2+R_2}.$$

Driving the resistor array from V_{REF}, the ADC's reference voltage, allows you to perform a ratiometric conversion that eliminates errors in key encoding due to fluctuations in V_{REF}. The following equation describes the voltage-division ratio, r(x,y), for any keystroke.

$$r(x,y)=\frac{V(x,y)}{V_{REF}}=\frac{1}{(1+x\times p+y)}.$$

The ratio $p=R_1/R_2$ represents the ratio between row- and column-group resistors' values. For p=4, you calculate 16 values of r(x,y), in the [1/16, 1] range, as a function of the pressed key's position. In general, the minimum difference between r partitioning ratios occurs for the nearest keys as the (3,2) and (3,3) x,y indexes indicate. For an N-bit ADC and a ratio of p=4, the ADC should have a resolution that satisfies the following equation: $2^{-N}<r(3,2)-r(3,3)=15^{-1}-16^{-1}=240^{-1}$. Note that the reciprocal of 240 (0.0041...) exceeds the reciprocal of 2^8, and the circuit thus requires an ADC capable of at least 8-bit resolution ($N\geq 8$ bits).

Unfortunately, standard-value components with nominal tolerance, T, cannot provide an ideal solution to this equation. Instead, you calculate a partitioning-ratio difference, $d=r(3,2)-r(3,3)$, for the worst-case condition. The lowest value of d occurs for a minimum value of R_G and R_D and the maximum value of R_A, R_B, R_C, R_E, and R_F. You can account for all the resistors' values and define a generic ratio, p, for the nominal values of R_1 and R_2:

$$d_{MIN}(p,T)=(1-T)^2/\{[3\times(p+1)+(3p+1)\times T]\times[(3p+4)+3\times p\times T]\}>2^{-N}.$$

The same value of T applies to all resistors. If n=8 and p=4, the previous equation yields a solution of $T<0.018$, which indicates that resistors of ±1% tolerance correctly encode 16 keys. Moreover, if you now impose the chosen fixed tolerance, T, you can solve the equation to obtain the required limit on the p ratio between the values of R_1 and R_2. If T=0.01, the solution to the equation becomes $p<4.074$.

The circuit in Figure 2 uses Freescale's (www.freescale.com) Nitron MC68HC-908QT4 microprocessor, which serves as a test bed for a keypad based on the above-calculated values, and uses pow-

er-supply voltage V_{CC} as the resistor matrix's reference voltage, V_{REF}. To satisfy the requirement for p(4.074 >p>4), use R_1=10 kΩ±1% tolerance and R_2=40.2 kΩ±1% tolerance, both standard values that the E48 series offers. Table 1 lists output codes corresponding to 16 individually pressed keys, and Table 2 lists data obtained when simultaneously pressing two keys and illustrates that two-key combinations can evoke special functions.

If your application requires a microcontroller that lacks an internal interrupt that the ADC generates, you can connect an external comparator to the output voltage in Figure 1. Set the comparator's threshold lower than the lowest voltage developed at the output voltage—approximately V_{REF} divided by 16 in the example—and the comparator's output serves as a keypad-interrupt source for the microcontroller.

Note that a microcontroller with a 10-bit ADC, such as a Freescale MC68-HC908QB or a Texas Instruments (www.ti.com) MSP430F11 can service a five-row by six-column keypad matrix encoded by 10 resistors. Repeating the analysis shows that a row-to-column p ratio of 5 to 5.51 and a required resistor tolerance of less than 4.3% correctly encode the keys. You can use values of 10 kΩ for R_1 and 51.1 kΩ or 53.6 kΩ for R_2 of the ±1%-tolerance E48 series.

REFERENCE

1 Amorim, Vitor, and J Simões, "ADC circuit optimizes key encoding," *EDN*, Feb 4, 1999, pg 101, www.edn.com/article/CA56657.

Gain-of-three amplifier requires no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Analog Devices' ADA4862-3 comprises three wideband amplifiers, each configured by an internal, fixed-value resistive-feedback network as a noninverting gain-of-two amplifier. Due to its internal feedback networks, the device offers a bandwidth of 300 MHz and excellent insensitivity to stray capacitance, variations in pc-board layout, and proximity of other devices. According to its specifications, each of IC_1's three internal amplifiers offers

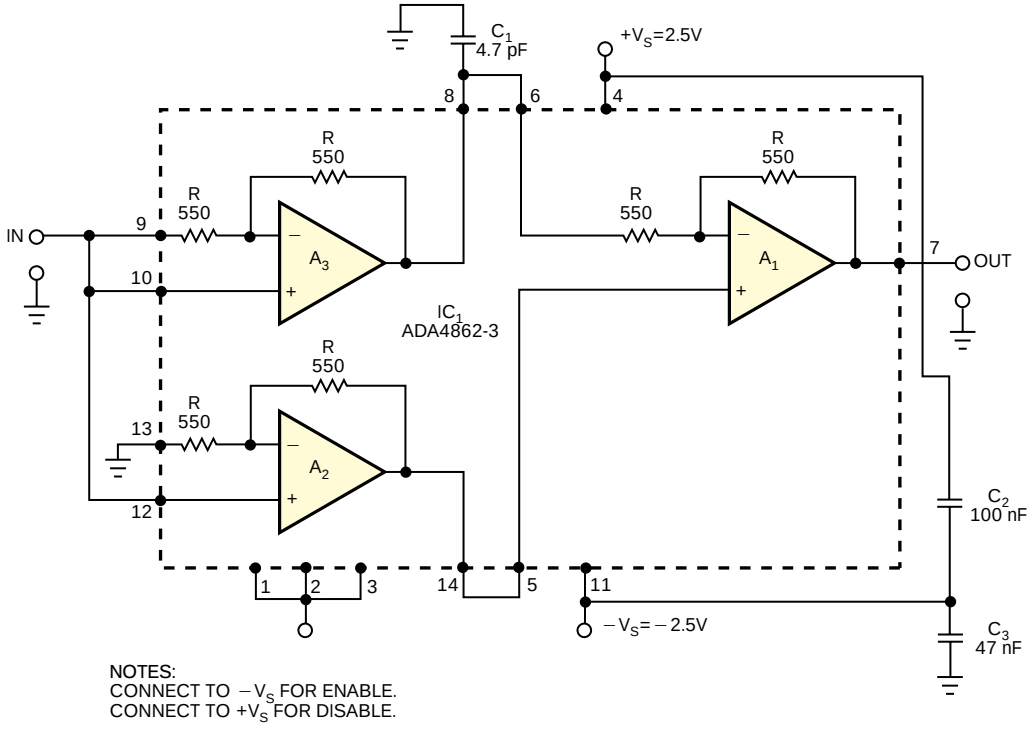

Figure 1 A one-IC amplifier with a voltage gain of three provides flat response to more than 60 MHz.

three gain configurations—two, one, or negative one (Reference 1). When you configure it for a gain of two, a cascade of two or three amplifiers yields gains of four or eight, respectively. If your application requires a gain of three, you can use the circuit in Figure 1. Amplifier A_3 serves as an impedance converter with a net voltage gain of one and a low-impedance driver for A_1's gain-setting network. Amplifier A_2 provides a gain of two at its noninverting input.

In addition, A_3 introduces the proper time delay (phase shift) in A_1's inverting-input path and thus roughly equalizes the time delay in A_1's noninverting signal path. This configuration improves the circuit's dynamic performance over that you can achieve when A_1's inverting input connects directly to the input signal. A 4.7-pF chip capacitor that connects from voltage follower A_3's output to ground reduces the voltage follower's output impedance at frequencies of 100 MHz and above to ensure A_1's stability.

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If you configure it as a differential amplifier, A_1 amplifies the input signal by a factor of two at its noninverting input and by a factor of negative one at its inverting input. The final voltage at A_1's output comprises the algebraic sum of both components: $V_{OUT}=4\times V_{IN}-V_{IN}=3\times V_{IN}$. In a conventional voltage amplifier, reducing negative feedback increases the overall gain. In contrast, cascading amplifiers with negative-voltage-feedback networks only slightly reduces the circuit's bandwidth. The net gain decrease at a frequency of 65 MHz amounts to 0.1 dB, or approximately 1.15% of a single gain-of-two amplifier's dc gain. For the gain-of-three amplifier in Figure 1, the gain decrease at 65 MHz amounts to approximately 2.3% of the circuit's dc gain.

For the best high-frequency performance, connect the ADA4862's internal amplifiers as Figure 1 shows to minimize the lengths of the device's external interconnections. You can cascade additional ADA4862-3 ICs to produce any gain expressed as $3^M\times 2^N$, where M and N represent integers, including zero—that is, gains of six, nine, 12, and so on. EDN

REFERENCE

1. ADA4862-3 data sheet, Analog Devices Inc, www.analog.com/UploadedFiles/Data_Sheets/360747397ADA4862_3_a.pdf.

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READERS SOLVE DESIGN PROBLEMS

PIC microprocessor drives 20-LED dot- or bar-graph display

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The circuit in Figure 1 uses only five I/O lines to drive a dot- or bar-graph display of 20 LEDs. Although this version of the design uses a small and inexpensive one-time-programmable microprocessor, such as a Microchip (www.microchip.com) PIC12C508A, you can use other microprocessors with N I/O lines to drive as many as $N\times(N-1)$ LEDs. For software development or modification, you can use a PIC12C508A-JW reprogrammable-EPROM version of the PIC12C508A, or you can substitute a less expensive PIC16F84A with flash memory.

To avoid application of excessive reverse voltage to the LEDs, the circuit's power supply, V_{DD}, must not exceed 3V dc. You can drive other types of loads and provide electrically isolated interfaces by replacing the LEDs with appropriately rated optocouplers. For demonstration purposes, IC_1's input line, GP3, connects to a pushbutton display-mode-selector switch and a pulldown resistor that simulates a digital-input-signal source with a voltage amplitude of 3V p-p.

Listing 1, available with the online version of this Design Idea at www.edn.com/060901di1, performs a variety of functions. To conserve battery power, the basic software drives one LED at a time in dot or bar mode with a minimum amount of current. Approximately 2 mA flashes a high-brightness LED. The software includes a delay routine that solves the problem of contact bounce. Tests show that a miniature pushbutton switch requires a delay of at least 1 msec for successful debouncing.

Consuming fewer than 256 words, the software avoids a C12C508A programming restriction that requires placement of subroutines only in page 0. Other features of the software include a two-level stack, the use of files common to both the PIC12C508A and

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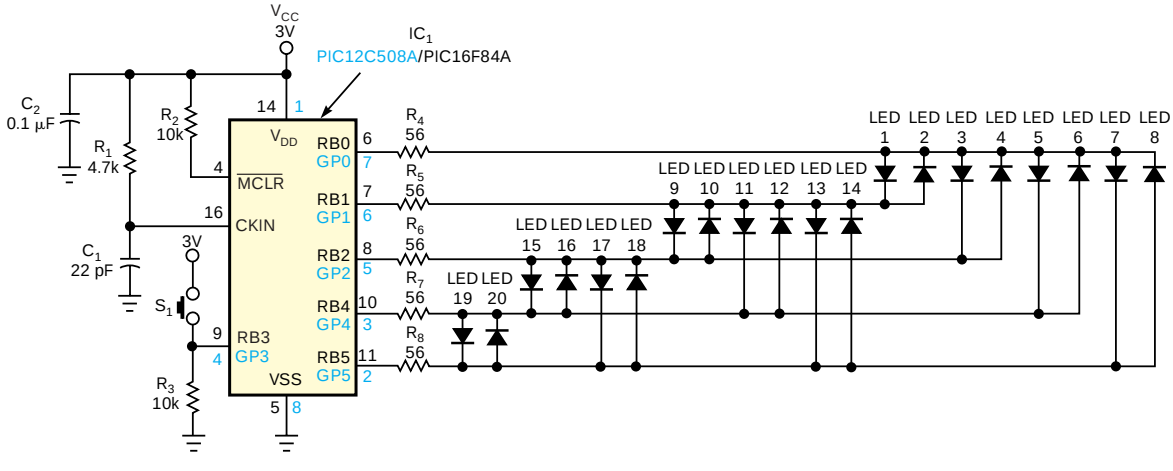

Figure 1 A dot- or bar-graph display uses either a one-time-programmable PIC12C508A or, for experimentation, a reprogrammable and reusable PIC16F84A. Use high-brightness diodes for LED 1 through LED 20.

the PIC16F84A in the $0C_H$ to $1F_H$ range, use of the RETLW 00_H instruction instead of Return, and avoidance of the ADDLW and SUBLW instructions. The software defaults to the dot-display mode. Pressing and holding S_1 before and during power application selects the bar-display mode. Note that the configuration settings for the MPASM assembler vary according to which microprocessor you select for programming. EDN

PC's serial port controls programmable sine-wave generator

Yongping Xia, Navcom Technology, Torrance, CA

This Design Idea describes a circuit that uses a PC's serial port to control a sine-wave generator that covers a frequency range of 2 Hz to 20 kHz in 1-Hz steps (Figure 1). The circuit's output voltage of approximately 2.2V p-p remains constant over the entire frequency range. The circuit's signal source, a Linear Technology (www.linear.com) LTC6904, IC_1, consists of a digitally programmable square-wave oscillator that, without using a clock crystal, covers a frequency of approximately 1 kHz to 68 MHz at 0.1% resolution and a few percentage points of accuracy. The LTC6904 features an I^2C serial-communications interface that controls the output frequency according to: $OSC_{CLK}=2a\times 2078\ Hz/[2-(b/1024)]$. The variables "a" and "b" represent 4- and 10-bit digital codes, respectively, and the equation's frequency unit, OSC_{CLK}, is in hertz.

The OSC_{CLK} output from IC_1 at Pin 6 drives IC_2, a 14-stage 74HC4020 binary counter whose outputs at Q4 and Q10 serve as the clock and input signals for IC_3, a Maxim (www.maxim-ic.com) eighth-order, switched-capacitor MAX291 lowpass filter.

The −3-dB corner of the filter's frequency response occurs at one-one-hundredth of IC_3's clock frequency. Fixed at one-sixty-fourth of the clock-signal frequency, only the input square wave's fundamental frequency can pass the filter without undergoing considerable attenuation. The filter's eighth-order response removes higher order harmonics, and the filter's output thus consists of a sine wave at the input's fundamental frequency. The filter's clock and input always occur in a 64-to-1 frequency ratio, and the sine wave's output amplitude thus remains constant over the entire frequency range.

To generate a 1-kHz sine wave, the circuit requires a filter clock at a frequency of 64 kHz, which sets the OSC_{CLK} frequency 64 times higher, or 1.024 MHz. To satisfy the equation, the LTC6904 requires programming constants of $a=09_H$ and $b=3d8_H$ to generate an OSC_{CLK} frequency of 1023.94 kHz and the nearest output frequency of 999.9 Hz.

Written for IBM-compatible PCs, the C-language program accompanying this Design Idea, which is available at www.edn.com/060901di2, accepts an

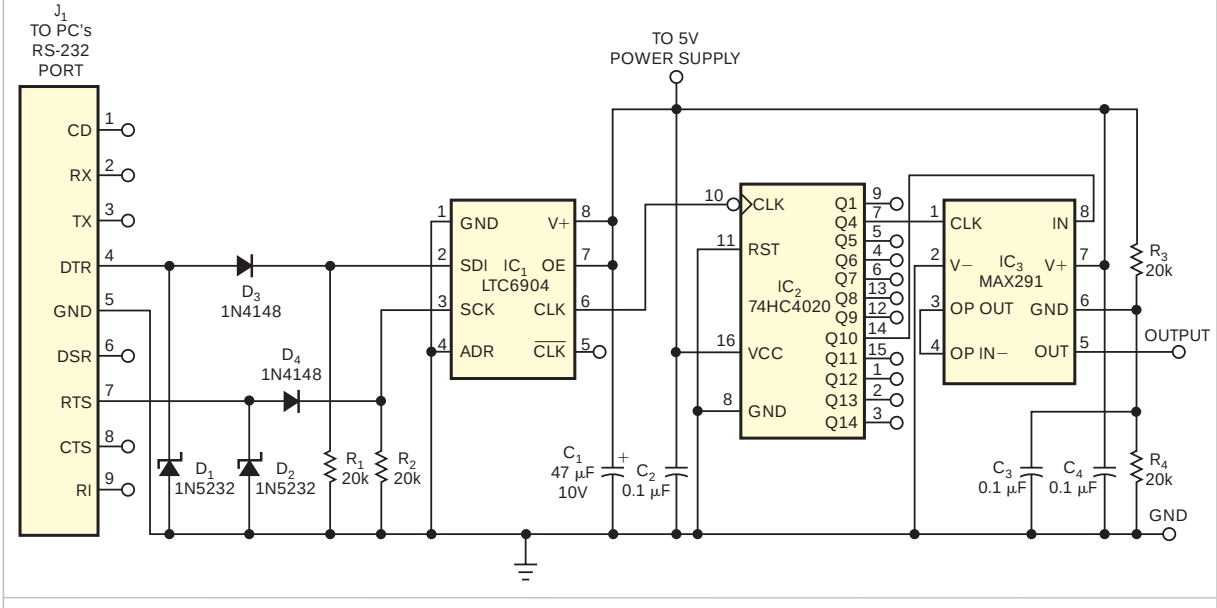

Figure 1 Three ICs and a few passive components generate sine waves under the control of a PC's serial port.

output-frequency request, calculates the nearest values of programming codes "a" and "b," transmits the codes to IC_1, and shows the calculated frequency on the PC's display. Although a PC's serial port delivers RS-232 signals, diodes D_1 through D_4 limit the voltages available at Pin 4, the data-terminal-ready pin, and Pin 7, the ready-to-send pin, to levels compatible with the I²C bus's SDI and SCK signals, respectively. EDN

I²C interface connects CompactFlash card to microcontroller

Fons Janssen, Maxim Integrated Products Inc, Sunnyvale, CA

Logging data from a large number of monitored channels usually requires a lot of memory for storing the measured data. Unfortunately, smaller microcontrollers offer only limited amounts of internal data RAM and EEPROM and may also lack spare address and data ports for adding external memory. Many low-end microcontrollers include an industry-standard I²C interface for attaching external ADCs, DACs, real-time clocks, and other peripherals.

The circuit in Figure 1 connects a CompactFlash card to a microcontroller's I²C interface through IC_1, a 16-bit I²C I/O extender. In memory-mapped mode, an 8-bit-wide data bus controls the CompactFlash card. Microcontroller IC_1's Port 1 (I/O lines 0 through 7) connects to the CompactFlash card's data bus and provides read and write access to the card's data registers. Port 2 provides the card's address and control registers and generates the read and write signals.

To write to a register, configure Port 1 as an output and write the data to the port. Next, write the register-control data three consecutive times to Port 2 while toggling the port's WR_N pin from Logic 1 to Logic 0 to Logic 1 to generate the "write" signal. Address bits A2, A1, and A0 select the register that receives the written data. Applying Logic 0 to the CE pin while RD_N rests at Logic 1 enables the CompactFlash card. To read from a register, configure Port 1 as an input port and apply three writes to Port 2 while toggling the port's RD_N pin from Logic 1 to Logic 0 to Logic 1 to generate the "read" signal.

After the three writes, the microcontroller reads Port 1 and makes the data available. Address bits A2, A1, and A0 address eight internal registers and allow read and write access (Table 1). Register 0x00 contains data for exchange between the host and the CompactFlash card. Registers 0x03, 0x04, 0x05, and 0x06 specify the track

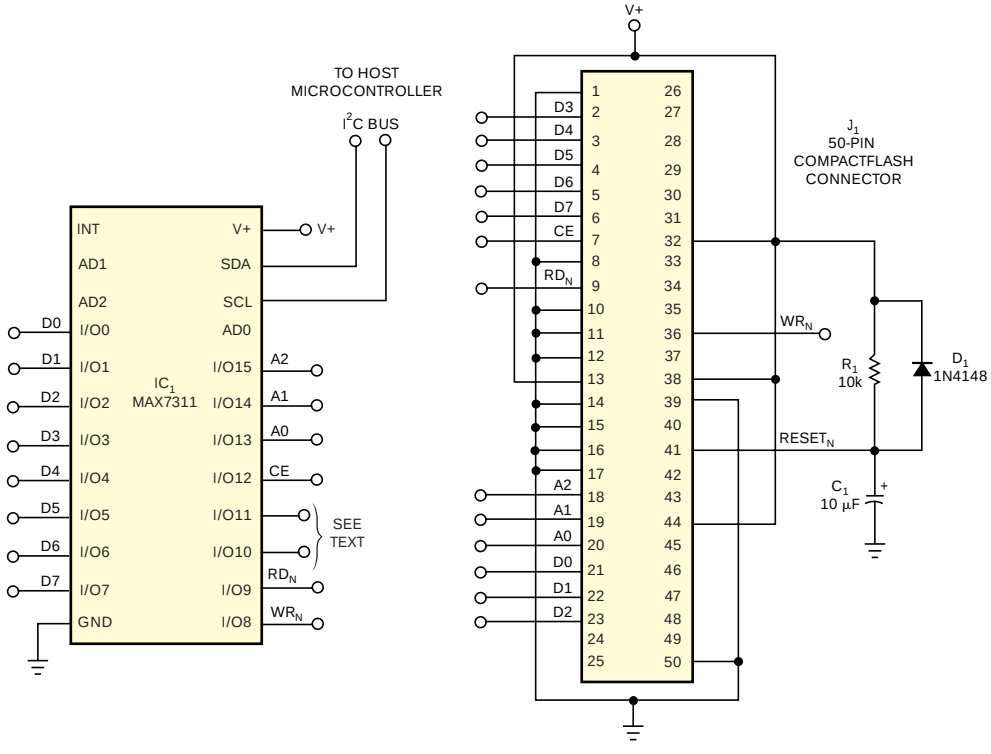

Figure 1 A 16-bit I/O extender, IC_1, and a CompactFlash connector add external data storage to a microcontroller's I²C bus.

for reading or writing data. Each track contains 512 data bytes. The processor indicates reading and writing tracks and other functions by writing to 0x07, the command register, and registers 0x01 and 0x07 contain error conditions and status information.

Two unused pins, 10 and 11, on Port 2 are available to drive LEDs that display circuit activity and status. As an alternative, the pins can support a user-installed configuration jumper. In this configuration, IC_1's interrupt output should connect to the host microcontroller's interrupt input so that installation or removal of the jumper can signal the microcontroller to recognize or ignore the CompactFlash card. Selecting a CompactFlash-card connector with hot-plugging contacts allows insertion or removal of a card without switching off power or disturbing an ongoing data-logging process.

With software modifications, a host microcontroller can switch between two CompactFlash cards. Adding a second MAX7311 supports an additional CompactFlash card and expands the circuit's storage capacity, and the hot-plug feature supports removal of a fully loaded card for data processing on another system. Microcontrollers that include hardware-based I^2C interfaces can use two relatively simple I^2C software functions to read and write a CompactFlash card through IC_1's I/O ports.

The first function is: Write_MAX 3711(slv,prt,dat). This procedure starts the I^2C bus and sends a data byte (dat) to a port (prt) on the MAX7311 using a slave address (slv). The other procedure, Read_MAX3711(slv,prt), starts the I^2C bus and reads a data byte from a port on the MAX7311 at a slave address. These functions serve as foundations for two additional functions, which read and write to the CompactFlash card's registers. The first, Write_CF_REG(reg,dat), uses Write_MAX3711 to place the data on Port 1. Use the same procedure to place the register address (reg) and other control signals on Port 2. Executing this function three times while toggling WR_N generates the write signal. The Read_CF_REG(reg) procedure uses Write_MAX7311 to address the CompactFlash card's register and generates the read signal. Invoking Read_MAX 7311 then reads the data from the register.

These functions, which in turn read and write the card's registers, create functions that access the CompactFlash-card sectors: Write_CF(cyl, head,sec). To perform a write operation, this procedure uses Write_CF_REG to designate the CompactFlash card's target cylinder, head, and sector registers (0x03 to 0x06). Next, writing 0x30 to the command register configures the CompactFlash card to accept data. Executing Write_CF_REG 512 times writes data in the microcontroller's global array to the data register. The CompactFlash card automatically adds this data to the current track. To perform a read operation, the Read_CF(cyl,head,sec) procedure uses Write_CF_REG to designate the target cylinder, head, and sector. Next, writing 0x20 to the command register configures the CompactFlash card to deliver data to the host processor. Executing Read_CF_REG 512 times reads all 512 bytes through the data register from the current CompactFlash card's track and places the data in a global array.

If the microcontroller lacks sufficient internal memory to store 512 data bytes, the software can write each digitized data-point measurement directly to the CompactFlash card. For additional information on controlling CompactFlash cards, review the material in Reference 1. EDN

TABLE 1 ADDRESSES AND REGISTERS

Address	Register	Address	Register
0x00	Data	0x04	Cylinder low
0x01	Error/features	0x05	Cylinder high
0x02	Sector count	0x06	Select card/head
0x03	Sector number	0x07	Status/command

REFERENCE

1. CF+ and CompactFlash specification, www.compactflash.org.

IC and DMM form direct-read-out temperature probe

Alfredo H Saab and Bich Pham,
Maxim Integrated Products Inc, Sunnyvale CA

The simple temperature-measurement probe in Figure 1 can serve as an indispensable tool for troubleshooting and debugging electronic circuits. To measure temperature at several points, you can equip IC_1, a Maxim (www.maxim-ic.com) MAX-6610, with a probe, or you can permanently integrate one or more devices into a pc board or attach them to components. Resistors R_1, R_2, and R_3 set the circuit's temperature-scaled voltage output to various values (Table 1). Figure 2 shows the circuit's representative output versus temperature.

You can display the circuit's temperature-proportional dc output voltage on any DVM (digital voltmeter) or handheld DMM (digital multimeter). The circuit draws only 200 μA from a nominal 3V power supply, such as a pair of AA alkaline cells. A CR2016 lithium-coin cell can operate the circuit continuously for several hundred hours or for several years if you equip the circuit with a normally open, momentary-contact pushbutton switch.

To produce the error curve in Figure 3, immerse the circuit and a platinum-resistance standard thermometer in a

temperature-controlled oil bath. The circuit's relative error with respect to the standard thermometer varies only 4°C over −40 to +125°C. The MAX-6610's data sheet includes additional information on temperature-measurement error and output range.

To apply the circuit as a temperature probe, solder a 5-mm length of 1-mm-diameter, uninsulated copper wire directly to a small copper pad at IC_1's GND pin. The wire should make thermal and electrical contact with the GND pin and thus provide a path of low thermal resistance from the sensor IC to the point of probing. Glue the wire to the pc board to add mechanical support. Heat loss affects the temperature measurement's accuracy, and, to minimize heat loss from the probe through the pc board, use long and thin copper traces to make electrical connections from IC_1 to its supporting components.

Applying the MAX6610 as a pc-board temperature sensor differs somewhat from using it as a temperature probe. For board-temperature sensing, IC_1 must reside in intimate thermal contact with the board. Connect large copper areas immediately to the IC's pins and use short, thick traces—or none at all—between the copper areas and the IC's pins. The copper areas guarantee accurate temperature readings by providing thermal contact with the board and good heat transfer between the board and the sensor. EDN

REFERENCE

1 "Precision, Low-Power, 6-pin SOT23 Temperature Sensors and Voltage References," MAX6610/6611 data sheet, Maxim Integrated Products, November 2003, http://pdfserv.maxim-ic.com/en/ds/MAX6610-MAX6611.pdf.

TABLE 1 TEMPERATURE-SCALED VOLTAGE OUTPUT

	10 mV/°C	1 mV/°C	1 mV/°F
R_1 (kΩ)	68.1	68.1	68.1
R_2 (kΩ)	2.8	2.8	19.6
R_3 (kΩ)	Open	2.21	3.32

Note: All resistors are of ±10% tolerance.

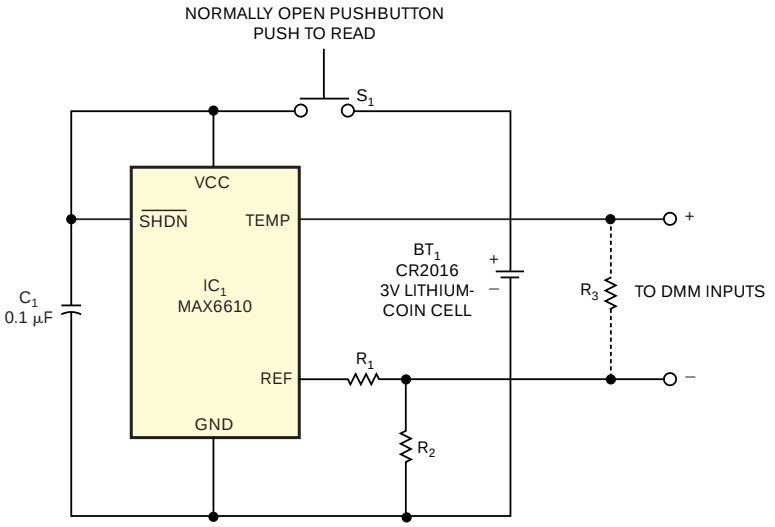

Figure 1 One IC and a few passive parts directly display temperature on an external voltmeter. See Table 1 for values for R_1, R_2, and R_3.

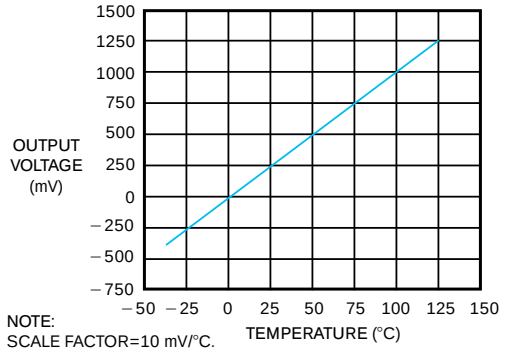

Figure 2 The circuit of Figure 1 exhibits a nearly linear output-voltage-versus-temperature characteristic.

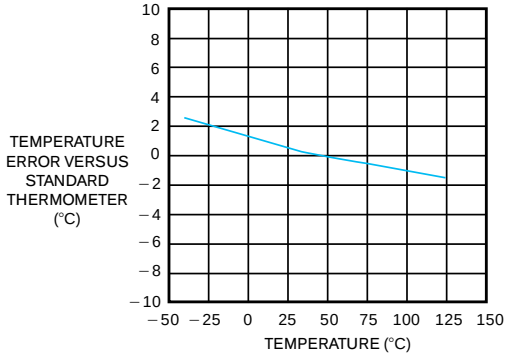

Figure 3 Immersed in a temperature-controlled oil bath and compared with a platinum-resistance standard thermometer, the circuit of Figure 1 exhibits ±2°C error over −40 to +125°C.

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READERS SOLVE DESIGN PROBLEMS

"Brick-wall" lowpass audio filter needs no tuning

Diego Puyal and Pilar Molina, University of Zaragoza, Zaragoza, Spain

When a system's specifications call for a lowpass filter with a steep frequency-cutoff characteristic, an engineer can opt for a "brick-wall"-filter design that features a sharp transition band. For example, in an FM stereophonic-broadcast system, the lowpass filter in the baseband audio's left and right channels should have a −3-dB cutoff frequency of at least 15 kHz, a passband ripple of less than 0.3 dB, a stopband start frequency of at least 19 kHz, a stopband attenuation greater than 50 dB, and identical phase response for both channels.

The filter should provide adjustable gain to maximize SNR at the audio processor's first stage. The filter's frequency response should also include a notch at 19 kHz to achieve maximum attenuation at the FM-subcarrier pilot-tone frequency and thus minimize phasing problems. To reduce manufacturing costs, the filter should require no in-process adjustments. Conventional analog active-filter designs cannot meet these goals at reasonable cost and complexity without time-consuming adjustments. This Design Idea outlines an active-filter-synthesis approach that reduces a filter's sensitivity to passive-component tolerances and enables construction of inexpensive, high-order and highly selective filters.

The design process begins with selection of an appropriate passive-filter topology—in this example, a seventh-order elliptic filter with 50Ω input and output impedances (Figure 1). Setting the beginning of the stopband frequency span at 18.72 kHz produces a notch at the 19-kHz stereo-pilot frequency. Using the following equation to transform each component's impedance leaves the filter's amplitude-versus-frequency response characteristics unaltered.

$$Z'(s)=\frac{k}{s}\times Z(s).$$

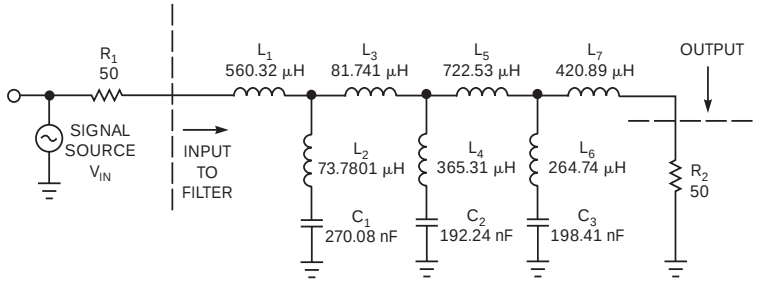

Figure 1 This seventh-order, elliptic, lowpass, passive-filter prototype features a 15-kHz cutoff frequency and stopband rejection exceeding 50 dB.

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As a result of the transformation, all resistors undergo transformation into capacitors, and adjusting the value of parameter k yields reasonable capacitance values for using 10%-tolerance parts. In this instance, select a value of 2.2 nF for C_1':

$$k=\frac{1}{R_1\times C_1'}.$$

Inductors transform into resistors, and using 2%-tolerance or better components meets the circuit's requirements. Capacitors transform into "supercapacitors" whose impedance exhibits a $1/s^2$ dependence:

$$Z'(s)=\frac{k}{s}\times\frac{1}{C_i s}=D_i'\times\frac{1}{s^2}.$$

Selecting a topology for a passive filter that contains the maximum number of inductors and references all capacitors to ground yields a transformed filter that consists of many resistors, several supercapacitors, and only two capacitors. You cannot obtain a supercapacitor as an off-the-shelf component, but its electrical analog comprises a few operational amplifiers and resistors (Figure 2). The following equation defines the gyrator's input impedance, Z_{IN}, with respect to ground:

$$Z_{IN}=\frac{Z_1\times Z_3\times Z_5}{Z_2\times Z_4}.$$

Selecting $Z_1=Z_3=1/Cs$ in the equation, setting capacitor value C at 2.2 nF, replacing impedances Z_2 and Z_5 with R=11 kΩ, and setting $Z_4=R_4$ yield a solution for D_i':

$$D_i' = \frac{C^2}{R_4}.$$

Figure 2 shows the filter's final schematic. Potentiometer R_1 adjusts the overall gain, and connecting resistors R_2 and R_{26} in parallel with capacitors C_1 and C_8 prevents dc blocking. The finished filter design uses medium-tolerance resistors, only eight capacitors, and two LF347 quad operational amplifiers—few amplifiers for a seventh-order active filter that requires no component adjustments to meet its specifications. Thanks to the design's precise implementation of the pilot-tone-rejection notch, the filter's measured attenuation at 19 kHz exceeds 60 dB. EDN

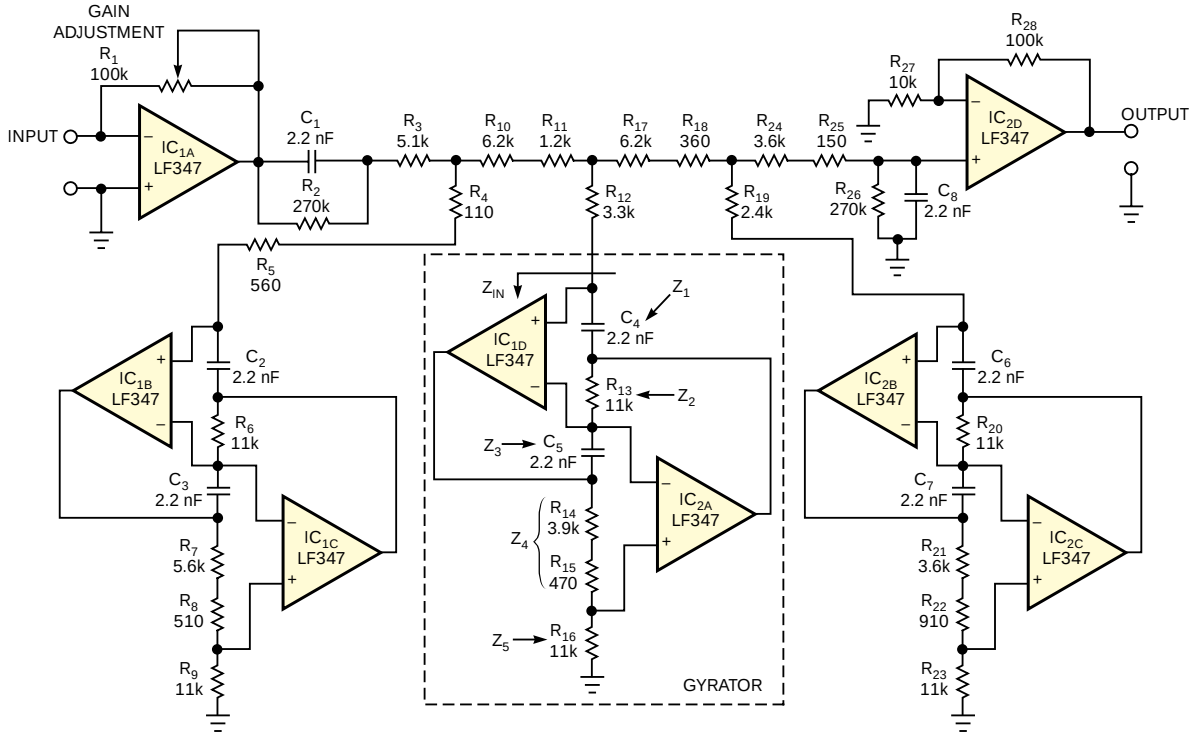
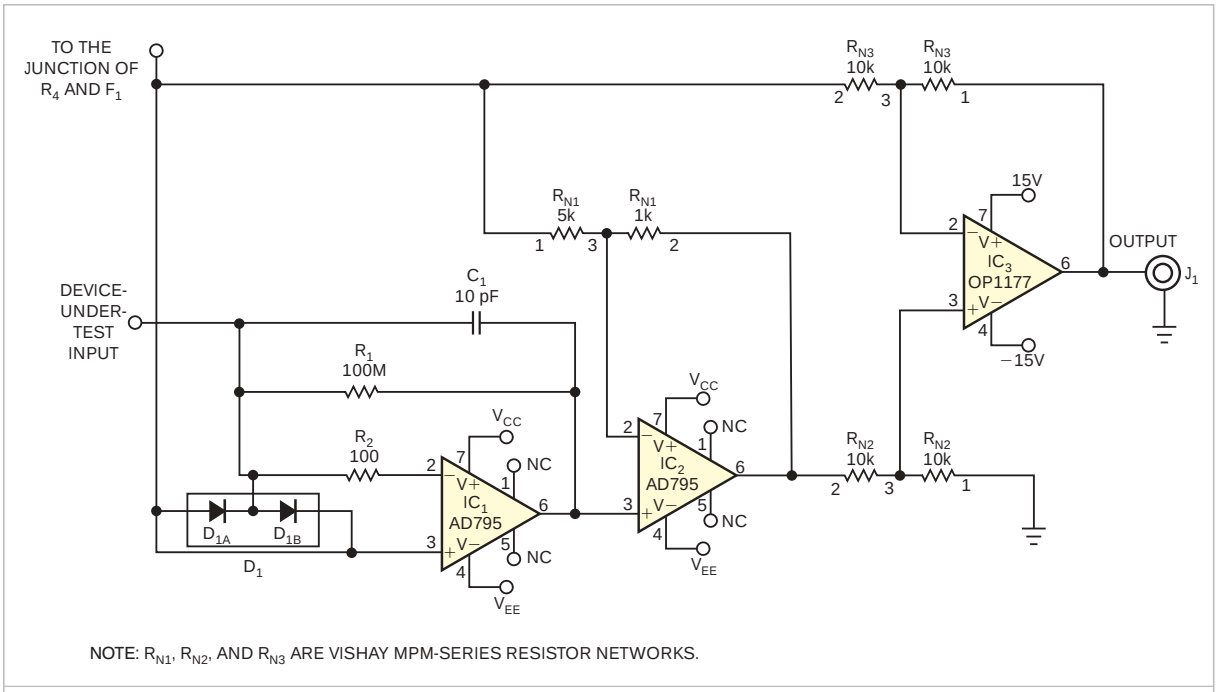


Figure 2 The finished circuit design eliminates inductors and substitutes gyrators as "supercapacitors." Using medium-tolerance components and quad op amps to reduce component count minimizes circuit cost.

Fast-settling picoammeter circuit handles wide voltage range

Rob Whitehouse, Analog Devices, Wilmington, MA

Evaluating analog switches, multiplexers, operational amplifiers, and other ICs poses challenges to IC-test engineers. A typical test scenario requires application of a test or forcing voltage to a device's input and measurement of any resultant leakage and offset currents, often at levels of 1 pA or less. In contrast to slow and expensive commercially available automated testers, the low-power measurement circuit in figures 1 through 3 can force a wide range of test voltages and offer fast settling to maximize device-test throughput. Extensive use of surface-mounted components minimizes



NOTE: R_{N1}, R_{N2}, AND R_{N3} ARE VISHAY MPM-SERIES RESISTOR NETWORKS.

Figure 1 This IVC uses a feedback-ammeter topology, which subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current.

its pc-board-space requirements and allows packaging of multiple measurement circuits close to the test fixture.

The circuit comprises a forcing-voltage buffer/amplifier, a floating-rail power supply, and an IVC (current-to-voltage converter). Applying a forcing voltage to a device under test induces leakage current, which the circuit converts to an output voltage proportional to the leakage current. In a conventional IVC, the current to be measured develops a voltage across a shunt resistor. The IVC uses a feedback-ammeter topology in which operational amplifier IC_1, an Analog Devices AD795, subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current (Figure 1).

In this design, the input's dc resistance consists mostly of R_2 and IC_1's effective input resistance, or slightly more than 100Ω at dc. At frequencies in the power-line range of 50 to 300 Hz, the circuit's ac impedance averages approximately 10 kΩ, or 1000 times less than a typical shunt-resistance IVC's input resistance of approximately 10 MΩ. The circuit's 100-MΩ feedback resistor, R_1, provides a current-to-voltage-conversion ratio that exceeds the shunt-conversion ratio by a factor of 10. This design settles much faster and provides better interference rejection at power-line frequencies than shunt converters. It also reduces unwanted voltage-divider effects when testing operational amplifiers' input currents.

R_1 produces a current-to-voltage-conversion ratio of 100 μV/pA. Amplifier IC_2, an AD795, provides an additional voltage gain of 10, boosting the ratio to 1 mV/pA and reducing the effect of errors that differential ampli-

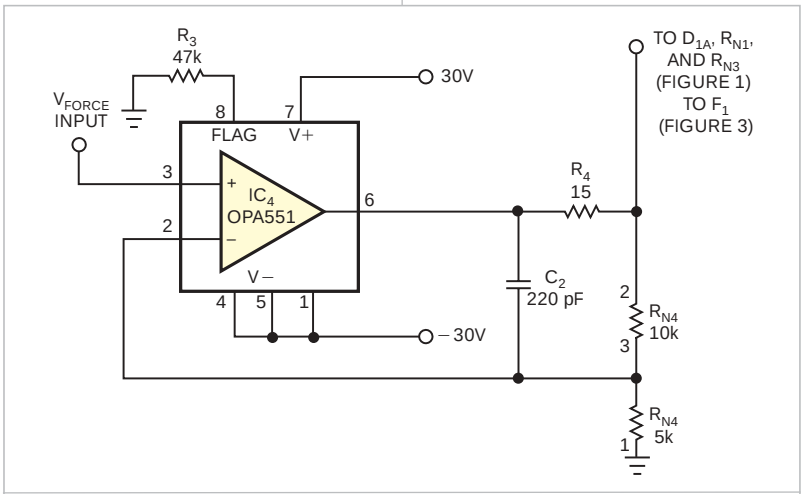


Figure 2 A gain-of-three high-voltage amplifier derives forcing voltages as high as ±22V from voltages of ±7V from test equipment.

fier IC_3's CMRR (common-mode-rejection ratio) introduces. Differential amplifier IC_3, an OP1177, subtracts the forcing voltage from the IVC's output and provides a ground-referenced output signal.

A back-to-back pair of BAV199 diodes, D_{1A} and D_{1B}, protects IC_1 from voltage overloads by shunting high currents to the forcing-voltage amplifier, IC_4, and its protective fuse, F_1. When the forcing voltage rapidly slews from one value to another, the diodes greatly improve the IVC's settling time by providing high-drive currents during high-slew-rate intervals.

Operating from ±30V supply rails, a lightly compensated, gain-of-three, high-voltage OPA551 amplifier, IC_4, derives forcing voltages as high as ±22V from ordinary ATE (automatic-test-equipment) voltages of ±7V (Figure 2). In case of a catastrophically shorted device under test, fuse F_1 prevents further damage by limiting fault current from IC_4, which can deliver as much as 380 mA of short-circuit current.

The output of IC_4 also drives a regulator circuit that produces ±5V floating-power-supply voltages referenced to the test-input forcing voltage (Figure 3). This part of the circuit dissipates less than 100 mW of power with ±30V supplies. Vishay/Siliconix (www.vishay.com) SST505 JFET constant-current regulator "diodes" Q_1 and Q_4 provide 1-mA constant-current sources, which transistors Q_2 and Q_3 buffer. Each current-regulator diode carries a 45V maximum rating, and the buffers provide overvoltage protection by limiting the voltages applied across the diodes to approximately 3V.

Applying 1 mA to resistors R_5 and R_6 develops the ±5V rail voltages. Diodes D_2 and D_3 compensate for the base-emitter-voltage drops across emitter followers Q_{6B} and Q_{7B}. Transistors Q_{6A} and Q_{7A} provide overvoltage protection when a defective device under test short-circuits its power supply to the IVC's input node. Transistors Q_5 and

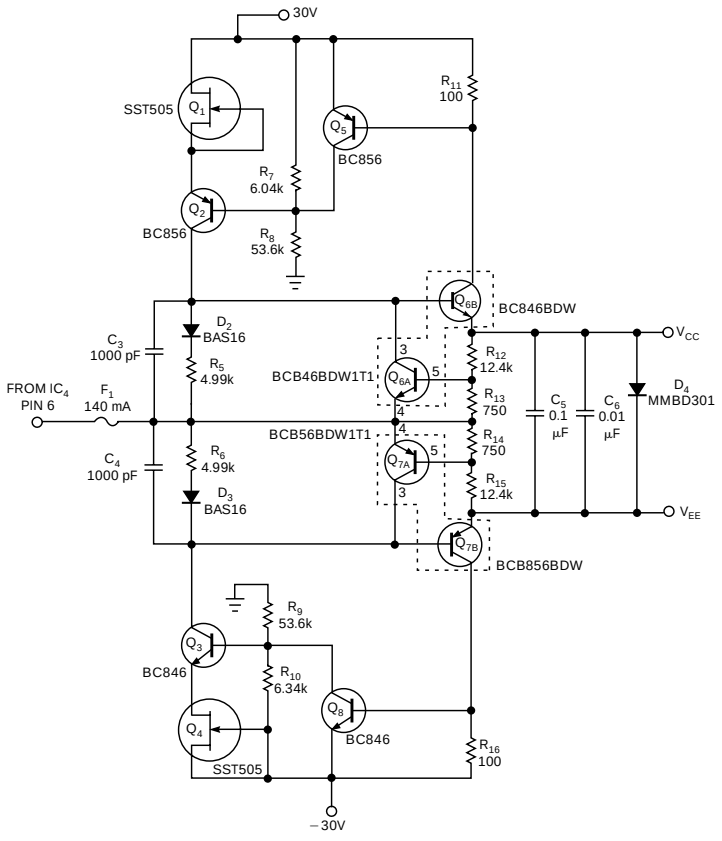


Figure 3 This floating-regulator circuit produces ±5V floating-power-supply voltages V_{CC} and V_{EE} referenced to the test input's forcing voltage.

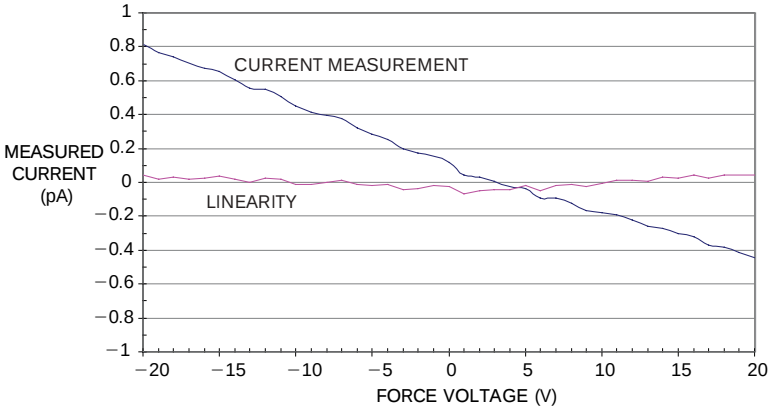


Figure 4 Over a ±20V forcing-voltage span, the circuit produces an unloaded-output current-measurement error of −31 fA/V.

Q_8 limit the floating supplies' output currents by shunting the current diodes. Diode D_4 protects against polarity inversion of the floating-supply rails during unusual start-up conditions.

In operation, the circuit delivers an output of 0.999V/nA over a ±4-nA full-scale input range at an effective transresistance of 1 GΩ. The circuit's output offset corresponds to approximately 143 fA. Beyond the forced-voltage span of ±22V, the floating-supply-rail voltages begin to saturate, the input-CMRR limitations of IC_3 become evident, and the IVC's output voltage becomes nonlinear. Figure 4 shows the circuit's current-measurement error of −31 fA/V from the circuit's unloaded output over a ±20V forcing-voltage span. The differential amplifier comprising IC_3, R_{N2}, and R_{N3} contributes most of the circuit's gain, and IC_1's low input-bias current contributes to the low offset error. Output linearity over the ±20V forcing-voltage range averages 111 fA p-p.

THE CIRCUIT'S SLEW-RATE CAPABILITY VARIES CONSIDERABLY, BUT IN GENERAL THE OUTPUT FAITHFULLY SLEWS THE ENTIRE 40V FORCING-VOLTAGE SPAN IN 100 µSEC OR LESS.

The circuit's slew-rate capability varies considerably, but in general the output faithfully slews the entire 40V forcing-voltage span in 100 µsec or less as D_1 drives the device under test. Once the high-slew period completes, the IVC comes out of saturation, and its output becomes an exponential voltage with a time constant of 1 msec. The output settles to 100 fA in approximately 10.6 msec. Under no-load conditions, the circuit consumes approximately 10.2 mA from the ±30V supplies and 400 µA from the ±15V supplies. The prototype circuit's layout occupies approximately 1.5 $in.^2$ on a single-sided pc board, and placing components on both sides of a double-sided board would reduce the area to 1 $in.^2$ For best performance, the layout must include guard rings around the input terminal and all traces attached to Pin 2 of IC_1. The circuit's size allows its placement on a device-under-test fixture to minimize lead lengths and power-line-induced electromagnetic interference. Although able to measure currents as small as 1 pA, the circuit can accommodate larger currents by reducing the value of R_1.EDN

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READERS SOLVE DESIGN PROBLEMS

High-impedance buffer amplifier's input includes ESD protection

Eugene Palatnik, Waukesha, WI

Certain measurement applications, such as for pH (acidity) and bio-potentials, require a high-impedance buffer amplifier. Although several semiconductor manufacturers offer amplifier ICs featuring low bias and offset-input currents, attaching a sensor cable to an amplifier circuit can inflict damage from ESD (electrostatic discharge). Figure 1 shows one unsatisfactory approach to ESD protection. Resistor R_1 limits an ESD event's discharge current, and diodes D_{1A} and D_{1B} clamp amplifier IC_1's input to its power-supply rails. Unfortunately, when shunting a pH sensor's 400-MΩ input impedance, even low-leakage diodes, such as Fairchild Semiconductor's (www.fairchildsemi.com) MMBD-1503A, introduce significant offset voltages.

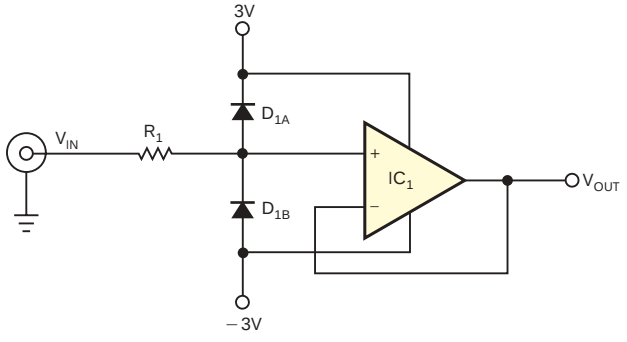

Figure 1 In a conventional ESD-suppression circuit, diodes clamp an amplifier's input voltage to its power-supply rails but introduce unwanted leakage currents.

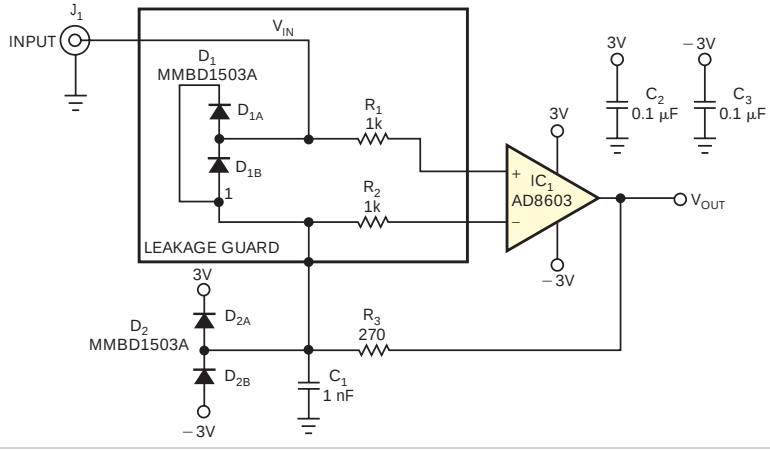

Figure 2 In this alternative design, voltage across both halves of D_1 normally approaches 0V and introduces no leakage currents. During an ESD event, both D_1 and D_2 conduct to protect IC_1's inputs.

The circuit in Figure 2 offers an alternative approach. An Analog Devices (www.analog.com) low-input-bias, low-offset-current AD8603 amplifier, IC_1, serves as a unity-gain input buffer. For any normal input, the circuit's output voltage, V_{OUT}, equals its input voltage, V_{IN}. Thus, the voltage across ESD-protection diode D_{1A} or D_{1B} approaches 0V, and neither diode's leakage current affects the sensor's output signal. Depending on the polarity of an ESD event you apply to the circuit's input connector, its high-voltage spike discharges through diode D_{1A} or D_{1B} into the positive or the negative

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power-supply rail. Capacitor C_1 acts as an intermediate "charge reservoir" that slows the ESD spike's rate of rise and protects IC_1's output stage from latching until diode D_{2A} or D_{2B} begins diversion of the ESD transient into the positive or the negative supply rail. In effect, C_1 compensates for D_1's parasitic capacitance. Resistor R_3 allows IC_1 to drive the capacitive load that C_1 presents without going into oscillation.

During an ESD event, both D_1 and D_2 can conduct, but the voltage at V_{IN} exceeds the power-supply-rail voltage by only two forward-biased diode voltage drops. Resistors R_1 and R_2 limit the amplifier input's currents below the manufacturer's recommended 5-mA maximum rating.

When packaging the circuit, pay special attention to the pc board's layout. Imperfections in the board's dielectric properties can provide parasitic-leakage-current paths. Adding copper traces on both sides of the board to form guard rings around the circuit's high-impedance nodes diverts leakage currents (Figure 3).EDN

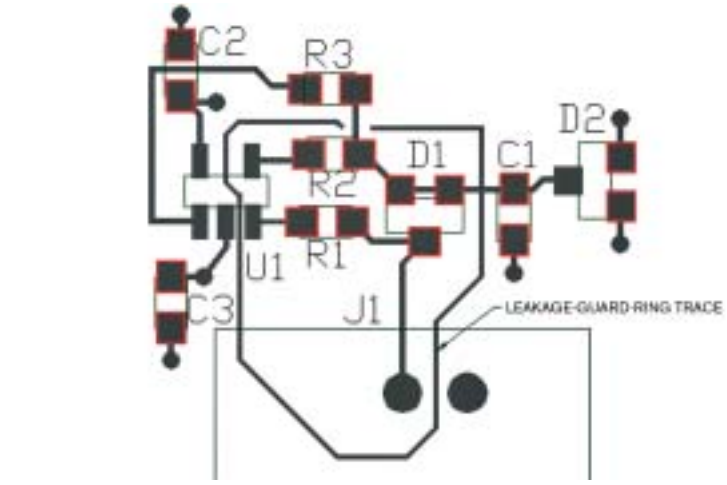

Figure 3 For best performance, place copper traces around the amplifier's high-impedance points to intercept leakage currents.

Composite-VGA encoder/decoder eases display upgrade

Werner Schwiering, Joystick Scoring Ltd, Whitby, ON, Canada

An older computer system fed RGB video and composite-synchronization signals through four 75Ω coaxial cables to an RGB color monitor 150 feet away. To upgrade it, the replacement VGA video cards could directly drive the 75Ω loads that the VGA monitors' internal terminations presented. However, the VGA standard uses separate horizontal and vertical positive-going synchronization signals. Adding an extra coaxial cable to the original cables to carry the separate synchronization signals presented a difficult and expensive proposition. An obvious solution would be to combine the separate synchronization signals into a composite format.

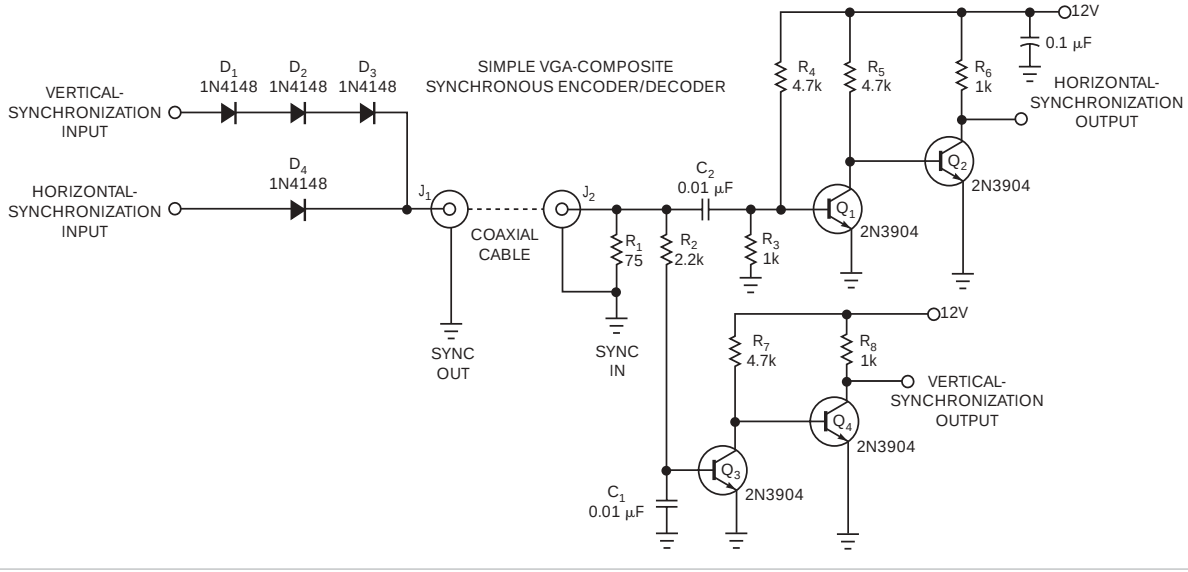

Figure 1 The synchronization-pulse combiner and recovery circuits comprise readily available and inexpensive components.

The combiner circuit in Figure 1 offers simplicity, low cost, and rapid assembly from readily available spare parts.

In operation, two 1N4148 diodes, D_1 and D_2, attenuate the VGA signal's 5V logic-level vertical-synchronization pulses by 1.4V, and diodes D_3 and D_4 form a diode-logical-OR gate to combine the vertical- and horizontal-synchronization pulses. The resultant output signal comprises an approximately 4.3V horizontal-synchronization signal superimposed on a 2.9V vertical-synchronization signal.

At the receiving end, a capacitively coupled highpass filter extracts the horizontal-synchronization signal, and a simple RC (resistor-capacitor) lowpass circuit removes horizontal-synchronization pulses from the directly coupled vertical-synchronization signal. Transistors Q_1 and Q_2 amplify the recovered horizontal-synchronization pulses, and transistors Q_3 and Q_4 amplify the vertical-synchronization pulses. The circuit's resulting outputs consist of clean synchronization pulses that closely approximate those of the original and provide extremely stable synchronization pulses for a VGA monitor operating at 640×480-pixel resolution (Figure 2).EDN

Figure 2 Applying the diode-gated composite-synchronization waveform to a 75Ω load results in clean synchronization pulses.

Solenoid-protection circuit limits duty cycle

Panagiotis Kosioris, Inos Automation Software, Stuttgart, Germany

Several safety-critical solenoids in a laser-measurement system on an automotive-assembly line required protection from internal overheating during normal operation. After a 60-sec activation, the solenoids required 180 sec to cool before their next activation. One apparently straightforward protection circuit would comprise a timer based on a microcontroller, some support components, and a short program written in C++. However, the project would require evaluation and selection of a suitable microcontroller, purchase or rental of a device programmer, and considerable time in programming the microcontroller and evaluating its operational hazards.

As an alternative, I recalled the words of my tutor: "Decrease the number of dangerous components to decrease the risk of danger." A simple analog circuit would be safer, smaller, and easier to maintain. The circuit in Figure 1 uses a traditional analog method of measuring time: the charge and discharge behavior of a resistance-capacitance circuit.

Figure 2 highlights the circuit's timing components. Capacitor C_2, a tantalum electrolytic with ±10% tolerance, diode D_1, and resistors R_2 and R_5 constitute a double-RC (resistor-

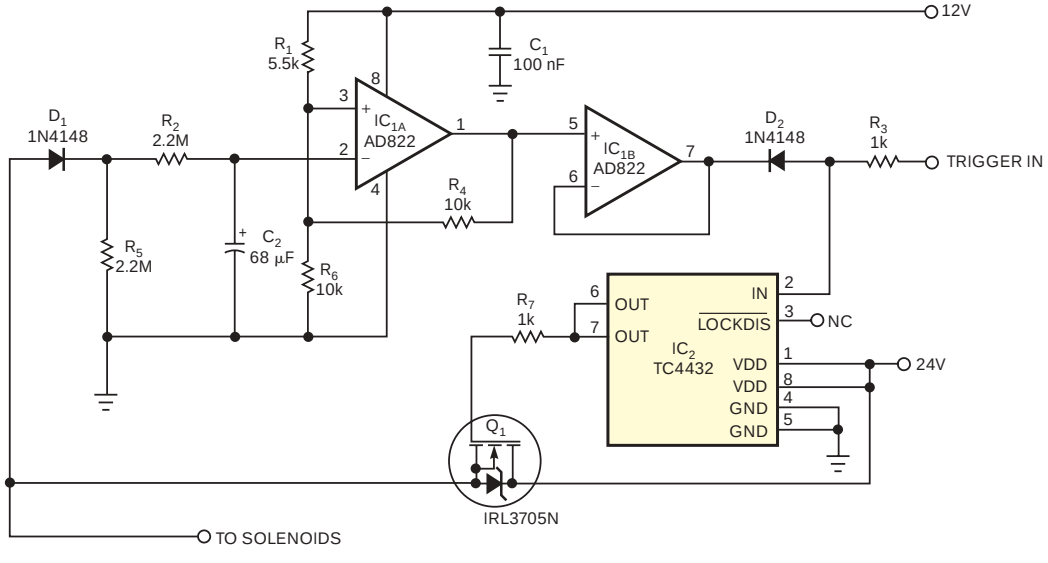

Figure 1 An externally triggered solenoid driver features an analog duty-cycle limiter.

capacitor) circuit. During solenoid activation, R_2 provides a charging path for C_2, and diode D_1 prevents C_2 from discharging through the solenoids. When the solenoids are off, the discharge path comprises R_2 plus R_5, which provides a longer time constant. The difference between the two time constants determines the solenoids' activation and recovery periods. A Schmitt trigger designed around one-half of IC_1, an Analog Devices (www.analog.com) AD822 dual operational amplifier, senses the voltage across C_2 and defines the solenoids' cutoff- and turn-on-timing intervals. An intermediate buffer stage, IC_{1B}, drives a Microchip (www.microchip.com) TC4432 MOSFET driver, which in turn controls the gate of Q_1, an N-channel power MOSFET that drives the solenoids from 24V.

When Q_1 switches on, the voltage level across C_2 increases, and, after 60 sec, the output of the Schmitt trigger falls from 12 to 0V. The buffer stage drives the cathode of diode D_2 to 0V. The voltage at D_2's anode reaches 0.7V and is insufficient to trigger MOSFET-driver IC_2. Q_1 now switches off, removing supply voltage from the solenoids and reverse-biasing diode D_1. Capacitor C_2 starts to discharge through R_2 and R_5, and the input voltage you apply to the Schmitt trigger falls at a slower rate than during the charging interval. After 180 sec, the Schmitt trigger's output rises to 12V, and the circuit awaits arrival of another external trigger pulse through resistor R_3.EDN

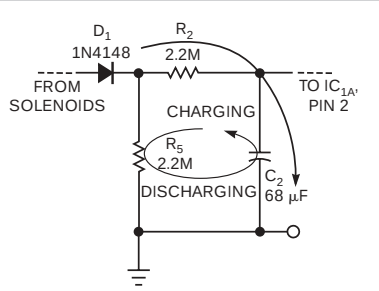

Figure 2 A resistance-capacitance circuit determines on- and off-time intervals.

SPST pushbutton switch combines power-control, user-input functions

Eugene Kaplounovski, Vancouver, BC, Canada

This Design Idea describes an enhancement to a previous one (Reference 1). The circuit in Figure 1 uses a normally open SPST pushbutton switch, S_1, instead of the SPDT switch that the original design required. You can use a membrane switch to significantly simplify the industrial design of the device and enhance its ergonomics. In addition, this circuit slightly reduces the current drain in active mode by eliminating current flow through the unactuated switch.

In standby mode, MOSFET Q_1 remains off and consumes less than 1 µA of leakage current from the battery. Pressing switch S_1 turns on Q_1 by pulling its gate to ground through diode D_1. Voltage regulator IC_1 turns on and supplies power to microcontroller IC_2. The microcontroller boots up and asserts its P1.1 output high, turning on transistor Q_2 and latching on the system's power to allow release of S_1. Meanwhile, resistor R_3 pulls the microcontroller's input, P1.2, to V_{CC}. Pressing the switch a second time pulls the microcontroller's P1.2 input low through diode D_2 and signals the button-pressed event to the firmware. After completing its program, the microcontroller asserts its output P1.1 low to turn off Q_2 and, consequently, Q_1, removing power from the system until the user presses S_1 and restarts the process.

When selecting components, ensure that Q_1's gate-source breakdown voltage exceeds the highest possible input voltage; otherwise, use a zener diode to limit Q_1's applied gate-source voltage. You can omit Q_1 if voltage regulator IC_1 includes an on/off-control pin. To replace Q_1 with a different power-switching device, such as an NPN bipolar transistor or a relay, specify Q_2 to provide the control current that the switching device requires. To further reduce the circuit's component count, replace diodes D_1

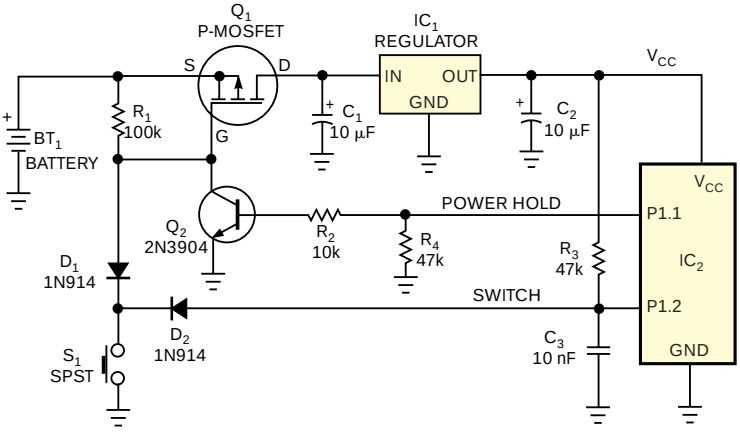

Figure 1 One switch can provide power control and user inputs to a microcontroller-based system.

and D_2 with a suitable common-cathode dual-diode array, such as the BAV70. Omit resistor R_3 if IC_2 includes built-in pullup resistors, as do many modern microcontrollers. EDN

REFERENCE

1 Hageman, Steve, "Single switch serves dual duty in small, microcontroller-based system," *EDN*, March 30, 2006, pg 96, www.edn.com/article/CA6317068.

Electronic circuit replaces mechanical push-push switch

Donald Schelle, Maxim Integrated Products Inc, Sunnyvale, CA

Mechanical push-pushbutton switches (also known as alternate-action or push-on/push-off switches) can be bulky and expensive. As an alternative, an electronic version uses a cheaper, NO (normally open), momentary-on switch (Figure 1). A supervisory microprocessor, IC_1, serves as a combination switch debouncer and intelligent controller. Applying power holds IC_1's $\overline{LBO}$ output (Pin 4) low, which in turn resets flip-flop IC_2's output to a logic-low state (off) (Figure 2). Pressing the NO momentary-contact switch, S_1, evokes a pulse from the $\overline{RESET}$ output (IC_1, Pin 5), which triggers IC_2's CK input (Pin 1) and toggles IC_2's output to a logic-high state (on). Pressing the switch a second time triggers another $\overline{RESET}$ pulse that toggles flip-flop IC_2's output to a logic-low state (off).

You can add an optional watchdog timer, IC_3, to reset IC_2's output to the logic-low state after a user-selectable interval as long as 60 sec. You can select shorter reset times using IC_3's programming pins: SET0, SET1, and SET2. The entire circuit costs about $2 (1000) and occupies a pc-board area that's no larger than its mechanical counterpart. EDN

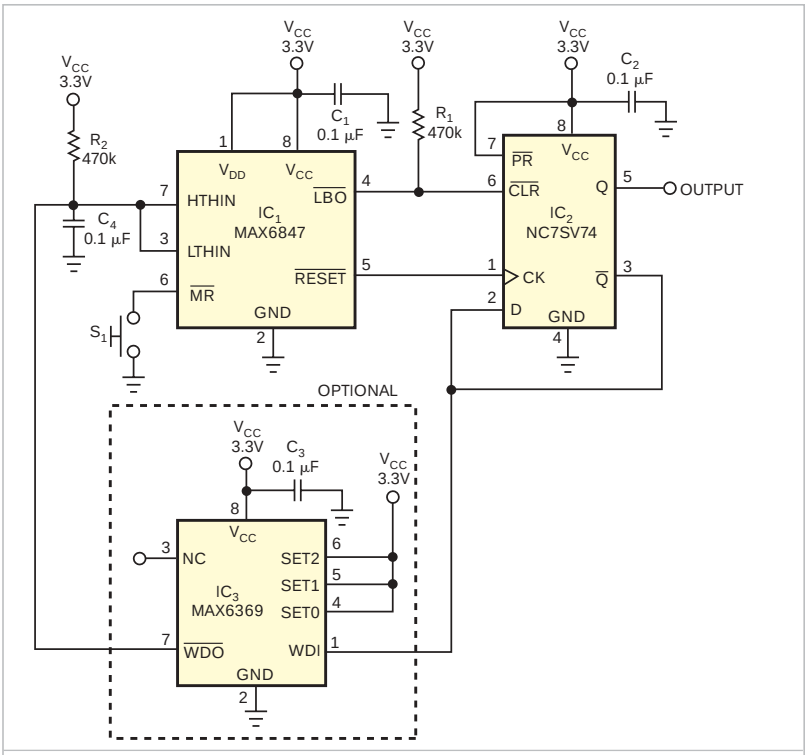

Figure 1 This simple electronic circuit uses a momentary-contact pushbutton switch, S_1, to replace a more expensive mechanical push-on/push-off switch.

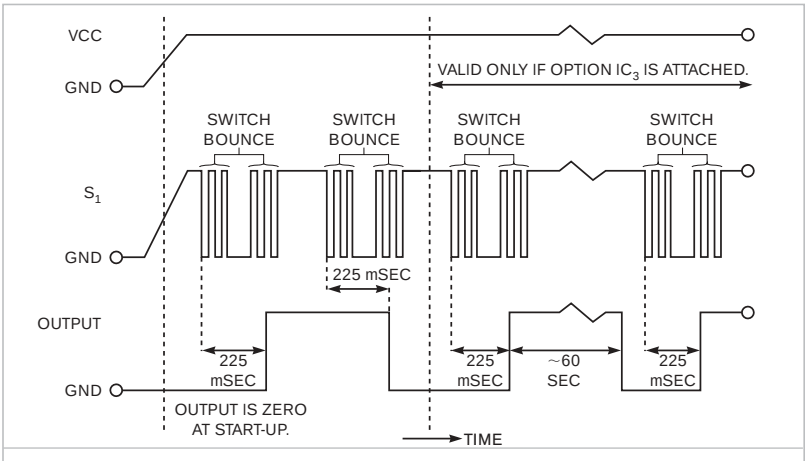

Figure 2 Repeatedly pressing the circuit's momentary-contact switch toggles the circuit's output on and off. After a preselected interval, an optional watchdog timer resets the output to the logic-low state.

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Soft limiter for oscillator circuits uses emitter-degenerated differential pair

Herminio Martínez and Encarna Garcia,
Technical University of Catalonia, Barcelona, Spain

Most oscillator circuits include a nonlinear amplitude control that sustains oscillations at a desired amplitude with minimum output distortion. One approach uses the output sinusoid's amplitude to control a circuit element's resistance, such as that of a JFET operating in its triode-characteristics region. Another control method uses a limiter circuit that allows oscillations to grow until their amplitude reaches the limiter's threshold level. When the limiter operates, the output's amplitude remains constant. To minimize nonlinear distortion and output clipping, the limiter should exhibit a "soft" characteristic.

Based on a waveform shaper that imposes a soft limitation or saturation characteristic, the circuit in **Figure 1** comprises a simple RC (resistor-capacitor)-ladder phase-shift oscillator and an amplitude-control limiter circuit. R_1, R_2, and R_3 have values of 10 kΩ each, and C_1, C_2, and C_3 have values of 1 nF each. The following **equation** defines output voltage V_{OUT}'s frequency, f_O.

$$f_O = \frac{\sqrt{6}}{2\pi RC} = \frac{\sqrt{6}}{2\times\pi\times 10\ \text{k}\Omega\times 1\ \text{nF}} \approx 39\ \text{kHz}.$$

The inverting-amplifier block in **Figure 1** comprises transistors Q_1 and Q_2, a differential pair that presents a nonlinear-transfer characteristic, plus an IVC (current-to-voltage converter) based on operational amplifier IC_1. For oscillation to occur, the inverting amplifier's gain magnitude must exceed 29. Selection of appropriate values of bias current, I_{EE}; the transistor pair's emitter-degeneration resistances, R_{E1} and R_{E2}; and R_{E3} produces the amplifier's nonlinear-transfer characteristic, V_{OUT} versus V_{IN} (**Figure 2**).

A small input voltage produces a nearly linear-amplifier-transfer characteristic. However, large values of input voltage drive Q_1 and Q_2 into their nonlinear region, reducing the amplifier's gain and introducing a gradual bend in the transfer characteristic. A current mirror comprising Q_3 and Q_4 converts the shaping circuit's output

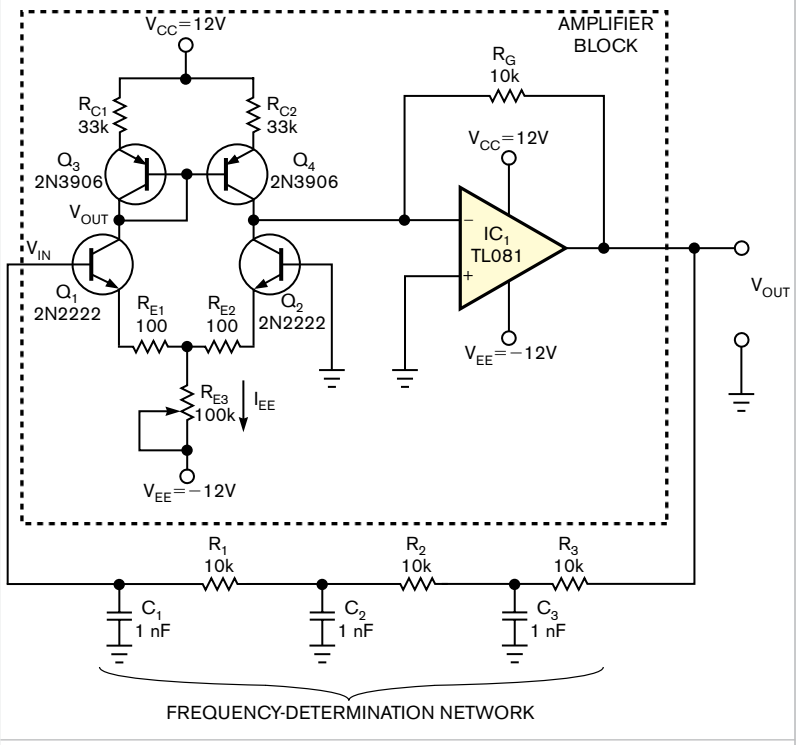

Figure 1 A phase-shift RC-oscillator circuit uses an emitter-coupled amplitude limiter.

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to a single-ended current, which operational amplifier IC_1 converts to an output voltage. In the prototype circuit, calibration trimmer R_{E3} has a value of approximately 33 kΩ. **Figure 3** shows the oscillator's output voltage for the component values in **Figure 1**, and **Figure 4** shows the sinusoidal output's spectral purity.

The nonlinear amplifier's wave-shaping action occurs independently of frequency, and this circuit offers convenience for use with variable-frequency oscillators. Note that IC_1's gain-bandwidth product limits the circuit's performance. To use the limiter portion of the circuit with a noninverting amplifier, such as a Wien-bridge oscillator, apply the signal input voltage to Q_2's base, and ground Q_1's base. EDN

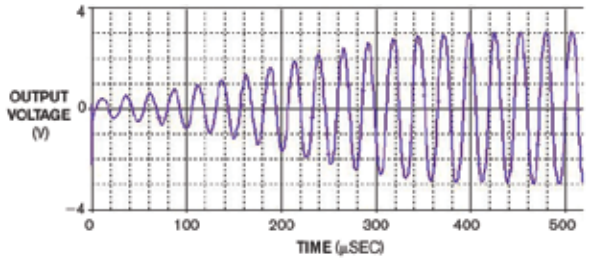

Figure 3 For the component values in Figure 1, the oscillator's output voltage reaches full amplitude in approximately 400 µsec, or 15 cycles after start-up.

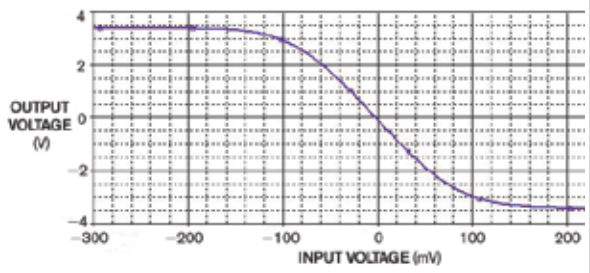

Figure 2 The transfer-characteristic output voltage versus input voltage for the nonlinear amplifier shows a gradual onset of limiting at approximately 100-mV input.

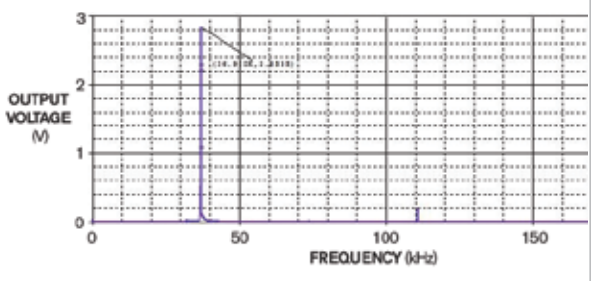

Figure 4 The oscillator's output spectrum shows only a slight amount of third-harmonic output.

Feedback circuit enhances phototransistor's linear operation

JC Ferrer and A Garrigós, University Miguel Hernández, Elche, Spain

A designer who uses a phototransistor to convert a modulated optical signal to an electrical signal frequently encounters problems when high-intensity background light saturates the phototransistor. When its base terminal floats, a phototransistor's collector-to-emitter voltage depends only on the photocurrent generated by the superposition of the signal and background light. The phototransistor's gain and its active-region range depend on R_1's resistance. For higher values of R_1, the circuit's gain increases, but the phototransistor saturates more quickly. In **Figure 1**, without background illumination, the transistor operates in its linear region at bias point ϕ_2, and Q_1's collector voltage varies linearly

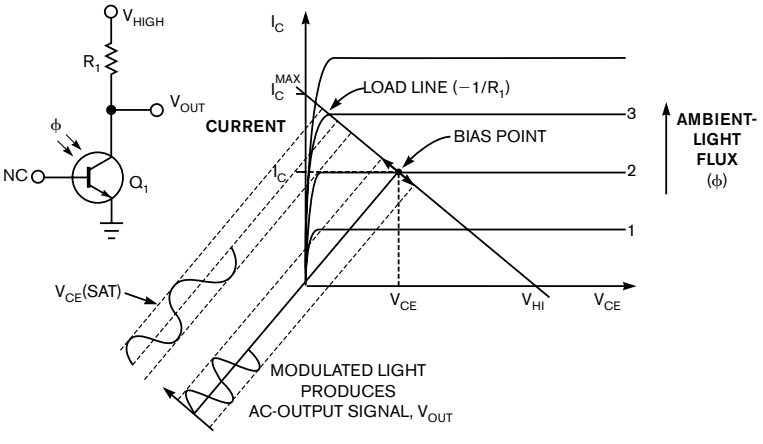

Figure 1 Varying levels of ambient-light flux affect the bias point of a basic phototransistor circuit. Higher levels force the bias point closer to saturation and compress the desired signal, V_{OUT}.

around V_{CE}. Its output, V_{OUT}, faithfully reproduces ampltude fluctuations in the modulated optical signal. Applying extraneous steady-state background illumination shifts the circuit's operating point to bias point ϕ_3, and the output voltage compresses and distorts.

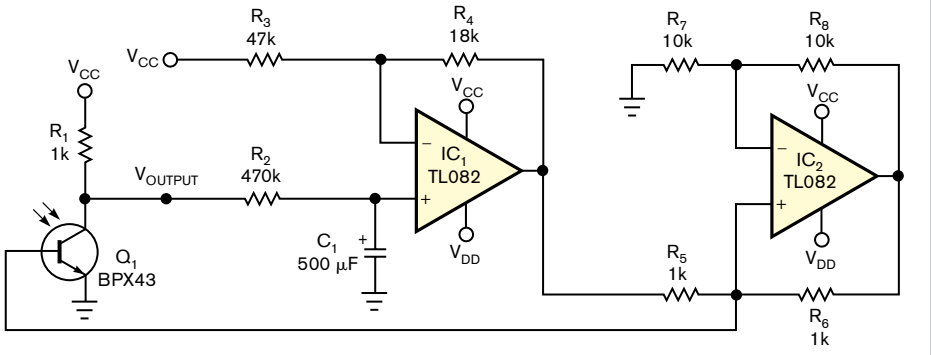

Figure 2 A feedback circuit consisting of a single-pole lowpass active filter and a Howland source diverts current from the phototransistor's base to avoid saturation at excessive background-light levels.

Unlike photodiodes and photovoltaic cells that have only two leads, a phototransistor's base connection allows a feedback circuit to control the device's bias point. Diverting current from the base terminal reduces collector current. In **Figure 2**, phototransistor Q_1 detects an optical signal plus background light that illuminates its base region. A lowpass active filter samples the collector voltage generated by the background light, and a Howland current source alters the circuit's bias point by draining current from the phototransistor's reverse-biased collector-base junction.

In general, extraneous background illumination fluctuates more slowly than the desired signal. For simplicity, this design uses a first-order lowpass filter, C_1 and R_2, with a cutoff frequency below the signal frequency to sample Q_1's collector voltage. Applying a reference voltage—V_{CC}, in this example—to R_3 sets the filter circuit's dc operating point midway between the phototransistor's cutoff and saturation voltages. The lowpass filter's output drives a Howland current source to produce a current proportional to the filter's output. As background illumination increases, Q_1's collector voltage decreases. The current source's output subtracts from Q_1's base current, which in turn raises Q_1's collector voltage to avoid saturation.

The ratio of R_4 to R_3 establishes the active lowpass filter's gain according to the equation $A_V=1+(R_4/R_3)$, and R_5 sets the current source's transconductance: $G_M=1/R_5$. Altering these resistors affects the amount of current drained from the phototransistor's base and the circuit's operating point. The phototransistor has much lower capacitance than the filter, ensuring that the circuit in **Figure 2** cannot oscillate. However, replacing the first-order lowpass filter with a second-order lowpass filter requires careful selection of the capacitors' values to avoid oscillation.

Illuminating the phototransistor with a 100W incandescent light bulb provides high-intensity-light background lighting plus a rapidly changing signal due to the applied ac-line

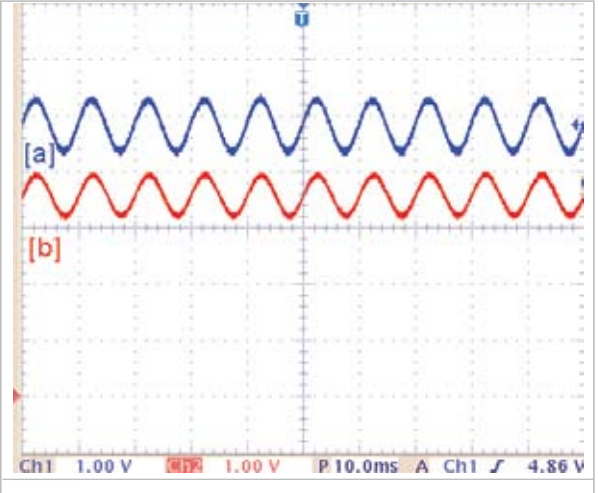

Figure 3 A 100W light bulb at a 40-cm distance illuminates a collector-emitter voltage of a phototransistor with a feedback circuit (a) and with no feedback (b). Both bias points remain in the linear region.

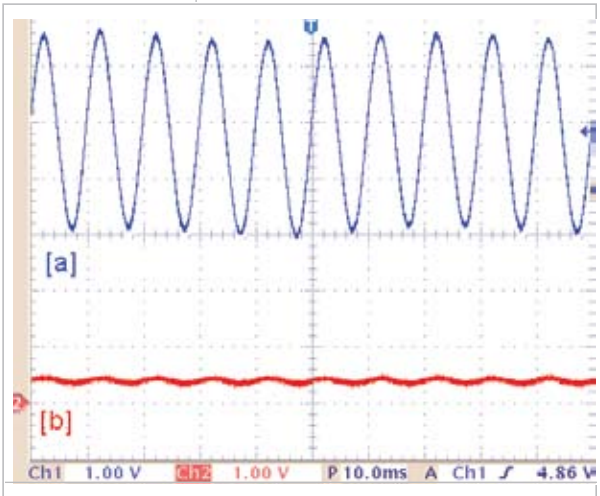

Figure 4 A 100W light bulb at a 20-cm distance illuminates the collector-emitter voltage of a phototransistor with a feedback circuit (a) and with no feedback (b). Saturation of the circuit with no feedback prevents signal detection.

voltage. **Figure 3** shows Q_1's collector-to-emitter voltage with the light bulb 40 cm from the phototransistor with the feedback circuit active (**Figure 3a**) and for the circuit with the phototransistor's base floating (**Figure 3b**). The responses appear similar because the phototransistor doesn't saturate at the applied light intensity.

Repositioning the light bulb at 20 cm from the phototransistor increases the background-light level and drives the phototransistor closer to saturation. When you apply feedback, the phototransistor delivers a higher amplitude signal, although its bias point remains almost unchanged (**Figure 4a**). The average dc-voltage level at Q_1's collector remains almost the same as at the lower light level (**Figure 3a**). However, with no feedback applied, the phototransistor's bias point moves close to saturation, and the ac-modulated light variations are barely detectable (**Figure 4b**).EDN

Three-phase sinusoidal-waveform generator uses PLD

Eduardo Perez-Lobato, University of Antofagasta, Antofagasta, Chile

Using the circuit in this Design Idea, you can develop and implement a lightweight, noiseless, inexpensive, three-phase, 60-Hz sinusoidal-waveform voltage generator. Although targeting use as a circuit for testing power controllers, it can serve other applications that require three sine waves with a 120° relative phase difference. A 22V10 PLD (programmable-logic device) at IC_1 generates three three-phase, 60-Hz, square-wave voltages. Internal register IC_1 and Q_0, Q_1, and Q_2 bits set the

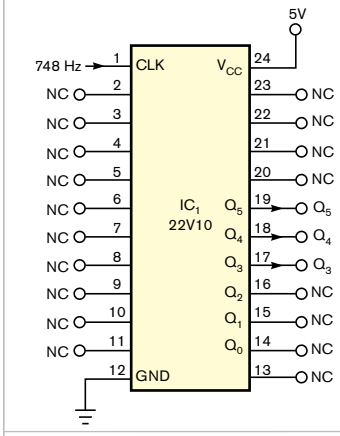

Figure 1 An external 748-Hz clock source drives this PLD-based, three-phase sine-wave generator.

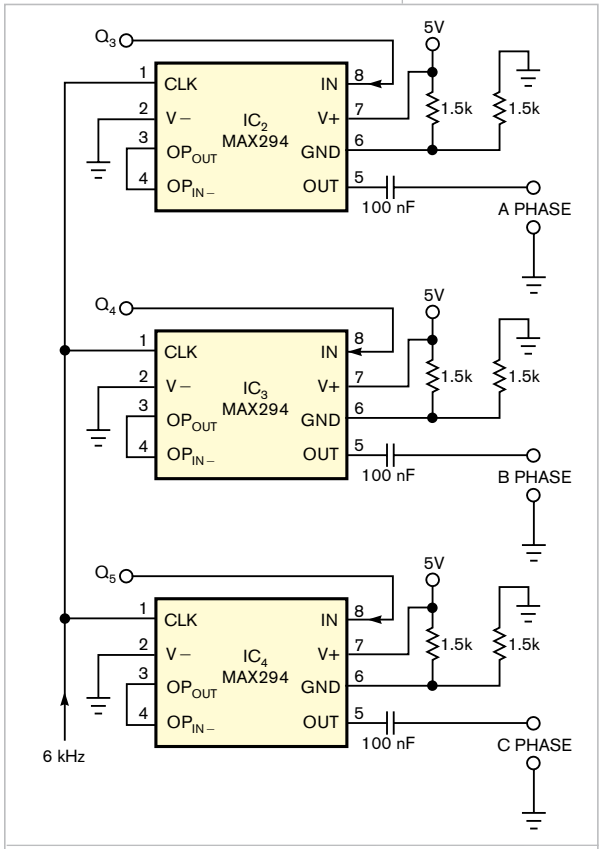

Figure 2 Switched-capacitor filters remove all but the sinusoidal fundamental signal from the PLD's three-phase square-wave outputs.

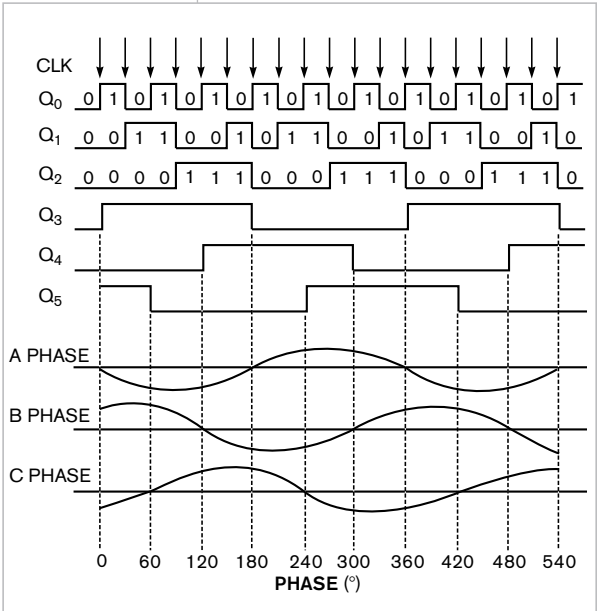

Figure 3 The timing diagram shows the relationship between the clock and the three-phase outputs.

Q_3 bit to lead the Q_4 bit by 120° and set the Q_5 bit to lag behind the Q_3 bit by 240° (**Figure 1**). Setting IC_1's clock frequency to 748 Hz produces 60-Hz outputs at Q_3, Q_4, and Q_5.

IC_1's three square-wave output voltages—Q_3, Q_4, and Q_5—drive IC_2, IC_3, and IC_4, three Maxim (www.maxim-ic.com) MAX294 eighth-order, low-pass, switched-capacitor filters to produce three 2V sinusoidal waveforms (**Figure 2**). When you connect IC_5, a common 555 timer as an astable oscillator, it produces a 6-kHz, TTL-level source that clocks all three filters at 100 times the desired 60-Hz output frequency. A 100-nF dc-blocking capacitor at each filter's output ensures that the three-phase outputs swing from +2 to −2V with respect to ground. Note that each filter inverts its output and introduces a 180° phase shift with respect to its input square wave.

Figure 3 depicts the phase relationships among IC_1's outputs and yields Boolean equations (**Table 1**). The equations translate into set/reset signals that produce 64 logic states when you apply them to a 6-bit sequencer block in IC_1. Outputs Q_5, Q_4, and Q_3 represent the three most-significant bits, and Q_2, Q_1, and Q_0 represent the three least-significant bits. After translation, an emulated Basic program (**Listing 1**), which you can download from www.edn.com/061012di1, produces fuse-programming code for IC_1's sequencer and logic states. Although only 16 logic states define the sequencer's functions, its remaining 48 states also require definition to avoid anomalous operation. EDN

TABLE 1 BOOLEAN EQUATIONS

$SET\_Q_0=\overline{Q_0}$	$RESET\_Q_0=Q_0$
$SET\_Q_1=\overline{Q_1}\times Q_0$	$RESET\_Q_1=\overline{Q_2}\times Q_1\times\overline{Q_0}+Q_2\times Q_1\times\overline{Q_0}$
$SET\_Q_2=\overline{Q_2}\times Q_1\times\overline{Q_0}$	$RESET\_Q_2=Q_2\times Q_1\times\overline{Q_0}$
$SET\_Q_3=\overline{Q_3}\times Q_2\times Q_1\times\overline{Q_0}$	$RESET\_Q_3=Q_3\times Q_2\times Q_1\times\overline{Q_0}$
$SET\_Q_4=\overline{Q_4}\times Q_2\times\overline{Q_1}\times\overline{Q_0}$	$RESET\_Q_4=Q_4\times Q_2\times\overline{Q_1}\times\overline{Q_0}$
$SET\_Q_5=\overline{Q_5}\times\overline{Q_2}\times Q_1\times\overline{Q_0}$	$RESET\_Q_5=Q_5\times\overline{Q_2}\times Q_1\times\overline{Q_0}$

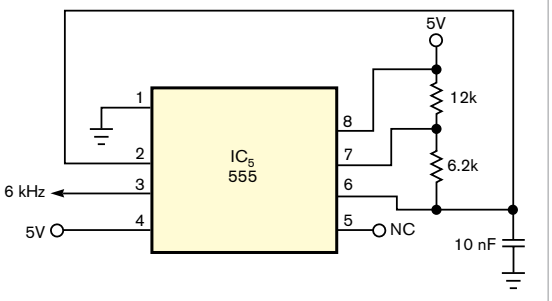

Figure 4 A garden-variety 555 timer IC provides a 6-kHz clock for the switched-capacitor filters.

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PSoC microcontroller and LVDT measure position

Sigurd Peterson, Sig3 Consulting, Aloha, OR

Connecting an LVDT (linear-variable-differential transformer) to a microcontroller can prove challenging because an LVDT requires ac-input excitation and measurement of ac outputs to determine its movable core's position (**Reference 1**). Most microcontrollers lack dedicated ac-signal-generation and -processing capabilities and thus require external circuitry to generate harmonic-free, amplitude- and frequency-stable sine-wave signals. Conversion of an LVDT's output signals' amplitude and phase into a form compatible with a microcontroller's internal ADC usually requires additional external circuitry.

In contrast with conventional microcontrollers, Cypress Semiconductor Corp's (www.cypress.com) PSoC microcontrollers include user-configurable logic and analog blocks that simplify generation and measurement of ac signals. PSoC devices have the unusual feature of being able to generate analog signals without demanding continuous CPU attention. The PSoC's flexible analog and digital blocks can drive an LVDT and measure its outputs without requiring any external circuitry. **Figure 1** shows the complete circuit of the LVDT interface, and **Figure 2** shows

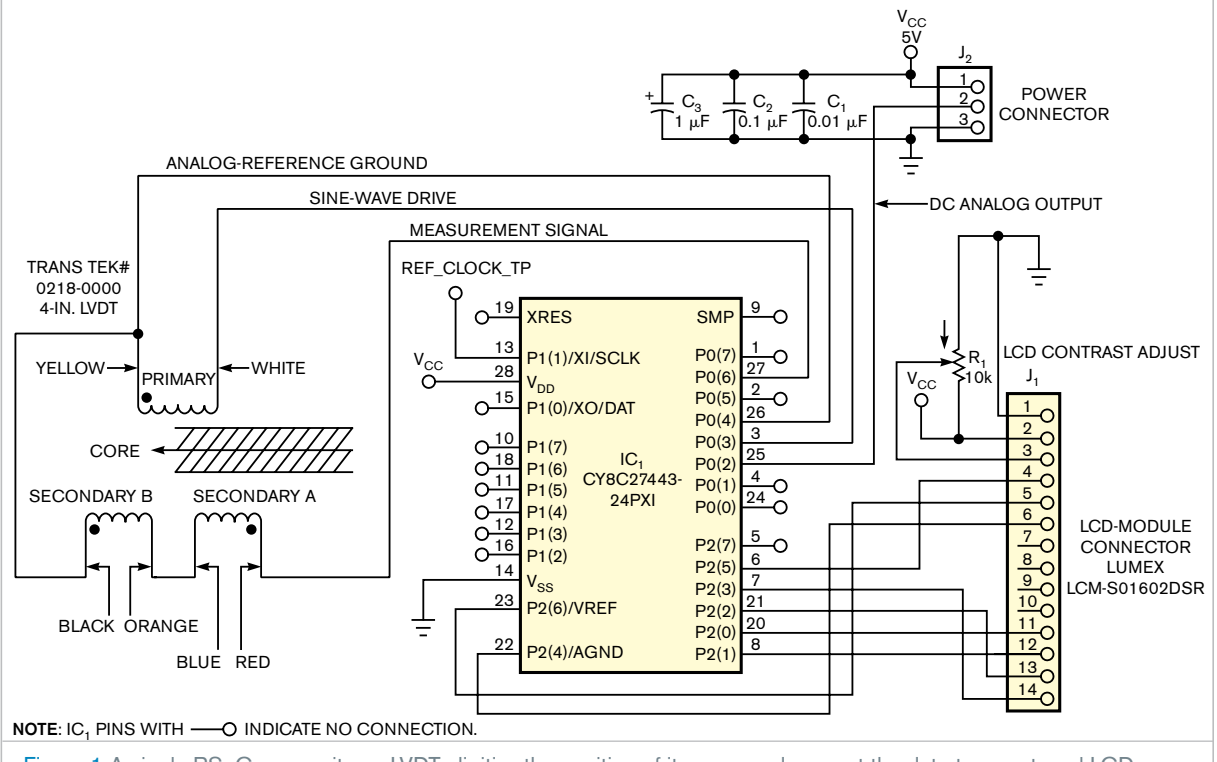

Figure 1 A single PSoC can excite an LVDT, digitize the position of its core, and present the data to an external LCD.

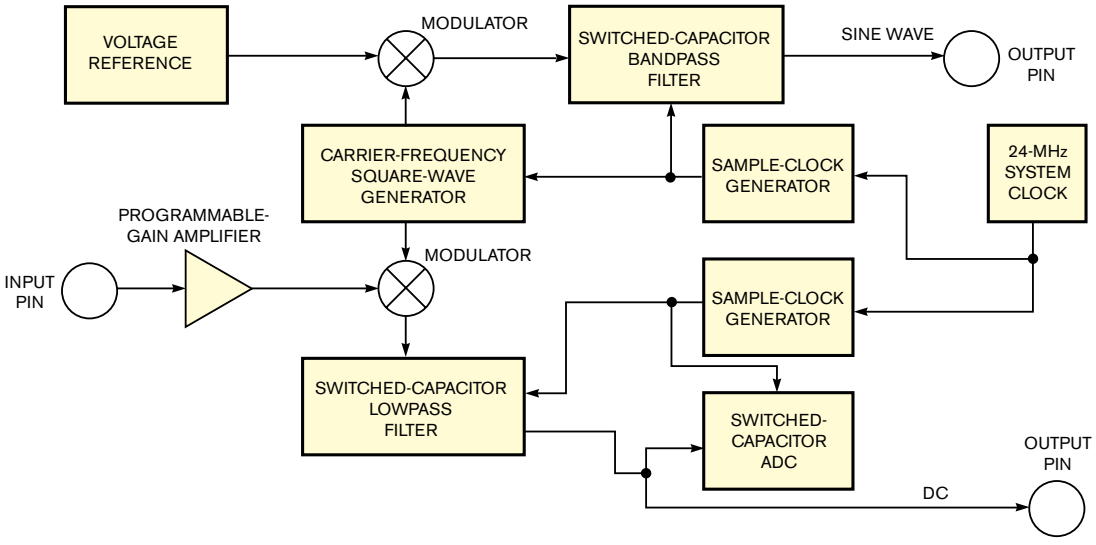

Figure 2 The LVDT-interface circuit requires many analog functions.

the PSoC microcontroller's internal circuit blocks.

The PSoC uses pairs of user-configurable switched-capacitor blocks to implement both bandpass and lowpass filters. You can create a high-quality sine wave by generating a square wave and applying it to a PSoC switched-capacitor filter through a modulator built into the first switched-capacitor block. Passing the square wave through a narrow bandpass filter centered on the square wave's fundamental frequency removes most of the harmonics.

To obtain the highest fidelity sine waveform from a PSoC switched-capacitor bandpass filter, use the highest possible oversampling rate—a factor of approximately 33—or 33 steps per sine-wave cycle. The resultant sine wave is smooth enough to drive an LVDT, which attenuates any residual higher order harmonics. Scaling the PSoC's internal voltage reference with a programmable-gain amplifier provides coarse control over the square wave's amplitude before it undergoes filtering. To compensate for the waveform's dc-offset voltage, an amplifier buffers the 2.6V internal analog-ground reference and drives an output pin that serves as the LVDT's analog-ground return.

The LVDT's output consists of a variable-amplitude sine-wave voltage whose phase angle with respect to the sine-wave excitation voltage undergoes a significant and variable shift that sometimes exceeds 180°. A signal from the LVDT drives one of the PSoC's programmable-gain amplifiers, whose output feeds a switched-capacitor lowpass filter followed by a modulator for synchronous rectification. The rectified signal drives an output pin and one of the PSoC's switched-capacitor ADCs.

Applying the LVDT's output to a synchronous rectifier followed by a lowpass filter produces a dc voltage that can feed an ADC or directly drive an analog feedback-control system. In a PSoC microcontroller, a lowpass switched-capacitor filter connected to an ADC requires that the same sample clock drive both circuits, resulting in a conversion rate for the PSoC's 11-bit delta-sigma ADC that's approximately one-half of the lowpass filter's corner frequency. Synchronous rectification produces a ripple frequency twice that of the excitation frequency and thus is easier to remove with a lowpass filter. Relocating the lowpass filter's corner frequency to one-third of the excitation frequency allows measurements of the LVDT's output to 11-bit resolution with a standard deviation of 1 LSB (least significant bit) or less.

Dividing the PSoC's 24-MHz internal system clock with logic blocks configured as counter chains generates all of the digital clock signals the switched-capacitor analog-circuit blocks require. After power application or a reset, the PSoC's CPU configures all the configured analog and digital blocks and starts their operation. From then on, the hardware excites the LVDT and measures its output at 500 samples/sec without further intervention by the CPU. With the PSoC's CPU running at 12 MHz, processing the ADC's housekeeping activities and interrupts consumes less than 3% of the CPU's resources.

Plenty of the PSoC's resources remain available for calculating the LVDT's position and for displaying the results in text format on an LCD module. Four analog blocks, five logic blocks, and many I/O pins remain available to support a more demanding application. **Figure 3** (next page) shows configurable blocks that are available for adding features. EDN

REFERENCE

1 "Linear variable differential transformer," *Wikipedia*, http://en.wikipedia.org/wiki/Lvdt.

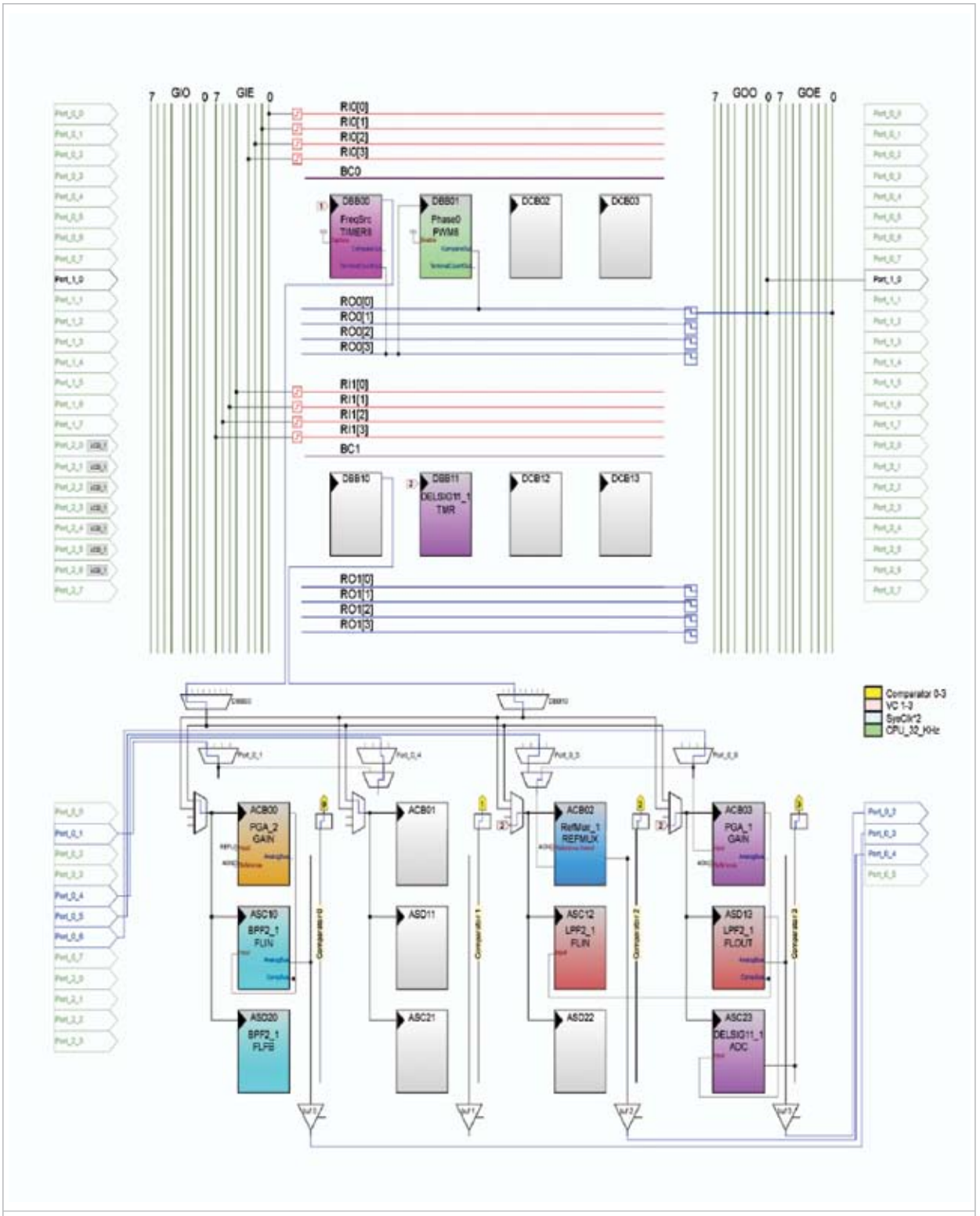

Figure 3 You can use the unlabeled circuit blocks for expansion.

Single microcontroller pin senses ambient light, controls illumination

Loren Passmore, Berkeley, CA

As in a previous Design Idea (**Reference 1**), this design uses an LED as a transducer to measure the ambient-light level and to provide illumination. This Design Idea uses the same principle as its predecessor but consists of only one LED, two resistors, one IC, and one 0.1-µF bypass capacitor. This circuit for providing ambient-light feedback requires no additional components. Despite requiring only a few components, the circuit in **Figure 1** offers considerable flexibility because the microprocessor's software controls the LED's brightness and its relationship to ambient-light levels. For night-light applications, one mode turns on the LED when ambient light decreases. Conversely, for power-saving regulation of a portable device's LCD backlight, a second mode turns on the LED when the ambient-light level increases.

You can download **Listing 1**, sample code for this Design Idea, at www.edn.com/061026di1. The code provides 64 levels of PWM (pulse-width-modulated) intensity control over the LED's brightness in either mode. In operation, one of the microprocessor's multifunction pins drives the LED with a PWM waveform for several hundred milliseconds. After the waveform's final cycle, the software switches the microprocessor's pin to input mode and connects the LED to the microprocessor's internal 16-bit sigma-delta ADC. Ambient light illuminates the LED, producing voltage, which the ADC measures, and the microprocessor computes the PWM waveform's parameters for the next series of illumination cycles. The cycle rate's high repetition frequency eliminates any discernible flickering of the LED.

In the **listing**, when the software and ambient-light level specify that the LED should turn off for an extended interval, the CPU goes into a low-power state for 250 msec. During its sleep mode and for a few hundred microseconds while performing ADC conversions, the circuit draws only about 20 µA and thus suits itself well to battery-powered-system applications.

At start-up, the microprocessor stores an initial voltage level, which the LED produces, and uses this value to scale the PWM levels. Shading the LED or moving the circuit into a darker area immediately increases the LED's brightness, which the **listing**'s 64 PWM levels control in small steps. The MSP430F2013's ADC presents input impedance of approximately 200 kΩ. When driving this impedance, an LED occupying a small, 0805, surface-mount footprint generates only a few 10s of millivolts. However, the MSP430F2013's 16-bit ADC resolves the LED's voltage with sufficient resolution to ensure good performance under normal room-lighting levels.

In addition, the MSP430F2013 includes a four-level PGA (programmable-gain amplifier), offering gains of one, four, eight, and 16 to further amplify the LED's minuscule output voltage. The circuit also exploits the microprocessor's onboard low-frequency clock oscillator, which allows low-powered operation without an external crystal. The resultant circuit includes only six components, including a battery. Note: The code can execute on Texas Instruments' (www.ti.com) eZ430 demonstration board without hardware modifications because the board includes an LED connected to port P1.0. EDN

REFERENCE

1 Myers, Howard, "Stealth-mode LED controls itself," *EDN*, May 25, 2006, pg 98, www.edn.com/article/CA6335303.

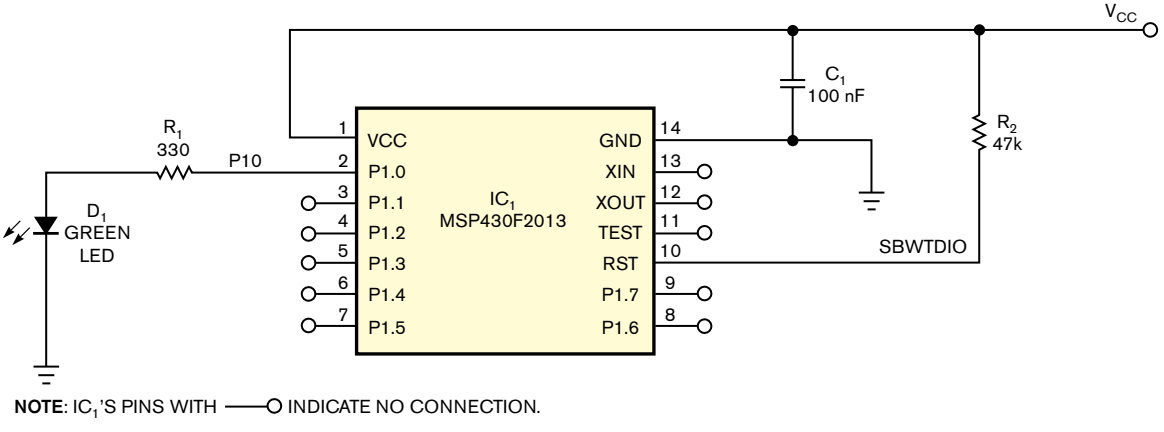

Figure 1 An LED, a microprocessor, two resistors, and one capacitor constitute the entire circuit.

Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

Editor's note: *EDN* originally ran this Design Idea in its June 22, 2006, issue. However, due to a number of schematic and textual errors, we have decided to run a corrected, up-to-date version here. We apologize for the errors and hope this version clears up any and all confusion.

Examine a traditional Hartley oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance required for a given frequency, finding the coupling coefficient, k, poses technical difficulties and may require experimental optimization, also referred to as the "cut-and-try" method. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

Figure 1 shows the Hartley oscillator's equivalent tuned circuit and component values for an 18-MHz oscillator. The mutual inductance is $L_M=k\sqrt{L_1\times L_2}$. For the equivalent circuit, the equations are: $L_A=-L_M$, $L_B=L_2-L_A=L_2+L_M$, and $L_C=L_1-L_A=L_1+L_M$. The rest of the equations for the equivalent circuit are:

$$C_A=-\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O=\frac{1}{2\pi\sqrt{(L_B+L_C)C}},$$

and

$$C_A=\frac{1}{(2\pi f_O)^2 k\sqrt{L_1\times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, L_A. However, for frequencies near the resonant frequency f_0, you can replace the negative inductor with a capacitor as (**Figure 1c**), where C_A replaces L_A. Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

Figure 2 illustrates an oscillator and output buffer using the equivalent circuit. When constructed, the circuit generally performed as expected from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design.

The oscillator's tank circuit consists of L_B, L_C, C_4, and C_5, plus the capacitance provided by the voltage divider C_6, C_7, and C_8—approximately 6 pF, including Q_1's and Q_2's input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors L_B and L_C consist of air-core coils mounted with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should consist of windings on dielectric cores or on toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application.

The information in **Reference 1** provided basic designs for both inductors, and adjusting the spacing of their turns tuned the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require some adjustment of the inductors.

The capacitive voltage divider, C_6, C_7, and C_8, applies the proper signal levels to Q_1 and Q_2. Because the divider's effective capacitance as "seen" by the tank circuit amounts to only 6 pF, you can replace the remaining 60 pF consisting of C_4 and C_5 with a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage consisting of Q_3 and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor C_3 bootstraps Q_1's Gate 2 to its source, which provides additional gain and reduces Q_1's Gate 1 input capacitance below its already-low value of approximately 2.1 pF (**Reference 2**). An 8.3-µH inductor, L_2, of less than 2Ω dc resistance connects to Q_1's source and presents a relatively high impedance at 18 MHz and provides a dc path from Q_1's source to ground through R_3. At 18 MHz, L_2 has an impedance that consists of an inductive reactance of about 940Ω

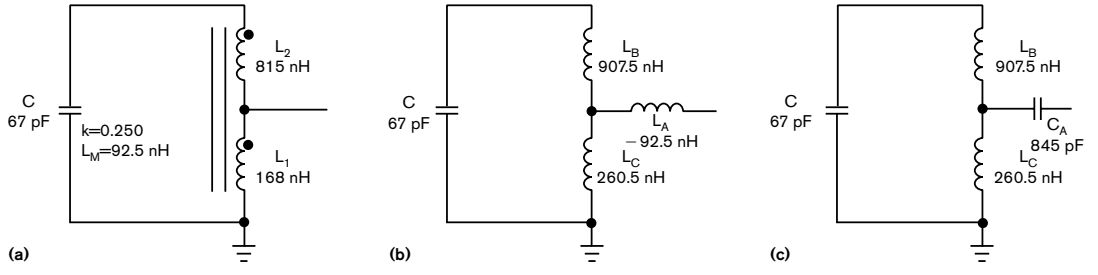

Figure 1 A traditional Hartley oscillator's resonant circuit consists of a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).

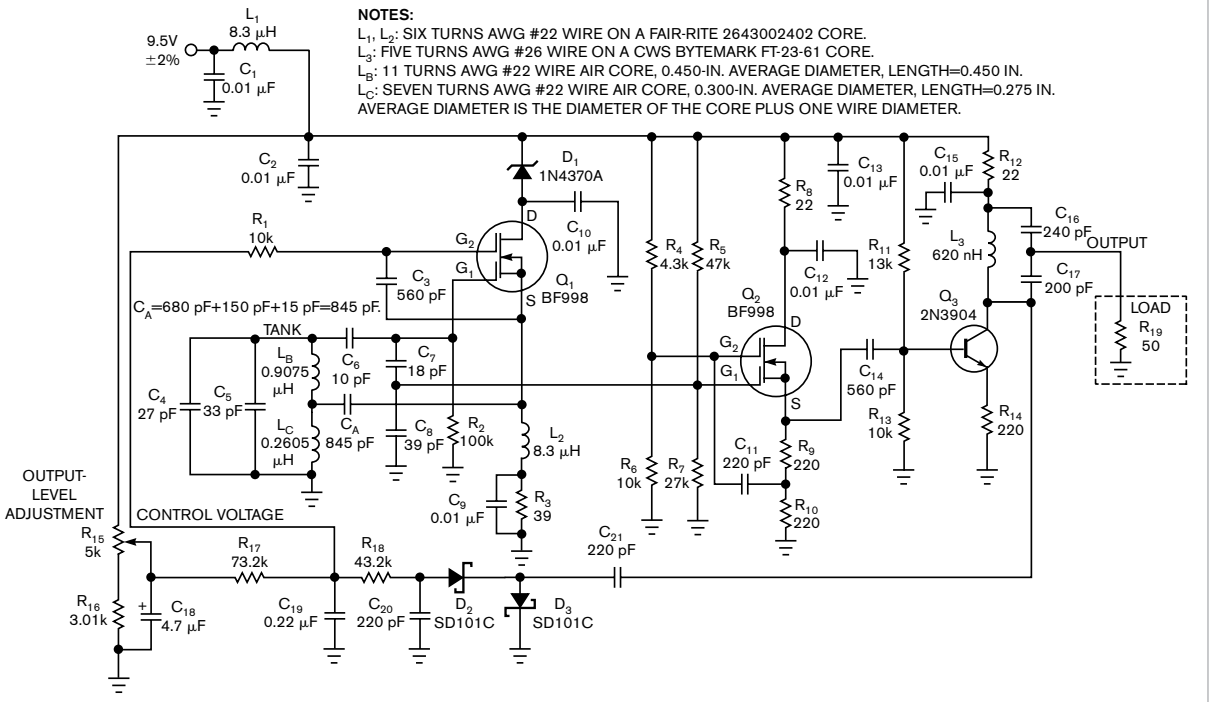

Figure 2 This buffered-output, 18-MHz oscillator features a resonant circuit that doesn't rely on mutual coupling for operation.

in parallel with a resistance of about 3.5 kΩ, which results in a very-low-Q choke. Provided that its inductance and reactance approximate L_2's original values, you can substitute a physically smaller inductor for L_2. Inductor L_1's properties are less critical, but it should present a low Q of 4 to 6 and a dc resistance of approximately 5Ω or less. You can use a standard-value choke for L_1 if it meets these requirements.

Source follower Q_2 drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at the collector of Q_3. Bootstrapping Q_2's Gate 2 by one-half of the stage's output voltage increases the source follower's gain and dynamic range and reduces its input capacitance.

You can use potentiometer R_{15} to adjust the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. At a constant room temperature of about 23°C, the frequency remains stable, and the circuitry that controls output level remains stable even with no load on the output. For a fixed-frequency application, the output circuit's loaded Q of 4 provides adequate bandwidth to eliminate retuning of the output circuit for small changes in frequency.

To set the output level to a safe maximum, connect a 50Ω load to the output, and then adjust the output to 1.5V p-p. The drain-to-source voltage applied to Q_1 will remain at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding Q_1's specified maximum 12V drain-to-source-voltage rating, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode D_1 reduces Q_1's drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit set the oscillator's gain through a control voltage applied to Q_1's Gate 2 (**Reference 3**). In this design, a simple passive circuit serves the same purpose. A portion of the signal at Q_3's collector drives a voltage doubler consisting of D_2, D_3, C_{20}, and C_{21}. Part of the negative voltage developed by the voltage doubler drives the junction of R_{18} and C_{19}, the control-voltage node, which also receives a positive voltage from variable resistor R_{15} through R_{17}, and the resultant voltage sets the output signal level. At start-up, only a positive voltage is present at Q_1's Gate 2, and Q_1's maximum gain easily starts the oscillator. When the output reaches a steady state, the control voltage reduces and maintains oscillation at the signal level determined by the output level control. **EDN**

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READERS SOLVE DESIGN PROBLEMS

LED senses and displays ambient-light intensity

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In addition to their customary roles as indicators and illuminators, modern LEDs can also serve as photovoltaic detectors (**references 1** and **2**). Simply connecting a red LED to a multimeter and illuminating the LED with a source of bright light, such as a similar red LED, produce a reading of more than 1.4V (**Figure 1**). One model for a reverse-biased LED comprises a charged capacitor that connects in parallel with a light-dependent current source (**Reference 1**). Increasing the incident light increases the current source and more rapidly discharges the equivalent capacitor to the supply voltage.

Figure 2 shows a method of using an LED as a photovoltaic detector. Connecting one of the microcontroller's outputs, Pin 2, to the LED's cathode applies reverse bias that charges the LED's internal capacitance to the supply voltage. Connecting the LED's cathode to Input Pin 3 attaches a high-impedance load to the LED. Illuminating the LED generates photocurrent. Originally charged to the supply voltage, the LED's internal capacitance discharges through the photocurrent source, and, when the voltage on the capacitor falls below the microcontroller's lower logic threshold voltage, Pin 3 senses a logic zero. Increasing the incident-light intensity more quickly discharges the capacitor, and lower light levels decrease the discharge rate. The microcontroller, an Atmel AVR ATtiny15 (www.atmel.com/dyn/products/product_card.asp?part_id=2033), measures the time for Pin 3's voltage to reach logic zero and computes the amount of ambient light incident on the LED. In addition, the microcontroller flashes the same LED at a frequency proportional to the incident light's intensity.

Figure 3 shows a 3-mm, superbright-red LED, D_1, from Everlight Electronics Co Ltd (www.everlight.com), which comes in a water-clear encapsulant as an ambient-light sensor. Having only four components, the circuit operates from any dc-power source from 3 to 5.5V. The circuit uses only three of six of the AVR ATtiny15's I/O pins, and the remaining pins are available to control or communicate with external devices. The sensor LED connects to the AVR microcontroller's port pins PB0 and PB1; another port pin, PB3, produces a square wave with a frequency proportional to the incident-light intensity. The circuit operates by

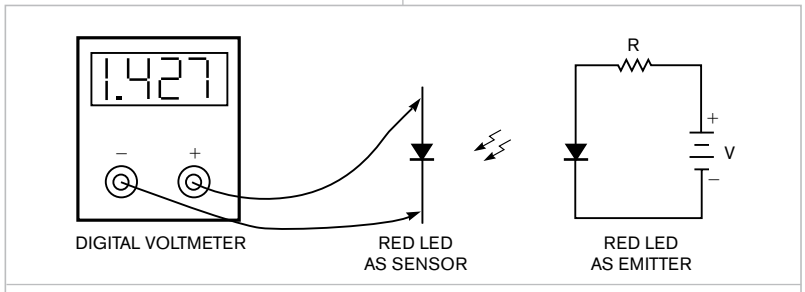

Figure 1 Two identical LEDs, closely spaced in a light-shielded housing, form a photovoltaic-characterization fixture. Choose resistor R and voltage source V to apply nominal forward current to the illuminating LED.

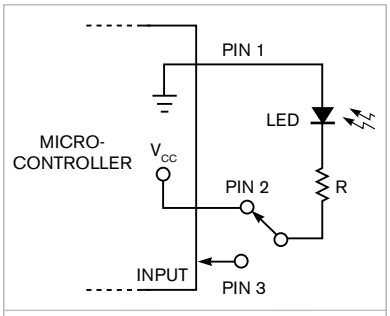

Figure 2 Connecting one of the microcontroller's outputs, Pin 2, to the LED's cathode applies reverse bias that charges the LED's internal capacitance to the supply voltage. Connecting the LED's cathode to Input Pin 3 attaches a high-impedance load to the LED. (Note that pin numbers are representative only and not actual pin numbers.)

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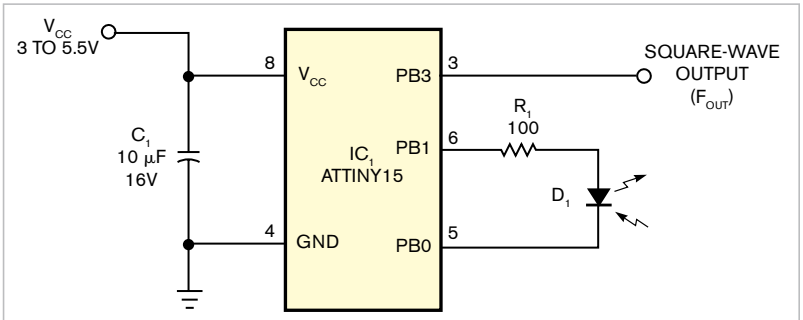

Figure 3 An LED doubles as a light-level sensor. Output PB3 delivers a square wave whose frequency increases as light intensity increases.

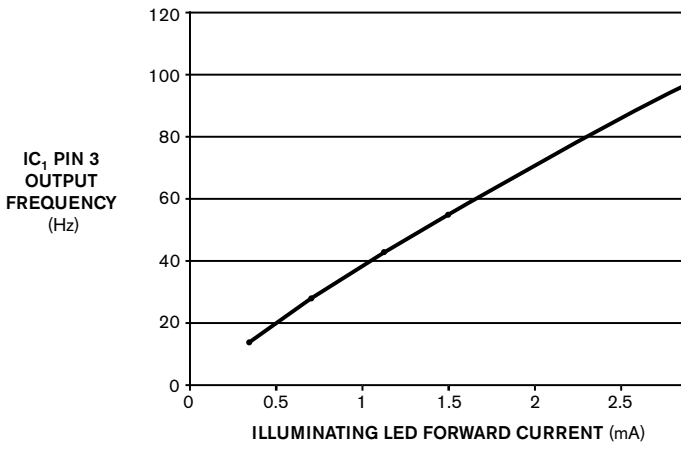

Figure 4 The frequency of the circuit's square-wave output exhibits good linearity versus light level for identical sensor and source LEDs.

first applying forward bias to the LED for a fixed interval and then applying reverse bias to the LED by changing the bit sequences you apply to PB0 and PB1. Next, the microcontroller reconfigures PB0 as an input pin. An internal timing loop measures the interval, T, for the voltage you apply to PB0 to decrease from logic one to logic zero.

Reconfiguring pins PB0 and PB1 to apply forward bias to the LED completes the cycle. Time interval T varies inversely with the amount of ambient light incident on the LED. For lower light, the LED flashes at a lower frequency, and, as the incident-light intensity increases, the LED flashes more frequently to provide a visual indication of the incident-light intensity.

For low values of forward current, an LED's light-output intensity is fairly linear (**Reference 2**). To test the circuit, couple the light output of a second and identical LED to the sensor LED, D_1, in **Figure 3**. Ensure that external light doesn't strike the sensor LED by enclosing the LEDs in a sealed tube covered with opaque black tape. Varying the illuminating LED's forward current from 0.33 to 2.8 mA produces a relatively linear sensor-flash-frequency plot (**Figure 4**).

The efficiency of an LED as a sensor depends upon its reverse-biased internal-current source and capacitance. To estimate the reverse photocurrent, connect a 1-MΩ resistor in parallel with a sensor LED and measure the voltage across the resistor while applying a constant level of illumination from an external source. Replace the 1-MΩ resistor with 500- and 100-kΩ resistors and repeat the measurements. For a representative LED under constant illumination and shielded from stray ambient light, we measured a photocurrent of approximately 25 nA for all three resistor values. For the same level of illumination applied to the sensor LED, measure the frequency generated at Pin PB3.

To calculate the LED's reverse-biased capacitance, substitute the delay-loop time, the LED's photovoltaic current, and the microcontroller's logic-one and -zero threshold voltages into the equation and solve for C, the LED's effective reverse-biased junction capacitance: (dV/dt)=(I/C), where dV is the measured logic-one voltage minus the logic-zero voltage, dt is the measured time to discharge the LED's internal capacitor, and I is the calculated value of LED's photocurrent source. The calculated values for the selected LED range from 25 to 60 pF. This range compares with the data in **references 3** and **4**, although **Reference 3** reports only the current source's values. You can download the AVR microcontroller's assembly-language firmware, **Listing 1**, from this Design Idea's online version at www.edn.com/061109di1.EDN

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AC line powers microcontroller-based fan-speed regulator

Abel Raynus, Armatron International Inc, Malden, MA

A microcontroller requires dc operating power in the 2 to 5.5V range, an amount that a battery or a secondary power source can easily supply. However, in certain situations, a microcontroller-based product must operate directly from a 120 or 220V-ac power outlet without a step-down transformer or a heat-producing, voltage-decreasing resistor. As an alternative, a polyester/polypropylene film capacitor rated for ac-line service can serve as a nondissipative reactance (**Figure 1**). Capacitor C_1, a 2-µF AVX (www.avxcorp.com) FFB16C0205K rated for 150V rms, provides a significant ac-voltage drop that reduces the voltage you apply to a diode-bridge rectifier, D_1. A flameproof metal-film resistor, R_1, limits current spikes and transient voltages induced in the ac-power line by lightning strikes and abrupt load changes. In this application, the ac current does not exceed 100 mA rms, and a 51Ω, 1W resistor provides adequate current limiting. R_2, a 5W, 160Ω Yageo (www.yageo.com) type-J resistor, and D_2, a 1N4733A zener diode, provide 5V regulated power for the microcontroller, a Freescale (www.freescale.com) C68HC908QT2.

The schematic shows a representative circuit for a microcontroller-based fan-speed regulator in which a thermistor senses air temperature and the microcontroller drives a

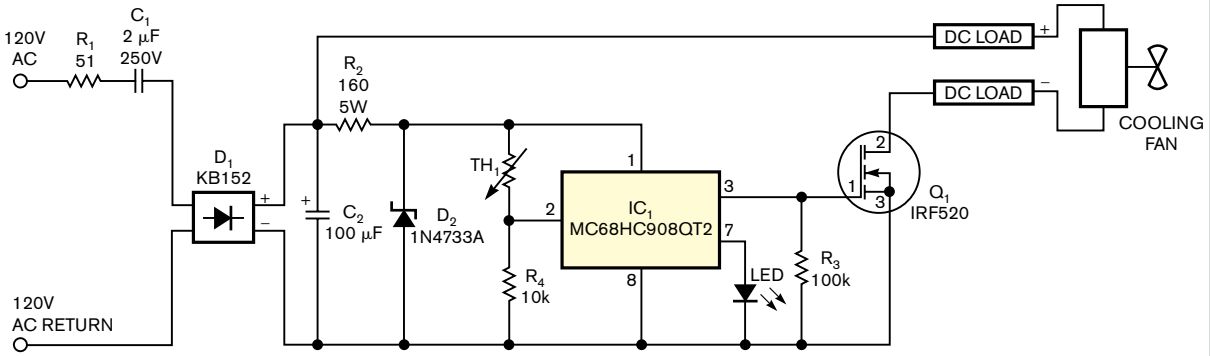

Figure 1 C_1 provides capacitive reactance, which limits ac-input current without dissipating excessive heat in this dc fan-speed controller.

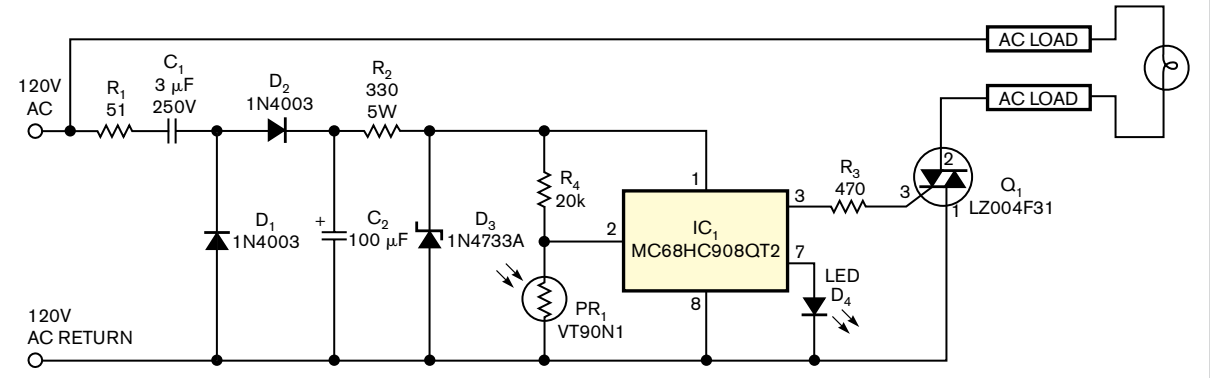

Figure 2 A two-diode rectifier and lamp-control bidirectional thyristor share a common return path to the ac line.

fan's motor. **Figure 2** illustrates a light-intensity regulator based on an inexpensive two-diode rectifier and a bidirectional-thyristor-lamp controller that share a common ground. IC_2, a Fairchild (www.fairchildsemi.com) MOC3021-M bidirectional-thyristor-driver optoisolator, separates the lamp-return path from the microcontroller's ground return (**Figure 3**). In each of the three circuits, the Kingbright (www.kingbright.com) W934GD5V0 LED indicator includes a built-in current-limiting resistor (not shown).EDN

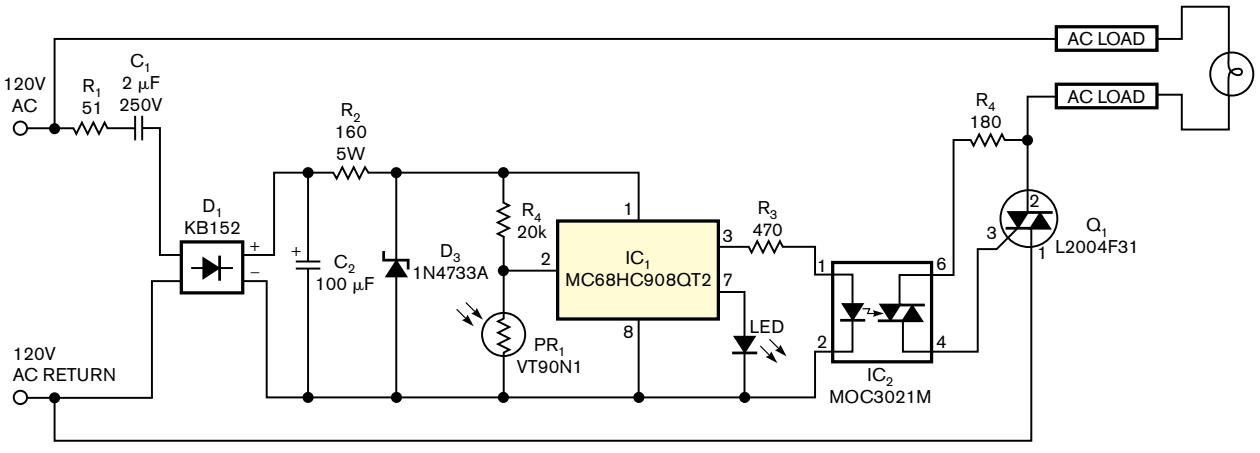

Figure 3 An optoisolator separates the bidirectional thyristor's high-current ac-line return path from the microcontroller's power supply.

Simple circuits sort out the highest voltage

Ezio Rizzo, Nova SNC, Genoa, Italy, and
Vincenzo Pronzato, Felmi SRL, Genoa, Italy

In a water-cooled power converter, analog-output sensors measure the cooling water temperature at three locations. If any of the three temperatures rises above a preset threshold, an alarm sounds and attracts the attention of the system's operator. When the alarm activates, knowing which measurement site has reached the highest temperature saves troubleshooting time and prevents system damage. The circuit in **Figure 1** delivers an analog-output voltage equal to the highest of three input voltages that drives a display for continuous temperature monitoring. LED indicators identify which of three sensors shows the highest temperature. An external adjustable-threshold comparator (not shown) monitors the analog-voltage output and activates an audible alarm.

Each of three analog input signals spans a range of 0 to 10V. Driven by the highest-voltage input, which you apply at IN_1 in this example, operational amplifier IC_{1A} functions as a voltage follower with diode D_1 in its feedback path. The op amp's open-loop gain divides the diode's forward-voltage drop to a fraction of its nominal value, producing an "ideal diode" with a voltage drop of millivolts.

THE CIRCUIT DELIVERS AN ANALOG-OUTPUT VOLTAGE EQUAL TO THE HIGHEST OF THREE INPUT VOLTAGES THAT DRIVES A DISPLAY FOR CONTINUOUS TEMPERATURE MONITORING.

Op amps IC_{1B} and IC_{1C} function as high-input-impedance inverting comparators. Each "sees" the highest input voltage on its inverting input and one of two lower input voltages, IN_2 and IN_3, on its noninverting input and delivers an output voltage near that of the negative-supply-voltage rail. Thus, only IC_{1A} delivers a positive-voltage output to MOSFET Q_1's gate, and IC_{1B} and IC_{1C} deliver negative outputs to the gates of Q_2 and Q_3. Q_1 turns on, lighting LED D_4 and drawing approximately 5 mA to develop 11V across R_3, which guarantees that Q_2 and Q_3 and their corresponding LEDs remain off. The voltage that develops across R_1 represents the largest voltage of the three inputs, and resistor R_4 and

capacitor C_1 form a lowpass filter that reduces high-frequency noise that the sensor cables pick up. Voltage follower IC_{1D} buffers the filter's output voltage. **Figure 2** (pg 136) shows the results of an LTSpice simulation featuring three sinusoidal inputs and the resultant analog output summed with a small dc-offset voltage for clarity.

The breadboarded circuit works as designed. Given its electrically noisy location near a 300-kHz, 30-kW switched-mode power converter, it uses slow-switching 1N4004 diodes to avoid malfunctions, which the rectification of stray high-frequency interference introduces. In less noisy environments, use any small-signal diode whose peak-inverse voltage exceeds at least 30V. Most varieties of operational amplifiers work well in the circuit, but for greater high-frequency immunity, use a JFET-input quad op amp, such as Texas Instruments' (www.ti.com) TL084.

Although the circuit's prototype uses red-LED indicators, LEDs of other colors work well. To change the LEDs' current to another value, change the values of R_2 and R_3, keeping approximately the same 3-to-2 ratio. For example, values of 1.8 kΩ for R_2 and 1.2 kΩ for R_3 drive the "on" LED with approximately 10 mA. If you increase the LED current, note that the resistors continuously dissipate power. For greatest reliability, choose resistors rated for twice the calculated power dissipation. EDN

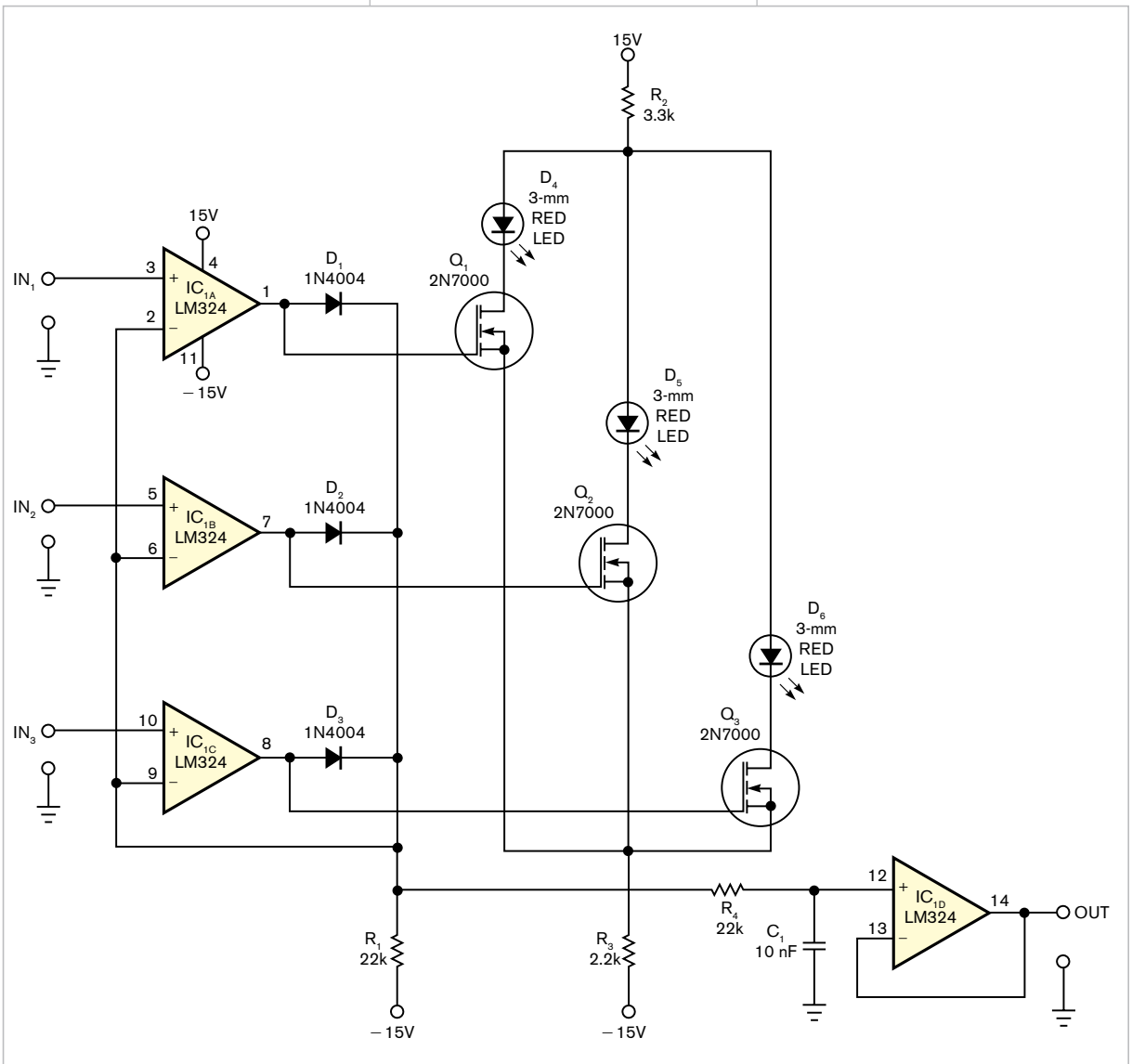

Figure 1 This circuit's output voltage tracks and indicates the highest of three input voltages and can drive an external strip-chart recorder or alarm comparator.

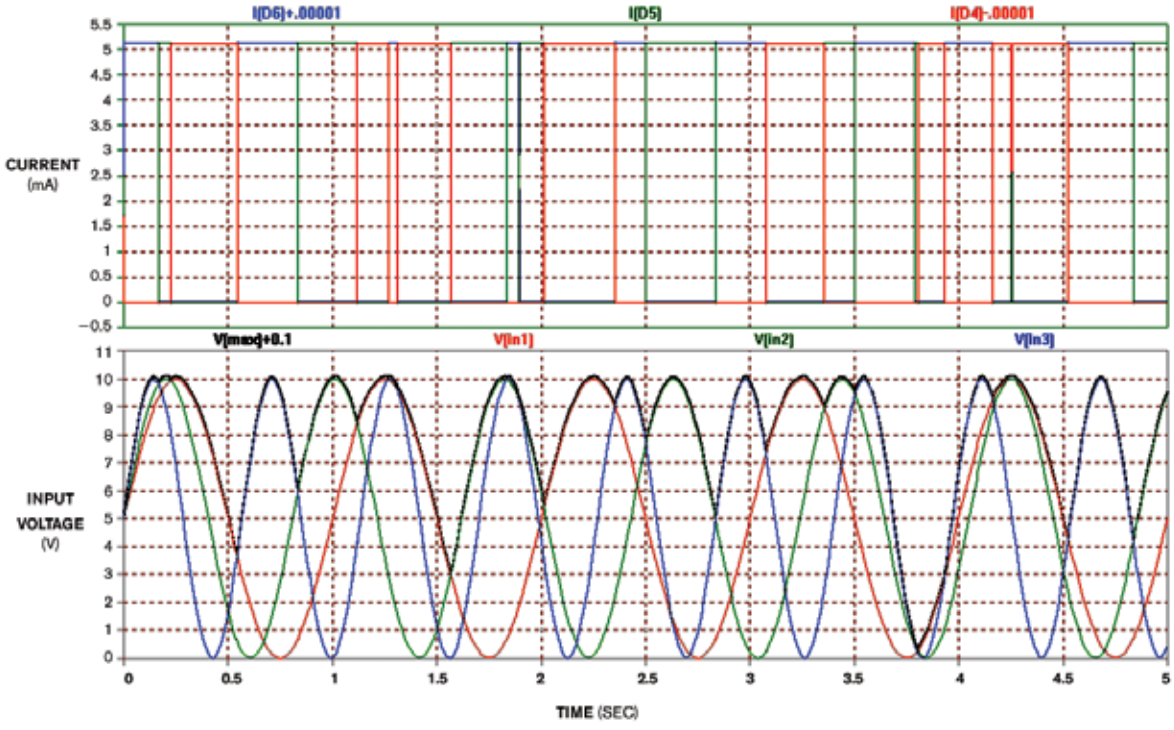

Figure 2 Three sine waves of different frequencies provide input voltages (lower traces) that evoke the greatest-of-three response in the current through R_2 (top trace, in which colored horizontal segments match the largest inputs).

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READERS SOLVE DESIGN PROBLEMS

Chopper-stabilized amplifier cascade yields 160 to 10,240 programmable gain

Jerome E Johnston, Cirrus Logic Corp, Austin, TX

Certain medical and scientific instrumentation applications require amplification and measurement of microvolt-level signals. For example, accurately measuring the output of a thermopile-based microcalorimeter demands an amplifier that achieves high gain and exhibits excellent thermal stability and low noise.

Figure 1 illustrates how combining two amplifiers yields a programmable-gain amplifier that provides selectable gains of 160 to 10,240. The circuit also offers typical offset voltage of 5 µV, offset drift of 20 nV/°C, and equivalent input-noise voltage of 9 nV$\sqrt{\text{Hz}}$ at 0.1 Hz. IC_1, a Cirrus Logic (www.cirrus.com) CS3301 low-voltage, differential-input, differential-output, chopper-stabilized programmable-gain amplifier, serves as an input-amplifier stage and drives IC_2, a higher voltage INA114 instrumentation-amplifier output stage. The CS3301 provides seven programmable gains of one to 64, and the INA114 provides a fixed gain of 160. The combination achieves gains of 160 to 10,240. A thermopile produces a 1-mV signal, yielding 10.24V output from the INA114. To select other values of

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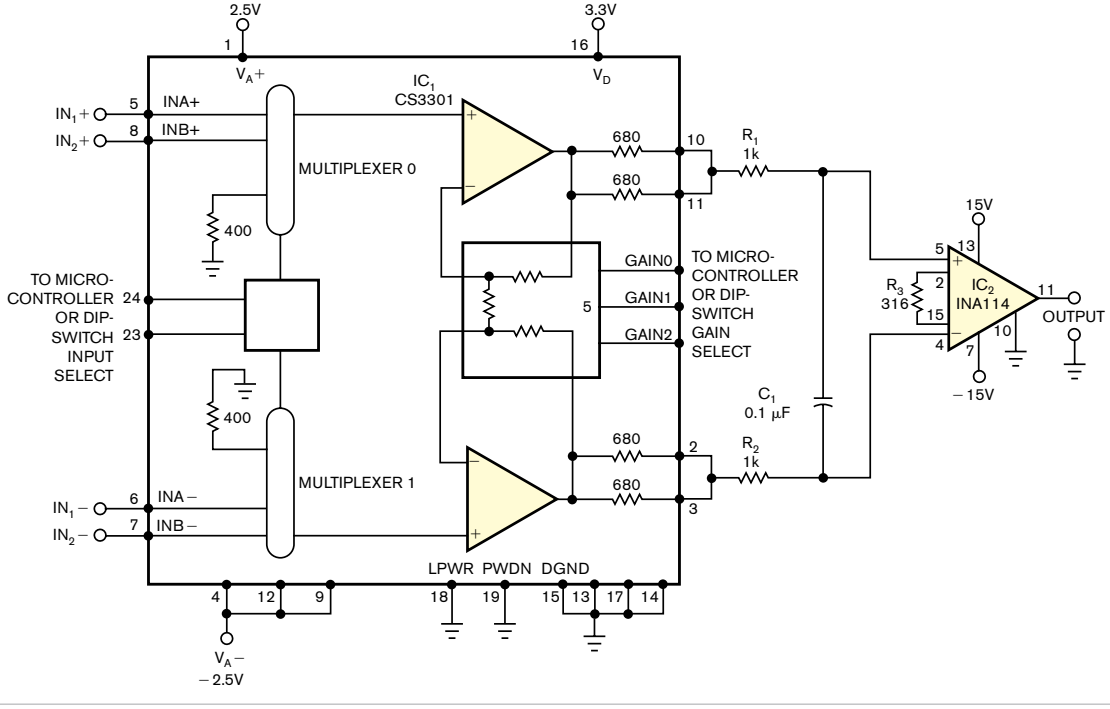

Figure 1 Combining a programmable-gain, chopper-stabilized amplifier with an instrumentation amplifier delivers high gain and low noise over a subaudible frequency range.

gain, change the value of the INA114's gain-setting resistor, R_3.

External DIP switches and pull-up resistors, which connect to the 3.3V supply (not shown), program the CS3301's gain- and multiplexer-control pins. A microcontroller that can drive 3.3V logic can also control these control inputs. Connecting the CS3301's outputs and the INA114's inputs, an RC lowpass filter composed of R_1, R_2, IC_1's output resistors, and C_1 limits noise above 500 Hz.

Figure 2 illustrates the combined amplifiers' measured input-referred noise performance at a gain of 10,000. With its 1/f noise corner at 0.08 Hz, the amplifier cascade achieves an equivalent input-noise voltage of about 9 $nV\sqrt{Hz}$ at 0.1 Hz. The noise-versus-frequency plot represents the results of FFT processing of more than 2 million output samples over an 18-hour period. For simplicity, the schematic doesn't show power supplies and bypass capacitors. Due to the circuit's extreme amplification factor, use construction techniques that maintain thermally balanced component placement and electrically balanced pc-trace lengths. EDN

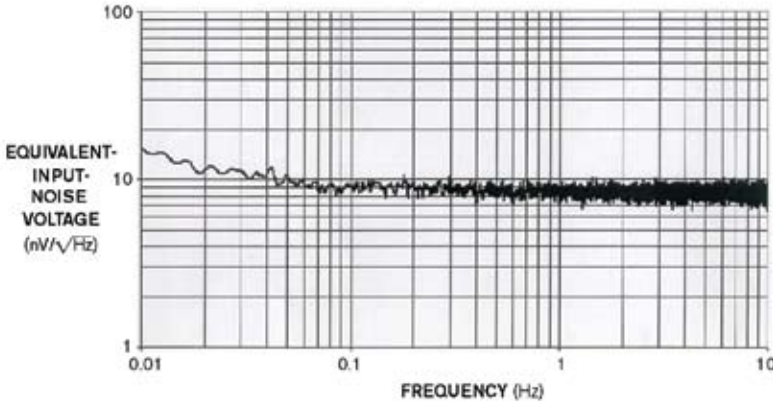

Figure 2 A three-octave plot displays the cascaded amplifiers' low equivalent-input-noise voltage versus frequency.

Current-mode instrumentation amplifier enhances piezoelectric accelerometer

Dave Wuchinich, Modal Mechanics, Yonkers, NY

A typical piezoelectric sensor comprises a disk of PZT-5A ceramic material with metallized electrodes on its surfaces. Applying electrically conductive epoxy to the electrodes connects external wiring to the sensor. An insulating adhesive attaches the assembly to the structure under test and isolates the sensor from ground-referenced potentials. The disk faces the direction of the expected acceleration. When you mount the piezoelectric disk on a target structure, it serves as a simple force sensor and accelerometer by producing a voltage that's directly proportional to the force acting parallel to the disk's direction of polarization. A piezoelectric disk's capacitive impedance presents a large reactance at

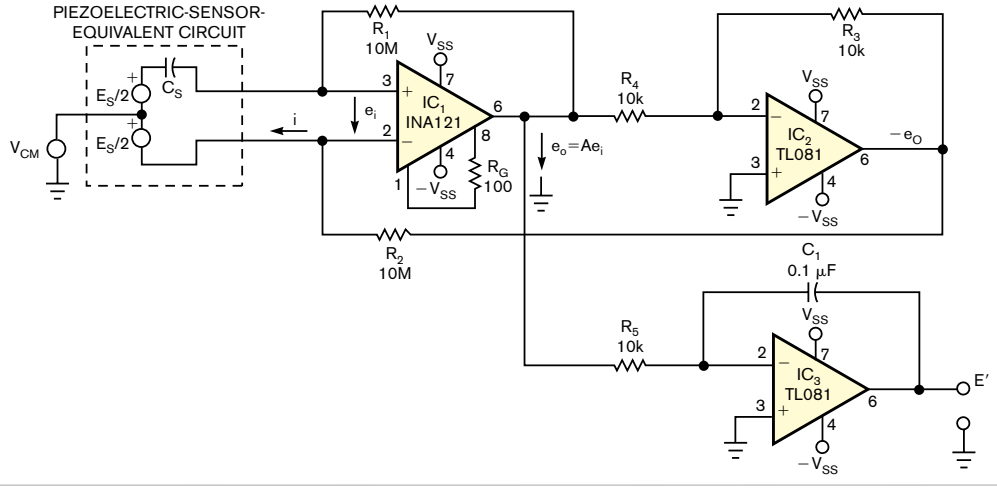

Figure 1 Three amplifiers and a handful of passive components suppress stray noise pickup on a piezoelectric accelerometer and its wiring.

low frequencies, making the disk and its wiring susceptible to interference that surrounding electrical equipment and power lines produce. Placing the sensor in a remote location requires shielded interconnecting cable, but even shielding is not entirely effective in removing common-mode signals because noise pickup can still occur at the disk's conductive surfaces.

One method of extracting the sensor's signal employs an instrumentation amplifier, which amplifies only the potential the sensor produces; the amplifier rejects common-mode-coupled noise potential that appears on each of the sensor's terminals.

A typical miniature piezoelectric-disk sensor that's 0.125 in. in diameter and 0.0075 in. thick presents a capacitance of approximately 500 pF. If the measurement application requires a dynamic response to force excitation frequencies of 10 Hz or below, the sensor's output reactance ranges into the tens of megohms. The circuit's pc-board insulating substrate and ambient humidity impose a practical limit of approximately 10 MΩ on the amplifier's input resistance.

You must carefully choose insulation and apply guarding potentials, and you must use an amplifier with picoampere input-bias currents. Otherwise, the sensor's capacitance and the amplifier's input-bias-current resistors impose a phase shift on the signal you apply to the instrumentation amplifier. To eliminate guarding and elaborate insulation requirements, the circuit in **Figure 1** uses an instrumentation amplifier with feedback to measure the sensor's short-circuit current and not its open-circuit voltage. V_{CM}, the common-mode voltage between the sensor and the signal ground, results from nearby noise sources resulting from stray capacitive coupling. The following **equation** relates the sensor's output current, i, and its open-circuit output voltage, E_S:

$$i = \left[\frac{2A+1}{\left(2R + \frac{(2A+1)}{j\omega C_S}\right)}\right] E_S,$$

where A represents IC_1's voltage gain, and $R=R_1=R_2$ in **Figure 1**. Resistors R_1 and R_2 provide feedback and input-bias-current-return paths for IC_1, an INA121 instrumentation amplifier, and resistor R_G sets the amplifier's gain. The INA121's input-bias-offset current of 0.5 pA produces 5 μV of voltage offset across its 10-MΩ feedback resistors. At an amplifier gain of 500, IC_1's output offset amounts to 2.5 mV. Amplifier IC_2, a TL081, provides unity-gain signal inversion.

If $2A+1>>2Rj\omega C_S$, then $i \cong j\omega C_S E_S$, and amplifier IC_1's input voltage, V_I, vanishes because the amplifier's input terminals act as a virtual short circuit across the sensor. Taking the sum of voltages around the loop comprising the instrumentation and inverting amplifiers' output, the two feedback resistors and the instrumentation amplifier's input terminals, whose potential difference is zero, yields $e_O=j\omega R_C E_S$, where e_O represents IC_1's output and also the negative value of IC_2's output.

An operational-amplifier-based integrator, IC_3, delivers the value for E_S at IC_3's output, E′ in the following **equation**.

$$E' = -\frac{RC_S E_S}{C(R_5)}.$$

For the component values in **Figure 1**, IC_1 provides a gain of 500. Resistors R_1 and R_2 are equal at 10 MΩ, and the piezoelectric sensor's capacitance measures 500 pF. For the highest frequency of interest, 10 Hz, the quantity $2R\omega C_S=0.6<<2A+1=501$ and the sensor's output, E_S, appear without phase error as E′. This circuit can measure quasistatic force changes; the circuit's ability to sustain a charge on C_1 imposes the ultimate limit on the circuit's frequency response. EDN

Low-cost RF sniffer finds 2.4-GHz sources

Vladimir Dvorkin, Linear Technology Corp, Milpitas, CA

Whether you measure or use RF circuits that operate in the popular 2.4-GHz ISM (industrial/scientific/medical) band, cordless telephones, Wi-Fi access points, Bluetooth devices, and microwave ovens can radiate RF signals, causing unwanted interference. A spectrum analyzer remains the instrument of choice for detecting and identifying interference sources, but analyzers are expensive, bulky, and sometimes not readily available.

The circuit in **Figure 1** shows an easily assembled, low-cost, and portable RF "sniffer" that provides a quick and reliable reading of the ambient-RF-signal level in the 2.4- to 2.5-GHz frequency band. At the circuit's heart, a Linear Technology (www.linear.com) general-purpose LT5534 RF-power detector, IC_1, measures RF-signal strengths from −55 to −5 dBm and provides an RSSI (received-signal-strength-indicator) dc-output voltage (**Reference 1**).

An antenna for this frequency band drives FL_1, a Toko (www.toko.com) filter (Part No. TDFU2A-2450T-10A), which restricts the circuit's passband to 2.4 to 2.5 GHz and limits out-of-band interference. The filter drives IC_1, whose internal circuitry comprises a cascade of RF detectors and limiters. The detectors' and limiters' summed outputs generate an accurate logarithmic-linear voltage proportional to the RF input in decibels. A single discrete transistor, Q_1, converts IC_1's RSSI output to a current that drives a low-current-LED signal-strength indicator. You can connect a digital voltmeter to IC_1's RSSI output to provide a digital readout of signal strength or rely on the lighted LED to visually indicate an RF signal. Two 1.5V alkaline batteries or three nickel-cadmium cells provide 3V power for the circuit.

The LT5534's frequency range of 50 MHz to 3 GHz covers the VHF, UHF, 800-MHz-cellular-telephone,

902- to 928-MHz-ISM, 2-GHz-PCS (personal-communications-system)/UMTS (Universal Mobile Telecommunications System), and 2.4-GHz-ISM bands. For the 2.4- to 2.5-GHz range, use a Laird Technologies (www.lairdtech.com) BlackChip antenna or a Toko dielectric antenna (Part No. DC2450CT1T). To build a sniffer for the 915-MHz band, replace the antenna with Part No. ANT-916-JJB-ST from Antenna Factor (www.antennafactor.com) and replace the input filter with a Toko 4DFA-915E-10 ceramic filter that provides 26 MHz of bandwidth centered on 915 MHz. EDN

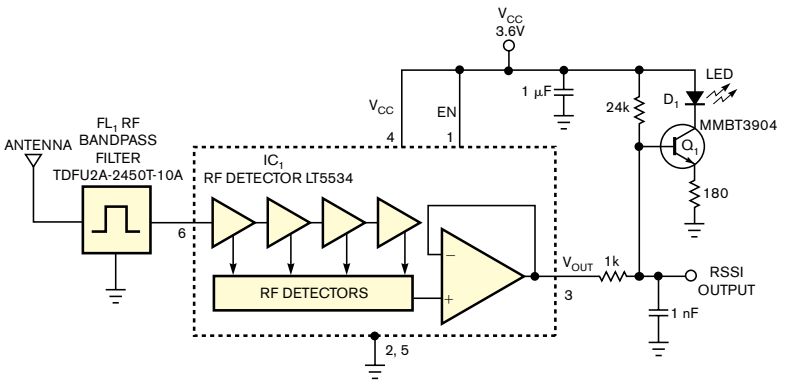

Figure 1 For best results, assemble this 2.5-GHz circuit on a double-sided pc-board layout according to the LT5534's data sheet and application notes.

REFERENCE

1 LT5534 data sheet, Linear Technology, www.linear.com.

Triangle waves drive simple frequency doubler

Jim McLucas, Longmont, CO

If you use a function generator, you may occasionally require a sine-wave output at a higher frequency than the generator can provide. If your function generator also produces a triangle-wave output, you can use a frequency doubler to extend the generator's available frequency by as much as a factor of two. A previously published Design Idea describes a triangle-wave-driven frequency-doubler circuit employing op amps that produce output frequencies limited to about 20 kHz (**Reference 1**).

This Design Idea describes a frequency doubler that provides a sine-wave output with a frequency of 4 to 6.7 MHz, with an output level that can range from 110 mV p-p to 1.30 V p-p into a 50Ω load. As **Reference 1** describes, applying a symmetrical triangle wave to a full-wave rectifier produces a triangle wave of twice the input frequency and offset by a dc level. Any asymmetry in the input waveform allows some of the input signal's fundamental frequency to pass through to the output. Also, the circuit's input transformer, T_1, may cause amplitude or phase imbalance, allowing some of the input signal to pass through to the output.

To construct a wideband transformer with good amplitude and phase balance, twist three AWG #30 enameled wires together at about 10 twists/in. Wind seven turns of the bundled wires onto a Fair-Rite (www.fair-rite.com) 2643002402 toroidal core. (Each pass through the core's central opening counts as one turn.) Connect the wires as shown in **Figure 1**. (Refer to **Reference 2** and **Figure 2** for additional information on this type of transformer.) This technique results in a wideband transformer with good amplitude and phase-balance characteristics.

To achieve maximum input-frequency attenuation, use a matched pair of Schottky diodes for D_1 and D_2. However, the prototype produced high-quality signals with unmatched Schottky diodes. In **Figure 1**, diode D_3 applies a small negative bias to D_1 and D_2 that allows operation at low signal levels. Capacitor C_1 passes the rectified and frequency-doubled triangle wave to the bases of a complementary emitter follower comprising Q_3, Q_4, and associated components. A simple, two-element lowpass filter at the follower's output removes higher frequency harmonics. Use any 1.6-µH inductor with a Q of 20 or greater for L_1. Although an inductor with a Q as low as 10 will not noticeably change the filter's frequency response, a value lower than 20 increases the inductor's insertion loss and decreases the maximum available output-signal amplitude.

A simple, two-element, lowpass output filter provides adequate performance for a symmetrical-triangle-wave input because the output's frequency components consist of the doubled input frequency signal and only the desired output signal's odd harmonics. For a 5-MHz output, the third harmonic occurs at 15 MHz with an amplitude of −19 dB relative to the 5-MHz signal. The lowpass filter imposes 15 dB more attenuation at 15 MHz, diminishing the 15-MHz signal to −34 dB relative to the 5-MHz output signal and attenuating higher order harmonics to even lower levels.

The complementary emitter follower's unfiltered output signal consists

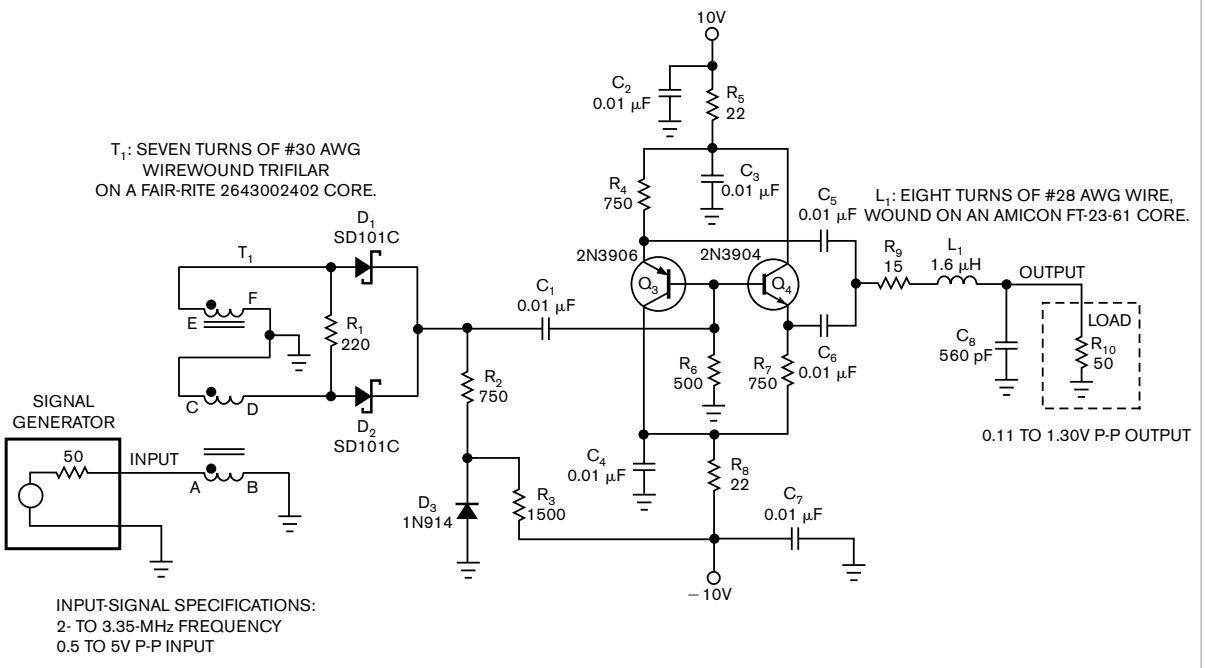

Figure 1 A full-wave rectifier, buffer, and lowpass filter produce a sine-wave output at twice the frequency of a triangular-wave input.

of a triangle wave of twice the input signal's frequency, plus odd harmonics of the doubled input frequency. For example, applying a 2.5-MHz triangle wave to the circuit's input produces a 5-MHz triangle-wave signal at the lowpass filter's input. For a nearly perfect triangle wave, the filter's input consists of a 5-MHz fundamental and only its odd harmonics. At −19 dB below the 5-MHz signal, the 15-MHz third harmonic represents the closest spurious signal and one that you can easily filter.

To use the circuit at higher frequencies, divide the values of output-filter components L_1 and C_8 by a factor of $F_{NEW}/5$, where F_{NEW} represents the desired output frequency in megahertz. For example, a nominal output frequency of 20 MHz requires division of the values of L_1 and C_8 by a factor of four, producing new values of 0.4 µH and 140 pF, respectively. Simulating the circuit with the revised filter in Spice shows adequate harmonic rejection over an output range of 16 to 26.8 MHz. Although designed for 5-MHz operation, the remainder of the circuit works well at 20 MHz without additional modifications. This frequency doubler also accepts a sine-wave input signal. However, the circuit's unfiltered output contains higher levels of the desired signal's even- and odd-order harmonics and requires additional filtering to produce a high-quality sine-wave output. EDN

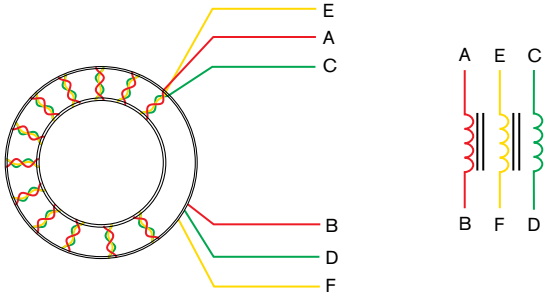

Figure 2 Transformer T_1 from Figure 1 consists of three windings on a toroidal ferrite core. For ease of assembly, twist three wires of different colors into a bundle to form the windings.

REFERENCES

1 Belousov, Alexander, "Frequency doubler operates on triangle waves," *EDN*, March 14, 1996, www.edn.com/archives/1996/031496/06di4.htm.
2 Demaw, MF "Doug," *Applying Toroidal Cores: Ferromagnetic-Core Design and Application Handbook,* ISBN: 0133140881, Prentice Hall, 1996, pg 97.

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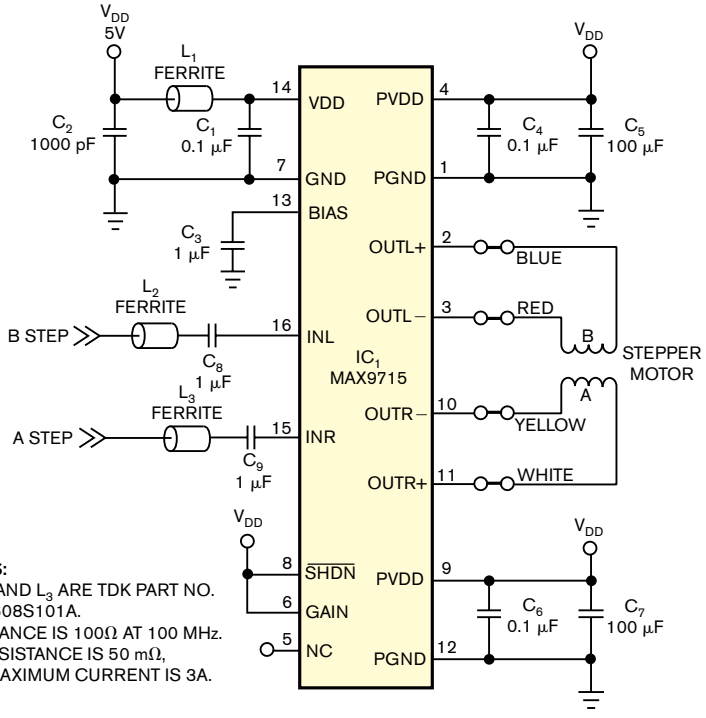
READERS SOLVE DESIGN PROBLEMS

Two-channel audio amplifier drives stepper motor

Phill Leyva and Bill Quach, Maxim Integrated Products, Sunnyvale, CA

Although relatively expensive, monofilar-wound, bipolar stepper motors provide strong torque for a given physical size. However, each of the motor's two windings requires eight driving transistors connected in groups of four in an H-bridge configuration. Each transistor must withstand and quickly recover from overloads and short-circuit conditions, and a driver must consequently include complex and large discrete-component protective circuitry.

As an alternative, **Figure 1** shows a motor-driver circuit based on Maxim's (www.maxim-ic.com) MAX9715, a tiny, surface-mount, 2.8W Class D audio amplifier, which typically drives 4 or 8Ω speakers. Each of IC_1's two outputs consists of a MOSFET H-bridge that drives a pair of output lines, OUTR+ and OUTR− and OUTL+ and OUTL−, that connect to the stepper motor's A and B windings, respectively. Each pair delivers a differential-pulse-width-modulated signal with a nominal switching frequency of 1.22 MHz. The circuit's low-interference design eliminates the requirement for output-line filters.



NOTES:
L_1, L_2, AND L_3 ARE TDK PART NO. MPZ1608S101A.
IMPEDANCE IS 100Ω AT 100 MHz.
DC RESISTANCE IS 50 mΩ,
AND MAXIMUM CURRENT IS 3A.

Figure 1 A single surface-mount circuit and a few passive components can drive a bipolar, monofilar-wound stepper motor.

Capacitors C_1, C_3, C_4, and C_6 provide bypassing for IC_1's power input and bias pins, and C_5 and C_7 provide bulk-holdup capacitance for the Class D power amplifiers' outputs. Capacitors C_8 and C_9 limit the amplifiers' input bandwidth to 16 Hz, and L_2 and L_3 suppress electrical-noise pickup by the long input cables. Comprising C_1, C_2, and ferrite bead L_1, a pi-section noise filter suppresses noise on IC_1's power-sup-

TABLE 1 A_STEP AND B_STEP PULSE SEQUENCE

Step	A_Step	B_Step
0	H	L
1	L	L
2	L	H
3	H	H
4	H	L

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ply input. A suitable controller feeds digital pulses to IC_1's A_Step and B_Step inputs, which respectively drive the motor's right and left channels. Internal short-circuit and thermal protection guards the amplifier against overcurrent and short circuits caused by the stepper motor or its connecting leads.

Table 1 illustrates the A_Step and B_Step pulse sequence that rotates a typical stepper motor in one direction by continuous application of steps 0 through 4. Step 4 returns the motor's shaft to its starting position and completes its 360° rotation. To reverse the motor, begin at the bottom of the **table** to reverse the pulse pattern and work upward. You can disable both of the amplifier's channels by applying a logic-low signal to Pin 8, IC_1's active-low $\overline{SHDN}$ input. **Figure 2** illustrates the circuit's input and output waveforms. EDN

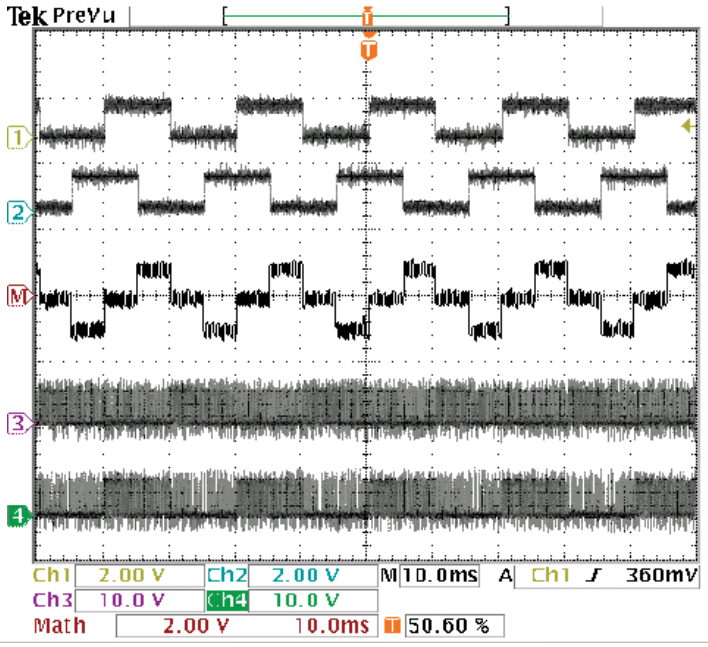

Figure 2 Waveforms from the circuit in Figure 1 include the A_Step input (Channel 1), B_Step input (Channel 2), outputs OUTR+ (Channel 3) and OUTR− (Channel 4), and the signal that arrives at the motor's windings (OUTR+ minus OUTR−, middle trace), which the oscilloscope's math function computes.

Get power from a telephone line without disturbing it

Yongping Xia, Navcom Technology, Torrance, CA

An idle telephone line tempts designers to use its 48V potential as a power source. However, Part 68 of the US Federal Communications Commission's telecommunications regulations states that any device that connects to the phone line and is not actively communicating must present a resistance of at least 5 MΩ (**Reference 1**). To meet this requirement, a device's continuous-current drain must not exceed 10 µA. Fortunately, many devices that connect to the phone line do not require continuous power and can remain off for long intervals, awakening only for a short time before relapsing into power-off mode. Providing power for these applications from the phone line presents obvious advantages by eliminating the need for a battery or another power source and the cost of battery maintenance.

The circuit in **Figure 1** charges a 1.5F supercapacitor, C_1, from the phone line through a diode bridge and a 5.6-MΩ resistor. A Maxim (www.maxim-ic.com) MAX917 nanopower comparator, IC_1, consumes only 0.75 µA from its power supply. Resistors

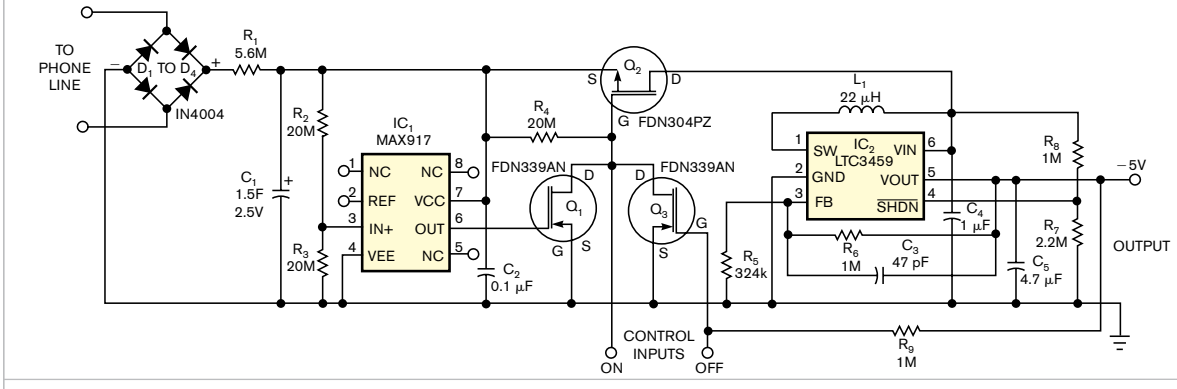

Figure 1 This power-conversion circuit delivers intermittent bursts of regulated voltage from a supercapacitor charged by a trickle of current from a telephone line.

R_2 and R_3 halve the voltage across C_1 and apply it to IC_1's positive input voltage at Pin 3 for comparison with its built-in 1.245V reference. For voltages across C_1 that do not exceed 2.49V, IC_1's output at Pin 6 remains low. When C_1's voltage reaches 2.5V, Pin 3's voltage exceeds the reference voltage, and IC_1's output goes high, turning on Q_1 and Q_2.

Several days must elapse before C_1 becomes fully charged, given its huge capacitance and a charging current of less than 10 µA. The voltage on C_1 can never exceed 2.5V because, once it reaches 2.49V, Q_1 and Q_2 turn on, connecting C_1 to a switched-mode-power-supply circuit. Because the power-supply current exceeds the charging current, the voltage across C_1 starts to decrease when Q_2 turns on. Transistor Q_3 holds Q_2 on when C_1's decreasing voltage causes Q_1 to turn off.

The switched-mode-power-supply circuit comprises a Linear Technology (www.linear.com) LTC3459 micropower boost converter, IC_2, and its associated components, which deliver 5V at 10 mA. A fully charged C_1 can supply power to a 10-mA load for approximately 40 sec. With no load, the circuit can sustain its 5V output for more than 10 hours. For greater output current and shorter operating time, select another boost converter that can operate at a low input voltage.

Mechanical switches, open-drain MOSFETs, open-collector transistors, or a microcontroller's open-drain output pins can drive two external control inputs to force the circuit on and off. Pulling the On input low forces Q_2 to turn on and deliver power from C_1 to the power converter, and pulling the Off input low turns off Q_2 and removes power from the converter. Note that the power converter's output-return line connects to the telephone line and thus should not connect to an earth ground or to grounded equipment. EDN

REFERENCE

1 "Part 68," Federal Communications Commission, www.fcc.gov/wcb/iatd/part_68.html.

Active-filter circuit and oscilloscope inspect a Class D amplifier's output

John Guy, Maxim Integrated Products Inc, Sunnyvale, CA

The increasing acceptance of Class D amplifiers has helped them gain market share from their linear Class AB brethren. That acceptance is no surprise; the advantages of Class D amplifiers are legion, but such amplifiers also require new techniques for evaluation. For example, consider a basic sine-wave test of a linear amplifier. You apply power, apply a sine wave of suitable amplitude to the input, and connect an oscilloscope probe to the output. You'll see a replica of the input, usually offset by about half the power-

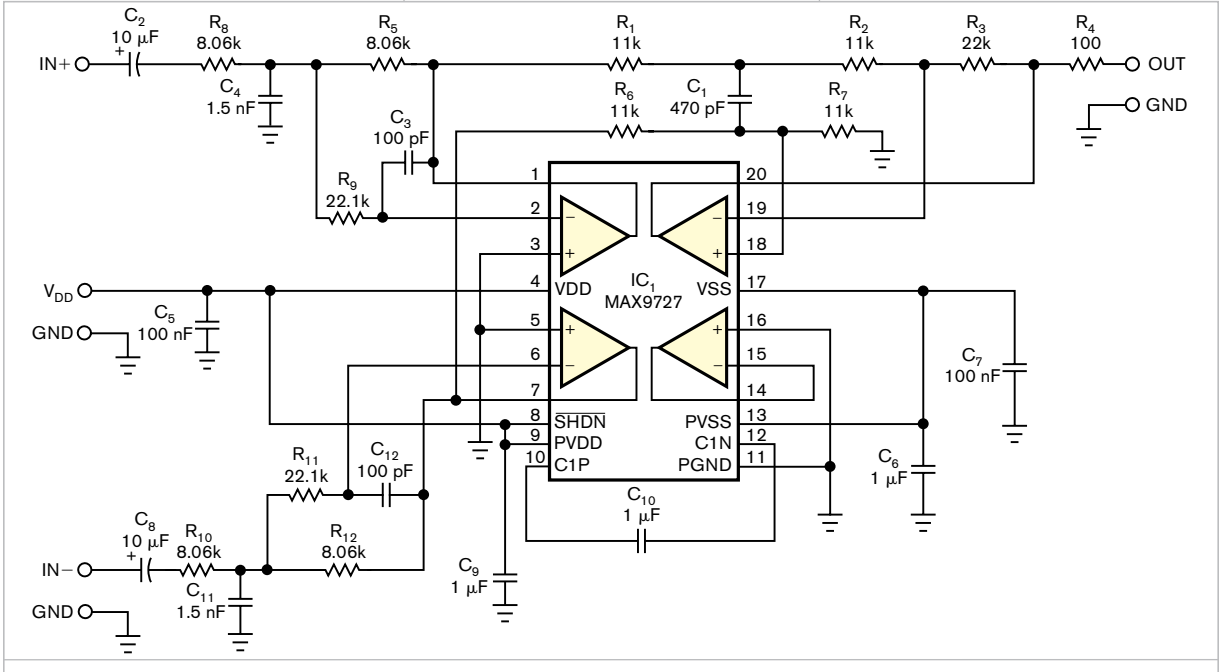

Figure 1 Use this third-order, 30-kHz filter circuit to observe a Class D amplifier's output signal on an oscilloscope.

supply voltage. Even if the linear amplifier drives a BTL (bridge-tied load), you'll still see a recognizable replica of the input at either end of the load, albeit at half of the output signal that's available.

Testing a Class D amplifier poses more difficulties. The amplifier's output comprises a PWM (pulse-width-modulated) signal that swings between ground and the supply voltage at a frequency that's usually 200 kHz to 2 MHz. However, when you view this PWM output on an oscilloscope, you'll see no resemblance to the sine-wave input.

You can observe a Class D audio amplifier's output if you introduce the filter circuit in **Figure 1**. Based on Maxim's (www.maxim-ic.com) MAX-9727 quad-audio-line driver, IC_1, the circuit combines separate single-ended filters—one for each of the BTL outputs' phases—with a third amplifier that provides a difference signal with additional filtering. The first stage of each single-ended-filter section contributes the complex-conjugate pole pair of a third-order, 30-kHz multiple-feedback Butterworth filter, for which many design guidelines and equations are available. Each third-order-filter section comprises a complex-conjugate pole-zero pair and one real pole.

To improve the match between the signal paths, the two separate multiple-feedback filters share a real pole, which 470-pF capacitor C_1 and 11-kΩ resistors R_1 and R_6 provide. The circuit implements that pole as a difference amplifier, thereby producing a filtered output that presents a single-ended version of the BTL amplifier's outputs. The filters' signal paths present 5.5-kΩ impedances to each of the A and B amplifier sections' inputs. By inspection, the net 5.5-kΩ impedance from Section B's output to C_1 comprises the Thevenin-equivalent impedance of resistors R_6 and R_7. Similarly, the net impedance from Section A's output to C_1, also 5.5 kΩ, comprises the Thevenin impedance of resistors R_1 and R_2. Note that the virtual ground from Amplifier D's inverting input effectively grounds resistor R_2.

Matched resistors attenuate each of Amplifier D's differential inputs by 6 dB (IN+ by R_1 and R_2 and IN− by R_6 and R_7). A 22-kΩ feedback resistor, R_3, provides Amplifier D with a gain of two, which sets a unity-gain-transfer function in the circuit's passband. The circuit's single-ended output with respect to ground allows the oscilloscope's ground to also serve as the output signal's ground. A version of this circuit using conventional op amps would require a negative-power-supply-voltage source, but Maxim's MAX9727 already includes a negative-voltage source, which its internal charge-pump circuit generates. When you operate the circuit from a 5V supply, the circuit's output delivers more than 2.5V rms. Although its third-order filter is inadequate for precise measurements of distortion or noise, the circuit provides an excellent tool for troubleshooting and evaluating Class D-amplifier circuits and inspecting their outputs on an oscilloscope. EDN

Voltage-to-pulse-width converter spares microprocessor's resources

James Christensen, Kris Design Co, El Cajon, CA

Although not an ADC in the classic "stream-of-ones-and zeros" sense, this voltage-to-pulse-width converter produces a logic-level output pulse whose variable width represents an analog of the input voltage. Based on Atmel's (www.atmel.com) AT89LP4052 microprocessor, IC_1, this circuit makes efficient use of the target microprocessor's limited analog-port pinout and code space by using a modified version of the classic timed-discharge-RC (resistor-capacitor) ADC design.

The timed-RC ADC allows a capacitor to charge through a resistor while the microprocessor increments a counter. When a comparator detects that the capacitor voltage and analog- input voltage are equal, the count terminates, and its stored value represents the ADC's output. However, an RC network's exponential charging characteristic produces a nonlinear conversion. Various software and hardware techniques can partially correct the nonlinearities, but all entail adding code, increasing the circuit's development time, or consuming additional I/O-port pins required for other purposes.

To produce a linear-charging characteristic that needs no correction, the circuit in **Figure 1** uses an LM334 constant-current source, IC_2, to drive capacitor C_2, which connects to IC_1's AIN_0 analog-input port. An internal timer in the microcontroller measures the elapsed time from the charging ramp's start to the instant when the ramp voltage crosses the analog-input-voltage threshold at IC_1's AIN_1 port.

In this application, potentiometer RV_1 provides an analog-input voltage proportional to its position. The width of the positive-going pulse at the output, P1.5, varies in proportion to the analog-voltage input. Note that I/O-port pin AIN_1 serves a dual purpose as an analog input and as an open-drain output that discharges ramp-forming capacitor C_2 before the next conversion cycle.

An 8-bit voltage-to-pulse-width-conversion cycle completes in less than 4 msec. The code performs the conversion function and outputs a pulse train at IC_1's port P1.5 (Pin 17) with a period of 100 msec and a positive-going pulse width proportional to the analog-input voltage at Pin 13 (AIN_1). Programming connector J_1 provides access to IC_1 for

uploading the compiled code. The AT89LP4052 microprocessor typically executes one instruction per clock cycle, and a 10-µsec timer routine can perform the required housekeeping functions with plenty of time left over for other program tasks, including a future application that requires a binary-coded analog-to-digital output. You can download **Listing 1**, which is written in C for the Keil Software (www.keil.com) compiler, from the online version of this Design Idea at www.edn.com/061201di1.EDN

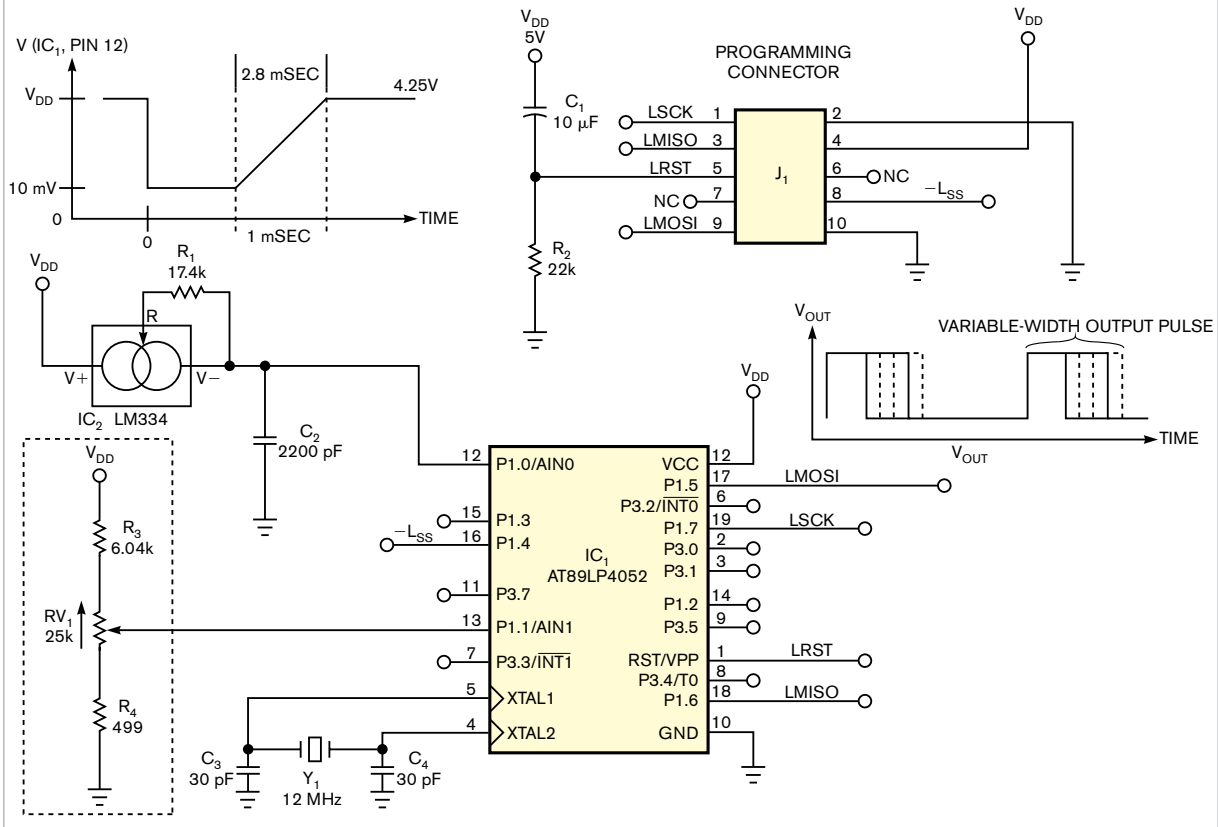

Figure 1 An analog-voltage-to-pulse-width converter features minimal parts. Subgraphs show timing-network and output-voltage waveforms. IC_1's unlabeled pins are available for user functions.

Precision voltage reference delivers 80 mA

James Horste and Gary Staiman,
Maxim Integrated Products Inc, Sunnyvale, CA

Large analog systems that present many loads to a voltage-reference source can often demand more current than a single reference IC can deliver. However, if the reference IC includes force and sense terminals, you can easily add a buffer to the circuit's feedback loop without affecting the reference's accuracy. For example, the circuit in **Figure 1** provides the same 0.04% initial accuracy and 7-ppm/°C temperature coefficient as IC_1, a stand-alone MAX6033. The buffer circuit delivers as much as 80 mA.

When you design a buffer stage for a force/sense-control loop, the buffer must provide unity-voltage gain with no phase inversion. In addition, the circuit's power supply must provide head-room voltage to accommodate the reference voltage plus voltage drop across the buffer stage. The simplest buffer circuit comprises an NPN transistor that connects as an emitter follower, which requires a drive voltage that exceeds the reference's output voltage by one transistor base-

emitter voltage drop. If you add the required minimum power-supply voltage plus the maximum allowable base-emitter voltage, the configuration runs out of head room. Using a PNP stage to drive the emitter drive stage solves the head-room problem but inverts the output voltage and prevents the force/sense loop from functioning. Adding a second PNP stage cancels the phase inversion but destabilizes the force/sense loop by adding excessive gain.

The modified complementary Darlington, or Sziklai, connection (**Reference 1**) in **Figure 1** solves both problems by providing an emitter follower's unity-voltage gain with no inversion. The output PNP stage provides plenty of head room, but the NPN stage does not. You can easily overcome this drawback by adding diode D_1 to shift the NPN transistor's emitter voltage downward by a diode drop. Thus, to a first approximation, the diode's voltage drop and the transistor's base-emitter voltage cancel one another, leaving plenty of voltage head room.

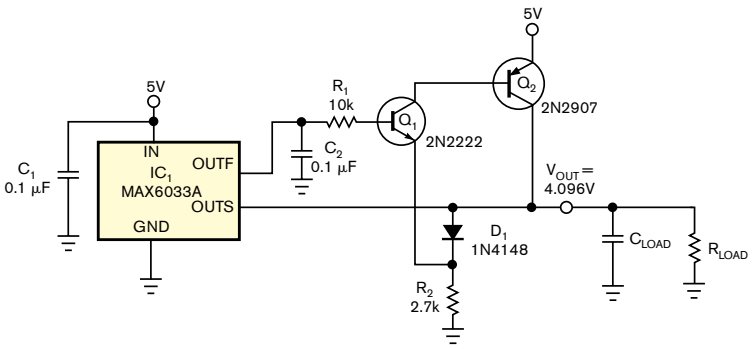

Figure 1 Add a two-transistor output buffer to a 4.096V, 15-mA reference IC to boost its output current to 80 mA or higher.

Transistor Q_2, a 2N2907, provides limited current gain, which in turn limits the circuit's maximum output current to 80 mA. Substituting a higher gain transistor can increase the output current to any reasonable level.

For stability, the MAX6033 requires 0.1-µF ceramic bypass capacitors on its In and OutF pins. Capacitor C_2 determines the circuit's response speed, but the buffer circuit exerts no significant effect on transient response. Most dc-reference-voltage ICs cannot accommodate a fast-changing load-current step; thus, the circuit's transient response and its ability to supply fast current spikes depend on the output capacitor, C_{LOAD}. Values of C_{LOAD} as high as 10 µF do not affect the circuit's stability. EDN

REFERENCE

1 "Sziklai Pair," Wikipedia, http://en.wikipedia.org/wiki/Sziklai_pair.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Three microcontroller ports drive 12 LEDs

Nedjeljko Lekic and Zoran Mijanovic, University of Montenegro,
Department of Electrical Engineering, Podgorica, Montenegro

Based on a previously published Design Idea (**Reference 1**), the circuit in **Figure 1** uses only three I/O lines to drive 12 LEDs. In this application, the circuit serves as a tachometer for a motor-vehicle engine and displays relative engine speed on an array of LEDs arranged in a line or a circular arc. Three pairs of inverse-parallel-connected LEDs (D_2 and D_3, D_4 and D_5, and D_6 and D_7) receive drive current from IC_1's ports through current-limiting resistors R_5, R_6, and R_7. Two groups of three LEDs, D_8, D_9, and D_{10} and D_{11}, D_{12}, and D_{13}) connect among IC_1's ports and two voltage dividers that supply reference voltages V_{REF1} and V_{REF2}. Varying the values of resistors R_5, R_6, and R_7 adjusts the brightness of the middle six LEDs, and R_1, R_2, and R_4 control the brightness of the outer six LEDs. In general, this circuit can use N of a host microprocessor's I/O lines to drive as many as $N(N-1)+2N$ LEDs, or 2N more LEDs than the circuit in the original Design Idea could drive.

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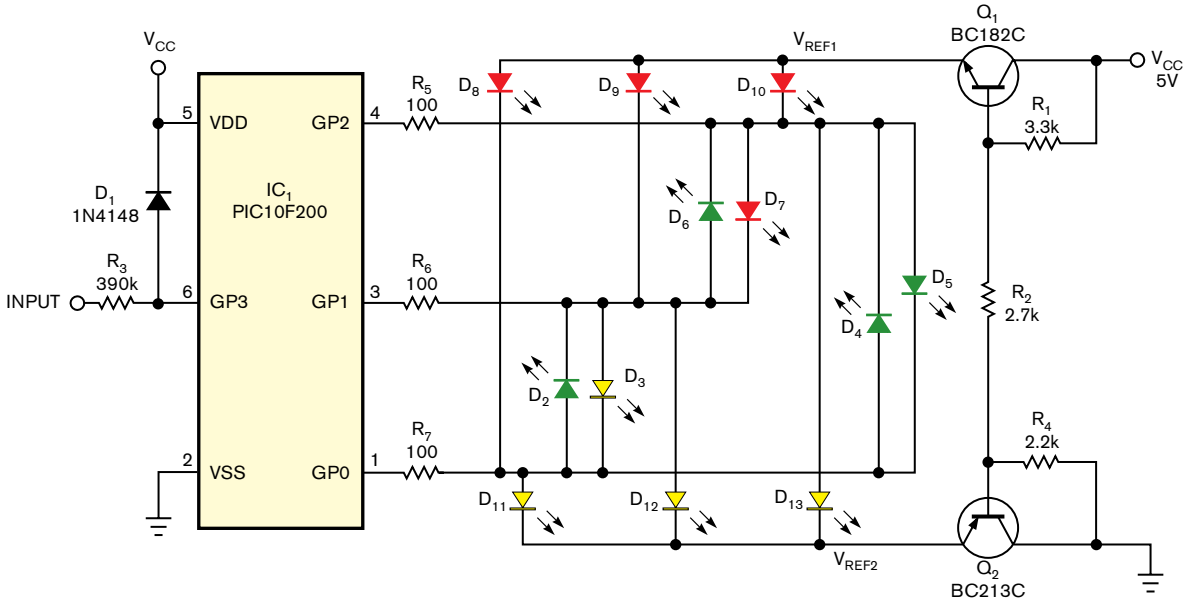
The circuit uses Microchip's (www.microchip.com) PIC10F200 microcontroller, IC_1, a small, inexpensive, six-pin device that provides only three I/O pins and one input-only pin. The I/O pins—GP0, GP1, and GP2—drive a 12-LED bar graph comprising



NOTE: LEDs ARE PANASONIC SSG LN224 SERIES (RED), LN324 SERIES (GREEN), AND LN424 SERIES (YELLOW).

Figure 1 A PIC microprocessor and a 12-LED bar-graph display form a simple tachometer circuit. (The decoupling capacitors are not shown.)

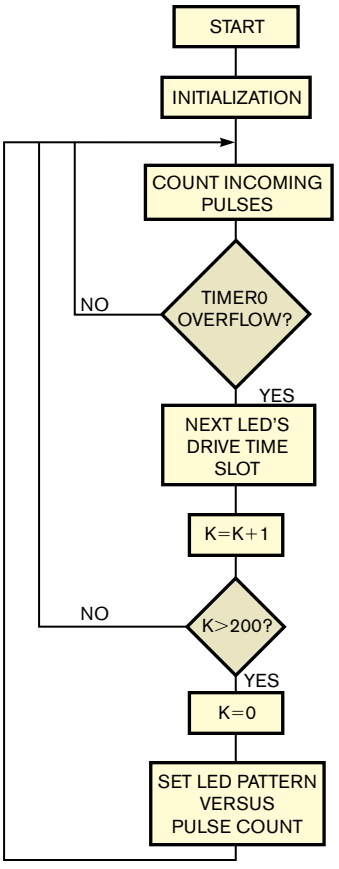


Figure 3. This flow chart shows the LED-driver software routine. (See the listings at www.edn.com/061215di1 for the complete tachometer routine.)

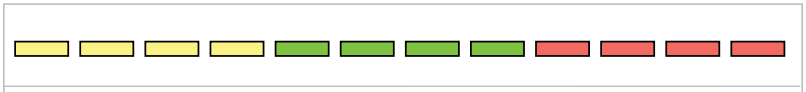


Figure 2. The bar graph display's 12 LEDs can form a linear array or circular arc (not shown).

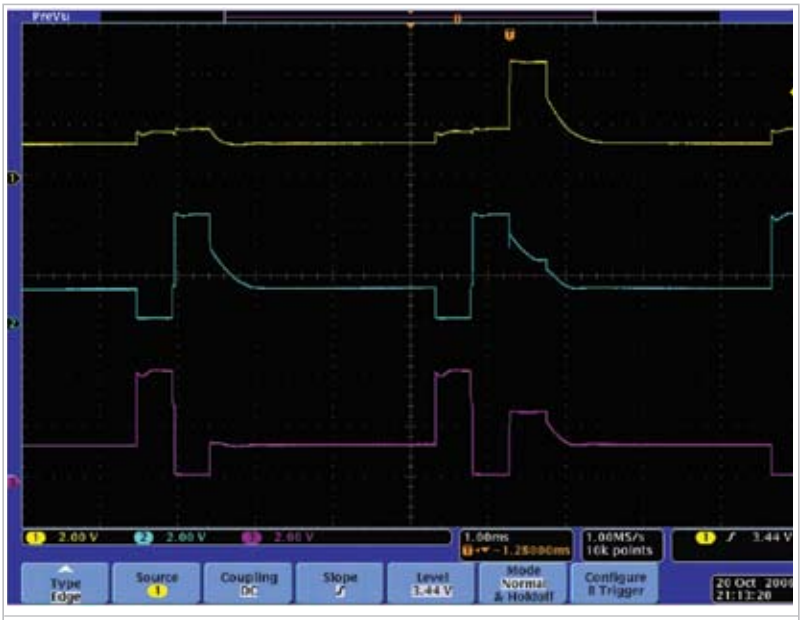


Figure 4 A digital oscilloscope captures the waveforms of GP0, GP1, and GP2 (upper to lower traces, respectively), which show a transition in the LED pattern from Case 7 to Case 8 (lines 62 and 63 in Listing led121.c.pdf).

four yellow LEDs, four green LEDs, and four red LEDs driven in multiplexed mode (**Figure 2**).

The microprocessor's input-only pin, GP3, serves as the input for pulses coupled from the ignition coil's primary terminal. Resistor R_3 and diode D_1 provide input-signal conditioning, and a software-debouncing routine removes ringing effects from the pulses. Given R_3's high value of 390 kΩ, the circuit tolerates high-voltage input spikes and prevents latch-up of the PIC10F200. Port GP3, which serves as the processor's programming port, differs from the processor's other ports because it incorporates an internal protection diode. The 20-mA diode prevents GP3 from negative-going transient voltages. The circuit operates reliably, but you can add an external protection diode for enhanced protection against transient-induced latch-up. Connect the diode's anode to ground and its cathode to pin GP3 of IC_1.

You can configure the bar graph to indicate engine speed by the number of LEDs turned on (bar mode) or by illuminating only one or two LEDs (dot mode). The color scheme in **Figure 2** uses yellow LEDs to indicate too-low speed, green LEDs for nominal speed, and red LEDs for excessive speed. **Figure 3** shows the indicator software's flow chart. The processor's internal clock drives Timer0 to overflow every 512 µsec, which represents one time slot—that is, a multiplexing phase. Of eight time slots, one drives the three upper LEDs, and a second drives the three lower LEDs. For software simplicity, the last six time slots drive the middle LEDs one by one. At the start of the main loop, the microprocessor counts clock pulses and waits for Timer0 to overflow. After overflow occurs, the output ports drive the LEDs according to their assigned time slots. After eight time slots elapse, the processor sets the ports to the same state. After 200 time slots, the processor counts incoming tachometer pulses and sets the LED pattern according to the incoming pulse count—that is, according to input frequency.

The tachometer indicates rotary speed as high as 120 cycles/sec. The accompanying software listings available at www.edn.com/061215di1 include files in C language (led12.c.pdf) and in assembly language (led12.asm.pdf). The source zip file contains a complete MPLab project. **Figure 4** shows the waveforms, which a digital oscilloscope captured at ports GP0, GP1, and GP2. EDN

Magnetic-field probe requires few components

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Popularly known as "gauss meters," various makes and models of magnetic field meters are available on the market at prices that make them unaffordable to many hobbyists and engineers. This Design Idea combines a commonly available DMM (digital multimeter) with a single semiconductor component to measure magnetic-flux density and, in turn, magnetic-field intensity.

Figure 1 illustrates the measurement equipment, comprising a probe, its battery pack, and a DMM. The probe's active element consists of a linear Hall-effect sensor. Although virtually any linear Hall sensor will work in this application, this version of the probe uses an Allegro MicroSystems Inc (www.allegromicro.com) A1323 sensor, which produces a voltage proportional to an applied magnetic field (**Reference 1**). Operating from a power supply of 4.5 to 5.5V, the A1323's quiescent output voltage (zero-field output) rests at 50% of the supply voltage. Given its nominal sensitivity of 2.5 mV/gauss, the A1323 provides a full-scale range of 1800 gauss (4.5V/2.5 mV/gauss=1800 gauss) for a supply voltage of 4.5V.

Applying a magnetic field oriented south of the sensor's face increases the sensor's output voltage in proportion to the applied field perpendicular to the sensor's branded face, and applying a magnetic field north of the same face causes a proportional decrease in output voltage. For a supply of 4.5V, the sensor's quiescent output voltage of 2.25V can increase to 4.5V for a 900-gauss, due-south field or decrease to 0V for a 900-gauss, due-north field. Although the sensor can detect the intensity and polarity of a dc magnetic field, its ac-field bandwidth extends to 30 kHz.

The probe's breadboard version comprises a small piece of pc board of sufficient length to fit the operator's hand (**Figure 2**). The sensor's leads connect to a length of high-quality, three-conductor shielded cable and two 10-nF surface-mounted decoupling capacitors. The sensor's power supply comprises three series-connected, miniature, 1.5V batteries for a total of 4.5V. For a larger full-scale-measurement range, use a 9V battery to feed a 5V regulator IC, such as a 7805 voltmeter and add an on/off switch if desired. Place the batteries near the meter. Otherwise, the batteries' steel cases will disturb the magnetic field under observation. Use 10-nF SMD capacitors to decouple the sensor's input and output pins. Although any DMM offering high dc accuracy and an ac bandwidth exceeding 50 kHz can display the sensor's output, a DMM with a RELΔ ("relative-difference-from-reference-reading") function, such as a Fluke (www.fluke.com) model 187 DMM, eases measurement

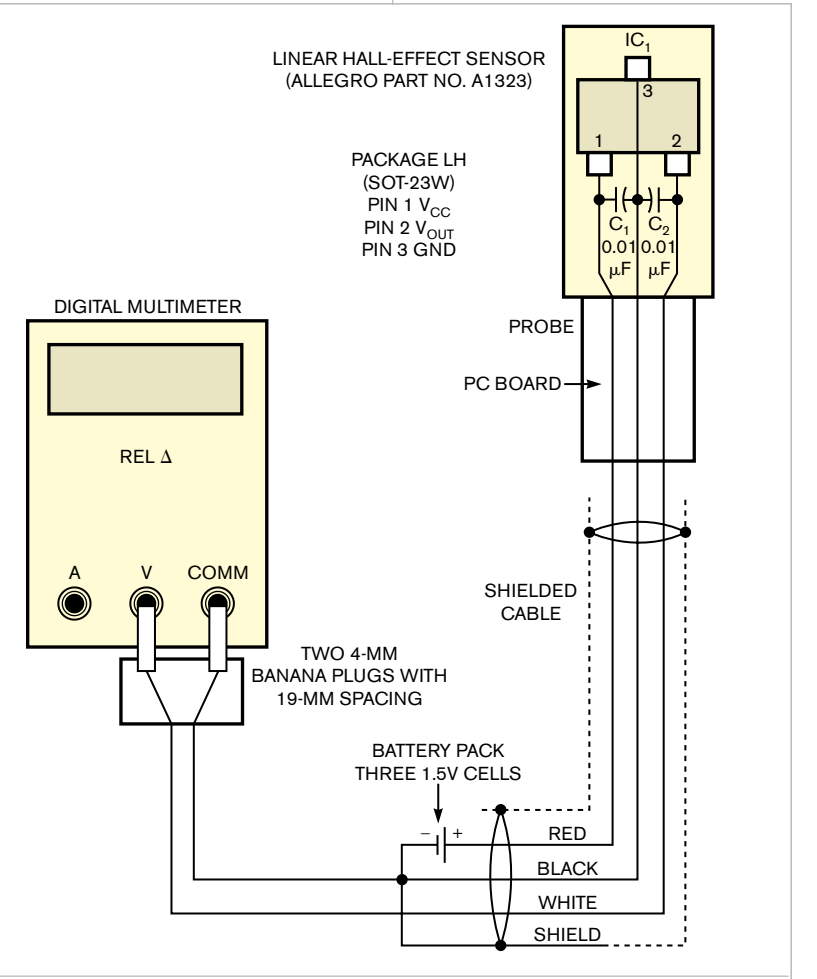

Figure 1 A digital multimeter and a Hall-effect sensor form an easily assembled magnetic-field probe.

and polarity detection of a dc magnetic field (**Reference 2**).

After assembling the circuit, connect the probe's output to the DMM using two 4-mm banana plugs. Allow a one-minute warm-up and place the probe's sensor in a magnetically shielded enclosure. (Editor's note: You can use salvaged steel, or "tin," concentrically fitting food cans to build a magnetically shielded enclosure. Arrange the cans so that their unopened ends point in opposite directions. Drill a small opening in the larger can's unopened end to accommodate the sensor's output cable.) Press the DMM's RELΔ function key. The DMM's display will show the sensor's quiescent voltage output of 2.25V as 0.0000V, indicating that the probe is calibrated for a zero magnetic field and ready for use.

Remove the probe from the shielded enclosure and measure the magnetic field under observation. To achieve maximum sensitivity, place the sensor's face perpendicular to the field. If the field's direction is unknown, rotate the probe about its longest axis to search for maximum voltage. To calculate the magnetic-flux density, divide the output-voltage reading by the sensitivity (2.5 mV/gauss). For example, if the meter reads −1.9800V, then the magnetic field is 792 gauss due north. For an ac-magnetic-field measurement, use the DMM's true-rms mode to read the sensor's ac output voltage.

Figure 2 The digital multimeter's relative-change mode (RELΔ) displays a near-zero magnetic field reading and the sensor's nominal zero-field output voltage of 2.25V.

You can calculate a magnetic field's intensity in air by applying the following formula: $B=\mu_0 \times H$, where B represents magnetic-flux density in teslas, H represents magnetic-field intensity in amperes per meter, and $\mu_0=4\pi \times 10^{-7}$H/m (the permeability of free space). Given that the tesla represents a relatively large measurement unit, a 1T field is quite strong.

For greater measurement resolution, apply the following conversion factors to use the gauss, a more popular unit: 10,000 gauss=1T, 1 gauss=79.6 A/m, 1.2560 mT=1 kA/m. Applications for the magnetic-field sensor include troubleshooting moving-magnet linear-position detectors, fabrication of dc motors and audio speakers, investigation of low-frequency-magnetic-field interference, and designing and fabricating electromagnetic-interference shields. EDN

REFERENCES

1 A1323 Ratiometric Linear Hall-Effect Sensor Data Sheet, Allegro MicroSystems Inc, www.allegromicro.com/sf/1321.

2 *User's Manual, Model 187 & 189, True RMS Multimeter*, Fluke Corp, www.fluke.com.

Dynamic siphon steals current from USB port

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A USB port offers a handy source of 5V power for auxiliary devices. A USB port not only supplies power to a microcontroller and other essential circuitry, but also provides enough extra current head room to charge a small battery or supercapacitor energy-storage element. One typical approach to exploiting a USB port's leftover-current capability begins with an estimation of the essential circuitry's maximum current drain. You then place an appropriate current-limiting

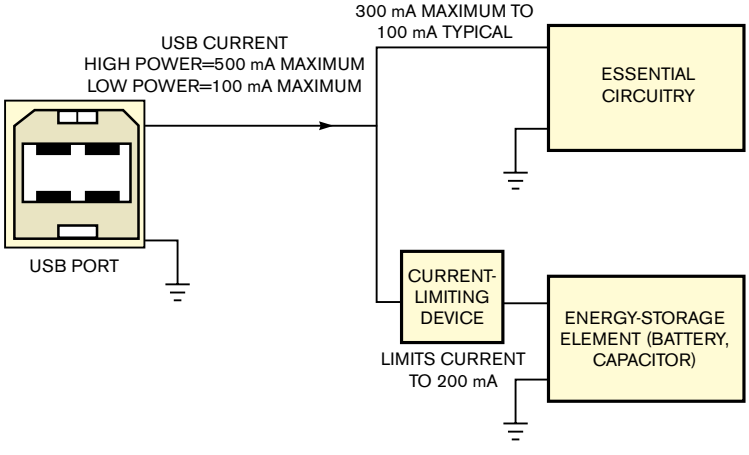

Figure 1 In this typical method for drawing power from a USB port, the storage-element current is limited to a fixed value that is less than optimal.

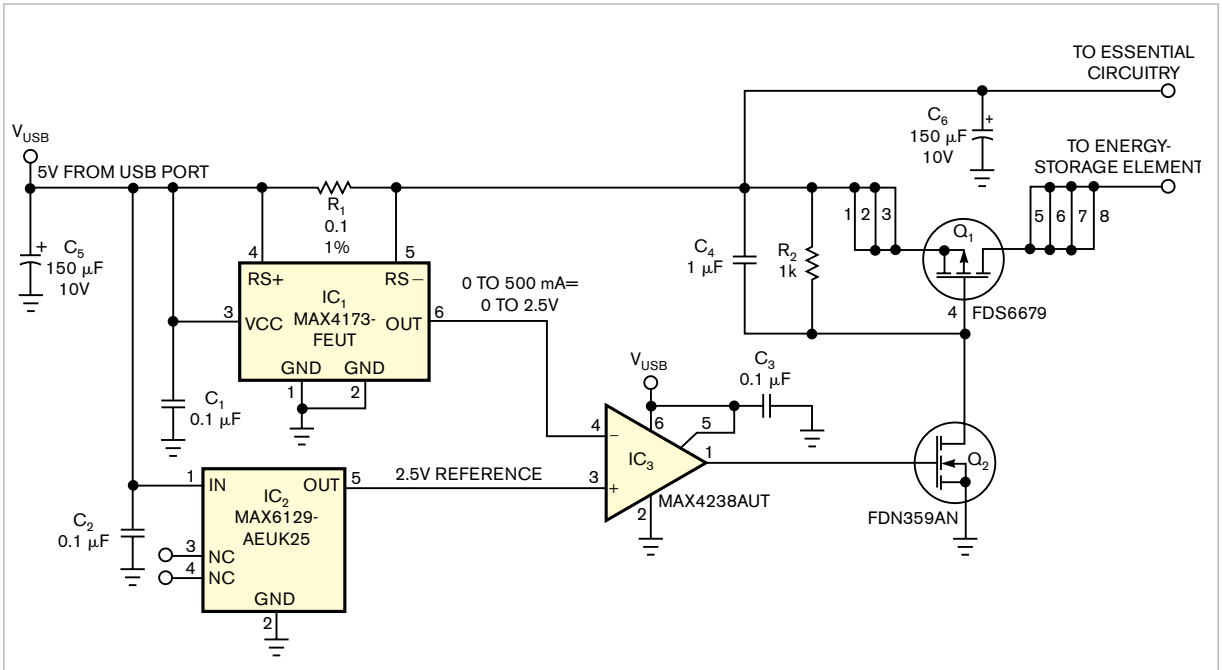

Figure 2 This circuit continuously monitors the total current drawn from the USB port and dynamically adjusts the storage-element current to avoid exceeding the port's maximum output capability.

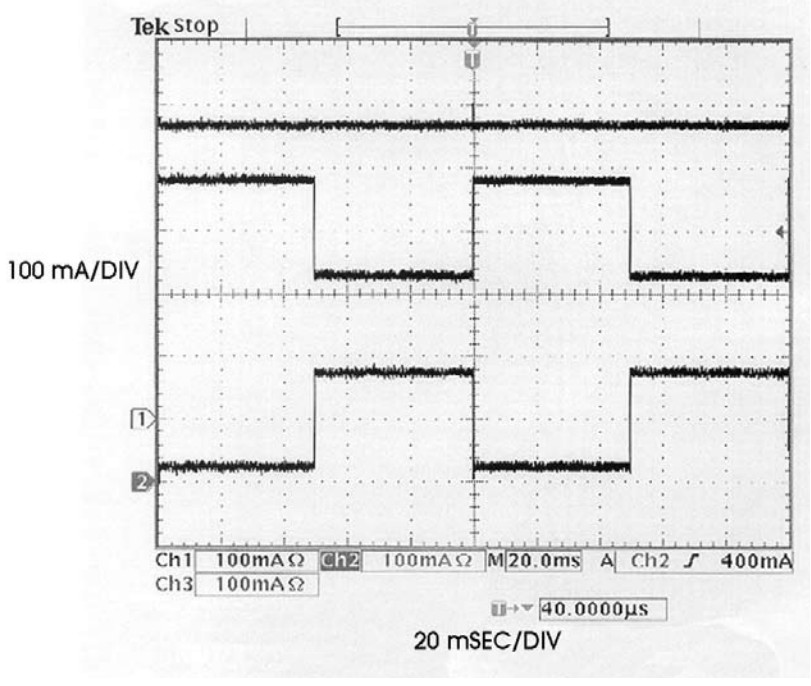

Figure 3 These waveforms taken from Figure 2 show that the sum of the essential-circuitry current (middle trace) and storage-element current (bottom trace) never exceeds the 500 mA maximum that the USB port (top trace) specifies.

device in the path of the energy-storage device (**Figure 1**). Although easy to implement, this method doesn't use all of the current available from the USB port, and the energy-storage device slowly charges or recharges.

The circuit in **Figure 2** uses all available USB power by dynamically adjusting the amount of current delivered to the energy-storage device and thereby siphoning a relatively constant and maximum current from the USB port. IC_1, a Maxim (www.maxim-ic) MAX4173FEUT; IC_2, a Maxim MAX-6123AEUK25; and the load-switch circuit comprising Q_1, Q_2, R_2, and C_4 form a control loop that limits the current flowing through Q_1. The circuit maximizes current flowing to the energy-storage element (**Figure 3**) by ensuring that the sum of battery and essential-circuitry currents never exceeds the maximum of 500 mA for a high-power USB device. To reconfigure the circuit for low-power USB operation of 100 mA maximum, you can replace IC_1 with a MAX4173HEUT, a device with 100V/V gain, and R_1 with a 0.25Ω resistor. EDN