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Cascade two decade counters to obtain 19-step sequential counter
Dual-input sample-and-hold amplifier uses no external resistors

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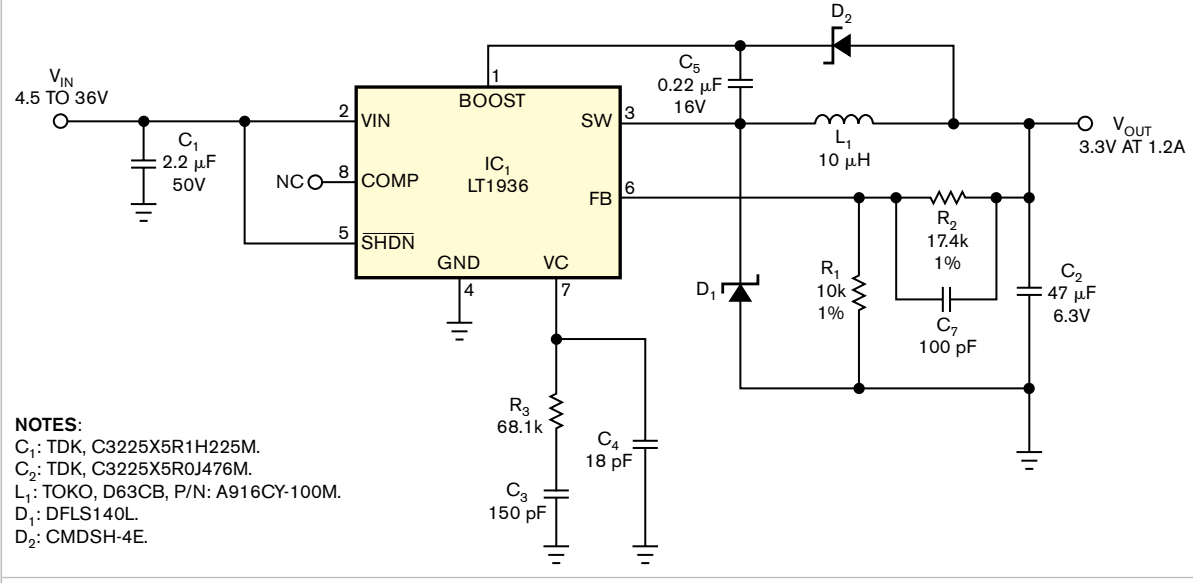
Extend low-output-voltage switching regulator's input range

Hua (Walker) Bai, Linear Technology, Milpitas, CA

Internal operating voltages in electronic devices continue to decrease, but input-source voltages don't change. As the difference between input and output voltages increases, so does the improvement in efficiency that a switching regulator offers. Unfortunately, as a switched-mode step-down converter's output voltage decreases, the decrease imposes limitations on the circuit's input-voltage range. This Design Idea shows how to extend a low-output-voltage step-down converter's input-voltage range.

A switching-mode step-down regulator, such as Linear Technology's (www.linear.com) LT1936 (IC_1), includes an internal high-side NPN power transistor between its input, V_{IN}, and switched-output (SW) pin. For highest efficiency, the high-side NPN transistor requires a base voltage that's higher than the input voltage. The circuit of **Figure 1** works best for output voltages greater than 3V. A charge pump comprising diode D_2 and capacitor C_5 maintains the voltage at the Boost pin 3V above V_{IN}. When IC_1's internal power transistor switches off, the voltage at SW goes to ground through D_1. Boost capacitor C_5 charges to 3V supplied from V_{OUT} through D_2. When the power transistor turns on, the voltage at SW jumps to V_{IN}, and the voltage at the Boost pin jumps to $V_{IN}+3V$, which provides sufficient head room to drive the power transistor into saturation for greatest efficiency.

However, output voltages below 2.8V no longer provide sufficient drive volt-



NOTES:
C_1: TDK, C3225X5R1H225M.
C_2: TDK, C3225X5R0J476M.
L_1: TOKO, D63CB, P/N: A916CY-100M.
D_1: DFLS140L.
D_2: CMDSH-4E.

Figure 1 For efficient operation at output voltages of 3.3V or higher, a charge pump comprising D_2 and C_5 provides a voltage boost that provides sufficient drive for IC_1's internal switching transistor.

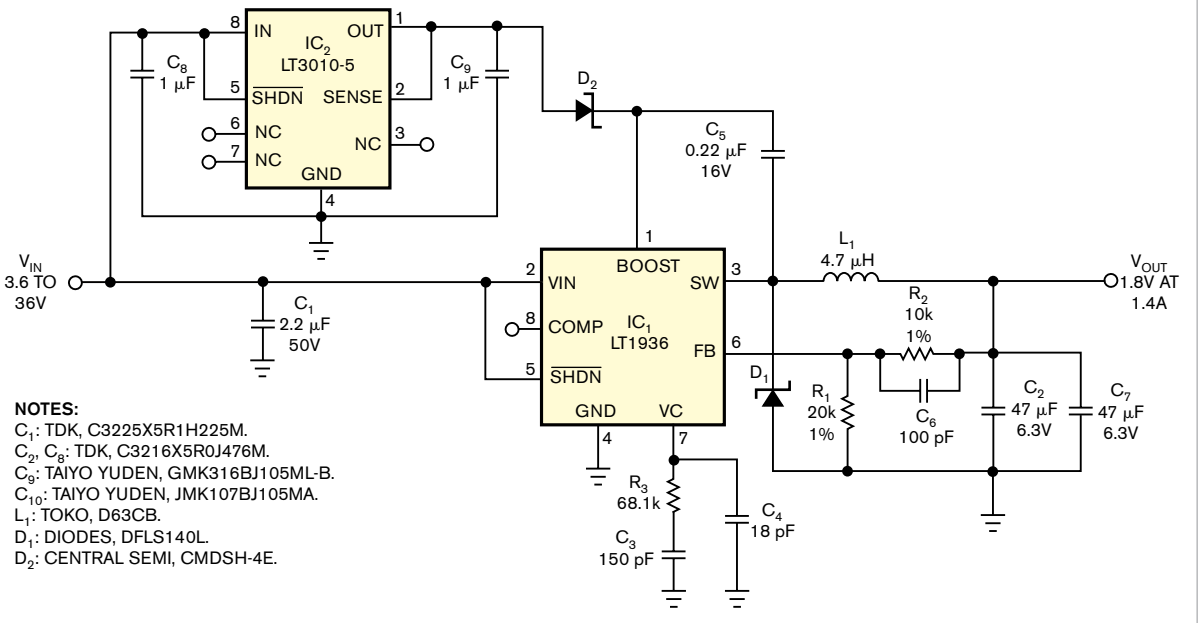


Figure 2 At outputs as low as 1.8V, efficient operation at low input voltages benefits from an added low-dropout regulator, IC_2, for the Boost pin, which extends the circuit's input-voltage range.

age to fully saturate IC_1's switching transistor, and the circuit's efficiency suffers due to increased voltage drop across the transistor. In this situation, connecting D_2's anode to V_{IN} instead of V_{OUT} doubles the Boost pin's voltage to twice the value of V_{IN} but limits V_{IN} to 20V to avoid exceeding the Boost pin's allowable maximum voltage. For outputs lower than 2.8V, the circuit in **Figure 2** extends V_{IN}'s maximum voltage to 36V. When the input exceeds 5.3V, a Linear Technology LT3010-5 low-dropout voltage regulator maintains the voltage across C_9 at 5V. As a result, for input voltages at V_{IN} of 5.3 to 36V, the voltage at the Boost pin always remains at 5V above V_{IN}. **Figure 3** shows a 36V input applied to V_{IN} and the resultant voltages at the SW and Boost pins. In **Figure 3**, the maximum Boost-pin voltage reaches 41V, safely below the pin's 43V maximum rating. For values of V_{IN} of 3.6 to 5.3V, IC_2 operates in dropout mode and introduces only a 300-mV drop from its input to its output. **Figure 4** shows that, even at the circuit's minimum 3.6V input, the Boost pin remains 3.3V above V_{IN}, and IC_1's internal NPN transistor receives sufficient drive voltage for saturated operation. EDN

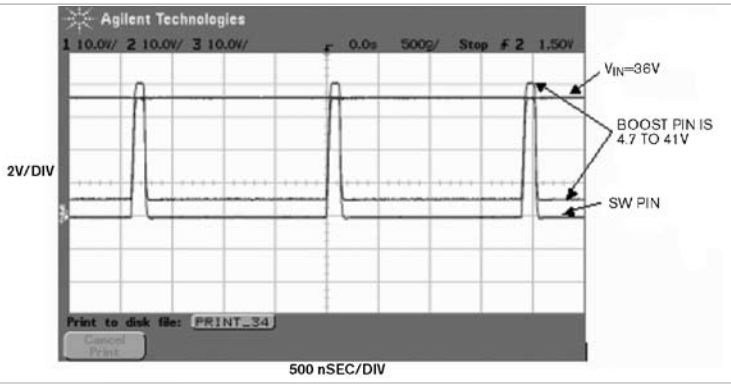


Figure 3 At a maximum input voltage of 36V (V_{IN}), waveforms at the SW and Boost pins show a 5V boost-voltage margin for the circuit of Figure 2.

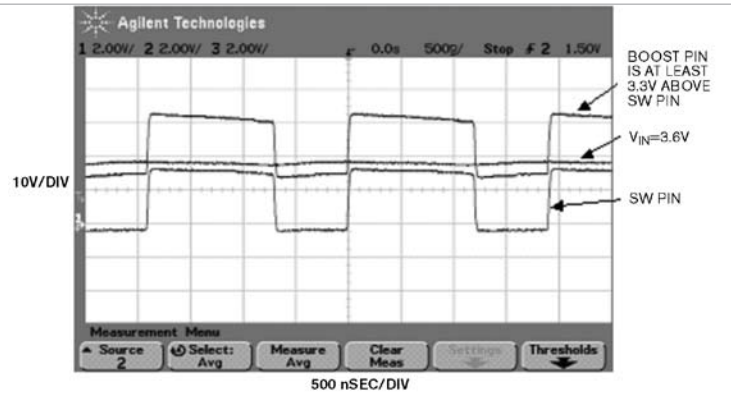


Figure 4 At 3.6V input (V_{IN}) and 1.8V output, a voltage of 3.3V at IC_1's boost pin ensures that IC_1's internal switch still operates in saturated mode.

Automatic latch-off circuit saves batteries

Kieran O'Malley, On Semiconductor, West Kingston, RI

Although rechargeable batteries offer many advantages, they can suffer damage and shortened service lives if they're fully drained of their charge. The circuit in **Figure 1** shuts off a battery-powered appliance—in this instance, an LED flashlight receiving power from NiMH (nickel-metal-hydride) cells—when the battery voltage falls below a preset limit. Although intended for an LED flashlight, this circuit can apply to any battery-powered application. Without ensuring that the user will remove the batteries for recharging, this circuit latches the flashlight off when the battery voltage falls below the usable limit and thus provides a strong hint that it may be time to recharge.

Although a simple nonlatching voltage comparator can switch off power, removing the battery's load causes a voltage rebound, and the comparator restores power, forcing the light into a flashing mode. This circuit turns off the flashlight, and it remains off until the user manually turns on the light using switch S_1.

A 600-mA NCP1421 PFM step-up synchronous-rectifier dc/dc-converter, IC_1, from On Semiconductor (www.onsemi.com) forms the heart of the circuit, but the basic design applies to many other converters offering similar features (**Reference 1**). The NCP1421's key features include an integrated LBI/EN (low-battery input/enable) and an open-drain LBO (low-battery output). Operating from two AA-size NiMH batteries, the circuit comprises the components of a normal boost regulator: an inductor, input and output capacitors, and a current-sense circuit to the right of IC_1. A combination of the LED's forward voltage, which R_3 and R_2 divide down, and voltage across current-sense resistor R_1 produces a feedback voltage for comparison with the NCP1421's 1.2V nominal reference voltage.

On the input side, IC_1's LBI/EN pin connects to the battery through a voltage-divider network formed by resistors R_4, R_5, and R_{10}. The NCP1421 remains enabled while the voltage on LBI/EN exceeds 1.2V. When the voltage on LBI/EN falls below 1.2V, the LBO-detector pin goes low, switching on Q_3 and supplying current to Q_1's base. When Q_1 switches on, Q_2's base goes low and latches the virtual SCR (silicon-controlled rectifier) formed by Q_1 and Q_2, an MBT3946DW1 integrated dual transistor, IC_2.

In addition, Q_1 latches the LBI/EN pin low to prevent IC_1 from turning on again upon load removal. To restart the circuit, switch S_1 must interrupt the circuit's power. Resistors R_4, R_5, and R_{10} set the battery-voltage trip point for the LBO detector. R_5 also sets the current drawn from the battery when the SCR activates. The circuit switches off when the battery voltage drops to approximately 1.3V, a point at which the LBI/EN pin reaches 1.2V. EDN

REFERENCE

1 NCP1421 data sheet, www.onsemi.com/pub/Collateral/NCP1421-D.PDF.

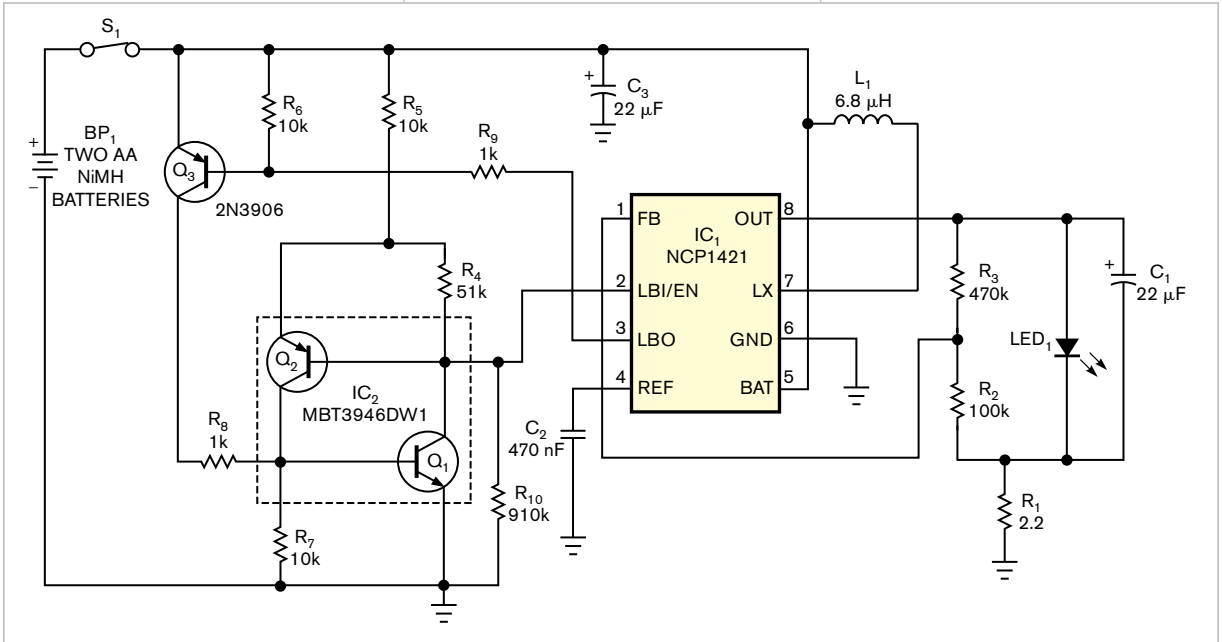


Figure 1 This circuit extends the lives of rechargeable batteries by removing power at a preset voltage and preventing overdischarge.

Switching regulator reduces motor brake's power consumption

Alain Minoz, Elekta Instrument AB, Stockholm, Sweden

For safety reasons, a motor that drives a safety-critical electromechanical assembly often includes an electromagnetic brake on its drive shaft. The brake typically comprises a solenoid coil that actuates a mechanical clutch, and, when you power it, the brake allows the drive shaft to rotate. Although simple and robust, the brake requires a lot of energy to release the clutch and then much less energy to remain actuated.

Measurements show that a brake rated for 24V dc requires a minimum of 18V to release and as little as 8V holding voltage. Substituting those numbers into the equation $P_{COIL}=V^2/R_{COIL}$ shows that, while actuated, the brake consumes less than a quarter of the power required for its initial release. Conversion of excess release power into heat normally doesn't pose problems. However, a precision positioner that uses a brake mounted on a long drive screw can suffer from unacceptable errors if the heat expands the drive screw and alters the assembly's position.

One method of solving the problem involves actuating the brake by applying 24V dc for a brief interval and then reducing the holding voltage to 12V. Under these conditions, the brake dissipates only a quarter of the initial power and thus operates at a reasonable temperature. **Figure 1** shows the influence of actuation voltage on the brake's temperature. As expected, lowering the voltage after actuation drastically lowers the brake's temperature and therefore its effects on the positioning screw.

Figure 2 shows one obvious voltage-reduction approach, which uses relays and a power resistor to halve the voltage applied to the brake. Setting the current-limiting resistance, R_{POWER}, equal to the brake's solenoid resistance, R_{BRAKE}, reveals a few problems. First, the power resistor must dissipate as much power as the brake solenoid's coil. Second, the relays and power resistor occupy considerable space on a pc board. Third, proportioning the values of the R_1C_1 delay circuit's components to achieve a few seconds' delay can prove difficult.

Figure 3 shows another approach, which uses the actuator coil's inductance and replaces relays with an IC. The voltage you apply to the brake need not be continuous, and applying a PWM (pulse-width-modulated) voltage works as well as applying a dc holding voltage because the coil's inductance integrates the current pulses.

A switched-mode voltage regulator can provide an inexpensive and effective PWM-drive voltage. For example, National Semiconductor's (www.national.com) LM2575 adjustable regulator, IC_1, operates over a 7 to 40V range and includes an on/off-control input and a high-impedance feedback input, but any other switching-regulator IC with these two characteristics would also serve. Resistors R_1 and R_2 determine the holding voltage (**Figure 4**). Capacitor C_3 filters the PWM signal to a dc voltage at the feedback input and also maintains the feedback input for a few seconds during start-up at ground, forcing the regulator to deliver the full input voltage to actuate the brake. Diode D_1 quickly discharges the capacitor when the regulator switches off, diode D_2 clamps the switch-off transient voltage that the brake's actuating coil produces, and diode D_3 protects IC_1 against reverse voltage. Photocoupler IC_2 isolates the brake controller from the control circuit.

During start-up, the duration of the regulator's 24V actuation-pulse output fluctuates from 1 to 4 seconds (**Figure 4**). Fortunately, the variation has no impact on the circuit's function but could

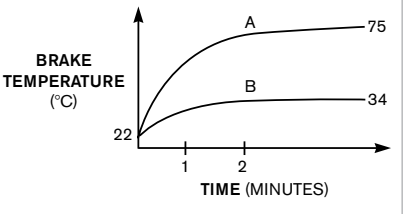


Figure 1 Under continuous operation with 24V applied, the brake's temperature stabilizes at 75°C, or 53°C above ambient temperature (Curve A). Applying a 24V actuation pulse for a few seconds and then applying a 12V holding voltage stabilizes the brake at 34°C, or only 12°C above ambient temperature (Curve B).

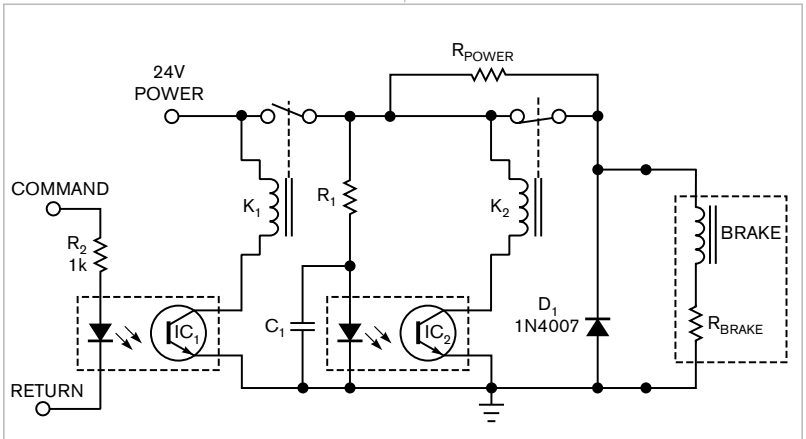


Figure 2 Actuating the brake release trips relay K_1 and applies 24V to the brake. An RC network delays K_2's actuation. When normally closed relay K_2 opens, resistor R_{POWER} reduces the voltage applied to the brake to the holding level.

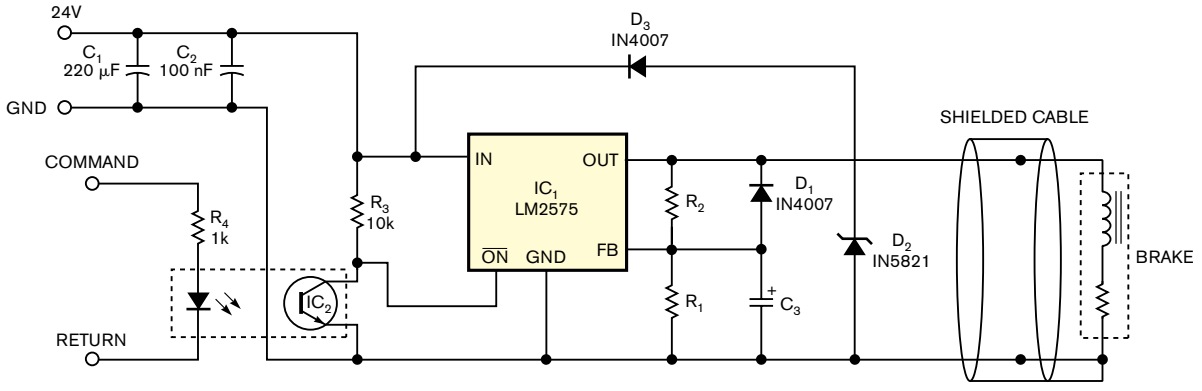


Figure 3 Applying the command input switches on PWM regulator IC_1, and capacitor C_1 holds IC_1's feedback input low, applying a maximum output voltage of 24V to the brake until C_1 fully charges. As the feedback voltage slowly rises to 1.23V, the regulator's output voltage decreases to approximately 12V, the brake's nominal holding voltage.

present a problem if another application requires a precisely timed actuation pulse. After start-up, the regulator delivers a 12V holding voltage, reducing the power demand to one-quarter of the start-up value. As a bonus, the circuit uses inexpensive components, occupies only a few square centimeters of pc-board area, and eliminates the need for two electromechanical relays. Wiring for the PWM-drive voltage can radiate electrical noise unless the circuit is adjacent to the brake. For remote installation, use a shielded twisted-pair cable to minimize noise radiation. EDN

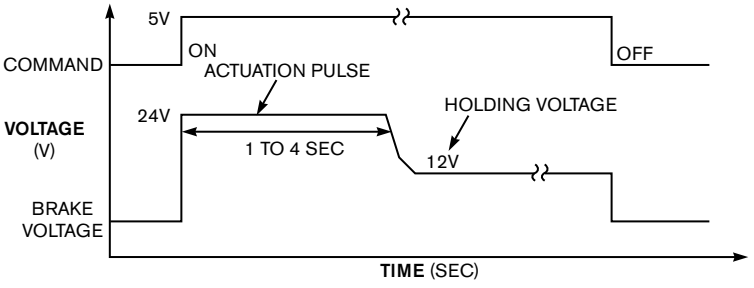


Figure 4 After the actuation pulse applies full voltage to the brake, the regulator's output gradually decreases to the nominal holding voltage.

Analog divider uses few components

David Cripe, Chatham, IL

Although microprocessors may offer more-precise calculations, there's still room for analog-computation techniques in a designer's circuit collection. As a case in point, the analog-divider circuit in **Figure 1** offers reasonably good accuracy for the price of a few inexpensive components. Given two voltages, V_A and V_B, as its inputs, the circuit delivers an output of 5V multiplied by the ratio of V_A divided by V_B. In operation, a TLC555, the CMOS version of the ubiquitous 555 timer, serves as a free-running Schmitt-trigger RC oscillator, IC_2. Its output signal at Pin 3 drives resistor R_1 and capacitor C_1. The voltage at C_1 drives IC_2's trigger (Pin 2) and threshold (Pin 6) inputs, closing the timing loop and establishing oscillation. A low-impedance open-drain MOSFET at IC_2's discharge pin switches low whenever IC_2's output goes low.

Representing the calculation's denominator, an input voltage, V_B, drives IC_2's discharge pin through a resistive-voltage divider comprising R_3 and R_4. Regardless of IC_2's frequency of oscillation, a pulsed voltage appears at IC_2's Pin 7 with the same duty cycle as IC_2's output signal at Pin 3 and an amplitude of 0V to $V_B/2$. A voltage follower, IC_{1B}, buffers IC_2's discharge output and drives a lowpass filter comprising R_8 and C_3, yielding a voltage that equals $V_B/2$ multiplied by IC_2's duty cycle. A second resistive voltage divider, R_6 and R_7, halves the numerator-input voltage, V_A, and applies the signal to integrator IC_{1A}, along with the output from the lowpass filter, R_8 and C_3. The integrator's output voltage drives current through R_2 into C_1, creating a bias voltage that in turn controls IC_2's output pulse width and forming a feedback loop.

In operation, the feedback loop forces IC_2's duty cycle to equalize the voltages at IC_{1A}'s Pin 2 and Pin 3, such that V_B multiplied by the duty cycle equals V_A, or the duty cycle equals the ratio of V_A to V_B. IC_2's output at Pin 3 comprises a 0 to 5V pulse waveform. The feedback circuit controls this waveform and in turn drives a lowpass filter, R_5 and C_4, to generate a dc-output

voltage equal to 5V multiplied by the pulse width, or $V_A \times 5V/V_B$.

Aside from the tolerances of the resistors in divider networks R_3 and R_4 and R_6 and R_7, the primary source for inaccuracy in the circuit arises from the nonzero on-resistance of IC_2's discharge switch and the inability of discharge-switch-voltage follower IC_{1A}'s output to reach 0V. Keeping the circuit's resistance values high tends to reduce this effect. A Spice simulation of this circuit indicates that, aside from the effects of resistor tolerances, the circuit achieves a worst-case accuracy of 0.5%. (Editor's note: For greatest accuracy, use a regulated, 5V power supply.) EDN

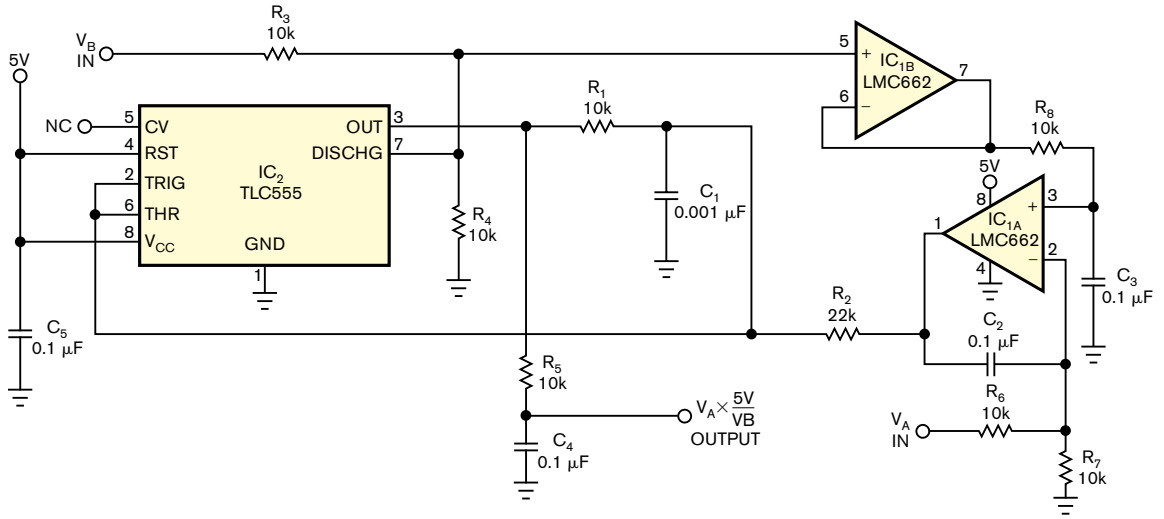


Figure 1 This low-cost pulse-width modulator performs analog division. Inputs V_A and V_B control this low-cost pulse-width modulator, and a lowpass filter follows it.

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Microcontroller drives logarithmic/linear dot/bar 20-LED display

Dhananjay V Gadre and Anurag Chugh,
Netaji Subhas Institute of Technology, New Delhi, India

Available for more than 20 years, National Semiconductor's (www.national.com) venerable LM3914 dot/bar-display driver still enjoys wide popularity among designers. The LM3914 can sense an analog voltage level and display it on 10 LEDs by illuminating one of 10 in dot mode or by progressively illuminating LEDs in bar-graph mode. Recently, an application needed an analog-input-voltage display capable of displaying more than 10 levels in linear- and logarithmic-scale formats. According to the LM3914's data sheet, you can cascade multiple 3914s to display more than 10 levels (**Reference 1**), but, even so, the LM3914 offers only linear displays of its input voltage. (**Editor's note:** National Semiconductor also offers the LM3915, a logarithmic, 3-dB-per-step version, and the LM3916, which displays its input in volume units, for audio applications.)

This application required more flexibility than the LM3914 offers, and it uses a circuit based on an Atmel (www.atmel.com) AVR-family ATTiny13 microcontroller, which features 1 kbyte of program memory; a four-channel, 10-bit ADC; and six general-purpose I/O pins. Altering the circuit's firmware allows linear or logarithmic scaling of the 0 to 5V input-voltage range.

The circuit in **Figure 1** continuously displays the input voltage in 20 levels. When closed, switch S_1 freezes the displayed reading at its then-current level. Five of the microcontroller's six I/O pins control all 20 LEDs and the switch. Configured as an ADC-input channel, the remaining I/O pin receives the analog-input voltage. The microcontroller uses Charlieplexing, a method of using I/O lines to drive as many as N×(N−1) LEDs, to drive 20 LEDs with only five I/O pins (**references 2** through **4**).

The firmware is written in C and compiled using AVR-GCC, a freeware C compiler and assembler available in Windows and Linux versions at www.avrfreaks.net. It uses the Tiny13's internal 10-bit ADC operating in free-

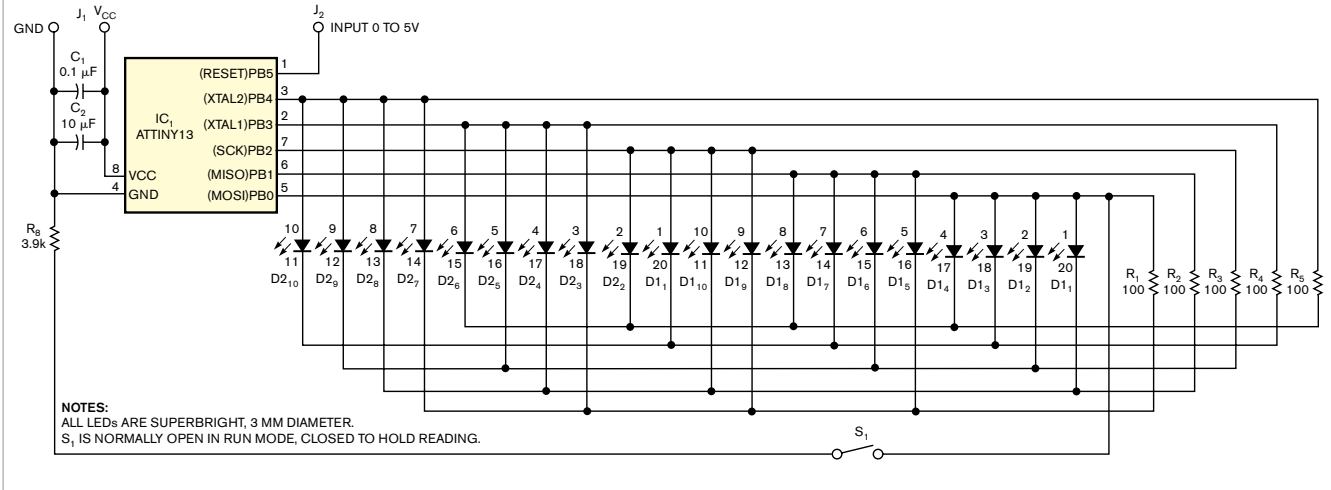

Figure 1 Based on a low-cost microcontroller, this dot/bar LED driver operates in linear or logarithmic modes.

running, interrupt-driven mode to convert the analog-input voltage into a digital number. Upon completion of each conversion, the ADC generates an interrupt that a subroutine reads; the interrupt stores the ADC's converted output in a shared variable.

To provide a flicker-free display, an internal timer generates a 1875-Hz interrupt derived from the 9.6-MHz system clock to drive the multiplexed LEDs at a rate exceeding 90 Hz. Dividing the ADC count by a constant yields a linear display of the input voltage. A look-up table scales the ADC count to produce a logarithmic display. **Figure 2** shows the logarithmic-conversion curve that defines the look-up table's values. Versions of the ATTiny13's control programs for linear and logarithmic scales are available for downloading from the online version of this Design Idea at www.edn.com/070118di1. You can modify the source code to display only a particular subrange of the input voltage of 0 to 5V. For example, you can specify a linear-display range spanning 1 to 3V or a logarithmic scale for input voltages of 2 to 3V. EDN

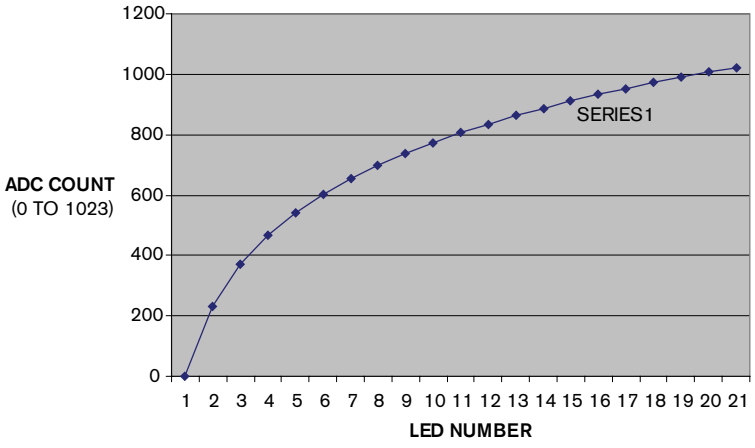

Figure 2 A linear-to-logarithmic-conversion curve defines the input voltage required to illuminate a particular LED.

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Optical feedback extends white LEDs' operating life

Bjoy Santos, Intersil Corp, Milpitas, CA

Regardless of its color, an LED's light output varies as a function of forward current and ambient temperature. As **Figure 1** shows, an LED's light output can vary by as much as 150% over its operating-current range. In response, a designer's first attempt to solve the problem focuses on driving the LEDs with a constant current. The most common white-LED-driver circuits use an inductor-based dc/dc boost-converter topology similar to the circuit in **Figure 2**. A current-feedback controller ensures that the voltage across current-sensing resistor R_1 remains constant. As a result, the controller varies the voltage across the entire string to maintain the LEDs' current constant without regard to

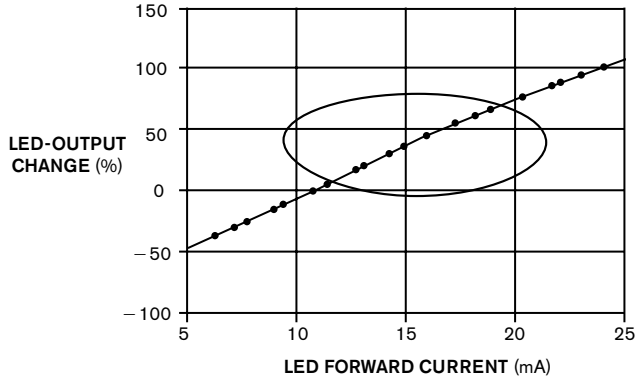


Figure 1 An LED's light output changes considerably as a function of its forward current, even within the sweet spot (oval area) of its nominal operating current.

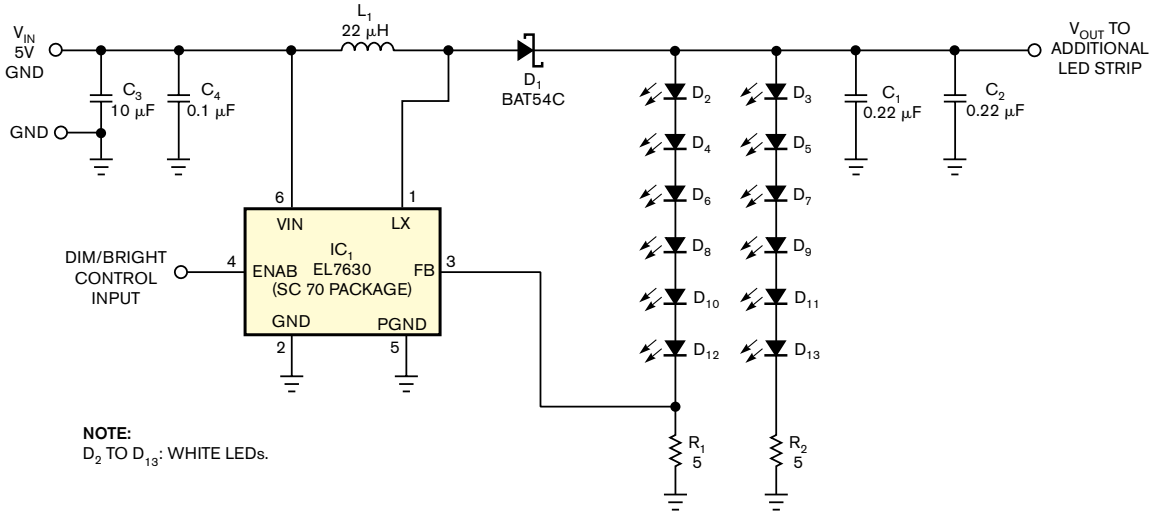
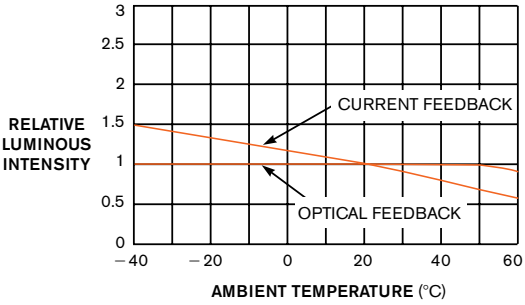


Figure 2 One method of driving an LED illuminator samples current through a string and adjusts the voltage across the entire string to maintain a constant current.

the LEDs' actual light output.

Driving series-connected white LEDs with a current source relies on the assumption that, at constant current, an LED's light output remains constant. Unfortunately, all LEDs exhibit a nonlinear decrease in brightness as a function of operating time. Although less obvious in colored LEDs that find use as indicators, the decrease in brightness of a white-LED-illuminator-array source becomes noticeable over an extended period. Brightness also varies as

Figure 3 Even at a constant forward current, an LED's light output correlates strongly with temperature and can vary by as much as 100% over the entire operating-temperature range (upper curve).



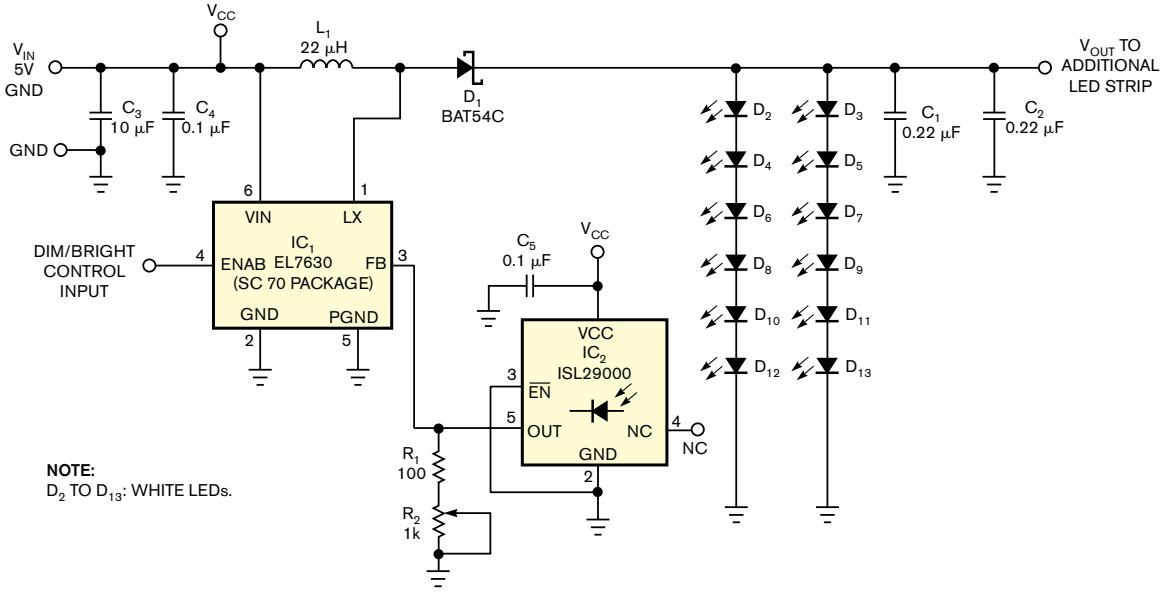


Figure 4 Photosensor IC_2, an Intersil ISL29000, resides near an LED to detect brightness fluctuations and provides compensating feedback to IC_1, the current controller, which is an Intersil EL7630 pulse-width regulator.

a function of temperature, which can affect an illuminator's performance over an extended-temperature range (upper curve, **Figure 3**).

To compensate for LED-output variations due to aging and temperature fluctuations, the control loop needs more information in addition to voltage or current data. Adding an ambient-light sensor and optical feedback to the control loop can ensure that a white LED's light output remains uniform and consistent over time and temperature variations. An optical sensor can measure the LED's light-output intensity and provide a feedback signal for the control loop, which can adjust the current to produce a relatively constant light output. As the LEDs' light outputs decrease, increased current compensates for aging and temperature-induced variations (lower curve, **Figure 3**).

The circuit in **Figure 4** includes an optical-feedback loop based on Intersil's (www.intersil.com) ISL29000 light-to-current optical sensor, IC_2, which senses changes in the LEDs' light output and decreases the feedback voltage applied to IC_1, the current controller, an Intersil EL7630. The pulse-width-modulated controller then increases the LED-drive current's duty cycle, boosting the LED current until the feedback voltage reaches its nominal value. As ambient temperature decreases, the LEDs' light output tends to increase, and IC_2 delivers a higher feedback voltage to the controller, which responds by lowering the duty cycle to decrease the LEDs' current and thereby compensates for the decrease in temperature. EDN

Sequencer controls power supplies' turn-on and turn-off order

Eric Schlaepfer, Maxim Integrated Products Inc, Sunnyvale, CA

When a design based on multiple point-of-load dc/dc converters requires a specific power-supply-start-up sequence, wiring each converter's power-good output to the next converter's enable input produces the desired voltage cascade. Although this approach works well for simple designs, it fails to satisfy a requirement of many modern microprocessors and DSPs: that, during shutdown, the power-supply rails switch off in reverse order. Although various vendors provide programmable-sequencing ICs, these components are usually too expensive for cost-sensitive applications.

Offering an alternative to programmable-sequencing ICs, the circuit of **Figure 1** can sequence and cheaply

(continued on pg 92)

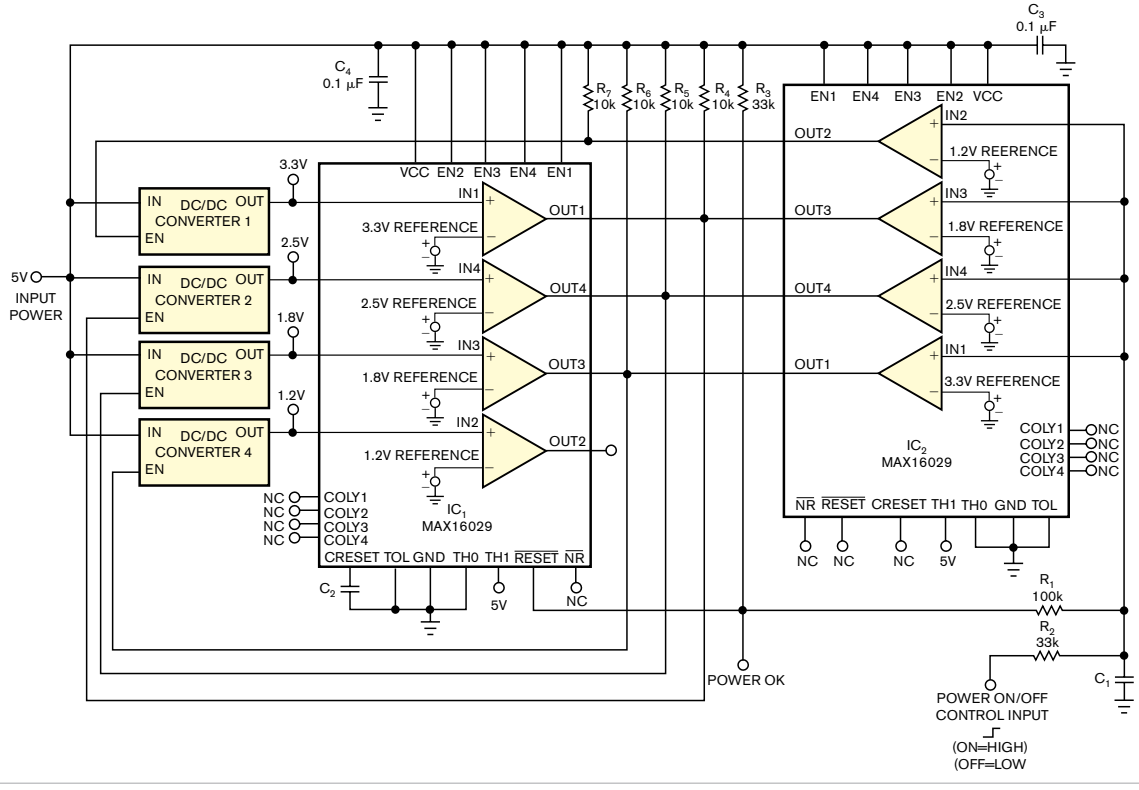


Figure 1 Comprising a pair of inexpensive ICs, this circuit applies four supply voltages in a specified order at power-up and then removes them in reverse order at power-down.

(continued from pg 88)

and effectively monitor four power-supply rails. Four dc/dc power supplies provide the application circuit with 3.3, 2.5, 1.8, and 1.2V. A quad supervisor circuit, IC_1, monitors each rail, generating the master POK (power-OK) signal and ensuring that, during power-up, the next supply in the sequence does not turn on until the preceding supply voltage is valid. Using an RC circuit comprising R_1, R_2, R_3, and C_1, a second quad supervisor, IC_2, creates the power-up and power-down sequences. Each supervisor's internally preset voltage threshold eliminates the need for external resistive-voltage dividers.

Connecting the power-on/off signal to 5V initiates a power-up sequence, which charges C_1 through R_2. As the capacitor's voltage gradually exceeds 1.2, 1.8, 2.5, and 3.3V, each of IC_2's corresponding open-drain outputs floats, thereby allowing the power supplies to turn on in the prescribed sequence. After a time delay, which C_2 sets, and after all four supplies turn on, the POK signal asserts—that is, goes high.

To monitor the supply rails, allow the power-on/off-control input to float. Resistors R_1 and R_3 sustain the voltage across C_1 and maintain the POK signal high to keep the power supplies on. When an output-voltage fault occurs, POK rapidly deasserts, discharging C_1 through R_1 and shutting off all of the power supplies. To remove power in an orderly sequence, connect the power-on/off signal to ground. Capacitor C_1 discharges through R_2 and also through R_1 when POK deasserts, turning off each power supply in reverse order (**Figure 2**).EDN

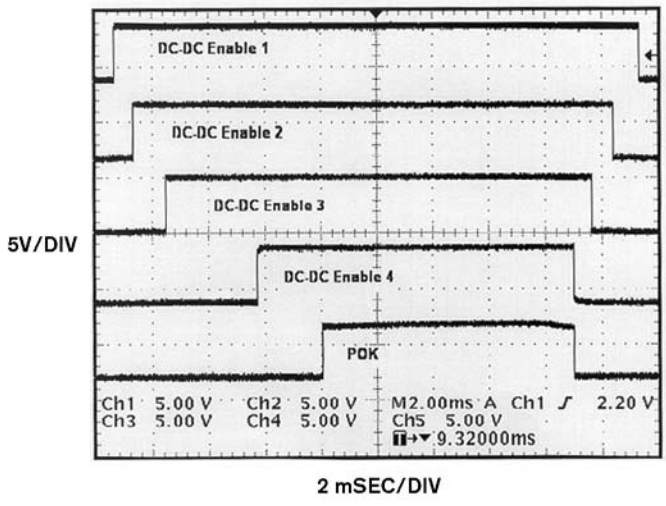


Figure 2 Beginning with a dc/dc converter, the circuit in Figure 1 switches on three additional converters in sequence and generates a POK signal. Pulling the circuit's on/off input low removes the POK signal and switches off all four converters in reverse order.

Use dual op amp in an instrumentation amp

Jerald Graeme, Burr-Brown Corp, Tucson, AZ

Editor's note: *Here's an oldie but goodie. EDN editors regularly field requests for copies of articles that predate our online archives (www.edn.com/archives). But this Design Idea from our Feb 20, 1986, issue has generated many more requests than normal. We aren't sure how readers know of this Design Idea, but its enduring popularity has led us to publish it once again, and now it will be available in our online archives.*

Although monolithic instrumentation amplifiers are more cost-effective than their discrete and modular predecessors, the limited variety of monolithic instrumentation amps restricts their use. You can widen your options, however, by deriving the differential response of an instrumentation amplifier from a dual op amp (**Figure 1**). The circuit uses FET-input op amps to provide lower noise and lower input-bias currents than monolithic instrumentation amps can offer.

In **Figure 1**, feedback networks for the two op amps are interconnected to establish IC_{1B} as an inverting amplifier in the feedback path of IC_{1A}. Each amplifier provides an external signal input with the high impedance expected of an instrumentation amplifier. (Input-bias currents for this circuit are 2 pA at 25°C.)

Feedback from each amplifier forces a voltage $(V_1 - V_2)$ across the gain-setting resistor R_G. Signal current in the combined feedback path is thus proportional to the differential input voltage and inversely related to R_G. The output voltage, V_{OUT}, equals $G(V_1 - V_2)$—that is, $V_{OUT}=2(1+R/R_G)(V_1 - V_2)$.

You choose R_G for the desired gain G, which may range from a value of 2 (R_G omitted) to a maximum that is limited only by the op amps' open-loop gain, the allowable gain error, and the required bandwidth. The **Figure 1** circuit provides a 2-kHz bandwidth at a gain of 2000; in general, the bandwidth is about 2 MHz/G. What's more, the output offset equals the difference in op-amp offsets multiplied by G.

The dc CMR (common-mode rejection) is an important spec for instrumentation amps; in **Figure 1**, CMR depends primarily on matching values for the four resistors labeled R. DC CMRR

(common-mode rejection ratio) is the reciprocal of the net fractional resistor mismatch; that is, 10,000-to-1 (−80 dB) for a 0.01% mismatch. AC CMR, on the other hand, is limited by the op amps' unequal feedback factors. The network within the shaded region lets you compensate for the effect of unequal feedback factors where necessary—in applications in which the frequency of common-mode voltage exceeds the useful frequency range for signals.

Finally, note that op amp IC_{IB}'s output (the combined differential and common-mode signals) has a wider swing than V_{OUT}. Consequently, this output—equal to $2V_1+(R/R_G)(V_1-2V_2)$—must remain within the op amp's common-mode range to ensure linear operation. EDN

Correction: In the print version of the Dec 15, 2006, Design Idea "Magnetic-field probe requires few components," we inadvertently omitted the byline of one of the Design Idea's primary authors: Sandeep M Satav. You can read this Design Idea and see the correct bylines online at www.edn.com/article/CA6399102. We apologize for the error.

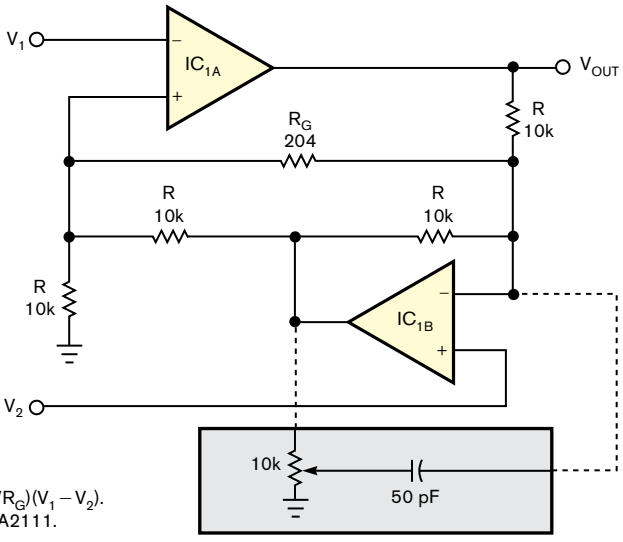


Figure 1 You can build an instrumentation amplifier by providing a common feedback path for the two sides of a dual op amp.

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READERS SOLVE DESIGN PROBLEMS

Simple circuit allows long PWM soft starts

Robert N Buono, Aeolian Audio LLC, Bloomfield, NJ

Available from multiple sources, the UC384X family of current-mode, PWM (pulse-width-modulated) power-supply controllers offers good performance and has spawned a variety of similar ICs. All members of the UC384X family and its variants share a common characteristic—an internal voltage-error amplifier that provides a current-limited output. Designated as the COMP pin, the amplifier's output provides a convenient connection for applying compensation to ensure overall feedback-loop stability. In addition, the COMP pin allows attachment of shutdown and soft-start circuitry and serves as a convenient point for setting an external power switch's output-current-limit threshold.

Two of the COMP pin's characteristics enhance its versatility: First, the pin delivers limited output current, and, second, the pin's voltage is directly proportional to the current flowing through an external power switch. Both features also allow the pin to serve as a control port. For example, perhaps the most common application for the pin involves addition of a soft-start feature to a UC384X-based power-supply design.

In soft-start mode, an external power switch's output current and the power supply's output voltage ramp up at a rate controlled by, and proportional to, the voltage at the COMP pin. **Figure 1** shows a typical soft-start circuit's implementation comprising a small-signal PNP transistor, Q_1, connected to the COMP pin. An RC network, R_1 and C_{SS}, drives Q_1's base from IC_1's internally generated, 5V precision-reference source.

When the external power-supply voltage, V_{DD}, exceeds IC_1's internally preset UVLO (undervoltage-lockout) threshold, the 5V reference source switches on. The voltage on C_{SS} ramps upward toward 5V at a rate that the time constant, τ, of $R_1 \times C_{SS}$ determines in seconds. Given Q_1's emitter-follower configuration, Q_1 applies the COMP pin's voltage, which "follows" Q_1's base voltage, and the power supply's output current ramps up proportionally.

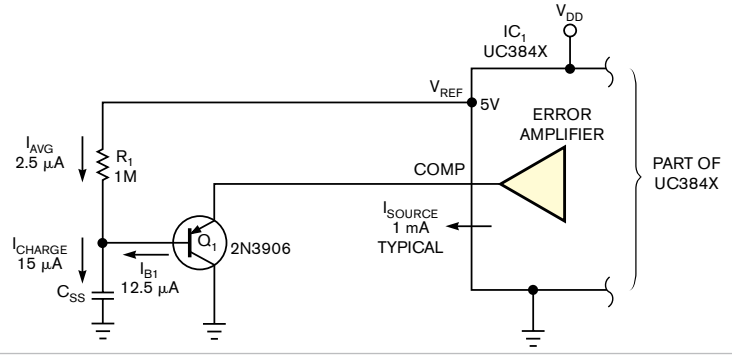

Figure 1 A single transistor, Q_1, implements a switching regulator's slow-start-up feature, but its base current introduces a timing error.

The simple circuit in **Figure 1** satisfies the requirements of many soft-start applications. To obtain longer soft starts, you can increase C_{SS} or increase R_1 to decrease C_{SS}'s charging current. However, increasing either component can cause problems. Depending on the construction of capacitor C_{SS}, its leakage current may be significant. Also, you can no longer ignore Q_1's base current. For example, a survey of PWM-control-IC designs shows that the COMP pin typically sources an output current of 1 mA. If Q_1, a 2N3906, provides a minimum beta of 80, Q_1's base draws a minimum current of 12.5 µA. The base current flows from the base pin of Q_1 and adds to C_{SS}'s charging current. If the circuit in **Figure 1** uses a 1-µF capacitor for C_{SS} and a 1-MΩ resistor for R_1, you would expect a nominal 1-second charging-time constant and an average charging-current flow of 2.5 µA through R_1. However, the charging current actually totals 15 µA—the sum of the 2.5-µA charging current plus Q_1's 12.5-µA base current, and the soft-start time falls considerably short of the nominal value.

As an alternative, the circuit of **Figure 2** better satisfies designs such as

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battery chargers that require a longer soft start or a more accurately timed soft-start ramp. Adding a second transistor to form a PNP-NPN compound transistor maintains the slow-start function. The circuit's composite current gain (beta) consists of the product of Q_1's and Q_2's current gains, or 70×60=4200, which greatly exceeds the single transistor's current gain of 60. The higher current gain reduces the charging current's base-current component to only 338 nA. **Figure 3** compares the responses of both circuits. The dark-green trace shows that the circuit of **Figure 2** produces the expected 1-second soft-start time interval, and the light-green trace illustrates **Figure 1**'s too-brief start-up time. Although the circuit of **Figure 2** yields a more accurate soft-start ramp, it also allows the use of smaller capacitors, such as multilayer ceramics, to reduce pc-board area and component cost.

Although a Darlington-connected transistor pair would also provide high current gain, its output transistor cannot saturate—a prerequisite for keeping the off-state voltage at IC_1's COMP pin below 1V. The PNP transistor, Q_1 in the PNP-NPN compound connection in **Figure 2** can saturate, and the NPN transistor, Q_2, maintains its voltage-controlled saturation voltage at significantly less than 1V over the circuit's operating-temperature range. EDN

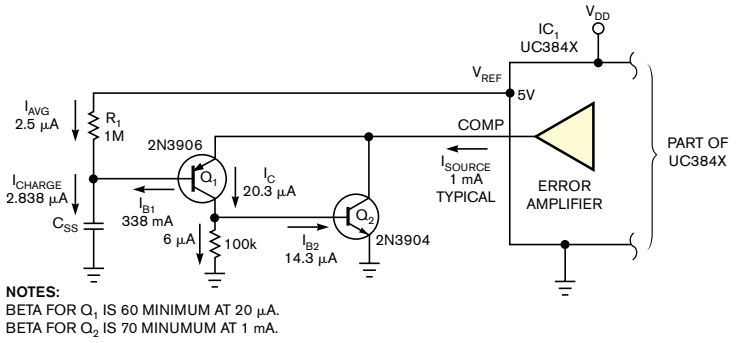

Figure 2 Replacing Q_1 in Figure 1 with a PNP-NPN compound-transistor pair dramatically reduces the circuit's start-up-ramp-timing error.

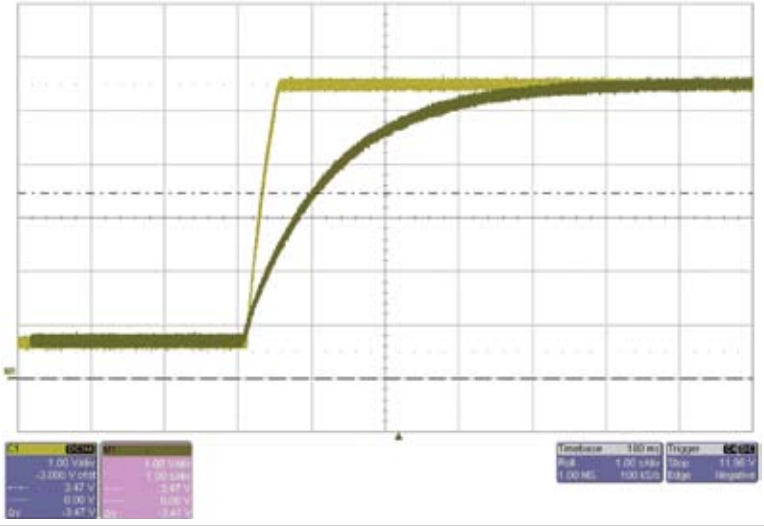

Figure 3 The dark-green trace shows that the circuit of Figure 2 produces the expected 1-second slow-start time interval, and the light-green trace illustrates Figure 1's too-brief start-up time. (The 1τ measurement equals 1 second.)

Open-door alarm prevents accidental defrosts

Tom Lyons Fisher, Juniata College, Huntingdon, PA

Laboratory refrigerators and freezers often contain very valuable materials. Some units include overtemperature alarms that typically don't sound until thawing has already damaged the units' contents or sound when no one is around to hear the warning. Rather than a power outage, the most frequent cause of thawing disasters involves a failure on someone's part to properly close the freezer's door. This Design Idea describes an alarm that provides a timely open-door warning that can prevent an expensive incident.

A decade ago, a designer would have based this circuit on a type-555 timer IC, but, today, a small microcontroller provides a less expensive approach. The alarm in **Figure 1** detects an open refrigerator or freezer door by means of a magnetic proximity switch that's available from Radio Shack (www.radioshack.com) as an intrusion-alarm-system component. The circuit allows the door to remain open for a software-selectable interval—in this instance, 20 seconds—before activating a piezoelectric buzzer that conserves battery power by sounding for only 1 second of every 5.

A low-dropout voltage regulator, IC_1, an STMicroelectronics (www.st.com) L4931CZ50, provides 5V regulated power for IC_2, a Microchip (www.micro

chip.com) PIC10F200. Because IC_2 "sleeps" between door openings and voltage regulator IC_1 consumes little quiescent current, the 9V alkaline battery that powers the circuit offers a projected life of approximately one month. When you activate the buzzer, it consumes approximately 2 mA, a drive current that's directly available from the microcontroller's output port. At this current level, only an unencased piezoelectric element provides a sufficiently loud warning. In high-noise environments, you can use a solid-state relay or a logic-level MOSFET to drive the buzzer directly from the 9V battery.

You can attach the normally open switches and their actuation magnets to the refrigerator or freezer using double-sided adhesive-foam tape. The switches are sensitive to magnet orientation and position, making it easy to find a mounting configuration that can detect a door that's open by as little as 2 mm. Source code for the microcontroller is available for downloading from the online version of this Design Idea at www.edn.com/070201di1. EDN

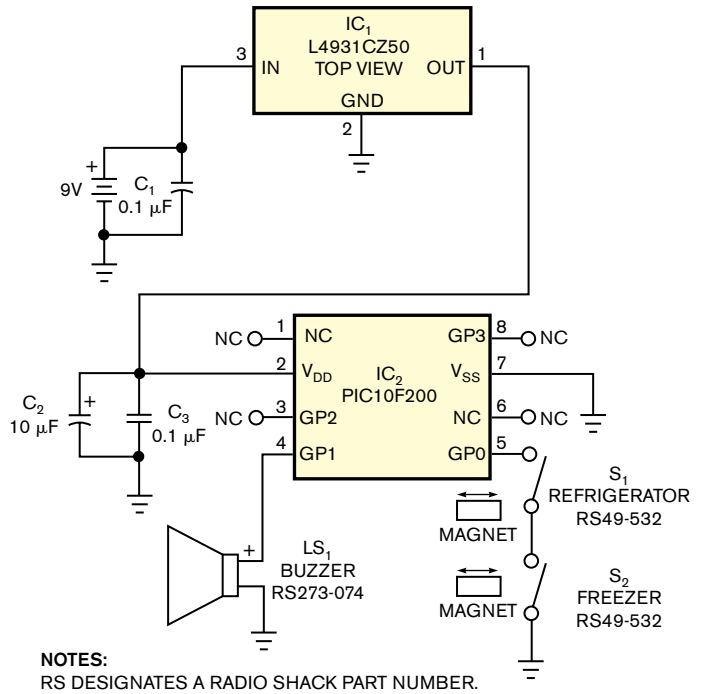

Figure 1 This circuit protects the contents of a laboratory freezer or refrigerator by sounding an alarm when a door opens.

LED drivers minimize power dissipation

Fons Janssen, Maxim Integrated Products Inc, Bilthoven, Netherlands

One option for driving high-brightness LEDs uses the standard stepdown buck converter (**Figure 1**). The sense resistor, R_S, generates a feedback voltage, V_{FB}, that sets the desired LED current, I_{LED}, according to the equation $R_S=V_{FB}/I_{LED}$. Unfortunately, most buck converters require a relatively high feedback

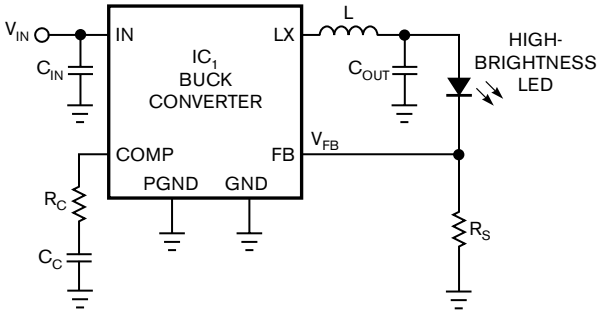

Figure 1 A generic buck converter, IC_1, provides constant-current drive for a high-brightness LED.

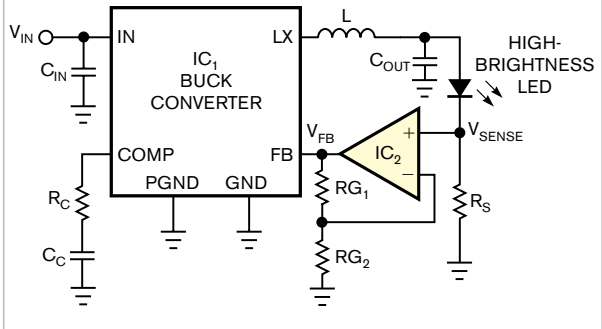

Figure 2 An op amp, IC_2, increases the LED-current error signal and reduces power dissipation in the sense resistor.

voltage on the order of 1V, which dissipates high power in the sense resistor ($P_{SENSE}=V_{FB}/I_{LED}$). Reducing the sense resistor's value and adding an op amp to boost the sensed voltage reduces the power penalty (**Figure 2**). In some cases, you can eliminate the op amp by using a stable reference voltage, which is available on some converter ICs, to pull up the sense voltage (**Figure 3**).

THE VARIATION OF LED CURRENT AVERAGES APPROXIMATELY 5 mA OVER AN INPUT-VOLTAGE RANGE OF 4 TO 5.5V.

The switching converter, a Maxim (www.maxim-ic.com) MAX1951, requires a feedback voltage of 800 mV and provides a 2V reference voltage at the reference pin. Connecting R_1, a 50-kΩ resistor, between R_S and V_{FB}, and R_2, a 100-kΩ resistor, between the reference and the feedback pins shifts the operating point from 200 mV at R_S to 800 mV at the feedback pin:

$$V_{FB} = V_{REF}\frac{50k}{50k+100k} + V_{SENSE}\frac{100k}{50k+100k} = 0.667V + {}^{2}/_{3}(V_{SENSE}).$$

Thus, for V_{SENSE}=0.2V, V=0.8V. For the cost of two inexpensive resistors, power dissipation in the sense resistor diminishes by a factor of four.

Using the Luxeon K2 LED from Lumileds (www.lumileds.com), power measurements on the circuits of **figures 1** and **3** illustrate how the feedback adjustment influences power that the LED driver delivers. Two graphs illustrate LED currents and voltages as a function of input voltage for a half-load of 400 mA (**Figure 4**) and a full load of 800 mA (**Figure 5**). As you would expect, the current regulation deteriorates at half-load. The variation of LED current averages approximately 5 mA over an input-voltage range of 4 to 5.5V and 1 mA for the circuit

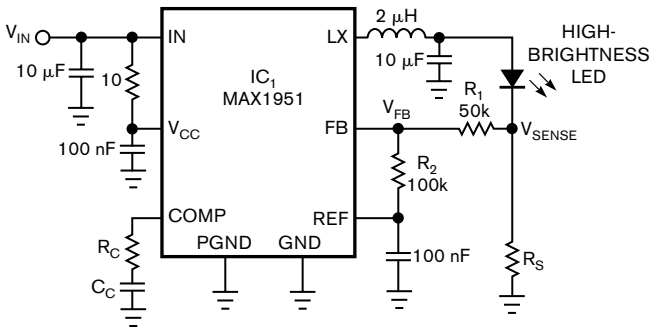

Figure 3 Adjusting the feedback signal improves the efficiency in this buck-converter driver for high-brightness LEDs.

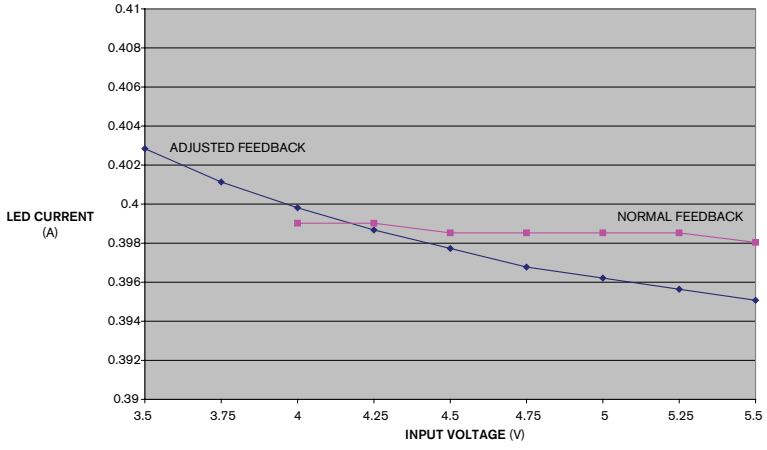

Figure 4 This graph shows LED current as a function of input voltage at half-load for the circuit of Figure 3.

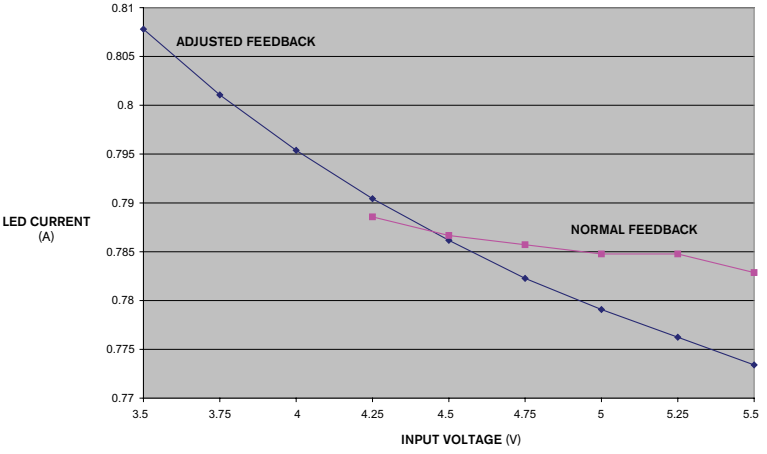

Figure 5 This graph shows LED current as a function of input voltage at full load for the circuit of Figure 3.

with normal feedback. The input-voltage range, however, increases by more than 0.5V. Regulation also deteriorates for full load, and the variation increases to approximately 22 mA versus 6 mA for the circuit with normal feedback (**Figure 6**). Again, the adjusted-feedback circuit of **Figure 3** increases the input-voltage range.

You can define the improvement in efficiency, η, as follows:

$$\eta = \frac{V_{LED} \times I_{LED}}{V_{IN} \times I_{IN}}.$$

The buck converter's power-conversion efficiency and power dissipated in the sense resistor determine the circuit's efficiency. As **Figure 5** shows, the adjusted feedback of **Figure 3** increases the efficiency more than 10% at either half-load or full load. Assuming that the sense voltage doesn't change, efficiency improves for lower output-current loads because the sense resistor dissipates less power. EDN

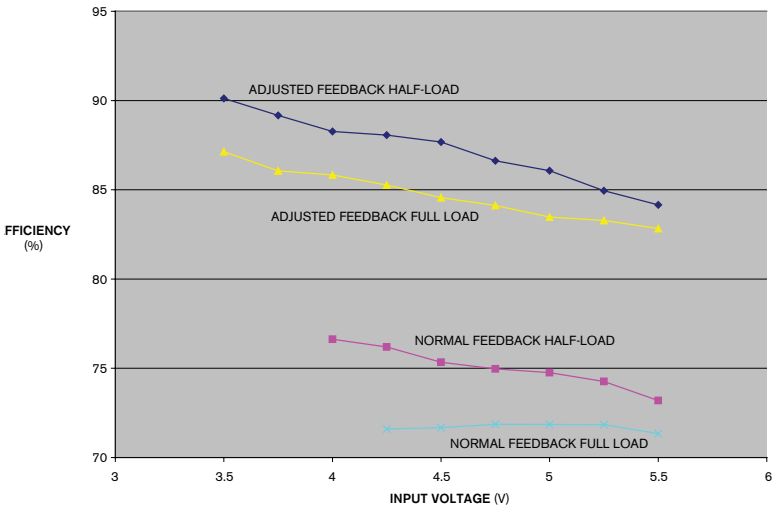

Figure 6 A comparison of a normal-feedback circuit (Figure 1) and an adjusted-feedback circuit (Figure 3) shows significant improvements in overall efficiency at half-loads and at full loads.

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Gain-of-two instrumentation amplifier uses no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

An instrumentation amplifier offers precise gain without feedback resistors, and, at any value of gain, it provides high input impedances at its noninverting and inverting inputs. In a typical IC instrumentation amplifier, a single resistor that connects across two gain-adjustment pins determines the circuit's overall gain. Integrated versions of most instrumentation amplifiers allow the pins to remain open for unity gain but require finite-value gain-setting resistors for gains exceeding one. Although the gain-adjustment resistor might comprise a tiny surface-mounted device, its electrodes and internal resistive layer extend the conductive surface connected to the IC's gain-adjustment pins. The extended surface acts as an antenna and thus makes the amplifier more susceptible to stray external electromagnetic fields.

Figure 1 shows an instrumentation amplifier that offers a gain of two without using any external resistors. The circuit comprises a cascade of a symmetrical, differential-output amplifier, formed by two channels of IC_1; an Analog Devices (www.analog.com) AD8222 instrumentation amplifier; and a difference amplifier comprising one half of IC_2, a second AD8222. All three instrumentation-amplifier sections in the circuit provide a standalone gain of one. Because the differential outputs of the first stage have opposite signs, their difference is twice

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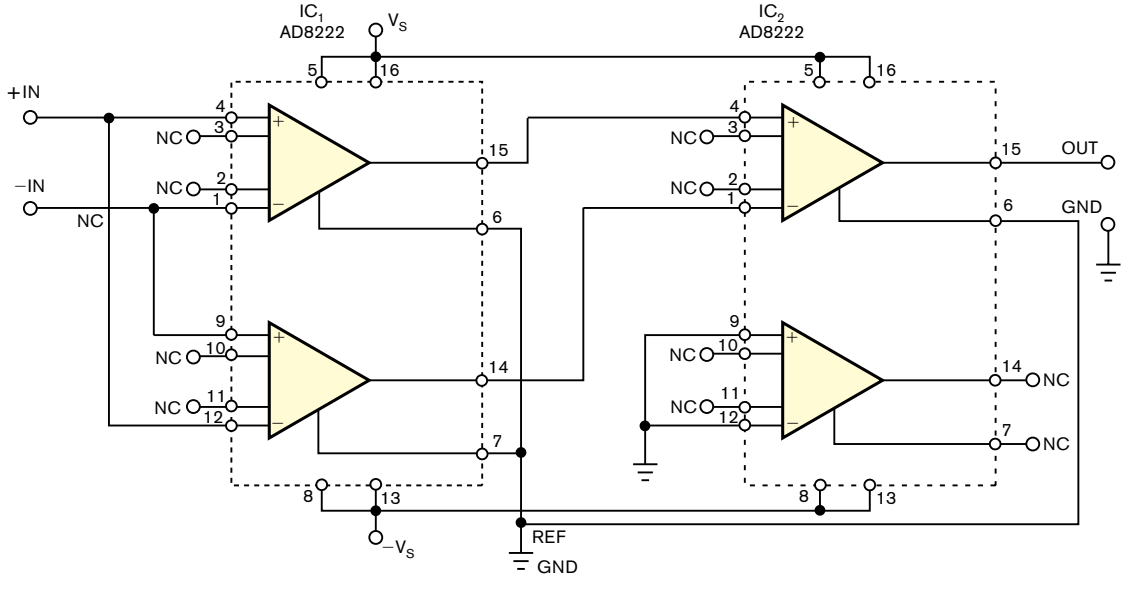

Figure 1 Based on two dual-section instrumentation amplifiers, this composite instrumentation amplifier offers a gain of two with an error margin of less than 0.06% and requires no gain-setting resistors.

that of the difference of the input signals.

The circuit's worst-case gain error does not exceed the value of $\delta_2=3\delta_1$, where, at a gain of one, δ_1 represents the maximum gain error of one section of the AD8222. For B-grade ICs, you calculate the value of δ_2 as $\delta_2 \leq$ 0.06% (**Reference 1**). Typically, the value of δ_2 rarely reaches its maximum value. Given the reasonable assumptions that all three amplifiers' gain errors are independent and obey a gaussian distribution, the probability of occurrence of $\delta_2=3\delta_1$ is about 1/20 the probability of encountering a single amplifier that has a maximum gain error of δ_1.EDN

REFERENCE

1 "AD8222 Precision, Dual-Channel Instrumentation Amplifier," Analog Devices Inc, www.analog.com/en/prod/0,2877,AD8222,00.html.

Analog switch converts 555 timer into pulse-width modulator

Jordan Dimitrov, Tradeport Electronics, Vaughan, ON, Canada

This Design Idea describes a new approach to producing a variable-duty-cycle waveform from a 555-based free-running oscillator. The circuit's wide modulation range, highly linear control over a wide range of duty-cycle values, and excellent linearity make it ideal for PWM (pulse-width-modulation)-based control applications. **Figure 1** shows the basic circuit, which works as follows: When IC_1's output goes high, switch S_1 closes, and IC_1's internal discharge, switch S_2, opens. Capacitor C_1 charges through R_1 and R_2. When IC_1's output goes low, S_1 opens, and S_2 closes, discharging C_1 through R_2 and R_3.

The generic configuration works well for producing a fixed-value duty cycle.

(continued on pg 86)

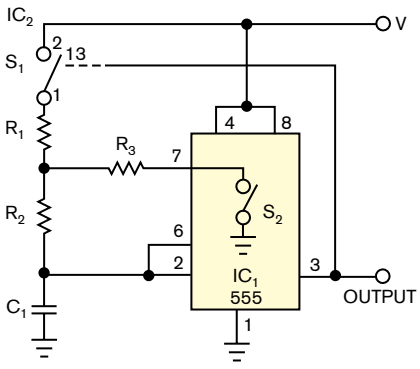

Figure 1 An external analog switch and a 555 timer provide a free-running oscillator with a fixed duty cycle.

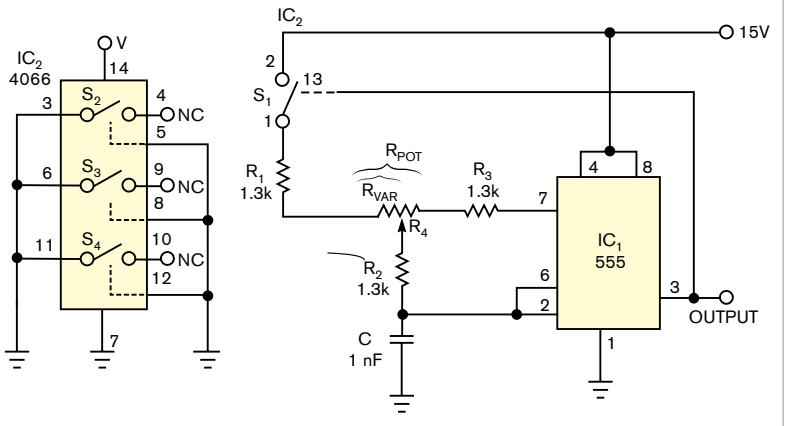

Figure 2 Add a potentiometer, R_4, to produce an output pulse that has a manually variable duty cycle.

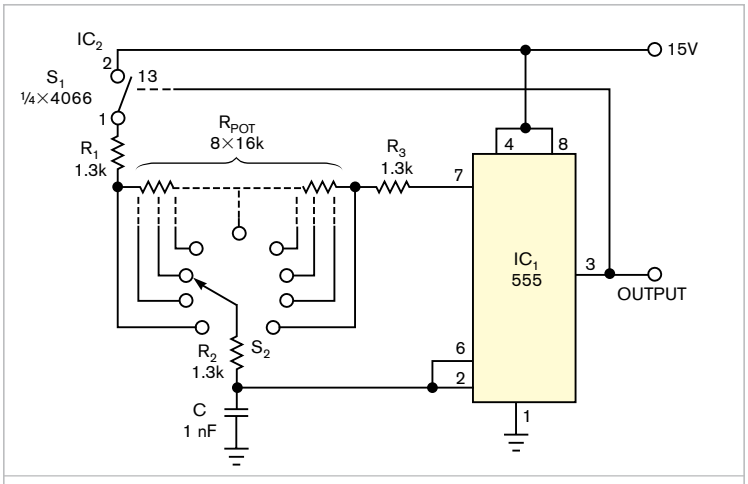

Figure 3 To obtain fixed-duty-cycle values for linearity evaluation, you can replace the potentiometer with a rotary switch and a series-connected string of precision resistors.

To obtain a continuously variable duty cycle, **Figure 2** shows how to connect potentiometer R_4 to the common junction of R_1, R_2, and R_3. The output waveform's duty cycle, D_TC, follows the equation: $D_TC=(R_1+R_2+R_{VAR})/(R_1+2R_2+R_3+R_{POT})$, where R_{POT} is the potentiometer's end-to-end resistance, and R_{VAR} is the fraction of R_{POT} between the rotor and R_1. As the equation shows, D_TC depends linearly on R_{VAR}. Switch S_1 comprises one section of a 4066 CMOS quad bilateral SPST switch, IC_2.

You can use the circuit in **Figure 3** to evaluate duty-cycle linearity. A rotary switch and a tapped series string of 16-kΩ resistors provide a 10-kHz signal with nine discrete, equally spaced duty-cycle values ranging from 2 to 98%. For accurate results, use a 5½-digit multimeter to match the values of resistors R_4 through R_{11} and a Tektronix 3012 oscilloscope or equivalent to gather D_TC data.

Microsoft's (www.microsoft.com) Excel-spreadsheet software includes a linearity analysis that returns the following trend line for the duty-cycle measurements: $D_TC=0.7565\times R_{VAR}+2.1548$; $R^2=1$. The value of 1 for R^2 as Excel calculates shows that the transfer function is perfectly linear. Switch S_1's on-resistance and particularly its leakage current slightly affect the D_TC-versus-R_{VAR} equation's slope and intercept, but the equation remains strictly linear. Using only one of IC_2's four switches eliminates leakage effects and crosstalk that would occur if other circuits used the remaining switches. In addition, using moderately low values for the resistor network further reduces leakage-current effects on circuit performance. EDN

Drive a blue LED from a 3V battery

Sergi Sánchez, Federal Signal Vama SA, Vilassar de Dalt, Spain

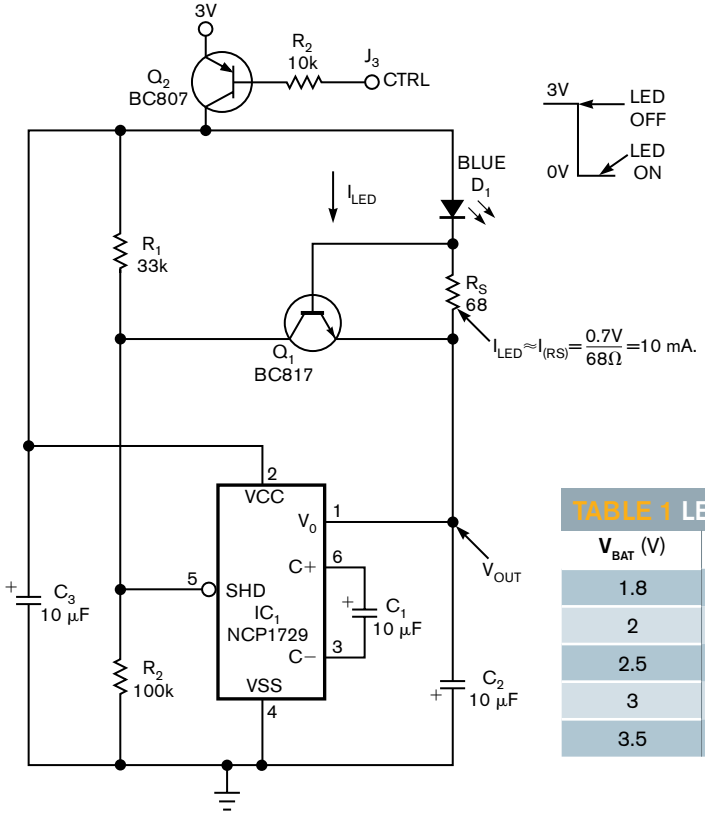

Figure 1 This circuit uses the On Semiconductor NCP1729 voltage inverter, IC_1, to produce enough voltage to drive blue LED D_1.

Using a blue LED can pose problems when available power-supply voltages don't meet or exceed the LED's 3V forward-voltage drop. This Design Idea shows how to drive a blue LED from a 3V battery or another power supply. The circuit in **Figure 1** uses the On Semiconductor (www.onsemi.com) NCP1729 voltage inverter, IC_1, to produce enough voltage to drive blue LED D_1. Transistor Q_1 serves as a constant-current limiter for the LED's forward current. When current through the LED and R_S increases to a level that develops enough base-emitter voltage to turn on Q_1, Q_1's collector draws current from the voltage divider comprising R_1 and R_2 and forces IC_1 to shut down. The voltage inverter restarts when the voltage drop across R_S falls below Q_1's base-emitter turn-on threshold. Pulling transistor Q_2's base to ground through R_2 turns on the circuit.

TABLE 1 LED APPLIED VOLTAGE

V_{BAT} (V)	V_{OUT} (V)	$V_{BE(Q1)}$ (V)
1.8	−1.5	0.41
2	−1.37	0.46
2.5	−0.79	0.42
3	−0.27	0.4
3.5	0.23	0.41

In this application, the LED exhibits a voltage drop of approximately 3.3V at 10 mA forward-bias current. **Table 1** illustrates the LED's applied voltage, $V_{BAT}+|V_{OUT}|$, and Q_1's base-emitter voltage for various battery-voltage values. EDN

Add simple disable function to a panoramic-potentiometer circuit

Lawrence Mayes, Malvern, United Kingdom

In audio-mixing applications, one frequently required function involves mixing a monaural or single-channel source into a stereo-sound field. Audio engineers refer to a panoramic-potentiometer circuit as a circuit that generates left and right signals of correct amplitudes from a monaural signal and places the signal's image anywhere in a stereo-sound field. For the image's loudness to appear independent of its final position, the derived left and right signals must add to produce a constant-power signal rather than a constant-voltage signal.

The widely used circuit in **Figure 1** performs this function by dividing the monaural signal between the two stereo channels and varying each channel's gain between zero and M such that at R_7's centered position, each channel's gain is 0.707M. If you calculate component values to achieve these conditions, then the circuit presents the remarkable property that, for all positions of R_7's wiper, the sum of the powers in the left and right channels is constant to within 0.19 dB.

You can use a DPDT switch, S_1, to bypass the circuit and thus remove it from the audio chain (**Figure 2**). As an alternative, you can add two resistors and use an SPST switch to disable or enable the circuit. The circuit in **Figure 3** presents the same gain characteristics as in **Figure 1**. Closing switch S_1 enables the panoramic-potentiometer function, and opening the switch produces a fixed central-sound image. Additionally, from a practical viewpoint, the circuit of **Figure 3** simplifies wiring and introduces no significant switching transient because enabling the panoramic-potentiometer function involves only grounding R_7's wiper. Even when you use preferred-value components and disregard component tolerances, the circuit introduces a maximum gain error of only 0.21 dB. EDN

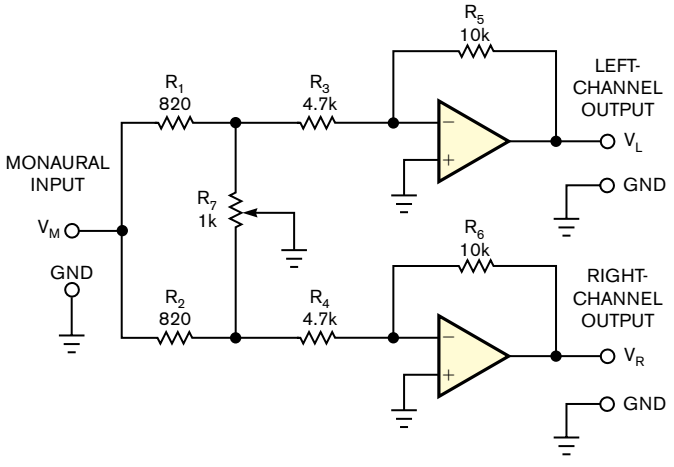

Figure 1 In this basic panoramic-potentiometer circuit, the position of R_7's wiper controls the position of a monaural image in a stereo audio signal.

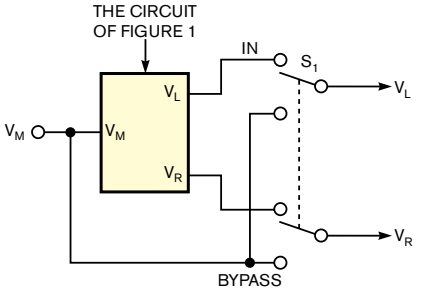

Figure 2 A DPDT switch removes the panoramic potentiometer but introduces wiring complexity and transients.

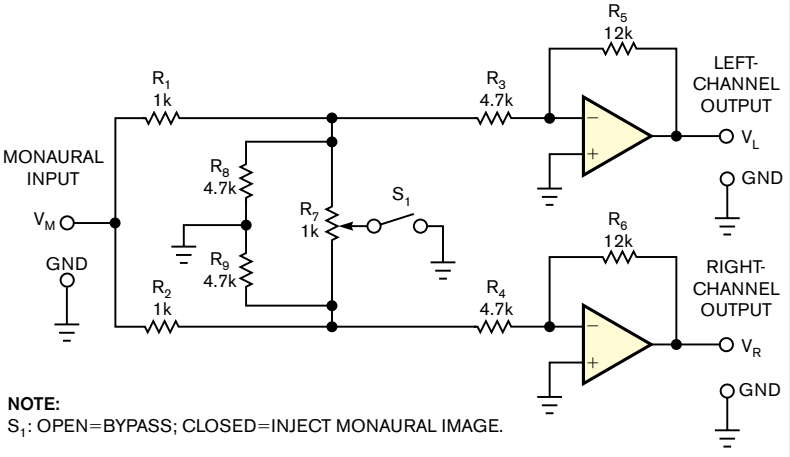

Figure 3 Adding resistors R_7 and R_8 and SPST switch S_1 simplifies wiring and minimizes transients.

Simple single-cell white-LED driver uses improvised transformer

Jim Grant, Scientific Controls, Orlando, FL

A white LED delivers a wide color spectrum and better visibility than do monochromatic LEDs. However, a white LED presents a higher forward-voltage drop than do its colorful counterparts and thus poses problems for operation from a single 1.5V cell. The self-oscillating step-up converter in **Figure 1** features a minimal component count and an easily assembled transformer, T_1.

During the time it takes to charge T_1's primary inductance, resistor R_1 and T_1's added secondary winding provide sufficient base current to turn on Q_2. Q_2's collector current increases until its base current can no longer hold the transistor in saturation. When Q_2 comes out of saturation, T_1's magnetic flux and secondary-voltage polarity reverse. During T_1's primary-discharge interval, the combination of T_1's secondary voltage in series with Q_1's base-emitter voltage applies reverse bias to Q_2's base and turns off the transistor. When Q_2 turns off, the voltage across T_1's primary inductance adds to the battery voltage and applies a forward bias to the LED, D_1. The current through R_1 determines the power applied to the LED and applies forward bias to Q_1's base-emitter junction to provide temperature-compensated bias voltage for Q_2.

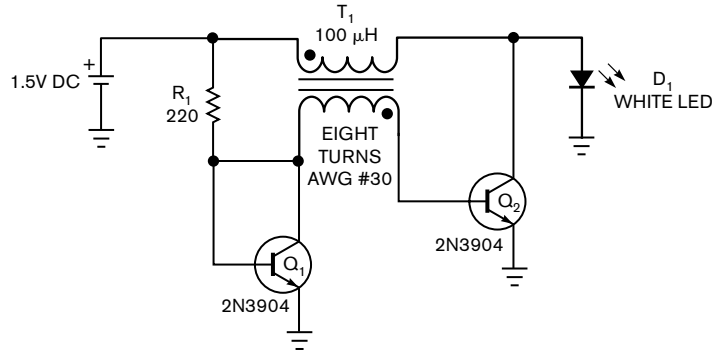

Figure 1 Two transistors and an easily assembled transformer drive a white LED from a single 1.5V battery.

The breadboarded circuit's transformer, T_1, comprises eight turns of AWG #30 insulated wire wound around the body of an unshielded 100-µH axial-lead inductor, producing approximately 400 mV p-p across the secondary winding. (**Editor's note:** Observe the winding's polarity dots. If the circuit fails to oscillate, reverse the connections to either the primary or the secondary winding.) The circuit operates over an input voltage range from just above Q_1's base-emitter voltage drop of approximately 0.6V to the LED's forward-voltage drop of approximately 3V. The circuit's switching frequency exceeds 340 kHz at 1.5V input. EDN

Implement a stepper-motor driver in a CPLD

Stephan Roche, Santa Rosa, CA

Based on the Motorola (now Freescale, www.freescale.com) heavily used but obsolete SAA1042 stepper-motor-driver IC, this Design Idea describes a CPLD (complex-programmable-logic-device)-based implementation of a stepper-motor driver that can also replace the driver in SAA1027- or UCN5804B-based designs. The design uses only six macrocells of a Xilinx (www.xilinx.com) XC9536 CPLD and thus can implement multiple stepper-motor drivers in one small-capacity CPLD. The CPLD stepper-motor driver requires clock, direction, step-size, and reset inputs. The clock input accepts logic-level pulses and goes active on the pulse's positive edge.

The direction, or CW/CCW (clockwise/counterclockwise), input determines the motor's rotational direction. Depending on the motor's electrical connections, holding this input at 0V normally produces CW rotation, and a logic-1 input produces CCW rotation. The step-size—that is, full- or half-step—input determines the motor's angular rotation for each clock pulse. Holding this input low commands the motor to execute a full step for each applied clock pulse, and a high input

TABLE 1 DRIVER OUTPUTS FOR EACH MACHINE STATE

Outputs	Step 0	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7
A	0	0	1	1	1	1	0	0
A_n	1	1	1	0	0	0	0	1
B	0	0	0	0	1	1	1	1
B_n	0	1	1	1	1	0	0	0

produces a half-step. A high level on the reset input puts the motor in a previously defined state and commands the CPLD to ignore any incoming clock pulses.

The CPLD's outputs comprise A and A_n and B and B_n phases, each of which controls one of the motor's two coils through external power drivers IC_2 and IC_3, which operate at the motor's nominal voltage (**Figure 1**). A pair of Schottky diodes at each driver's output protects the drivers' outputs during inductive-voltage transients induced by reversing the windings' currents. Using MOSFET drivers with internal diodes, such as Microchip's (www.microchip.com) TC4424A dual driver, may eliminate the requirement for external diodes.

The CPLD's program comprises an eight-state Moore finite-state machine that corresponds to the motor's eight half-step states. **Table 1** shows the driver's outputs for each machine state. In full-step state mode, the state machine executes only Step 0, Step 2, Step 4, and Step 6. At each clock pulse's rising edge, the machine state changes from Step(n) to Step(n+1) if CW/CCW is high or from Step(n) to Step(n−1) if CW/CCW is low. You can download a generic VHDL implementation of the stepper-motor-driver firmware from this Design Idea's online version at www.edn.com/070215di2. Although written for an XC9536 CPLD, the code is also suitable for any CPLD or FPGA target device. EDN

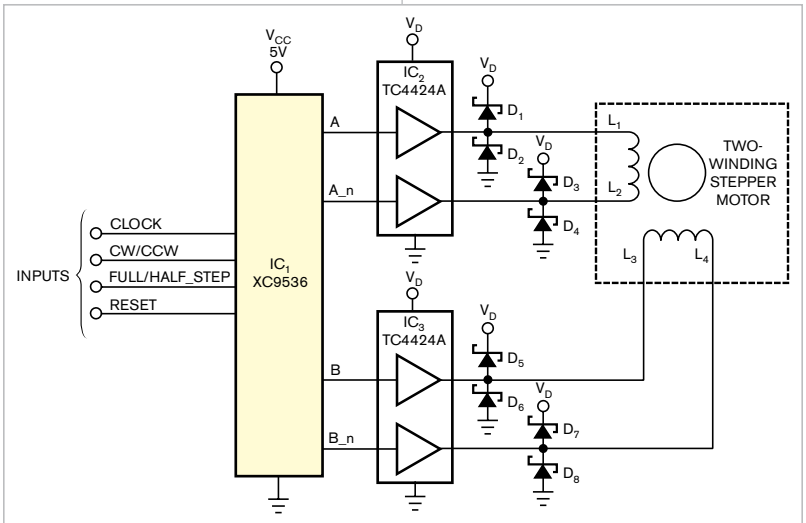

Figure 1 Emulating a dedicated stepper-motor controller, a programmable-logic device, IC_1, applies stepper-motor signals to motor drivers IC_2 and IC_3.

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READERS SOLVE DESIGN PROBLEMS

Current mirror improves PWM regulator's performance

Grant Smith, National Semiconductor, Phoenix, AZ

Power-supply designs requiring high-performance isolated feedback often use an error amplifier similar to the one in **Figure 1**, which relies on a second amplifier, IC_{1B}, to provide the necessary inversion to keep the optocoupler, IC_2, referenced to ground. To prevent bias-supply noise from entering the feedback path and causing oscillations, the amplifier relies on its ground reference and power-supply-rejection characteristics. The power supply's output drives a voltage divider comprising R_1 and R_2 that maintains the amplifier's inverting input at the same voltage as the reference voltage that IC_3 provides. C_2, R_3, and C_3 comprise frequency-compensation components for the power supply's stable operation. This component-intensive error-amplifier configuration requires two operational amplifiers, one precision shunt-voltage reference, four capacitors and often a fifth in parallel with R_6, and seven resistors.

Figure 2 shows an alternative single-amplifier design in which IC_3, an LM4040 precision-voltage reference, drives optocoupler IC_2 with a "stiff" positive-voltage source over a wide current range. The voltage reference suppresses any noise present on the bias-supply rail. Variations in the reference and power-supply voltages appear in common mode at the amplifier's inputs and thus provide additional noise immunity. A resistive-voltage divider comprising R_2 and R_3 reduces the reference voltage to equal the power supply's regulated output voltage, which drives IC_1's inverting input through R_1. Given its single voltage divider, the error-amplifier circuit of **Figure 2** provides the same output voltage as the circuit of **Figure 1** and requires a single operational amplifier and precision shunt reference, four capacitors, and six resistors.

Miller-effect coupling of collector-emitter-voltage transitions into a typical phototransistor-based optocoupler's high-impedance, optically sensitive

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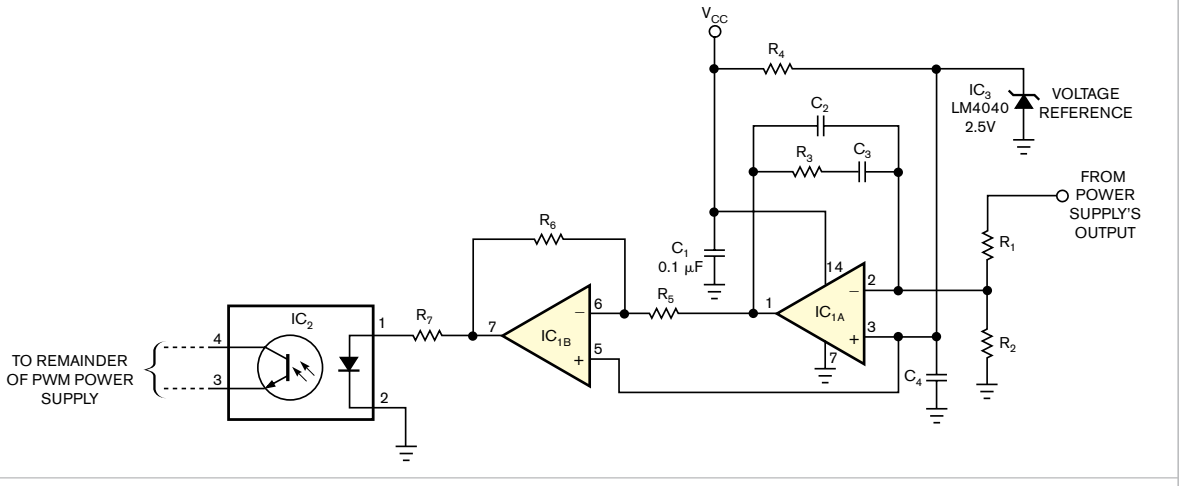

Figure 1 A conventional isolated-feedback circuit requires an extra operational amplifier and adds several passive components to a representative pulse-width-modulated power-supply design.

base region introduces a bandwidth-limiting pole, which dramatically slows the device's response time. Holding the phototransistor's collector-emitter voltage constant and allowing only its collector-emitter current to change provide an order-of-magnitude switching-speed improvement.

National Semiconductor's (www.national.com) LM5026 active-clamp current-mode PWM controller, IC_4, provides a convenient method of reducing an optocoupler's Miller-effect-induced slowdown. **Figure 2** shows the LM5026's internal current mirror driving what would normally serve as a frequency-compensation pin. Optocoupler IC_2 connects directly between two constant-voltage sources comprising the current mirror and a voltage reference. The resultant decrease in response time relocates the bandwidth-limiting pole and improves the circuit's transient response.

The values of C_2, C_3, R_3, and R_1 apply only to this design and may require modification for other applications. Select R_1 to provide equal impedances at both of the op amp's inputs. C_2 forms a high-frequency noise filter. After you measure the converter's overall gain, calculate values for C_3 and R_3 that will provide proper gain and phase response. Several methods of calculation are available, most of which will provide adequate results. EDN

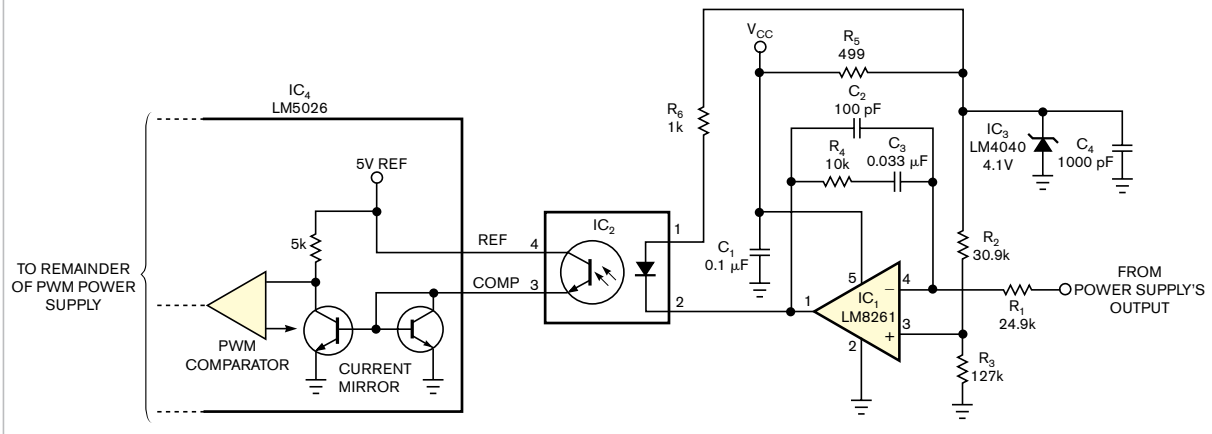

Figure 2 Clamping an optoisolator's voltage excursion improves the PWM-regulator loop's transient response.

Low-cost current monitor tracks high dc currents

Susanne Nell, Breitenfurt, Austria

To measure high levels of direct current for overload detection and protection, designers frequently use either a current-shunt resistor or a toroidal core and Hall-effect magnetic-field sensor. Both methods suffer from drawbacks. For example, measuring 20A with a 10-mΩ resistor dissipates 4W of power as waste heat. The Hall-effect sensor delivers accurate measurements and wastes little power, but it's

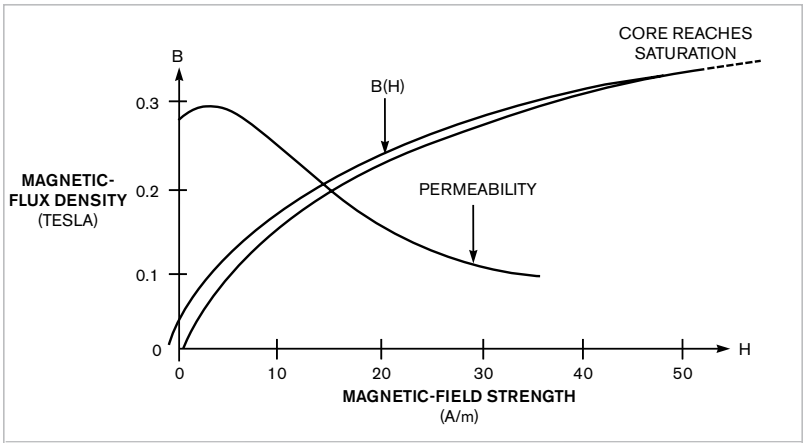

Figure 1 This representative magnetization (BH) curve shows that, as current through an inductor's winding increases, so does magnetizing-field strength, H. When magnetic-flux density, B, can no longer increase, the core's magnetic material has reached saturation.

an expensive approach to simple current monitoring.

This Design Idea describes an inexpensive, low-power current-measurement circuit that's useful for measurements of modest accuracy. As a bonus, a filter inductor in a dc/dc converter's input line can double as a current sensor for the measurement circuit. A representative ferrite core's permeability decreases as the core nears saturation (**Figure 1**). The curve's shape and values depend on the core material's characteristics and whether the core includes an air gap.

The core's permeability depends on the magnetic-flux level in the ferrite material, which in turn depends on the amount of current flowing through the core's windings. This circuit uses a simple LC oscillator to measure the core's permeability. A primary winding

A FILTER INDUCTOR IN A DC/DC CONVERTER'S INPUT LINE CAN DOUBLE AS A CURRENT SENSOR FOR THE MEASUREMENT CIRCUIT.

comprising one or more turns wound on the core carries the measurement current. A multiturn secondary winding on the core forms an inductor, L, that determines the oscillator's resonant frequency.

In theory, any LC oscillator circuit will serve in this application, but, in practice, the current-measurement winding presents a low impedance that damps the LC-tank circuit and causes start-up and stability problems in some oscillator circuits. Of a variety of tested oscillator circuits, the design in **Figure 2** offers the best performance. A number of factors affect the core's permeability, which in turn impacts the circuit's frequency stability and limits its applications to current-overload detection and low-accuracy current measurements.

Figure 3 illustrates the circuit's output-frequency-versus-current characteristics for three vendors' ferrite cores of identical dimensions and number of secondary turns. For best linearity, use a low-hysteresis core material. Cores of virtually any dimensions and materials work in the circuit but require optimization of the number of turns on the oscillator tank and primary windings. Increase the core's air gap, if present, when the current you apply to the core causes saturation before reaching the overload value. For improved performance and linear measurements, use the circuit in a closed-loop configuration (**Reference 1**).EDN

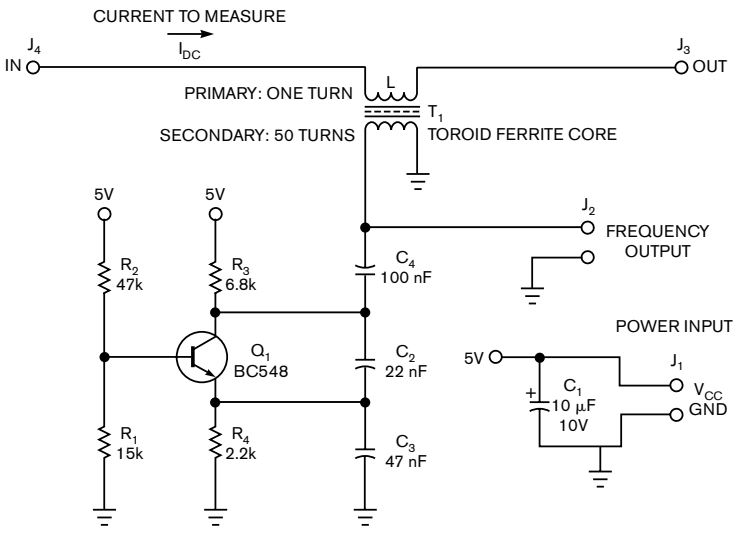

Figure 2 Varying the direct current flowing through the single-turn primary winding alters T_1's secondary winding's inductance, which in turn varies the oscillator's output frequency.

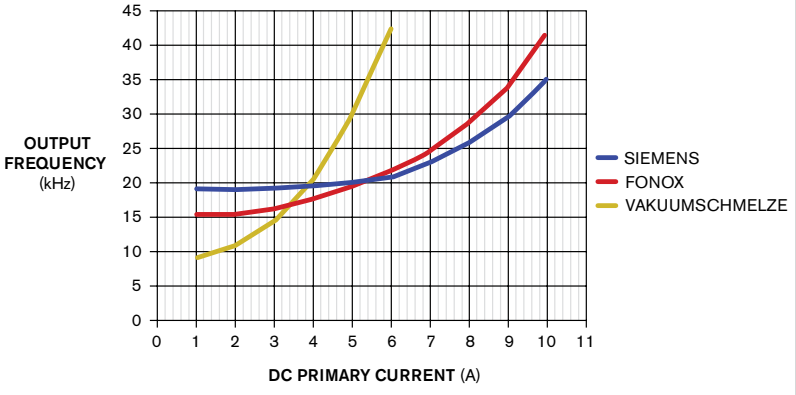

Figure 3 Current-versus-output-frequency plots for three manufacturers' toroidal cores show the influence of the cores' characteristics on frequency linearity and relative sensitivity.

REFERENCE

1 Nell, Susanne, "Improved current monitor delivers proportional-voltage output," *EDN*, Jan 19, 2006, pg 84, www.edn.com/article/CA6298271.

Digital-I/O circuit adapts to many interface voltages

Steve Hageman, Windsor, CA

To test products in my R&D lab, I build many universal data-acquisition systems that connect to a PC or another controller through RS-232 links or LANs. These small systems typically include multiple ADC, DAC, and digital-I/O channels to control various hardware functions during product design and development. Over the years, I have established a simplified analog-interface standard that spans a 0 to 5V range. On the digital side, many of the newer logic families no longer tolerate 5V inputs and have rendered 5V-only digital-I/O ports obsolescent.

To solve the problem, I designed a flexible digital-interface circuit around a MAX7301 I/O expander from Maxim Integrated Products (www.maxim-ic.com) and a programmable linear-power supply comprising a MAX1658 adjustable linear-voltage regulator under the control of a MAX5400 256-position, digitally programmable potentiometer. This circuit provides a programmable interface matching the logic levels of ICs that require 2.5, 3, 3.3, and 5V power supplies.

Two SPIs (serial-peripheral inter-

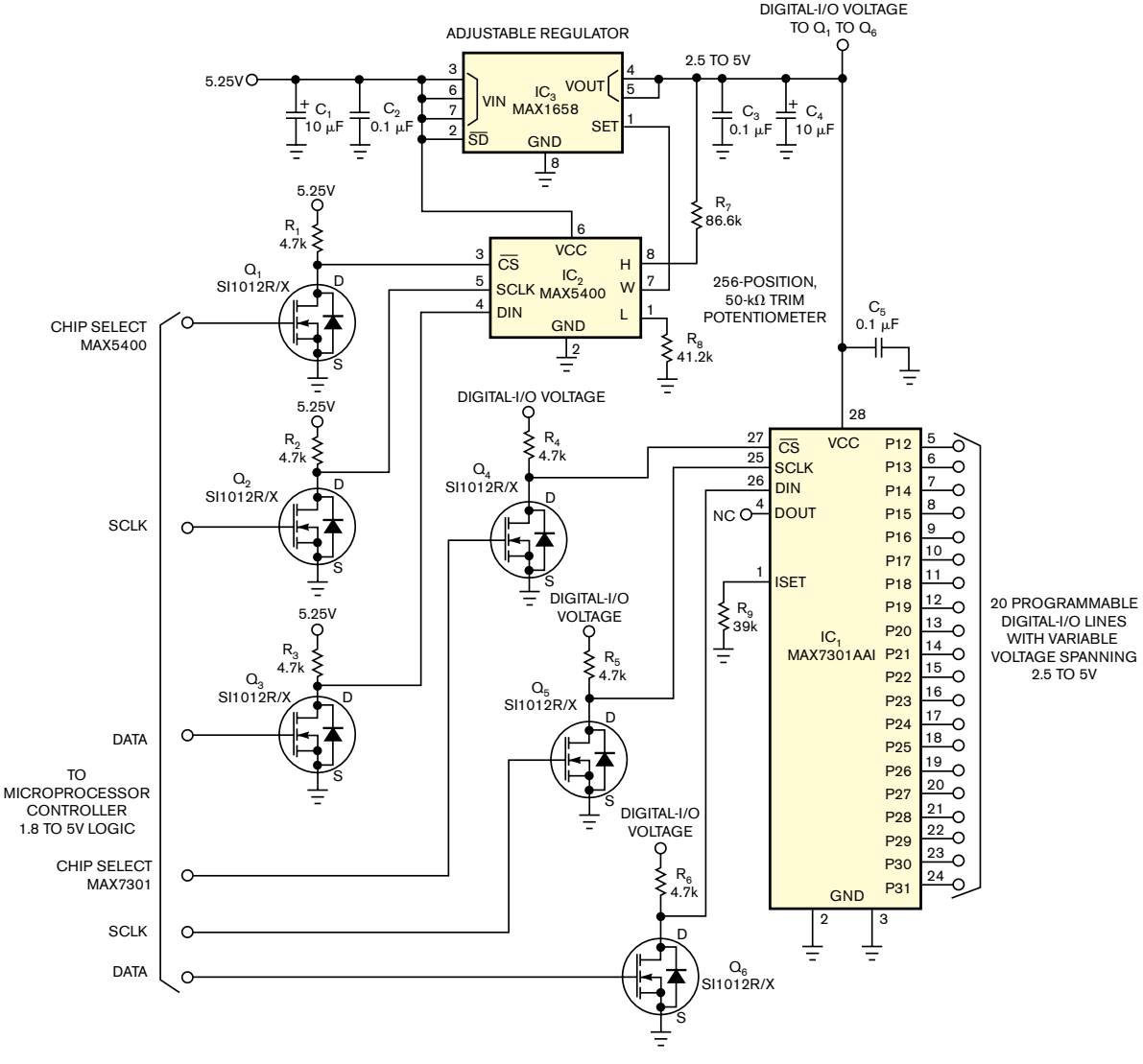

Figure 1 A programmable power supply sets voltage thresholds for a universal digital-I/O device.

faces) control all 20 of the MAX-7301AAI's input and output pins and voltage thresholds (**Figure 1**). Unlike some SPI-port expanders that include weak, resistor-only pullups, the MAX7301, IC_1, features true, active-pullup, "totem-pole" outputs that can source higher currents. When powered by the SPI-programmable linear regulator, the MAX7301's outputs can deliver logic levels of 2.5 to 5V. The programming interfaces for both devices comprise two three-wire (plus ground) SPI connections that use only six of the controller's signal lines.

Six Vishay (www.vishay.com) Si-1012R low-gate-voltage-threshold N-channel MOSFETs, Q_1 through Q_6, isolate the controllers' fixed-output-voltage levels from IC_1's variable-input-threshold voltages. Although any of several IC-level-translator ICs work equally well, the inexpensive MOSFET buffers occupy small footprints on the interface's PCB (printed-circuit board). For operation at serial-interface clock rates approaching IC_1's 26-MHz maximum, optimize the values of resistors R_1 through R_6 to provide adequate rise times at the selected clock rate. These values are adequate for operation at the 1-MHz SPI clock rate that a low-power microcontroller produces.

UNLIKE SOME SPI-PORT EXPANDERS THAT INCLUDE WEAK, RESISTOR-ONLY PULLUPS, THE MAX7301, IC_1, FEATURES TRUE ACTIVE-PULLUP, "TOTEM-POLE" OUTPUTS THAT CAN SOURCE HIGHER CURRENTS.

To alter the circuit's output-voltage level, IC_2, a 256-step Maxim MAX5400 digital potentiometer, controls IC_3, a Maxim MAX1658 adjustable-voltage linear regulator. Writing all zeros to IC_2 sets IC_3's output voltage to slightly more than 5V, and writing all ones (255 decimal) to IC_2 reduces IC_3's output voltage to slightly less than 2.5V. To compensate for component tolerances, the circuit provides enough voltage overrange to cover the full 2.5 to 5V range. Writing 128 (decimal) to IC_2 should produce a nominal 3.25V output. Measure IC_3's actual output voltage and subtract it from the nominal voltage to produce an offset count for calibration correction.

In operation, the host controller sets IC_3's regulated output voltage through IC_2 and determines the maximum voltages of IC_1's logic inputs and outputs. Next, the controller configures IC_1's inputs and outputs as necessary for the interface task at hand. The MAX7301's standard CMOS logic-threshold voltages of 0.3 to 0.7 times its supply voltage for low and high inputs, respectively, interface with other CMOS parts. EDN

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READERS SOLVE DESIGN PROBLEMS

Linear-brightness controller for LEDs has 64 taps

Ahmad Ayar, Maxim Integrated Products, Sunnyvale, CA

Applications that include LEDs but no microcontroller or other form of control intelligence can benefit from a simple circuit that provides manual control of the LEDs' light intensity. Among the devices suitable for this purpose are mechanical (analog) and electronic (digital) potentiometers. The digital potentiometer with up and down pushbuttons, an alternative to the mechanical potentiometer, is smaller, more reliable, and usually less expensive (**Figure 1**).

IC_2, a current regulator, drives a chain of LEDs with current as high as 200 mA. In a standard application circuit, IC_2's internal regulator senses the drop across current-sense resistor R_{SENSE} in series with the LED chain. Thus, IC_2 controls current through the chain by regulating voltage at the differential inputs, CS− and CS+, to the set value of 204 mV. Resistors R_A and R_B allow the output voltage IC_1's Pin 6 to adjust the current level. IC_1 is a 64-tap linear digital potentiometer whose resistance connects between ground and V5, a well-regulated voltage that IC_2 internally generates. You manually adjust the RW control voltage (Pin 6), a fraction of V5, using the up and down pushbuttons. A few assumptions allow a quick and simplified calculation of the necessary resistor values. Initially, you fix R_A and then calculate R_B and R_{SENSE}. The assumptions are that you can neglect the maximum 6.93-µA error induced by the bias current at CS+; that the value you choose for R_A is much higher than IC_1's equivalent resistance, for which the worst-case value at position 32 (top and bottom resistances plus the wiper series resistance) is 2.9 kΩ; and that R_{SENSE} is much less than R_B.

After setting R_A at 25.5 kΩ, $V_{WIPER}=(5V/63)\times N$, where N is the wiper setting (0 to 63). Then, you solve the equation $(V_{WIPER}-0.204V)/R_A=(0.204V-I_{LED}\times R_{SENSE})/R_B$. Solve the above equation for R_B under the conditions for which $I_{LED}=0$, which are N=63 and $V_{WIPER}=$ 5V (top position): $R_B=25.5\ k\Omega\times 0.204V/(5V\times 0.204V)=1.085\ k\Omega$. You can choose R_B from the standard values of 1.07 kΩ (1% series) or 1.1 kΩ (5% series). At the bottom position, where $V_{WIPER}=0$ and LED current is the maximum of 200 mA, brightness should be the maximum available. Solving for R_{SENSE}, $R_{SENSE}=[0.204V+(0.204V\times(1.085/25.5))]/0.2A=1.063\Omega$; 1.07Ω is a standard value in the 1% series.

A graph of LED current versus tap position shows a slight nonlinearity

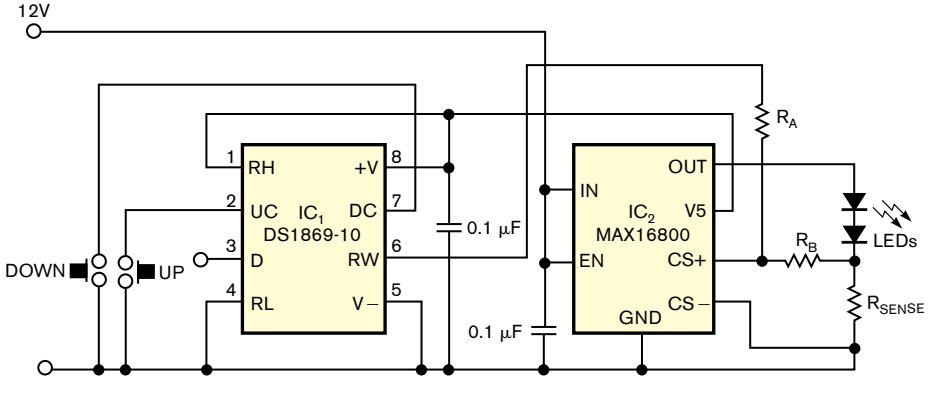

Figure 1 This brightness-control circuit lets you manually adjust the LED brightness using the up and down buttons.

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because of the variation in resistance you see looking into the wiper at different tap positions (**Figure 2**). At the extreme ends of the potentiometer, you see only the 400Ω wiper resistance. As the wiper moves toward midpoint, the resistance increases toward a maximum of one-quarter of the end-to-end resistance value. Because IC_1 is a 10-kΩ potentiometer, the resistance the wiper sees at midpoint is about 2.5 kΩ in series with R_{WIPER}. This variation introduces a maximum linearity error of 8%, which is negligible in most LED applications. IC_2 offers thermal protection against excessive heat and overload conditions. For effective power dissipation and to avoid thermal cycling, you must connect the exposed pad of the package to a large-area ground plane. EDN

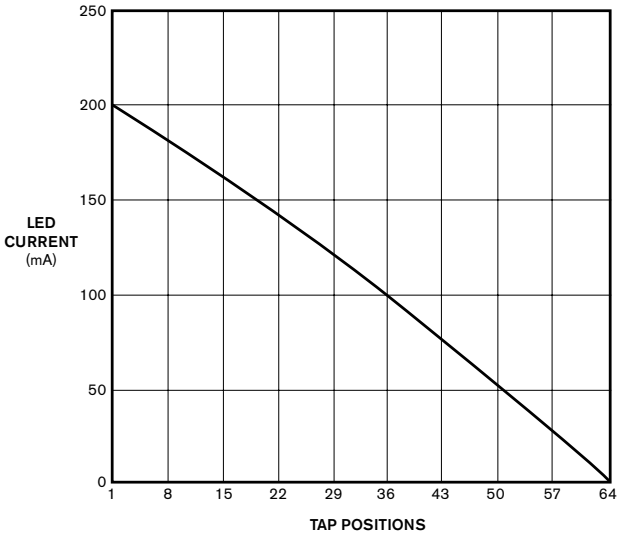

Figure 2 A plot of LED current versus tap position in Figure 1 exhibits only a slight nonlinearity.

Controlled power supply increases op amps' output-voltage range

Yakov Velikson, Lexington, MA

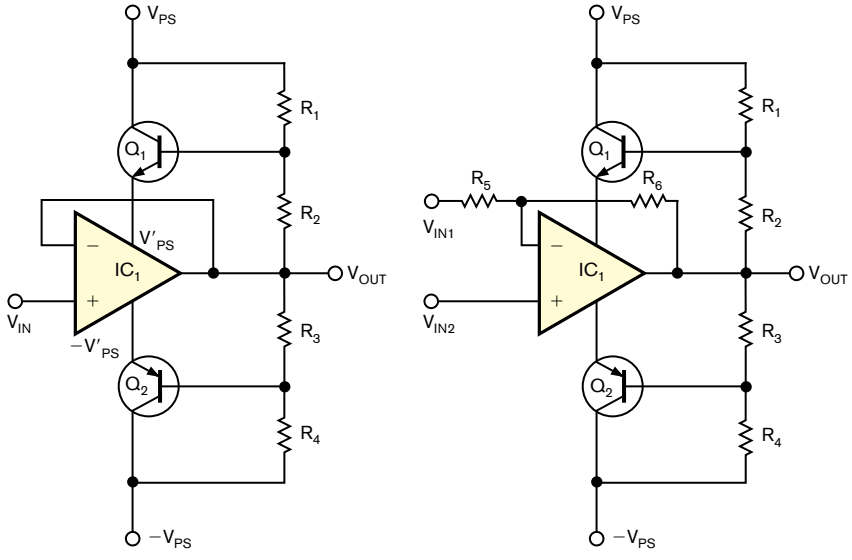

Figure 1 These simple circuits present the general methods of connecting the amplifier as an inverter or a follower to effect increased output voltage.

Increasing the output voltage of IC operational amplifiers usually involves adding high-voltage external transistors. The resulting circuit then requires correction to retain its operating characteristics. This correction is difficult, especially for precise amplifiers. This Design Idea presents an alternative: the use of a controlled power supply for the operational amplifier itself, which can increase the output voltage for many precise operational amplifiers without altering their operational characteristics. You can accomplish this task by connecting controlled transistors to the power supply of the amplifier. Resistor dividers that connect to the amplifier's output and bipolar high voltages control these transistors (**Reference 1**). The simple circuits in **Figure 1** present general methods of connecting the amplifier as an inverter or a follower to effect increased output voltage.

Dividers with resistors R_1, R_2, R_3, and R_4 determine the scale of power supply V'_{PS} and $-V'_{PS}$ for the amplifiers. If the output voltage ranges from ±22V,

resistor $R_1=R_2=R_3=R_4=R$, and V_{PS} and $-V_{PS}$ are 28V, then voltages V'_{PS} and $-V'_{PS}$ fall in the following range, allowing for any additional loss: $V'_{PS}=V_{PS}R_2/(R_1+R_2)+V_{OUT}(-V_{OUT})R_1/(R_1+R_2)$, and $-V'_{PS}=-V_{PS}R_3/(R_3+R_4)+V_{OUT}(-V_{OUT})R_4/(R_3+R_4)$ or $3V<V'_{PS}<25V$ and $-3V>-V'_{PS}>-25V$. However, power-supply circuits include transistors, which create junction resistance, affecting the amplifier's operation.

You can use supporting amplifiers to reduce losses and increase the quality of the output voltage of the primary amplifier. The requirements for supporting amplifiers are simple. They should have power supplies with opposite polarity from and lower applied voltage than that of the main power supply. They should provide the necessary power to the primary amplifier, and their frequency range should be slightly higher than that of the primary amplifier. You can use supporting amplifiers to eliminate the transitional resistances of transistors in power-supply connections. Thus, these circuits offer flexibility across a range of amplifier configurations (**references 2** and **3**).

Figure 2 shows an example of how to connect supporting amplifiers as followers. You derive output voltages V'_{PS} and $-V'_{PS}$ from resistor connections with the following equations: $V'=V_{PS1}R_7/(R_6+R_7)+V_{OUT}(-V_{OUT})R_6/(R_6+R_7)$, and $-V'=-V_{PS1}R_8/(R_8+R_9)+V_{OUT}(-V_{OUT})R_9/(R_8+R_9)$. If the supporting amplifiers have a power supply of 28V for V_{PS1} and $-2V$ for $-V_{PS2}$ for amplifier IC_2, then $-V_{PS1}=-28V$, $V_{PS2}=2V$ for amplifier IC_3, and the output voltage of amplifier IC_1, V_{OUT}, is 24V or $-24V$. Also, $R_6=R_7=R_8=R_9=R$, such that $V'=28V\times0.5+24V\times0.5=26V$. Further, $-V'=-28V\times0.5+24V\times0.5=-2V$ for $V_{OUTMAX}=24V$. $V=28V\times0.5-24V\times0.5=2V$, and $-V'=-28V\times0.5-24V\times0.5=-26V$ for $V_{OUTMIN}=-24V$. You can achieve the greatest voltage range by using separate power supplies—one for the normal voltages of the amplifier and one for the regulated part of the output voltage (**Figure 3**).

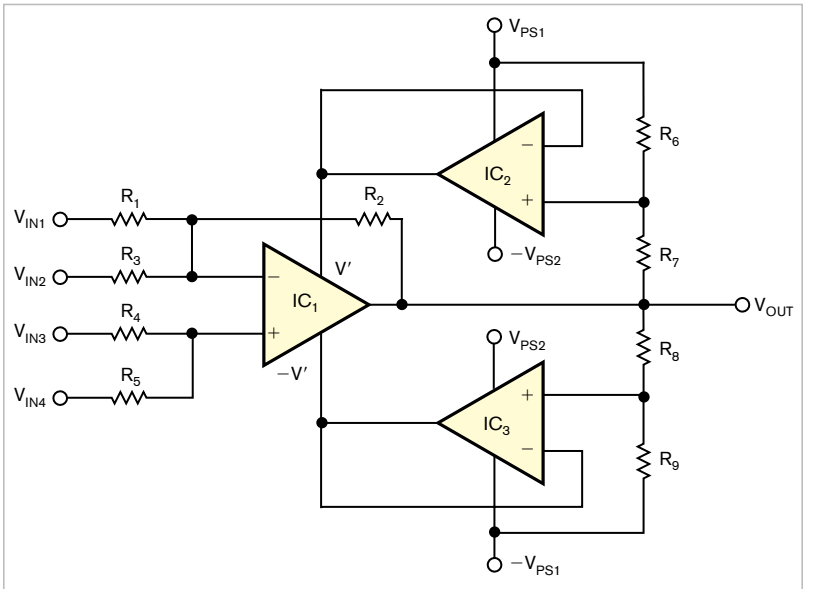

Figure 2 Replacing the transistors with op amps reduces losses and increases the quality of the output voltage of the primary amplifier.

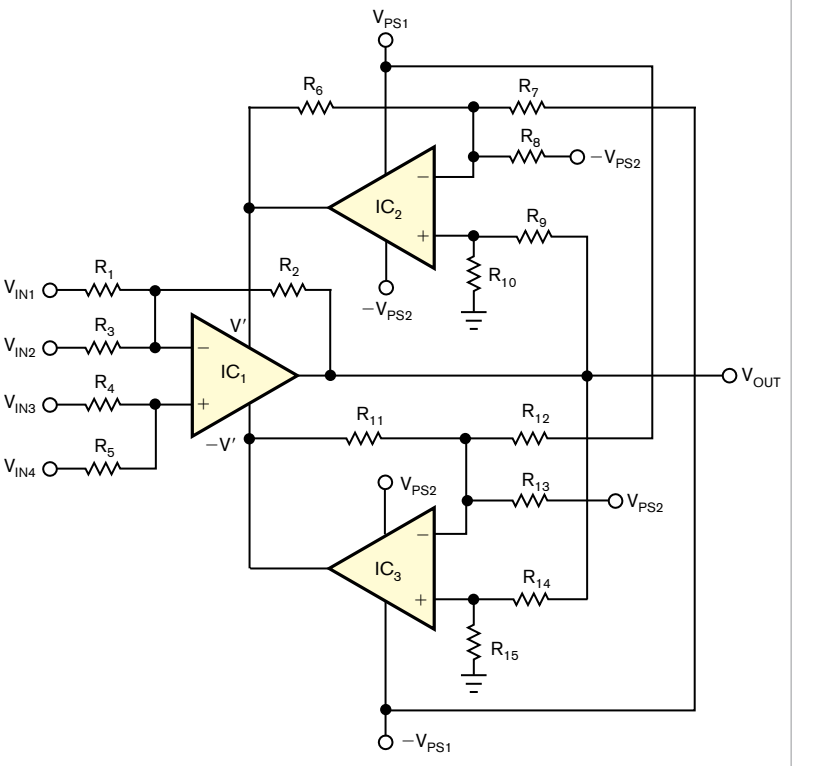

Figure 3 You can achieve the greatest voltage range by using separate power supplies—one for the normal voltages of the amplifier and one for the regulated part of the output voltage.

IC_1 is the primary amplifier. Supporting amplifiers IC_2 and IC_3 have asymmetrical power supplies. You could use many types of amplifiers in this circuit, but modern operational amplifiers may be preferable because they allow the use of the complete range of the power supply and because they handle rail-to-rail input and output. In this circuit, $V_{PS1}=28V$, $-V_{PS1}=-28V$, $V_{PS2}=2V$, and $-V_{PS2}=-2V$. The voltages of the primary amplifier are $V'=-(-V_{PS1})R_6/R_7-(-V_{PS2})R_6/R_8+(-V_{OUT})R_{10}/(R_9+R_{10})[R_7R_8+R_6(R_7+R_8)]/R_7R_8$. Further, $-V'=-(V_{PS1})R_{11}/R_{12}-(V_{PS2})R_{11}/R_{13}+(-V_{OUT})R_{15}/(R_{14}+R_{15})[R_{12}R_{13}+R_{11}(R_{12}+R_{13})]/R_{12}R_{13}$. Set $R_6=R_{10}=R_{11}=R_{15}=R$, $R_7=R_8=R_{12}=R_{13}=2R$, and $R_9=R_{14}=3R$, such that $R_6/R_7=R_6/R_8=R_{11}/R_{12}=R_{11}/R_{13}=0.5$, $R_{10}/(R_9+R_{10})=R_{15}/(R_{14}+R_{15})=0.25$, and $[R_7R_8+R_6(R_7+R_8)]/R_7R_8=[R_{12}R_{13}+R_{11}(R_{12}+R_{13})]/R_{12}R_{13}=2$. Then, substitute these values into the amplifier voltages yields $V'=14V+1V+(-V_{OUT})0.5$, and $-V'=-14V-1V+(-V_{OUT})0.5$. Minimum and maximum values for each power supply are $1.5V\le V\le 28.5V$, and $-1.5V\ge -V\ge -28.5V$. The total voltage of the power supply has a limit of 30V, ranging from 1.5 to 28.5V and from −1.5 to −28.5V. This range permits an increase of the output voltage of the primary amplifier by ±27V. EDN

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3. Velikson, Yakov, A Murigin, and V Uchno, "The multichannel conversion of a revolving sine-cosine resolver to code," *Bulletin of Izobreteny* (copyrights and patents), No. 44, 1988.

Single-IC-based electronic circuit replaces mechanical switch

Santosh Bhandarkar, Bangalore, India

A simple and inexpensive electronic circuit uses a low-cost pushbutton switch to toggle the electrical power on and off. The circuit replaces a more costly and bulky push-push mechanical switch. The pushbutton switch triggers a monoshot circuit. The monoshot circuit's output triggers a toggle flip-flop, which inverts its output state and controls power to the load.

Several implementations of the scheme are possible. **Figure 1** shows a single-IC implementation. The circuit uses two flip-flops, IC_1 and IC_2, in the same IC, CD4027B. You configure IC_1 as a monoshot circuit by feeding its output back to its reset pin through an RC network. IC_1 outputs a high on the rising edge of the clock by tying its J input high and its K input low. The pushbutton switch connects between the clock input of IC_1 and ground. The switch can also connect between the clock input and the positive supply, V_{DD}. By tying IC_2's J and K inputs high, IC_2 becomes a toggle flip-flop. The output of IC_1 clocks IC_2 and toggles its output on the rising edge of the IC_1 output.

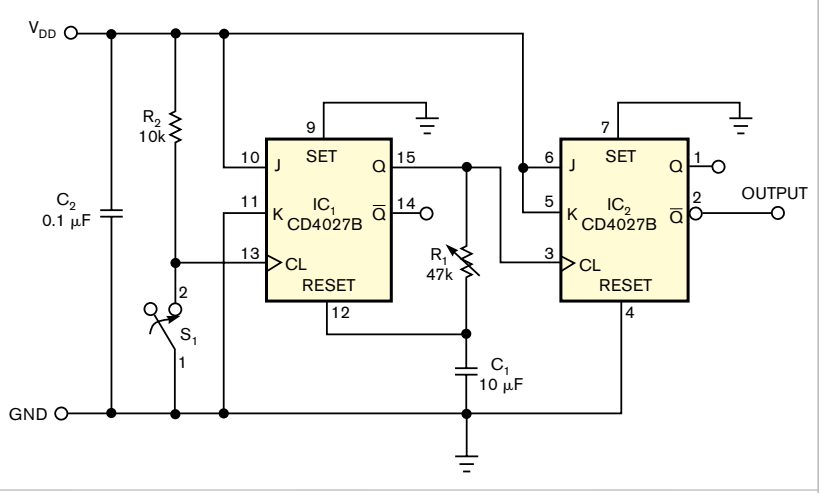

Figure 1 A pair of flip-flops configured as a monoshot and a toggle flip-flop debounce a simple, inexpensive pushbutton switch.

You can understand the operation of the circuit by observing the waveform at different points of the circuit (**Figure 2**). When you press the pushbutton switch, due to debouncing, IC_1's output goes high on the clock's rising edge. Capacitor C_1 starts charging through R_1 toward high voltage. At the same instant, IC_2 receives a rising-edge transition at its clock and toggles its output. When capacitor C_1's voltage exceeds the threshold of the IC_1 reset pin, IC_1 resets, and its output goes low. C_1 now discharges through R_1 to low voltage. The charging and discharging rate of C_1 are equal. The duration of the monoshot circuit's output pulse handles the switch-press time and the debouncing period. Varying

the value of R_1 varies the pulse period, and you can set R_1 for different types of pushbutton switches. Complementary outputs of IC_2 are available, and you can use them to drive power switches, such as transistors, MOSFETs, relays, and shutdown pins of switching regulators. The circuit operates over a supply voltage of 3 to 15V and can control power to analog and digital circuits. EDN

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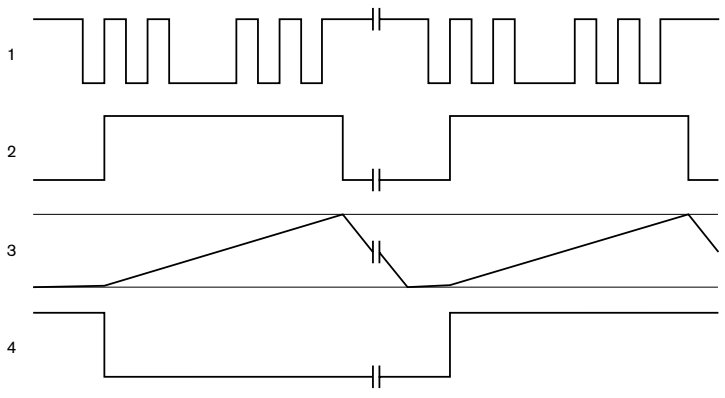

Figure 2 Trace 1 is the voltage across the clock of IC_1, Trace 2 is the output of IC_1, Trace 3 is the voltage on capacitor C_1, and Trace 4 is the output of IC_2.

Microcontroller drives H bridge to power a permanent-magnet dc motor

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

A traditional method of driving a low- to medium-power permanent-magnet dc motor involves using four MOSFET or bipolar transistors in an H-bridge configuration. For example, in **Figure 1**, the motor connects between collector pairs C_1 and C_2 and C_3 and C_4. Turning on diagonally opposite transistor pairs Q_1 and Q_3 or Q_2 and Q_4 steers current through the motor and allows for reversal of its direction of rotation. However, this method requires that each of the four transistors receive its own control input. Depending on the motor's voltage requirements, the upper two drive signals may require electrical isolation or a level-shifter circuit to match the microcontroller's output-voltage limitations.

This Design Idea describes an alternative circuit that drives only the H bridge's two low-side switching transistors. In a standard bipolar-transistor H bridge for bidirectional motor control, Q_1's and Q_4's bases connect to Q_3's and Q_2's collectors through resistors R_3 and R_4 (**Figure 2**). Inputs V_{INA} and V_{INB} each control a pair of switches. When Q_2 turns on, resistor R_4 and diode D_6 pull Q_4's base low, saturating Q_4 and pulling current through the motor and Q_2. Similarly, turning on Q_3 pulls Q_1 into saturation and drives the motor in the opposite direction. Diode D_5 ensures that Q_1 remains off when Q_4 conducts, and D_6 performs the same function for Q_4 when Q_1 conducts. Resistors R_1, R_2, R_7, and R_8 increase the switching speed of their associated transistors, and resistors R_5 and R_6 limit base-current drain from the microcontroller's 5V high-logic-level outputs to approximately 15 to 20 mA. Resistors R_3 and R_4 set Q_1's and Q_4's saturation base currents. Their value depends on the motor-supply voltage and Q_1's and Q_4's dc current-gain according to the following equation: $R_3 = R_4 \leq [V_{CC} - V_{BE(ON)}(Q_4) - V_F(D_6) - V_{CE(SAT)}(Q_2)]/[(I_{MOTOR})/$

(continued on pg 82)

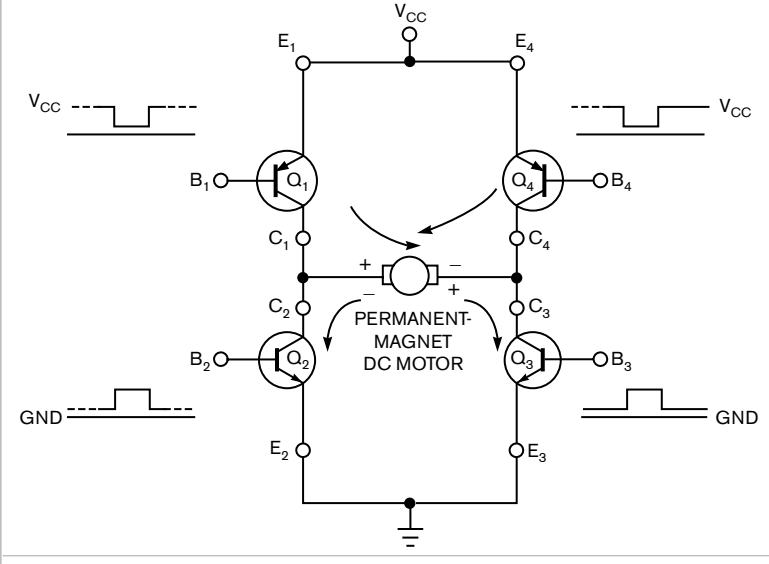

Figure 1 In an H-bridge output-driver stage, diagonally opposed transistor pairs conduct to energize a dc motor. The circuit requires four control signals.

$h_{FE(MIN)}(Q_4)$]. For best performance, select bipolar-junction transistors with low collector-emitter saturation voltages, $V_{CE(SAT)}$, and high values of dc-current gain, h_{FE}. Currently available medium-power transistors compete favorably with MOSFETs by offering these characteristics in combinations that minimize collector-power dissipation and require little base drive.

Discrete devices such as On Semiconductor's (www.onsemi.com) NSS40200LT1G PNP and NST489AMT1 NPN bipolar transistors work well in the circuit in **Figure 1**. For a more compact implementation, you can select an integrated H bridge, such as Zetex's (www.zetex.com) ZHB6790, which operates at power-supply voltages as high as 40V, with 2A continuous and 6A peak pulse-current collector ratings. Its minimum current gain of 500 at a collector current, I_C, of 100 mA can decrease to 150 at I_C of 2A. At a worst-case collector current of 2A in Q_2 and Q_3, achieving a saturation voltage of 0.35V or less requires a base current of 13 to 20 mA. Fortunately, many microcontrollers' outputs can source or sink as much as 25 mA and thus directly drive the H bridge independently of the motor's power-supply voltage. To further reduce drive current or to use a standard CMOS or TTL IC as a drive source, you can buffer Q_2's and Q_3's inputs with small-signal transistor inverters. As an option, you can connect fractional-ohm resistors between the emitters of Q_2 and Q_3 and ground. This approach can provide analog voltages proportional to motor current, allowing the microcontroller to detect a stalled or overloaded motor. EDN

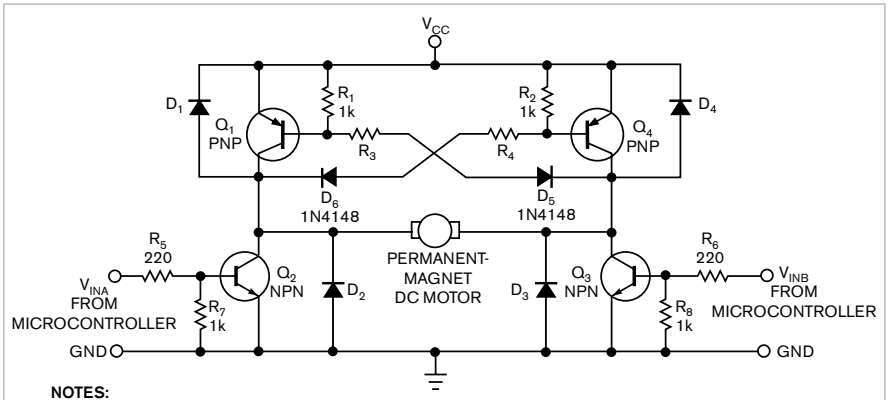

Figure 2 This improved H-bridge-driver circuit uses transistors in complementary pairs and requires only two low-level control signals.

EDITED BY CHARLES H SMALL
AND BRAD THOMPSON

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Oscilloscope helps obtain Bode plots in non-50Ω environments

Antonio Eguizabal, Freescale Semiconductor Inc, Tempe, AZ

A Bode plot can simplify characterization of an active or a passive network by showing frequency and phase representations of the network's transfer function, T. In its classic form, a Bode plot graphs frequency data on an X-axis logarithmic scale and amplitude and phase data in logarithmic or linear format on the Y-axis scale. However, most network analyzers' input ports typically present fixed, low impedances of either 50 or 75Ω that load any device under test that connects to the ports. To measure passive or active circuits in environments other than 50 or 75Ω, you can buffer the analyzer's inputs with amplifiers that present high input impedances to the device under test and low output impedances that match the network analyzer's inputs.

As an alternative to building or purchasing custom buffer amplifiers, you can use the near-ideal amplifiers in an analog oscilloscope that provides a vertical amplifier output on its rear panels—for example, the venerable Tektronix (www.tektronix.com) 465B. Its more commonly available cousin, the Tektronix 2465, provides a Channel 2 output on its rear panel. This Design Idea describes a proven measurement method that obtains magnitude and phase graphs of both active and passive devices. A Bode plot displays the magnitude $|T(j\omega)|$ as a function of angular frequency, $\omega=2\pi f$.

Most measurements span a broad range of frequencies, and it is thus helpful to present the frequency data in logarithmic format (log f) on the graph's abscissa (X axis) and amplitude data formatted as $20\log(|T(j\omega)|)$ on the ordinate (Y axis). Two graphs of magnitude and phase versus frequency thus present a compact representation of the network's electrical characteristics. Using the analyzer's controls, select the magnitude of S21 and phase of S21 as Y-axis displays in rectangular coordinates and select the log f display option for the X axis.

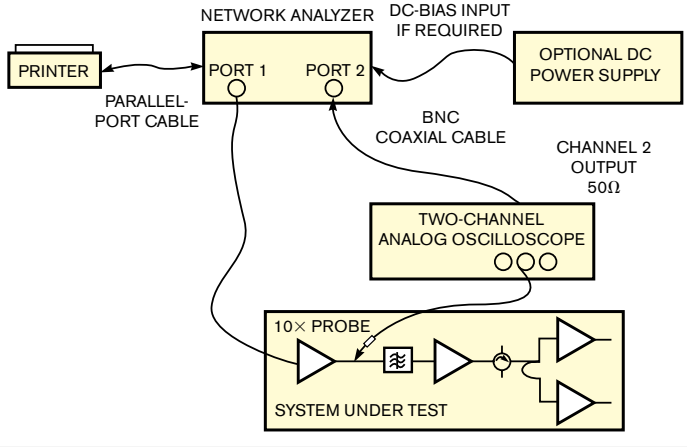

Figure 1 The basic test setup for generating Bode plots requires a network analyzer, an analog oscilloscope with one or more vertical outputs, an optional dc-bias power supply, and a printer.

A Tektronix 465B or 2465 oscilloscope's vertical amplifier presents a 100-MHz bandwidth, a 1-MΩ input impedance, and a 50Ω output impedance. Connect the scope's low-impedance output to the network analyzer's Port 2 input. A 10× probe that connects to the oscilloscope can raise its effective input impedance to as high as 10 MΩ. Oscilloscopes other than those mentioned or stand-alone amplifiers can deliver wider bandwidths, higher dynamic-input-voltage range, and reduced phase error and group delay for more accurate measurements. **Figure 1** illustrates the basic measurement configuration. Use coaxial cables with appropriate connectors to match the network analyzer's inputs. If the network analyzer requires dc bias for Port 1, use an external power supply.

For best results, calibrate the system as follows.

1. Perform the network analyzer's

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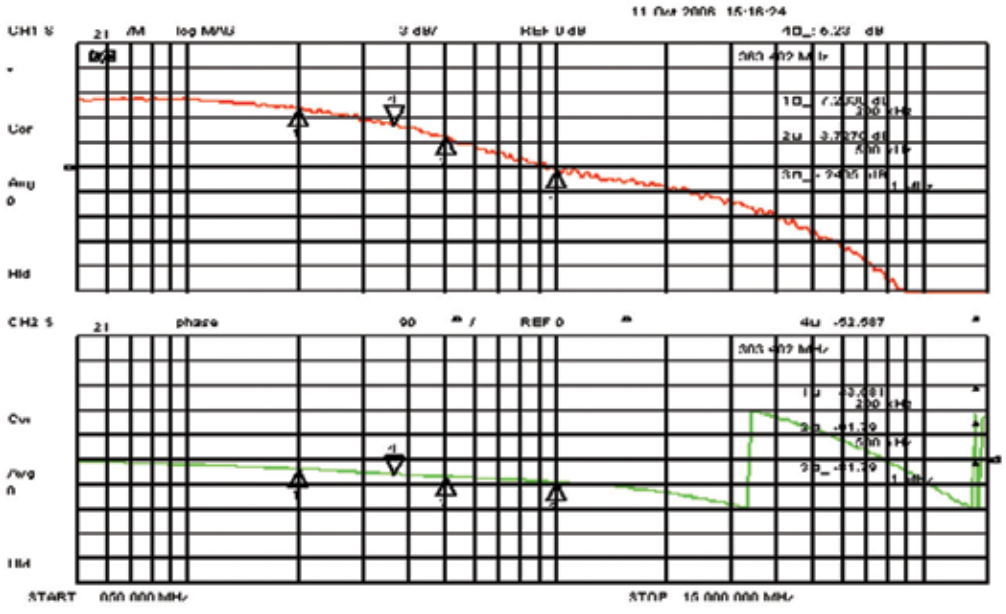

Figure 2 A vertical amplifier with 100-MHz bandwidth fairly accurately measures a device under test operating at 10 MHz, plotting the magnitude (top-trace) behavior and phase (bottom-trace) behavior of a typical device in log-frequency format spanning a 50-kHz to 15-MHz range. Markers show measured values at reference points.

two-port calibration procedure over the frequency range of interest.

2. Set the network analyzer to produce a dual display, with the magnitude of S21 on top and phase of S21 at the bottom of the display screen. Change the frequency-display mode from linear to log.

3. Set the oscilloscope for dc coupling and center its trace at midscreen. Select the required sweep rate and the triggering mode to ac and adjust the trigger level to produce a trace.

4. Connect the oscilloscope's Channel 2 input or probe to the network analyzer's Port 1 input and set the analyzer's controls to establish a reference line.

5. Adjust the vertical amplifier's gain and attenuation (volts/division) controls until the analyzer displays random noise, which represents the lowest detectable signal.

6. Set the analyzer's gain-per-division scale to 3 dB/division, a convenient value for determining the frequencies at which the gain of the device under test decreases by 3 dB.

7. Adjust the network analyzer's source (output) power range in decibels referred to milliwatts and the oscilloscope's gain/attenuation settings in volts per division to obtain an optimum data display. If the device under test introduces appreciable gain or loss, adjust the analyzer's scale-reference control to recenter the displayed trace. **Figure 2** shows a Bode plot derived from an active device that would not tolerate analyzer loads of less than 10-kΩ impedances.

To minimize the phase shift that the oscilloscope's vertical amplifier introduces, choose an amplifier whose bandwidth greatly exceeds the operational bandwidth. In **Figure 2**, a vertical amplifier with 100-MHz bandwidth fairly accurately measures a device under test operating at 10 MHz. You can eliminate phase-shift and amplitude errors that the test fixture introduces by storing a reference trace and subtracting it from the active trace. Refer to the network analyzer's operating manual for details. EDN

PRBS generator runs at 1.5 Gbps

Lukasz Sliwczynski, AGH University of Science and Technology, Institute of Electronics, Krakow, Poland

PRBS (pseudorandom-binary-sequence), or PN (pseudonoise), generators find a broad range of applications in digital-data transmission (**Reference 1**). These circuits often comprise simple shift registers with feedback that can serve as test sources for serial-data links. As their name implies, the output sequence is not truly random and in fact repeats after 2^N-1 bits, where N denotes the shift register's length. Polynomial notation, in which the polynomial order corresponds to the shift register's length and, thus, the PRBS' period provides a convenient method of describing the sequence.

Communications-equipment tests use certain standard polynomials. For example, x^7+x^6+1 yields a PRBS period of 127 bits, $x^{23}+x^{18}+1$ yields a period of more than 8 million bits, and $x^{31}+x^{28}+1$ yields a period that's 256 times longer. A PRBS with a longer period generally produces a greater variety of data patterns that more thoroughly check the transmission system's performance.

A simple shift register with feedback from an intermediate stage can generate a PRBS. The flip-flops constituting the register must run at a speed equal to the transmission speed, which may pose a problem if you want to build a long-period PRBS generator that runs at a gigahertz clock rate. A high-speed serializer such as Texas Instruments' (www.ti.com) TLK2201B, which runs at data rates as high as 1.6 Gbps, offers one potential solution to the problem. However, instead of accepting a PRBS in its natural fully serial format, the serializer accepts only 10-bit portions at a time.

The circuit in **Figure 1** illustrates a 31st-order, parallel-PRBS generator that delivers 10-bit output segments and can easily adapt to other PRBS orders and output widths. To design the circuit, begin by drawing a diagram with 31 flip-flops arranged in rows containing nominally 10 flip-flops. In this instance, the design comprises four rows, with only one flip-flop in Row 1. **Figure 1** shows the timing relationships among the flip-flops and the numbering convention.

The resulting structure forms a parallel shift register, with the fourth row fed directly from the third row, the third fed from the second, and so on. Flip-flops 10 through 2 in Row 2 and flip-flop 1 in Row 1 receive their inputs from the feedback path. This arrangement ensures that flip-flops in consecutive rows always deliver their outputs 10 time instants apart, and the generator's clock thus runs at one-tenth the speed of an equivalent serial-shift-register PRBS implementation.

To determine the feedback signals, derive the equation that describes a standard—that is, serial—

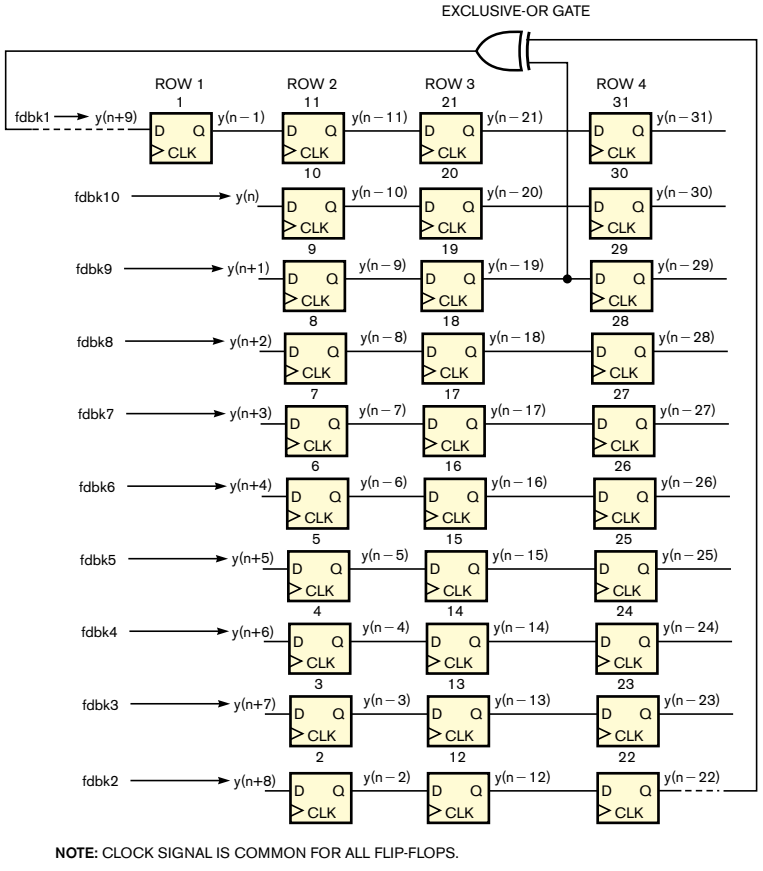

Figure 1 This circuit implements a 10-bit parallel-output PRBS generator defined by the polynomial equation $x^{31}+x^{28}+1$. To reduce clutter, the schematic shows only one of 10 exclusive-OR gates that generates the register's feedback signals. A common clock source (not shown) drives all 31 flip-flops' clock inputs.

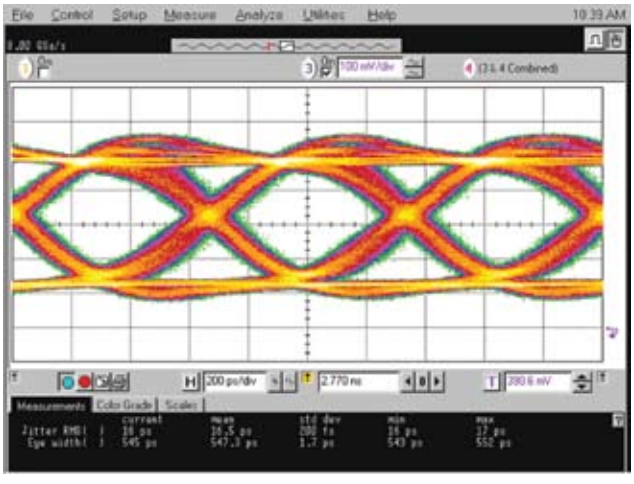

Figure 2 A pseudorandom sequence produces this eye diagram as measured at the output of a TLK2201B serializer that an FPGA-sequence generator drives.

PRBS generator's output, which, for a polynomial of $x^{31}+x^{28}+1$, yields: y(n)=y(n−31) xor y(n−28). Using that equation, you can derive the equations that describe feedback signals fdbk1 through fdbk10. That is, fdbk1: y(n+9)=y(n−22) xor y(n−19), fdbk2: y(n+8)=y(n−23) xor y(n−20), … fdbk10: y(n)=y(n−31) xor y(n−28). For example, feedback signal fdbk1 derives from the output of a two-input exclusive-OR gate driven by the outputs of flip-flops 22 and 19.

Listing 1, which is available at the Web version of this Design Idea at www.edn.com/070329di1, contains the VHDL code that implements the circuit of **Figure 1** in either a CPLD or an FPGA device. Lines 15 through 18 define the parallel-shift register, and lines 21 through 23 define the feedback circuit's construction. The circuit in this Design Idea fits into an XC3S50 Spartan 3 device from Xilinx (www.xilinx.com), runs at a 150-MHz clock rate, and drives a Texas Instruments TLK2201B serializer at 150 MHz through a 10-bit interface. Xilinx's ISE 7.1i software compiled the circuit's VHDL files. **Figure 2** displays an eye diagram for the serializer's output and confirms the circuit's operation at 1.5 Gbps. The compilation software predicts that the circuit should run at clock rates exceeding 300 MHz, but the TLK2201B limits operation to 150 MHz. EDN

REFERENCE

1 Miller, Andy, and Mike Gulotta, "PN generators using the SRL macro," Application Note APP211, Xilinx Inc, June 15, 2004, www.xilinx.com/bvdocs/appnotes/xapp211.pdf.

Use SystemVerilog for coverage metrics

Thomas L Anderson, Cadence Design Automation, San Jose, CA

The design-and-verification industry is at the intersection of two important trends in the design and verification of SOC (system-on-chip) devices: the adoption of SystemVerilog HDVL (hardware-description and -verification language) and the increasingly critical role for coverage metrics. The interest in SystemVerilog is understandable; this IEEE-standard language has the features for RTL (register-transfer-level) design, high-level modeling, testbench creation, and assertion specification (**Reference 1**).

SystemVerilog also provides constructs for design-and-verification engineers to specify functional coverage points—conditions that designers must exercise for complete verification of the design. Designers increasingly use functional coverage to supplement traditional code coverage. The primary driver for this evolution is the widespread use of constrained-random-stimulus generation.

Traditional verification plans typically include a list of design features or tests that verify features and test status. This approach has worked well with handwritten, directed tests because of the clear correspondence between features and tests. However, verification consists of writing and running each test in simulation, perhaps after turning on some code coverage to help identify features you may have missed in the plan.

Constrained-random-stimulus generation requires a different approach, in which each automatically generated test can exercise many features and parts of the design. A modern verification plan lists features, functional coverage points for the features, and coverage status. You gauge verification closure by the number of coverage points you exercise rather than the number of tests you complete.

SystemVerilog provides all the features necessary to develop both handwritten tests and constrained-random testbenches and to track progress toward closure. Most simulators have built-in code coverage for the new design constructs that SystemVerilog introduces. Thus, code-coverage metrics are available for designs taking advantage of the language's advanced RTL features.

SystemVerilog provides several powerful specification methods for functional coverage. The first is cover property, which is part of the SVA (SystemVerilog Assertions) subset of the language. SVA's assertion features, including temporal sequences, are also available for functional coverage. For example, **Listing 1** ensures that the simulator exercises the two extremes—one and five cycles—of a request-acknowledge handshake. Both simulators and many formal-

LISTING 1 MINIMUM AND MAXIMUM RESPONSE

```
minimum_response: cover property (@(posedge clk)
          (req ##1 ack ));
maximum_response: cover property (@(posedge clk)
          (req ##5 ack ));
```

LISTING 2 PAYLOAD SIZES OF INCOMING PACKETS

```
covergroup payloads_seen (@(packet_received);
     coverpoint payload_size {
          bins empty = { 0 };
          bins minimum = { 1 };
          bins maximum= { 1023 };
          bins others = default; }
endgroup : payloads_seen
```

analysis tools support the cover-property construct. If formal analysis can prove that a coverage point is unreachable, a design bug may be blocking important functions from being exercised. If formal analysis instead provides a trace showing how to reach a coverage point, this trace can provide a good hint on how to write or generate a test.

LISTING 3 ENUMERATED TYPE FOR FOUR PACKET CLASSES

```
enum { read, write, atomic, ctrl } packet_class
covergroup packets_seen (@(packet_received);
     coverpoint payload_size {
          bins empty = { 0 };
          bins minimum = { 1 };
          bins maximum= { 1023 };
          bins others = default; }
     coverpoint packet_class;
     cross payload_size, packet_class;
endgroup : packets_seen
```

Beyond individual coverage properties, you sometimes must track ranges of values. SystemVerilog provides the cover-group construct, which is not part of SVA, to perform this function. For example, **Listing 2** tracks the payload sizes of incoming packets on a network interface and ensures the coverage of corner cases of empty, minimum, and maximum payloads. SystemVerilog also provides the cross construct to measure cross-coverage between two coverage points. This feature allows the tracking of combinations of coverage metrics. For example, **Listing 3** specifies an enumerated type for four packet classes for the network interface, adds a cover point to track the packet classes, and crosses the packet types with the payload sizes.

Ultimately, the SOC-tapeout decision must take into account all coverage metrics. Although functional coverage is the primary method, code coverage has value as a backup to identify areas of the design with no functional coverage due to an incomplete verification plan. The project team needs to merge together code- and functional-coverage results to assess verification progress and help determine verification closure. Coverage is critical for modern, constrained-random verification. Without effective metrics, no reliable way exists to gauge status and manage progress. In addition to its other features and benefits, SystemVerilog provides support for functional coverage. By including coverage in the verification plan from the start of the project and taking advantage of SystemVerilog, the SOC team can employ a complete plan-to-closure methodology that greatly increases the chances for a successful product. EDN

REFERENCE

1 www.systemverilog.org.

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AND BRAD THOMPSON

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READERS SOLVE DESIGN PROBLEMS

Real-world power tests model FPGA's thermal characteristics

Jeremy Willden, Ad Hoc Electronics, Pleasant Grove, UT

Given ever-increasing clock frequencies and higher gate counts, many systems that include high-performance FPGAs (field-programmable gate arrays) routinely require a thoroughly analyzed thermal model. While working on a project that contained an FPGA, I realized that I had insufficient data to determine the FPGA's exact power dissipation, which my mechanical-engineering colleague required to construct a system model for thermal analysis using Flomerics' (www.flomerics.com) Flotherm software.

Although we had created fully functional hardware, we hadn't included a method of measuring the FPGA's exact power consumption, a problem further complicated by the presence of multiple power-supply voltages that fed additional circuits on the board. Although the manufacturer's FPGA-power-calculation spreadsheet allowed us to approximate the circuit's total wattage, the calculated values related only to its internal power consumption and didn't account for power not dissipated in the chip—that is, power delivered to I/O lines that drive other devices. To further confuse the issue, we lacked information about the FPGA package's thermal properties.

My mechanical-engineering colleague and I decided to create a controlled experiment by placing a functioning PCB (printed-circuit board) inside an improvised temperature chamber—a cardboard box. We would apply a precise amount of power only to the FPGA, measure its package's external temperature, and measure its internal die temperature using the FPGA's on-chip temperature-sensing diode. We would then model the experiment in Flotherm and adjust the package's thermal properties until the simulation's results matched the measurements.

Next, we would measure the FPGA's temperature while it executed an actual VHDL application within the temperature-controlled environment and work backward to determine the true power dissipation. Finally, we would create an accurate Flotherm model that would allow completion of a properly rated heat-sink design for the FPGA.

The only nonobvious part of this process involved how to dissipate a controlled amount of power within the FPGA. Acting on a flash of inspiration, I connected a nonfunctional PCB to a power supply and reversed the polarity of the FPGA's core voltage. By doing so, I applied forward bias to the FPGA's internal parasitic diodes that connect between power and ground and the device's I/O-voltage rails and protection diodes (**Figure 1**). Under normal circumstances, these diodes remain reverse-biased and dissipate no power. Reversing the power-supply polarity forward-biased the diodes, dissipating power and heating the FPGA's die.

To obtain an exact voltage measurement, I added Kelvin-connected sense leads to the FPGA's power pins. I configured the power supply to operate in constant-current mode and adjusted its output to deliver exactly 2W of power as determined by multiplying the supply current and the voltage at the FPGA's power pins. My colleague configured the test probes' placement and performed the temperature measurements. Upon completion of our experiments, the temperatures that the Flotherm model predicted agreed with those we measured in our system's final configuration, including its heat sink, within a margin of 3 to 4°C. EDN

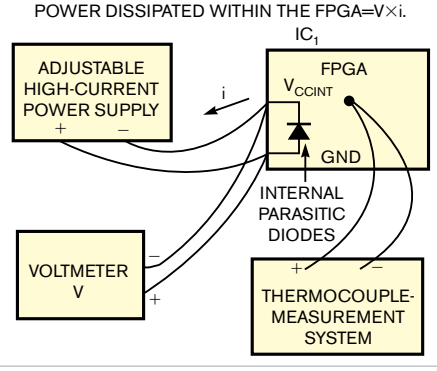

Figure 1 To measure an FPGA's thermal parameters, apply controlled forward bias to its internal parasitic diodes, thereby dissipating a known amount of power within its die.

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CPLD autonomously powers battery-powered system

Rafael Camarota, Altera Corp, San Jose, CA

A common industrial and consumer application is a system that samples an environmental condition, such as GPS (global-positioning-system) location, voltage, temperature, or light, at a wide interval, such as once every minute. This type of system is becoming increasingly wireless and battery-powered; it wakes up every minute, takes a sample, transmits data to a central data-collection terminal, and then goes back to sleep. This Design Idea uses a small portion of an Altera (www.altera.com) EPM240-T100 CPLD (complex programmable-logic device) with a few discrete capacitors, resistors, diodes, and MOSFETs to autonomously wake a CPLD-based system from a full power-down state to an on state using an RC-timer circuit. This approach results in minimal

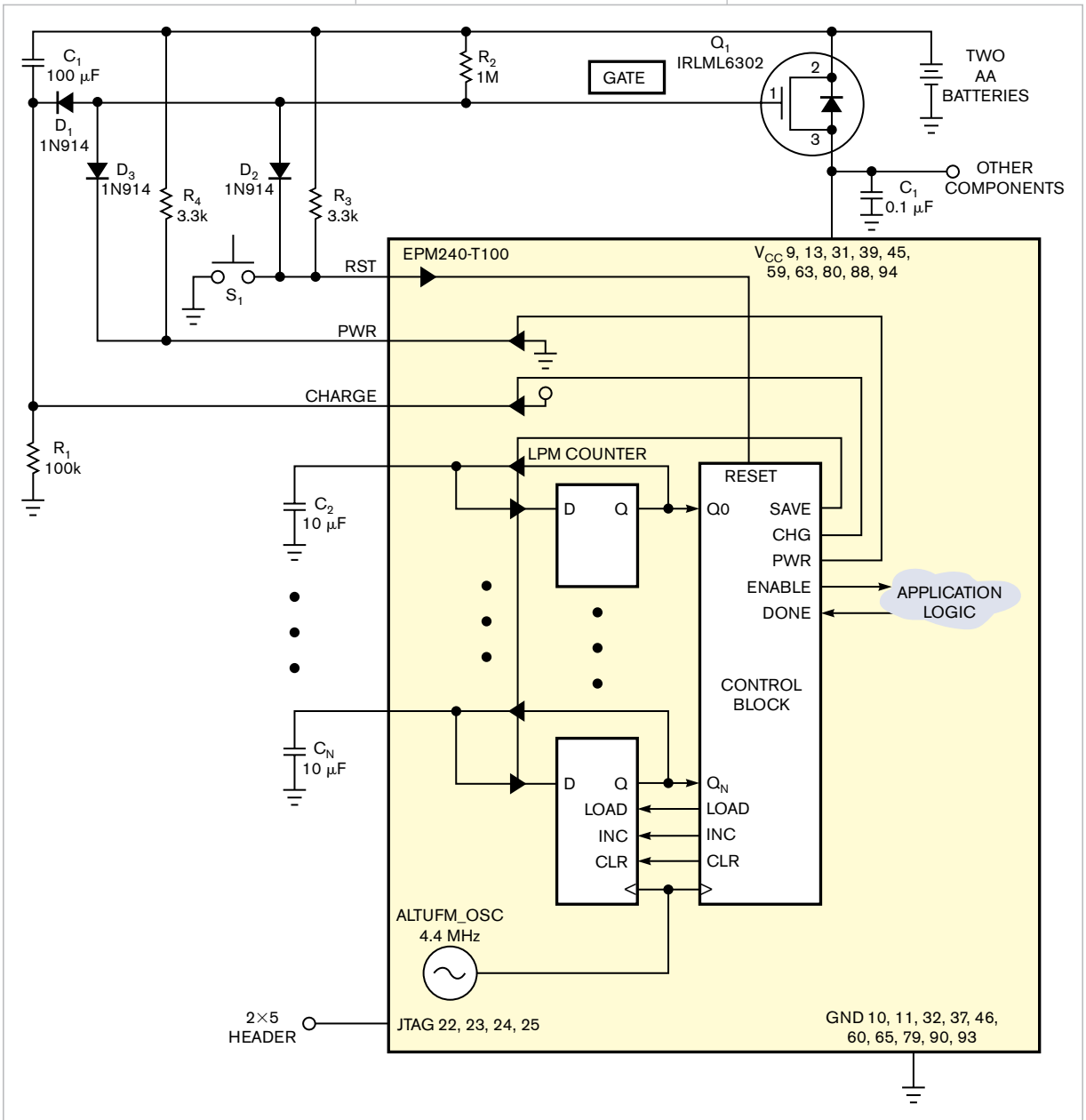

Figure 1 The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

power consumption during samples when the power is on and between samples when the system, except for the RC circuit, is effectively off.

Figure 1 shows the basic CPLD on/off timer. Q_1, an IRLML6302 P-channel MOSFET, is the power-control switch for the system. When the gate node is at V_{CC}, which R_2 pulls up, the power to the CPLD and the entire system is off, leaving only the RC circuit to use a minute amount of power. The CPLD comprises a control block, a 4.4-MHz internal oscillator, a 3-bit register, and six I/Os.

Figure 2 shows the state machine of the control block. The outputs in the state box are high, and all others are low. The dashed line from power-down to power-up represents the time delay, which the RC circuit comprising R_1 and C_1 measures when the system is off. Switch S_1 turns on and initializes the circuit. When S_1 closes, D_2 drives the gate node low, consequently turning on Q_1 when the gate voltage is 0.7V below V_{CC}. The EPM240-T100 is then operating in the power-up state less than 200 µsec after Q_1 applies power. The power-up state drives the power node low, which holds the gate voltage at 0.7V, keeping Q_1 on after the switch is open. The power-up state also drives the charge node to V_{CC}. This action charges the negative terminal of C_1 to V_{CC}. Because reset=0, the control block goes to the reset state and Register 1 gets reset. Once S_1 opens, the control block goes to the enable state and drives the enable signal to one.

The sample-and-transmit circuit then begins operation and drives the done signal to zero. Once the sample and transmit are complete, the done signal becomes one, and the control block goes to the save state. The save state charges capacitors C_2 to C_N based on the value in Register 1. The save state is active for 100 µsec, allowing the outputs to fully charge the 10-µF capacitors. After 100 µsec, the control block goes to the power-down state, which stops driving the charge and power nodes. R_4 pulls the power node high, leaving R_2 to pull up the gate node.

CAPACITORS C_2, C_3, AND C_4 ACT AS NONVOLATILE MEMORY, STORING THE COUNT OF PREVIOUS POWER CYCLES.

Once the gate node reaches $V_{CC} - V_{TQ1}$ at about 2.3V, Q_1 shuts off power to the system. All EPM240-T100 I/O is in a high-impedance state and does not affect the gate or charge nodes. The charge node starts at V_{CC} and begins to discharge through R_1 once power is off. Once the charge node drops to 2.3V, D_1 pulls down the gate node. Once the charge node reaches 1.6V, the gate node reaches 2.3V, and Q_1 turns on. The time for Q_1 to turn on is slightly less than the τ of R_1 and C_1. Off time equals $R_1 \times C_1 = 100{,}000 \times 0.0001 = 10$ sec.

The device powers up in the power-up state but moves quickly to the sample state. The sample state reads the value on capacitors C_2, C_3, and C_4. These capacitors act as nonvolatile memory, storing the count of previous power cycles. If the Register 1 value sampled on C_2 through C_4 is less than 7, then the control block goes to increment, and the Register 1 value increments by one. Then, the control block again goes to the save state to charge C_2 through C_4 to a new binary value, 001. The device powers down again. On the eighth power cycle, or about 80 seconds after power-up, the control block moves to the enable state, thus enabling a new sample-and-transmit sequence. This process repeats every 80 seconds. You can change the period by adjusting C_1 and R_1 and by changing the Register 1 size and count between enable cycles. Based on an 80-second period comprising eight smaller power-up samples, test, and power-down cycles, the duty cycle for power is less than 3%; therefore, this approach increases battery life by as much as 33 times. EDN

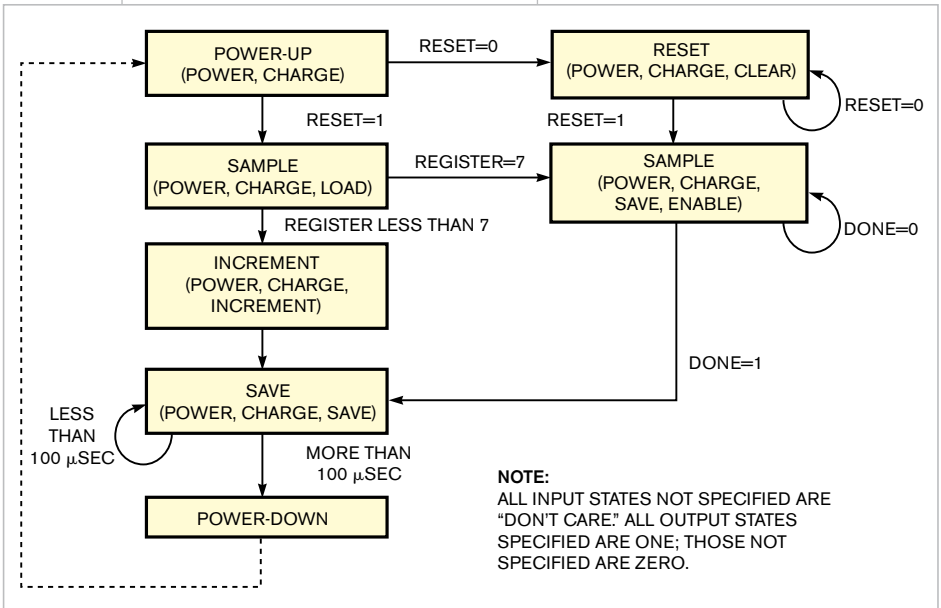

Figure 2 In the state machine of the control block, the outputs in the state box are high, and all others are low.

Find hex-code values for microcontroller's ADC voltages

Harry Gibbens Jr, Deafworks, Provo, UT

This Design Idea is for low-end, eight-pin, flash-memory, 8-bit microcontrollers, such as the MC68HC908QT4A from Freescale (www.freescale.com), but it would apply to any 8-bit microcontrollers that use the ADC feature. In a nutshell, the ADC converts an input-analog-voltage level to a digital-signal format. The digital-signal format has an 8-bit hex-code value, such as $00. The microcontroller "sees" the input-analog-voltage level from its ADC ports ranging from $00 at V_{SS} to $FF at V_{DD}. Based on those hex-code values, there are a total of 256 ticks. The input voltages between V_{SS} and V_{DD} represent a straight-line linear conversion. In other words, the higher the input voltage, the higher the hex-code value.

The difficulty is that a programmer who needs to write assembly code for a programming algorithm must know what the hex-code value is for a different input-analog-voltage level—1.6V, for example. Referring to the microcontroller's specs and even contacting its manufacturers do not yield satisfactory answers.

However, this Design Idea presents a solution to the problem. Given the microcontroller's power operating-voltage source, V_{DD}, use the following simple formula to obtain the hex-code value corresponding to an identified input-analog-voltage level: $V_{IN}/(V_{DD}/255)$=result value=hex code. Note that you must round off the result value to a whole number before converting to a hex-code value for better accuracy. The following sample calculation finds the hex-code value for a measured input-analog-voltage level of 1.6V when using a known microcontroller's V_{DD} of 5V: 1.6V/(5V/255)=81.6=82, or $52. EDN

Cheap and easy inductance tester uses few components

Al Dutcher, Consulting Engineer, Paulsboro, NJ

In the absence of expensive test equipment, the circuit in **Figure 1** offers a simple and rapid alternative method of measuring inductance. Its applications include verifying that an inductor's value falls close to its design parameters and characterizing magnetic cores of unknown parameters that accumulate in the "junk box." As designed, the circuit tests most inductors for use in power supplies and many inductors for RF circuits.

The circuit comprises two cascaded common-emitter-amplifier stages that form a nonsaturating, cross-coupled flip-flop. A common-emitter stage performs a phase inversion, and two cascaded stages form a noninverting feedback amplifier with gain that produces regeneration. Without the presence of the inductor that is undergoing test, L, regeneration occurs at dc, and the circuit behaves as a bistable flip-flop that assumes either of two stable states. Connecting the inductor reduces the dc positive feedback to below the regeneration level. Thus, regeneration can occur only at ac, and the circuit becomes an astable oscillator.

Keeping the transistors out of saturation speeds the circuit's operation by minimizing the transistors' storage time. Although virtually any type of high-speed, small-signal RF transistor provides adequate switching speed, lower frequency devices also work but decrease the low-inductance-measurement range. The circuit's frequency of oscillation is inversely proportional to the inductance that is undergoing test, and you can use either a frequency counter or an oscilloscope to measure the frequency of oscillation.

Figure 2 shows the waveform produced by an inductor with a value of approximately 100 µH. The frequency of oscillation depends on the L/R time

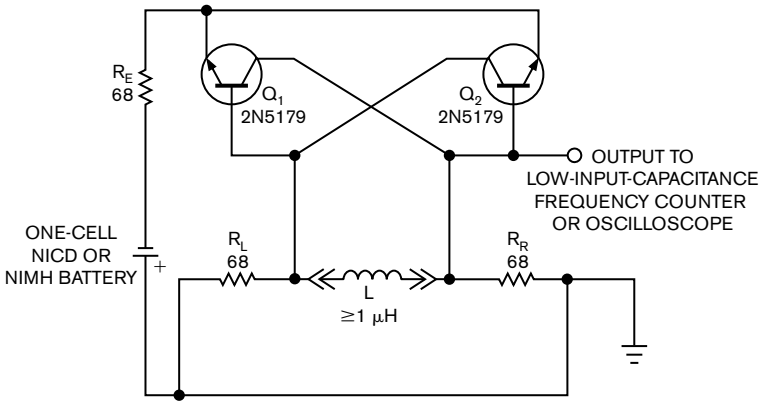

Figure 1 An inductance-test oscillator comprises two transistors and a few passive components. (Editor's note: For best results, minimize the lengths of all components' leads.)

constant comprising the inductance under test and resistors R_L and R_R. The time the waveform takes to change its state is directly proportional to the inductance, and, for one-half cycle, it approaches $T_{HALF}=L/100$. The period of a full oscillation cycle is twice that amount, or $T_{FULL}=L/50$. Solving for the inductance yields $L=50\times T_{FULL}$. As an alternative, the frequency is inversely proportional to the inductance, or $f_{OSC}=50/L$. Using a frequency counter allows measurement of inductance as $L=50/f_{OSC}$.

The circuit's finite switching speed of approximately 10 nsec imposes a lower floor of 1 µH on its measurement range. You can measure a small inductance by connecting it in series with a larger inductance, noting the reading, measuring the larger inductance alone, and subtracting the two measurements.

Although the circuit imposes no upper limit on inductance values, when the inductor's ESR (equivalent-series resistance) exceeds approximately 70Ω, the circuit stops oscillating and reverts to bistable operation. The circuit measures values of all inductors and transformer windings except for small, low-frequency iron-core devices that present a high ESR. For greatest accuracy, use a low-input-capacitance instrument to measure the frequency of oscillation.

A single NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) rechargeable cell provides power for the circuit. These cells present a relatively flat voltage-versus-time discharge characteristic that enhances the circuit's measurement accuracy. The circuit consumes approximately 6 mA during operation. EDN

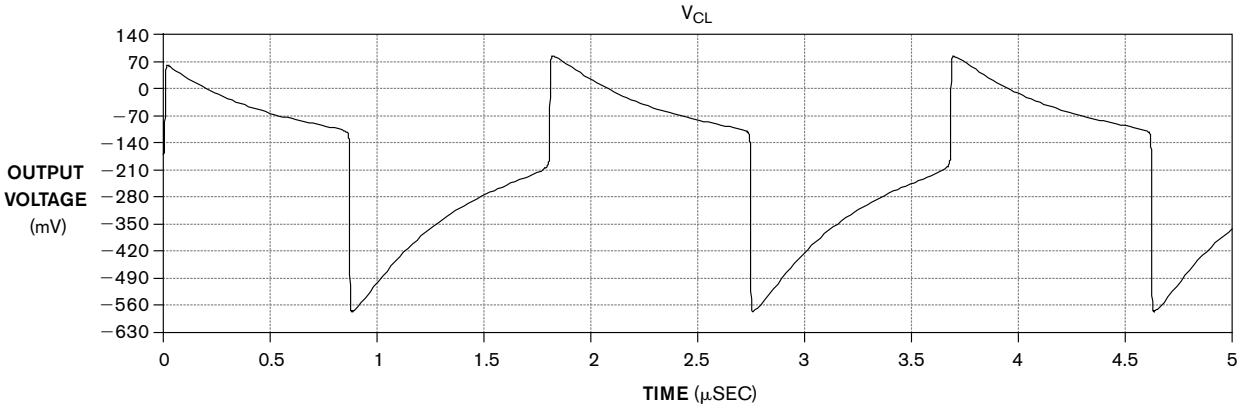

Figure 2 Testing an inductor with a value of approximately 100 µH produces this output waveform.

Add a manual reset to a standard three-pin-reset supervisor

Derek Vanditmars, Delta Controls, Surrey, BC, Canada

Adding a manual reset to a design usually involves designing in a new part with a manual-reset input. But, by adding a couple of low-value resistors, a standard three-pin-reset supervisor can work in most applications. The circuit in **Figure 1** ensures a clean $\overline{\text{RESET}}$ signal during and after you have pressed the manual-reset button. When you activate the manual-reset button, the supply voltage drops below the reset supervisor's minimum reset threshold because of the R_1/R_2 voltage divider formed when S_1 is active. This action causes the reset supervisor to activate its $\overline{\text{RESET}}$ output. When you realease S_1, the supply voltage returns to above the reset-supervisor maximum-reset threshold, and $\overline{\text{RESET}}$ remains active for the timeout period of the reset supervisor.

When you do not press S_1, R_2 has a voltage drop arising from the reset supervisor's supply current and $\overline{\text{RESET}}$ output loading. For most reset supervisors, the maximum supply current is 50 µA. For most designs, the $\overline{\text{RESET}}$ output goes to one or more CMOS inputs that require about 10 µA each. With two CMOS devices connected to $\overline{\text{RESET}}$, the total current through R_2 would be (2×10 µA)+50 µA=70 µA. The voltage drop across R_2 due to the current flow effectively adds 70 µA×100Ω=7 mV to the reset su-

pervisor's reset-threshold voltage.

You should consider several tradeoffs for the selection of values for R_1, R_2, and C_1. The value of the local bypass capacitor, C_1, for the reset supervisor should be low enough to allow the reset supervisor to detect transient supply-voltage drops. The time constant of R_2 and C_1 determines this factor; in this example, the time constant is $100\Omega \times 0.01\ \mu F = 1\ \mu sec$. This figure is typically much higher than the decay rate of a regulated power supply that has lost power.

When you activate S_1, current flows through R_1 and R_2. In the circuit in **Figure 1**, the current flow when you activate S_1 is $3.3V/(100\Omega+100\Omega)=16.5$ mA. This amount of current would be OK for a line-powered system but may not be OK for a battery-powered system. You can reduce the current by increasing the value of R_1 and ensuring that the reset supervisor's supply voltage drops below the minimum reset threshold. You can also increase the value of R_2, along with that of R_1, but doing so will cause increased voltage drop and slower response to transients. Note that the increased current of the manual reset occurs only while the manual reset is active, and typical system current drops while $\overline{\text{RESET}}$ is active. EDN

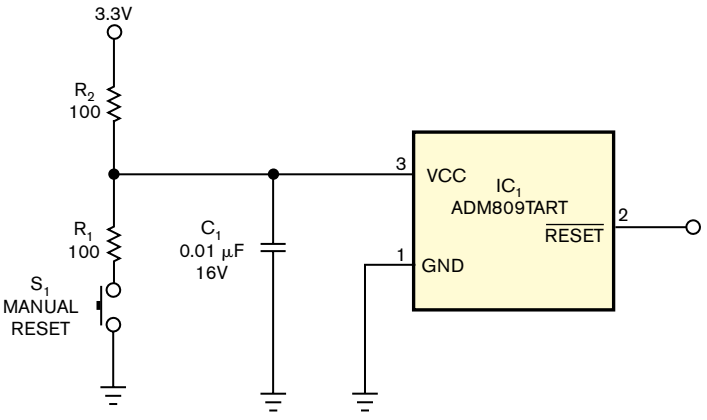

Figure 1 A pair of low-value resistors, a capacitor, and a pushbutton add a manual-reset function to a standard three-pin-reset supervisor.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Use a CFL ballast to drive LEDs

Christian Rausch, Unterhaching, Germany

Designers use ballast ICs, such as International Rectifier's (www.irf.com) IR53HD420, in CFLs (compact fluorescent lamps) for heating the filaments, igniting the lamps, and supplying the lamps with current (**Reference 1**). Manufacturers produce these ICs in high volumes, and they cost approximately $2. This Design Idea shows how you can use a CFL-ballast IC for driving LEDs instead of CFLs. A ballast IC essentially is a self-oscillating half-bridge for offline operation. It typically operates from 320V dc, which is approximately the same power as that from a 230V-ac mains rectifier or a 120V voltage doubler. The IC generates square-wave voltages with an amplitude of 320V p-p and a frequency of tens of kilohertz.

Usually, this square-wave voltage connects to a series combination of a CFL tube and a current-limiting inductor, L_1 (**Figure 1**). Together with a parallel capacitor and using the LC resonance, you can warm up, ignite, and supply the tube with current. This approach works well because CFL tubes have high impedances when they are off and low impedance when they are running. The tube voltage is typically 150V p-p.

By putting several LEDs in series and connecting them to a bridge rectifier, you can effect an imitation of a CFL, at least in the on-state. Imitating the off-state is less important, because LEDs need no ignition procedure. At the given values for R_T and C_T, the bridge runs at 70 kHz. The circuit supplies 64 LEDs with a current of approximately 80 mA. The infrared LEDs illuminate the field of view of a CCD camera in a machine-vision system. The circuit prototype uses a 2.7-mH inductor from a dead CFL.

The LED current comprises dc current plus a small ripple current; keep

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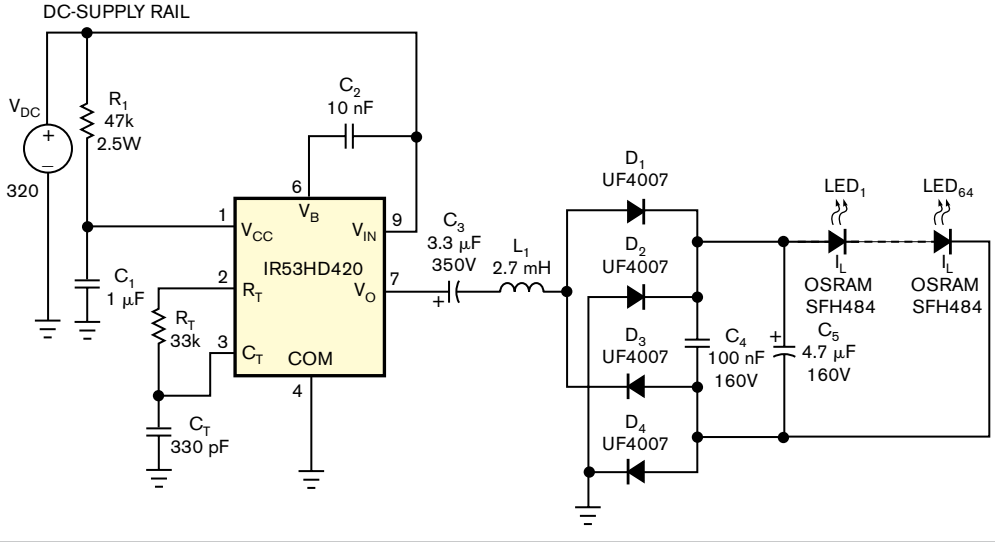

Figure 1 A CFL ballast drives a long string of LEDs.

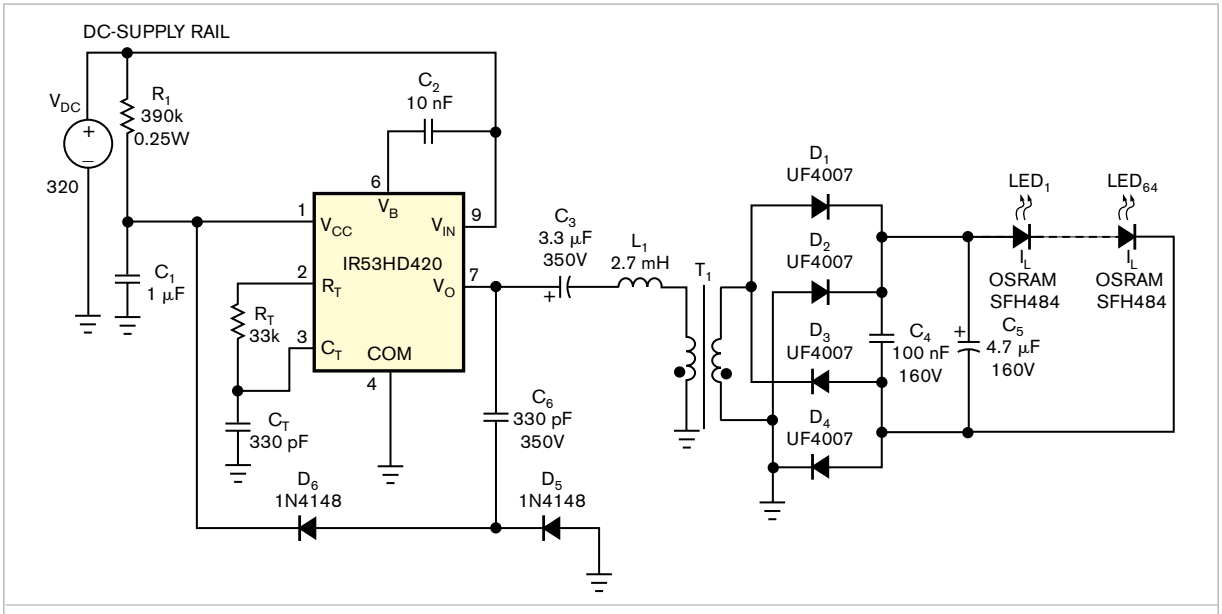

Figure 2 Adding a transformer to the circuit of Figure 1 allows you to connect as many LEDs as necessary.

the ripple current low for high efficiency and long LED lifetime. LED manufacturers usually demand values of a few percentage points. Such a low ripple current may be difficult to achieve with one electrolytic capacitor, C_5, but a parallel combination with an additional foil capacitor, C_4, works well enough in most cases. The voltage at the input of the LED rectifier is fairly constant during one oscillation period, so the inductor current has a triangular shape, which is good for EMC (electromagnetic compatibility). The equation for the average LED current is $I_{LEDAVG}=(½\times V_{DC}-N\times V_{FLED})/(4\times f\times L_1)$, where V_{DC} is the supply voltage, N is the number of LEDs in series, V_{FLED} is the LED forward voltage, f is the oscillation frequency, and L_1 is the inductance of the current-limiting inductor.

Although the circuit of **Figure 1** works well, it has some deficiencies that the circuit of **Figure 2** remedies by adding C_6, D_5, D_6, and T_1, wound on an EPCOS EP13 coil former, with an ungapped-EP13-core of T38 material with an inductance of 7000 nH. Both the primary and the secondary windings are 90 turns of 0.2-mm wire; the secondary winding is wound on top of the primary winding. Stray inductance is not important in this case, and the inductance for both the primary and the secondary windings is 50 mH. The circuit in **Figure 2** has several advantages over the one in **Figure 1**. For example, the supply current for the ballast IC of **Figure 1** must flow through R_1 and into the IR53HD420, where it gets clamped to 15.6V. At a supply current of about 6 mA, R_1 must dissipate more than 2W. In **Figure 2**, R_1 can have a much higher value, because it must supply only a small start-up current. After start-up, a charge pump comprising C_6, D_5, and D_6 pumps enough current into the V_{CC} pin so that the internal zener diode clamps to 15.6V. The design equation for the charge pump is $I_{SUPPLY(AVG)}=f\times C_6 2\times V_{DC}-15.6V$. The dissipation of R_1 now stays below 0.25W.

WITH THE TRANSFORMER, YOU CAN GROUND ONE END OF THE LED STRING EITHER DIRECTLY OR THROUGH A CAPACITOR.

Also, the summed forward voltages of the LEDs in **Figure 1** must be smaller than one-half the supply voltage. For the circuit in **Figure 2**, by tailoring the transformer-winding ratio, you can connect as many LEDs as needed, as long as you do not exceed the ratings of the components. (LED voltages even higher than V_{DC} are possible.) A less obvious problem of the circuit in **Figure 1** is that the full voltage swing of the bridge appears at both ends of the LED string. This situation does not present a problem when all the LEDs are close together and the LEDs are close to the bridge. However, in many light fixtures, you wish to separate the LEDs from the electronics. Due to stray capacitances, this approach would lead to high capacitive currents from the LEDs to ground, corrupting the efficiency and producing EMC problems. With the transformer of **Figure 2**, you can ground one end of the LED string either directly, as shown, or through a capacitor. Now, you can use long cables to easily separate the LEDs from the electronics. EDN

REFERENCE

1 "IR53H420(D)420, Self-Oscillating Half Bridge," Preliminary Data Sheet No. PD60140-K, International Rectifier, Aug 19, 2003, www.irf.com/product-info/datasheets/data/ir53h420.pdf.

Photodiode amplifier exhibits one-third the output noise of conventional transimpedance amp

Glen Brisebois, Linear Technology Corp, Milpitas, CA

A conventional 1-MΩ transimpedance amplifier has at least 130 nV/√Hz of output-noise density at room temperature (**Figure 1**). You can consider the 130 nV as the theoretical noise floor limit of the amplifier because that is the noise density of the 1-MΩ resistor itself. Any noise in the op amp can only make things worse. Cooling the resistor to 77.2K, the temperature of liquid nitrogen, quiets it to 65 nV/√Hz, provided that it survives, but is that the only option? Can you beat the 130-nV theoretical noise floor without cooling?

Figure 2 shows one way. IC_1, a Linear Technology (www.linear.com) LTC6240, provides an overall transimpedance gain of 1 MΩ, but it has an output-noise density of only 43 nV/√Hz, about one-third of a conventional 1-MΩ transimpedance amplifier at room temperature. It achieves this figure by taking an initial transimpedance gain of 10 MΩ and then attenuating by a factor of 10. The transistor section provides voltage gain and works on a 54V supply voltage to guarantee adequate output swing. By achieving an output swing of 50V before attenuation, the circuit maintains an output swing to 5V after attenuation. The 10-MΩ resistor sets the gain of the transimpedance-amplifier stage and has a noise density of 400 nV/√Hz. After attenuation, the amplifier's effective gain drops to 1 MΩ, and the noise floor drops to 40 nV/√Hz, which dominates the observed 43 nV/√Hz. To achieve this noise performance by cooling requires a temperature of 33K, much colder than liquid nitrogen. Note also that the additional benefit of this method is that it divides the offset voltage of the op amp by 10. The worst-case output offset for this circuit is 105 µV over temperature. Bandwidth is 28 kHz. EDN

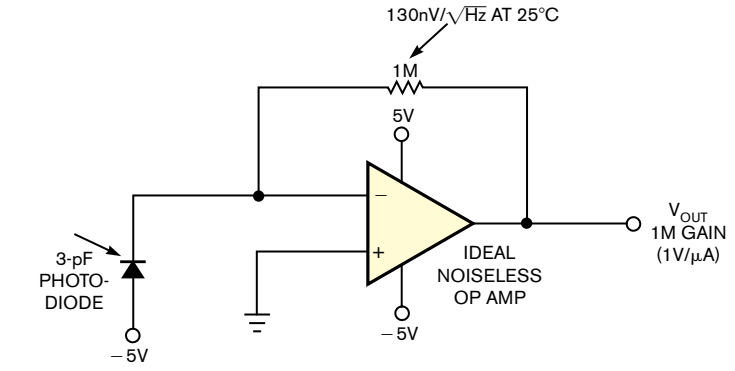

Figure 1 A conventional 1-MΩ transimpedance amplifier exhibits 130 nV/√Hz of output noise, even with a noiseless op amp. Cooling the resistor reduces the noise, but can you do better without cooling?

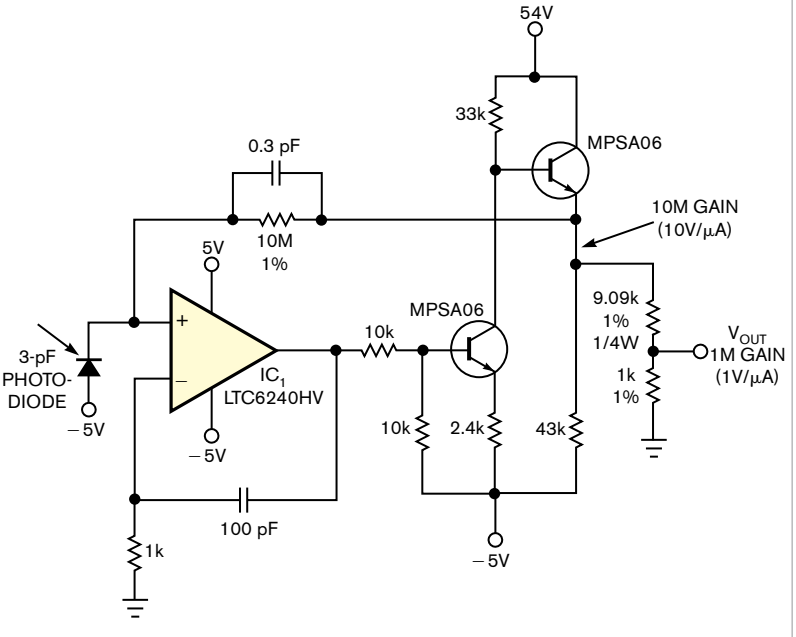

Figure 2 This effective 1-MΩ transimpedance amplifier has only 43 nV/√Hz of output noise. The circuit takes 10 times the high amplifier gain and then attenuates by a factor of 10. The LTC6240 has low current and voltage noise. The discretes allow for high output swing at the 10-MΩ gain node, so that a 0 to 5V output swing remains after attenuation.

Microcontroller programmer taps power from PC's serial port

GY Xu, XuMicro, Houston, TX

Just like a PC's USB port, the serial port on a PC can also in some cases serve as a power supply. A USB port can provide as much as 500 mA at 5V, but a serial port provides less power. Even with the serial port's limited capacity, serial-port power can still be a convenient power source for today's electronics. One obvious example is to light up an LED. **Figure 1** shows a simple way to tap the serial port's power. Under Windows XP, this task requires appropriate software. You can download the **listings** for this Design Idea from www.edn.com/070426di and run the program pwon.exe for this demo.

A far more useful case is to provide a power supply for the microcontroller programmer, which has no wall wart. Today's microcontrollers consume less current than their predecessors, so you can easily tap the serial port's power for an Atmel (www.atmel.com) AVR programmer (**Figure 2**). The programmer uses only two chips: IC_1, a Maxim (www.maxim-ic.com) DS275 for the RS-232 interface between the programmer and the PC, and IC_2, an Atmel AT89C2051 firmware microcontroller, which is the heart of programmer and handles all programming chores and communications with the PC. IC_3 is the AVR microcontroller, an AT90S1200/2313. You can also substitute an eight-pin AT90S2323/2343 or a 40-pin AT90S4414/8515. The SPI (serial-peripheral-interface) bus performs the device programming.

The basic requirement is that the circuit's total current consumption must be less than 10 mA. The programmer uses two RS-232 pins: DTR (data-terminal ready) and RTS (request to send) as a minuscule power source. The

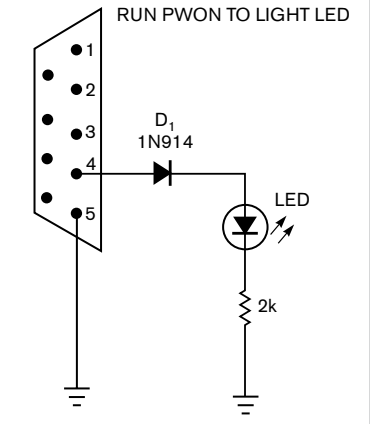

Figure 1 With the aid of a simple PC program, you can tap a PC's serial port for enough power to light an LED.

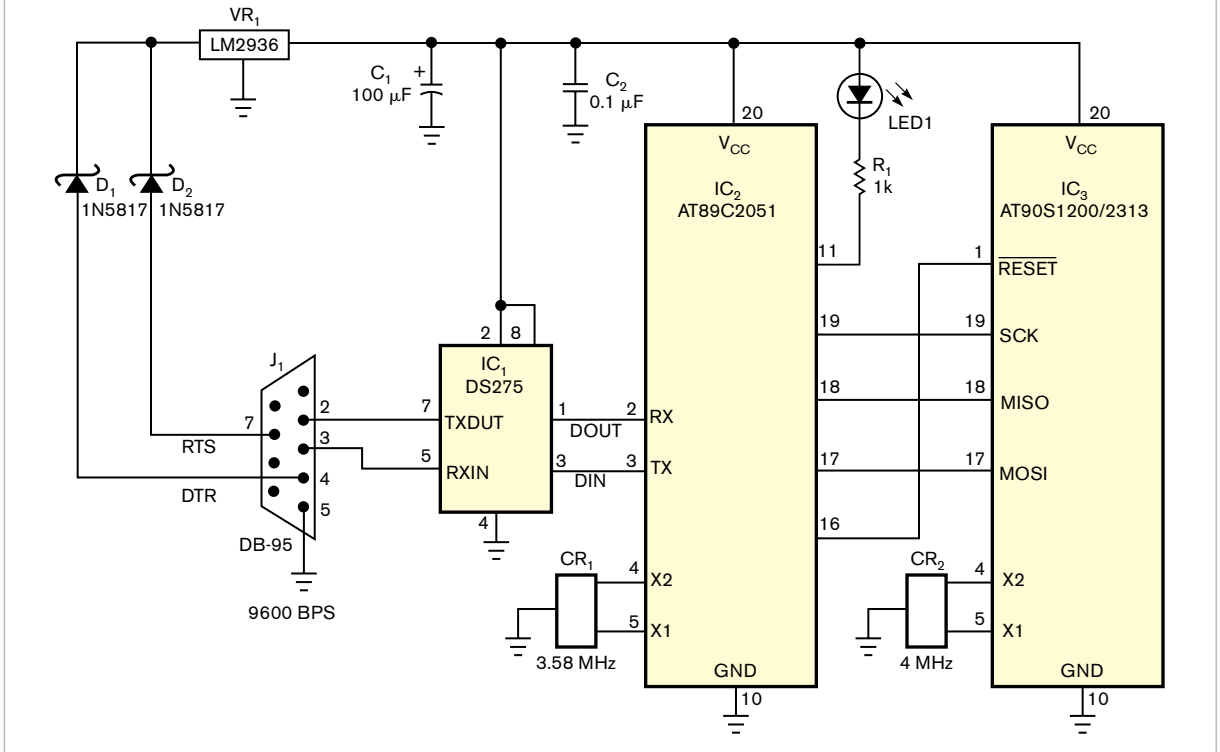

Figure 2 This microcontroller programmer gets its power from the PC's serial port.

outputs from these pins arrive at a pair of Schottky diodes, D_1 and D_2, which cause a forward-voltage drop of only 0.3V, and then to VR_1, an LM2936 low-dropout-voltage regulator. Capacitors C_1 and C_2 smooth the output voltage. To reduce current consumption, LED_1 uses a 1-kW current-limiting resistor, and the control firmware turns it on only after the programming task completes; otherwise, LED_1 is off.

The circuit for the programmer is easy to build. The 8051-like AT89C2051 has 2 kbytes of flash program memory. It needs no components connected to the reset (Pin 1), and it uses the 3.58-MHz ceramic resonator to generate 9600 bps for communication with the host PC. In addition to eliminating an external power supply, the programmer needs only firmware design. The programmer uses the Windows HyperTerminal program to communicate with the programmer firmware. You configure the HyperTerminal to use a COM port with 9600 bps and set the flow-control parameter to XON/XOFF.

You can program the firmware files in **Listing 1** into the AT89C2051 using any 8051 programmer, and the **listing** includes one AVR sample demo file to program into the AT90S1200/2313. EDN

Circuit charges supercapacitors to 7V from USB power

Fran Hoffart, Linear Technology, Santa Clara, CA

Charging a supercapacitor from a 5V USB port may seem simple at first, but to charge three supercapacitors to 7V and to limit the input current to the 500 mA maximum limit on the USB port is somewhat more difficult. The circuit in this Design Idea uses a Linear Technology (www.linear.com) LTC3458 switching regulator to charge three series-connected supercapacitors and provide input-current limiting. This regulator limits the input current, as the capacitors charge, to less than 500 mA to satisfy USB specifications, and it provides the boost function to charge the capacitor to a voltage greater than the 5V USB input. Once the supercapacitor charges, the regulator maintains 7V at the output and can supply a continuous load of approximately 300 mA in addition to brief current surges of several amperes without exceeding 500 mA at the input. Typical loads requiring high surge current can include motors when initially starting up.

Removing the input voltage shuts down the regulator and reduces the capacitors' discharge current to approximately 3 µA, essentially the current through the voltage programming resistors. Manual shutdown is also possible by pulling the shutdown pin low, but, with the input voltage still applied, the capacitors' discharge current increases to approximately 30 µA. The circuit in **Figure 1** is programmed for a switching frequency of 1 MHz with an output voltage of 7V. A resistor on

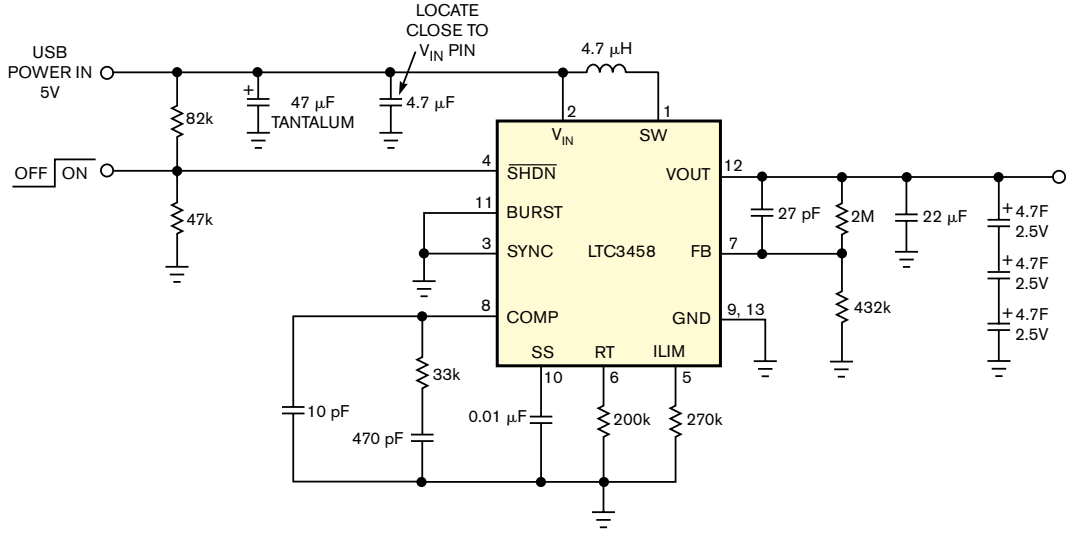

Figure 1 This circuit has a switching frequency of 1 MHz and an output voltage of 7V.

the current-limiting pin, ILIM, sets the input-current limit. The circuit contains all surface-mount components, and the high switching frequency allows the use of tiny inductors and capacitors, thus reducing total circuit size. You should use good PCB (printed-circuit-board)-layout practices.

The series-connected Polystor aerogel supercapacitors, available from various online sources, are each rated at 4.7F at 2.5V and feature a typical ESR (equivalent-series resistance) of 25 mΩ, thus allowing high discharge current. Low leakage current provides long capacitor-voltage-holdup time. The individual capacitor voltages track within 100 mV when charging and charge completely in less than 60 seconds at the rated charge current. **Figure 2** shows the capacitors' voltage, charge current, and resulting current drawn from the USB port when charging. EDN

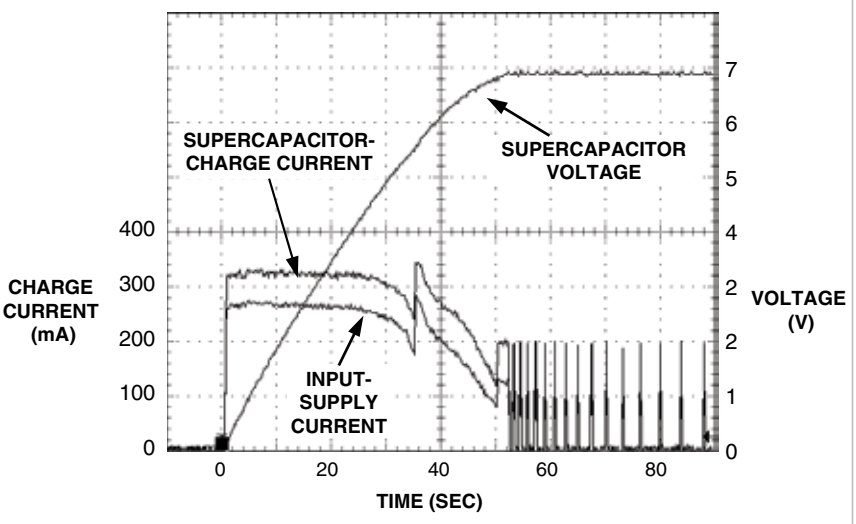

Figure 2 These curves show the super capacitors' voltage and charge current. Note that the charging current is 300 mA—the USB maximum allowable current draw.

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READERS SOLVE DESIGN PROBLEMS

Microcontroller functions as voltmeter

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The circuit in **Figure 1** is an extension of a previous Design Idea on how to use an analog input in a microcontroller lacking a built-in ADC, and it takes into account tricks from another Design Idea on how to drive a seven-segment LED display without external switching transistors (**references 1** and **2**). This circuit adds a serial link and needs only a twisted pair to send each measurement to a compatible PC. The serial link was tested using a Microsoft (www.microsoft.com) Hyper Terminal configured at 115,200 baud; at 8, N, and 1; and with no flow control.

Briefly, the software drives one seven-segment LED display at a time, through lines RA0 and RB7. Setting the RA0 output high and RB7 as the

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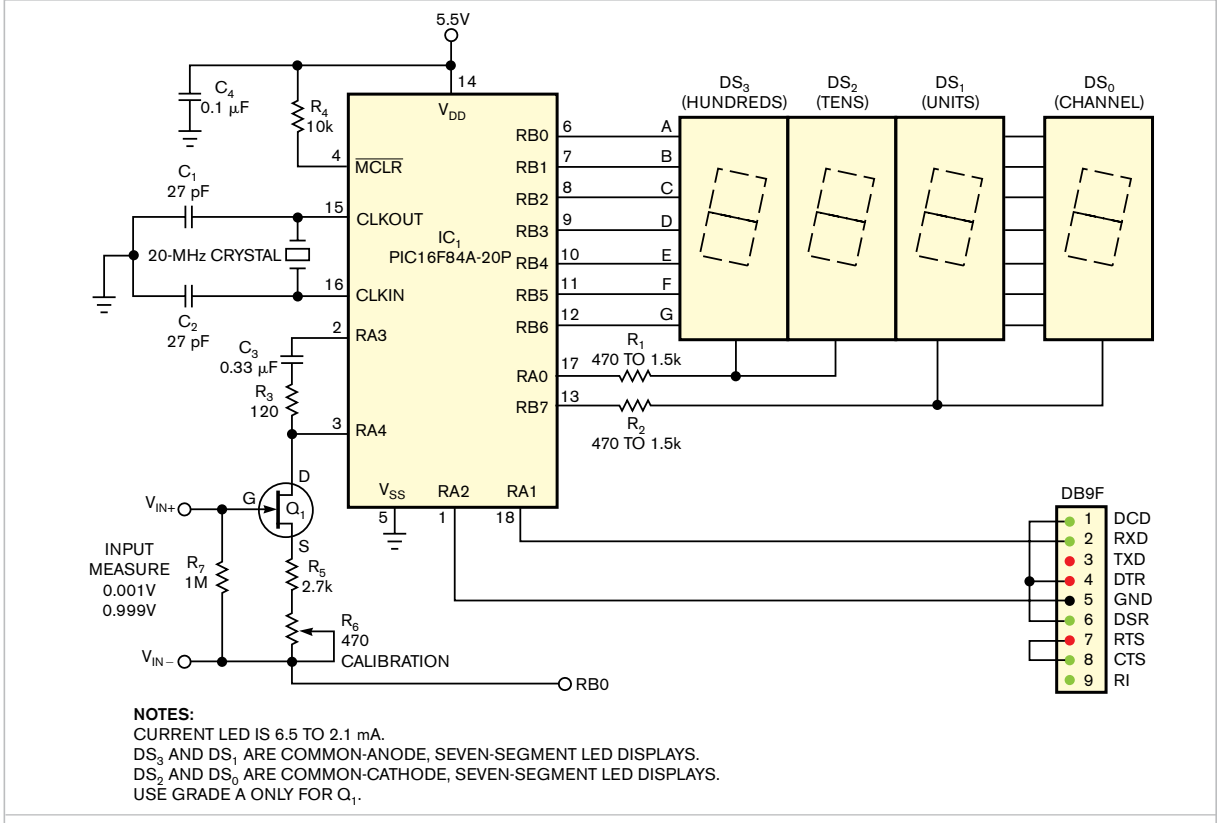

NOTES:
CURRENT LED IS 6.5 TO 2.1 mA.
DS_3 AND DS_1 ARE COMMON-ANODE, SEVEN-SEGMENT LED DISPLAYS.
DS_2 AND DS_0 ARE COMMON-CATHODE, SEVEN-SEGMENT LED DISPLAYS.
USE GRADE A ONLY FOR Q_1.

Figure 1 By using common-anode and common-cathode, seven-segment LED displays, the I/O ports of a microcontroller can drive the displays without using additional external components.

input activates common-anode display DS_3. Setting the RA0 output low and RB7 as the input activates common-cathode display DS_2. With RA0 as the input, setting the RB7 output high activates common-anode display DS_1, and, with RA0 as the input, setting the RB7 output low activates common-cathode display DS_0. While successively activating one display, only one line, RB0 to RB6, is configured as an output to drive one LED segment. This design no longer is limited to a V_{DD} of 3V or lower, because LEDs inversely connect in parallel, so the forward voltage of one diode limits the reverse voltage of the other. Using a red-diode display requires 1.6V.

Figure 2 illustrates the new aspects of this Design Idea. Q_1, R_5, and R_6 act as an equivalent variable resistor, R_X, which charges capacitor C_3. Instead of pulling R_X to ground, just connect it to one I/O—RB0, for example—of the microcontroller. If RB0 is an output with a low state, then the first analog channel activates, and the measure subroutine counts pulses of charge as high as 66% of V_{DD}; then, a look-up table converts this time delay to a three-digit millivolt value. To expand the number of analog inputs, you can connect as many as seven variable-resistor circuits in a parallel configuration—that is, each one connects between C_3 and one I/O line, RB1 through RB7. Notice that I/O lines connect to the display and also activate or deactivate the analog channels. When one analog-input channel activates through one I/O line with the output in the low state, the other lines are high-impedance inputs, which deactivate all other channels. Meanwhile, the display is off.

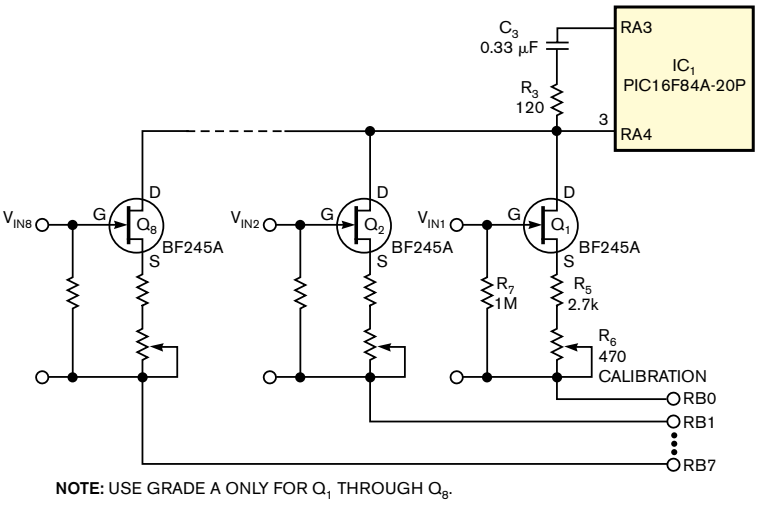

Figure 2 You can expand the number of voltages measured in Figure 1 by multiplexing additional transistor circuits.

The circuit in **Figure 1** also adds a simple serial link with no added components. If you connect two I/O lines, RA1 and RA2, configured as outputs, to RXD (Pin 2) and GND (Pin 5) of an RS-232 connector, you can reproduce, by software, positive and negative voltages with respect to ground of the PC's RS-232 port. When RA1 is high and RA2 is low, then RXD has a positive voltage of 5V with respect to ground of the PC's RS-232 port. When RA1 is low and RA2 is high, then RXD has a negative voltage of −5V with respect to ground of the PC's RS-232 port. **Listing 1**, available at www.edn.com/070510di1, gives a practical example with a PIC16F84A-20P. It is not optimized but is fully commented to make it easy to translate to another Microchip (www.microchip.com) midrange device, such as a PIC16F628A, that supports a frequency of 20 MHz with more I/O lines. EDN

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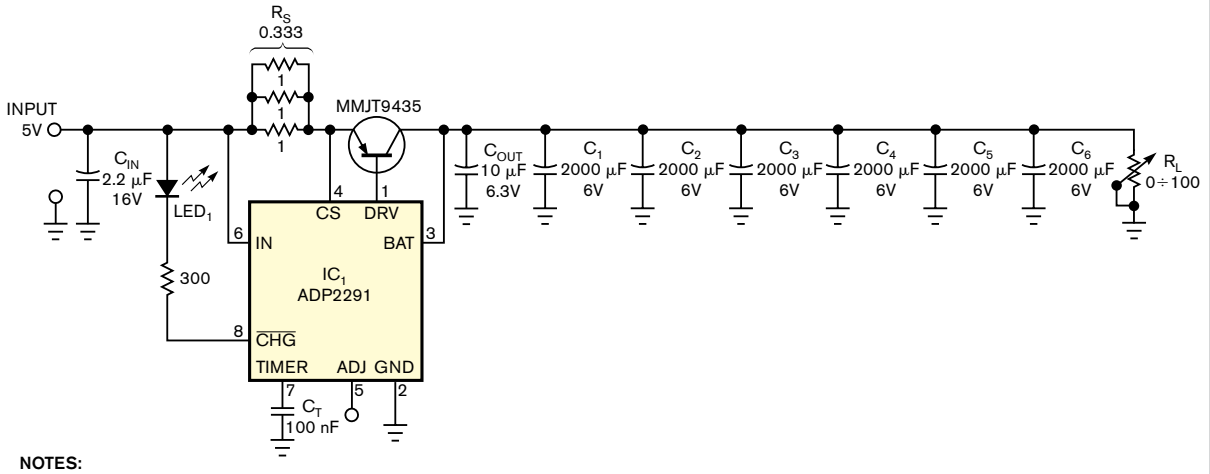
2 Benabadji, Noureddine, "Ultralow-cost, two-digit counter features few components," *EDN*, Aug 17, 2006, pg 69, www.edn.com/article/CA6360316.

Simple test setup performs functional testing of linear, single-cell lithium chargers

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Most currently available battery chargers are switched-mode types. Yet, a niche application exists for modern lithium-ion, single-cell linear-IC chargers, which have per-cell voltage of 4.2V. Further, the 5V-dc supplies, which are convenient for supplying single lithium-cell chargers, are ubiquitous. A linear charger charges the lithium cell from the 5V supply voltage at an efficiency, η, of approximately 4.2V/5V, or 84%. Although this value is ideal, the practical value is somewhat lower because of the power consumption of the charger's control circuitry. However, its efficiency is comparable with that of the switched-mode chargers. Linear chargers also provide some additional



NOTES:
C_{IN} AND C_{OUT} ARE TANTALUM-CHIP CAPACITORS.
C_1 THROUGH C_6 ARE ALUMINUM-FOIL CAPACITORS.
C_T IS A CERAMIC-CHIP CAPACITOR.
LED_1 IS A 0805-SIZE, RED-CHIP LED.

Figure 1 A handful of off-the-shelf components allows you to qualitatively and quantitatively check the operation of a linear lithium single-cell charger.

benefits. They produce almost no EMI (electromagnetic interference), they require no inductors, and they require fewer capacitors than do switched-mode chargers.

The test setup in **Figure 1** employs IC_1, an Analog Devices (www.analog.com) ADP2291 for a lithium-cell linear charger. The device comes in 3×3-mm LFCSPs and QFN packages. The otherwise-welcome small dimensions of this IC pose an inspection problem. After soldering in the IC, you must perform a functional test of the charging circuit. You cannot rely on a visual inspection of solder joints, which are 0.5 mm apart.

In the charger circuit in **Figure 1**, for testing purposes, a bank of electrolytic capacitors substitutes for the lithium cell, dramatically reducing the charging interval and cutting the test time to seconds. Additionally, charging a capacitor has a well-defined course, and you can easily delete all previous charging and discharging by metallically short-circuiting the capacitor.

Also, a linear charger allows you to discharge the capacitor to 0V, which a lithium cell does not. After powering-on the circuit, you should momentarily light and then dim the LED annunciator to ensure that the charger is properly functioning. You estimate the time that the LED is on using the following **equation**:

$$t_{LEDON} \approx C\left(\frac{V_T}{I_{PR}} + \frac{V_{OUT}-V_T}{10I_{PR}}\right) = \frac{C}{I_{PR}}(9V_T + 1V_{OUT}),$$

where V_T is 2.8V, the threshold value of output voltage at which the charger enters its fast-charging mode; C is the total capacitance of the bank of capacitors that connect to output; I_{PR} is the precharge current; and V_{OUT} is 4.2V, the nominal output voltage at the end of the charging. The charge-current level is about 10 times that of the precharge mode. This condition occurs when you leave the ADJ (adjust) pin of the IC open. The first term in the parentheses of the **equation** corresponds to the precharge interval, and the second one expresses the charge interval. For a total capacitance of 0.012F, the precharge current is 46.5 mA, and the on-time of the LED is approximately 0.76 sec.

You can determine the value of the output threshold voltage by slowly turning the rotor of the variable-load resistor, R_L, from the minimum value of resistance until the LED dims. At that instant, you stop the rotor movement by disconnecting one end of the load resistor and measuring its value with an ohmmeter. The value of precharge current is then the output voltage divided by the measured value of the load resistor and the output voltage, or 4.2V. For the values of components in the **figure**, the experimentally determined value of a 44.4-mA precharge current is consistent with the typical value of 45 mA when the value of the current-sensing resistor is 0.33Ω (**Reference 1**).

You can measure the value of the threshold output voltage, V_T, as follows: Turn the rotor of the load resistor from minimum value of resistance while measuring the output voltage of the charger with a voltmeter. When the output voltage increases to about 2.6V, slowly proceed until the output abruptly changes to 4.2V. Using this method, you can determine the threshold voltage to be 2.75V. EDN

REFERENCE

1 "Compact, 1.5 A Linear Charger for Single-Cell Li+ Battery," ADP2291, Analog Devices, 2005, www.analog.com/en/prod/0%2C2877%2CADP2291%2C00.html.

Microcontroller provides low-cost analog-to-digital conversion, drives seven-segment displays

Name withheld by author's request

A previous Design Idea demonstrated how to use shift registers to increase a microcontroller's output capabilities (**Reference 1**). This expanded Design Idea provides low-cost analog-to-digital conversion and

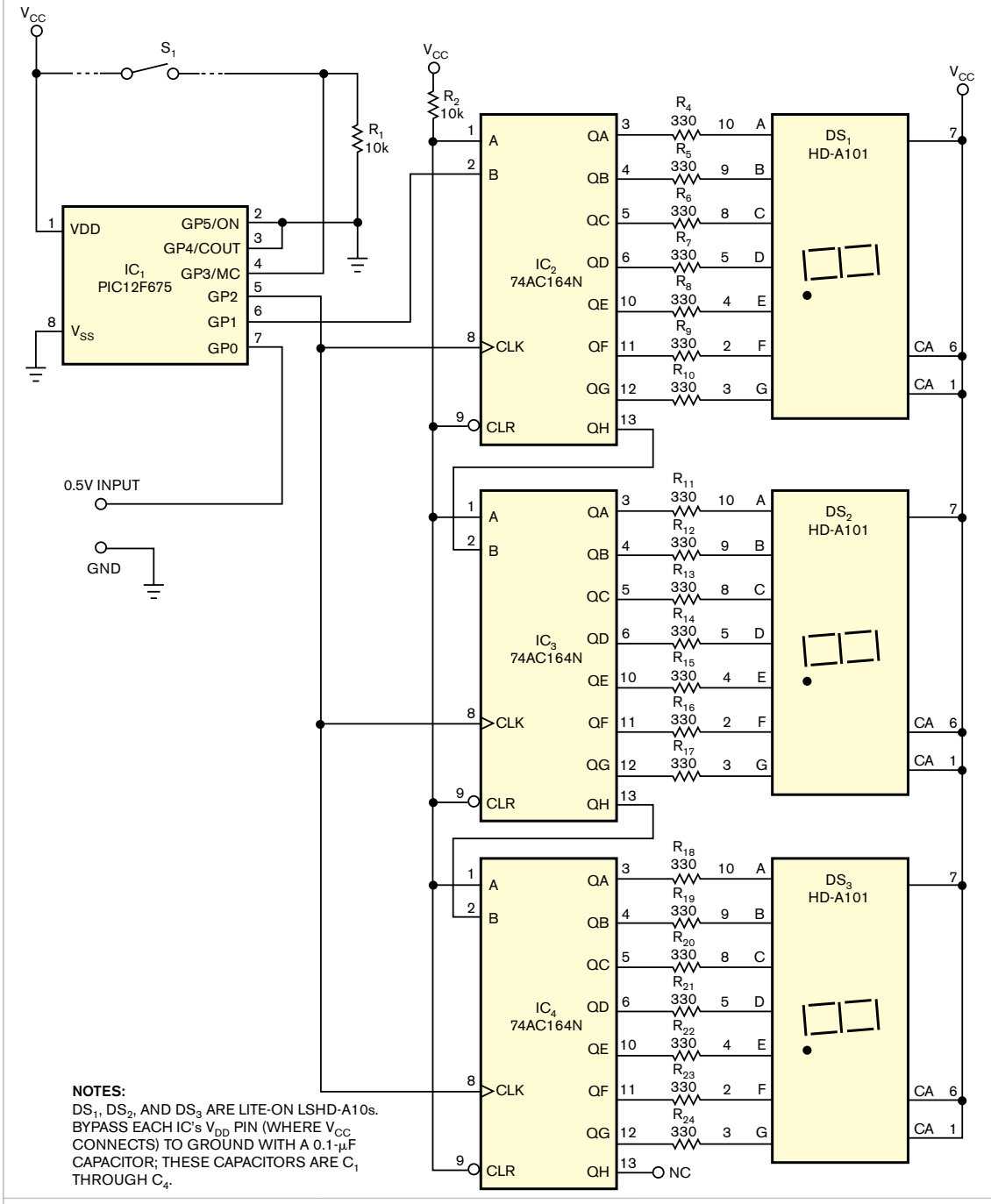


Figure 1 A low-cost microcontroller captures an analog voltage, converts it to a peak reading, and displays the results in decimal format on LED displays.

a three-digit, seven-segment display. Although applicable to other microcontrollers, the circuit in **Figure 1** uses a Microchip (www.microchip.com) PIC12F675 controller and three multiply sourced 74AC164 serial-input/parallel-output shift registers.

The circuit accepts incoming signals of 0 to 5V. The microcontroller, IC_1, performs the analog-to-digital conversion and subsequently converts the binary-voltage value to BCD (binary-coded-decimal) format. Next, the microcontroller converts the BCD values to hardware-specific seven-segment-display masks and shifts the masks to the 74AC164 registers, IC_2 through IC_4, which in turn drive the seven-segment displays.

Available for downloading from the online version of this Design Idea at www.edn.com/070510di2, **Listing 1** implements an additional function. Instead of displaying each input value as it's converted, the microcontroller operates as a peak detector. When the maximum value changes, the microcontroller updates the three-digit display. A pushbutton switch, S_1, resets the maximum value. You can modify the code to apply other functions to the input data and calculate and display the data in other formats. In addition, you can modify the interrupt-driven conversion process to accommodate different sampling rates. When you modify the sampling rate or the ISR (interrupt-service routine), ensure that the ISR completes execution within a single sample period. EDN

INSTEAD OF DISPLAYING EACH INPUT VALUE AS IT'S CONVERTED, THE MICROCONTROLLER OPERATES AS A PEAK DETECTOR.

REFERENCE

1 Raynus, Abel, "Squeeze extra outputs from a pin-limited microcontroller," *EDN*, Aug 4, 2005, pg 96, www.edn.com/article/CA629311.

Amplifier cancels common-mode voltage

W Stephen Woodward, Chapel Hill, NC

Since the dawn of time—or at least since the dawn of precision electronics—a major headache for analog designers has been CMV (common-mode-voltage)-induced errors, also known as the dreaded ground loop. Although almost mystical is the fear it strikes in the hearts of engineers, there's nothing particularly mysterious about CMV. CMV errors occur for a simple reason: The common voltage references—that is, ground—of circuitry in different places, such as sensors in one chassis and an ADC in another, are apt to differ. Therefore, when you

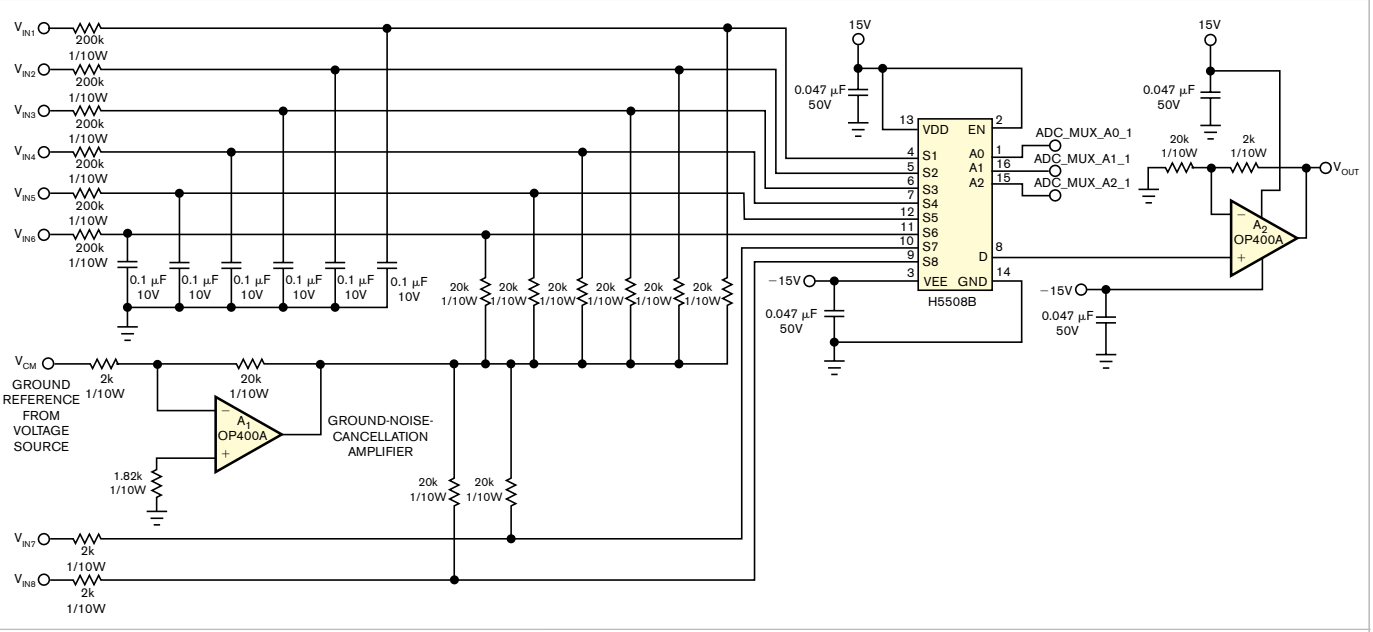


Figure 1 Amplifier A_1 amplifies and inverts the common-mode voltage by a factor of −10. Then, the circuit applies this signal to an array of passive summation networks. An analog multiplexer selects the desired input signal, and op amp A_2 supplies a compensating gain.

route signals between remotely located circuits, the CMV differential appears as additive noise and offset, corrupting the desired signals.

Many approaches exist for eliminating CMV errors. These methods include the brute-force approach of using massive amounts of copper in ground interconnections, fully differential instrumentation-amplifier signal conditioners, and galvanic isolators. Each has its place, depending on such factors as the severity of the CMV problem and the number of signal channels needing CMV remediation. One of the most popular and effective CMV remedies is differential amplification, in which you perform an analog subtraction to remove the CMV component from the signal. The downside of this method is that it requires a dedicated amplifier for every signal channel. The circuit in **Figure 1** is a variation on that same differential-amplifier idea, but it combines two shared CMV amplifiers with simple passive-resistor pairs among eight multiplexed channels to provide CMV cancellation for a large number of analog channels at minimum component count.

ONE OF THE MOST POPULAR AND EFFECTIVE CMV REMEDIES IS DIFFERENTIAL AMPLIFICATION, IN WHICH YOU PERFORM AN ANALOG SUBTRACTION TO REMOVE THE CMV COMPONENT FROM THE SIGNAL.

Here's how it works. Amplifier A_1 amplifies and inverts the CMV by a factor of −10. You then apply this CMV to an array of passive-summation networks—one for each input signal. The 10-to-1 ratio of the two legs of each network combines the incoming input-voltage and CMV signals with the –10V CMV ground-noise reference: $V=10/11\times(V_I+V_{CM})+1/11\times(10\times V_{CM})=10/11\times V_I+10/11\times(V_{CM}-V_{CM})=10/11\times V_I$. V_{CM} is attenuated by a factor depending mainly on the accuracy of 20- versus 2-kΩ resistor-ratio matching. For 1% matching, the CMRR (common-mode-rejection ratio) is approximately 100-to-1, or 40 dB; for 0.1% matching, CMRR is 1000-to-1, or 60 dB.

The analog multiplexer then selects the desired input voltage for input to the 11/10 scale-factor-correction amplifier, A_2. The optional 0.1-μF filter capacitors provide a modicum of low-pass noise filtering, and you should tailor them for the bandpass requirements of your application. The approximately 180 μsec, or approximately 88 Hz, is too slow for many applications and too fast for others. EDN

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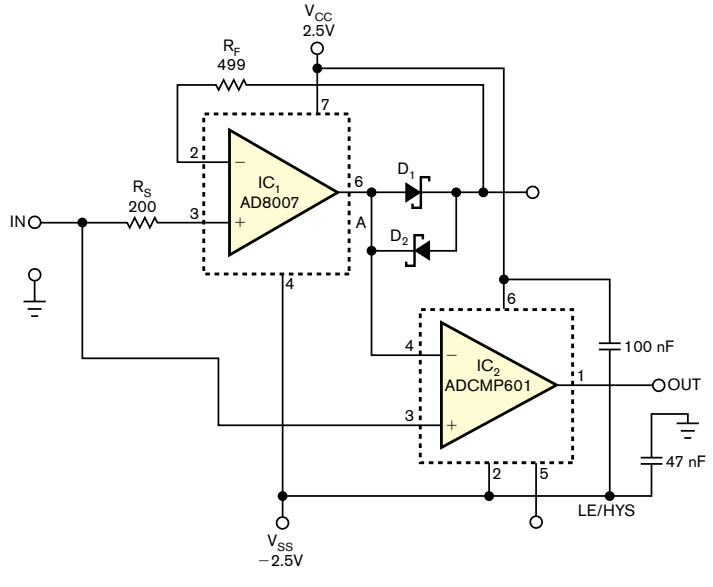
Comparator detects position of peaks and valleys in a waveform

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The recent advent of Analog Devices' (www.analog.com) ADCMP60x family of comparators has filled a gap between the less-than-1-nsec-response comparators consuming 100 to 200 mW and those exhibiting approximately 1-µsec response, requiring about one-thousandth that power. The ADCMP60x comparators exhibit a low value of the product of propagation-delay-by-supply-current drain; possess rail-to-rail input and output operation; and offer a variety of options for hysteresis, latch-mode operation, and shutdown mode. Some of them also have inherent level-translating capability. Moreover, the ratio of propagation delays for the positive and negative transitions at the output is close to the ideal value of 1 within 8% tolerance for the ADCMP600, ADCMP601, ADCMP602, and ADCMP603 and with in a 6.7% tolerance for the ADCMP608 and ADCMP609 members of the family (**Reference 1**).

This ratio is important in applications in which both positive- and negative-output-level transitions are equally significant. **Figure 1** shows one such circuit. Voltage-level transitions at the output of the detector indicate changing of the sign of the first derivative of the input signal; in other words, the circuit detects time positions of peaks and valleys in the input-voltage waveform. The detector circuit uses an ADCMP601 for IC_2, and IC_1 is an Analog Devices AD8007 current-feedback amplifier. IC_1 connects as a voltage follower with an antiparallel combination of Schottky-barrier switching diodes, D_1 and D_2, between the output and the inverting input of the amplifier. Comparator IC_2's inputs connect to the source of the input voltage and to the output of the current-feedback amplifier. This configuration enhances the voltage difference of $V_{IN}-V_A$ between inputs of the comparator. It performs this enhancement in a steplike manner at the instant, or region, at which the sign of slope of the input signal changes. This voltage difference is a measure of the double-forward voltage of diodes D_1 and D_2 at their forward current, which you derive from V_{IN}/R_F.

You use a current-feedback amplifier as IC_1 because a dynamic current flows into its inverting input even when you



NOTE: D_1 AND D_2 ARE HSMS-282Ls OR HSMS-282Cs.

Figure 1 Comparator IC_2 produces an output that switches state at the positive and the negative peaks of the input-voltage waveform.

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connect it as a voltage follower. The values of the R_S and R_F resistors are those that **Reference 2** recommends for a gain of 1. You needn't worry about instability due to the presence of antiparallel diodes in the feedback path of the current-feedback amplifier. These diodes increase the value of feedback resistance to more than 499Ω. Whenever the input voltage is only approximately 0V, the frequency-gain response of IC_1 for an R_F value greater than 499Ω remains flat.

An analysis of the response of the voltage follower in **Figure 1** to a harmonic input voltage uses ω/ω_T and $\omega=2\pi f$, where f is the input-voltage frequency and ω_T is the radial transition frequency of the amplifier. At the radial-transition frequency, the ratio of Z_M (the magnitude of the amplifier's transimpedance) to R_F drops to one. This simplification leads to an **equation** for the delay, t_D, in **Figure 2**:

$$\Delta\varphi = 2\sqrt{\frac{V_F}{V_m}\times\frac{R_F}{r_{m0}}},$$

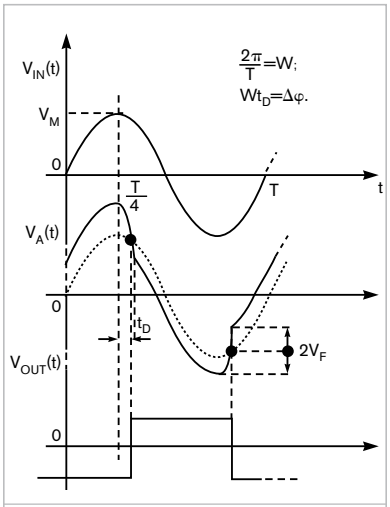

Figure 2 The output of comparator IC_2 switches a slight time delay, t_D, after the positive and the negative peaks of the input voltage.

where V_F is the forward voltage of diode D_1, V_m is the amplitude of input voltage, R_{m0} is the dc transresistance of the current-feedback amplifier, and $\Delta\phi$ is the electrical-error angle in radians. The period of input harmonic voltage, T in **Figure 2**, represents 2π radians. The final error of the detector is $\Delta\phi$, which decreases by a factor of $\sqrt{2}$. This reduction occurs because the necessary operating overdrive over the midpoint of the steplike transition in the $V_A(t)$ voltage that the comparator requires is more than an order of magnitude less than the value of V_F. EDN

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Precision integrator sparks current-ratio-to-frequency converter

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Università degli Studi di Roma Tre, Rome, Italy

The Design Idea in **Figure 1** uses the S_1 switch of the Texas Instruments (www.ti.com) IVC102 precision integrator to select between a single input current or the superposition of two input currents. This function allows you to obtain an output signal whose characteristics directly relate to the ratio between the two input currents. The circuit achieves high accuracy independent of most of the system parameters. In addition, you can enhance accuracy if you let a digital counter control the IVC102-based circuit (**Figure 2**). In this case, the system's output is a number in the BCD (binary-coded-decimal) format proportional to the input-current ratio, realizing a true digital conversion.

The circuit divides into two phases. The first phase begins when the output voltage of the IVC102 becomes slightly greater than the threshold voltage of the LM311 comparator. The comparator generates a falling-edge signal, and the 555 monostable starts a pulse, which closes S_1. In this case, the total input current, I_2-I_1, generates a negative-going ramp if I_2 is greater than I_1. In the delta-time period, ΔT_A, the integrator's output voltage reaches the final voltage value. Hence, $|V_{FIN}-V_{TH}|=(I_2-I_1)\Delta T_A/C_{INT}$, where C_{INT} is the value of the IVC102's integrating capacitor. When the 555 monostable's output pulse ends, the second phase starts: S_1 opens, and input current I_1 discharges C_{INT}. The ΔT_B for the output voltage to assume the threshold voltage's value is then $C_{INT}|V_{FIN}-V_{TH}|/I_1$, and the comparator generates a new trigger command to the monostable so that a new cycle can start. Manipulating the previous **equations** yields: $I_1/I_2=\Delta T_A f$, where $f=(\Delta T_A+\Delta T_B)^{-1}$. This **equation** states that the generated output signal, a train of pulses, has a frequency, f, proportional to the I_1/I_2 current ratio. The accuracy of the monostable directly affects the accuracy of the system. Conversely, the integrating capacitor's and threshold voltage's values do not influence the accuracy if they maintain constant values at least in the 1/f time scale.

You can increase the accuracy of the circuit in **Figure 1** by modifying the section that generates the constant, ΔT_A-wide pulse. The circuit in **Figure 2** generates a ΔT_A-wide pulse using three

(continued on pg 108)

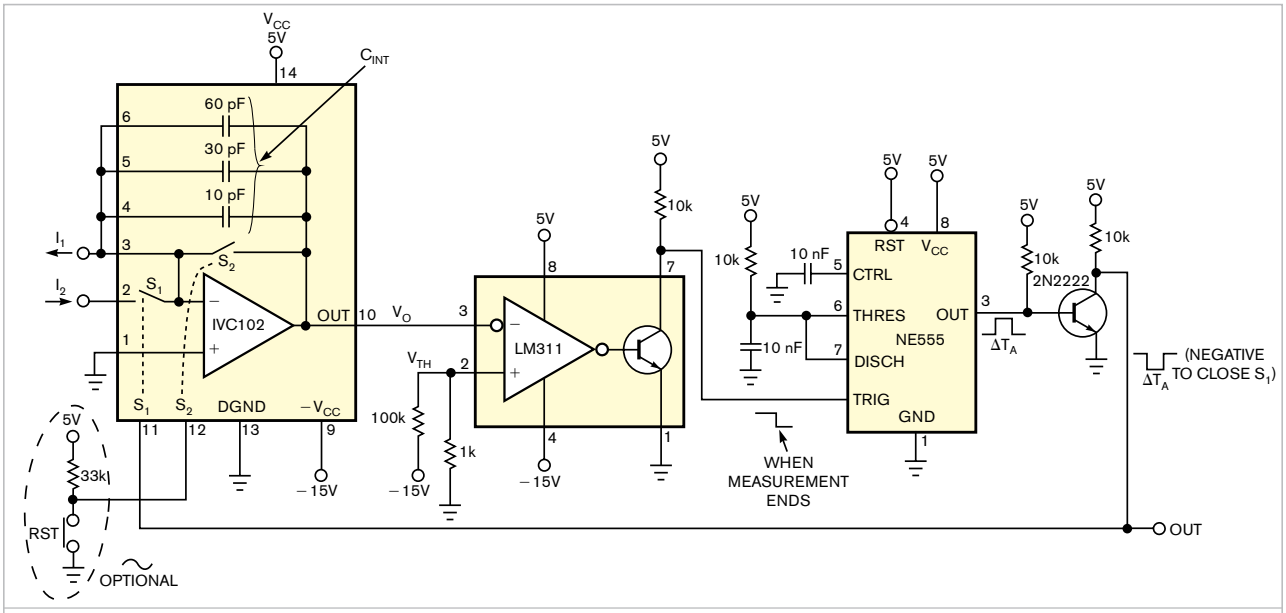

Figure 1 This circuit allows you to obtain an output-signal frequency that directly relates to the ratio between the two input currents.

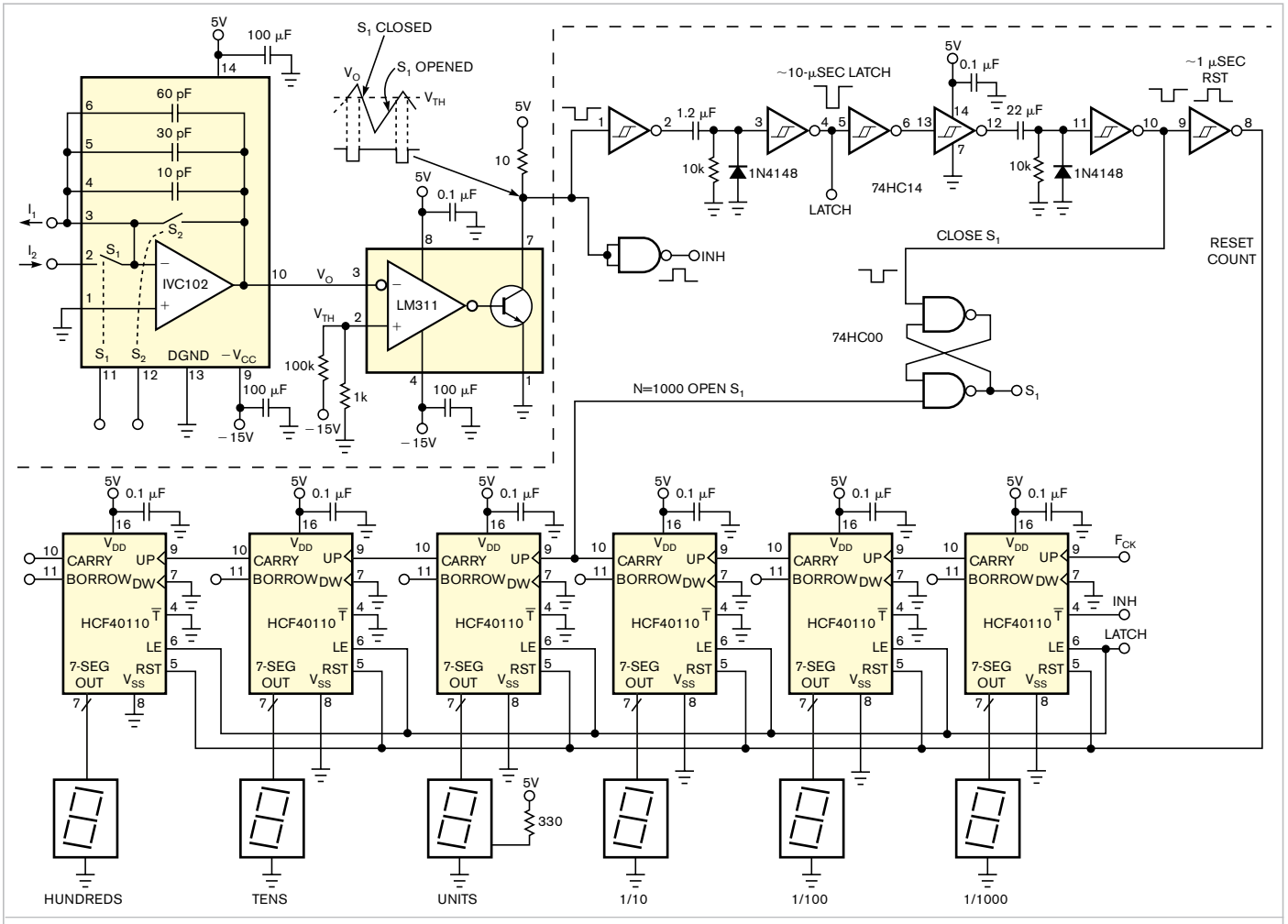

Figure 2 To the circuit in Figure 1, this design adds a BCD counter to obtain direct readouts on seven-segment LED displays.

HCF40110 BCD counters. When the third counter generates a carry, 1000/f_{CK} seconds have elapsed. In **Figure 2**, a set/reset flip-flop controls S_1's state, and the 74HC14 hex inverter with a Schmitt-trigger input generates the pulses that reinitialize the system. A brief description of the measurement cycle follows. When the IVC102's output voltage becomes greater than the threshold voltage, the INH (inhibit) signal connected to the toggle input of the first HCF40110 inhibits counting. At the same time, the negative-going edge of the comparator output generates a negative-going pulse of approximately 10 µsec, which latches the counters' values at the output to display the actual result. After this step, a negative-going pulse sets the SR flip-flop to close S_1. A corresponding positive-going pulse resets the counters. The latch-enable lines of the 40110s are tied high, so the counters' reset doesn't affect the displayed value. When the reset pulse ends and the comparator's output goes high, the HCF40110s can count up. When the third counter generates a carry (negative-going pulse), the 1000th clock period has elapsed, and the SR flip-flop resets to open S_1. The cycle ends at the next falling edge of the comparator's output. The time period in which I_2-I_1 charges C_{INT} is $N_A/f_{CK}(N_A=1000)$, and the I_1 requires for discharging is N_B/f_{CK}. Manipulating the integrator-related relationships yields $I_2/I_1=N/N_A$, where $N=N_A+N_B$.EDN

Accurate USB 2.0 temperature sensor needs only a handful of parts

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This Design Idea presents a simple, accurate, and reliable design to measure temperature using the USB. **Figure 1** shows the complete circuit of the temperature-sensor device. The heart of the sensor device is an FT232RQ USB-to-serial converter from FTDI (Future Technology Devices International, www.ftdichip.com). In addition to using the FT232 in its default UART mode, the FT232 works in a so-called bit-bang mode (**references 1**, **2**, and **3**). This mode changes its I/O lines into a bidirectional data bus, which the user can fully control. The connection with the USB takes place in a standard manner, and the back end of the chip interconnects to an AD7814 digital temperature sensor from Analog Devices (www.analog.com, **Reference 4**).

The temperature sensor uses a four-wire SPI but only three pins: SCK (serial clock), SS# (slave select), and SDO (serial-data out). To avoid any malfunction of the sensor, the SDI (serial-data-in) line must be grounded. The FT232 acts as an SPI master and emulates the protocol for the AD7814 by setting or clearing the appropriate port pins for SS# and SCK. The data from the sensor gets read back together with all the other bus lines. This process occurs simultaneously with the write process.

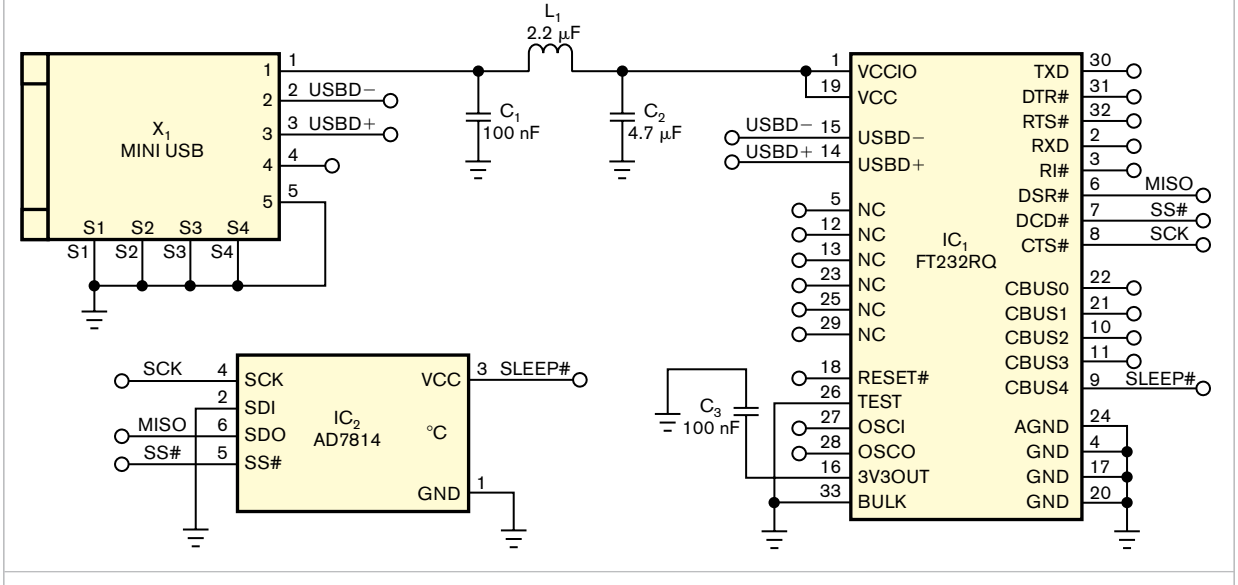

Figure 1 This circuit for a USB temperature sensor works in default UART and bit-bang modes.

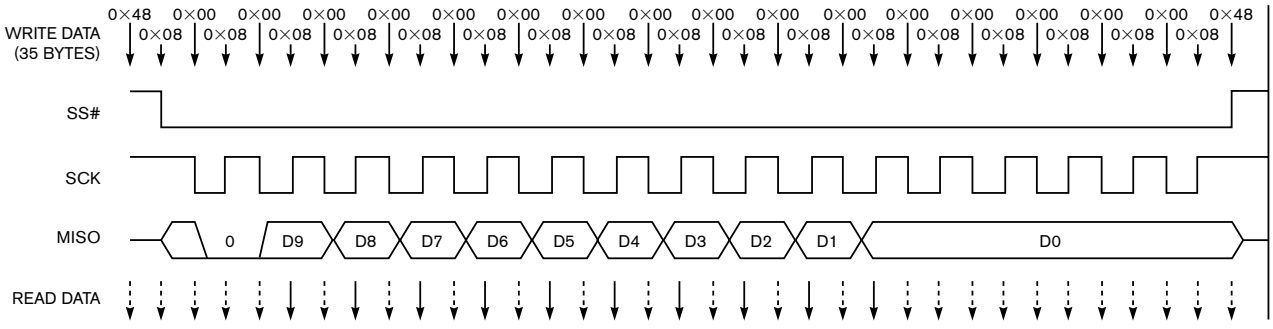

Figure 2 The timing diagram for the AD7814 shows considerable data overhead to download 10 bits of temperature data.

Figure 3 Two sample circuits (left and center) are smaller than a USB Type A plug (right).

To comply with the USB specification, you power down the temperature sensor using the sleep signal while the USB logic is in suspend mode. The sensor device receives its power through the USB and draws only about 20 mA. On the software side, you need only to open the device and switch the chip into the bit-bang mode. After that action, you can send the fixed pattern to emulate an SPI master from the host PC to the FT232 (**Figure 2**). The software returns a data array of the port samples of both the PC and the FT232, whose ports are inputs and outputs.

Because the FT232 chips come with a unique serial number, you can identify the correct device within a multichip environment. So, you can put more than one FT232-based sensor onto a computer. The core of this Design Idea is not limited to measuring temperature. You can use other sensors with digital interfaces, as well.

To get the current temperature, you must write 35 fixed bytes into the port register. The sensor expects 16 clock pulses on the SCK line while the SS# is low. The clock frequency is 1 MHz. The device samples sensor-read data during the write operation. After the protocol on the back end finishes, you can retrieve the data from the host PC for further processing. To get just 10 bits out of the sensor involves considerable data overhead (**Figure 2**). The dashed-line arrows mark the bytes, which need no further evaluation.

This Design Idea realized two sample circuits on a two-layer PCB (printed-circuit board) measuring only 18×12 mm (0.7×0.47 in.) and 7.6×30.5 mm (0.3×1.2 in.). **Figure 3** shows them in comparison to the size of a USB Type A plug. EDN

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Integrator enables simple ohmmeter with gigohm range

Stefano Salvatori and Gennaro Conte,
Università degli Studi di Roma Tre, Rome, Italy

The Texas Instruments (www.ti.com) IVC102 precision integrator has high-quality internal capacitors. The circuit in **Figure 1** allows you to measure very-high-resistance values of R_X. A precision difference amplifier, a TI INA105, applies a reference voltage to R_X. During integration, a negative voltage ramp, V_O, is generated at the output of the IVC102. The two LM311s compare the amplitude of V_O with two fixed thresholds and generate the two digital signals: start and stop. The delta time between two such events relates to the system parameters by the expression: $\Delta T = C_{INT}[(V_A - V_B)/V_{REF}]R_X$, where ΔT is the delta time and C_{INT} is the internal integrating ca-

pacitance of the IVC102, which external connections on pins 4, 5, and 6 select. (Note: when S_1 is open, C_{INT}=10 pF, whereas, when S_1 is closed, C_{INT}=100 pF.) The V_A threshold allows the circuit to see the output ramp without any offset on the V_O signal. Because of the INA105 difference amplifier, $V_{REF}=V_A-V_B$, so the previous **equation** reduces to: $\Delta T=C_{INT}R_X$. Also note that the precision of resistors R_1, R_2, and R_3 is not critical. The difference amplifier guarantees the precision of the ohmmeter.

External digital-control circuitry can measure delta time by counting the clock periods between the start and the stop events. At the end, the control circuit can generate a reset signal for the IVC102 to perform a new measurement. EDN

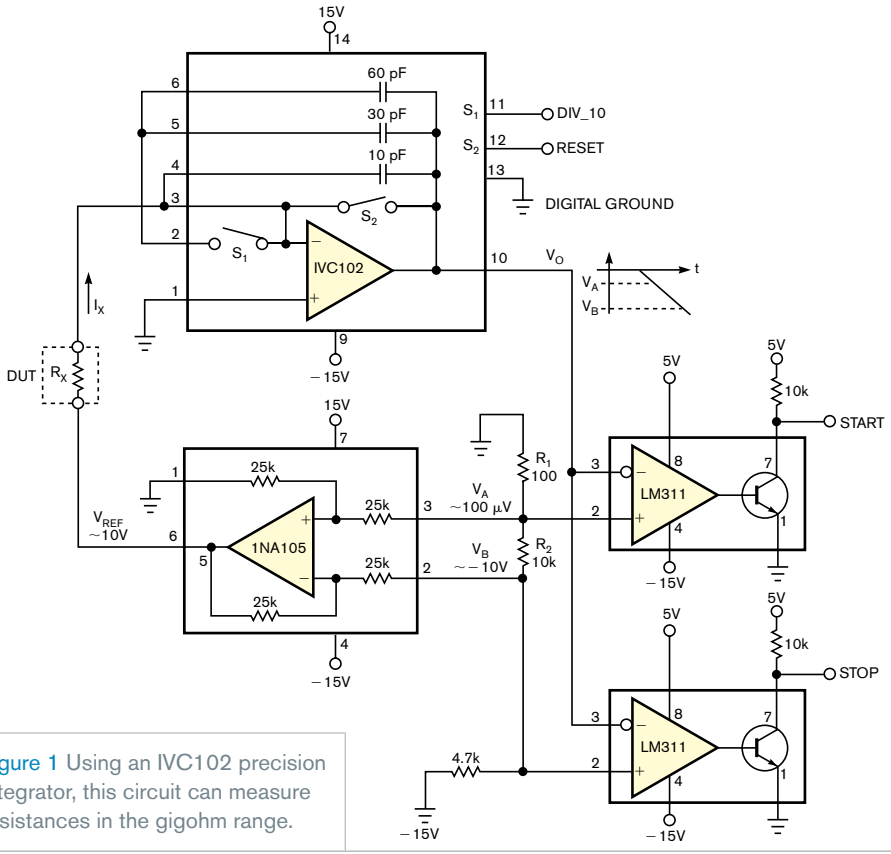

Figure 1 Using an IVC102 precision integrator, this circuit can measure resistances in the gigohm range.

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AND FRAN GRANVILLE

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Simple fixture determines leakage of capacitors and semiconductor switches

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The circuit in **Figure 1a** comprises a voltage follower, IC_1, and the reference-voltage source of IC_2. IC_1 is an Analog Devices (www.analog.com) AD8661 op amp, which has a guaranteed input-bias current of no more than 1 pA and a typical input-bias current of 0.3 pA (**Reference 1**), and IC_2 is an Analog Devices ADR391 precision voltage reference (**Reference 2**). The manufacturer trims the input offset voltage of this op amp not to exceed 100 µV, and the typical value is 30 µV. These properties suit this amplifier for observing self-discharging of almost any type of capacitor. The leakage currents of solid-tantalum capacitors and those having high-quality plastic dielectrics are well above the input-bias current of voltage follower IC_1. The CUT (capacitor under test) initially charges to the reference-voltage level of 2.5V by connecting Point A to the output of IC_2. Subsequently, at some convenient time, Point A disconnects from the source of the reference voltage. A DVM (digital voltmeter) measures the output voltage of the follower at some reasonable time. The measured voltage drop, V_O, with regard to initial value, should be 0.1 to 0.5V. The leakage current, I_O, is $C \times \Delta V_O / t_{MEAS}$, where C is the value of the CUT and t_{MEAS} is the time between releasing the connection of the CUT to the 2.5V source and the instant of readout at the voltage drop of V_O.

The fixture also allows determining leakage currents of reverse-polarized diodes and of various switching devices in the off state, such as JFETs, MOSFETs, BJTs (bipolar-junction transistors), SCRs (silicon-controlled rectifiers), and IGBTs (insulated-gate bipolar transistors). In this case, the parallel combination of the DUT (device under test) and the added capacitor, C_{ADD}, replaces the CUT (**Figure 1b**). The measurement and the formula for evaluating the value of leakage current are the same as those for leakage current in the **equation** $I_O = C \times \Delta V_O / t_{MEAS}$, but C_{ADD} substitutes for the CUT. A polystyrene-dielectric, 10-nF C_{ADD} works well for low-power devices. For high-power devices, however,

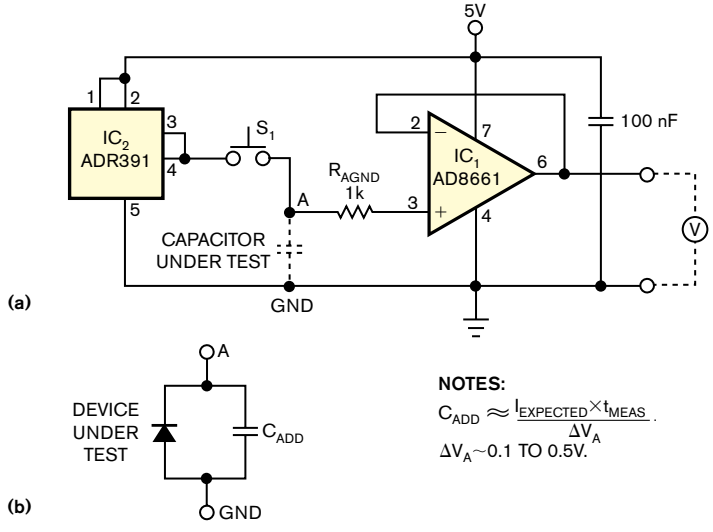

Figure 1 This simple fixture first impresses a reference voltage across a capacitor under test and then measures the voltage drop versus time at the output of the voltage follower (a). The circuit measures the leakage current of a reverse-biased active device (b).

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the value of C_{ADD} should be at least 10 times the value of the parasitic capacitance of the DUT at 0V.

Further, the fixture in **Figure 1b** can also determine the values of resistors of tens of megohms to about 2 TΩ. The current in the **equation** $I_O = C \times \Delta V_O / t_{MEAS}$, in this case, is the current flowing through resistor R_{AGND} at approximately the reference voltage. The resistance is roughly:

$$R_{AGND} \approx V_{REF} \times \frac{t_{MEAS}}{C_{ADD} \times \Delta V_O},$$

or, more precisely:

$$R_{AGND} = \left(\frac{V_{REF}}{\Delta V_O} - \frac{1}{2} \right) \frac{t_{MEAS}}{C_{ADD}}.$$

In all measurements, the voltage drop of V_O should not exceed about one-fifth of the reference-voltage value to allow approximating the inherently exponential droop of V_O by a linear decrease. The pushbutton switch in **Figure 1a**, S_1, must exhibit a leakage of less than 1 pA. Stranded, isolated leads terminated with a gold-plated phosphorus-bronze pin can serve as a low-leakage switch. You can find gold-plated metal pieces in any type of high-quality connectors. Also, you can clip the DUT or CUT between two gold-plated clips made of similar connector parts. To minimize the circuit's leakage, it uses no PCB (printed-circuit board). EDN

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Recycle precision potentiometers as useful voltage sources

Mark Thoren, Linear Technology, Milpitas, CA

An analog- or a mixed-signal lab cannot have too many voltage sources. A simple, reasonably high-precision voltage source can set bias points in an op-amp circuit, tweak the feedback node of a power supply through a large resistor, or run a quick linearity test on an ADC. Engineers often use a dc-power supply because it is the only thing they can find, and many labs lack a true voltage-calibration source. This Design Idea describes a circuit that recycles old precision potentiometers that have direct-reading scales into useful laboratory "volt boxes."

Several types of potentiometers work in the circuit in **Figure 1**. Standard 10-turn potentiometers typically have 0.1% linearity and work well for general-purpose tweaking. However, a five-decade Kelvin-Varley divider with a total resistance of 100 kΩ or less achieves 10-ppm accuracy. Having some indication from a voltage source that its output is correct proves useful. A digital panel meter is one way of achieving this goal. However, even a 0.1% potentiometer is more accurate than most of these meters. So, to indicate that the output is correct, you need to know only whether the power is on, whether the supply voltage is high enough, and whether the output amplifier is working properly and not sourcing or sinking too much current or oscillating.

A single red-green-blue LED provides all three indications. The green LED flashes at a low duty cycle when the power is on and stays lit continuously when the battery voltage is too low. The red LED illuminates when the output is out of regulation because IC_{4B} is a low-duty-cycle relaxation oscillator that pulses a green LED for 5 msec at approximately 0.5 Hz. The blue LED lights when sinking too much current. If the output is oscillating, the LED glows purple.

IC_{4A} compares the positive battery voltage to the precision 10V reference output and continuously turns on the green LED when the positive battery voltage drops below 11.5V. This level is the dropout voltage of the reference, so you know it's time to change the batteries. The load on the positive supply is greater than that on the negative supply, so these cells wear out first. And, because only two cells constitute the negative supply, battery wastage is minimal. Alternatively, you can move the negative cells to the positive side to squeeze the last bit of juice from them.

The reference is IC_1, an LT1236-10 with an added trim circuit. The LT1236 is quiet and stable over time and temperature. Its output drives the top of the precision potentiometer or Kelvin-Varley divider. The output of the circuit is trimmed to 10V when the potentiometer or divider is at its maximum value. The two halves of an LT1881 amplifier, IC_{2A} and IC_{2B}, buffer the output of the potentiometer or divider. The combined bias current for both buffers is 400 pA maximum, which causes a change of approximately 10 μV in the output voltage of a 100-kΩ potentiometer when it is at midscale. Make sure to properly guard the noninverting inputs to prevent leakage. The 50-μV maximum offset and 130-dB CMRR (common-mode-rejection ratio) keep overall accuracy well within 10 ppm of a 10V total span.

One-half of the LT1881 is the voltage output of the volt box. The other half is necessary to drive the two inputs to IC_5, an LT1017 dual comparator that has an input-bias current of 15 nA per comparator. Q_1 to Q_6 form a 100-µA current sink and source referred to the negative supply and positive supply, respectively. You adjust potentiometers R_1 and R_2 to set up a window around the output voltage that is compared with the output of IC_{2A}, which is a replica of the correct output voltage. If IC_{2B} is sourcing or sinking too much current, one of the comparators will trip, turning on the respective LED. If the output is oscillating, both LEDs will light. The window is adjustable from 0 to approximately ±9.3 mV; ±1 mV is a good place to start.

Should you need more output current than the 5 mA that the LT1881 guarantees, you can switch in an LT1010 buffer to provide a "turbo-boost" feature, increasing the output-current capability to ±150 mA and greatly increasing the ability to drive capacitive loads. You should normally disable this buffer because it draws 10 mA more from the supply. Switch S_3 allows reverse polarity, and, if you use a center-off switch, you can disconnect the output. S_1 is the power switch and can also select power from an external supply or battery power when isolation is critical. EDN

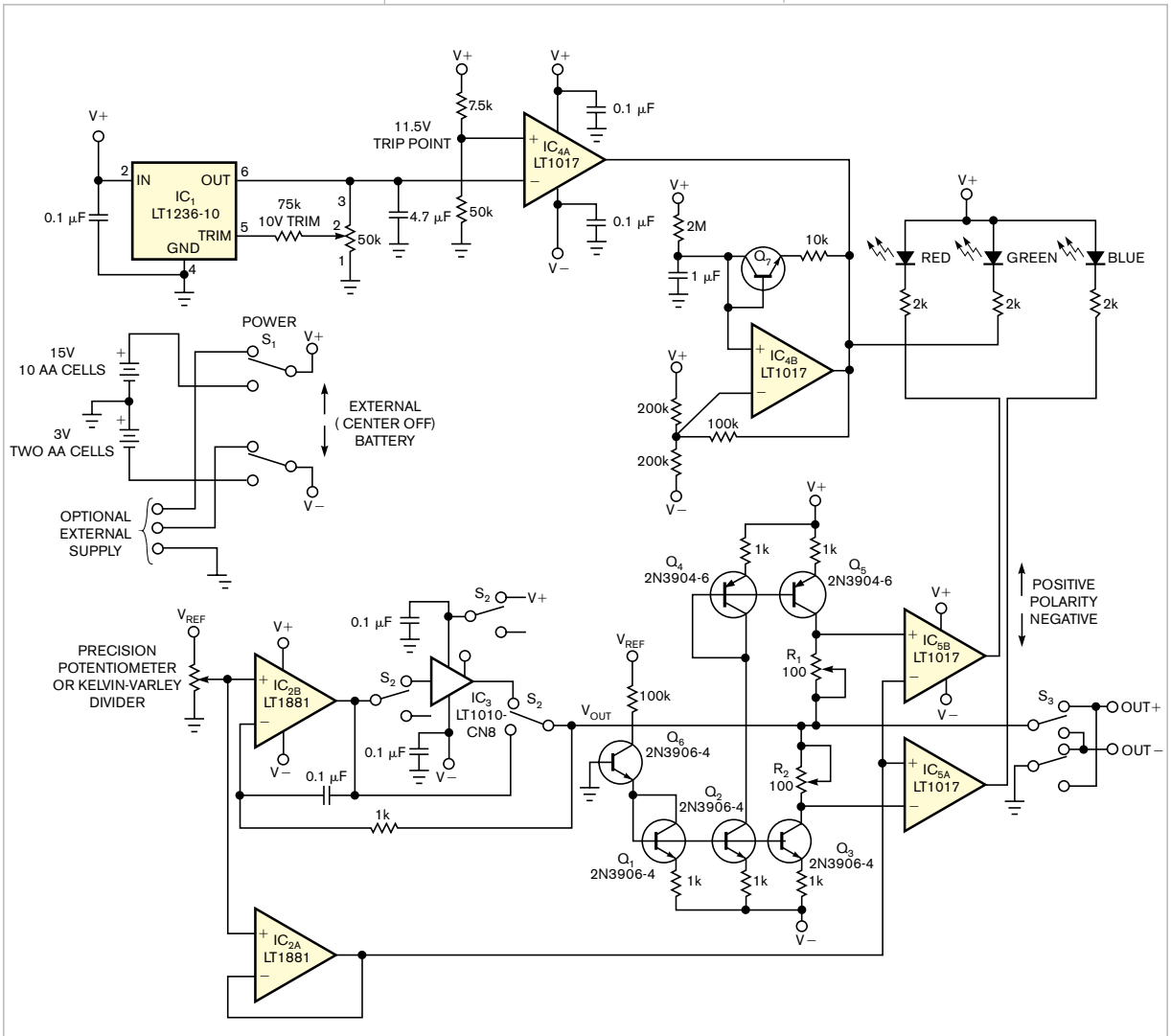

Figure 1 You can recycle old 10-turn potentiometers as precision "volt boxes." The LEDs provide a visual indication that the output voltage is in regulation.

Circuit breaker provides overcurrent and precise overvoltage protection

Anthony H Smith, Scitech, Bedfordshire, England

Requiring only a handful of inexpensive components, the circuit breaker in **Figure 1** responds to both overcurrent- and overvoltage-fault conditions. At the heart of the circuit, D_2, an adjustable, precision, shunt-voltage regulator, provides a voltage reference, comparator, and open-collector output, all integrated into a three-pin package.

Figure 2 shows a simplified view of the ZR431, D_1. The voltage appearing at the reference input is compared with the internal voltage reference, V_{REF}, nominally 2.5V. In the off state, when the reference voltage is 0V, the output transistor is off, and the cathode current is less than 0.1 µA. As the reference voltage approaches V_{REF}, the cathode current increases slightly; when the reference voltage exceeds the 2.5V threshold, the device fully switches on, and the cathode voltage falls to approximately 2V. In this condition, the impedance between the cathode and the supply voltage determines the cathode current; the cathode current can range from 50 µA to 100 mA.

Under normal operating conditions, D_2's output transistor is off, and the gate of P-channel MOSFET Q_4 goes through R_9, such that the MOSFET is fully enhanced, allowing the load current, I_{LOAD}, to flow from the supply voltage, $-V_S$, through R_6 into the load. Q_2 and current-sense resistor R_6 monitor the magnitude of I_{LOAD}, where Q_2's base-emitter voltage, V_{BE}, is $I_{LOAD} \times R_6$. For normal values of I_{LOAD}, V_{BE} is less than the 0.6V necessary to bias Q_2 on, such that the transistor has no effect on the voltage at the junction of R_3 and R_4. Because the input current at D_2's reference input is less than 1 µA, negligible voltage drops across R_5, and the reference voltage is effectively equal to the voltage on R_4.

In the event of an overload when I_{LOAD} exceeds its maximum permissible value, the increase in voltage across R_6 results in sufficient base-emitter voltage to turn on Q_2. The voltage on R_4 and, hence, the reference voltage now pull up toward V_S, causing D_2's cathode voltage to fall to approximately 2V. D_2's output transistor now sinks current through R_7 and R_8, thus biasing Q_3 on. Q_4's gate voltage now effectively clamps to the supply voltage through Q_3, and the MOSFET turns off. At the same instant, Q_3 sources current into R_4 through D_1, thereby pulling the voltage on R_4 to a diode drop below the supply voltage. Consequently, no load current flows through R_6 because Q_2, whose base-emitter voltage is now 0V, has turned off. As a result, no load current flows through R_6, D_2's output transistor latches on, and the circuit remains in its tripped state in which the load current is 0A. When choosing a value for R_6, ensure that Q_2's base-emitter voltage is less than approximately 0.5V at the maximum permissible value of the load current.

As well as responding to overcurrent conditions, the circuit breaker also reacts to an abnormally large value of the supply voltage. When the load current lies within its normal range and Q_2 is off, the magnitude of the supply voltage and the values of R_3 and R_4, which form a potential divider across the supply rails, determine the voltage at the reference input. In the event of an overvoltage at the supply voltage, the voltage on R_4 exceeds the 2.5V reference level, and D_2's output transistor turns on. Once again, Q_3 turns

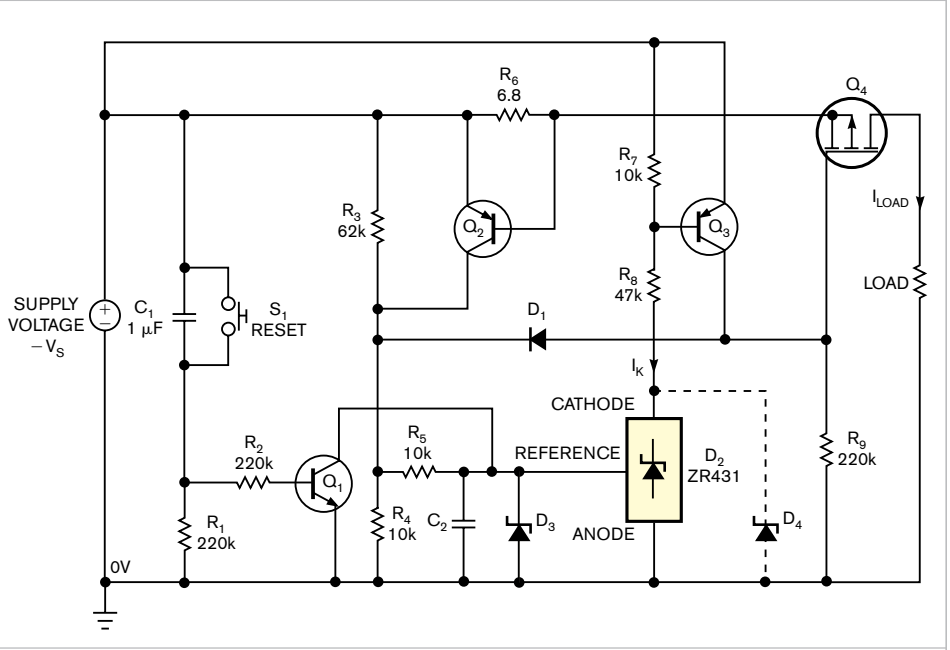

Figure 1 This circuit breaker provides both overvoltage and overcurrent protection. Other than the current flowing in R_3, R_4, and D_2's cathode, the circuit draws no current from the supply in its normal untripped state.

on, MOSFET Q_4 switches off, and the load becomes effectively isolated from the dangerous transient.

The circuit now remains in its tripped state until reset. Under these conditions, Q_3 clamps Q_4's gate-source voltage to roughly 0V, thereby protecting the MOSFET itself from excessive gate-source voltages. Ignoring the negligibly small voltage across R_5, you can see that the reference voltage is $V_S \times R_4/(R_3+R_4)$ in volts. Because D_2's output turns on when the reference voltage exceeds 2.5V, you can rearrange the equation as $R_3=[(V_{ST}/2.5)-1]\times R_4$ in ohms, where V_{ST} is the required supply-voltage trip level. For example, if R_4 has a value of 10 kΩ, a trip voltage of 18V would require R_3 to have a value of 62 kΩ. When choosing values for R_3 and R_4 to set the desired trip voltage, ensure that they are large enough that the potential divider will not excessively load the supply. Similarly, avoid values that could result in errors due to the reference-input current.

When you first apply power to the circuit, you'll find that capacitive, bulb-filament, motor, and similar loads having large inrush current can trip the circuit breaker, even though their normal, steady-state operating current is below the trip level that R_6 sets. One way to eliminate this problem is to add capacitor C_2, which slows the rate of change of the voltage at the reference input. However, although simple, this approach has a serious disadvantage in that it slows the circuit's response time to a genuine overcurrent-fault condition.

Components C_1, R_1, R_2, and Q_1 provide an alternative solution. On power-up, C_1 initially discharges, causing Q_1 to turn on, thereby clamping the reference input to 0V and preventing the inrush current from tripping the circuit. C_1 then charges through R_1 and R_2 until Q_1 eventually turns off, releasing the clamp at the reference input and allowing the circuit to respond rapidly to overcurrent transients. With the values of C_1, R_1, and R_2, the circuit allows approximately 400 msec for the inrush current to subside. Selecting other values allows the circuit to accommodate any duration of inrush current you apply to a load. Once you trip the circuit breaker, you can reset it either by cycling the power or by pressing S_1, the reset switch, which connects across C_1. If your application requires no inrush protection, simply omit C_1, R_1, R_2, and Q_1 and connect S_1 between the reference input and 0V.

When choosing components, make sure that all parts are properly rated for the voltage and current levels they will encounter. The bipolar transistors have no special requirements, although these transistors, especially Q_2 and Q_3, should have high current gain, Q_4 should have low on-resistance, and Q_4's maximum drain-to-source and gate-to-source voltages must be commensurate with the maximum value of supply voltage. You can use almost any small-signal diode for D_1. As a precaution, it may be necessary to fit zener diodes D_3 and D_4 to protect D_2 if extremely large transient voltages are likely.

Although this circuit uses the 431 device, which is widely available from different manufacturers, for D_2, not all of these parts behave in exactly the same way. For example, tests on a Texas Instruments (www.ti.com) TL431CLP and a Zetex (www.zetex.com) ZR431CL reveal that the cathode current is 0A for both devices when the reference voltage is 0V. However, gradually increasing the reference voltage from 2.2 to 2.45V produces a change in cathode current ranging from 220 to 380 µA for the TL431CLP and 23 to 28 µA for the ZR431CL—roughly a factor of 10 difference between the two devices. You must take this difference in the magnitude of the cathode current into account when selecting values for R_7 and R_8.

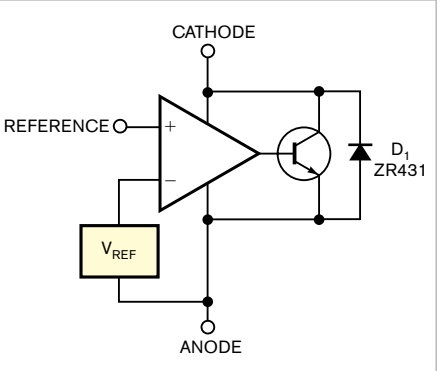

Figure 2 In this simplified view of the ZR431, the voltage at its reference input is compared with the internal voltage reference, which is nominally 2.5V.

The type of device you use for D_2 and the values you select for R_7 and R_8 can also have an effect on response time. A test circuit with a TL431CLP, in which R_7 is 1 kΩ and R_8 is 4.7 kΩ, responds within 550 nsec to an overcurrent transient. Replacing the TL431CLP with a ZR431CL results in a response time of approximately 1 µsec. Increasing R_7 and R_8 by an order of magnitude to 10 and 47 kΩ, respectively, produces a response time of 2.8 µsec. Note that the relatively large cathode current of the TL431CLP requires correspondingly small values of R_7 and R_8.

To set the overvoltage-trip level at 18V, R_3 and R_4 must have values of 62 and 10 kΩ, respectively. The test circuit then produces the following results: Using a TL431CLP for D_2, the circuit trips at 17.94V, and, using a ZR431CL for D_2, the trip level is 18.01V. Depending on Q_2's base-emitter voltage, the overcurrent-detection mechanism is less precise than the overvoltage function. However, the overcurrent-detection accuracy greatly improves by replacing R_6 and Q_2 with a high-side current-sense amplifier that generates a ground-referred current proportional to load current. These devices are available from Linear Technology (www.linear.com), Maxim (www.maxim-ic.com), Texas Instruments, Zetex, and others.

The circuit breaker should prove useful in applications such as automotive systems that require overcurrent detection to protect against faulty loads and that also need overvoltage protection to shield sensitive circuitry from high-energy-load-dump transients. Other than the small current flowing in R_3 and R_4 and the current in D_2's cathode, the circuit draws no current from the supply in its normal, untripped state. EDN

Paralleling decreases autozero-amplifier noise by a factor of two

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Autozero amplifiers have almost zero drift and input-offset values of 1 to 20 µV. You can compensate for the initial voltage offset of an autozero amp in sensitive circuits, such as dc amplifiers and integrators, requiring the processing of voltages of 10 µV to 1 mV. Total compensation down to an offset of 0V, however, is an illusion because residual low-frequency output noise is still present in any autozero amp.

The Analog Devices (www.analog.com) AD8628 autozero amp has a low-frequency-noise value of 0.5 µV p-p at 0.1 to 10 Hz. If your application requires zero drift and low output noise, you can use the circuit in **Figure 1**. A quad autozero amp develops a gain of almost 1000. The resistor network comprising the R_3 resistors averages the output signals of these amplifiers to create the final output voltage.

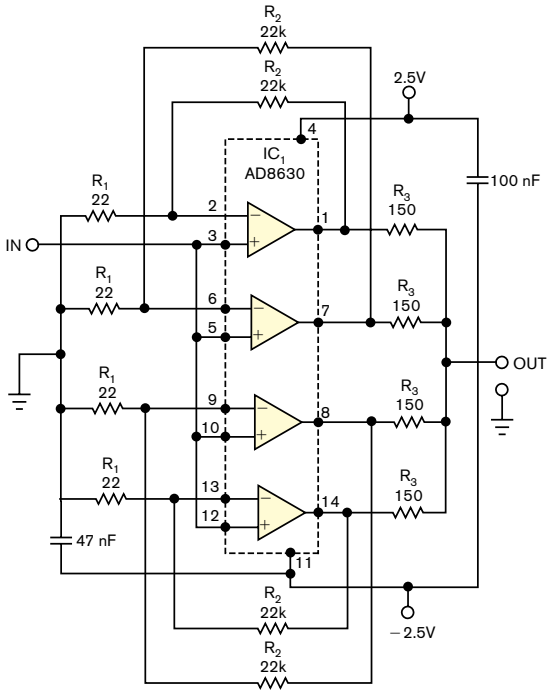

Figure 1 Use this circuit when your application requires zero drift and low output noise.

The quad autozero amps are the four sections of IC_1, an Analog Devices AD8630 (**Reference 1**). Quad integrated resistors having one common lead can substitute for the four R_3 resistors. The R_1 and R_2 resistors should be high-quality, precision, film devices with 0.5% or less tolerance. The tolerance of the R_3 resistors should not exceed 1%. The basis for decreasing the circuit's noise at the output in comparison with a single amplifier of IC_1 is the principle of averaging the signals containing the same deterministic component of random noise. If you assume that the amplifiers of IC_1 represent independent or uncorrelated noise sources that obey the gaussian distribution, then the standard deviation of the average of noise outputs of these sections is:

$$\sigma_{AVE2} = \frac{\sqrt{\sigma_X^2 + \sigma_Y^2}}{2},$$

where σ_X and σ_Y are the standard deviations of noise signals at outputs of the single respective amplifiers. If $\sigma_X = \sigma_Y$—an assumption that you can make without hesitation because the op amps reside in one chip—then:

$$\sigma_{AVE2} = \frac{\sigma_X}{\sqrt{2}}.$$

If you average four amplifiers, you obtain:

$$\sigma_{AVE4} = \frac{\sigma_X}{2}.$$

If the value of output resistance of the circuit, which is about $R_3/4 \approx 38\Omega$, is too high for your application, place a voltage follower between the output terminal and the next stage. EDN

REFERENCE

1 "AD8630 Quad, Zero Drift, Single-Supply, Rail-to-Rail Operational Amplifier," Analog Devices Inc, www.analog.com/en/prod/0,2877,AD8630,00.html.

Two transistors form high-precision, ac-mains ZCD

Djessas Zoheir, Constantine, Algeria

Many applications that use 110V/230V-ac mains require a ZCD (zero-crossing-detection) circuit for the ac-line voltage, for example, to synchronize the switching of loads. One method of ZCD uses a high-value current-limiting resistor or a voltage-resistive divider to sense the ac voltage at the controller's I/O pin. However, depending on whether the I/O pin is in TTL or Schmitt-trigger mode, the ZCD has a delay that depends on the threshold swing of the I/O pin and the slew rate of the power line. For example, assume a 230V, 50-Hz ac system voltage and a voltage divider of 100—that is, 230V/100=2.3V. Further, assume that the I/O pin triggers at 1V. This trigger level implies $1V \times 100 = 100V$ referenced to the 230V-ac mains. Thus, $100 = 230 \times \sin(2 \times \pi \times 50 \times t)$ yields a delay of 1.43 msec, which represents 14.3% of the half-cycle period—a significant error.

Figure 1 shows a low-cost, efficient ZCD using two standard transistors. Coming directly from the ac mains,

the supply network comprising C_1, C_2, D_1, D_2, and R_1 forms a simple half-wave rectifier, which powers the ZCD. Q_1 toggles with the ac-mains-voltage ZCD. To compensate for the base-emitter gap, Q_2 acts as a diode to block the ac-positive cycle. For efficiency, the detector must sense the ac-mains cycles at as high a voltage as possible. This requirement drives the choice of the transistor. Q_2 and Q_1, low-noise, small-signal BC549B transistors, have collector-to-emitter-voltage limits of 30V. With this choice, you must attenuate the ac-mains voltage from 230 to 30V. (For a BC546 transistor, you can attenuate 230 to 80V.) Thus, the voltage-divider ratio is 30V/230V=13.4%, and the values of the divider resistors are $R_2/(R_3+R_2)=13.4/100$, or $R_3=6.46\times R_2$. R_2 and R_3 must be high enough for current limiting. The normalized value of R_3, 820 kΩ, means that R_2 is 820 kΩ/6.46=126.9 kΩ or 120 kΩ, the nearest standard-value resistor. With these values, Q_2 can block $230V\times R_2/(R_2+R_3)=29.3V$, which is less than the transistor's maximum rating of 30V.

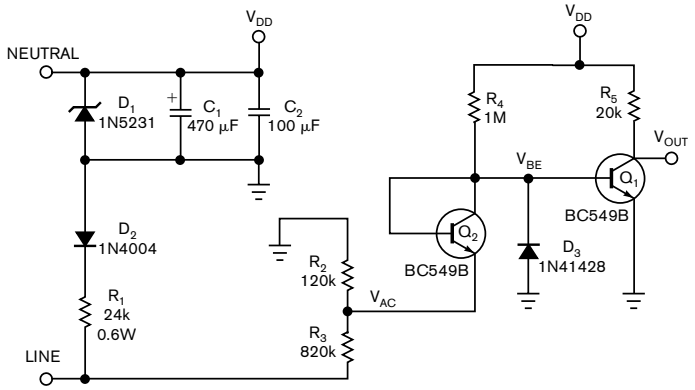

Figure 1 This simple two-transistor circuit accurately detects the zero crossing of the input ac mains.

Upon the ac-positive cycle, the base of Q_1 rises to approximately 0.6V through R_4. Q_2 acts as a simple diode. So, when the cycle voltage is higher than 0V, Q_2 is reverse-biased and blocks any current flow. At 0V, Q_2 is forward-biased, but it maintains 0.6V across the base-emitter junction, V_{BE}. Thus, the collector, or base, of Q_2, which connects to the base of Q_1, stays at 0.6V. Q_1 is saturated for the positive cycle, and the output voltage is low. At the ac's negative cycle, when the ac voltage is less than 0V, current flows through Q_2. Consequently, the base of Q_1, which connects to Q_2's collector, falls to less than 0.6V, which leads to the blocking of Q_1 and the output voltage's becoming high. Note that the base of Q_1 can reach about −30V from Q_2; you can add clamp diode D_3 for Q_1 junction protection higher than −1V. EDN

EDITED BY CHARLES H SMALL
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Add a grounded-switch feature for Topswitch on/off control

Robert N Buono, Aeolian Audio LLC, Bloomfield, NJ

The Power Integrations Topswitch family (www.powerint.com/topgxproduct.htm) of integrated flyback-regulator ICs provides exceptional performance in small, low-pin-count packages. For the lowest-pin-count packages, the multifunction, or M, pin serves multiple purposes, including on/off control and undervoltage- and overvoltage-input detection. Other package types include an L pin, which also provides this function. The application notes and data sheets show how to implement the various features available at these pins. For example, to allow remote on/off control and still preserve undervoltage and overvoltage functions, the application drawings show an NPN transistor, Q_R, which connects between the M or L pin and the Control pin (**Figure 1**). To turn off the regulator, Q_R must be biased on. To achieve this goal requires a base voltage of 2.6V dc or greater.

The circuit in **Figure 2** provides a new feature that allows you to switch the regulator on or off using a grounded switch that is sometimes more convenient to implement than a switch that references to the Control pin. In the case of a mechanical switch, this circuit would require no external power to implement this function. This feature is important in applications in which the Topswitch power supply is the only source of power. This circuit does not disturb the functioning of the undervoltage and overvoltage functions of the M or L pin. To understand the functioning of the circuit in **Figure 2** requires an explanation of the internal workings of the M or L pin. This pin acts as a constant voltage source at approximately 2V dc and sinks current from the external circuit, which R_{LS} supplies. The internal current-sense thresholds for undervoltage and overvoltage detection are roughly 50 µA

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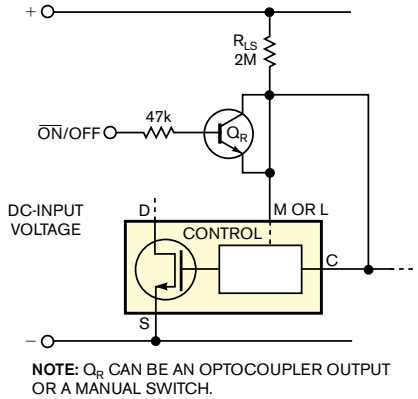

Figure 1 Adding transistor Q_R to the L pin of a Topswitch switching power controller enables an on/off-control feature.

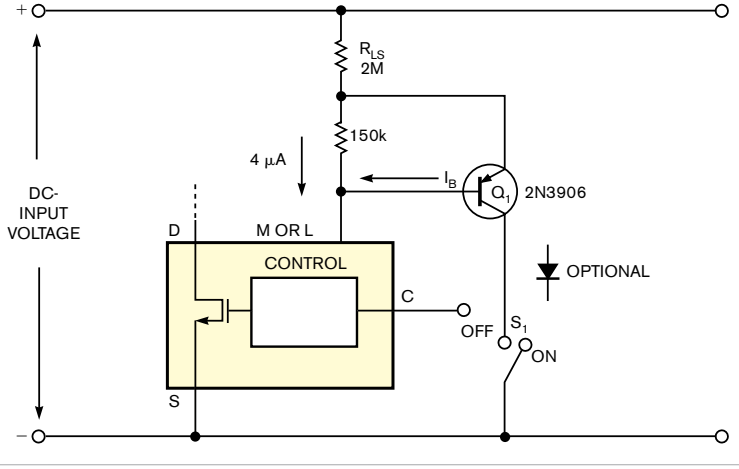

Figure 2 Instead of using just the external transistor to switch a Topswitch on or off, a simple on/off switch provides manual on/off control.

with 30 µA of hysteresis for undervoltage and 225 µA for overvoltage. That is, when the current into the M or L pin is less than 20 µA, or 50−30 µA, the regulator output switches off because of undervoltage. When the current into the M or L pin exceeds 225 µA, the regulator output switches off because of overvoltage. When the current into the M or L pin is 50 to 225 µA, the output is enabled.

The circuit of **Figure 2** works as follows: When the switch in the collector lead of Q_1 is open, Q_1 functions as a simple diode with a 0.6V drop from emitter to base. All the current that R_{LS} supplies flows into the M or L pin through the base-emitter junction of Q_1 and the 150-kΩ resistor. In this mode, the Topswitch IC senses the undervoltage and overvoltage thresholds. However, when the switch to ground closes, Q_1 functions as a nonsaturated transistor with high gain. The circuit siphons off most of the current through R_{LS} to ground as the collector current of Q_1. Only a small base current from Q_1 plus 4 µA through the 150-kΩ resistor flows into the M or L pin. For the values in **Figure 2**, this base current is less than 3.8 µA, even when Q_1 has minimum gain and input voltage is at a maximum of 450V dc. Therefore, 3.8+4 µA, or 7.8 µA, flows into the M or L pin. This low current flowing into the pin "fools" the regulator into "thinking" that the input voltage is undervoltage, and the regulator output switches off.

If another voltage or current source is present, you could replace S_1 with an open-collector switch that sinks current only. If the remote on/off driver can source and sink current, as the output of a logic gate can, then you should insert a diode in the collector lead of Q_1, and the driver must drive the cathode of that diode above 2V dc to turn off the regulator (optional in **Figure 2**). The M pin also allows current-limit-threshold adjustment. EDN

RC lowpass filter expands microcomputer's output port

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

It's almost a corollary to Moore's Law: Next year, microcomputers will have more features, and the software team will have bigger ideas. Unfortunately, though, the number of output pins will stay the same. Finding even one spare output for diagnostics, test, or even standard I/O can be a tussle. The single-pin "bus" in **Figure 1** can provide an unlimited number of parallel outputs with simple additional hardware. A microcomputer output with an RC lowpass filter controls serial-to-parallel converter HC164. To enter data into the serial-to-parallel converter, each bit consists of a one-to-zero-to-one transition, which alters the length of the low state. If the low state is longer than the lowpass filter's time constant, a zero shifts into the register. If the low state is short, then a one shifts into the register. The clock and data signals thus combine into one signal. A lowpass filter separates the clock and data signals (**Figure 2**).

Listing 1, a simple "Whip" routine,

LISTING 1 WHIP-ROUTINE OUTPUT FUNCTION

```
Whip                                    ;  the data to transmit is in W
        MOVWF       My_Data
        MOVLW       8
        MOVWF       Bit_Counter         ; set up for eight bits
        BSF         My_Port,  My_Bit    ; ensure output is initially high
B1:
        RLF         My_Data,  F         ; data to send is in CC
        BTFSS       STATUS, CC
        BCF         My_Port,  My_Bit    ; zero, so falling edge is early
        CALL        Delay_10us          ; if a one, pin stays high for 10us
        BCF         My_Port,  My_Bit    ; if a one, edge falls here
                    NOP                 ; ensures output pin is low for 0.2us min
        BSF         My_Port,  My_Bit    ; rising edge here clocks data into HC164
        DECFSZ      Bit_Counter
        GOTO        B1

        RETURN
```

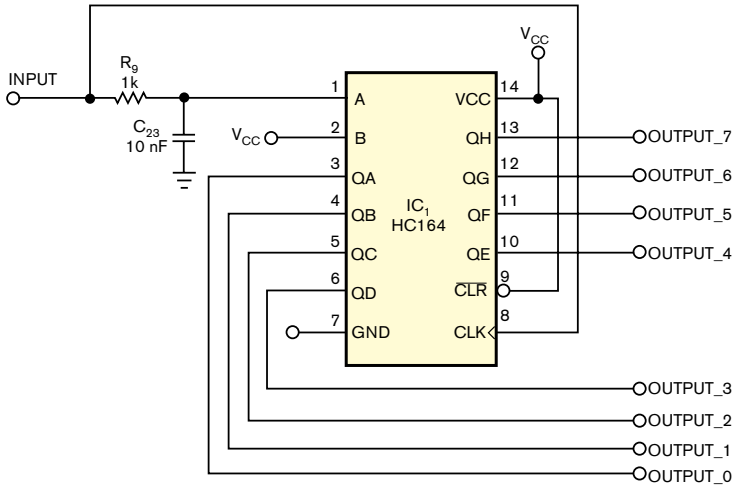

Figure 1 This single-pin "bus" can provide an unlimited number of parallel outputs with simple additional hardware.

performs the output function for eight bits. Assume that the RC time constant is 3 µsec, and the instruction time should be 1 µsec or less at a crystal frequency of 4 MHz or greater. The routine uses bitwise manipulation of output My_Bit of port My_Port.

Although the circuit in **Figure 1** can control slow-reacting devices, such as relays or LCDs, using it with LEDs can give an annoying flicker when the HC164 is writing. To address that problem, the circuit in **Figure 3** uses another serial-in/parallel-out register, the 4094, which has a strobe input to allow simultaneous updates of all outputs without temporary levels. A twin monostable circuit supplies the data and strobe signals. This circuit should be able to control parallel devices, such as display modules based on HD44780 devices. EDN

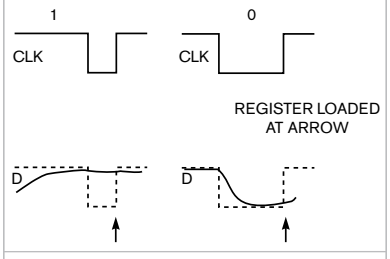

Figure 2 The clock and data signals combine into one signal.

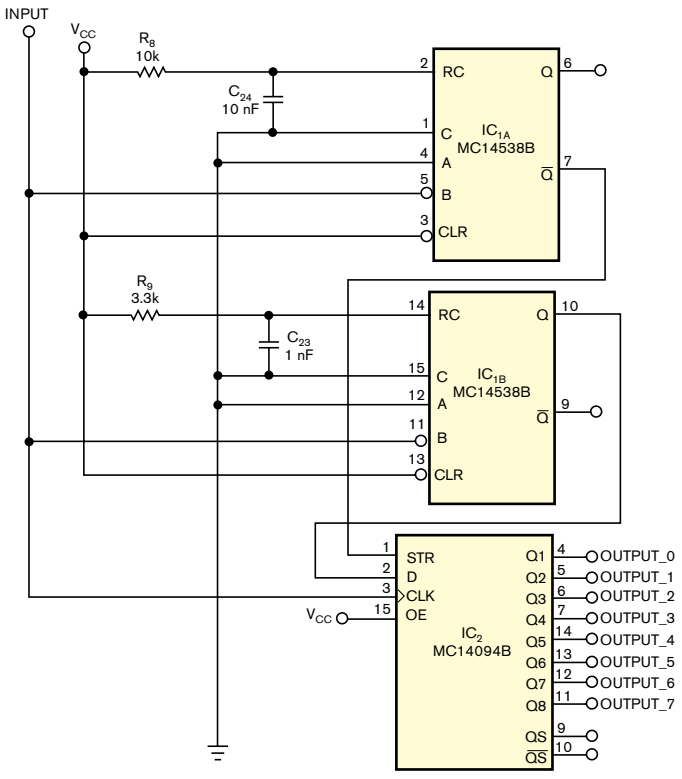

Figure 3 This circuit uses another serial-in/parallel-out register, the 4094, which has a strobe input to allow simultaneous updates of all outputs without temporary levels.

Simple dual constant-current load tests low-current power supplies

John S Lo Giudice, STMicroelectronics, Schaumburg, IL

Today's small electronic appliances, such as washers, dryers, and stoves, use switched-mode power supplies to replace bulky, heavy, linear-power supplies. The engineer testing these power supplies, which range in current from 50 mA to 1A, typically uses resistors or standard off-the-shelf electronic loads. An engineer would employ a variety of high-wattage resistors to verify multiple loading conditions to satisfy a proper design. Most off-the-shelf electronic loads target an average of 300W. When measuring 50 to 300 mA, a display is inaccurate; most of them display 0.1A, but accuracy is questionable at that low range. You can alternatively use the simple dual constant-current-load design in **Figure 1**, which you can build with inexpensive, common parts.

The load current passes through a MOSFET and a 1%, 1Ω sense resistor, R_6. Pin 2 of IC_{1A} compares the voltage drop in the resistor to a reference voltage. IC_1, an LM358 op amp, compares the two inputs and adjusts its output accordingly. The reference voltage at Pin 3 of IC_{1A} comes from a voltage-divider potentiometer, R_2 or R_3, which derives from a TS431 1.25V 1% reference. Because the maximum voltage can be 1.25V and the sense resistor's value is 1Ω, the maximum current per channel can reach 1.25A.

R_2 and R_3 are 15-turn, 1-kΩ potentiometers, which you can finely adjust to the desired load. One can set a minimum current, and the other can set a maximum current. Switch S_1 can then switch between minimum load, no load in the middle position, and maximum load. Furthermore, by attaching a standard DMM (digital multimeter) across R_6, you can directly read the current and adjust it to the proper level.

Input-voltage change does not affect the DMM's reading because it monitors the constant current through sense resistor R_6. The second channel is a duplicate of the first. Each chan-

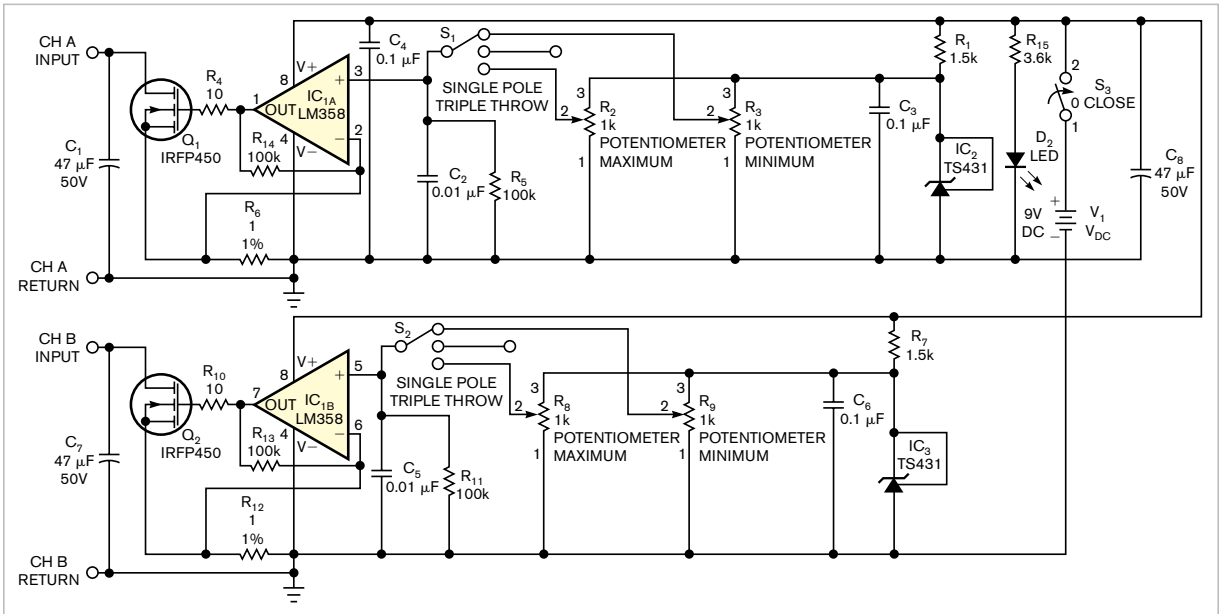

Figure 1 This dual constant-current load can measure the performance of dual power supplies supplying 0 to 1.25A per channel.

nel can control 0 to 1.25A and can handle a voltage of 3 to 50V. The capacitor input and the MOSFET set the upper limit. The two inputs can be in parallel to a load of 2.5A. For a two-output power supply, you can set the minimum and maximum current by precisely reading the level on a multimeter and then quickly testing a matrix of no load, minimum load, and maximum load. A 9V battery powers the unit. EDN

Stepper-motor motion controller and driver fit into a CPLD/FPGA

Stephan Roche, Santa Rosa, CA

This Design Idea further develops a previous one integrating a stepper-motor driver in a CPLD (**Reference 1**). However, this idea integrates not only the driver, but also a simple one-axis stepper-motor motion controller. Depending on the size of the target CPLD, you can implement multiple motion controllers into a single device. For example, a single-axis motion controller fits into a Xilinx (www.xilinx.com) XC95108 using 68 of, or 63% of, the available macrocells. The motion controller rotates the stepper motor clockwise or counterclockwise a given number of steps with a given speed profile versus time. When a motion begins, the controller accelerates until it reaches the cruise speed and then decelerates before stopping (**Figure 1**).

The controller can adjust the motor speed to 16 values, $V=V_{MAX}\times speed/16$, where speed is an integer with a value of one to 16. During the acceleration phase, the speed ramps up by increasing from one to 16; during the cruise phase, speed stays at 16; finally, during the deceleration phase, speed ramps down to one before stopping. If there are insufficient steps for the controller to reach the cruise phase, the controller goes directly from the acceleration phase to the deceleration phase. You can adjust the acceleration/deceleration rate in the program, which you can find at www.edn.com/070621di1 by the constant "accel," which can be one to 255. A high value of accel results in a slow acceleration/deceleration, and a low value results in a fast acceleration/deceleration. The inputs of the CPLD stepper-motor controller are clock, direction, full/half-step, reset, Nstep, start, and stop.

The clock input is active on the positive edge of the clock pulse. The maximum motor speed is one step every 16 clocks. The direction input determines the motor's rotational direction. The motor runs clockwise or counter-

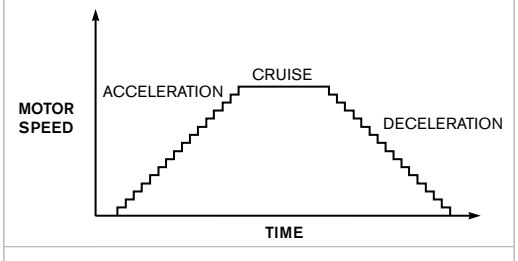

Figure 1 This design can control the motor with 16 speeds. The maximum speed in the cruise phase is such that the motor makes a step or half-step every 16 clock cycles.

clockwise, depending on the level of this input and the motor connections. That value is latched at the first rising clock edge after start goes high. The full/half-step input determines the angular rotation of the motor for each clock pulse. In the low state, the motor makes a full step for each applied clock pulse, and, in the high state, the motor makes a half-step. A high level on the reset input sets the motor in a defined state. The motor ignores any clock pulse when reset is high. The 16-bit Nstep value defines the number of steps the next motion will perform. That value is latched at the first rising clock edge after start goes high. A high level on the start input starts the motion, and a high level on the stop input stops the motion, aborting the current motion.

The outputs of the CPLD stepper-motor driver are A, A_N, B, and B_N (**Figure 2**). The A and A_N outputs control one of the motor's coils through power drivers, and the B and B_N outputs control the motor's second coil through power drivers.

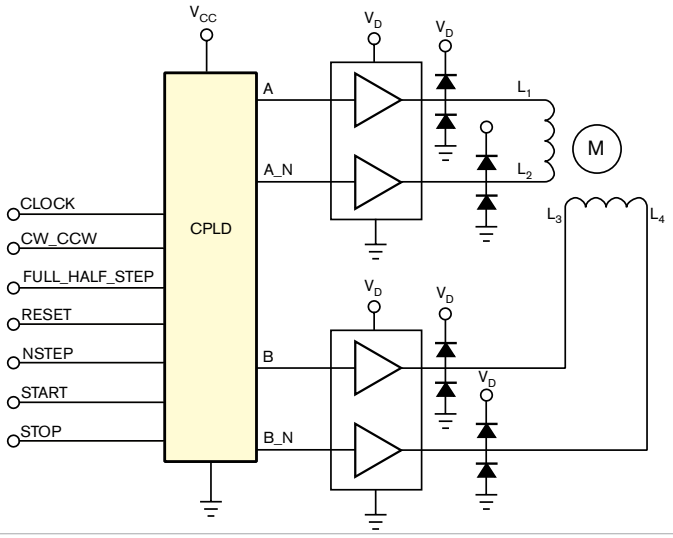

Figure 2 The FPGA/CPLD requires external drivers.

The CPLD/FPGA cannot directly drive the motor, so it requires external drivers. The driver must arrive at the motor's nominal voltage. The Schottky diodes at the output of each driver allow current freewheeling in the motor coils. If you use MOSFET drivers, external Schottky diodes should be unnecessary because MOSFETs have built-in diodes; the Microchip (www.microchip.com) TC4424A dual driver can drive motor coils to 18V and 3A. EDN

REFERENCE

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READERS SOLVE DESIGN PROBLEMS

Build a complete industrial-ADC interface using a microcontroller and a sigma-delta modulator

Patrick Weber and Craig Windish,
Siemens Energy and Automation, Pittsburgh, PA

Designers commonly use 0- to 20-mA, 0 to 10V isolated inputs for industrial-application-control signals. A combination of isolated supplies, the built-in isolation of an Analog Devices (www.analog.com) AD7400 sigma-delta modulator, and a Texas Instruments (www.ti.com) MSP430 microcontroller creates a design for industrial designers requiring complete, isolated, and robust analog-signal interfaces. A precise signal-conditioning circuit generates the small differential voltage that the AD7400 requires (**Figure 1**). The circuit generates the required 200-mV differential voltage. For clarity, the **figure** omits overvoltage diodes and protection circuits.

A 0- to 20-mA current loop converts to a voltage through a properly scaled resistor, R_2, and enters a precision operational amplifier. The signal level, which connects to the negative input, gets a positive offset by maintaining constant voltage on the positive input of the amplifier. The 0 to 10V signal, such as that from a potentiometer, also scales to a similar voltage to that of the 0- to 20-mA sig-

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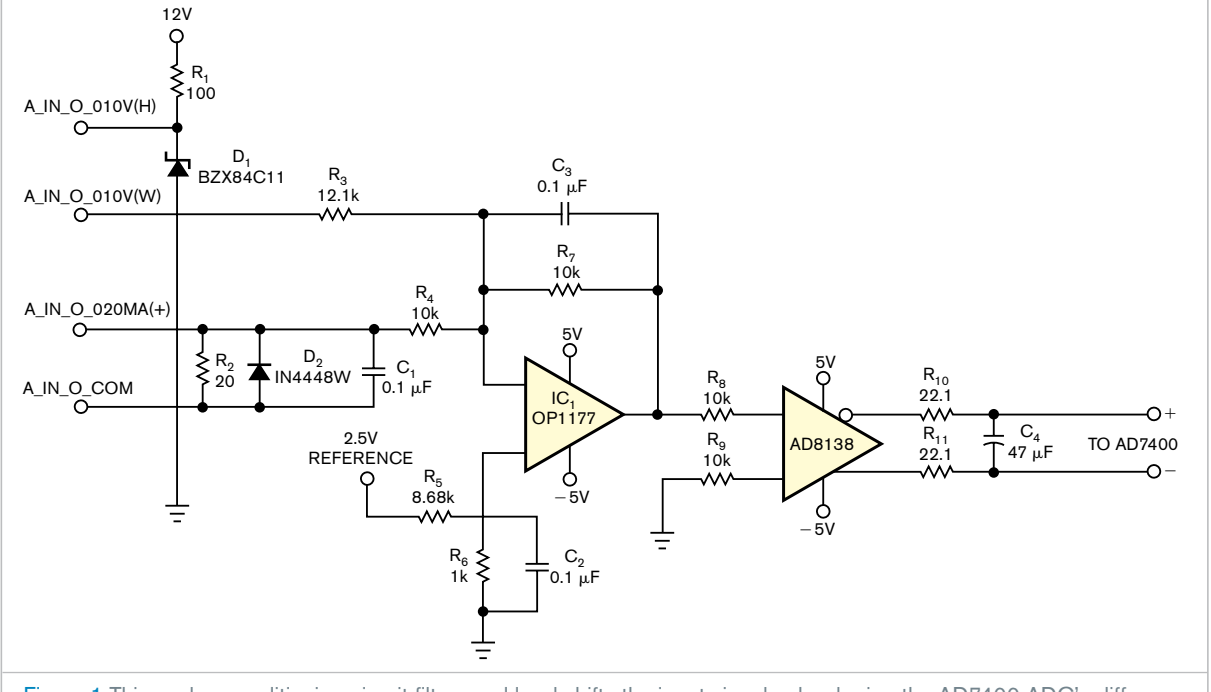

Figure 1 This analog-conditioning circuit filters and level-shifts the input signals, developing the AD7400 ADC's differential input.

nal and gets summed into the negative terminal of the Analog Devices OP1177 amplifier, IC_1.

Shifting the signal above 0V results in a signal that is similar to a positive, single-ended analog signal. A differential ADC-driver amplifier, Analog Devices' AD8138, drives the AD7400. The gain scales such that the resultant signal is within ±200 mV, which the ADC requires. Finally, before connecting to the AD7400, the signal runs through a lowpass filter, which R_{10}, R_{11}, and C_4 create between the positive and the negative terminals. The AD7400 converts this differential signal and processes it using a low-cost microcontroller. Sigma-delta-modulator ADCs, such as the AD7400, commonly interface to an FPGA or a DSP. However, this approach comes at a high price in both cost and complexity. For cost-sensitive applications not requiring advanced filtering, you can use a simple microcontroller.

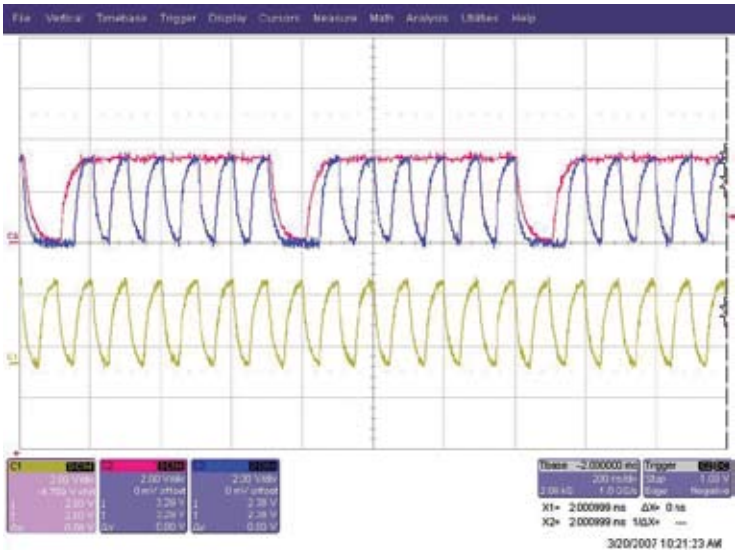

Figure 2 These oscilloscope traces show MDAT, inverted MCLKOUT, and the resulting data stream (courtesy LeCroy).

The AD7400 device has two outputs, MCLKOUT and MDAT (**Figure 2**). MCLKOUT, a 10-MHz clock, synchronizes the modulated data stream, MDAT. The AD7400 interprets MDAT as a percentage of ones over time. Because MDAT changes

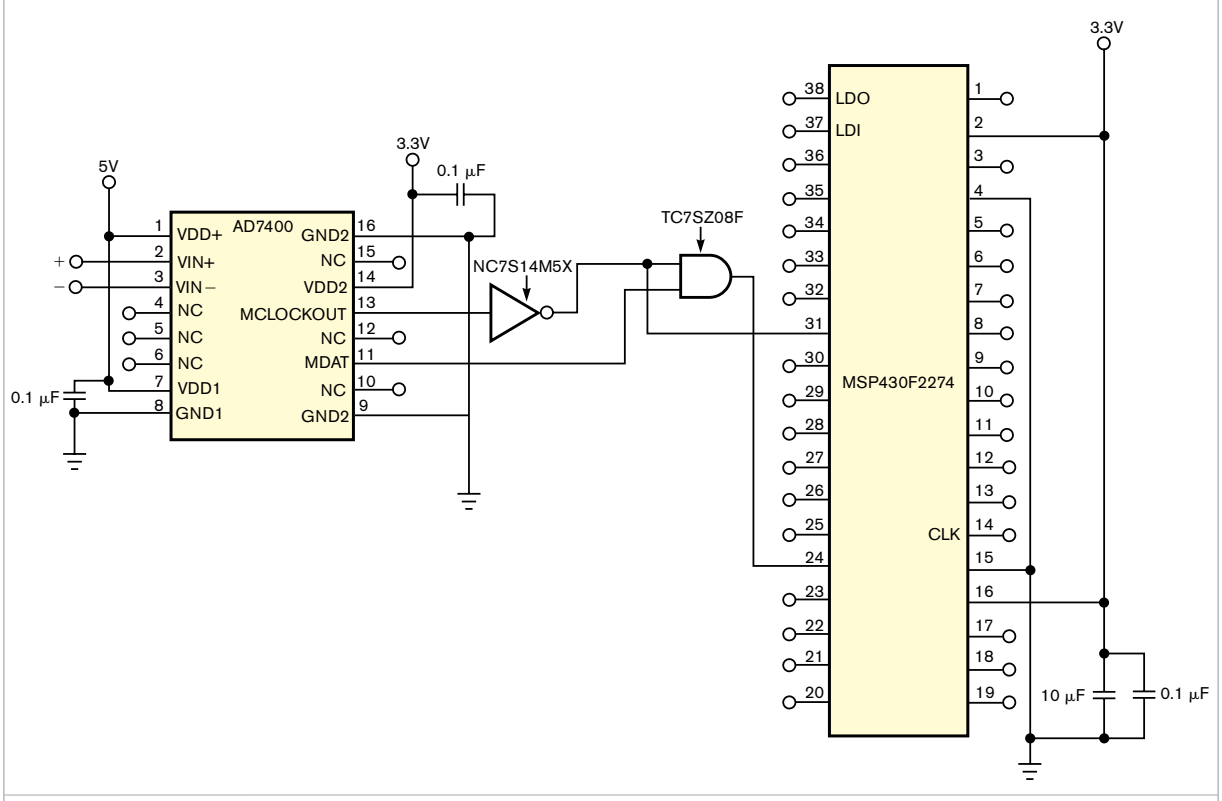

Figure 3 The AD7400 serial ADC digitizes the analog input and feeds the simple, low-cost microcontroller.

only at the rising edge of MCLKOUT, the circuit must AND together MDAT and MCLKOUT to create a stream of pulses that the microcontroller can count. The microcontroller first inverts MCLKOUT to prevent unintentional glitches from being counted at the transition edges of MDAT. The **figure** shows MDAT, inverted MCLKOUT, and the resulting data stream.

The pulsed data signal and the inverted MCLKOUT each feed into a separate timer/counter on the microcontroller (**Figure 3**). The TI MSP430F2274 provides two 16-bit counters and can support operation as fast as 16 MHz. The circuit measures the ADC value by sampling the data counter when the clock counter signals an overflow interrupt. For this application, running an average number of data measurements on a circular buffer may conveniently filter the data. EDN

Circuit guards amplifier outputs against overvoltage

John Guy, Maxim Integrated Products, Sunnyvale, CA

A universal requirement for automotive electronics is that any device with direct connections to the wiring harness must be able to withstand shorts to the battery voltage. Though brutal, this requirement is necessary for reliability and for safety. One example of the need for this protection is an audio amplifier that produces indicator noises in the automotive interior. Though operating from a voltage of 3.3 or 5V, which is lower than the battery voltage, the amplifier must be able to stand off the full battery voltage. You can also use a protection network appropriate for these amplifiers for other automotive circuits (**Figure 1**). A dual N-channel MOSFET disconnects the amplifier's outputs from the wiring harness in response to a high-voltage condition on either output. The MOSFETs, Q_{1A} and Q_{1B}, are normally on; zener diode D_4 and its bias components drive the MOSFETs' gates to approximately 11V. Dual diode D_3 provides a diode-OR connection to the dc voltage on each output, thereby producing a voltage that controls the output of shunt regulator IC_2. The circuitry protects IC_1, a 1.4W Class AB amplifier suitable for audible warnings and indications for the automotive electronics.

During normal operation, the amplifier outputs' dc components are at

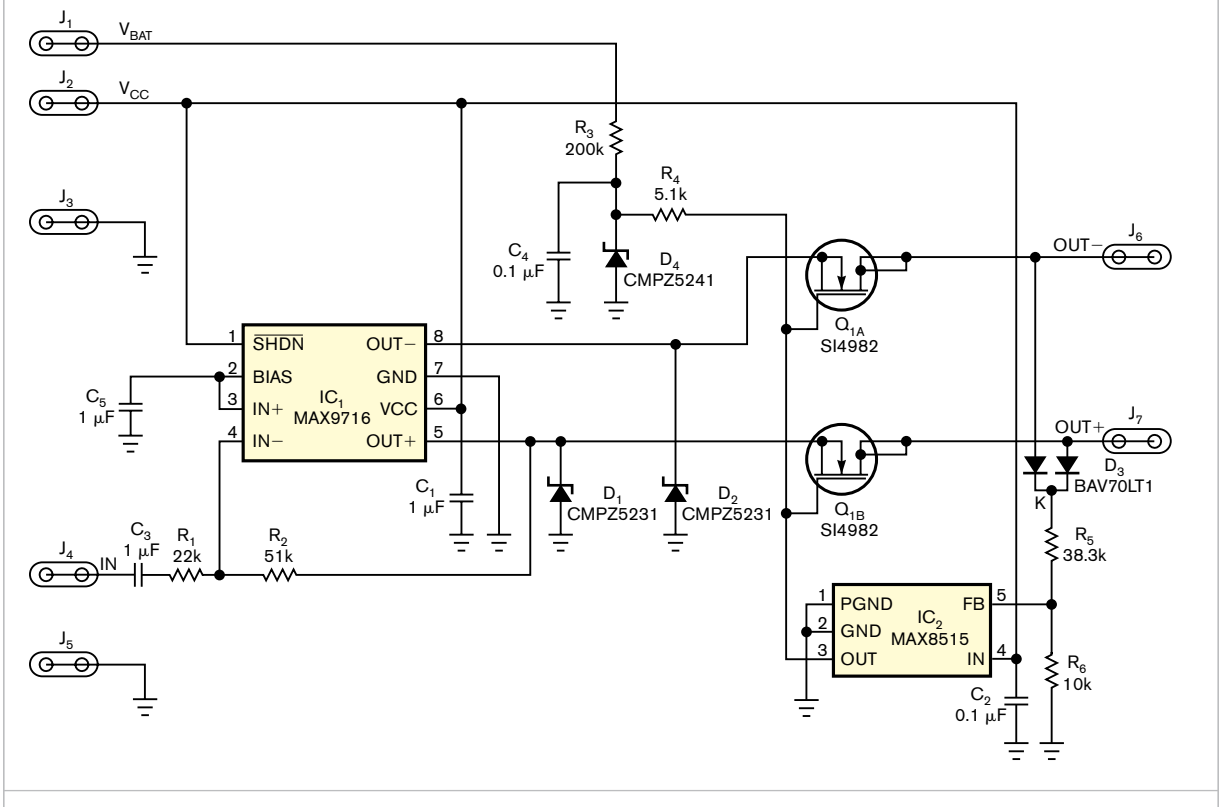

Figure 1 This output-protection circuit provides continuous protection against overvoltage faults.

one-half of the V_{CC} supply—2.5V in this case, for which V_{CC} is 5V. The 11V gate drive fully enhances the MOSFETs, and the shunt-regulator output is off because its feedback input, Pin 5, is below its internal 0.6V threshold. If either output exceeds 5V, current flows through D_3 into the R_5/R_6 divider, pulling the feedback terminal above its threshold. The shunt-regulator output then pulls the MOSFET-gate voltage from 11V almost to ground, which blocks high voltage from the amplifier by turning off the MOSFETs. The MOSFETs easily withstand the continuous output voltage, and the circuit returns to normal operation when you remove the short. Because the circuit does not respond instantaneously, zener diodes D_1 and D_2 provide protection at the beginning of a fault condition.

The waveforms of **Figure 2** represent an operating circuit. One of the amplifier's outputs (Trace 1) is a 1-kHz sine wave biased at a dc voltage of 2.5V. Trace 2 is the signal on the wire harness. It also starts as a 1-kHz sine wave biased at a 2.5V-dc voltage, but, at 200 µsec, it shorts to an 18V supply. Trace 3 is the shunt regulator's output, initially biased at 11V but pulled to ground in response to the overvoltage condition. Trace 4 is current in the wire harness. Initially a sine wave, this current drops to zero in response to the overvoltage condition.

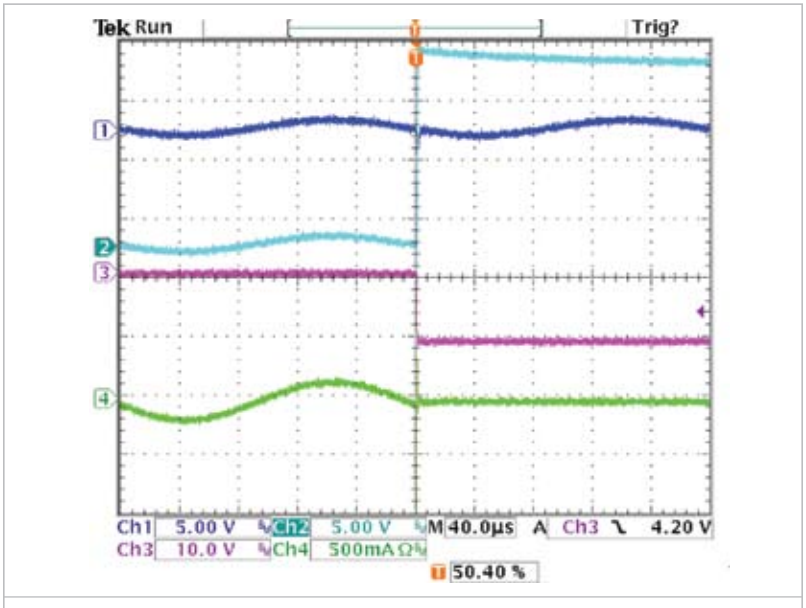

Figure 2 In Figure 1, one of IC_1's two audio outputs (Trace 1) has protection when its external terminal accidentally contacts an 18V supply voltage (Trace 2).

The components in **Figure 1** optimize this circuit for 5V operation. For other voltages, you can adjust the R_5/R_6 resistor values. The shunt regulator must be able to function in saturation and, therefore, requires a separate supply pin in addition to the shunt output pin. The circuit repeatedly withstands 28V shorts without damage. EDN

Isolated circuit monitors ac line

David Williams, Millington, MI

The circuit in **Figure 1** provides a low-cost, isolated ac-line monitor that measures ac-line-voltage level and has some other unique capabilities. The analysis of the circuit is straightforward: When the ac input, V_{IN}, is positive relative to neutral, you apply it to the network comprising R_1, R_2, D_1, and the LED in optocoupler IC_1. Current flows in this network when the voltage is high enough to get zener diode D_1 and the diode in the optocoupler to conduct. This diode pair's conducting voltage is the enable voltage, V_E. The zener diode's reverse-breakdown voltage of 47V and the optocoupler's LED forward voltage of 1.2V make the enable voltage 48.2V. Any voltage below this level drives the output of the optocoupler high. When the voltage exceeds the enable voltage, the transistor in the optocoupler becomes saturated, pulling the output low. The output continues to stay low until the input voltage drops below the enable voltage.

The resulting output is a square wave with a fixed time, t_{TOTAL}, based on how long the input voltage is above the enable voltage. If the voltage on the input varies from 120 to 144V, the resulting square-wave waveform becomes wider; if the voltage varies downward, the pulse width decreases. To calculate the formula for this circuit, consider the input waveform as a cosine function. Because the input voltage peaks at time zero, the optocoupler circuit is on, and the output voltage is low. It continues to be low until the input voltage moves below the enable voltage. The following **equation** yields the time when this crossover happens:

$$V_E = V_{IN} \times \cos(2 \times \pi \times f \times t_{ON}).$$

Because the cosine function is symmetrical around zero, time t_{ON} is half the total time that the output pulse is high. Because a microprocessor's timer port usually captures the time, the simplest way to calculate the input voltage from the pulse width is to replace the on-time with the total time and then to solve the equation for the input voltage, which gives the result as a function of the measured pulse-width output from the optocoupler:

$$V_{IN} = \frac{V_E}{\cos(\pi \times f \times t_{TOTAL})}.$$

You can implement this formula in software or a look-up table that converts pulse width to input voltage. Take note that the input voltage is the peak ac voltage, so you must convert it to the rms value if necessary. You can also use this circuit as a clock line because the output frequency is independent of the duty cycle. The output is consistently 60 Hz, and you can use it for timekeeping. You can also potentially use it for zero-crossing-load driving if you extrapolate the time back to the zero crossing based on the input voltage, because the duty-cycle edge timeshifts from the real zero crossing.

Some other design principles in this circuit require attention. D_2 protects the diode in the optocoupler when the ac input goes negative. In most cases, the optocoupler diode is unaffected because the reverse leakage through the network ensures that the LED does not exceed its maximum reverse voltage. However, bypassing the diode is the best approach for clamping the voltage across this optocoupler using a diode. Adding this diode does more than double the quiescent current in the circuit, and, because you apply this current to the ac line, it may be a concern for both energy consumption and power dissipation in the resistors in the input circuit.

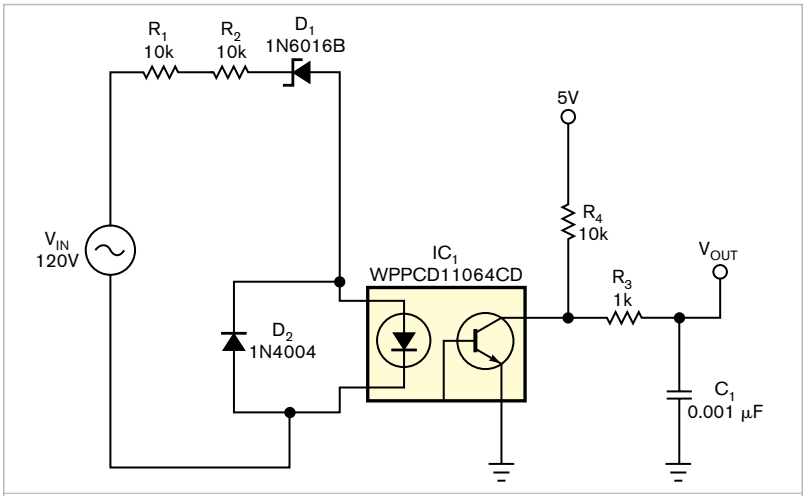

Figure 1 This simple ac-mains voltage monitor's output is a square wave whose width is proportional to the input-voltage level.

If you need a more accurate estimation of input voltage, some options improve circuit function. The main source of this variation is the 5% tolerance on the zener voltage. A 5% variation on this voltage can result in a significant error in your estimate of the input-voltage amplitude. Specifying a more precise diode or calibrating each board by applying a known input voltage and storing that value in memory as a fixed calibration improve the overall accuracy of this circuit. EDN

I²C interface has galvanic isolation, wired-OR capability, improved noise margin

Michele Costantino, Microsaic Systems Ltd, Woking, United Kingdom

This Design Idea describes a simple and effective way to provide optoisolation for devices connected on the I²C bus (**Figure 1**). It improves on an earlier version (**Reference 1**). SDA and SCL are on the bus master's side of the I²C bus; SDA_1 and SCL_1 are on the slave device's side. It is fairly easy to optoisolate the clock line because it is unidirectional, from the master to the slave device. A P-channel MOSFET, Q_3, provides the current for the LED of the fast optocoupler, IC_2, buffering the clock line.

The data line, however, is bidirectional. This section of the circuit is symmetrical. Resistors R_6 and R_7 are the I²C pullup resistors on the slave device's side of the bus, and R_3 and R_1 are dummy pullups in parallel with the main I²C pullup resistors on the SDA/SCL side. If both SDA and SDA_1 lines are high—that is, no I²C devices are pulling them down—Q_1 is off, no current flows into the LED of optocoupler IC_2, IC_2's Pin 7 is high, Q_2 is off, and the LED of optocoupler IC_1 is also off.

THE LED OF IC_1 DOES NOT TURN ON BECAUSE THE VOLTAGE APPLIED ACROSS IT IS BELOW ITS THRESHOLD.

If a device drives the SDA line low, Q_1 and the LED of IC_2 turn off, driving IC_2's Pin 7 low; diode D_2 then starts to conduct. The result is a low level on the SDA_1 line—the low output voltage of IC_2 plus the threshold voltage of Schottky barrier diode D_2. In this situation, it is important to notice that the LED of IC_1 does not turn on because the voltage applied across it is below its threshold. This situation means that the circuit does not latch, and it can recover from this state once you release the SDA line.

Q_3 and the PNP BJT (bipolar-junction transistor), Q_1, effectively buffer the two SDA/SCL lines so that no extra current flows into the open-collector and -drain stages of the I²C

devices that connect to the bus when they hold the lines down. This configuration allows the optoisolated interface to repeatedly pull low, providing wired-OR capability. Using Schottky barrier diodes for D_1 and D_2 rather than common diodes reduces the low-level voltage on the bus, improving the noise margin. Finally, because of the low propagation-delay times of the Fairchild Semiconductor (www.fairchildsemi.com) HCPL06XX devices that this design uses, this interface has no bus-glitch problems and works well at speeds of 400 kHz or higher (**Reference 2**).EDN

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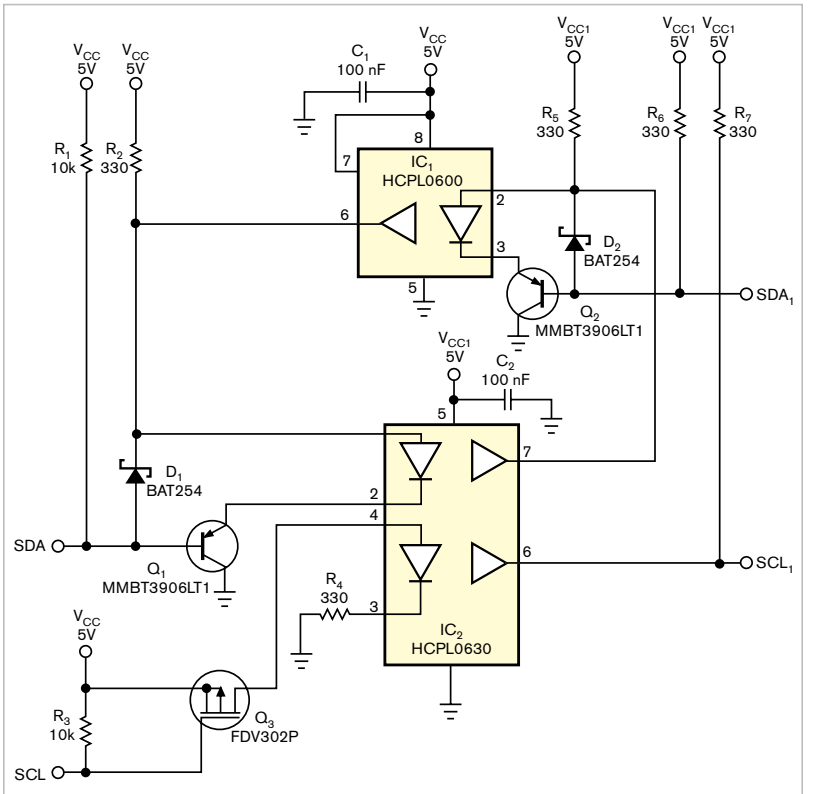

Figure 1 This circuit provides an isolated, bidirectional, wired-OR connection of slave devices to the I²C-bus master.

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READERS SOLVE DESIGN PROBLEMS

Analyzer tests reverse-recovery behavior of diodes

Louis Vlemincq, Belgacom, Evere, Belgium

Testing the reverse-recovery behavior of diodes normally requires complex testing gear. You must be able to establish the forward-conduction conditions, the blocking state, and the transition between the two. You also need a means of extracting the characteristics from the resulting waveform. In short, a specialist should handle this complex job; it is not something you routinely control in the field. This fact explains why engineers generally prefer to rely on published data.

Checking the reverse-recovery time yourself could be advantageous, however, if testing were simple and straightforward. Such a setup would enable you to compare devices from different manufacturers under identical conditions and test devices having no such specification, such as substrate diodes of driver ICs, zener diodes, and standard rectifiers. (Because of the number of combinations of the test parameters, a direct comparison of the data is rare-

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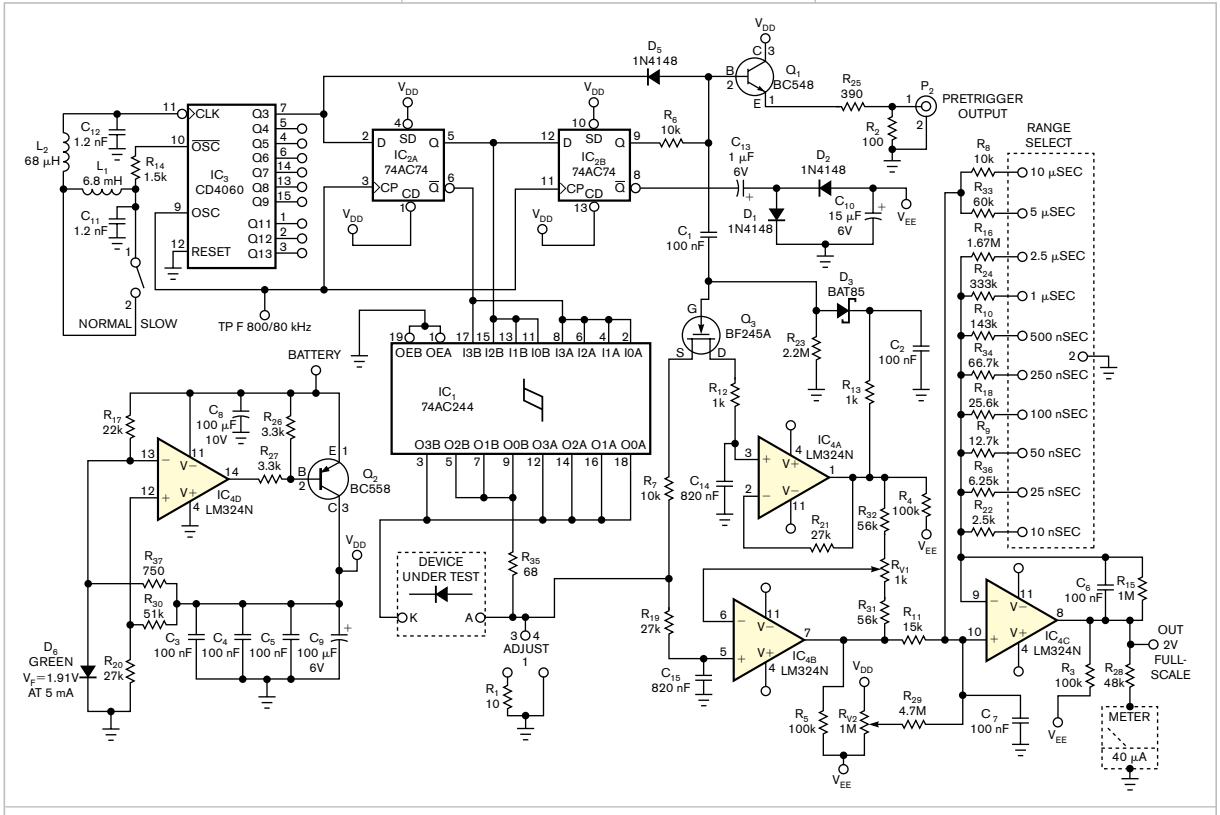

Figure 1 This diode-recovery test setup allows you to compare devices from different manufacturers under identical conditions.

ly possible.) Note that shorter reverse-recovery time is not necessarily better. Slow diodes can be useful, too. They can generate small dead times, improve the efficiency of converters, and provide other benefits (**Reference 1**).

This Design Idea presents a tester that, using only a handful of inexpensive, standard components, allows you to check reverse-recovery time. The test conditions are fixed for simplicity, to normalize the tests and to provide a common standard for comparison purposes. These conditions are compatible with 99% of the devices susceptible to test. The tester's forward current is just low enough to be safe with small switching diodes but high enough to overcome the capacitive effects in larger devices.

A diode-resistor AND gate lies at the heart of the circuit; the gate's diode is the DUT (device under test, **Figure 1**). IC_1 buffers flip-flop IC_{2A}, which derives the antiphase square waves that drive this gate. R_{35} sets the DUT's forward current to approximately 75 mA. With an ideal diode, the gate's output would always stay low, because one of the inputs is always low. But a real diode remains conductive after the transition, generating a positive pulse across R_{35}. Instead of using the brute-force approach of directly measuring this pulse width, the circuit uses a subtler scheme. The R_{19}/C_{15} network averages the pulse and amplifies and displays the resulting voltage. Because the measurement frequency is fixed at 50 kHz, a correct scaling factor is all that is necessary.

A real diode also has a forward voltage, which you would average with the result. Q_3 takes care of this problem by sampling this forward voltage through IC_{4A} and subtracting it from the output voltage through R_{32}. Varying the gain of amplifier IC_{4C} sets the various ranges. In this case, the ranges are in a 1, 2.5, 5 sequence, which suit the salvaged galvanometer this circuit uses as an indicating device. You could easily create other ranges by adapting the values of R_8 through R_{22}. The big advantage of this measuring method is that it handles only dc or low-frequency signals, requiring no fast comparators or samplers, yet it can resolve a few hundreds of picoseconds.

The built-in oscillator of IC_3 generates the clock. The clock frequency is 800 kHz and divides down to produce the 50-kHz reference at Q_3. An optional slow mode is available for those needing to test devices slower than 5 µsec. The insertion of coil L_1 decreases the clock frequency to 80 kHz and enables you to measure reverse-recovery time as fast as 50 µsec. IC_2 generates the test waveforms and shifts the 50-kHz signal at the clock rate. The leading and trailing states then exit through the D_5/R_6 AND gate to produce a sampling pulse that centers on the conduction period. Because the sampling occurs far from any transitions, it need not be particularly fast or accurate. C_1 transfers the sampling pulse and provides a convenient pretrigger signal, which Q_1 buffers. This option enables a comfortable observation of the waveform when you connect an oscilloscope to the anode of the DUT.

The unused output, Pin 8 of IC_{2B}, feeds a negative-voltage generator, serving as a bias source for the outputs of IC_4 to let them reach a true zero. The measurement circuits receive power from a 9V battery by a supply encompassing IC_{4D}. An LED serves as a reference to the 5.5V and provides some temperature compensation because the reverse-recovery time depends highly on ambient temperature.

You can make some adjustments to the circuit. For example, with no diode inserted, you can short the Adjust testpoint 1 to 4. In the 10- or 25-nsec range, R_{V2}, which is 0 nsec in the range, to get a midscale reading. Move the short to Adjust testpoint 3, R_1, and R_{V1}, thereby providing V_F cancellation, to read the same value. Repeat the procedure until the reading is independent of the position of the short. The adjustment interacts with the zero due to the offset of the amplifiers.

Now, you have eliminated the effect of V_F. You can adjust the 0 nsec by shorting Adjust testpoints 1 and 4 and adjusting R_{V2} to read zero on the 10-nsec range. This adjustment yields 0 nsec with a typical offset of 1 to 2 nsec in the positive direction. Residual skew in the timing and charge-injection effects cause this offset. Normally, this offset should not be a problem, because it is small, stable, and constant. If you need an absolute accuracy down to the picosecond, you have to test a known, ultrafast diode, such as an FD700 or a BAY82, and adjust the 0 nsec to read the actual value. If you lack access to such a diode, you can always arbitrarily shift the value by 1.5 nsec. This adjustment is normally sufficient to reach a ±500-psec accuracy. Schottky diodes are unsuitable. Despite their low recovery time, they generate a nonzero reading because of their relatively high capacitance and non-negligible leakage currents. Low-capacitance, mixer-type diodes are too fragile for this tester. EDN

REFERENCE

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High-power LED drivers require no external switches

Alfredo H Saab and Steve Logan, Maxim Integrated Products, Sunnyvale, CA

As the latest generation of new LEDs achieves higher levels of power and efficiency, use of these devices extends to new areas, such as flashlights and vehicular applications. High-power LEDs are finding use even in ambient lighting, long the sole province of incandescent bulbs and fluorescent tubes. A current source is the best way to power LEDs. Because most energy sources, including batteries, generators, and industrial mains, look more like voltage sources than current sources, LEDs require that you insert some

electronic circuitry between them and the source of power. This circuitry can be as simple as a series resistor, but a better choice, considering energy efficiency and other factors, is a high-efficiency, voltage-fed current source. For LEDs with currents greater than 0.35A, an inductive switching regulator is usually the best choice.

This Design Idea presents a series of circuits based on single-power-IC switching regulators, with efficiency and miniaturization as the main objectives. The circuits' designers approach these objectives by minimizing the use of large components, such as external power transistors, switches, high-value capacitors, and current-sense resistors, and by maintaining regular operation by delivering constant, high-intensity light over as extended a range as possible.

The circuits in **figures 1** through **3** are suitable for applications in which the power source comprises three or four alkaline, NiMH (nickel-metal-hydride), or NiCd (nickel-cadmium) cells. Those in **figures 4** and **5** are for vehicular applications in which the nominal line voltage for the power-distribution system is 12, 24, or 42V. The circuits of **figures 4** and **5** are also useful in industrial systems that include a 24V distribution line for control and emergency subsystems and in telecom applications for which the system power is distributed as a −48V line.

The designers of these circuits based them on the same concept: a fully integrated, single-die-IC switching regulator and a micropower operational amplifier. The op amp drives the 1.25V feedback terminal on the IC. Although that node targets the topology of a standard voltage regulator, the op amp matches it to the much smaller current-sense voltage and the slightly different topology of a current regulator. None of the circuits requires the use of external power switches. The design eliminates the use of the large-valued filter capacitors you usually find in a switching regulator, because there is no need to smooth out high-frequency ripple in the LED current. Common to all circuits is the option of adding a dimming capability by introducing adjustable bias at an op-amp input through

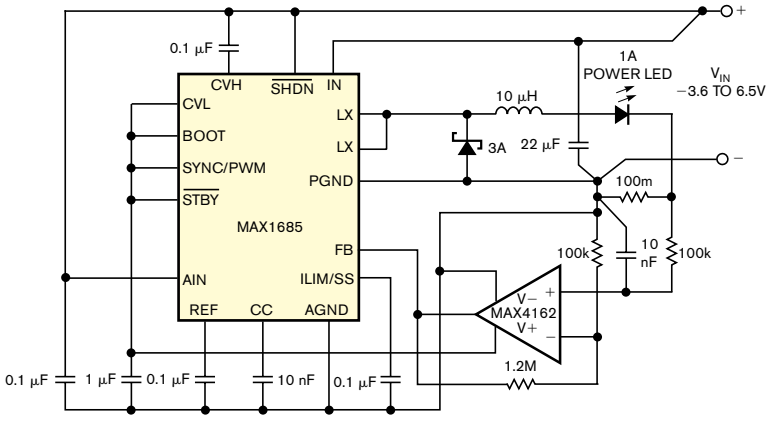

Figure 1 This miniature, 1A, high-power LED driver operates on 3.6 to 6.5V.

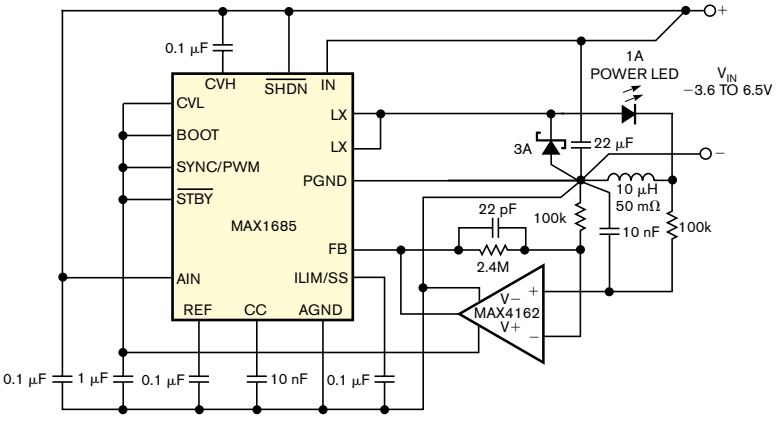

Figure 2 Similar to the circuit in Figure 1, this miniature, 1A, LED driver operates on 3.6 to 6.5V but requires no current-sense resistor.

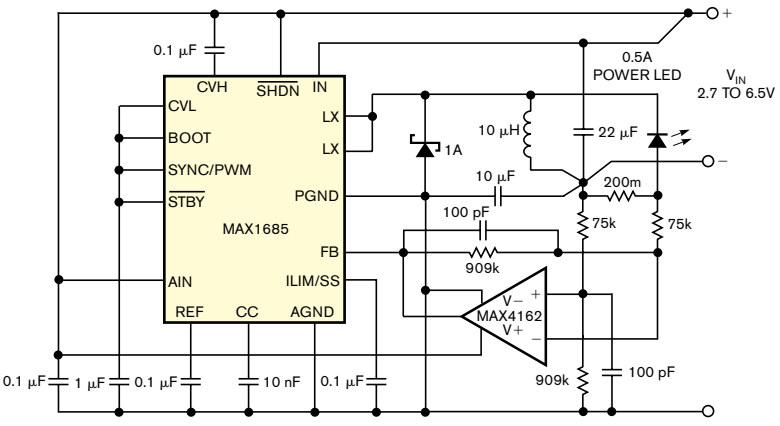

Figure 3 Another miniature, high-power LED driver delivers 0.5A and operates on 2.7 to 6.5V.

a resistor and a potentiometer powered from the internal regulator—the VD or CVL terminal, depending on the IC.

A high-frequency switching regulator powers the basic regulator circuit for LEDs (**Figure 1**). It operates with input voltages of 3.6 to 6.5V, drives a single LED with currents as high as 1A, and uses a current-sense resistor to control the current-regulation loop. The circuit of **Figure 2** is similar, but, in place of a current-sense resistor, it employs the parasitic resistance of the inductor as a current-sensing element. Like the circuit in **Figure 1**, it operates with 3.6 to 6.5V inputs and drives one LED with currents as high as 1A.

For the single-LED circuit of **Figure 3**, the starting voltage of the MAX1685 defines the input range, which goes as low as 2.7V. Its maximum current capability is 0.5A versus 1A for the circuits in **figures 1** and **2**. The upper operating limit remains 6.5V. Once this circuit is operating, it maintains power to the LED even for input voltages as low as 1.7V. Applications for the circuits of **figures 1**, **2**, and **3** include headlights, flashlights, and any other portable lights powered by three or four alkaline primary cells, three or four NiMH/NiCd secondary cells, or a single lithium secondary cell.

The circuits of **figures 4** and **5** operate over 8 to 50V. Assuming a 12V system in which all the components are properly specified, these circuits can survive load dumps, thanks to the 76V absolute maximum rating for the IC's input-power terminal, V_{IN}. The maximum available current is 1A, and the circuits can drive as many as three LEDs in series, provided that you increase the lower limit of the operating range to 11.5V. These two circuits are similar, except for the use of the inductor resistance as a current sensor in **Figure 5**. The disadvantage of using the inductor resistance in this way is the resulting dependence of output current on temperature, due to the large temperature coefficient of copper resistivity. The inductor winding is made of copper, and its dc resistance has a first-order temperature coefficient of 3.9 parts/1000/°C. As a result, the regulated current decreases about 4% for each 10°C increase in operating temperature. EDN

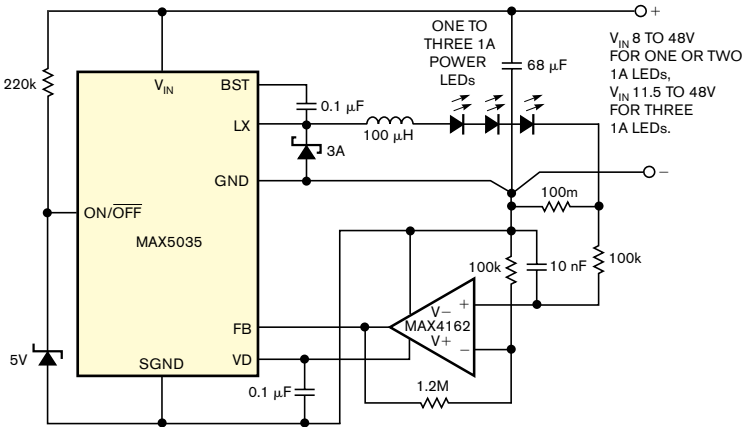

Figure 4 This miniature, 1A, LED-driver circuit operates on 8 to 50V and drives as many as three LEDs in series.

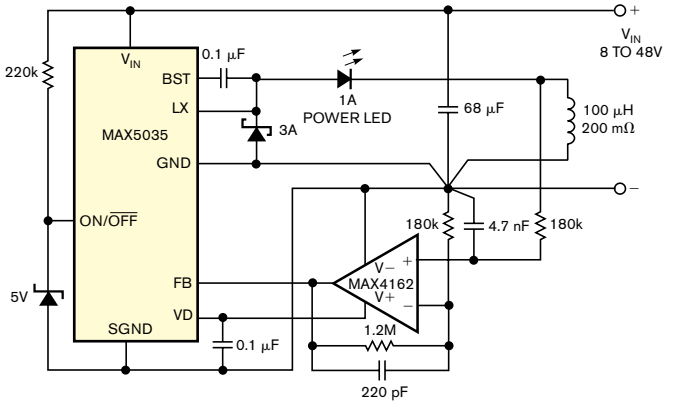

Figure 5 Otherwise similar to the circuit in Figure 4, this circuit requires no sense resistor.

Perform PSRR testing with analyzers having no dc-bias ports

David Karpaty, Analog Devices, Wilmington, MA

An amplifier's PSRR (power-supply-rejection ratio) is among the most commonly characterized parameters when analyzing the performance of an op amp. Examples of some noise sources on an amplifier's power-supply pins include parasitic supply-line traces, their interaction with currents that the amplifier draws, and the noise that switching circuits sharing the same supply create. Both sources produce voltage-amplitude variations reproduced as noise signals at the amplifier's input pins.

Characterizing PSRR over frequency

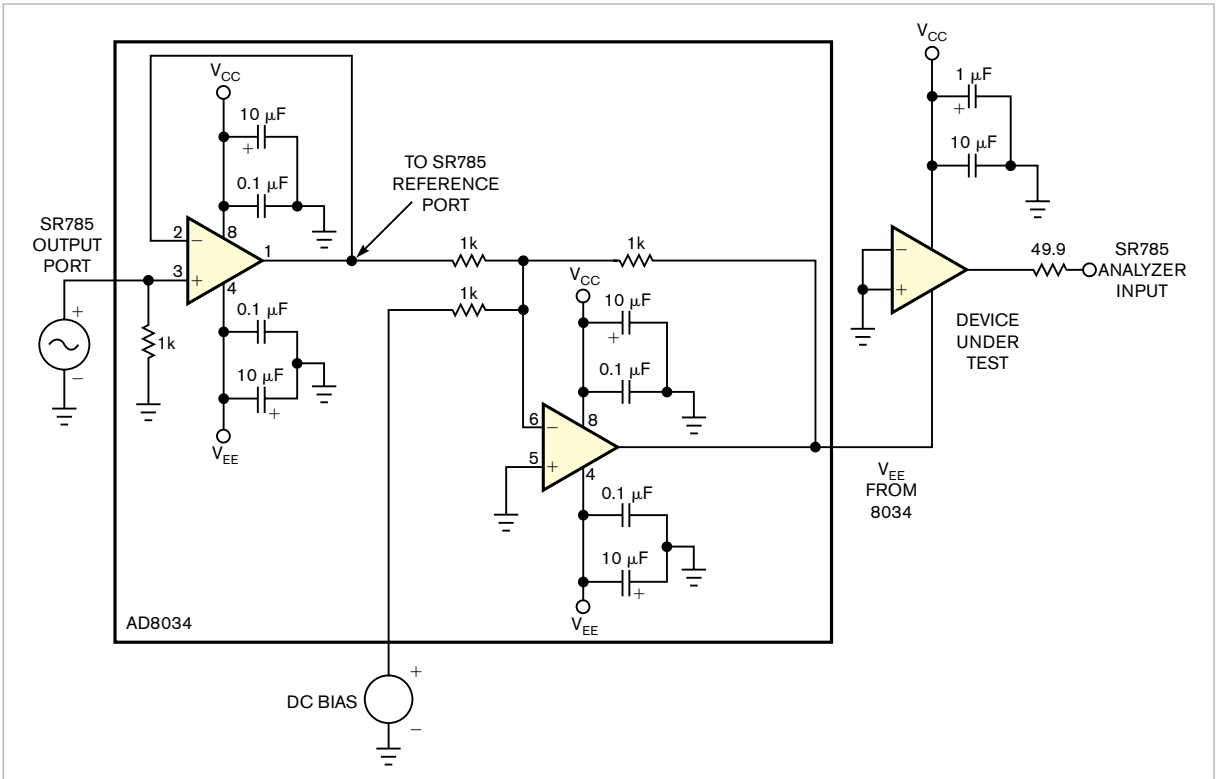

Figure 1 The AD8034 sums the analyzer's reference output and a dc bias, supplying the negative-supply voltage for the device under test to perform negative-PSRR analysis.

commonly involves the use of analyzers equipped with a dc-bias port, such as Agilent's (www.agilent.com) 8753. To measure negative PSRR, for example, the amplifier's $-V_S$ pin comes through Port 1, with the negative dc voltage through the bias port, of the 8753 with a superimposed sinusoid. To complete the measurement, you measure the amplifier's output on Port 2. Unfortunately, the 8753 doesn't measure frequencies below 30 kHz because of the limitations of the analyzer's internal bias, T. Additionally, most PSRR-versus-frequency plots begin at frequencies far below 30 kHz.

An alternative technique would involve the use of an analyzer that has no dc-bias port but that can characterize frequency response as low as 10 or even 1 Hz. One such analyzer is the Stanford Research Systems (www.thinksrs.com) SR785, which can make measurements better than −120 dB. One way of approaching this problem is to connect the output port of the SR785 to a buffer/inverting-summer circuit constructed with an Analog Devices (www.analog.com) AD8034.

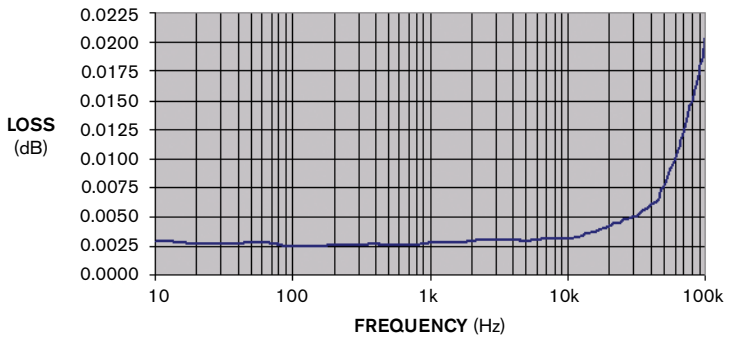

Figure 2 You can neglect any loss the AD8034 incurs. The response of the AD8034 buffer/inverting summer from 10 Hz to 10 kHz is approximately flat.

Figure 1 illustrates a negative-PSRR test-circuit configuration. Pin 3 connects to the SR785 source-output port. Pin 1, which is V_{OUT} of the buffer amplifier, connects to the reference port of the SR785. Here, the first amp isolates the output port of the SR785 from the dc bias and provides the sinusoidal output. The second amplifier within the AD8034 sums the dc bias and sinusoid, which it uses to feed the DUT's (device under test's) negative-supply pin. The **figure** omits all bypass capacitors at the DUT's negative-supply pin. A 1-kΩ resistor from Pin 3 to ground prevents the noninverting input from

floating. The positive terminal of the external dc-power supply feeds Pin 6 through a 1-kΩ resistor. Connecting the DUT's output to Channel 2A of the SR785 completes the test-circuit configuration.

Building the buffer/inverting summer with an AD8034 dual amplifier is a good choice because it has a supply range of 5 to 24V; a signal-frequency response well beyond 1 MHz; and a large capacitive-load-drive capability, allowing you to neglect the capacitance of test cables. Further, the AD8034 can deliver as much as 40 mA of load current.

To instill confidence that this buffer/inverting-summer configuration works, **Figure 2** proves that you can neglect any loss that the AD8034 incurs. The **figure** demonstrates that the response of the AD8034 buffer/inverting summer of 10 Hz to 10 kHz is approximately flat with a loss of only 0.0025 dB, and the loss from 10 to 100 kHz is approximately 0.024 dB. **Figure 3** shows negative-PSRR test results. The Hewlett-Packard (www.hp.com) HP8753 provides the PSRR-versus-frequency responses beyond 100 kHz. You can measure positive PSRR (**figures 4** and **5**) by connecting Pin 3 to the SR785's output port. Pin 1, V_{OUT} of the buffer amplifier, connects to the reference port of the SR785. Here, you use the first amp to isolate the output

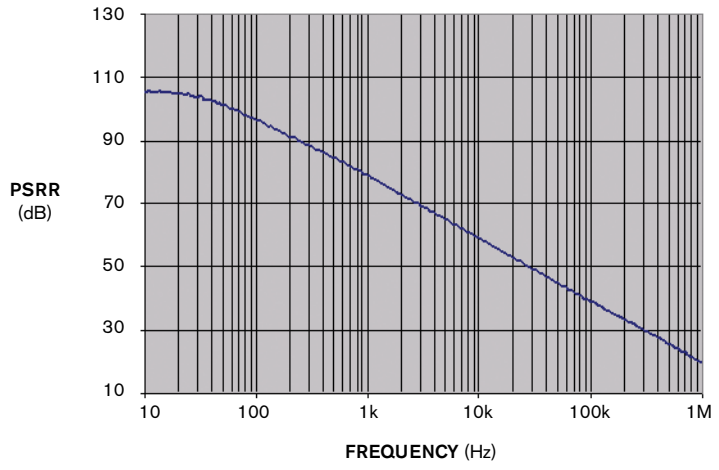

Figure 3 The negative-PSRR test results show responses beyond 100 kHz.

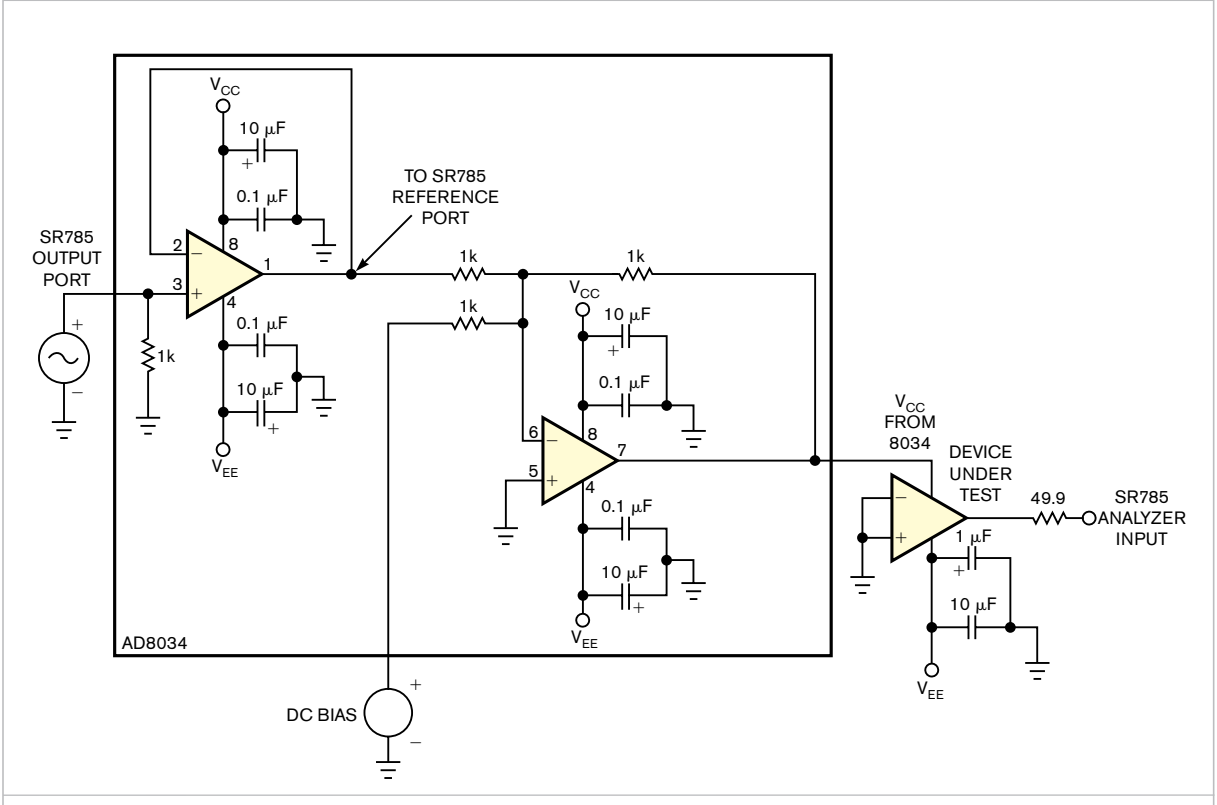

Figure 4 This test setup measures the positive PSRR. Note that bypass capacitors are absent from the device under test's positive-supply input.

port of the SR785 from the dc bias and provide the sinusoidal output. The second amplifier within the AD8034 sums the dc bias and sinusoid, which you use to feed the DUT's positive-supply pin. You must remove all bypass capacitors at the DUT's positive-supply pin. A 1-kΩ resistor from Pin 3 to ground prevents the noninverting input from floating. Feed the negative terminal of the external dc-power supply to Pin 6 through a 1-kΩ resistor. Connecting the DUT's output to Channel 2A of the SR785 completes the test-circuit configuration.

For the AD8034, assume that the DUT has a maximum supply voltage of ±15V, that you need to test negative PSRR, and that the DUT supplies ±10V. If you want to accommodate the maximum SR785 output of 5V peak, the first amplifier of the AD8034 needs enough head room to avoid clipping the ±5V signal from the output port of the SR785. In this case, a supply setting for the AD8034 of 6 and −16V is sufficient to prevent any problems.

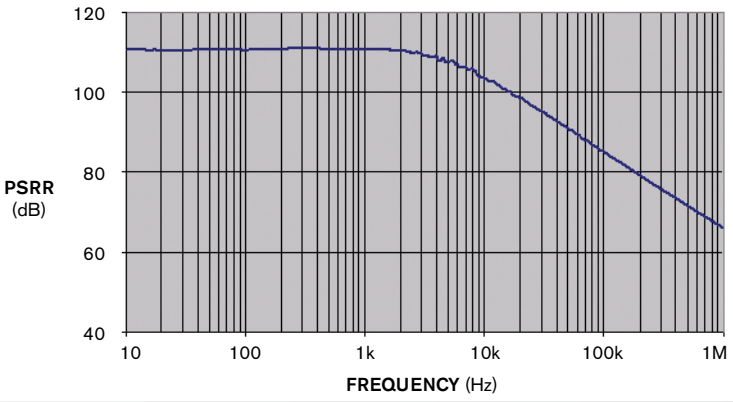

Figure 5 The positive-PSRR test results show responses beyond 100 dB.

This amount provides enough head room to accommodate the first amp of the AD8034, which handles a ±5V signal centered at ground. The −16V accommodates the dc bias of −10V and the ±5V signal centered at −10V at the output of the second amplifier of the AD8034. Positive PSRR is similar: Just set the AD8034 supplies to 16 and −6V for this example.

You might consider using separate power supplies for the DUT and the AD8034 to simplify matters. However, you can use the same dc-power supply for the DUT to provide the dc-bias voltage at Pin 6 of the AD8034 buffer/inverting summer. Choose the output voltage of the SR785 or whichever analyzer you use so that the DUT operates within its linear region of operation. You can apply this technique to other applications. EDN

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READERS SOLVE DESIGN PROBLEMS

Simple and effective inrush-current limiter stops surges

Gregory Mirsky, Juno Lighting Group, ModuLight Division,
Des Plaines, IL

Offline power supplies that drive loads of 200W and more require inrush-current limiters. Unrestricted inrush currents can reach hundreds of amperes, which may damage the line rectifier, open the fuse and input-filter inductors, and damage the PFC (power-factor-correction) filter capacitors. A simple method of limiting the inrush current uses an NTC (negative-thermal-coefficient) thermistor that connects in series with the supply line. When cold, the thermistor presents a high resistance, but its resistance decreases significantly as its temperature increases, limiting the inrush current by virtue of its thermal inertia and inability to quickly decrease its resistance.

However, an NTC thermistor also presents some resistance to the power supply's normal operating current. To keep the thermistor's normal resistance low, it should operate at a sustained and relatively high temperature, but this scenario may impair the power supply's temperature profile and raise the temperature in an enclosure in which power dissipation is already substantial.

This Design Idea offers an alternative circuit that effectively limits inrush current and does not add an extra source of heat to the power-supply package. Without increasing power losses during normal operation, a switchable series resistor in the power supply's dc section can efficiently limit inrush current until the PFC-rail electrolytic capacitors acquire a full charge. Then, an electromechanical or optically isolated semiconductor relay short-circuits the resistor.

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However, determining whether the PFC capacitors are fully charged presents a problem. Universal power-supply designs operate over a range of ac-input voltages, and determining the voltage that indicates a full charge can thus prove elusive. In addition, the inrush-current limiter should delay operation of any internal auxiliary power supplies and other power-consuming circuits to allow the PFC-rail capacitors to charge to their full predetermined extent.

The easiest method of solving these

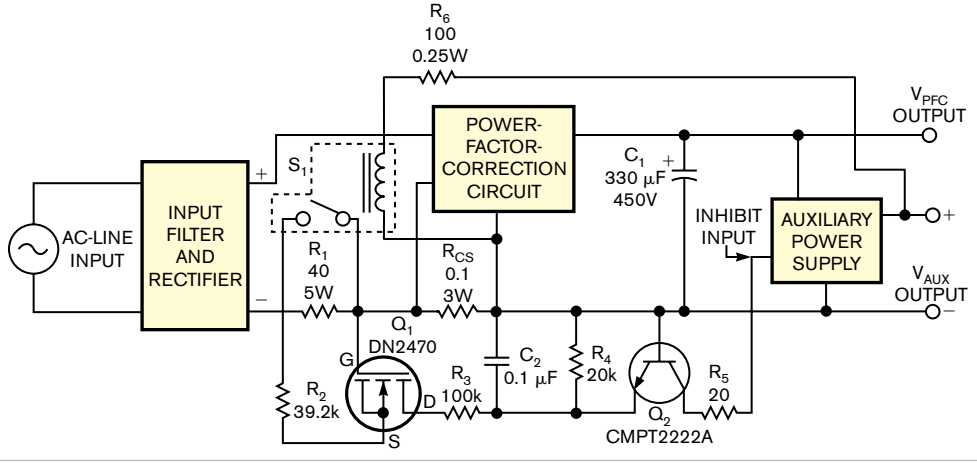


Figure 1 This inrush-current-limiter circuit features an electromechanical relay, S_1, and a current-limiting resistor, R_1. (Unless otherwise mentioned, all resistors in the schematic are rated for 0.125W.)

problems uses a circuit that measures the inrush current itself and not the voltage across the PFC capacitors. It determines the end of the inrush process by monitoring extinction of the inrush current's amplitude. Upon reaching a preset threshold, the circuit commands the start-up of auxiliary power supplies and other circuits. Monitoring the inrush current allows effective control of the power supply's starting point and renders the start-up threshold independent of the input-line voltage.

Figure 1 shows a practical version of a PFC circuit, which employs a switched-resistor inrush-current limiter. The inrush-current-sensing subcircuit comprises a wirewound resistor, R_1, and a parallel depletion-mode MOSFET, Q_1, which connects to resistor R_2 as a current source that drives resistors R_3 and R_4. Over a wide range of the voltage drop across R_1, from a few hundred volts to a few volts, this circuit generates a small constant current that suppresses operation of the auxiliary power supply and prevents interference with the inrush-current-limiting process.

When the inrush current decreases sufficiently, the voltage drop across R_1 becomes insufficient to keep Q_1 in operation as a current source. Q_1's current extinguishes, allowing the auxiliary power supply to turn on and start the power supply, by activating relay S_1, whose contacts short-circuit R_1. R_2's value determines the current necessary to hold the auxiliary power supply in a disabled mode, allowing PFC-rail capacitor C_1 to charge fully.

A 12V electromechanical relay, such as Omron's (www.omron.com) G2RL-1, provides low-resistance contacts to bypass R_1 (**Reference 1**). As an alternative, an optically isolated solid-state relay, such as the Carlo Gavazzi (www.gavazzionline.com) RP1A48D5, with a MOSFET or an SCR (silicon-controlled-rectifier) output device can replace S_1, provided that the voltage drop across the output device introduces no substantial power loss (**Reference 2**).

Figure 2 depicts the charging process's waveform as the voltage drop across R_1. The exponential envelope and its subcycles represent components of the inrush process; R_3 and C_2 filter out the subcycles and produce a decreasing exponential voltage waveform across R_4, holding Q_2 on for the duration of the inrush process. Q_2 suppresses the auxiliary power supply's operation by pulling its disable input low. At a few volts across R_1, Q_1 stops generating constant current and shuts down Q_2 to enable the auxiliary power supply. Thus, the entire power supply waits until the inrush current attains a safe value that R_2 sets. The power supply starts immediately after relay S_1 trips and shorts out inrush resistor R_1. The remainder of **Figure 1** comprises a conventional PFC but may also represent a part of any other power-supply configuration.

Trace 1 in **Figure 3** depicts the start-up of a 2.4-kW power supply with the inrush-current limiter and a slow-start

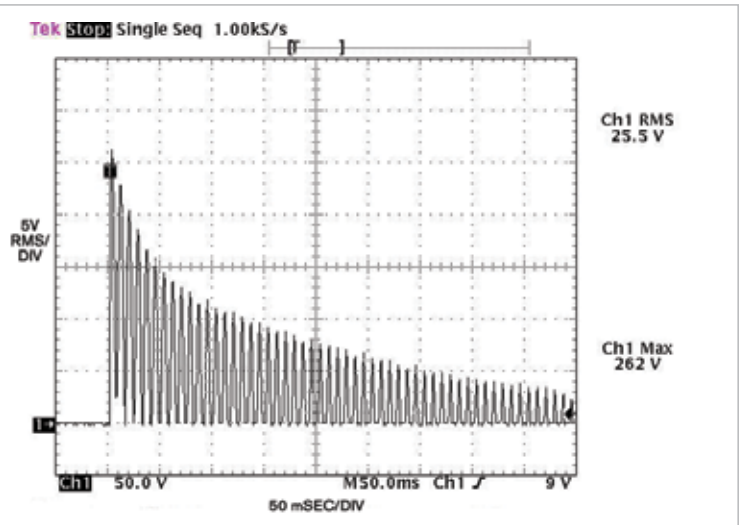


Figure 2 The voltage across the 40Ω current-limiting resistor, R_1, exhibits a classic exponential decay as the power-factor-correction capacitor approaches a full charge; the auxiliary power supply is deactivated for clarity.

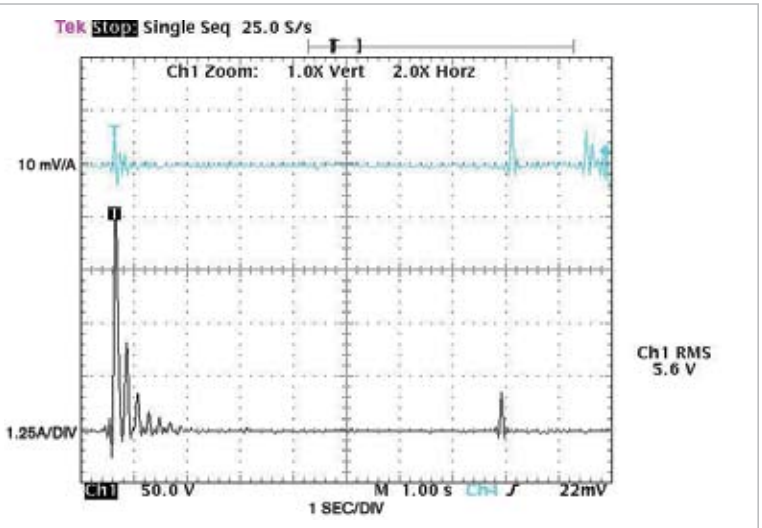


Figure 3 The upper trace shows the current as measured with a current probe. The lower trace depicts the voltage drop that the input current across resistor R_1 produces.

circuit, which allows the separation of the inrush and the start-up processes. The inrush-current value is 5A, a relatively low value for a 2.4-kW power level. Trace 4 shows the input current measured with a current probe. **Figure 4** depicts a 2400W power-supply start-up. Its inrush current is intentionally approximately 5A, which is far less than its operating current of approximately 14A. EDN

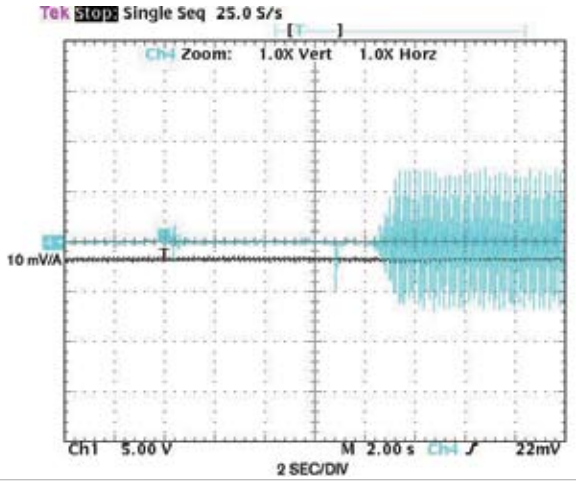


Figure 4 The input-current waveform shows the effects of the inrush-current limiter with the power supply driving a 2400W load.

REFERENCES

1 "PCB Relay, G2RL," Omron Corp, http://ecb.omron.com.sg/pdf/relay/power/G2RL.pdf.

2 "Solid State Relays PCB, 1-Phase ZS/IO Types RP1A, RP1B," Carlo Gavazzi, www.gavazzionline.com/pdf/rp1a48d5.pdf.

Inverting sample-and-hold amplifier requires no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Many applications require a sampling circuit whose output is inverted with regard to the respective sample of an input signal. A simple approach is a cascade of a common noninverting sample-and-hold amplifier and an inverting amplifier. A classic inverting amplifier is an op amp with voltage feedback from two resistors. The values of these resistors, which are usually equal, should be high enough to decrease the total power loss

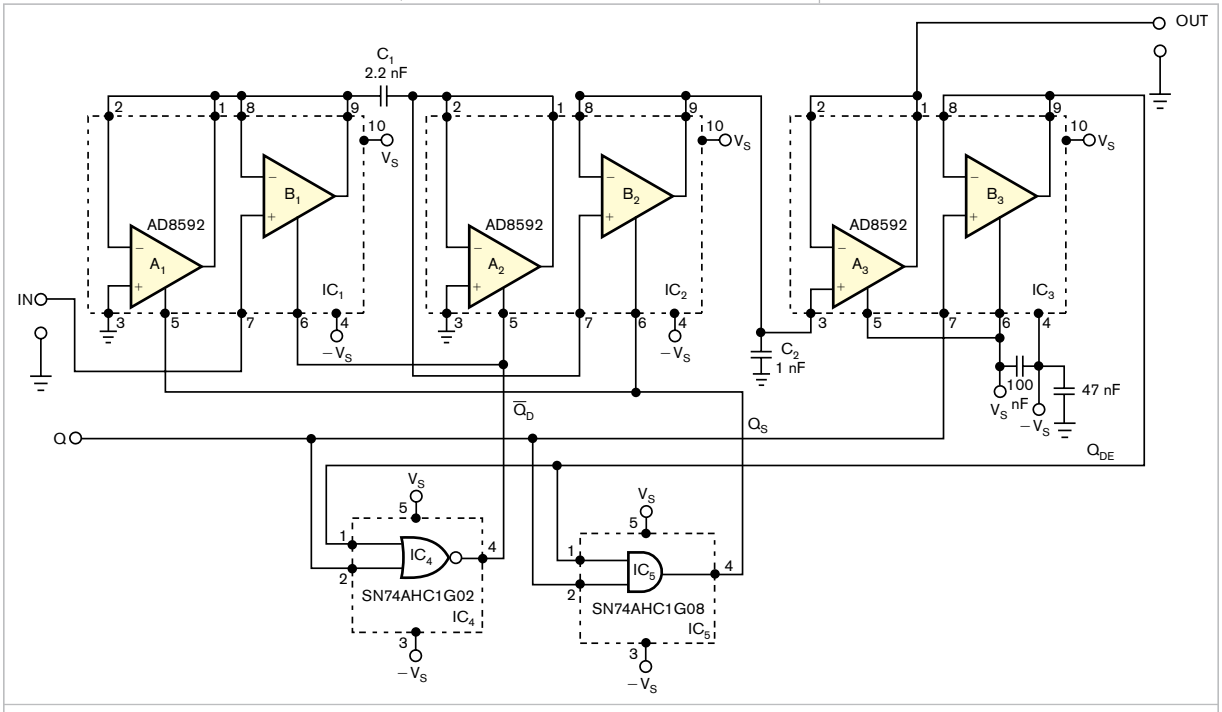


Figure 1 This sample-and-hold amplifier inverts the input signal by extension of its switched-mode circuitry.

of $P=2V^2/R$, which is proportional to the square of the output voltage. The values of these resistors should be as low as possible to preserve the bandwidth of the op amp.

Any parasitic capacitance (C_2 in the following **equation**) parallel to feedback resistor R_2 forms a pole in the transfer function of the inverter. This pole results in an additional breakdown of the gain-frequency characteristic of the inverting amplifier, with the value of breakdown frequency of $f_2=(1/2\pi)\times(1/R_2C_2)$. To retain the widest possible bandwidth, $f_2>f_T$, where f_T is the transition frequency of the op amp—in other words, the frequency at which the open-loop gain of the op amp drops to unity.

The Analog Devices' (www.analog.com) AD8592 dual op amps, which have a high-quality shutdown function, allow you to use a different approach (**Reference 1**). The inverting sample-and-hold circuit in **Figure 1** uses no external resistors. Thus, no power dissipates at external passive devices in the hold state of the circuit. All op amps act as voltage followers. In the hold state, followers B_1 and A_2 are enabled; thus, the B lead of the C_1 capacitor, Pin 1 of IC_2, is grounded through the output of A_2, and the input voltage, V_{IN}, gets followed at the A lead of the C_1, Pin 9 of IC_1. Upon the sampling command, Q is high, and, at this time, the A lead of C_1 gets grounded through the output of the A_1 follower. This scenario causes a negative voltage of $-V_S$ to appear at the input of the B_2 voltage follower, which in turn charges the C_2 capacitor to the voltage of $-V_S$ at the beginning of the sampling command. Voltage follower A_3 serves as an impedance converter.

THE OP AMPS' HIGH OUTPUT CURRENT OF 250 mA CONTRIBUTES FURTHER TO THE FAST CHARGING OF CAPACITORS C_1 AND C_2.

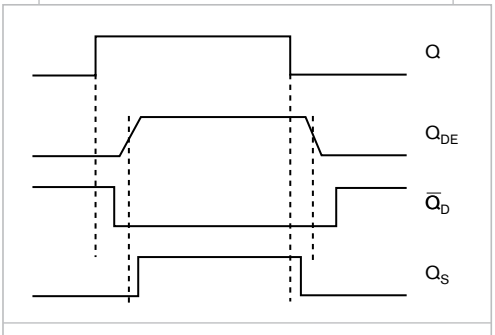


Figure 2 The external control-logic signal, Q, splits into two quasicomplementary signals to ensure the internal break-before-make operation of the sample-and-hold amplifier.

The AD8592's data sheet does not directly specify the leakage current at the output of the voltage follower; however, you can estimate it as being lower than 10 pA. Capacitors C_1 and C_2 thus can have unusually low values. On the other hand, the op amps' high output current of 250 mA contributes further to the fast charging of capacitors C_1 and C_2.

The B_3 voltage follower serves as a delay line, which, in conjunction with one AND gate and one NOR gate, generates two semicomplementary logic-control signals (**Figure 2**). Both of these signals, Q_S and $\overline{Q}_D$, are thus kept at an inactive low level for a sufficiently long time, before moving to an active high level, providing a break-before-make operation. The input voltage gets tracked at the C_1 capacitor with $\overline{Q}_D$ high, and the last value of this voltage, at the high-to-low transition of $\overline{Q}_D$, is a sample. The sample, at the instant of the low-to-high transition of Q_S, appears with a negative sign at capacitor C_2 and subsequently at the output. EDN

REFERENCE

1 AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ±250 mA Output Current and a Power-Saving Shutdown Mode, Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.

Single IC forms inexpensive inductance tester

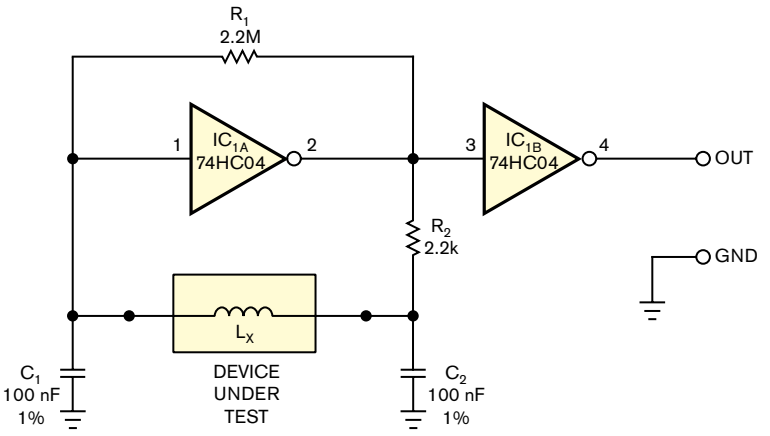
Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

This Design Idea shows how to build a reliable, low-cost, and simple inductance tester. The basis for the tester is a Pierce buffered CMOS oscillator (**Figure 1**). Instead of using the usual quartz crystal, you connect the inductor under test. This oscillator uses a single CMOS inverter biased through resistor R_1 in its linear region to form a high-gain inverting amplifier. Because of its high gain, the inverter dissipates lower power than an unbuffered gate; even a small signal drives the output high and low.

The LCπ network forms a parallel resonator that ideally resonates at the frequency $f_O=1/2\pi\sqrt{L_XC_S}$, which corresponds to a period, T_O, of $2\pi\sqrt{L_XC_S}$, where $C_S=C_1||C_2=50$ nF. So, you can calculate the inductance, L_X, by measuring the resonant frequency, f_O, or the period, T_O. At the resonant frequency, the LCπ network provides a 180° phase shift from input to output. To oscillate, the phase shift at frequency f_O around the oscillator loop must be 360°, and the gain of the oscillator loop must be greater than one. Inverter IC_{1A} provides an addi-

tional 180° phase shift from input to output and a high gain to compensate for the attenuation of the network.

Resistor R_1 is not critical, and its value can be 1 to 10 MΩ. Resistor R_2 isolates the output of gate IC_{1A} from the LCπ network so that you can obtain a nearly clean square wave from the output of the gate itself. In addition, R_2 improves frequency stability because it increases the slope of phase shift around the resonant frequency. For best performance, use film capacitors with low self-inductance, such as the MKP1837 polypropylene-film-capacitors series with 1% tolerance from Vishay (www.vishay.com). You can also use other film capacitors with standard tolerance provided that you select the value with a precision capacitance tester for best accuracy. The low supply current of the circuit allows you to use a battery as a power source. EDN



NOTES:
CONNECT IC_1'S UNUSED INPUTS TO GROUND OR V_{CC}.
CONNECT A 100-nF DECOUPLING CAPACITOR CLOSE TO THE POWER-SUPPLY PINS.
KEEP ALL COMPONENTS' LEADS SHORT.

Figure 1 Replacing a Pierce oscillator's crystal with an unknown inductance allows you to measure its value by observing the resulting oscillation's frequency.

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READERS SOLVE DESIGN PROBLEMS

Circuit compensates system offset of a load-cell-based balance

Luca Bruno, ITIS Hensemberger, Monza, Italy

It's a challenge to interface a resistive bridge sensor with an ADC receiving its power from a 5V single-supply power source. Some applications require output-voltage swings from 0V to a full-scale voltage, such as 4.096V, with excellent accuracy. With most single-supply instrumentation amplifiers, problems arise when the output signal approaches 0V, near the lower output-swing limit of a single-supply instrumentation amp. A good single-supply instrumentation amp may swing close to single-supply ground but does not reach ground even if it has a true rail-to-rail output.

In this application, the sensor is a precision load cell with a nominal load of 5 kg, or about 11 lbs, to weigh objects on an aluminum pan weighing approximately 150g, or approximately 5 oz. Because of the pan's weight, the instrumentation amplifier's output signal can never go down to 0V, even if there are no objects to weigh. Now, the problem arises of how to compensate the instrumentation amp's output-offset voltage and the voltage that the pan itself produces.

A software approach is the simplest way to compensate the system offset. During power-up, there are no objects to weigh on the pan, and the system can thus acquire the offset voltage and hold the data in the microcontroller's memory, subsequently subtracting it from the data it acquired when there was an object to weigh. This approach, however, does not reach the 5-kg full-scale of the balance, reaching only 5−0.15 kg, or 4.85 kg.

This Design Idea shows how to achieve hardware compensation us-

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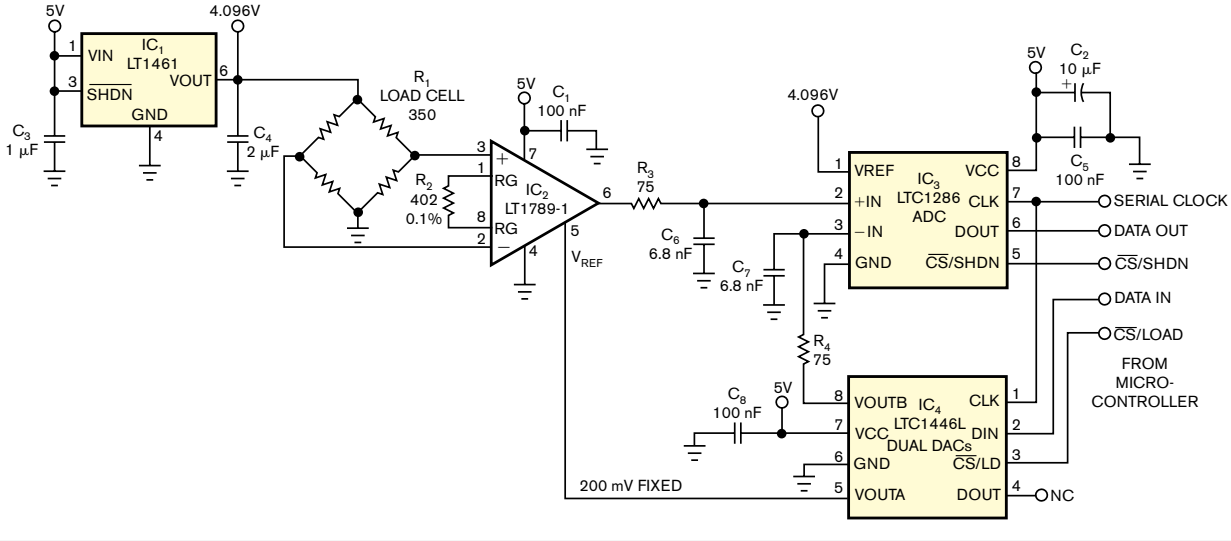

Figure 1 The serial dual DAC in this circuit gets an offset voltage from the microprocessor (not shown) during a power-on-calibration routine.

ing a microcontroller that, on power-up, starts a software routine to reset the system offset. The solution is a simple circuit based on four ICs from Linear Technology (www.linear.com) in **Figure 1**. A precision voltage reference, IC_1, has a high minimum output current of 50 mA. It provides an output voltage of 4.096V to power the load cell and to set the full-scale of the 12-bit ADC, IC_3. The highly accurate LT1789-1 instrumentation amplifier, IC_2, features maximum input-offset voltage of 150 µV over the temperature range of 0 to 70°C and maximum input-drift-offset voltage of 0.5 µV/°C over the temperature range of 0 to 70°C with rail-to-rail output that swings within 110 mV of ground. You set the gain through precision resistor R_2 to a nominal value of 500Ω to give an output span of 4.096V when the load is 5 kg and its maximum input signal is $V_{CC}\times S=4.096V\times 2$ mV/V=8.192 mV, where S is the sensor's sensitivity.

The output of DAC_A of dual-DAC IC_4 provides a reference voltage of 200 mV at the reference pin of the instrumentation amp to avoid saturation near ground of the amplifier itself, where its transfer characteristic is not quite linear. The amplifier's total worst-case output offset is: $V_{REF}+V_{PAN}\pm V_{OFFSET}=200$ mV+125 mV±500×150 µV=325 mV±75 mV=250 mV/400 mV, where V_{PAN}=125 mV and is the voltage that the pan's weight produces.

The system-output offset is thus 250 to 400 mV. On power-up, the microcontroller starts a routine that sets the output of the DAC_A equal to 200 mV, while it increases the output of the DAC_B of dual-DAC IC_4 until it is equal to the system offset on Pin 2 of ADC IC_3, and the result of the conversion is 000h. This result is possible because IC_4 contains two 12-bit DACs with the same full-scale voltage of 2.5V, making 1 LSB equal to 0.61 mV, which is smaller than IC_3's resolution of 1 mV. This figure corresponds to the resolution of the balance: 5000g/4096=1.22g. The maximum output voltage of the instrumentation amp with a maximum load of 5 kg is $4.096V+V_{OUT\_TOTAL\_OFFSET\_INA}=$ 4.346V/4.496V, which is less than the minimum worst case over temperature of 4.62V high saturation.

IC_3 has a single unipolar differential input, so you can subtract from the +IN input voltage a constant voltage of value equal to the system offset that that DAC_B of IC_4 provides. During the first one and a half clock cycles, the ADC samples and holds the positive input. At the end of this phase, or acquisition time, the input capacitor switches to the negative input, and the conversion starts. The RC-input filters on the inputs of IC_3 have a time constant of 0.5 µsec to permit the negative and positive input voltages to settle to a 12-bit accuracy during the first clock cycle of the conversion time, using the maximum clock frequency, which is 200 kHz. If you want to increase the time constant, then you must use a lower clock frequency.

Furthermore, the DAC and ADC have a three-wire serial interface that easily permits transferring data to a wide range of microcontrollers with a maximum sampling rate of 12.5k samples/sec. When the ADC performs no conversions, it automatically powers down to 1 nA of supply current, and, if the microcontroller shuts down IC_1 through its Pin 3, the circuit draws a worst-case supply current of just 1 mA, because all the ICs are micropower. EDN

Voltage doubler uses inherent features of push-pull dc/dc converter

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This Design Idea presents a minimal-parts-count, wide-range voltage doubler using the inherent voltage-doubling characteristics of a one-transformer push-pull dc/dc converter. The implementation uses a high-voltage Darlington-array driver, ULN2023A. The circuit exhibits a wide input-voltage range of 5 to 30V and provides a typical power output of 1 to 4W at moderate efficiency.

Figure 1 shows a simple, one-transformer dc/dc converter in which cross-coupled RC networks from the collectors of Q_1 and Q_2 to the corresponding bases provide regenerative feedback. In operation, the transformer alternates between positive and negative saturation, with collapse in transformer flux leading induced voltages to drive the transistors alternately off and on. The input-voltage and saturation charac-

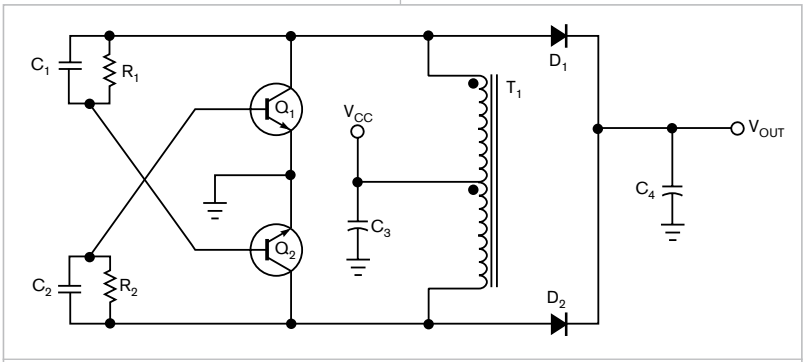

Figure 1 A simple one-transformer dc/dc voltage doubler has cross-coupled RC networks from the collectors of Q_1 and Q_2 to the corresponding bases. These networks provide regenerative feedback.

TABLE 1 EXPERIMENTAL RESULTS

Input voltage (V)	Input current (mA)	Oscillating frequency (kHz)	Output voltage (V)	Load current (mA)	Power input (W)	Power output (W)	Efficiency (%)
5	245	1.79	7.59	105.95	1.22	0.8	65.77
10	250	4	17.68	104.13	2.5	1.84	73.72
15	274	6.06	27.7	111.7	4.12	3.09	75.08
20	280	8.2	37.9	110.12	5.6	4.17	74.53
25	242	10.53	48.1	88.23	6.05	4.24	70.15
30	205	13.33	58.7	66.25	6.15	3.89	63.23

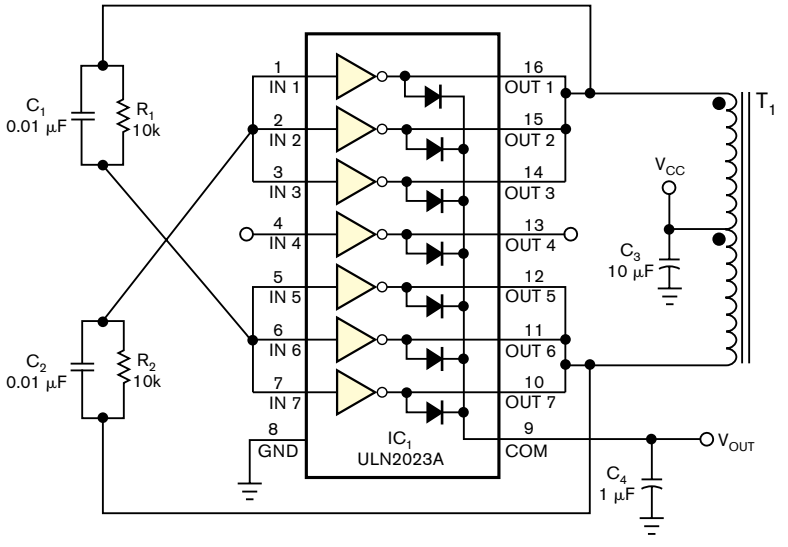

Figure 3 Taking advantage of the multiple drivers in one package, three drivers are parallel in each leg of the circuit.

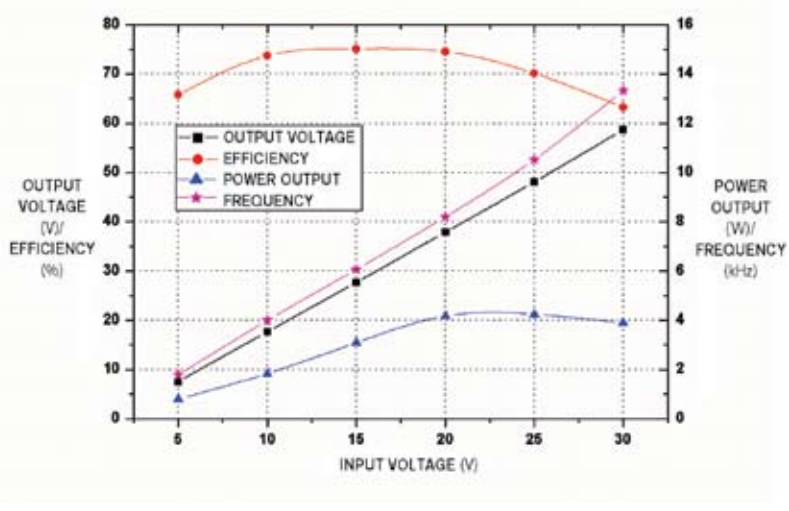

Figure 4 Experimental results show the circuit in Figure 3 operating as a low-power, moderately efficient, wide-range voltage doubler.

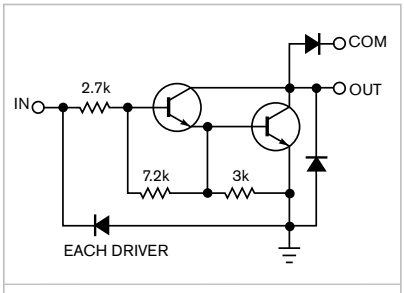

Figure 2 The internal configuration of the high-voltage Darlington-array ULN2023A driver exactly matches the requirements of the circuit in Figure 1 by providing rectifier diodes at the collector outputs.

teristics of the transformer core determine the operating frequency based on the relationship

$$f = \frac{V_{CC} \times 10^8}{4\beta_S AN} \text{Hz},$$

where V_{CC} is the input voltage, β_S is the saturated flux density in gauss, A is the cross-section area of the core in square centimeters, and N is the number of turns in half of the primary. The circuit uses the property that the collector-to-emitter voltage of each device is approximately twice the supply voltage, V_{CC}, plus induced voltages, which occur because of leakage inductance. Rectification and filtration of the collector voltages of Q_1 and Q_2 through D_1 and D_2 directly provide an output voltage that is approximately double the input voltage, V_{CC}.

The internal schematic of the high-voltage Darlington-array ULN2023A driver in **Figure 2** exactly matches the requirements for the circuit in **Figure 1** by providing rectifier diodes at the collector outputs. The voltage-breakdown specification of 95V meets the maximum requirement of twice V_{CC} plus transients when operating at an input of 30V. The device exhibits a low collector-to-emitter saturation voltage at the desired current level of approximately 100 mA and low switching times when switching at rates as high as tens of kilohertz.

Figure 3 shows the final circuit configuration. Three drivers operate in parallel, sharing the drive current, minimizing the collector-to-emitter

voltage, and maximizing the permitted power dissipation. **Table 1** shows the experimental results with the voltage-doubler circuit operating over the input voltage of 5 to 30V. In that range, the input current is less than 300 mA to remain within the current values of the transformer at lower input voltages and within the power-dissipation limit of the ULN2023A at higher input voltages. **Figure 4** shows the plot of the experimental results, clearly indicating the operation of a low-power, moderately efficient, wide-range voltage doubler.EDN

Voltage timer monitors line-connected ac loads

Michael Petersen, Maxim Integrated Products, Sunnyvale, CA

A simple circuit monitors the elapsed time over which a line-connected ac load energizes (**Figure 1**). You can then access the elapsed-time count over a standard one-wire protocol. When you energize the ac load, the optoisolator provides pulses at the ac-line frequency to the input of the one-wire counter, a DS2423 IC. Thus, the counter continuously increments whenever you energize the load. Resistors R_1 and R_2 limit the current, and diode D_1 protects the optoisolator from reverse-polarity voltages during the negative half of the line cycle.

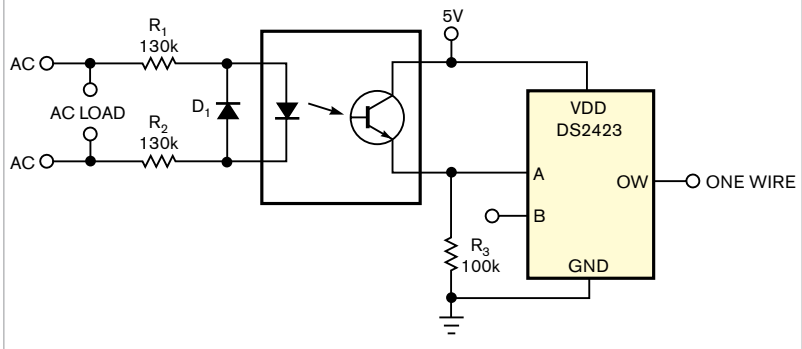

Figure 1 This circuit monitors line-connected ac loads by counting one pulse per cycle when the load is energized.

As an example, the circuit can monitor the duration of operating intervals for a 240V-ac well pump, thereby giving an indirect measure of the amount of water the well pumps and the approximate amount of power it consumes. The one-wire master counter—a Linux-based PC, for example—reads the elapsed count once per minute. Any change in the count from one reading to the next indicates that the pump is energized and running, and you calculate the length of time in seconds by simply taking the difference in counter values divided by the line frequency—60 Hz, in this case. The time in seconds equals the new count minus the old count divided by 60 Hz.

The circuit can monitor a water heater, a furnace, an air-conditioning unit, or any other ac-connected load. You may need to adjust the R_1 and R_2 values to accommodate line voltages other than 240V ac or the characteristics of other optoisolators. You can also monitor two independent loads by attaching a second optoisolator circuit to the Counter B input of a single DS2423.EDN

Cascaded converter boosts LED-drive capability

Grant Smith, National Semiconductor, Phoenix, AZ

Powering 20 to 30 white LEDs from three alkaline cells presents an interesting problem for the conventional boost converter. The required boost ratio and duty factor are simply impractical. If you are determined to design with off-the-shelf components, cascading two stages of boost can yield reasonable results. This topology has been around for decades, but engineers often perceive it as too complicated. There are, however, certain inherent advantages in this approach's component requirements. The first-stage switch need not tolerate the total output voltage of the second switch, and the second switch does not have the current requirements of the first. If the duty factor were not a concern, the current/voltage requirements of a single-stage boost would require a larger, more expensive switch that might easily approach the cost of both switches in the cascaded boost. You can also realize similar advantages of the inductors, rectifiers, and filter capacitors.

This Design Idea powers 24 white or ultraviolet LEDs in series at approximately 20 mA. At a nominal 4.5V-dc input, the measured efficiency is 84.2%. This figure is reasonable for a 2 to 2.5W converter. At a 3V-dc input, the overall boost ratio for a noncascaded converter is potentially more than 30-to-1, requiring an on-time duty factor of approximately 97%. In a cascaded boost converter, this duty factor is a function of the square root of the total boost ratio. This ratio equates to

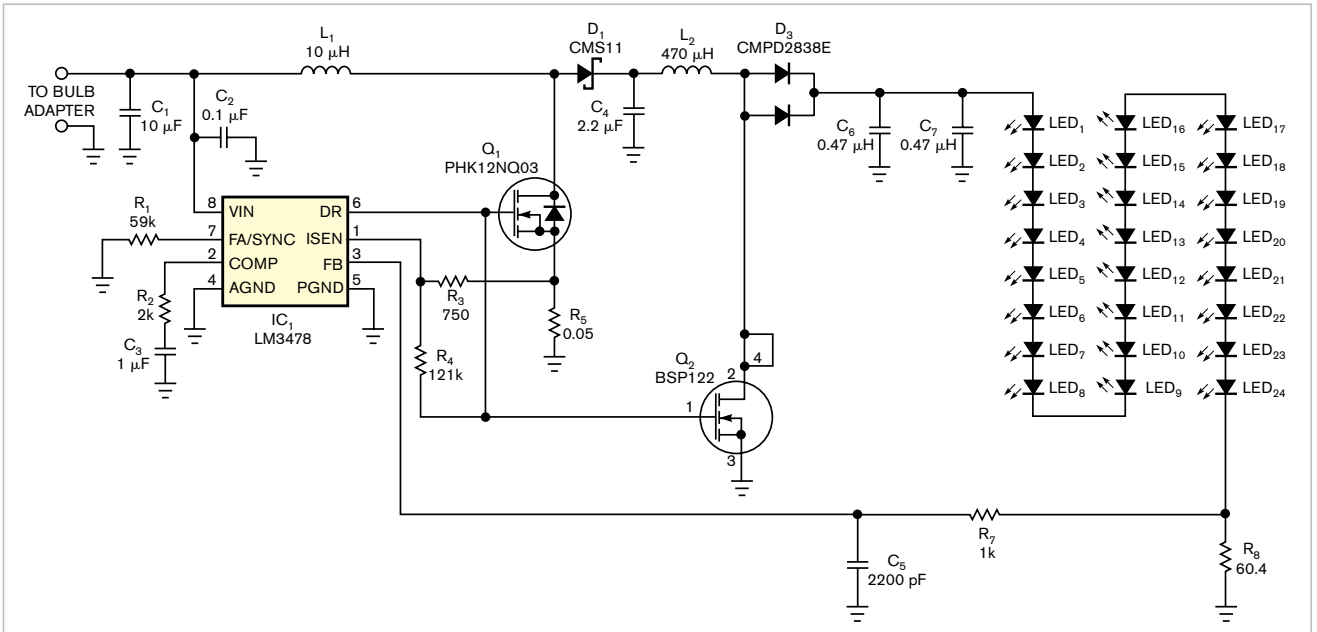

Figure 1 Comprising off-the-shelf components, this circuit cascades two stages of boost to drive a string of 20 to 30 LEDs.

a maximum of about 82% just before the occurrence of undervoltage shutdown. At a normal 4.5V-dc input, the duty factor should be slightly more than 77%.

The circuit in **Figure 1** implements a cascaded boost converter, which takes the place of the lens assembly in a popular heavy-duty flashlight. It includes 24 white or ultraviolet LEDs on one side of the circular PCB (printed-circuit board) and the active circuitry on the other. You can substitute red LEDs for three or four of the ultraviolet LEDs to offer an appropriate visible backlight. Although you may prefer to use a single high-powered white LED, high-powered ultraviolet LEDs appear to be unobtainable. This project uses 20 inexpensive LEDs offering 400 mW of optical power for 1.52W input at a more useful 30° viewing angle. Its directional nature also helps prevent accidental eye damage. Ultraviolet-light sources find use in many applications, including gem inspection, currency inspection, and scorpion detection.

The PWM controller, IC_1, an LM3478, operates at voltages as low as 3V dc, eliminating the need for a charge pump. The transistors are rated for less than 3V gate drive. IC_1 simultaneously drives Q_1 and Q_2. The circuit requires only one controller and uses off-the-shelf inductors. The first-stage inductor and filter capacitor can produce substantial ripple without adversely affecting the final output ripple. The first rectifier is an inexpensive, 40V Schottky unit, and the second is a simple signal diode rated for 120V.

IC_1 operates at a switching frequency of approximately 300 kHz, which R_1 sets. The design uses a current-mode-control scheme with slope compensation. A signal from current-sense resistor R_5 modulates slope compensation through R_3. In this case, the value of R_5 is small for enhanced efficiency. R_4 sums the signal with the gate-drive output to increase its apparent amplitude by the current-sense input at Pin 1. R_2 and C_3 are the usual compensation components. In this case, the response time of the converter is unimportant, so it is easy to choose the components.

It is easy to overlook the cascaded boost converter without sufficiently analyzing it. Mass-produced components that suit their function afford a more cost-effective and simple approach than you might realize at first. An integrated flyback regulator can easily require many components to provide this kind of solution without any real advantage. It is also likely to require custom magnetics. EDN

Dual transistor improves current-sense circuit

Robert Zawislak, PE, Consultant, Palatine, IL

In multiple-output power supplies in which a single supply powers circuitry of vastly different current draws, two perplexing steps are sensing the current that each output draws and deactivating the power supply in the event of an overload on that output. These issues are especially important in protecting the fragile PCB (printed-circuit-board) traces in low-level circuits. A typical circuit would use the base-emitter threshold volt-

age of approximately 0.6V of a bipolar transistor to trigger the power-supply-protection circuits. Although economical, the transistor's threshold varies excessively over temperature; hence, the protection level is unstable.

The circuit in **Figure 1** essentially eliminates the base-emitter-voltage temperature-variation problem as the derivation of the output voltage and as a function of the load current. By using dual bipolar devices in one case, the manufacturer nearly perfectly matches the two devices. Although this Design Idea describes a positive power supply, you can realize a similar negative-output-supply current-sense circuit using a dual NPN transistor in place of the dual PNP that the **figure** shows.

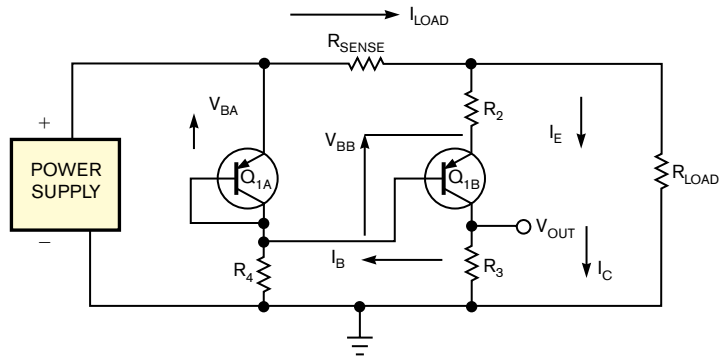

Figure 1 This simple two-transistor circuit provides a voltage output proportional to the current through sense resistor R_{SENSE}.

The following **equations** show the derivation of the output voltage as a function of the load current (referring to **Figure 1**):

$$V_{BA}+(I_{LOAD}\times R_{SENSE})+(I_E\times R_2)-V_{BB}=0.$$

$$[(V_{BA}-V_{BB})+(I_{LOAD}\times R_{SENSE})]-I_E R_2=0.$$

$$I_C+I_B=I_E.$$

$$(V_{BA}-V_{BB})+(I_{LOAD}\times R_{SENSE})-(I_C+I_B)R_2=0.$$

$$I_B=I_C/\beta.$$

$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-(I_C+I_C/\beta)R_2=0.$$

$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-[I_C\times(\beta+1)/\beta]R_2=0.$$

$$V_{OUT}=I_C R_3.$$

$$I_C=V_{OUT}/R_3.$$

$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-(V_{OUT}/R_3)(\beta+1/\beta)R_2=0.$$

If $V_{BA}=V_{BB}$, then $V_{BA}-V_{BB}=0$, and

$$I_{LOAD}\times R_{SENSE}-(V_{OUT}/R_3)(\beta+1/\beta)R_2=0.$$

$$V_{OUT}=I_{LOAD}\times R_{SENSE}[R_3/(\beta+1)](\beta/R_2).$$

If β is high, then $\beta/(\beta+1)\beta)\approx 1$, and

$$V_{OUT}=(I_{LOAD}\times R_{SENSE}\times R_3)/R_2.$$ EDN

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READERS SOLVE DESIGN PROBLEMS

Nonvolatile digital potentiometer gates logic signal

Reinhardt Wagner, Maxim Integrated Products, Ottobrunn, Germany

This Design Idea describes a simple alternative to a nonvolatile gating function you typically implement using PAL (programmable-array logic), GAL (gate-array logic), or a CPLD (complex-programmable-logic device). To gate a logic signal to block or transmit it, you usually employ a logic gate, such as an AND gate, and use the gate's second input to define whether the gate blocks or transmits the applied signal. Because logic gates perform immediate Boolean operations, their operations are combinational and without memory.

However, if you must program a gate that should always either block or transmit the signal after system start-up, you must store the "transmit/block" logic state in some form of nonvolatile memory. Two basic methods are available for storing such logic states. The first involves using a microcontroller in combination with nonvolatile memory, such as EEPROM. This method is suitable if the system can wait until the microcontroller reads the logic state from memory and applies it to a hardware pin—typically, through a general-purpose I/O pin. Some systems, however, require that the transmit/block signal be present at start-up. For those systems, the read delay from memory is unacceptable.

A second method, which is useful for systems without a microcontroller or that cannot wait for the microcontroller to read from memory at boot time, stores the logic state in a device that makes it immediately available at power-up. For this purpose, PAL devices, GAL devices, and CPLDs implement the gating function in combination with programmable nonvolatile memory. These devices offer more than gating with memory, however, and may be overspecified for systems that need only a few such gates. Also, their packages are relatively large to accommodate the many logic-I/O pins they offer.

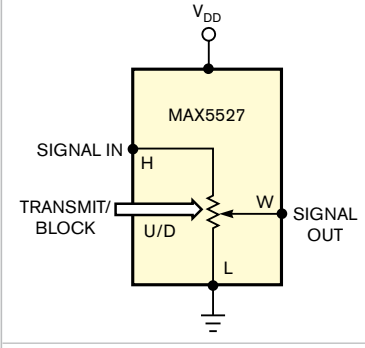

Figure 1 A programmable, nonvolatile digital potentiometer functions as a simple AND gate. Setting the wiper to the device's highest value allows the input signal to propagate to the output; setting the wiper to the lowest value blocks the input signal.

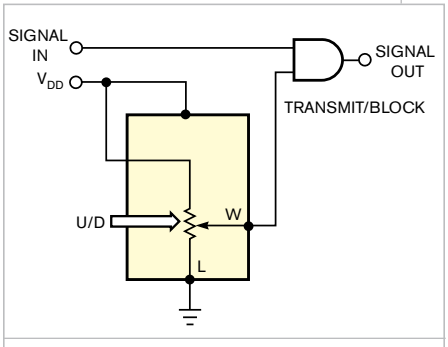

Figure 2 If the bandwidth of the digital potentiometer is too low, you can use the device to drive an AND gate.

If you need only a few nonvolatile gates, consider using a component common in analog- and mixed-signal systems: the digital potentiometer (**Figure 1**). Ground the L end of the resistor string and route the signal into the H end of the string. Then, the wiper output either shorts to ground for blocking or connects to the input signal for transmission.

You can program the digital potentiometer through its serial interface during board or system test. The up/down interface on some digital potentiometers is suitable for that purpose. When selecting a nonvolatile digital potentiometer, you should consider the following criteria:

- Digital potentiometers typically have 32 or more taps; you need at least two. A digital-poten-

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tiometer wiper has a resistance associated with the internal switches and should be as small as possible to avoid distorting the switching signal. A typical wiper resistance is 100Ω to 1 kΩ. For the MAX5527 from Maxim (www.maxim-ic.com), wiper resistance measures 90Ω.

- Because the resistance of a digital-potentiometer wiper decreases with increasing supply voltage, you should select a high supply voltage.
- To minimize loading on the signal source and not limit the potentiometer's signal bandwidth, you should select a device with a high end-to-end resistance; 100 kΩ is acceptable for many applications.
- Select a nonvolatile digital potentiometer if you must program the gate's state in nonvolatile memory. Some digital potentiometers are OTP (one-time-programmable); this feature allows you to save the wiper's setting. Using the OTP feature is suitable when you don't expect to make changes in the gating function. The number of gates for which the state must be stored determines the number of potentiometers you need. They are available in arrays of one to six or more per package.

The digital potentiometer's bandwidth determines the maximum data rate for signals transmitted through the potentiometer. If the switching rate of these applied logic signals is too high for the available potentiometers, you can use a conventional, high-speed logic gate with a digital potentiometer controlling the transmit/block input (**Figure 2**).EDN

Soft-limiter circuit forms basis of simple AM modulator

Herminio Martínez, Encarna García, and Juan Gámiz,
Technical University of Catalonia, Barcelona, Spain

One of the most popular circuits for amplitude control in oscillators is the soft-limiter circuit (**Figure 1a**). When the output voltage, $V_{OUT}(t)$, is small, diodes D_1 and D_2 are off. Thus, all of the input current, $V_{IN}(t)/R_1$, flows through the feedback resistor, R_2, and the output voltage is:

$$V_{OUT}(t) = -\frac{R_2}{R_1} V_{IN}(t).$$

This portion is the linear part of the limiter-transfer characteristic in **Figure 1b** with slope of $-(R_2/R_1)$.

On the other hand, when $V_{OUT}(t)$ goes positive, V_A becomes more positive, thus keeping D_1 off; however, V_B becomes less negative. Then, if you continue to decrease $V_{IN}(t)$, you will reach a positive value of the output voltage, at which V_B becomes approximately 0.7V, and diode D_2 conducts.

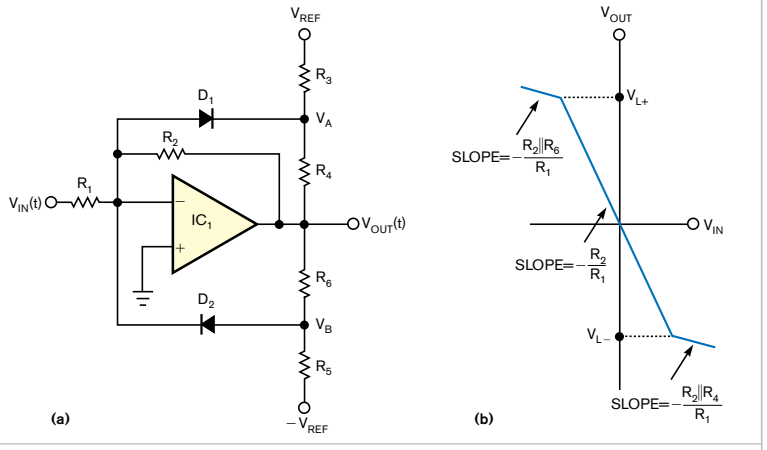


Figure 1 Diodes in the feedback circuit form the basis of this soft limiter (a). The transfer characteristic of the limiter circuit shows inflection points when the diodes begin to conduct (b).

Thus, the positive-limiting value at the output, V_{L+}, is:

$$V_{L+} = \frac{R_6}{R_5} V_{REF} + \left(1 + \frac{R_6}{R_5}\right) V_\gamma,$$

where V_γ is the forward voltage of the diodes—approximately 0.7V. If $V_{IN}(t)$ decreases beyond this value, $V_{OUT}(t)$ will increase, more current is injected into diode D_2, and V_B remains at approximately $-V_\gamma$. Thus, the current through R_5 remains constant, and the additional diode current flows through R_6. Therefore, R_6 appears, in effect, in parallel with feedback resistor R_2, and the incremental gain, A_V, ignoring the diode's resistance, in the positive-limiting region is:

$$A_V = -\frac{R_2 \| R_6}{R_1}.$$

Note that, to make the slope of the transfer characteristic small in the limiting region, you should select a low value for R_6. You can derive the transfer characteristic for positive $V_{IN}(t)$ or negative $V_{OUT}(t)$ in a manner identical to that of the above description. You can easily see that, for a positive $V_{IN}(t)$, diode D_1 plays an identical role to the one that diode D_2 plays for negative $V_{IN}(t)$. So, the negative-limiting level, V_{L-}, is:

$$V_{L-} = -\left[\frac{R_4}{R_3} V_{REF} + \left(1 + \frac{R_4}{R_3}\right) V_\gamma\right],$$

and the slope of the transfer characteristic in the negative-limiting region is:

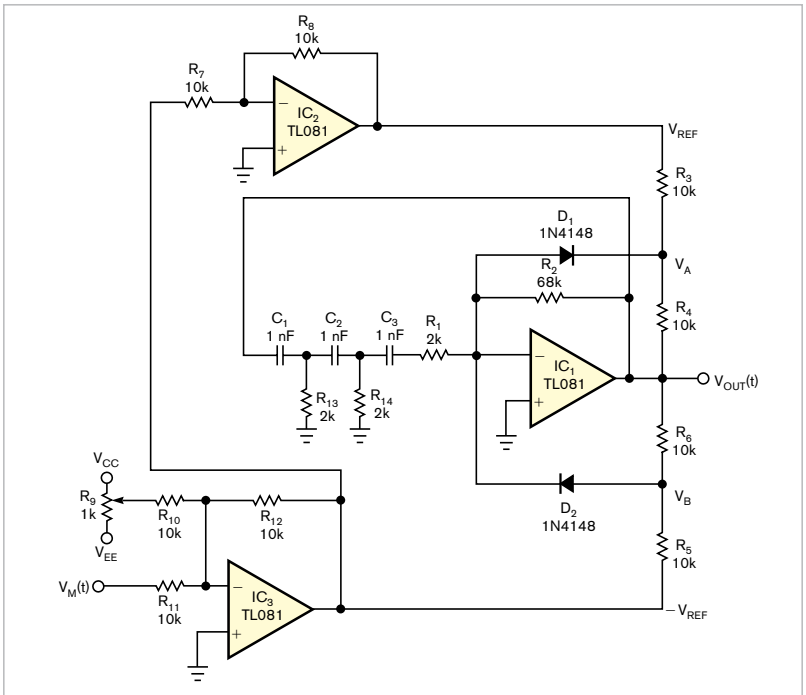


Figure 2 Inserting the soft limiter into the feedback loop of a phase-shift oscillator enables a simple AM modulator.

$$A_V = -\frac{R_2 \| R_4}{R_1}.$$

Note that increasing R_2 results in a higher gain in the linear region and keeps V_{L+} and V_{L-} unchanged. When you remove R_2, the soft limiter turns into a comparator.

Thus, the circuit of **Figure 1a** functions as a soft limiter, and you can independently adjust the limiting levels V_{L+} and V_{L-} by selecting the appropriate resistor values and reference voltages, $\pm V_{REF}$. Therefore, you can use a control voltage to change these limiting levels. You can base a simple AM modulator on this configuration. The RC (resistance/capacitance) phase-shift oscillator in **Figure 2** includes a soft limiter in its voltage amplifier. You can alternatively use any similar RC or LC (inductance/capacitance) oscillator. You can modify the reference voltages, V_{REF} and $-V_{REF}$, with the input modulating voltage, $V_M(t)$. This voltage dynamically adjusts the saturation levels of the oscillator's output. The ratio of the limiter resistors determines the output amplitude and the modulation index.

Figure 3 shows the waveforms of the modulating input, $V_M(t)$, and the oscillator's modulated output, $V_{OUT}(t)$, with the component values of **Figure 2**. In this case, $V_M(t)$ is a sinusoidal waveform with an amplitude equal to 3V, and trimmer R_9 adds a 5V offset voltage. The circuit works in a similar way to a four-quadrant analog multiplier. EDN

REFERENCE

1 Sedra, Adel S, and Kenneth C Smith, *Microelectronic Circuits: Fourth Edition*, ISBN 0-19-511663-1, 1998, Oxford University Press, New York.

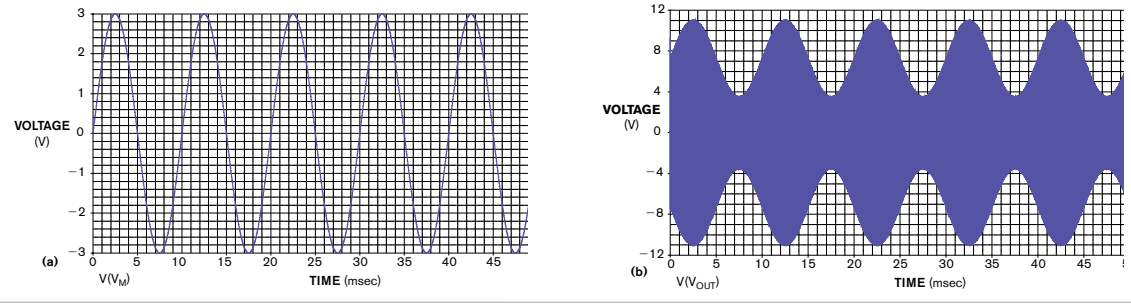
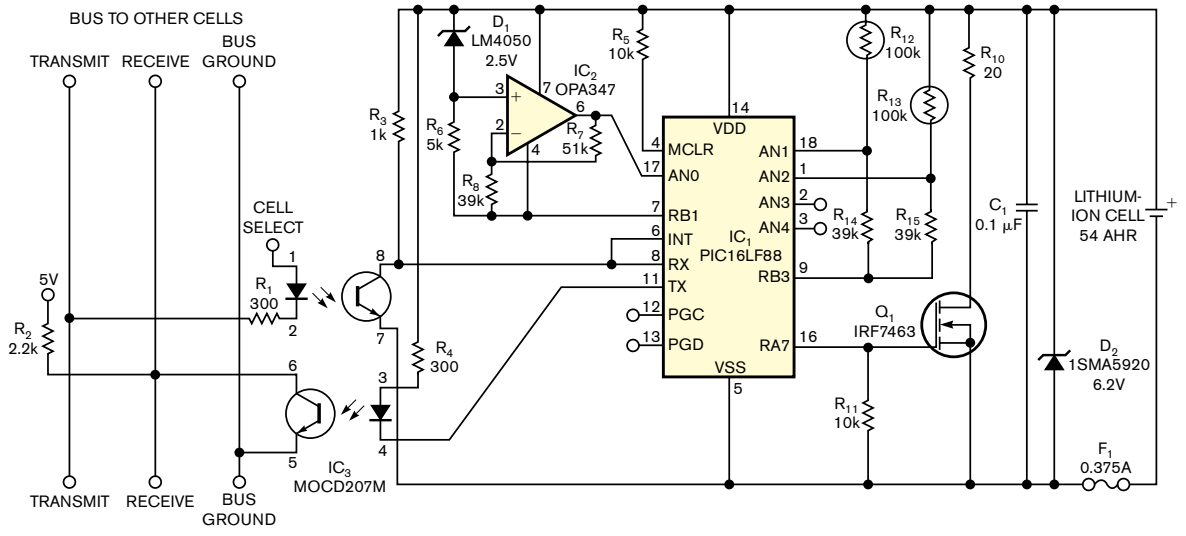


Figure 3 The modulating input, $V_M(t)$ to the circuit in Figure 2 (a) obtains the modulated output voltage, $V_{OUT}(t)$ (b).

Circuits monitor and balance large lithium-ion batteries

Daniel Gomez-Ibanez, Woods Hole Oceanographic Institution, Woods Hole, MA

When using rechargeable lithium-ion cells in large batteries, such as those in an electric vehicle, you encounter unique problems. Bus voltages greater than 100V preclude the use of a standard IC for overcharge and overdischarge protection. In addition, because many cells connect in series, small differences in cells' self-discharge rates eventually lead to unequal levels of charge. Therefore, you must correct the cell balance. This Design Idea provides one strategy for protecting and balancing large, high-voltage batteries. The circuit in **Figure 1** monitors



NOTE: R_{12} AND R_{13} ARE VISHAY 232264066104 THERMISTORS.

Figure 1 A microcontroller connects directly to a lithium-ion cell and a battery string to monitor the cell's voltage and temperature. This process shunts current through R_{10} under program control to equalize the cell's self-discharge. Each cell in the battery gets its own monitor. The monitors communicate with a controller through optoisolators.

the voltage of a single lithium-ion cell that connects in series in a battery. The circuit communicates with a supervisor processor. The supervisor monitors all cells in the battery, opens a protection switch in case of a problem, and determines where and when balancing is necessary. This approach easily scales to an arbitrarily high bus voltage.

A PIC16LF88 microcontroller gets power directly from the cell voltage, which ranges from 3 to 4.2V. With no need for voltage regulation, the quiescent current of the entire circuit is less than 1 µA, minimizing self-discharge of the battery. Fuse F_1 and zener D_2 protect the monitor from high voltage in the unlikely event that the cell becomes disconnected from the battery. An optocoupler connects between the cell monitor and an asynchronous serial bus, running at 9600 baud. A cell-select line, driven by the supervisor, selects one cell at a time. The MOCD207M optocoupler has a tightly toleranced current-transfer ratio, so it operates predictably over the possible range of supply voltages. Although the quiescent current of this isolator is near zero, the supervisor can wake up the monitor from sleep at any time by sending a pulse over the serial line.

The monitor measures cell voltage by measuring the fixed voltage of the LM4050 with respect to the unknown supply. Op amp IC_2 scales the signal to achieve 3-mV resolution using the microcontroller's built-in 10-bit ADC. The reference, op amp, and gain error introduce voltage offsets, which you can calibrate in software. The remaining error arises from temperature variation of these parameters. R_7 and R_8 use a temperature coefficient of 25 ppm/°C. The resulting accuracy of the voltmeter is ±7.5 mV over 0 to 50°C. By biasing the reference from a digital output, the voltmeter draws current only when necessary. The same trick biases several thermistors, which measure the temperature of the monitored cell.

This cell monitor can balance an overcharged cell by shunting 200 mA through R_2. Although the shunt current is smaller than the battery's maximum discharge current of 12A, it is more than enough current to balance the differential self-discharge of series-connected cells. EDN

White-LED driver operates down to 1.2V supply voltage

Dave Wuchinich, Modal Mechanics, Yonkers, NY

Many LED drivers, using both charge pumps and inductors, are available to boost the 1.2 to 2.4V available from single- and dual-cell NiMH (nickel-metal-hydride) batteries to the 3.6V that white LEDs require. However, most of these circuits, such as the Maxim (www.maxim-ic.com) MAX1595, require a minimum input voltage of approximately 2.5V to operate properly. The MAX1595 works with an input voltage of 2.4V but does not ensure an adequate output until the input voltage reaches approximately 3V. Furthermore, as the battery voltage decreases to the threshold level, the output becomes erratic. The circuit in **Figure 1** uses a flip-flop

to generate flux in an inductor, which then charges a capacitor in the common boost configuration. US Patent 4,068,149 describes the flip-flop's operation in an application for operating an incandescent safety lamp's flasher (**Reference 1**).

In **Figure 1**, R_1 provides a path for starting current through the base-emitter junctions of Q_1 and Q_2. Q_2 thus turns on and, in so doing, turns on Q_1, rapidly forcing both transistors into saturation. However, C_1 charges through R_2 to the battery voltage minus the base-emitter drop of Q_1 and the saturated collector-emitter voltage of Q_2, eventually causing Q_1 to turn off and thereby also turning off Q_2. C_1 then discharges through R_1 and R_2 and the forward-biased base-collector junction of Q_2. The R_2C_1 time constant determines the turn-on time, and $(R_1+R_2)(C_2)$ determines the turn-off time. C_2 acts as the capacitive input filter for the current flowing from L_1 when Q_2 is off and provides a substantially constant voltage to power D_2, a standard white LED.

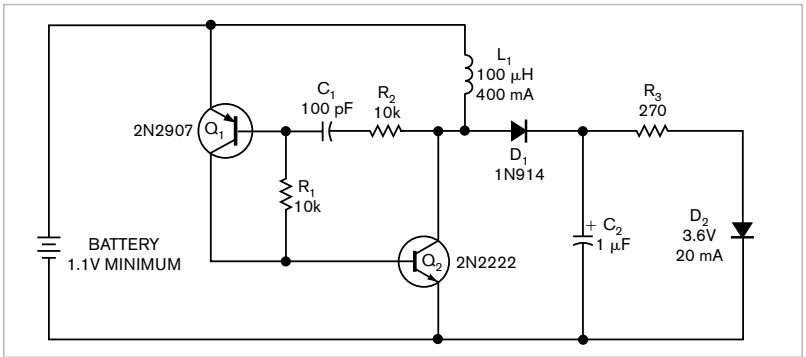


Figure 1 In this circuit, transistors Q_1 and Q_2 form a flip-flop that toggles at 60 kHz, providing a drive current for the output LED down to the 1V battery voltage.

The output voltage is proportional to the battery voltage.

With the component values in **Figure 1** and with L_1, a Coilcraft (www.coilcraft.com) MSS7341-104MLB, the operating frequency is approximately 60 kHz. With a battery voltage of 2.36V from two NiMH cells, approximately 20 mA of current flows through the LED. In tests simultaneously driving two LEDs, each with its own current-limiting resistor, R_3, the energy-conversion efficiency of the circuit at this battery voltage is approximately 80%. Operation continues with battery voltages of slightly more than 1V, and the delivered current diminishes but still provides usable illumination. EDN

REFERENCE

1 Wuchinich, David G, "Flasher circuit with low power drain," US Patent 4,068,149, Oct 28, 1975, http://patft.uspto.gov.

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READERS SOLVE DESIGN PROBLEMS

CPLD's internal oscillator performs autocalibration

Rafael Camarota, Altera Corp, San Jose, CA

The MAX II CPLD family from Altera (www.altera.com) features an internal oscillator that dissipates much lower power than do external oscillators. The internal oscillator has an accuracy of only ±25%, sometimes limiting its usage. For example, many applications, such as an interval timer for data gathering and a real-time clock, require more accuracy—±0.1 and ±0.001%, respectively. A simple circuit uses an external crystal oscillator to calibrate a timer to better than ±0.3% accuracy. The internal oscillator sustains the calibrated output even after you shut down the external oscillator to save power. The circuit maintains this accuracy as long as the V_{CC} and temperature are stable. Whenever you enable the external oscillator, the circuit quickly recalibrates if necessary.

A remote industrial sensor should sample an event every second. To save power, a timer powers down most of the sensor circuit most of the time to increase battery life. The system powers up for a short sample; then, the system, except for the CPLD, powers down, which times the period to the next power-up, sample, and calibration. Most of the components of a wireless receiver in a power-saving mode power down; however, the CPLD timer and wake-up mode stay on for monitoring and calibration.

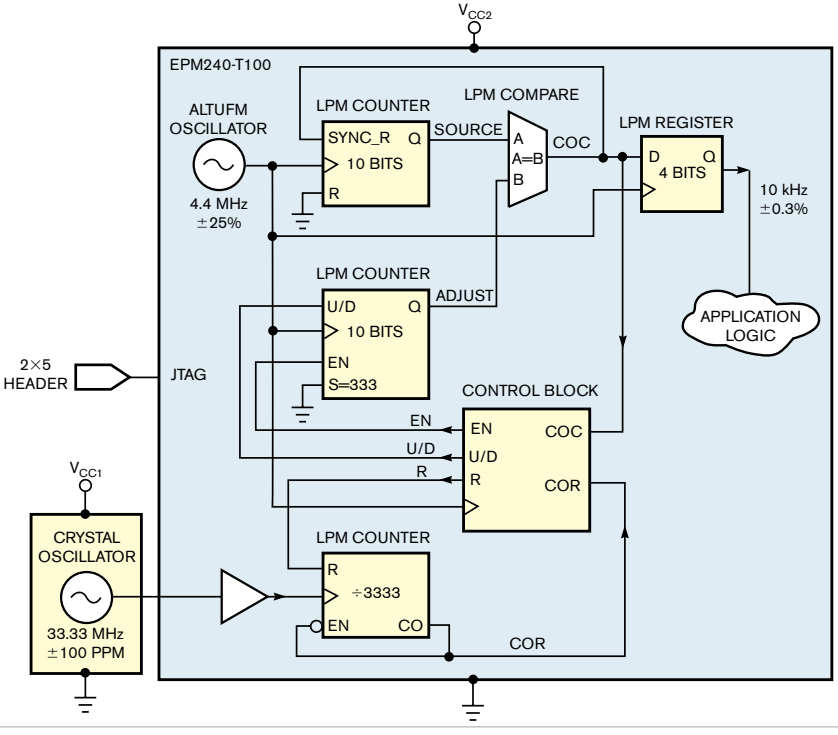

Figure 1 This internal CPLD counter first synchronizes with an external clock to ±0.3% accuracy and stays at that frequency until reset.

Figure 1 shows a simple circuit with a crystal oscillator with typical ±100-ppm accuracy; an EPM240 CPLD with a ±25%-accurate, 4.4-MHz internal oscillator; and an autocalibration circuit in the programmable-logic array that generates a ±0.3%-accurate, 10-kHz clock. For simplicity, the **figure** omits the external oscillator's V_{CC1} power-down or enable circuit and the application logic using the 10-kHz clock. The 33.33-MHz clock drives a reference counter, which is a divide-by-3333 LPM (library-of-parameterized-macros) counter. You derive LPM blocks from Altera's Quartus II LPM. The COR (carry-out-reference) signal feeds back to the count-enable input such that the COR signal stays at one after reaching the 3333 count until you apply the reset signal. The divide-by-3333 counter generates a 0.1-msec reference period. The 4.4-MHz LPM oscillator drives all other clocks in the autocalibration circuit: the source

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counter, a 10-bit counter with a power-up asynchronous reset; a synchronous reset; and a 10-bit output source. The 4.4-MHz clock also drives the 10-bit up/down-adjust counter that presets to 333 at power-up. It has an enable input, an up/down-control-input signal, and a 10-bit output adjustment. The adjust and source drive the inputs of the compare LPM that generates a one on the COC (carry-out-from-comparator) signal when adjust equals the source. The COC signal drives the synchronous input of the source counter, making it a free-running counter with a period equal to the adjustment signal. An LPM register converts the COC signal into a synchronous, 10-kHz pulse when you calibrate the system. The control-logic block generates enable, up/down, and synchronous-reset output signals based on the COC and COR inputs.

Figure 2 shows the operation of the control-block state machine. It also illustrates how the 10-kHz signal calibrates to the oscillator input. The system powers up in the start state, and the source and reference counters both start counting. Adjust starts at 333, the minimum count that the slowest variation of the LPM oscillator would require to generate a 10-kHz clock. The COR signal typically goes high before the COC signal. This action moves the state machine to the slow state, enabling the adjust counter in the up mode. It counts up from 333 until the source equals the reference, removing most of the difference between adjust and the value necessary to achieve calibration. Once the source equals the reference, the state machine moves to the calibrate state. Calibrate disables the adjust counter and resets the reference counter. The free-running source counter resets at the same time.

The COR signal will likely occur again before the COC signal and will repeat the last sequence. Eventually, the COC signal will happen before the COR signal, moving the state machine to the sustain state. In this state, the adjust counter is disabled. Once the COR signal goes high, the COC signal comes around again, making the COC and COR signals ones. The state machine then goes to the fast state. Fast enables the adjust counter in the down mode, resets the reference counter, and then goes to start. The free-running source counter resets at the same time.

When you calibrate the circuit, the COR and COC signals occur at the same time, and the state machine goes to the calibrate state. The adjust counter remains constant, the source counter resets, and the state machine moves to start. Meanwhile, the free-running source counter resets. The system stays in this calibrated loop with an occasional cycle through slow or fast to make minor adjustments to the adjust counter. If the external oscillator stops, the COR signal stays low, resulting in the state machine's staying in the sustain state until the external clock starts again. In the sustain state, the 10-kHz output stays constant assuming no significant change in system temperature or V_{CC}.

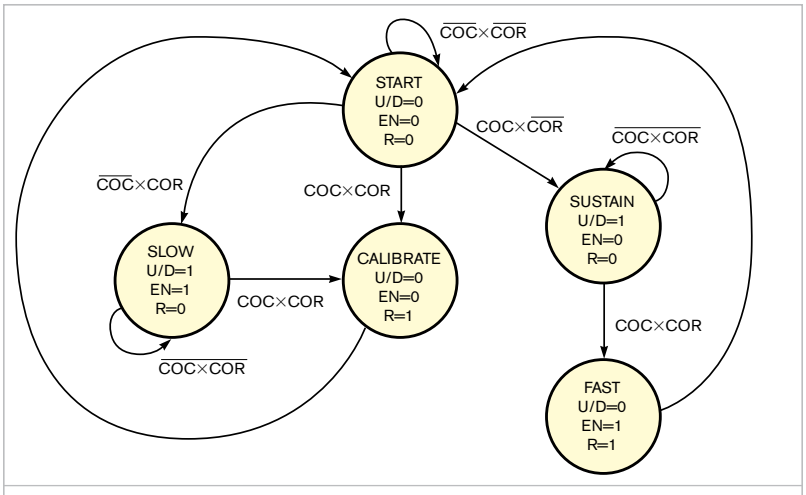

Figure 2 This state machine shows the transitions of the control block in Figure 1.

The following **equations** set the reference-count, adjust, and source-counter bit width; the adjust-counter start value; and the output-frequency accuracy: Adjust and source bit width=log2(5,555,555/output frequency) rounded up; adjust-start value=3,333,333/output frequency; reference-counter period=external-oscillator frequency/output frequency; output-frequency error=±1%/(3,333,333/output frequency); maximum output jitter=±1/3,333,333 sec; and maximum calibration time=output frequency×5.

You can achieve accuracy better than ±0.3% with a slower output frequency, but it cannot exceed the accuracy of the external oscillator. Therefore, you can build a real-time clock with a 0.01-second resolution and ±0.003% accuracy. EDN

Swapping bits improves performance of FPGA-PWM counter

Stefaan Vanheesbeke, Ledegem, Belgium

When you need some analog outputs and you have an FPGA in your system, you probably choose to use a PWM module and a simple low-pass filter such as those in **Figure 1**. The output of the FPGA is typically a waveform with a fixed-frequency, variable-duty cycle, which a counter and a digital comparator generate (**Listing 1**).

Suppose that Enable is high, the counter counts up every clock cycle,

LISTING 1 FPGA OUTPUT

```
module pwm(Clk, Reset, Enable, Value, Out);

parameter CountBits = 8;

input  Clk, Reset;
input  Enable;
output Out;
input  [CountBits-1:0] Value;

reg    [CountBits-1:0] Count;

assign Out = Count < Value;

always @(posedge Clk or posedge Reset)
  if (Reset)
    Count <= 0;
  else
    if (Enable)
      Count <= Count + 1;

endmodule
```

LISTING 2 REWIRING MODIFICATION

```
module pwm(Clk, Reset, Enable, Value, Out);

parameter CountBits = 8;

input  Clk, Reset;
input  Enable;
output Out;
input  [CountBits-1:0] Value;

reg    [CountBits-1:0] Count;

reg [CountBits-1:0] Swapped;
integer k;
always @*
  for (k = 0; k < CountBits; k=k+1)
    Swapped[k] = Count[CountBits-1-k];

assign Out = Swapped < Value;

always @(posedge Clk or posedge Reset)
  if (Reset)
    Count <= 0;
  else
    if (Enable)
      Count <= Count + 1;

endmodule
```

and the frequency of the PWM output is the clock frequency divided by 2 count bits. You can use Enable to lower the output frequency by connecting it to a prescaler. Because the output frequency is fixed, the filter is easy to calculate, because you know that the worst-case ripple happens at a duty cycle of 50%. The combination of the desired maximum ripple and settling time determines the filter type and RC (resistance/capacitance) values.

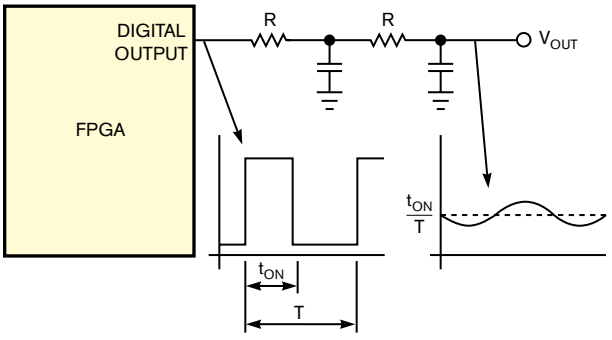

Figure 1 A simple lowpass filter changes the PWM digital output from an FPGA to an analog voltage level. The maximum ripple occurs at a 50% duty cycle.

LISTING 3 SIMULATION RESULTS

```
Simulation results :

Testing   0 : 0000000000000000
Testing   1 : 0000000000000001
Testing   2 : 0000000100000001
Testing   3 : 0001000100000001
Testing   4 : 0001000100010001
Testing   5 : 0101000100010001
Testing   6 : 0101000101010001
Testing   7 : 0101010101010001
Testing   8 : 0101010101010101
Testing   9 : 1101010101010101
Testing  10 : 1101010111010101
Testing  11 : 1101110111010101
Testing  12 : 1101110111011101
Testing  13 : 1111110111011101
Testing  14 : 1111110111111101
Testing  15 : 1111111111111101
```

With a small change to the code in **Listing 1**, you can improve the performance of the PWM circuit. Whereas in the original system, the maximum ripple currents occur at a duty cycle of 50% and the minimum ripple currents occur at the minimum duty cycle, the improved version shows a maximum ripple equal to the minimum of the standard version. The trick is to generate the highest frequency possible but keep the average duty cycle constant. The higher the frequency of the pulses on the output, the better the filter does its job.

The modification to **Listing 1** consists of rewiring the binary comparator with all the bits swapped from left to right. The MSB (most significant bit) becomes the LSB (least significant bit), the LSB becomes the MSB, and so on (**Listing 2**). You do only a rewiring requiring no extra registers or logic.

Listing 3 shows the pulse trains that a 4-bit PWM emits. In **Listing 3**, you see that at 50% duty cycle (Value=8, second column), the frequency is maximum and equal to the clock frequency divided by two. At the first point at which some ripple shows up (Value=1, second column), there is exactly the same ripple as in the conventional PWM system—that is, the pulse train is the same. EDN

Relays eliminate high-voltage noise

Jui-I Tsai, Woei-Wu Pai, Feng-Chang Hsu,
Po-Jui Chen, Ching-Cheng Teng, and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

Most laboratories and industrial environments have many kinds of electrical-noise sources at all frequencies from heavy machinery, instruments, power supplies, and TV stations. Engineers have used many simple devices and techniques to handle this noise. These techniques include the use of proper grounding methods, shielded and twisted wires, signal averaging, differential-input-voltage amplifiers, and filters. Although these methods can control and reduce the noise in most measurements, some techniques just prevent noise from entering the system, whereas others remove only extraneous noise from the signal. These methods usually find use only in low-voltage sys-

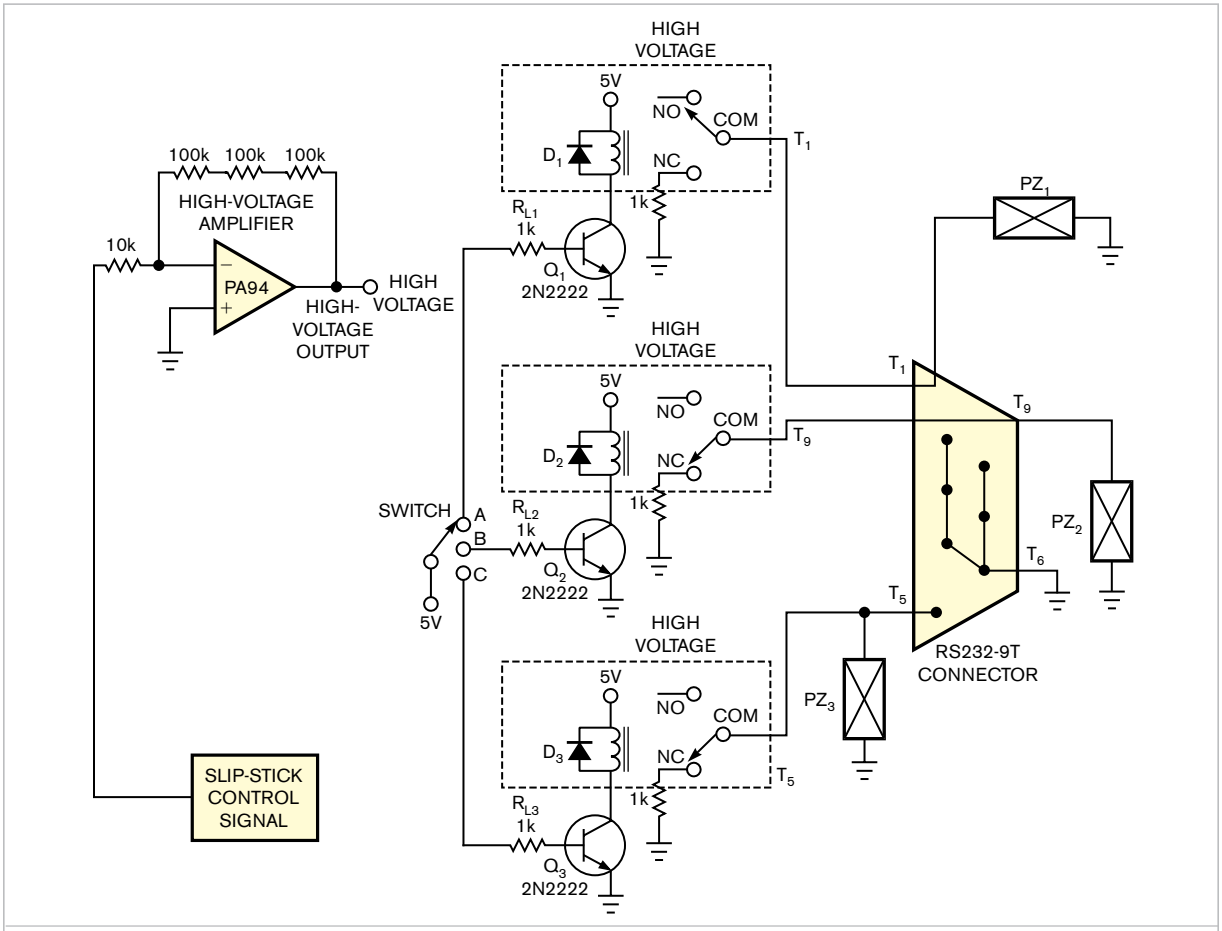

Figure 1 This simple circuit connects unenergized inputs to ground through a resistor.

tems; they do not address high-voltage-induced noise. This Design Idea offers a practical approach to reducing high-voltage-induced noise. The floating input of a scanning electron microscope has high impedance, and it acts as an antenna, picking up noise signals. The microscope's actuators need a high-voltage signal to drive their piezoelectric slip-stick stack motors. The motion mechanism requires a ramping waveform spanning to 800V p-p. The mechanism requires multiple channels because there are three degrees of tip motion. Some microscopes incorporate optical-path-adjustment microsliders for atomic-force microscopy; those scopes need even more channels.

Traditionally, each channel needs a high-voltage amplifier. So, two degrees of tip motion need two high-voltage amplifiers, three degrees need three amplifiers, and so on. High-voltage amplifiers are expensive and need considerable space on the PCB (printed-circuit board), however. Therefore, controlling multiple degrees of tip motion using only one high-voltage amplifier that switches among multiple channels saves cost and space. The pins of high-voltage connectors have enough space between them to avoid disturbing adjacent signals. But high-voltage connecters are expensive and too large to easily arrange. So, the best choice is to use a commercial RS-232-standard, nine-pin/25-pin connector (**Figure 1**). The pins of most commercial RS-232 connectors are close enough together to easily pick up induced high-voltage signals. You can solve this problem by connecting a low impedance to the floating pins of the RS-232 connector.

THE FLOATING INPUT OF A SCANNING ELECTRON MICROSCOPE HAS HIGH IMPEDANCE, AND IT ACTS AS AN ANTENNA, PICKING UP NOISE SIGNALS.

In this circuit, three piezoelectric motors, PZ_1, PZ_2, and PZ_3, connect to the T_1, T_5, and T_9 pins of the RS-232-9T connector. The circuit has three relays that switch the high-voltage input to the piezoelectric motors. The normally open node of the relays connects to the high-voltage-amplifier output. The normally closed nodes of the relays connect to three 1-kΩ resistors to bypass high-voltage-induced noise to ground. EDN

VHDL program enables PCI-bus-arbiter core

Antonio Di Rocco, Selex Communications, Chieti, Italy

This Design Idea describes a VHDL implementation of a PCI 2.2-bus arbiter (**Figure 1**). Any PCI system may have one or more PCI-master devices. Most devices can behave as target hosts, but one must be a PCI-bus initiator, or master. Normally, only microprocessors or high-level DSPs perform both PCI master and target modes, and they may include a PCI arbiter. **Listing 1**, a simple VHDL program, is available at www.edn.com/070913di. It performs an arbitration function by enabling access to the PCI bus depending on the predetermined priorities of each PCI device. The PCI-arbiter core interfaces with 33- and 66-MHz PCI systems, supports as many as six PCI-bus masters, supports "bus parking," enables a pure rotational-arbitration scheme, supports bus latency and broken masters, and is a synthesizable VHDL source without FGPA- or PLD-library intellectual property.

The PCI bus supports more than one master device. If only one master requests the bus, that master immediately gets the grant. If several devices simultaneously require the use of the PCI bus to perform a data transfer, they assert their request signal, REQ_N, to the arbiter. The one with highest priority gets the GNT_N grant. After that, the one with the second highest priority has the highest priority, and so on. The PCI_RST assertion resets the arbiter's priority-shift register to device 0.

The PCI bus has no pullups on the AD bus and C/BE lines. To avoid having these signals float for a long period, PCI designs must implement bus parking, meaning that a master device drives the AD bus and C/BE lines during bus-idle states. The arbiter selects which master will be park master. The arbiter asserts GNT_N of the park master, even though the park master did not assert REQ_N. The constant "Bus_parker" in the VHDL code defines the park master. After a device has access to the PCI bus, this device must start the bus access within 16 PCI clock cycles. If this start-up does not happen, the device loses the bus grant, and the device with the next highest priority gets the bus. To check bus latency, the arbiter must check the signals FRAME_N and IRDY_N. The PCI-arbiter core fits into any PLD or FPGA and consumes few resources. EDN

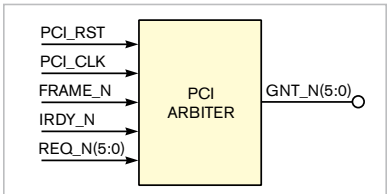

Figure 1 This PLD/FPGA-based PCI-bus arbiter grants bus requests based on a simple rotational-priority scheme.

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READERS SOLVE DESIGN PROBLEMS

Single op amp achieves double-hysteresis-transfer characteristic

Herminio Martínez, Encarna García, and Juan Gámiz,
Technical University of Catalonia, Barcelona, Spain

In process-control applications requiring discontinuous controllers, the most elementary choice is a two-position-mode or on/off controller. A typical example of such a controller is a space heater. If the temperature drops below a setpoint, the heater turns on, and, if the temperature rises above the setpoint, it turns off. In the analog domain, the basis for the basic implementation of a two-position controller is an analog comparator or an open-loop operational amplifier. However, to avoid false switching, the typical implementation uses the well-known Schmitt trigger.

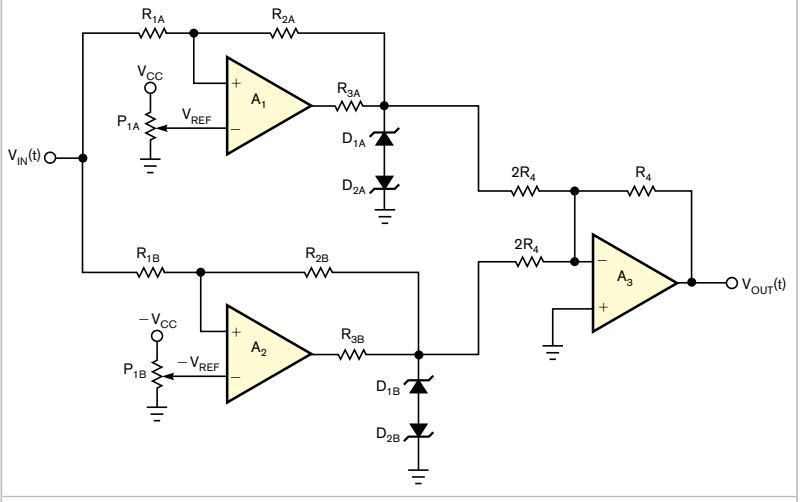

Figure 1 One straightforward way of obtaining a double-hysteresis-transfer characteristic uses three op amps with voltage references and zener diodes.

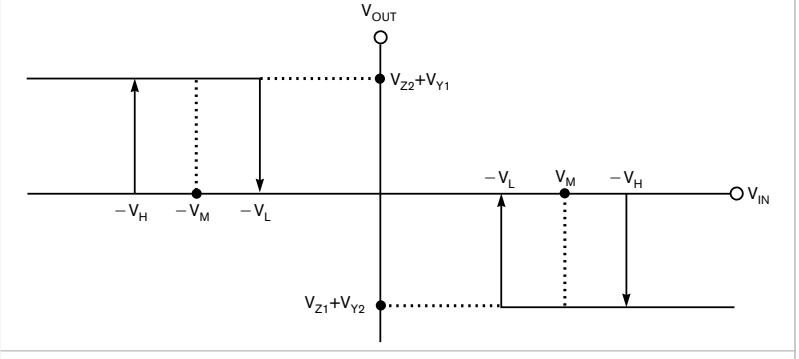

Figure 2 The I/O-transfer characteristic of the circuit in Figure1 exhibits two hysteresis bands.

A logical extension of the two-position control mode is to provide several—rather than two—intermediate settings of the controller's output. You can use this discontinuous-control mode to reduce the cycling behavior, overshoot, or undershoot inherent in the two-position mode. In fact, however, it is usually speedier to use some other mode when the two-position mode is unsatisfactory. The most common example is the three-position controller. **Figure 1** shows one simple way to implement this controller. In this configuration, the Schmitt triggers around the operational amplifiers, A_1 and A_2, which implement the negative and positive hysteresis, respectively. You can replace A_1 and A_2 with analog comparators, such as an LM311 or similar. **Figure 2** shows the I/O-transfer characteristic of the circuit in **Figure 1**:

$$V_M = V_{REF}\frac{R_1 + R_2}{R_2},$$

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$$V_H = V_M + (V_Z + V_Y)\frac{R_1}{R_2},$$

and

$$V_L = V_M - (V_Z + V_Y)\frac{R_1}{R_2}.$$

V_Z and V_Y are, respectively, the breakdown and the forward voltages of the four zener diodes.

Figure 3 shows a more efficient way to implement a three-position controller. The circuit's basis is a single operational amplifier, and it needs no reference voltages. The input and output diodes determine the upper high-voltage and lower low-voltage switching-threshold levels and the hysteresis of the comparator. Putting $V_{IN}(t)$ in the middle band eliminates the input diodes from the circuit, and the circuit is essentially a voltage follower with positive feedback. The output voltage follows $V_A(t)$, but the positive feedback establishing $V_A(t)$ sets this voltage at some fraction of the output voltage. So, two constraints define the output level in this circuit state: $V_{OUT}(t)=V_A(t)$, and

$$V_A(t) = V_{OUT}(t)\frac{R_1}{R_1 + R_2}.$$

The only condition satisfying these two constraints is that V_{OUT} and $V_A=0V$; so, the output remains at 0V when the input diodes are reverse-biased. A 0V output state continues until input voltage increases with positive or negative values. Then, one of the two input zener diodes conducts, driving the amplifier output positive or negative at an input voltage of $\pm V_H$. In this condition, when absolute input voltage decreases, the amplifier output again goes to 0V at an input voltage of $\pm V_L$. Thus, the design equations for V_H and V_L are $V_H=V_{Z1}+V_\gamma$, and

$$V_L = (V_{Z1} + V_{Y1}) - (V_{Z2} + V_{Y2})\frac{R_1}{R_1 + R_2}.$$

Figure 4 shows the I/O-transfer characteristic of the circuit with the values in **Figure 3**, where D_{1A} and D_{1B} are 6.8V 1N4099 zener diodes and D_{2A} and D_{2B} are 3V 1N5225 zener diodes. **Figure 5** shows the output voltage when you apply a triangular waveform at the circuit's input. EDN

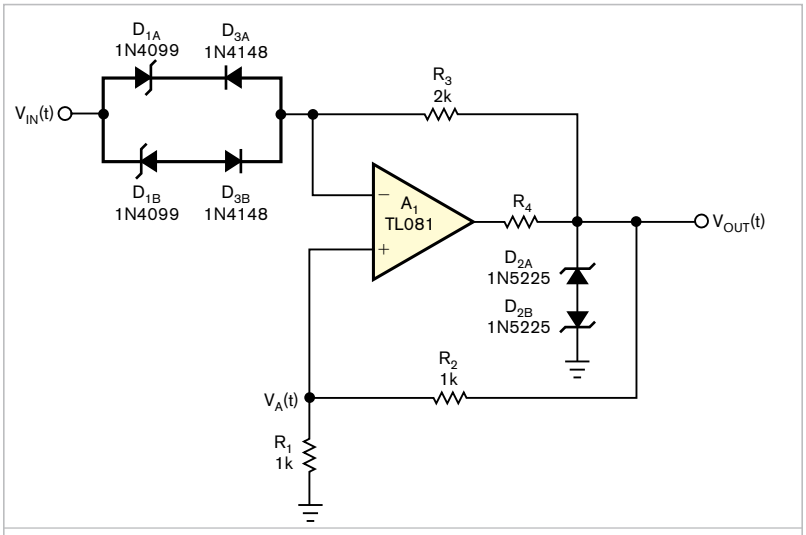

Figure 3 This circuit achieves dual hysteresis using only one op amp.

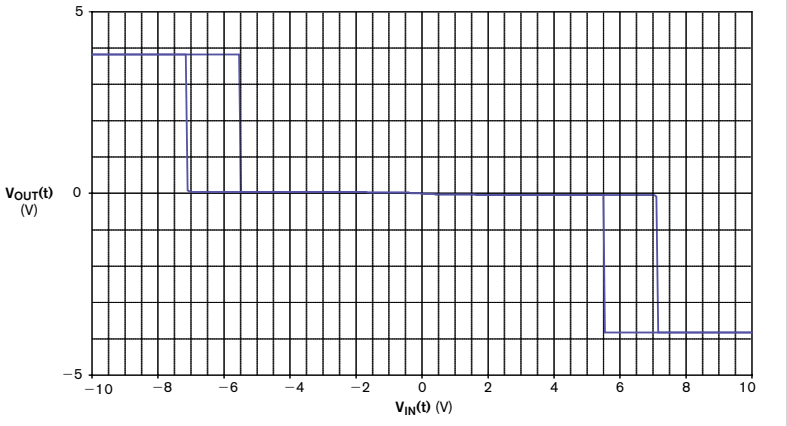

Figure 4 This oscilloscope trace shows the transfer characteristic of the circuit in Figure 3.

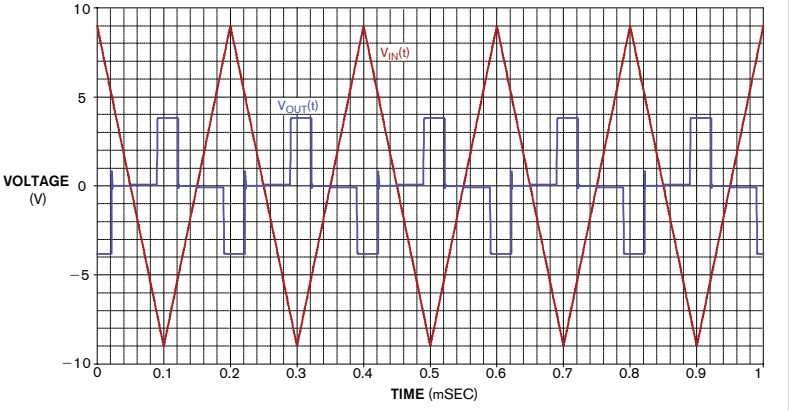

Figure 5 This oscilloscope trace shows the response of the circuit in Figure 3 to a triangular input waveform.

Integrator ramps up/down, holds output level

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

Op-amp integrators can ramp to saturation, and a capacitor-discharge switch can reset them. Alternatively, you can input-switch them to ramp up and down in triangle-waveform-generator applications. Much searching through online "cookbook" circuits turned up no means of ramping an op-amp integrator to hold at a preset constant voltage level. This Design Idea describes a single-supply op-amp circuit that outputs a rising or falling linear-voltage ramp in response to a step change of a positive dc-input voltage of 0V to V_{CC}. The output ramp's dV/dt slope is adjustable to 1V/minute with the values in **Figure 1**, is independent of the input-step amplitude, and terminates at a constant dc level approximately equal to the input-step voltage. Any further change in the dc-input voltage causes the output to ramp up or down at the preset dV/dt to the new dc-input voltage. In effect, this circuit is an amplitude-bounded constant-slope integrator.

The circuit uses a rail-to-rail I/O quad op amp, the National Semiconductor (www.national.com) LMC6484. The rail-to-rail feature makes it easy to use, the low input leakage is great for long-time-constant integration, and the 3-mV maximum input-offset voltage is respectable. Potentiometer R_1, a linear taper, sets the input voltage for final output voltage after the ramp ends. IC_{1A}'s output is in saturation at V_{CC} or ground while the output is ramping down or up, respectively.

Nonpolarized capacitor C_1 and potentiometer R_2, a linear taper, determine the time constant of integrator IC_{1B}. The adjustment range is 0.5V/msec to 1V/minute. The reference bias for IC_{1B} is 108 mV, which you derive from IC_{1D} as a unity-gain buffer for divider R_7 and R_8. R_6 ensures that you do not exceed IC_{1B}'s input current when you turn off the power, that C_1 discharges through IC_{1B}'s input and output diodes, and that IC_{1B}'s output does not excessively load back into IC_{1D}'s output with R_2 at a minimum.

R_3 and R_4 divide the saturated IC_{1A}'s output to approximately 100 mV unloaded above or below the 108-mV bias. This division causes approximately 20 mV to drop across R_5 to slew IC_{1B} upward or downward at the integration rate that C_1 and R_2 set; 20 mV is comfortably above the op amp's possible 3-mV input-offset voltage to minimize offset effects. When IC_{1B}'s output-voltage ramp reaches that of the input voltage from the R_1 wiper, IC_{1A} comes out of saturation and rests at approximately 2.5V, providing the loop-negative feedback to maintain integrator IC_{1B}'s output equal to the input voltage. This action sets the boundary on the integration ramp's terminal voltage. IC_{1C} can be spare, or, as the **figure** shows, you can drive it with a triangle-wave signal to convert IC_{1B}'s dc level or ramp to a corresponding PWM (pulse-width-modulated) signal for a motor-drive circuit (not shown).

R_5 eliminates differential errors arising from bias-resistor tolerance, and it provides a compromise between IC_{1B}'s 3V maximum input-offset voltage at 25°C and 20-mV input amplitude to allow the slowest dV/dt. The values in the **figure** result in a maximum time of approximately 1V/minute, or 5 minutes at V_{CC} of 5V to reach full speed. If you require longer times,

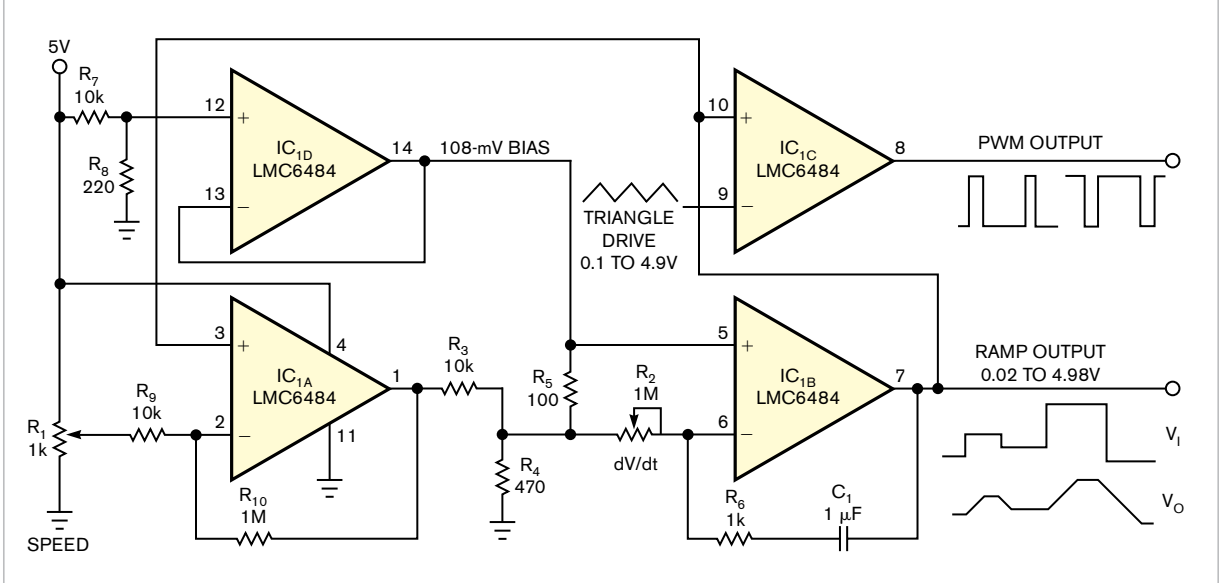

Figure 1 This op-amp integrator ramps up or down at a preset rate, holding a final value equal to the input-voltage dc level.

you can raise V_{CC} to 15V with adjustments to the bias resistors or raise C_1's value by using parallel nonpolarized capacitors. Alternatively, you could raise R_2's value, although selection is sparser for potentiometers with values greater than 1 MΩ.

If your application does not require a long time constant or if you use the aforementioned methods to increase the time constant, you can eliminate R_5 at the expense of a higher level differential input to IC_{1B} and correspondingly faster integration. You could also eliminate IC_{1D} and the R_7-R_8 resistive-bias divider that connects directly to IC_{1B}'s Pin 5, but resistor tolerance becomes more critical to minimize differential error (**references 1** and **2**). EDN

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Switcher adds programmable-PWM-duty-cycle clamp

Michael O'Loughlin, Texas Instruments, Nashua, NH

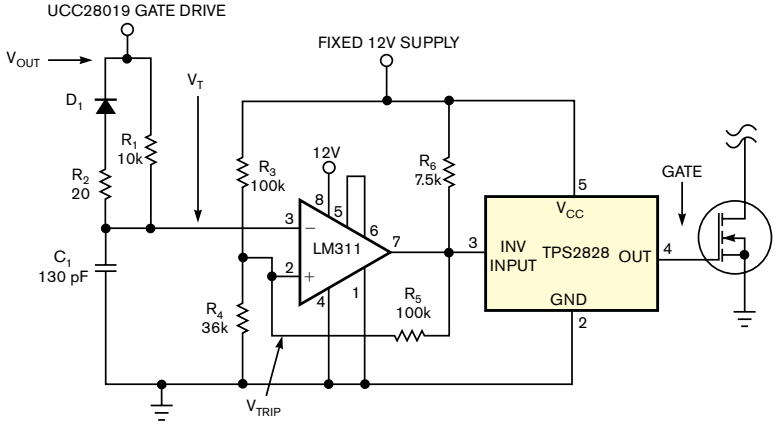

Figure 1 This simple circuit clamps the duty cycle of a switching regulator to 90%.

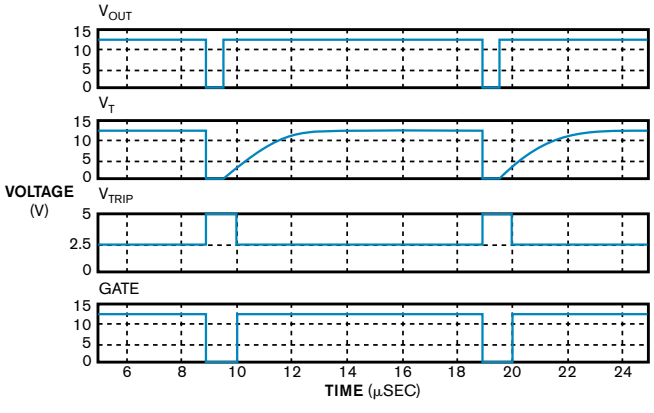

Figure 2 A SPICE simulation of the circuit in Figure 1 shows the clamping action cutting in at 90% duty cycle.

Power-supply applications require the use of a duty-cycle clamp. Such applications include those using current-sense transformers and two-switch forward converters. If a duty-cycle clamp is not present, the transformers could saturate, causing a catastrophic failure in the system. However, to drive down the cost of the design, many power-supply designers use inexpensive, eight-pin PWM controllers that have no duty-cycle clamp. This Design Idea shows how to add an inexpensive duty-cycle clamp to these PWM controllers.

You can add the circuitry to most PWM controllers to provide a programmable duty-cycle clamp (**Figure 1**). The circuitry comprises a few passive components, a hysteretic comparator, and a gate-driver IC. Resistor R_1 and capacitor C_1 program the duty-cycle clamp's dead time. Resistor R_2 and diode D_1 reset the timing circuitry when the output of the PWM controller goes low. Resistors R_3, R_4, and R_5 set the comparator's trip point, V_{TRIP}, at 5V. Resistor R_5 adds −2.5V of hysteresis to the comparator to ensure circuit stability.

The following example shows how to set the circuitry in **Figure 1** for a maximum duty cycle, D_{MAX}, of 0.9. The PWM controller operates at a switching frequency, f_S, of 100 kHz. Most PWM controllers cannot reach 100% duty cycle and have a specified dead time. For this example, the dead time is 300 nsec. To set the timing capacitor also requires knowing the maximum output of the PWM output voltage, V_{OUT}. In this example, the maximum output voltage is 12V. The timing ca-

pacitor is roughly 130 pF. The design uses a standard, 120-pF capacitor. The following **equations** describe the calculations: $t=(1-D_{MAX})(1/f_S)-$dead time$=700$ nsec, and

$$C_1=\frac{-t}{\ln\left(1-\frac{V_{TRIP}}{V_{OUT}}\right)R_1}\approx 130\text{ pF}.$$

A SPICE simulation with the circuitry in **Figure 1** ran to ensure that the duty-cycle clamp works with the circuitry. **Figure 2** shows the results of this simulation. V_{OUT} is the output of the PWM controller, V_T is the voltage at the inverting pin of the comparator, V_{TRIP} is the voltage at the noninverting input of the comparator, and gate is the output of the gate-driver IC. From the waveforms in **Figure 2**, you can see that the duty-cycle clamp appears to be working correctly, clamping the output of the gate driver to 90%.EDN

Circuit provides low-cost QAM mapping and translation

Pieter Demuytere, Cedric Mélange, Elena Matei, Els De Backer, Johan Bauwelinck, and Jan Vandewege, Ghent University, Department of Information Technology, Ghent, Belgium

This Design Idea presents an efficient way to do QAM (quadrature-amplitude-modulation) mapping and translation into two's-complement values with only two inverters and no look-up tables.

Suppose you want to create a 256-level QAM signal using a microcontroller and two 10-bit DACs with a parallel input in two's-complement notation. Because you can split a 256-level QAM signal into a 16-level ASK (amplitude-shift-keying) signal for the in-phase component and a 16-level ASK for the quadrature component, a symmetrical approach is feasible. The fully symmetrically circuit performs the 16-level ASK mappings and translations (**Figure 1**). Two inverters are the only glue logic you need for the conversion. Each part of the circuit converts four output bits of the microcontroller into a 10-bit two's-complement vector, which feeds directly to the DACs (**Table 1**). The possible DAC-input values are equally distributed. The third column of **Table 1** gives the normalized DAC output after an optional current-to-voltage conversion.

For 256-level QAM signals, you need 8 input bits, which exactly fit the width of a general-purpose-I/O bank on most microcontrollers. Simultaneously setting all 8 bits ensures synchronization between in-phase and quadrature signals. You can easily adapt this circuit for any QAM constellation or DAC resolution. Because this circuit is fully digital, you can also embed it in FPGAs or CPLDs, using the inverters available in the output buffers.EDN

TABLE 1 INPUT AND OUTPUT

Microcontroller output	DAC input	DAC output (V)
0000	1000 0000 10	−0.998
0001	1001 0001 10	−0.863
0010	1010 0010 10	−0.730
…	…	…
0111	1111 0111 10	−0.066
1000	0000 1000 10	0.066
…	…	…
1101	0101 1101 10	0.730
1110	0110 1110 10	0.863
1111	0111 1111 10	0.998

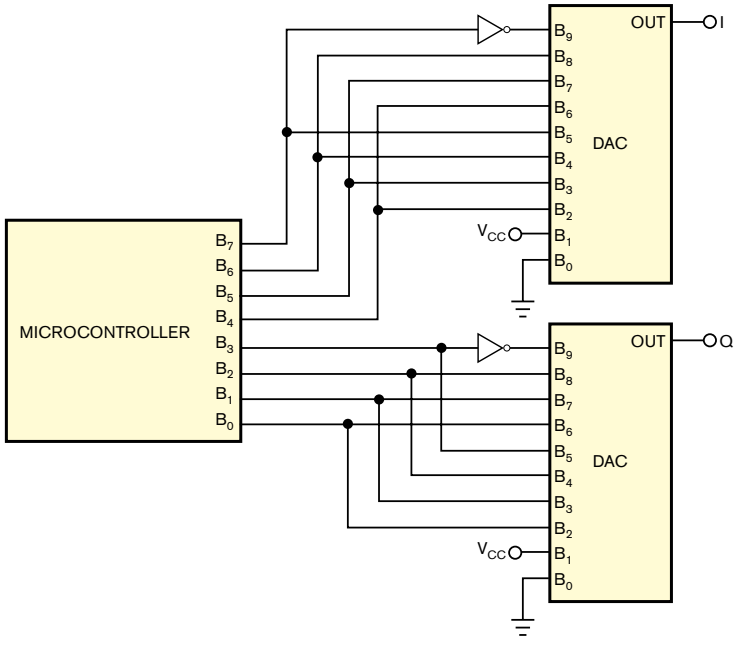

Figure 1 This circuit converts 2×4-bit outputs from the microcontroller into 2×12-bit, 16-level ASK values.

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READERS SOLVE DESIGN PROBLEMS

Circuits protect outputs against overvoltage

Dimitri Danyuk, Kiev, Ukraine

In test-and-measurement applications, you must provide overvoltage protection for the output terminals of amplifiers, power supplies, and similar components. The conventional way to accomplish this task is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages (**Reference 1** and **Figure 1**). This resistor significantly reduces current-output capability and the output-voltage swing with low-resistance loads. The alternative approach is to use fuses or other current-limiting devices, which precede these clamps' high energy-absorption capability. The circuit in **Figure 2** works as a bipolar current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2, thus limiting the current through the clamping diodes (**Reference 2**). The drawback of this approach is high power dissipation on series components during the overload condition.

A reasonable approach disconnects the amplifier-output node from the output terminals for the period when the overload voltage exists on output terminals. Engineers for decades have used such serial disconnection by means of electromechanical relays in audio power amplifiers but for a different reason: loudspeaker protection. SSRs (solid-state relays), including optoelectronic, photovoltaic, OptoMOS, and PhotoMOS devices, suit the task

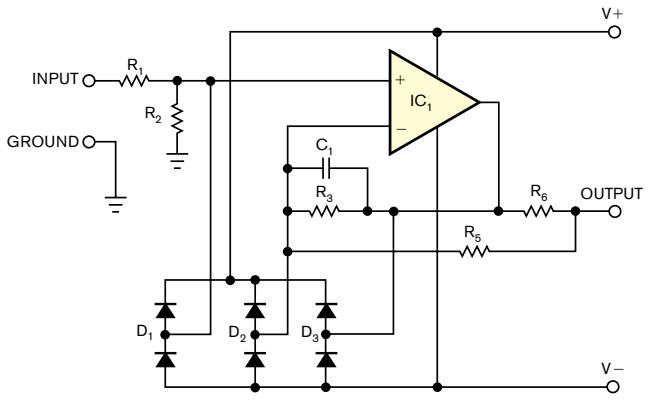

Figure 1 The conventional way to provide overvoltage protection is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages.

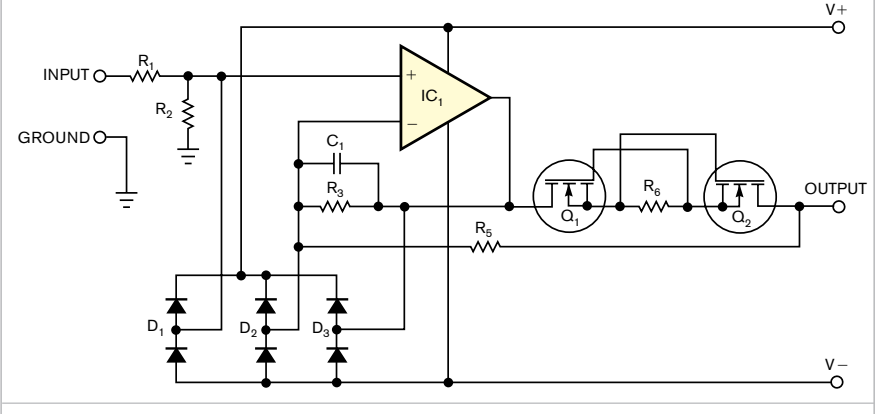

Figure 2 This circuit works as a bipolar-current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2, thus limiting the current through clamping diodes.

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of load disconnection at moderate current levels because of galvanic isolation between the control and the load pins (**Reference 3**).

The series-protection circuit of **Figure 3** disconnects the amplifier-output terminal using a series-connected, high-voltage SSR. Raising the output voltage above the positive-reference-voltage or below the negative-reference-voltage threshold causes either the IC_2 or the IC_3 comparator to change its output state and turn off SSR IC_4 through AND logic element IC_5. **Figure 4** shows the simple circuit realization of this approach.

The circuit in **Figure 4** requires only a couple of external components to use an SSR for output-overvoltage protection. Rising overvoltage turns off both transistors in IC_2, interrupting current flow through the control LED of IC_3. Relay IC_3 opens, protecting the amplifier and clamping diodes. The circuit was tested with a handful of Clare, Matsushita Electronic Works, and Panasonic (www.clare.com, www.naisis.co.jp/english, www.panasonic.com) SSRs with and without internal current protection. The power-supply rails are ±15V; R_{10}, R_{11}, and R_{12} set the triggering levels and are equal to ±16V. Omitting R_{11} shifts the triggering levels to ±14.5V. The SSR turn-off delay in protection-circuit operation is 100 to 200 µsec for relays with 0.5V overvoltage protection and becomes slightly shorter with higher overvoltage. Note that the peak current through clamping diodes can be rather high with low-on-resistance SSRs. EDN

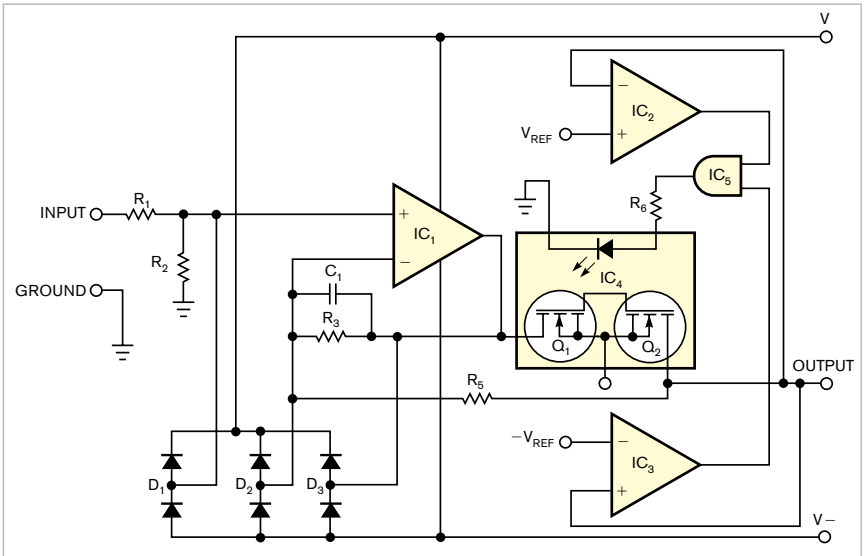

Figure 3 This series-protection circuit disconnects the amplifier-output terminal using a series-connected, high-voltage SSR.

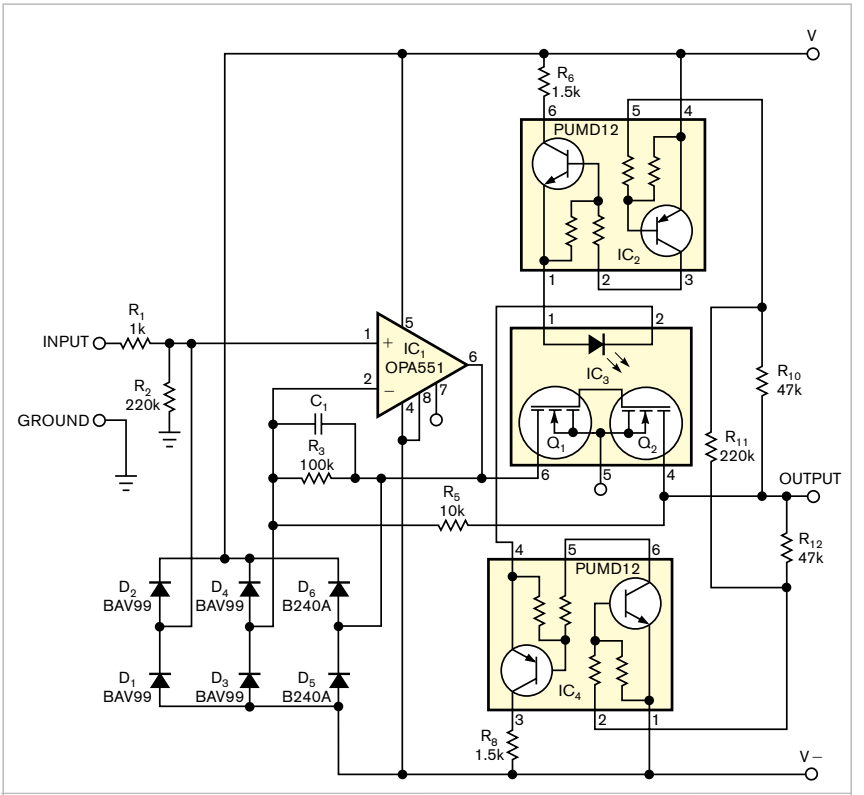

Figure 4 This circuit requires only a couple of external components to use an SSR for output-overvoltage protection.

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CPLD connects two instruments with half-duty-cycle generator

Yu-Chieh Chen and Tai-Shan Liao,
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When synchronizing two instruments' signals, it is important to make sure that the receiver can latch the sender's synchronous signal. For example, a pulse generator generates synchronizing pulses while generating the main pulse signal. For the Avtek (www.avtekcorp.com) AV-1015B, the pulse generator's duty cycle is approximately 50 nsec at TTL with a 50Ω load. The goal of this Design Idea is to increase the pulse generator's high-level width to meet the triggering spec of a lock-in amplifier. The synchronizing pulse's frequency is 10 Hz to 102 kHz, which is the lock-in amplifier's frequency range.

Because the synchronizing pulse synchronizes to the main pulse, you must minimize any delay in calculating the lock-in amplifier's synchronizing input. And, because the user can change the frequency of the pulse train from the pulse generator, the synchronizing signal's frequency also changes. Therefore, you must make sure that the circuit properly calculates and generates the synchronizing signal, no matter how the user sets the output of the pulse generator.

Figure 1 shows the half-duty-cycle generator's algorithm. The CPLD first waits for the positive-edge trigger, then starts to count at a frequency of 60 MHz, and waits for the next positive-edge trigger. When the next positive edge comes, the synchronizing signal's period counting is complete. The counting value then gets saved in a buffer and divided by 2 to yield the value for half-duty-cycle generation.

In tests, the half-duty-cycle generator in this Design Idea worked over a frequency range of 2 Hz to 450 kHz. You can use this design not only in a pulse generator, but also in any synchronizing signal in which the pulse is too narrow for other system triggering. The half-duty-cycle generator fits into a CPLD, such as an Altera (www.altera.com) EPM570 with a 60-MHz system clock and an MM74-HCT244 buffer to output a TTL signal. **Listing 1** contains the program for the CPLD. EDN

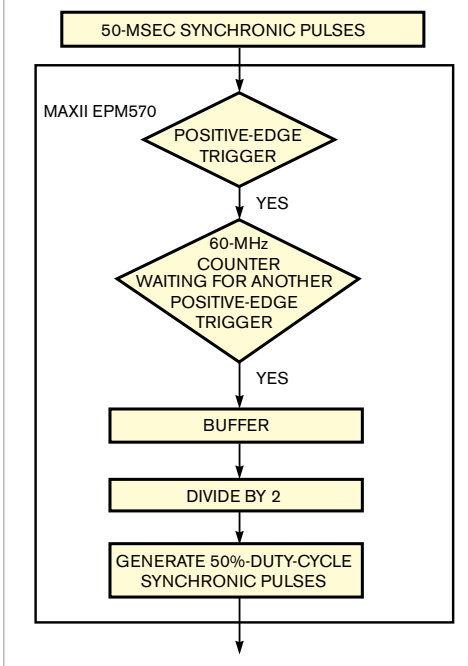

Figure 1 When programmed into a CPLD, this algorithm expeditiously generates a synchronizing signal at half the input frequency.

LISTING 1 GENERATING 50% DUTY CYCLE

```
module PulseDutyCycle  (
            input  iReset,
            input  iClk,
            input  iPPS,

            output  oSynPulse
           );

 reg   mOldPulse;
 reg    mState;

 reg   [25:0]  mCount2;
 reg   [25:0]  mCount1;
 reg   [25:0]  mCount;     //67108864


 always @( posedge iClk )    //trigger by 60MHz clock
 begin
  if( !iReset )
  begin
  case( mState )
   1'd0:
   begin
    if( mOldPulse==0 && wClk==1 )  //postive edge trigger
    begin
      mCount     = 0;    //start to count
      mOldPulse   = wClk;
      mState     = 1;
    end
    else
    begin
      mCount      = mCount + 1;
      mOldPulse   = wClk;
      mState     = 0;
    end
   end
   1'd1:
   begin
    if( mOldPulse==0 && wClk==1 )
    begin
      mCount2  =  (mCount+1)/2;    //add the first flag count,
the first count done,and divide by two
      mCount1   = mCount;         //save the total end count
      mount   = 0;
      mold Pulse  = walk;
      mutate   = 0;
    end
    else
    begin
      mount   = mount + 1;
      mold Pulse  = walk;
      mutate   = 1;
    end
   end
  encase
  end

  else if( ((mold Pulse==0)&&(walk==1)) || (mount>=mCount1)
  begin
   mount   = 0;
   mold Pulse  = walk;
  end

  else
  begin
   mount   = mount + 1;
   mold Pulse  = walk;
  end
 end

  assign oSynPulse  =  (mCount<=mCount2)? 1:0 ; //Output the
cycle pulse

endmodule
```

Achieve simple IR-data transmission from a PC's serial port

Andreas Grün, Wedemark, Germany

Often, you need to transmit a couple of bits or bytes of data to a microcontroller without a direct cable connection. One simple way to achieve this goal is to use a widely available IR receiver, such as a TSOP17xx or similar receiver from Vishay (www.vishay.com) that finds use in IR-remote-control applications, such as TVs and VCRs. These devices are easy to implement because they require no external parts. These receivers usually work with a pulsed 38-kHz carrier and include an amplifier, automatic gain control, and a demodulator.

The main problem for simple applications is building the transmitter, which requires a 38-kHz start-stop oscillator, additional supply voltage, and modulating pulses in the millisecond and submillisecond range. These factors are difficult to control with PC operating systems. On the other hand, a PC's serial port at a standard transmission rate of 38,400 bps can generate precise bursts of 38.4-kHz data with a simple frequency doubler and two IR LEDs (**Figure 1**). When transmitting bytes with an alternating zero/one pattern (hex 55), each hex-55 byte generates a burst of 18 pulses, adding the start and stop bit, and consecutive bytes can generate longer pulses.

The receiver needs pulse trains ranging from 10 to 70 pulses with approximately equal pauses between them; you can easily meet these requirements with this setup. You can generate short pauses by sending hex-0 bytes, although two pulses will transmit for each byte because of the start and stop bits. However, the receiver eliminates these pulses. Stopping the transmission for a time can generate longer pauses. You must occasionally insert longer pauses, depending on the receiver you use. You can achieve data transmission by using short and long bursts and an appropriate protocol.

The circuit in **Figure 1** forms a high-pass filter with the output impedance of the serial port and the capacitor. The positive pulses drive one IR LED; the negative pulses drive the other. Both should point to the receiver. PC ports usually provide a maximum current of 5 to 20 mA and a voltage of ±15V, thus having an output resistance in the low-kilohm range. A current-limiting resistor is usually not necessary. A value of 1 to 10 nF for the capacitor works in most cases. The receiver is tolerant. You need to adjust the capacitor's value for non-PC ports, such as the microcontroller, which have lower impedance. In practical applications, you can reliably achieve a transmission distance of 2 to 4m with a peak LED current as low as 5 mA if you point the LEDs at the receiver. A sample program for the PC is available at the *EDN* version of this Design Idea at www.edn.com/071011di1.EDN

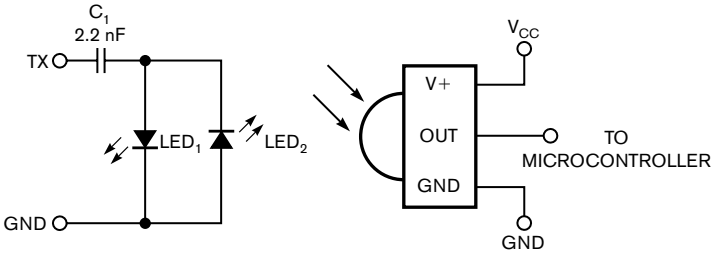

Figure 1 By sending appropriate hex values to a PC's serial port, this circuit generates precise bursts of 38.4-kHz data.

Circuit limits dV/dt and capacitor inrush at regulator turn-on

W Stephen Woodward, Chapel Hill, NC

Unusual design constraints sometimes reveal the unfriendly side of everyday components and circuits. A case in point is the design of power-supply-regulation circuitry in which the primary power source has an absolute current-limit specification, such as spacecraft photovoltaic, or "solar," panels and radioisotope-thermoelectric generators. Such applications require that you pay scrupulous attention to strict control of current consumption, including transient-current consumption, and infrequent consumption spikes, such as those that typically occur on power-up. The problem is that current-limited primary-power sources can suffer catastrophic voltage droop and shutdown in response to momentary overcurrent faults, even when the fault is brief. Common causes of such faults are the current spikes that charge the regulator output's decoupling capacitor.

Unless the current limit of the regulator clips the resulting spikes, the spikes are equal to the regulator's output-voltage rate of rise multiplied by the sum of the parallel output capacitances: $I_{MAX}=dV/dt\times C_{OUT}$, where I_{MAX} is the maximum current, dV/dt is a differential in voltage with respect to a differential in time, and C_{OUT} is the output capacitance. The math suggests that the best strategy for limiting the regulator's turn-on maximum current is

to limit dV/dt. The circuit in **Figure 1** relies on this trick and works with industry-standard adjustable linear regulators, such as the popular low-dropout LM2941.

The basis of the dV/dt-limiting technique comprises the six added components: R_3, R_4, C_T, D_1, D_2, and Q_1. On power-up, the control current through R_3, C_T, and D_2 delays the rise of the output voltage and thus prevents excessive maximum-current transients.

Here's how it works. When V_{IN} is on and Q_1 is off, current through R_3, C_T, and D_2 pulls the adjust pin of the regulator to the reference. This action limits V_{OUT}'s dV/dt to the rate of C_T charging through the series resistance, $(R_3+R_1R_2/(R_1+R_2))$, and thereby limits I_{MAX} to any desired value using the design **equations** $R_3=(V_{IN}-V_{REF}-1)/V_{OUT}$, $R_4=<20R_3$, and $C_T=C_{OUT}V_{OUT}/(I_{MAX}(R_3+R_1R_2/(R_1+R_2)))$. For example, given the circuit constants in the **figure** and assuming $C_{OUT}=100$ µF, dV/dt=2500V/s, and $I_{MAX}=0.25$A. At the end of the modified power-up sequence, D_1 and D_2 decouple the dV/dt circuit from the regulator's feedback network, preventing the coupling of ripple voltages from the input voltage into the output voltage. EDN

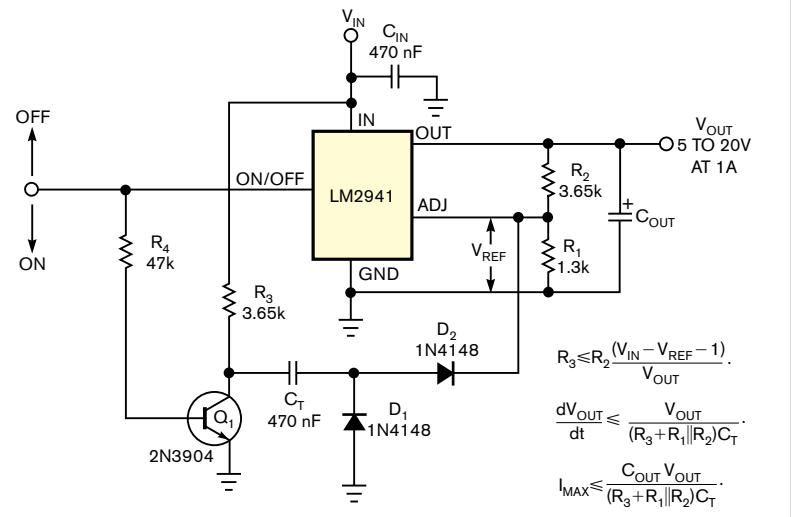

Figure 1 On power-up, the control current through R_3, C_T, and D_2 delays the rise of V_{OUT} and thus prevents excessive I_{MAX} transients.

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READERS SOLVE DESIGN PROBLEMS

Use a TL431 shunt regulator to limit high ac input voltage

Todor Arsenov, STMicroelectronics, Prague, Czech Republic

Most isolated, offline SMPSs (switched-mode power supplies), including flyback, forward, and resonant, must operate at input voltages of 90 to 260V rms. Some cases even use line-to-line voltages of 400V rms±10%, leading to increased component-voltage ratings and, thus, increased cost of the overall design. In such cases, it is preferable to use input-limiting circuits, allowing you to increase the input voltage to 440V rms without damaging the power-supply components.

The circuit in **Figure 1** limits, or clamps, input-ac voltages higher than 260V rms to levels safe for the operation of the power MOSFET in an SMPS. The circuit employs MOSFET Q_1 working as a 100-Hz switch and shunt-regulator IC_1, a TL431CZ, setting the clamped high-voltage level by divider R_2 and R_4. The circuit uses the component values shown. The clamped output voltage is 360V dc, the input voltage is 260V rms, and the maximum input voltage is 440V rms. The circuit was tested at power levels of 5 to 10W.

At an input voltage of less than 260V rms, Point C is less than 2.5V, and IC_1 is off, sinking the minimum off-state cathode current. Zener diode D_2 breaks down to 15V, ensuring a stable on-state for Q_1. This operation is the normal condition of Q_1 at input voltages lower than 260V rms. Accordingly, at these voltage levels, the circuit works as a standard full-bridge rectifier under capacitive load C_3.

At an input voltage of 260V rms or greater, Point C becomes higher than 2.5V, and IC_1 turns on, diverting and sinking the current from D_2. The gate-to-source voltage of Q_1 drops to approximately 2V, and Q_1 switches off. Now, no current flows to charge bulk capacitor C_3 even if the D_1 bridge-rectifier diodes are forward-biased. The rectified input-ac voltage is higher than the voltage across C_3, but Q_1 is off, the loop is interrupted, and no current flows. Accordingly, the output-dc voltage across C_3 gets limited because no charging current is available.

When the rectified ac-input voltage starts decreasing, it eventually hits the 2.5V threshold level of Point C, and Q_1 again switches on. But current does not flow because the rectifier bridge's diodes are now reverse-biased; the rectified input-ac voltage is less than the voltage across C_3. The voltage across C_3 decreases at a rate that the output-power level determines. Eventually, the voltage across C_3 and the rectified input-ac voltage intersect at a level when the rectifier bridge's diodes get forward-biased. Q_1 is still on; therefore, charging current starts flowing. A short interval follows, during which both Q_1 and D_1 conduct. The short

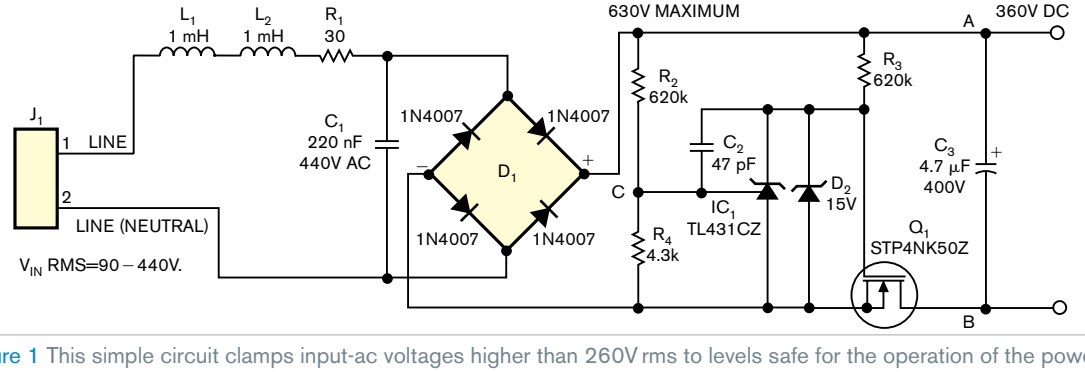

Figure 1 This simple circuit clamps input-ac voltages higher than 260V rms to levels safe for the operation of the power MOSFET in a switched-mode power supply.

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charging pulses replenish the energy loss, increasing the voltage to the limited level. When the input voltage gets higher than 260V rms, Q_1 again switches off, and the whole process repeats.

Q_1 has small power dissipation. During every switching period, the MOSFET is on for only 450 µsec, resulting in high efficiency for this high-voltage-limiting circuit. You can use it as a MOSFET switch with the STMicroelectronics (www.st.com) SuperMesh MOSFET STP4NK50Z, which comes in a TO-220 package, but you can also use a Dpak to save space because the MOSFET is not a dissipative-voltage limiter. The current through Q_1 gets interrupted when the 50/60-Hz rectifying diodes are forward-biased. This current interruption causes ringing on the drain-to-source voltage. The clamping circuit passed the conducted EMI (electromagnetic-interference) tests, according to EN 55022 Class B, using peak and average detection. The 1-mH, 0.2A chokes, L_1 and L_2, suppress EMI. The 220-nF, 440V-ac capacitor, C_1, is a simple snubber element across the rectifying diodes of the D_1 bridge. EDN

Autozeroed amplifier with halved noise needs few components

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The Analog Devices (www.analog.com) AD8553 autozeroed instrumentation amplifier has a unique architecture in that its two gain-setting resistors have no common junction (**Reference 1**). The first stage of the IC is a precise voltage-to-current converter, in which the first gain-setting resistor, R_1, sets the magnitude of the transconductance. The end stage of the IC is a precise current-to-voltage converter, in which the value of its feedback resistor, R_2, co-determines the overall voltage gain as $G=2(R_2/R_1)$. You can exploit the fact that the two gain-setting resistors are separate and that the input stage is a voltage-controlled current source to lower the component count in amplifiers with extreme noise-reduction demands.

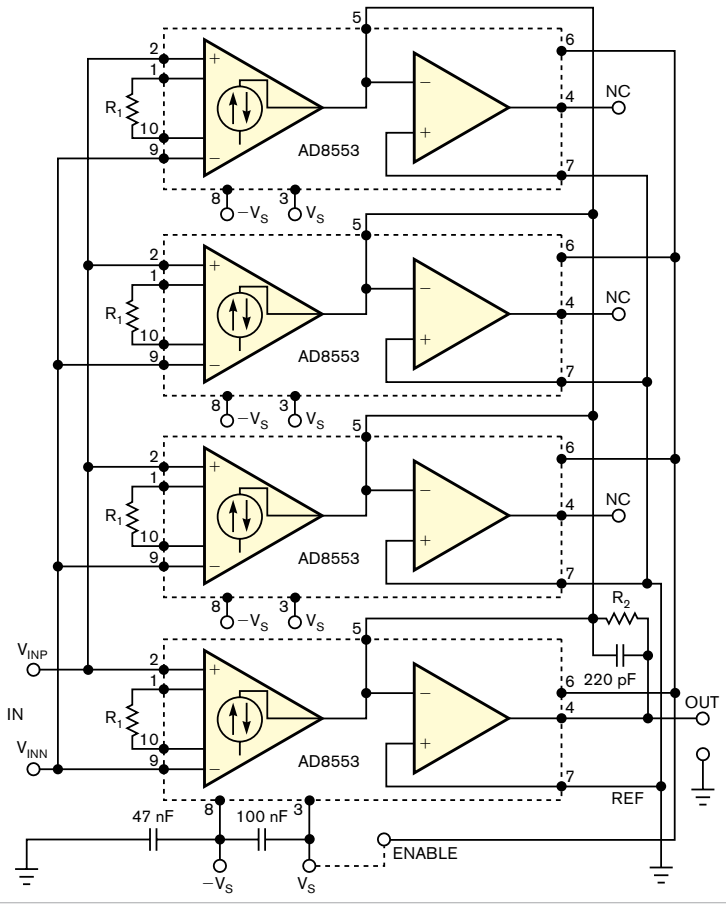

Figure 1 The unique architecture of the AD8553 instrumentation amplifier, incorporating an input-voltage-to-current converter, allows 50% noise reduction with fewer components.

You can use more amplifiers to reduce noise in two ways. First, assume that the sources of random noise in the amplifiers are mutually independent. Further, assume that the noise obeys a gaussian distribution. When averaging the outputs of classic voltage amplifiers, you can reduce the noise to a fraction of $1/\sqrt{N}$ by using N amplifiers and three times as many resistors (**Reference 2**). The internal structure of the AD8553 allows you to use just N+1 resistors for an almost-unlimited number of ICs operating in parallel. By paralleling the respective input pins of more ICs, the connected internal voltage-to-current sources easily operate in parallel (**Figure 1**). The microvolt-range input-voltage-offset mismatch at paralleled input pins of several ICs is harmless here because the output resistances of the voltage-to-current converters are theoretically infinite.

The net result of paralleling N input stages is that they output current of $N(V_{INP}-V_{INN})/(2R_1)$, or N times that of a single IC. You use only one of the current-to-voltage stages of the N ICs. That stage's feedback resistor has the

value of R_2/N, where R_2 is the value for a desired voltage gain of A_V in a single IC. Because the primary source of noise in an amplifying IC is its input stage, you can assume that the standard deviation of the random component of output current of the paralleled-N voltage-to-current converters is $\sigma_{NI}=\sigma_I\times\sqrt{N}$, where σ_I is the standard deviation of the random component of output current of a voltage-to-current converter. These results differ from those in **Reference 2**, in which the authors perform noise reduction by averaging multiple voltages. On the other hand, the deterministic part of current at the common output of the voltage-to-current converters in **Figure 1** has the value of N times that of the single IC. The following **equation** calculates the RSNR (relative signal-to-noise ratio), which you define as the output current over the standard deviation of output noise: $RSNR_N=(N\times I)/(\sigma_I\times\sqrt{N})=\sqrt{N}\times RSNR_I$. It means that, in effect, the noise of the circuit has decreased to a fraction of $1/\sqrt{N}$ compared with that of a single IC. EDN

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Buck regulator controls white LED with optical feedback

Dhananjay V Gadre, Netaji Subhas Institute of Technology, New Delhi, India

There is much interest in LED-based lighting due to the availability of high-power, high-efficiency white—and other-color—LEDs (**Reference 1**). Because an LED is a current-controlled device, typical control circuits regulate the current through the LED to maintain uniform intensity. To optimize available power, users often operate the LEDs with a switching-converter circuit—either a buck or a boost converter—depending on the input-dc voltage. **Figure 1** illustrates the configuration of typical buck- and boost-converter white-LED-driver circuits. Adding the resistance, R, in series with the white LED sets the current through the LED. The value of the resistance depends on the desired LED current and the feedback voltage that the buck/boost converter requires. For example, the required resistance is 12Ω for a 100-mA average current through the LED and a 1.23V feedback voltage.

To reduce the power dissipated in the series resistance, engineers often employ the circuit configurations in **Figure 2**. In this configuration, the amplifier's gain reduces the power dissipated in the series resistor by a factor equal to the gain (**Reference 2**).

The circuit configurations in **figures 1** and **2** work well in regulating

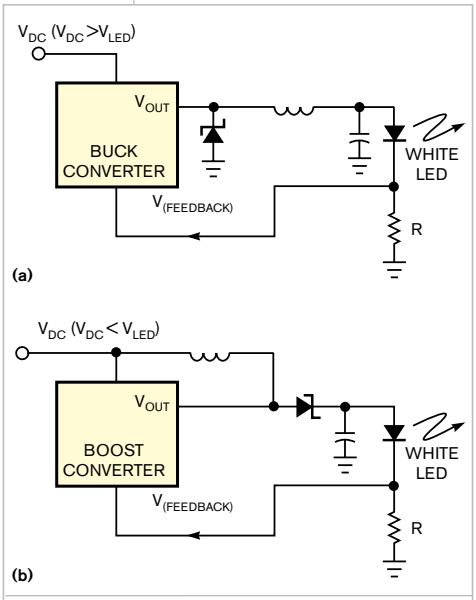

Figure 1 Depending on the input voltage, buck (a) or boost (b) regulators drive high-intensity white LEDs.

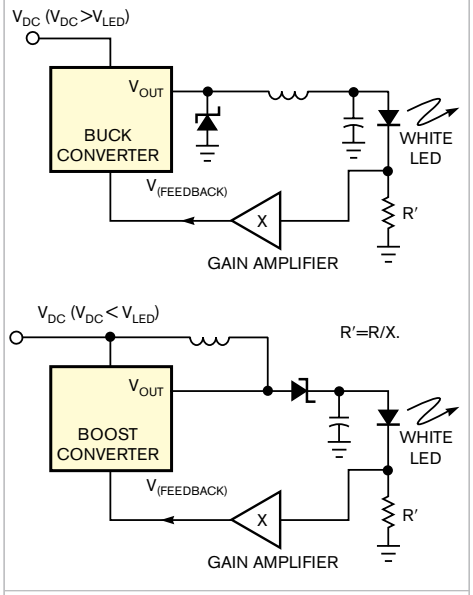

Figure 2 In these circuits, an amplifier gain reduces the power dissipated in the series resistor by a factor equal to the gain.

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the current through the LED, provided that the ambient temperature remains constant. However, white and other-color LEDs exhibit significant variation in luminosity as a function of temperature (**references 2** and **3**). Typical figures for variation in luminosity range from 40 to 150% for a 100°C change in temperature. Thus, if you expect the ambient temperature to vary, regulating only the current through the LED is an inefficient way to control the LED. An alternative is to use optical feedback to control the LED (**Reference 3**).

However, rather than use an expensive light sensor and amplifier circuit, you can use a suitable LED as a light sensor (**Reference 4**). **Figure 3** illustrates a controller for a white LED using an inexpensive buck-regulator IC, an adjustable LM2575. A 3-mm red LED in a transparent package senses the light from a 10-mm white LED. The white-LED spectrum is wide enough to excite the red LED as a sensor. For a test current of 60 mA through the white LED, the red-LED-sensor voltage is approximately 40 mV. Because the circuit uses the red-sensor LED's voltage as a feedback to the buck regulator, you must use an amplifier with a gain of approximately 30 because the internal reference voltage of the LM2575 buck regulator is 1.23V. Resistors R_1, R_2, and R_3 control the gain of the amplifier, which comprises an inexpensive LM358 dual op amp. The input-dc voltage powers the op amp. Resistors R_1, R_2, and R_3 have values of 270, 560, and 10 kΩ, respectively. Because R_2 is a variable resistor, changing its setting changes the gain and, thus, the current through the white LED. Thus, R_2 acts as brightness control. The amplifier gain ranges from 28 to 84, depending on the setting of R_2.

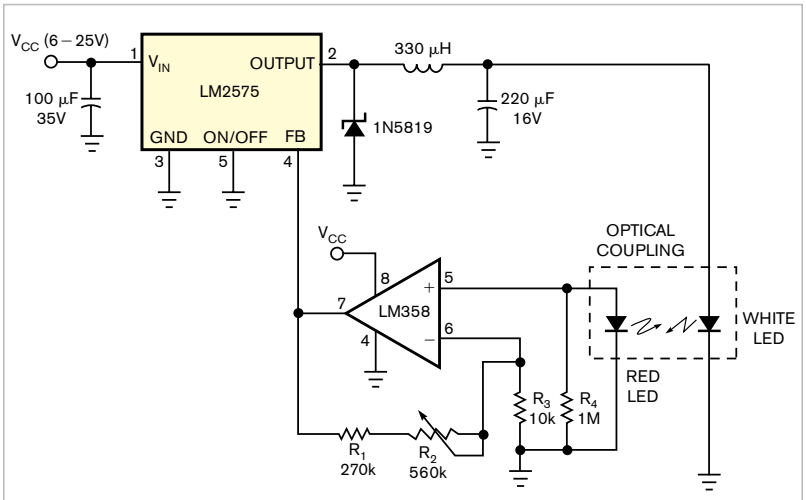

Figure 3 Use an inexpensive buck regulator and a red LED as a sensor for optical feedback to control the intensity of a white LED.

The red LED as a sensor mounts on the side of the white LED itself, thereby using only a fraction of the emitted light from the white LED. File the 3-mm red LED's top to get a flat surface, and then use a drop of superglue to secure the 3-mm red LED onto the side of the white LED.

The LM2575 buck regulator works by changing its duty cycle to regulate the output voltage. If the white-LED output light falls because of increased temperature, the red-LED sensor's voltage falls proportionately. The output of the red-LED sensor connects to the feedback input (Pin 4) of the regulator IC, and, in response, the regulator IC increases the duty cycle of the output voltage you apply to the white LED, thus stabilizing the light. In case of a decrease in ambient temperature, the white-LED light increases, and the regulator reduces the output voltage, which stabilizes the white-LED light. EDN

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Routines directly measure microcontroller-bus clock

Kerry Erendson, Bulova Technologies

The Freescale HC08 and newer HCS08 microcontroller families have versatile peripheral modules. Their clock generators are no exceptions. They range from the internal clock, which frees I/O pins, to external crystals or oscillators. Once you select the timing source, you have many options for controlling the final bus frequency. For instance, connecting a 32,768-Hz crystal to an MC9S08GB microcontroller allows you to use the FLL (frequency-locked loop) to generate many bus frequencies as high as 18.874 MHz.

Selecting the source, the divisors, and the FLL settings allows versatility but also can get complicated.

Once you write the bus-clock-initialization routine, you may want to verify that the bus is running at the speed you intend before moving on to the rest of the project. This Design Idea presents routines that output a square wave at exactly one-tenth the bus speed on any I/O port (**listings 1** and **2**). Just connect a frequency counter to this pin, and it will display your bus frequency. All you have to do is move the decimal point one place to the right. Once you verify the bus speed, you can confidently write the timer, serial-I/O, and other clock-dependent routines.

You need to write code only to first disable interrupts and disable the COP (common on-chip processor). In your bus-clock-initialization routine, be sure to initialize the I/O port you want to use as an output. Then, just jump to the toggle clock, which outputs the bus frequency divided by 10 until power-down. This Design Idea uses PB0 in the HC08 version and PD0 in the HCS08 version. You can use any available I/O port by altering the first line to identify the port and the second line to choose a bit. Also, this Design Idea names ports with the older notation PB, instead of today's more fashionable PTB. EDN

LISTING 1 CODE FOR HC08

```
;TOGCLK - toggle PB0 at 1/10th the bus clock freq. (square wave)
;(NEVER ENDS)

TOGCLK  LDHX #PB        ;put 16-bit address of PB in H:X
        LDA #$01        ;make whatever bits in PB that will toggle=1
TOG01   CLR ,X          ;2
        NOP             ;1
        NOP             ;1
        NOP             ;1
        STA ,X          ;2
        BRA TOG01       ;3
```

LISTING 2 CODE FOR HCS08

```
;TOGCLK - toggle PD0 at 1/10th the bus clock freq. (square wave)
;(NEVER ENDS)

TOGCLK  LDHX #PD        ;put 16-bit address of port PD in H:X
        LDA #$01        ;make whatever bits in PD that will toggle=1
TOG01   STA ,X          ;2
        NOP             ;1
        CLR ,X          ;4
        BRA TOG01       ;3
```

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Gain-of-two sample-and-hold amplifier uses no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When you need to simultaneously sample a signal and amplify the signal level, you can cascade a common gain-of-one sample-and-hold amplifier and an amplifier with a voltage gain of one. With some exceptions, such an amplifier has two external resistors (**Reference 1**). These resistors dissipate power even at the steady state of the sample-and-hold amplifier. In monolithic ICs, power dissipation and the consequent generation of heat from resistors are not the only items in the list of the drawbacks of external resistors. Integrating precise resistors within a silicon chip requires more processing steps, because such resistors are thin-film NiCr (nickel-chromium) or SiCr (silicon-chromium) elements. Manufacturers laser-trim these resistors to a tight tolerance value, contributing to the cost of an IC. Because these resistors occupy more chip area than standard signal-processing transistors,

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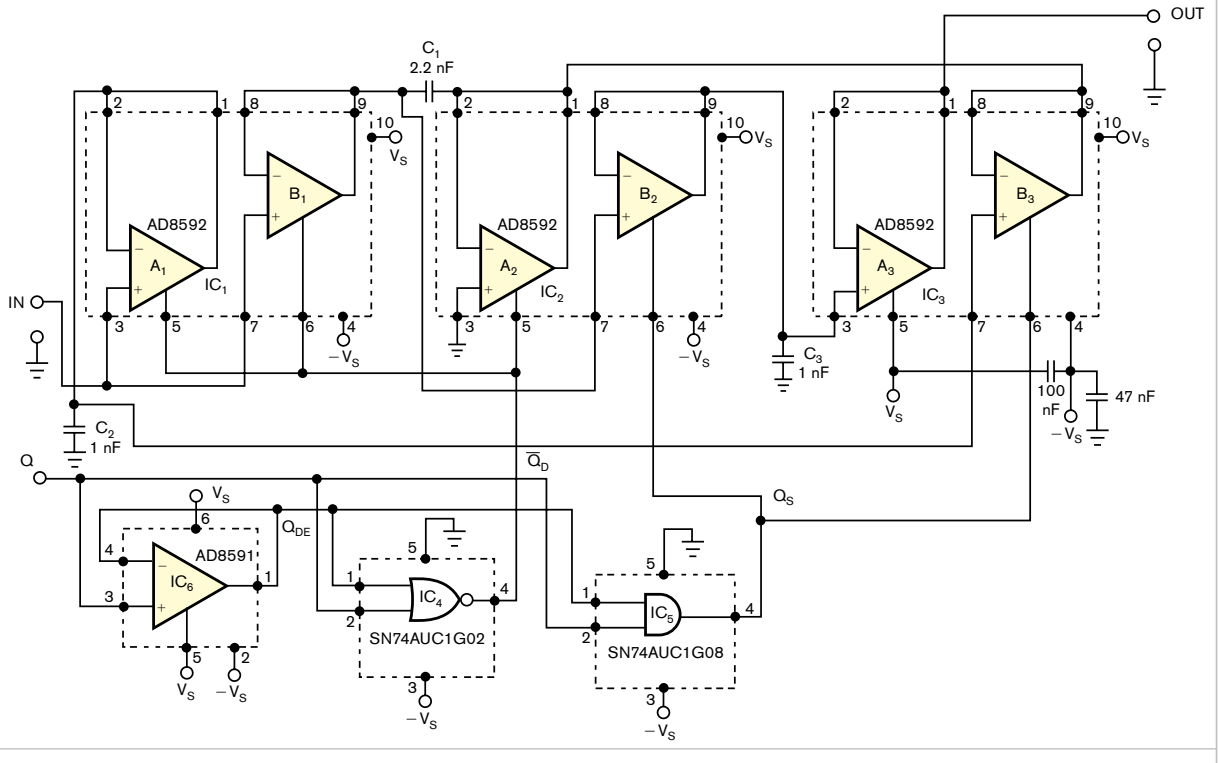

Figure 1 This sample-and-hold amplifier achieves a voltage gain of two by simultaneously tracking the input voltage on capacitors C_1 and C_2, "stacking" these capacitors within the sample interval, and storing the value of the stack's voltage in capacitor C_3.

the chip must be larger, further increasing the final cost. It's no wonder that designers of monolithic ICs as much as possible avoid using precision resistors.

If the required voltage-gain of a sample-and-hold amplifier is an integer, which it is in most cases, you can use an alternative way of increasing the magnitude of the output signal. For a voltage gain, G, the circuit can simultaneously track input voltage, V_{IN}, on temporarily ground-referenced tracking capacitors. Subsequently, an interruption occurs in tracking and cancels the ground referencing of G−1 of these capacitors. Meanwhile, the tracking capacitors stack on top of each other. The voltage on the stack is the sum of voltages of all of these capacitors, and it thus has the value of GV_{IN}. Upon the sample command, the constant voltage of GV_{IN} gets stored in the G+1 ground-referenced storing capacitor.

Figure 1 shows an example of a sample-and-hold amplifier with a voltage gain of two. Voltage followers control the potentials on capacitors C_1, C_2, and C_3 using their shutdown function. The design uses Analog Devices' (www.analog.com) AD8592 dual op amps because their output-leakage current in shutdown mode can be lower than 10 pA (**Reference 2**). You can follow the operation of the sample-and-hold amplifier with the timing diagram (**Figure 2**). The external logic-control signal, Q_S, is at a low level, and the C_1 and C_2 capacitors simultaneously track the voltage at its input. The shutdown inputs of followers A_1, B_1, and A_2 are tied together. At $\overline{Q}_D$=high, they are enabled, so the input voltage appears at the outputs of A_1 and B_1, and no voltage appears at the output of A_2. After the high-to-low transition of $\overline{Q}_D$, a dead slot follows with each of the controlled followers turning off. At Q=high, B_3 and B_2 turn on. Thus, the voltage in C_2 appears at the output of B_3. The potential of the input voltage occurs, therefore, at the lower node of C_1 (Pin 2 of IC_2). Because C_1's voltage has the same value as the input voltage and the output voltage, the B_2 follower is $2V_{IN}$. Capacitor C_3 thus charges to the voltage of $2V_{IN}$. After the high-to-low transition of $\overline{Q}_S$, another dead slot follows to prevent any cross-conduction in the circuit. At the next high-to-low transition of Q_S, the process repeats.

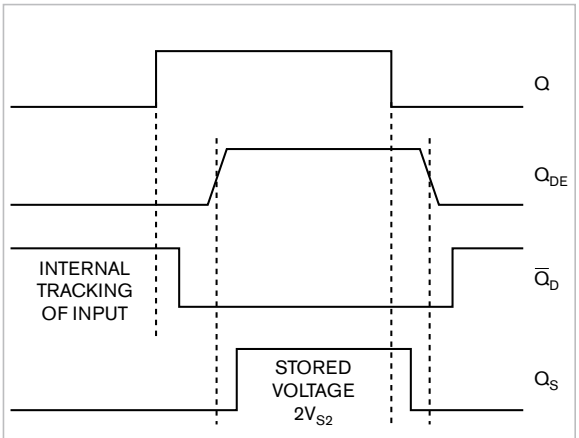

Figure 2 The external-control-logic signal, Q, splits into two quasicomplementary signals, Q_S and $\overline{Q}_D$, to avoid any internal cross-conduction in the amplifier.

The A_3 follower serves as an impedance converter, outputting the voltage in C_3. The single NOR and AND gates, together with op amp IC_6 functioning as a delay line, modify the single external-logic-control signal to create the properly timed internal logic signals, $\overline{Q}_D$ and Q_S.

For a noise analysis, assume that the noise characteristics of each of the followers are the same—namely, the standard deviation, σ_A, of the random component of the output voltage of a single follower. At the end of the tracking interval, both C_1 and C_2 charge to the input voltage. The standard deviation of the V_{C2} voltage is σ_A only for the A_1 follower. The standard deviation of V_{C1} voltage is, however, $\sqrt{2}\sigma_A$, because C_1 charges through two series-configured followers, B_1 and A_2. The standard deviation of $V_{C1}+V_{C2}$ voltage thus has the value of $\sqrt{3}\sigma_A$. The voltage of $V_{C1}+V_{C2}$ applies to C_3 through two followers in a cascade, B_3 and B_2, within the sample interval. Further, the V_{C3} voltage applies to the output through the A_3 follower. Because all of the noise sources are mutually independent and because they all effectively act in series, the standard deviation of the output voltage is $\sigma_{OUT}=\sqrt{6}\sigma_A$. Increasing the integer gain to the value of G yields $\sqrt{3G}\sigma_A$. You now pose an RSNR (relative signal-to-noise ratio) as gain, G, over a relative increment of noise at the output, yielding:

$$RSNR = \frac{G}{\frac{\sigma_{OUT}}{\sigma_A}} = \sqrt{\frac{G}{3}}.$$

For the sample-and-hold amplifier in **Figure 1**, the RSNR equals 0.8165, meaning that the noise characteristics of the circuit are slightly worse than those of a single follower. For a gain of three, the RSNR has the value of one, and, starting from a gain of four, at which the RSNR is 1.155, it gradually rises with increasing gain. The conclusion is that, for voltage gains of four or higher, the noise characteristics of the sample-and-hold amplifier are better than those of a single follower. EDN

IT'S NO WONDER THAT DESIGNERS OF MONOLITHIC ICs AS MUCH AS POSSIBLE AVOID USING PRECISION RESISTORS.

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Circuit for measuring motor speed uses low-cost components

R García-Gil, J Castelló, and JM Espí,
Escola Tècnica Superior d'Enginyeria, University of Valencia, Spain

This Design Idea uses a microcontroller, a 16×2-key LCD, and a rotary encoder to measure and visualize the speed of a motor (**Figure 1**). You measure the rotor speed of the motor using an incremental encoder coupled to the motor shaft, which provides quadrature pulses with a frequency proportional to the rotor speed. The 1024-pulse rotary encoder is the RS-32-0/1024ER.11KB from Hengstler (www.hengstler.com). You can calculate the rotational speed of the motor, ω_R, by counting the number of revolutions that the encoder axis, n_V, makes during a certain time period, t_P. You calculate n_V by counting the number of pulses, n_P, that the encoder generates during this fixed period, t_P: $n_V=n_P/1024$ for this encoder. And the rotational speed is

$$\omega_R = \frac{60 \times n_V}{t_P} = \frac{60 \times n_P}{t_P \times 1024} = \delta \times n_P,$$

where $\delta=60/(t_P\times1024)$ rpm represents the resolution of the measured speed. To obtain a resolution of 1 rpm for this application, the fixed period you use as a timebase is 60/1024=58.59 msec. In this Design Idea, a low-cost microcontroller, the PIC16F873, IC_1, from Microchip (www.microchip.com) performs these operations. This microcontroller also drives the LCD, IC_2, which shows the rotational speed in rotations per minute.

In a similar fashion to the circuit in **Reference 1**, you apply the quadrature pulses of the encoder to IC_1's RB0/INT input, which generates a high-priority interrupt at the rising edge of the pulse. These interruptions allow you to compute n_P by increasing a counter, which initializes after it reaches fixed period t_P. Moreover, the microcontroller's internal 8-bit timer, Timer 0, registers t_P, which generates a t_M (timer interruption) each 286 μsec for a clock frequency, f_{CLK}, of 14.3 MHz: $t_M=4\times2^8/f_{CLK}/4=286$ μsec. This calculation means that fixing the timebase, t_P, requires 205 timer interruptions (t_P/t_M).

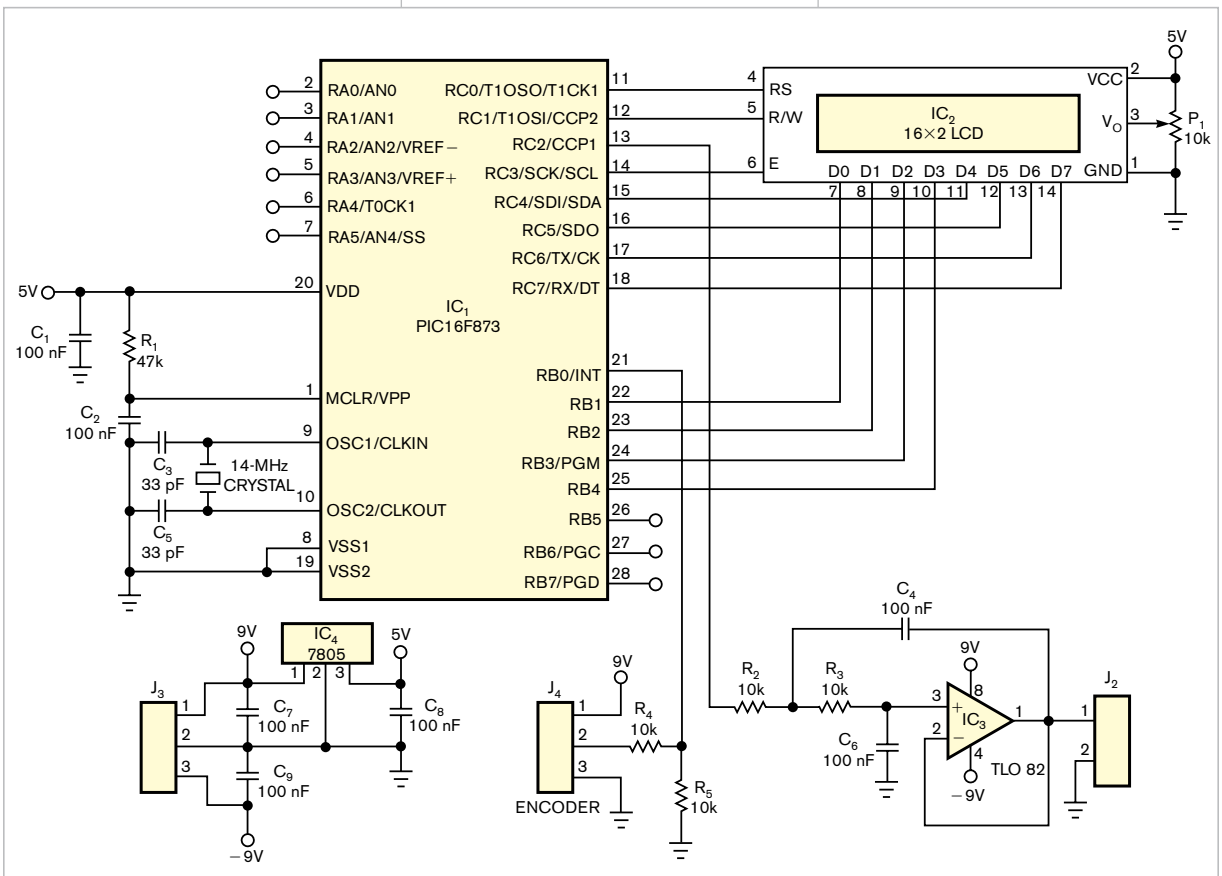

Figure 1 This circuit for measuring a motor's speed includes a PIC microcontroller and an LCD. It also provides an analog-to-digital conversion without an ADC.

When the counter reaches this time, the count, n_p, determines the rotational speed, according to the **equation**. Finally, this value appears on the screen of the LCD.

In addition, a digital-to-analog conversion is necessary if the control system must measure the rotational speed. You can do this conversion without adding an expensive DAC by applying a PWM (pulse-width-modulation) output of the microcontroller to a lowpass filter comprising R_2, R_3, C_4, C_6, and IC_3. The frequency of the PWM signal is 20 kHz, and the cutoff frequency of the lowpass filter is 160 Hz, which is much lower than the PWM frequency. In this design, the maximum duty cycle of the PWM signal corresponds to a rotational speed of 1500 rpm.

You can download the source code for IC_1's program from the online version of this Design Idea at www.edn.com/071108di1 and assemble the software with MPLab from www.microchip.com. You can alter constants within the software according to the encoder you use and your required resolution from the **equation**.EDN

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Battery monitor also enables constant-power-boost converter

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

Some microcontrollers permit operation below a supply voltage of 3V. This feature allows powering directly from a 3V alkaline or lithium battery without the voltage drop and leakage current of a regulator. It is important to monitor the battery voltage to ensure system integrity, and you can also use this information for system purposes. The circuit in this Design Idea maintains constant power to a white-LED-display backlight by adjusting the duty cycle of a boost-power converter. However, an ADC normally needs a fixed voltage reference (**Figure 1**), which would require two input pins for this function. This Design Idea turns the ADC's architecture inside out, providing the voltage-reference function using no extra pins.

The monitor circuit in **Figure 2** integrates an ADC within the microcontroller. The converter uses the battery voltage as a reference voltage. The principle is the opposite of normal: You want to measure a fixed voltage using a variable-voltage reference (the battery). For an 8-bit converter, the result for this example is $(1.18V/V_{BAT})\times256$. Note that a high value indicates that the battery voltage is low. Also, you can use the microcomputer pin that connects to the reference for another purpose. This example normally uses Pin 6 as an output to the pulse-indicator LED, LED_1. However, by briefly changing the port direction to analog-input mode, you can complete the battery-measurement operation, including settling, sampling, and conversion, in less than 0.1 msec.

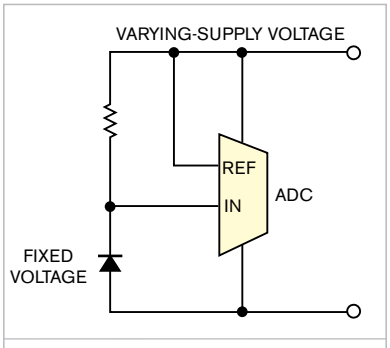

Figure 1 An ADC normally needs a fixed voltage reference, which would require two input pins for this function.

The example uses a PIC12F683 microcontroller and a voltage reference of 1.25V for the LM4041. R_1 biases the reference. R_2 ensures that the microcontroller output can rise to 3V to turn on transistor Q_1 without damag-

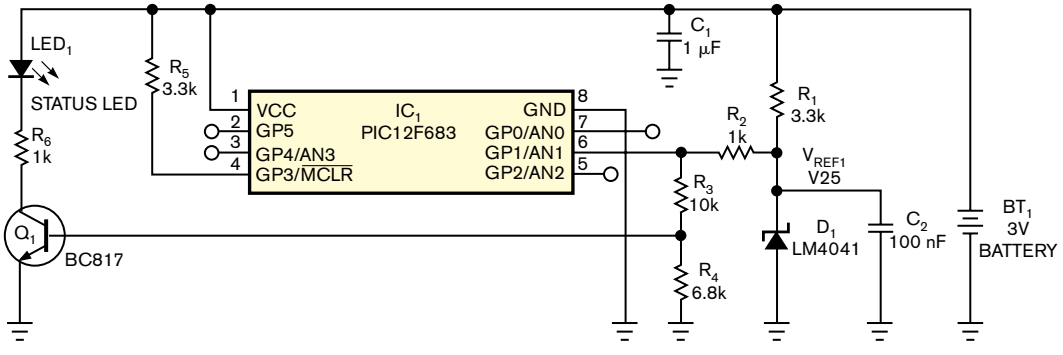

Figure 2 This monitor circuit integrates an ADC within the microcontroller. In this circuit, the converter uses the battery voltage as a reference voltage.

ing D_1. Resistors R_3 and R_4 ensure that the transistor is extinguished during the battery measurement. R_2, R_3, and R_4 introduce some attenuation, which you must take into account.

Figure 3 shows the monitor with the addition of a constant-power voltage-booster circuit. The PWM (pulse-width-modulation) output of the microcontroller drives the converter. For constant power from the booster, the required duty cycle linearly relates to the ADC's converted value.

Battery technologies vary in their discharge characteristics. Alkaline batteries have high capacity but drop their open-circuit voltage as they operate. The open-circuit voltage can provide a good estimate of battery charge. However, alkaline batteries also have internal resistance and exhibit a recovery phase after supplying a heavy load. The resistance increases with low temperature and low battery charge. To determine the battery's state, you can take measurements before and immediately after a high-current load is active. This approach allows estimation of both internal resistance and battery charge. EDN

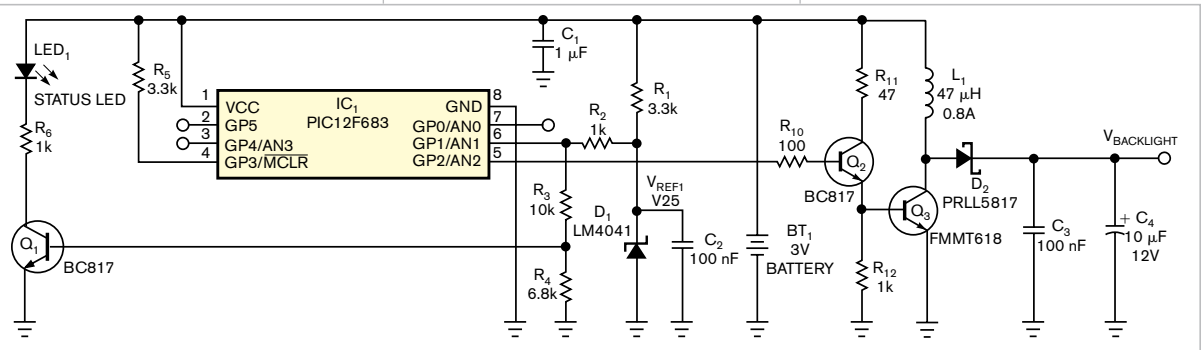

Figure 3 This monitor adds a constant-power voltage-booster circuit. The PWM output of the microcontroller drives the converter.

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Measure power-line distortion with a mixed-signal-THD analyzer

John R Ambrose, Mixed Signal Integration, San Jose, CA

Because of the performance of compressors and other inductive loads, it becomes more important to monitor the distortion on a power line. With alternative power sources, such as wind or solar, a distorted 60-Hz sine wave is more likely to be present. To measure this distortion, you can use a mixed-signal-THD (total-harmonic-distortion) analyzer to monitor the fundamental frequency amplitude and the second-, third-, fourth-, and fifth-harmonic content of the input signal. The analyzer, from Mixed Signal Integration (www.mix-sig.com) includes five bandpass filters and two op amps. The op amps provide gain and continuous-time filtering. The

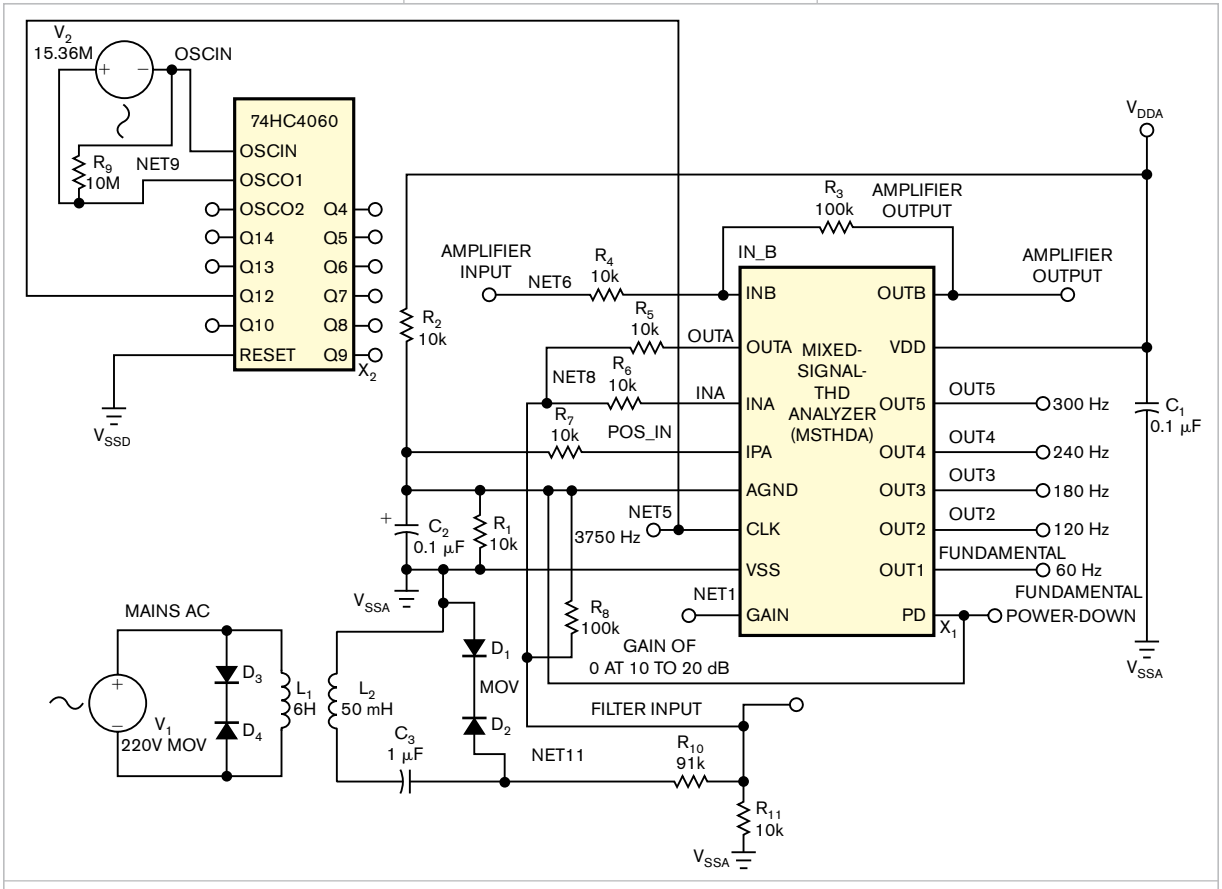

Figure 1 This mixed-signal-THD analyzer monitors the fundamental frequency amplitude and the second-, third-, fourth-, and fifth-harmonic content of the mains-input voltage.

analyzer also has digital-gain control for measurements in which the input amplitude is 10 or 20 dB lower than nominal: 2V p-p. The outputs of the analyzer are analog. Depending on the display that an application requires, you could tie the outputs to a bar-code interface, such as the LM3915 for 3-dB steps, or interface them with a multiplexer on a microcontroller for a digital readout.

Figure 1 shows the connections of the analyzer to the mains supply. A "wall-wart" transformer reduces the 120V mains voltage to 9V ac. This transformer provides 1500V isolation from primary to secondary and has low-distortion performance. The resistors in the divider act as fuses in case of a large surge voltage, and they reduce the voltage you apply to the analyzer. The back-to-back diode clamp protects the analyzer during momentary overvoltage conditions. In addition, a 220V MOV (metal-oxide varistor) across the transformer's primary protects the transformer. The analog ground centers on 2.5V and is derived from a 100-kΩ resistor-divider network. A 0.1-μF capacitor provides ac filtering. A 74HC4060 operates at 15.360 MHz; the divide-by-4096 (Q12) output connects to the analyzer's input-clock signal and supplies the clock for the device's switched-capacitor filters. EDN

Wireless "battery" energizes low-power devices

Carlos Cossio, Santander, Spain

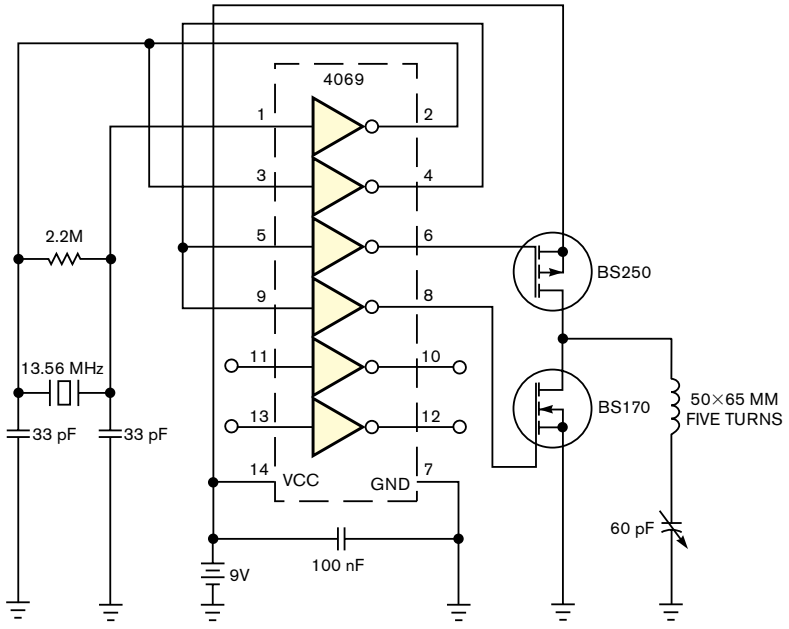

Figure 1 A simple 13.56-MHz oscillator energizes an antenna coil, broadcasting power to the receiving circuit in Figure 2.

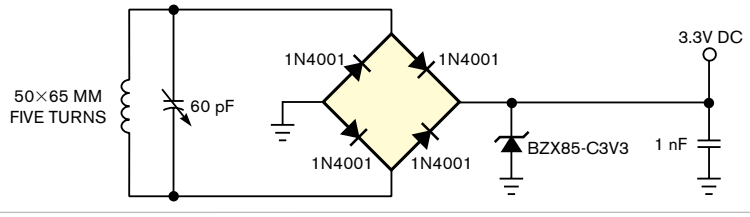

Figure 2 This receiver rectifies the signal from the oscillator in Figure 1, powering low-current consumer gadgets.

Wireless connectivity is a growing trend in portable consumer gadgets. Unfortunately, designs cannot achieve true mobility because of short battery life, so the power cord still must connect the device to the power grid to get the required energy or to recharge the batteries. However, thanks to the low-power requirements of today's electronic devices, it is feasible to power them wirelessly. This Design Idea describes a simple approach to wirelessly transmitting energy to low-power devices at distances as great as 10 cm. This design uses the resonant-inductive-coupling principle working at 13.56 MHz. The system comprises the RF-power transmitter and the RF-power receiver.

Figure 1 shows the transmitter circuit, which incorporates a 13.56-MHz oscillator. The oscillator encompasses a CMOS 4069 inverter using power from a 9V battery to get a wide voltage swing. The oscillating signal then passes through a push-pull output stage comprising two small-signal MOSFETs to get enough current in the output coil. Finally, the output signal broadcasts to the outside by means of a serial-resonant-LC circuit incorporating a coil and a 60-pF variable capacitor tuned to 13.56 MHz.

Figure 2 shows the receiver circuit, which comprises an LC network tuned to a carrier frequency of 13.56 MHz. It includes a coil and a 60-pF variable capacitor in parallel with the coil. A full-bridge rectifier comprising four 1N4001 diodes rectifies RF power. Rectification efficiency is approximately

50%. Reaching 3.3V of output voltage requires a 9V p-p ac voltage across the coil's pins. A shunt regulator incorporating a 3.3V zener diode provides voltage clamping beyond 3.3V to prevent power-level variations with distance. Finally, a 1-nF capacitor after the full-bridge rectifier decouples the power supply. The two coil antennas use five turns of 1-mm enameled-copper wire in a rectangular, 50×60-mm shape.

As an improvement, if your application requires greater distance, you can increase the power supply to 15V to get a greater voltage swing on the transmitter coil, thanks to the CMOS technology the oscillator design employs. In addition, designing a larger-coil antenna in the transmitter and the receiver sides helps to increase the distance of operation. EDN

Solid-state analog-data recorder runs for 7.4 days

S Vinay Kumar, Mysore, India

The solid-state data recorder in **Figure 1** can continuously record the temperature for approximately 178.42 hours, or 7.434 days. The LM35DZ transducer converts the temperature to an analog-voltage equivalent. The analog voltage then goes to the HI5812 ADC, and the digital data gets stored in the nonvolatile DS1270W SRAM at a rate of 3.265 samples/sec. To retrieve the analog signal, the digital data in memory goes to the DAC08. The output of the DAC then goes to the current-to-voltage converter, then to analog switch MC14066, and finally to the output buffer. The address generator is a simple counter, the MC14040. A record-and-play circuit uses an MC14049, and analog switches control the read and write states of the nonvolatile SRAM. A 10-kΩ potentiometer sets the reference voltage of both the ADC and the DAC.

Pressing and releasing the reset button once causes the recording or playing to start from the beginning of the memory location; the recording or playing function depends on the position of the record-and-playback switch. If you close the record-and-playback switch, recording takes place; if the switch is open, playing occurs. EDN

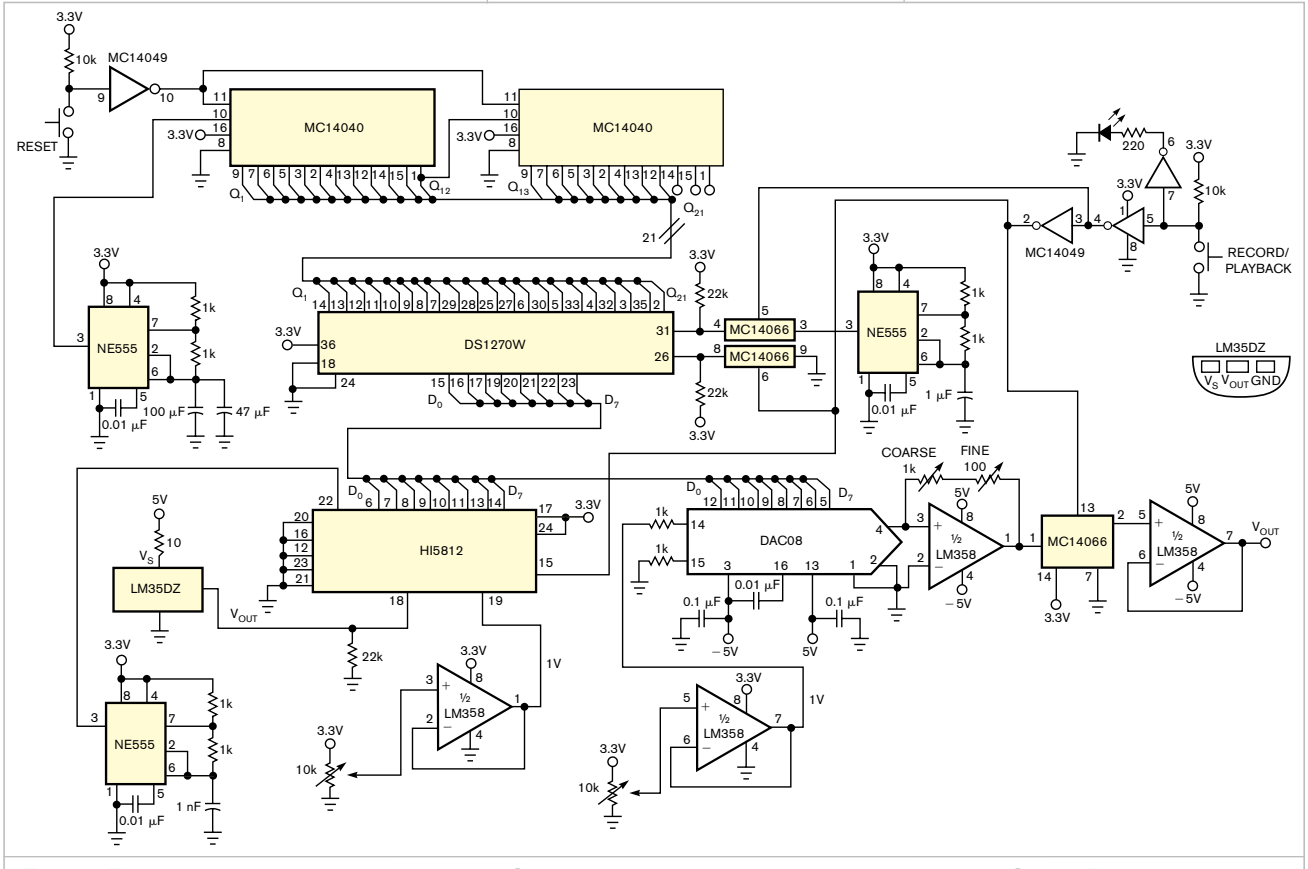

Figure 1 This solid-state data recorder uses an ADC to digitize data, which gets stored in a nonvolatile SRAM. To read back the analog data, the memory's contents shift to a DAC, depending on the state of the record-and-playback switch.

Wideband peak detector operates over wide input-frequency range

Jim McLucas, Longmont, CO

This Design Idea builds on a previous one (**Reference 1**) to realize a precision peak detector with a bandwidth of 15 to 30 MHz or more, depending on the maximum input-signal level of your application. The crucial feature of this Design Idea is an ultrafast comparator that provides the high slew rate and low propagation delay that this application requires. The comparator in this design is the Analog Devices (www.analog.com) AD8561, a 7-nsec device (**Reference 2**). This peak detector provides accuracy from 100 Hz to more than 14 MHz at input-signal levels of 100 mV p-p to 6V p-p. At higher frequencies, the maximum usable input-signal level decreases. The circuit exhibits an accuracy of ±3% over much of the input-level range. Also, its high input impedance of about 100 kΩ in parallel with 3 pF does not significantly load the circuit under test in many applications; 3 pF results in an impedance of 3.5 kΩ at 15 MHz.

Referring to **Figure 1**, the high-input-impedance buffer comprising IC_1 and its associated components provides the ac signal to the ultrafast comparator, IC_3. The output of IC_1 centers on 0V dc by the action of op amp IC_{2A} and its associated components, which sample the dc level at Pin 6 of IC_1 and then provide a dc-correction voltage to Pin 3 of IC_1. This action virtually eliminates the effects of IC_1's input-offset voltage and input-bias currents. R_1, R_4, and C_1 provide a small amount of gain boost as the frequency increases to 25 MHz, and C_5 then begins to roll off the gain.

The input signal capacitively couples to the input buffer, so, for proper operation, the input-ac signal must have a symmetrical waveform, such as a sine wave. An unsymmetrical waveform has a shift in its peak value after passing through C_2, and, as a result, the output of the peak detector will be inaccurate.

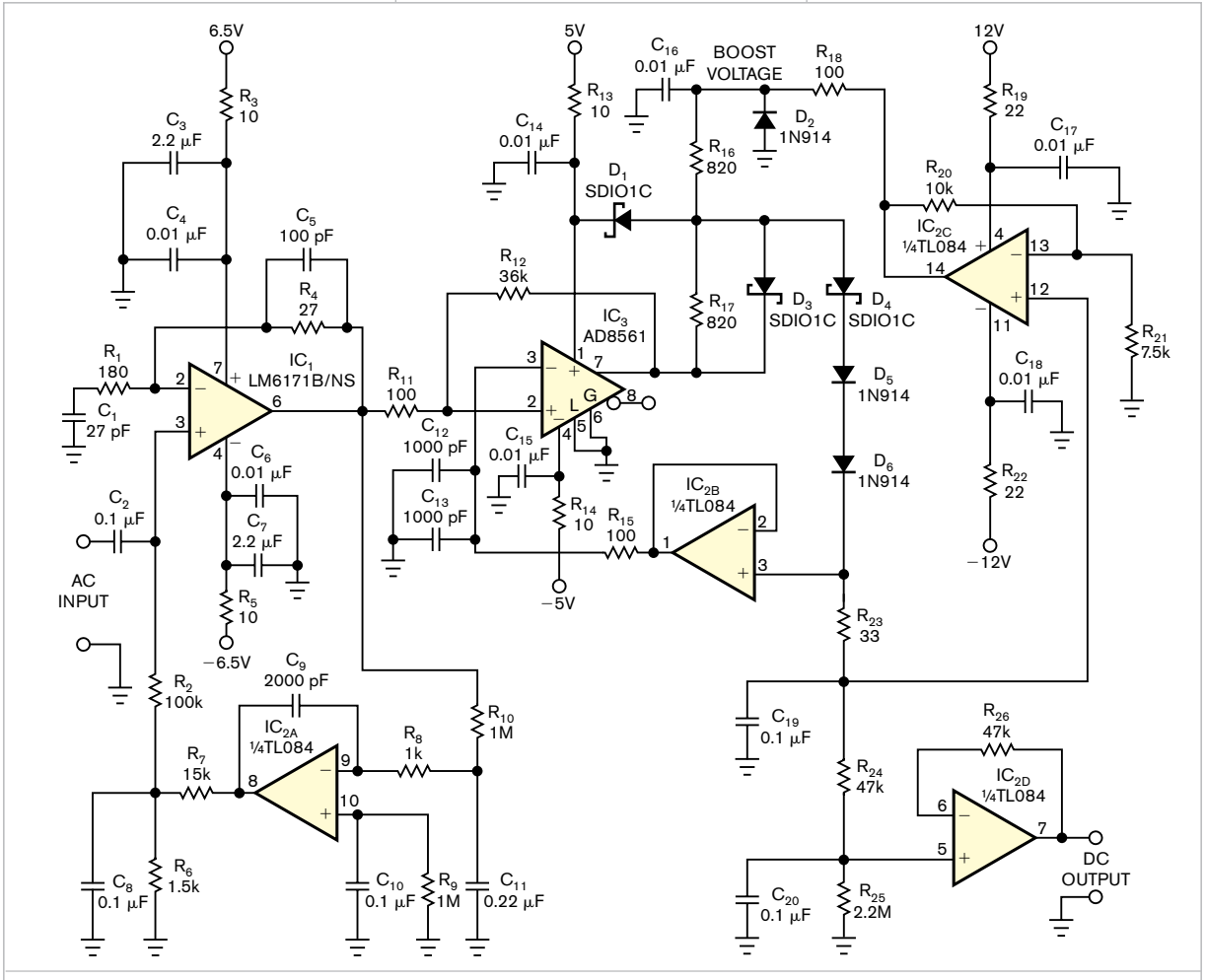

Figure 1 This precision peak detector uses an ultrafast comparator to achieve high accuracy over a wide input-frequency range.

The output of comparator IC_3 swings high when the input at Pin 2 is higher than the dc level at Pin 3. This action, in turn, charges holding capacitor C_{19} through R_{17}, D_4, D_5, D_6, and R_{23}. When the voltage on C_{19} is higher than the peak signal level at Pin 2 of IC_3, the comparator stops providing charging pulses at its output. At equilibrium, the comparator provides output pulses with the correct amplitude and width to maintain the voltage on C_{19} at approximately the peak level of the input signal. The high-input-impedance dc buffer, IC_{2B}, minimizes the discharging of C_{19} between charging pulses.

The network comprising R_{24}, R_{25}, and C_{20} filters and attenuates the dc output by 2.1%. This attenuation is necessary because the output tends to be slightly higher than the actual peak level of the input signal at Pin 3 of IC_1. The circuitry comprising IC_{2C} and its associated components provides a novel feature: a voltage boost at Pin 14 of IC_{2C} as the voltage on holding capacitor C_{19} increases. The circuitry then applies this voltage boost to R_{16}, which in turn causes the voltage swing at the junction of R_{16} and R_{17} to increase as the charge on C_{19} increases. This action causes the amplitude of the pulses driving D_4 to increase. This action maintains a relatively constant drive to C_{19} as its charge increases.

Diode D_1 keeps the voltage at the output of IC_3 from exceeding its supply voltage. Diode D_2 keeps the boost voltage from going to a large negative level at start-up, which could cause the circuit to latch up. The switching action of the comparator and diode D_3 prevents latch-up due to a large positive-boost transient. This circuit exhibits no indication or tendency for instability. The maximum input signal is 6V p-p because of the input common-mode-voltage specification of the AD8561 comparator. The supply voltages for the input buffer are ±6.5V to avoid the possibility of severely overdriving the comparator.

You can improve the precision of the circuit by substituting a 100-kΩ potentiometer for R_4 to provide an output-level adjustment, and a dc-offset adjustment would improve accuracy at low signal levels.

This circuit used a 300-MHz-bandwidth oscilloscope to make the performance measurements. As a result, the data in **Table 1**, which is available in the online version of this Design Idea at www.edn.com/071122di1, may include some measurement errors. Therefore, take the results in the **table** as representing the circuit's performance rather than as precise data. The data is simply the result of the best equipment on hand when the measurements were made. EDN

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1 McLucas, Jim, "Precision peak detector uses no precision components," *EDN*, June 10, 2004, pg 102, www.edn.com/article/CA421510.
2 "AD8561 ultrafast 7 ns single supply comparator," Analog Devices, www.analog.com/UploadedFiles/Data_Sheets/AD8561.pdf.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Filter simplifies software-defined radio

John Wendler and Ray Tremblay, Tyco Electronics,
M/A-Com Wireless Systems, Lowell, MA

SDRs (software-defined radios) provide enormous flexibility, permitting you to change modes or waveforms at will. This Design Idea focuses on the "exciter" portion of a moderate-bandwidth SDR (**Figure 1**). The RF carrier or transmitter IF enters the quadrature modulator, and the modulated output exits for further frequency translation or amplification, depending on the details of the design. The DSP section generally works with analytic signals—in this case, signals with real and imaginary parts—at baseband. These signals may have started out as a voice speaking into a microphone that attaches to an ADC, or they may have started out as data from a computer. Regardless of the signals' origin, the DSP performs calculations on the stream of numbers, performing filtering, perhaps adding signaling tones or packetizing the data, and converting the stream into the final I and Q modulating signals. For moderate bandwidths, a stereo sigma-delta DAC or codec provides the conversion to analog signals and performs some additional filtering on the signal. Such filtering is often necessary because the quadrature modulator comprises a pair of mixers. These mixers translate any noise at baseband frequencies directly to the modulator's output.

Output noise is problematic. The FCC (Federal Communications Commission) sets spectral masks or adjacent-channel-power-ratio requirements on some services, such as land mobile radio. These requirements govern the allowed spectrum of a transmission and vary according to the bandwidth of the channel and the frequency of transmission. Their function is always the same, however: They limit the interference to other users on nearby channels to the transmitter. Meeting the spectral mask is a regulatory requirement; you cannot certify a radio without proving that it meets this requirement, and, without this certification, you cannot legally sell it. **Figure 2** shows a sample spectral mask, 47 CFR 90.210 G, with a normalized X axis to show the offset from the center of the channel and a normalized Y axis to show the unmodulated carrier output. This mask applies to the 800-MHz SMRS (specialized-mobile-radio service) in which channels are 25 kHz apart but signals can occupy only 20 kHz.

The unmodulated carrier first transmits at the center of the mask, and the top of the mask adjusts to correspond with the output power of the transmitter. You then turn on the modulation, thereby spreading the spectrum. The resulting spectrum must fall below the mask line in all places.

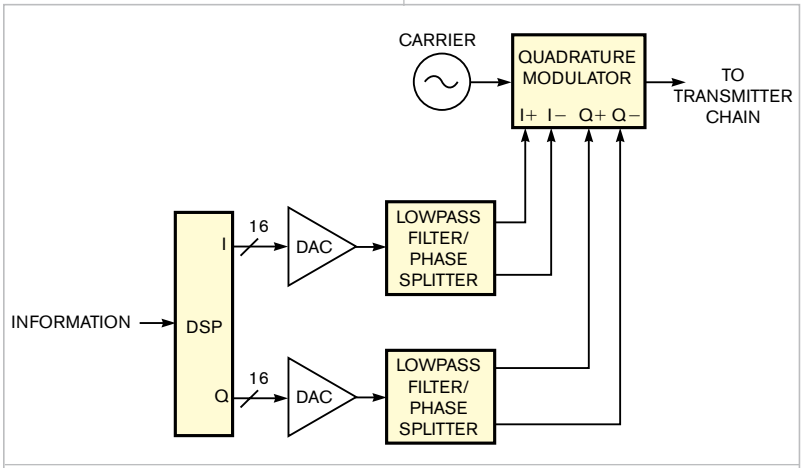

Figure 1 A pair of DACs converts the baseband signal from a DSP into I and Q signals for the quadrature modulator of a software-defined radio.

DIs Inside

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A close examination of **Figure 2** shows some interesting features. On the carrier trace, the sampling-frequency spurs appear at ±19.2 kHz away from the center. The modulated spectrum is also interesting. The filter in the sigma-delta DAC causes the nearly vertical roll-off at approximately ±10 kHz. The mounds that appear around ±12 kHz and gradually roll off are spectral regrowth, which nonlinearities in the high-power amplifier cause.

Many moderate-bandwidth SDRs need a translator between the sigma-delta DAC's single-ended output and a typical balanced-input quadrature modulator. It is frequently desirable to follow up the DAC output with a hardware filter that removes the DAC's high-frequency noise and ensures compliance with spectral-mask requirements. Further complicating things, the optimal common- and differential-mode output voltages of the DAC are likely to differ from those that the modulator requires. An easy scaling factor does not relate common- and differential-mode voltages.

Handling all of these considerations with a conventional approach can require as many as four operational amplifiers with multiple filter sections per I or Q channel. The filters require close component matching to guarantee that carrier and single-sideband suppression—key measures of quadrature-modulator ideality—do not degrade as a function of baseband frequency. The Linear Technology (www.linear.com) LTC1992, on the other hand, addresses the problem in a single section. Linear shows a fully balanced approach to the problem in its data sheet (**Reference 1**).

It turns out, however, that a fully balanced approach is unnecessary. The circuit in **Figure 3** has excellent phase and amplitude balance between the output channels and eliminates some critical component-matching requirements. Pin 2 is set for the desired common-mode output voltage, and the DAC's midpoint voltage connects through an input resistor to Pin 8. Note that any mismatch between the input voltage and the midpoint voltage appears at the outputs and causes asym-

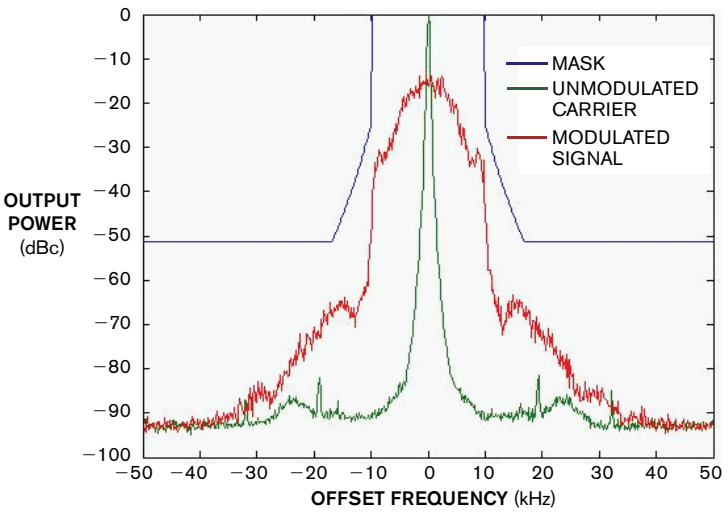

Figure 2 A sample spectral mask, 47 CFR 90.210 G, has a normalized X axis to show the offset from the center of the channel and a normalized Y axis to show the unmodulated carrier output.

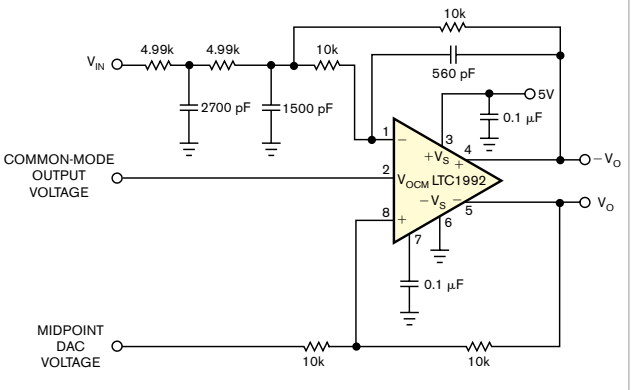

Figure 3 This circuit has excellent phase and amplitude balance between the output channels and eliminates some critical component-matching requirements.

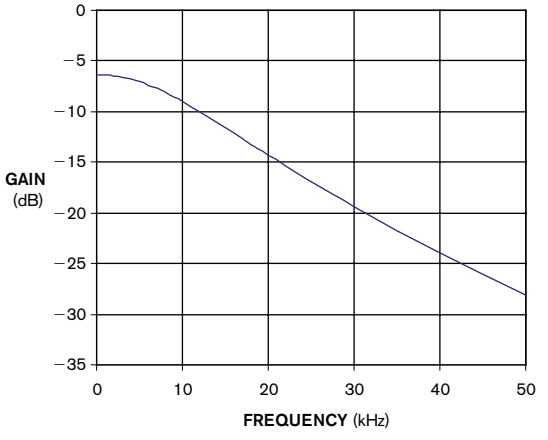

Figure 4 The measured frequency response of the positive channel with respect to ground shows an apparent 6-dB loss as a result of looking at only half the differential-output voltage; when you examine the full balanced output, the net gain is 0 dB.

metrical swing. This application bypasses Pin 7. The filter is a passive single-pole circuit cascaded with an inverting Sallen-Key filter, but other topologies are feasible.

Figure 4 shows the measured frequency response of the positive channel with respect to ground. The apparent 6-dB loss is a result of looking at only half the differential-output voltage; when you examine the full balanced output, the net gain is 0 dB. **Figure 5** shows the measured deviation from an ideal equal-amplitude, 180° phase shift between the positive and the negative outputs. The agreement in the critical 300-Hz to 3-kHz range is less than 0.1 dB and 0.1°. Even at 50 kHz, the error is less than 0.5 dB and 1°. EDN

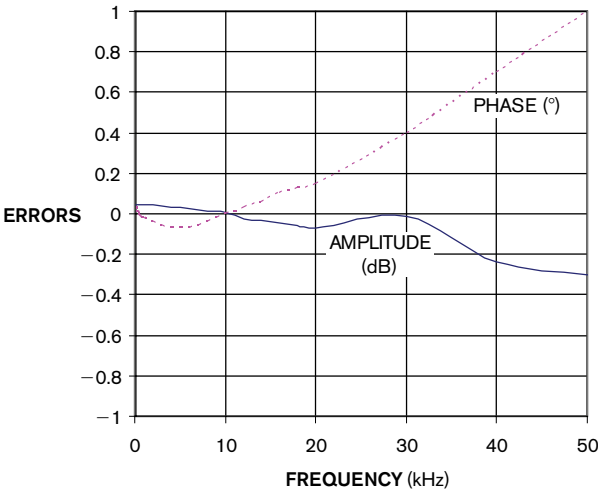

Figure 5 The measured deviation from an ideal equal-amplitude, 180° phase shift between the positive and the negative outputs shows agreement of less than 0.1 dB and 0.1° between 300 Hz and 3 kHz.

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1 "LTC1992: Fully Differential Input/Output Amplifier/Driver," Linear Technology, July 2003, www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1154,C1009,C1126,P2348,D3455.

ACKNOWLEDGMENT

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Thermoelectric-cooler unipolar drive achieves stable temperatures

W Stephen Woodward, Chapel Hill, NC

Most engineers know about the solid-state refrigerators called Peltier devices or, more commonly, TECs (thermoelectric coolers) and how they can actively cool temperature-sensitive electronic components, such as optical detectors and solid-state lasers. It's also common knowledge—although perhaps less so—that TECs are bidirectional heat pumps and can therefore both heat and cool, depending on the direction of the supplied drive current. TECs can therefore serve as the basis for precision microthermostats, maintaining a predetermined temperature against ambient-temperature excursions that range both above and below the setpoint.

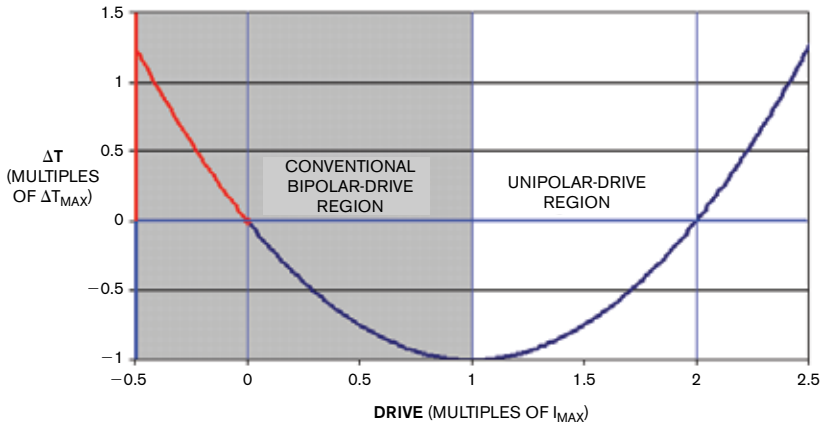

Figure 1 This plot of temperature versus maximum current shows that operating a TEC at high currents achieves heating and cooling from a unipolar drive.

The rub is that bidirectional-TEC drive tends to be an inconvenient design problem. It requires either dual bipolar power supplies or relatively complex H-bridge-drive output circuits involving arrays of power transistors that selectively reverse the TEC excitation as the required direction of heat flow dictates. But an alternative method offers advantages whenever simplicity matters more than efficiency. This Design Idea presents a novel approach to bidirectional-TEC-temperature control that avoids both the inconvenience of dual power supplies and the complexity of bidirectional drive. It works by exploiting a little-known quirk of all TECs: the inherent reversal of net heat flow at unconventionally high levels of drive current.

The specifications of every TEC include I_{MAX}, the drive current that results in maximum net cooling. Plotting heat transfer versus drive current relative to I_{MAX} results in a typical parabolic curve (**Figure 1**). The left-hand, gray half of the plot in the **figure** shows the usual bipolar TEC's operating region, which confines drive current to the range of $-0.5\times I_{MAX}<I<I_{MAX}$. The right-hand half shows the region of interest, in which the same bipolar-temperature excursion results from unipolar-current drive: $I_{MAX}<I<2.5\times I_{MAX}$. Operation of the TEC in this second operating region thus allows bidirectional temperature control without the complexity of bidirectional-current drive.

Figure 2 shows an implementation of the concept in a high-performance PID (proportional-integral-derivative)-feedback loop. The component count is less than one-fourth that of a comparable bipolar-drive design. Feedback stability is robust, and settling time is short. The downside is a current draw as much as 150% higher than that for a conventional bipolar driver, which limits the technique to applications in which power consumption and heat dissipation aren't critical priorities and small TECs are adequate. EDN

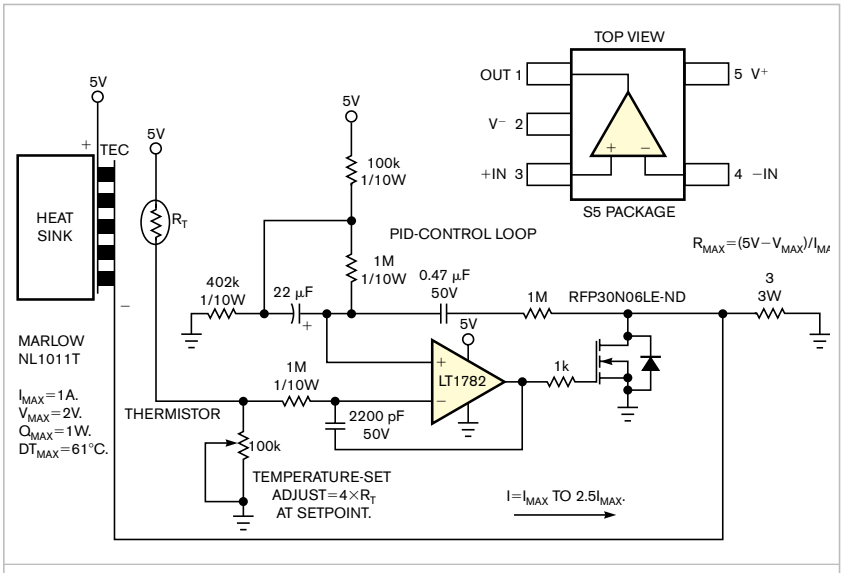

Figure 2 This circuit puts unipolar drive in a PID-feedback loop to stabilize the temperature of the target device.

Transimpedance synchronous amplification nulls out background illumination

Stefano Salvatori and Gennaro Conte, University Roma Tre, Rome, Italy

Light sensors find use in a host of important applications, spanning from consumer electronics, such as ambient-light measurements and exposure control for cameras, to scientific instruments, such as optical-absorption spectroscopy, IR (infrared) detection for thermography, and two-color pyrometry. For example, in optical spectroscopy, a correct intensity measurement of the probe beam is fundamental during material and device characterization. You must eliminate any influence that dc or very-low-frequency background light induces. Also, to increase the SNR (signal-to-noise ratio), you can apply narrowband, phase-sensitive, or lock-in detection techniques to mechanically chopped or otherwise modulated probe-light sources.

In this Design Idea, the reference signal from the light chopper as a square wave of frequency, f_{CHOP}, modulates the gain of an op-amp-based inverting amplifier (**Figure 1**). The amplifier input is a voltage proportional to the photocurrent signal produced by a photodiode, which is irradiated by a modulated light beam at the same chopper frequency. In this case, because the gain and input are at the same frequency content, a dc component, which a low-pass filter can easily detect, is present at the amplifier's output.

Op amps A_{1A} and A_{1B} convert the photogenerated current into a voltage including only the ac components. You can change the value of R_1 depending on the light level you want to detect. Neglecting A_{1A}'s input capacitance, the value of C_1 strongly depends on the terminal capacitance of the input photodiode, and you must select the value to ensure the stability of the transimpedance circuit (**Reference 1**).

The heart of the system, op amp A_{1C}, includes photoresistor R_{PR}, which represents the feedback element that determines the gain of the stage. The value of R_{PR} depends on the light that D_1 emits. A_{2B}, a voltage-to-current converter, drives D_1. The converter has a fixed voltage, V_B, and a ΔV signal through A_{2A} and A_3. A_{2A} determines the dc value of R_{PR}, whereas A_{2B} and ΔR_{PR} change at the same frequency as the reference signal. The A_3 Schmitt trigger converts any TTL/CMOS level of the reference signal into a balanced ±4.6V square wave attenuated to ±0.5V to generate an LED current change of approximately 1.8 mA p-p. For the photoresistor, R_{PR}, and LED elements, a Silonex (www1.silonex.com) CdS (cadmium-sulfide) NSL-19M51

cell couples to a red LED and resides in a black box to ensure the absence of background light on the optocoupler.

To calibrate the circuit, first disconnect or obscure the input photodiode so that A_{1A} converts no ac signal. Then, switch S_1 to the "measure" position and adjust R_{T2} to null any voltage offset referred to the output voltage. When the A_{1B} buffer generates the known approximately 300-mV test voltage and S_1 is in the calibrate position, adjust R_{T1} to fix the output voltage at 0V. In such a case, V_B voltage can set the $R_{PR}/R_C=R_A/R_B$ condition. EDN

REFERENCE

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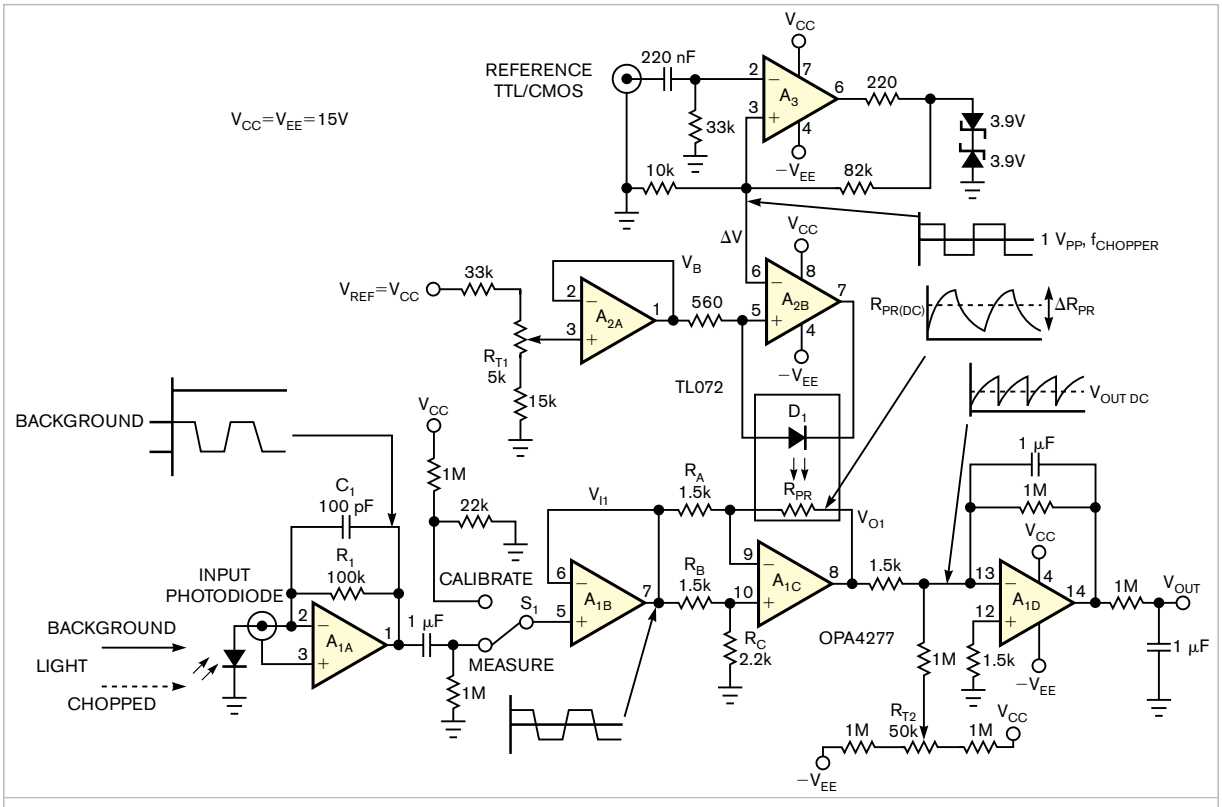

Figure 1 The reference signal from a light chopper acts as a square wave of frequency and modulates the gain of an omp-amp-based inverting amplifier.

Microcontroller drives LCD with just one wire

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

HD44780 LCDs are the most popular alphanumeric displays in embedded systems. The only downside is that they use six I/O pins in 4-bit nibble mode and as many as 11 pins in 8-bit mode. Earlier Design Ideas have described many approaches to saving or expanding I/O pins (**references 1**, **2**, and **3**). In driving an HD44780-compatible LCD, it would be better to use a baseline microcontroller instead of logic chips, because the microcontroller is lower cost, uses less board space, and has programming features. Microchip (www.microchip.com) has introduced the smallest PIC10F microcontroller family, which comes in a six-pin SOT-23 package.

The circuit in **Figure 1** proves useful for any pin-limited embedded system that must interface with an HD44780-compatible display through a one-wire serial link using an asynchronous, simplified RS-232 protocol at 9600 baud. It uses a PIC10F202, but any member of the PIC10F family is suitable, because the highly optimized source code in **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com/071203di1, allows the program code to take fewer than 256 words. It is useless to try higher baud rates than 9600, because the PIC10F202 uses an RC internal oscillator with 1%-frequency tolerance, and the LCD requires a delay as long

as 1.6 msec for some instructions, such as "clear display."

Listing 1 is the fully commented assembler source code for the LCD232 module; the main routine consists of the display of a 2-sec-delay "splash screen," and then it enters an endless loop to wait for 1 byte as a command for the LCD, a maximum of 16 bytes as data for the LCD, and an ASCII zero. For test purposes with an external PIC microcontroller embedded system, **Listing 2**, also available at www.edn.com/071203di1, is a simple assembler source code, which sends another splash screen. EDN

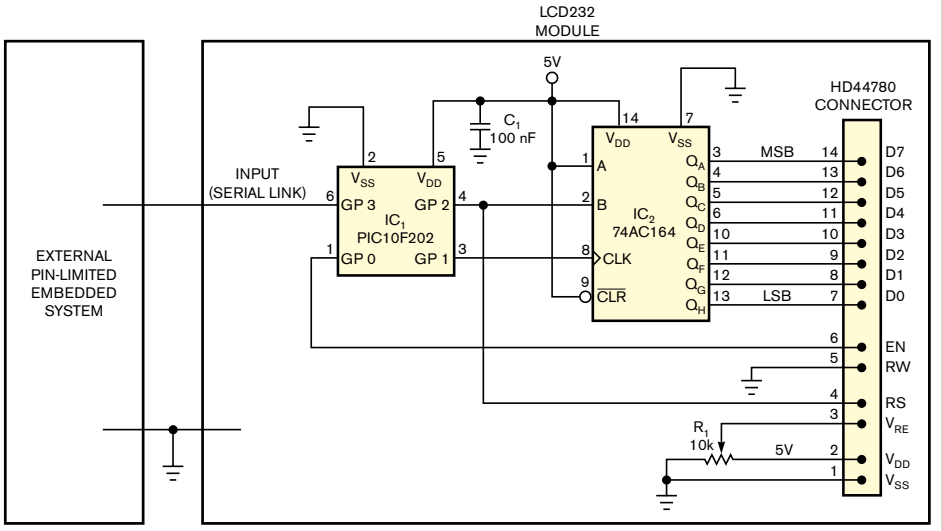

Figure 1 This circuit interfaces a pin-limited embedded system with an HD44780-compatible display through a one-wire serial link using an asynchronous, simplified RS-232 protocol.

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3 Niven, Rex, "RC lowpass filter expands microcomputer's output port," *EDN*, June 21, 2007, pg 74, www.edn.com/article/CA6451248.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Actively driven ferrite core inductively cancels common-mode voltage

W Stephen Woodward, Chapel Hill, NC

An earlier Design Idea illustrated one approach to that traditional headache for the analog designer: the dreaded ground loop (**Reference 1**). That Design Idea described a simple and efficient multichannel circuit. But it's an asymmetrical CMV (common-mode-voltage) approach in that it works only at the receiving end of a cable. It therefore applies only to signal inputs and does nothing for outputs. However, in cases in which CMV consists of purely ac noise, a different CMV-remediation method—active inductive cancellation—works bidirectionally and therefore cancels CMV-error components in both input and output signals.

Engineers have for many years used passive-CMV inductive cancellation (**Figure 1**). Sometimes called a "humbucker transformer" because the power mains' 60-Hz "hum" is often a dominant CMV component, the CMV inductor comprises a primary winding in series with the ground connection between the signal source (1) and the destination (2) and a secondary winding with a 1-to-1 turns ratio.

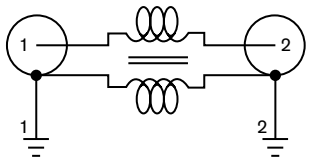

Figure 1 In the classic humbucker configuration, the CMV inductor comprises a primary winding in series with the ground connection between a signal source (1) and a destination (2) and a secondary winding with a 1-to-1 turns ratio.

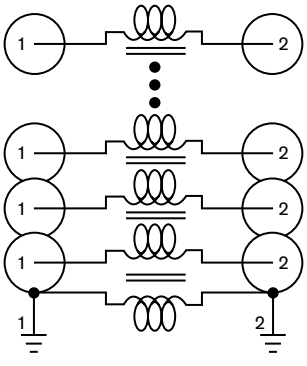

Figure 2 You can extend the passive approach in Figure 1 to multiple channels at the expense of a large magnetic component.

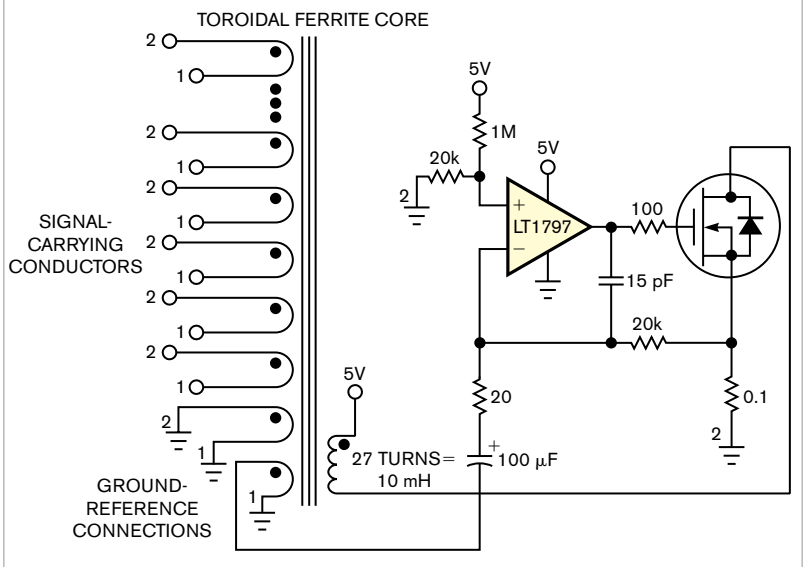

Figure 3 Using the active drive of the CMV core, you can achieve CMV reduction of 40-dB or more cancellation, extending from tens to millions of hertz.

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The principle of the CMV transformer relies on magnetic coupling between the primary and the secondary, such that any voltage that appears across the primary induces an equal and opposite voltage in the secondary, thus canceling it. You can easily extend the principle to multiple signal channels simply by adding more secondary windings—one secondary for each channel (**Figure 2**).

However, the Achilles' heel of the CMV transformer is the fact that the decibels of cancellation fall off at the low-frequency end of the noise spectrum. This situation occurs because noise cancellation depends on the fact that the inductive reactance of the windings must be much larger than the impedance of the cable. Hundreds of millihenries of inductance are necessary to satisfy this criterion for frequencies as low as 60 Hz. For multichannel applications requiring cancellation for frequencies as low as 60 Hz, this fact translates to lots of copper, core, bulk, and weight. However, if you don't mind if your designs consume a little power, then a work-around exists: actively driving the CMV core.

In **Figure 3**, the power amplifier comprising the LT1797 high-frequency op amp and MOSFET forces the driven core to precisely cancel CMV as sensed in the ground-reference connection. The result is such a large multiplication of the apparent winding inductance that you can reduce the "windings" to a simple single pass-through of the toroid core. In other words, you need to thread a multiconductor-signal cable only once through the "hole in the doughnut" to achieve CMV of 40-dB or more cancellation, extending from tens to millions of hertz. EDN

REFERENCE

1 Woodward, W Stephen, "Amplifier cancels common-mode voltage," *EDN*, May 10, 2007, pg 82, www.edn.com/article/CA6437955.

Improved optocoupler circuits reduce current draw, resist LED aging

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It seems deceptively simple to establish galvanic isolation with the help of optocouplers between circuits that operate at different ground potentials. Optocouplers draw power from the isolated circuit, and switching can be relatively slow and uncertain because of LED aging. Substitutes without optocouplers, such as the ADUM12xx from Analog Devices (www.analog.com) or ISO72x from Texas Instruments (www.ti.com), are available. This Design Idea describes a method of improving the simple optocoupler.

Figure 1 shows two popular designs of 0V synchronization with ac. An attempt to reduce power draw from the isolated circuit by decreasing the optocoupler's LED current with a corresponding increase of the optocoupler's load resistor yields slower and more uncertain switching. To achieve faster and sharper switching, you would have to sacrifice power efficiency; however, the benefit of this sacrifice is limited because of the inverse relationship between power efficiency and the ac-voltage magnitude.

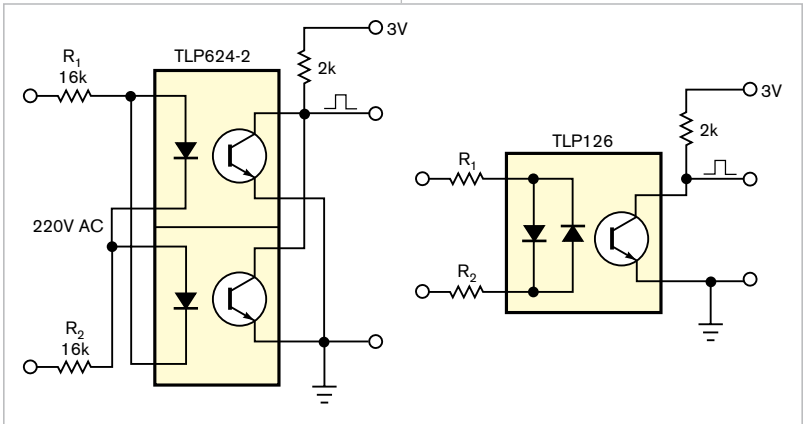

Figure 1 Establishing galvanic isolation with the help of optocouplers between circuits that operate at different ground potentials looks deceptively simple. Optocouplers draw power from the isolated circuit, and switching can be relatively slow and uncertain because of LED aging.

An optocoupler's LED emits almost continuously during nearly all ac cycles exceeding the nominal, leading to low power efficiency and relatively fast aging of the optocoupler. One more drawback is excessively large and nearly uncontrollable zero-crossing error; the circuit's sensitivity threshold depends on the parameters of the optocoupler. The designs in **Figure 1** do not provide an ideal approach. With respect to efficiency, they can draw 5 to 100 mA, depending on the optocoupler's current-transfer ratio and the ac amplitude.

The design in **Figure 2** overcomes the problems of excessive power consumption, uncertain switching, and LED aging. It lends itself well to wide-ac-range applications. Compared with the circuit in **Figure 1**, **Figure 2**'s LED emits only in close vicinity of the zero-crossing point and receives its power from the previously charged capacitor, so you can reduce the average current draw by a factor of 10 to 100. The design also provides faster, more

deterministic, and sharper switching. What's more, you can expect slower LED aging. Resistors R_1 and R_2 in **Figure 1** dissipate no less than 1.5W of power as waste heat, so changing them to 0.1W devices allows placement of additional components on the same board area (**Figure 2**).

The circuit's main components comprise amplitude detector D_1, capacitor C_1, and Schmitt trigger Q_1/Q_2 to control a current through the optocoupler's LED. D_2 and D_3 stabilize the base voltage of Q_2 and, hence, its collector current, which activates the optocoupler. Capacitor C_1 charges up through R_1, R_2, and D_1.

During nearly all of the ac-cycle time, except in the vicinity of the zero-crossing point, Q_1 is on, and Q_2 is off. Then, approaching the zero-crossing point, the state of Schmitt trigger Q_1 and Q_2 changes, and Q_2 discharges capacitor C_1 with the constant current, because the circuit comprising Q_2, D_2, D_3, R_5, and R_6 stabilizes current as $I=(2\times V_D-V_{BE2})/R_6$, where V_D is the voltage drop on D_2 or D_3 and V_{BE2} is the base-emitter voltage of Q_2.

Some applications require none of the hysteresis that is inherent to a Schmitt trigger; **Figure 3** shows such a design. It also shows how to manage without a requirement for minimal reverse current in D_1. This circuit, however, better suits pure synchronization and not thyristor control. Because of the stability of LED current, these designs provide an expanded input-ac-voltage range, which may be useful for a multistandard ac-powered gadget; an opportunity to set the LED current without the risk of overloading the LED; and a reduced influence of the optocoupler's instability. One more advantage of these designs is their inherently safer nature. In the case of a short circuit in their terminals, optocouplers deliver 10 to 100 times less current between the isolated and the nonisolated sides than the circuit in **Figure 1**. The optocoupler also offers advantages. Thanks to the low duty cycle, you can freely reduce the value of the optocoupler's load resistor, R_8, without sacrificing power efficiency. This reduction results in low zero-crossing error. EDN

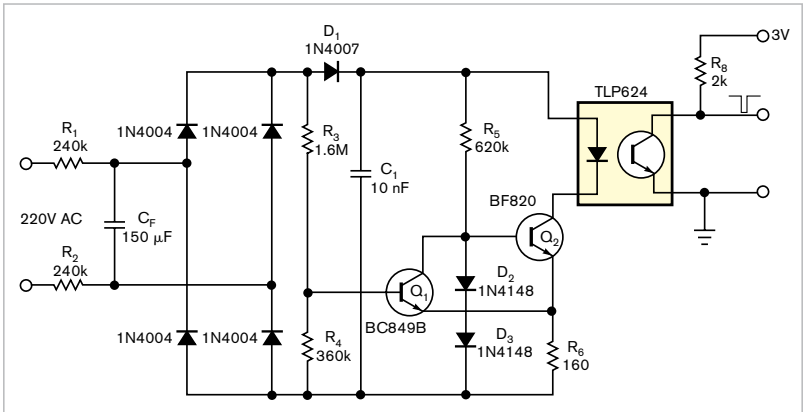

Figure 2 This circuit overcomes problems of excessive power consumption, uncertain switching, and LED aging.

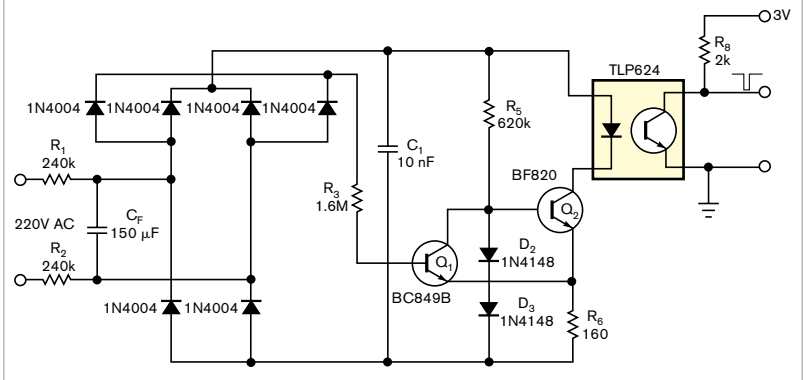

Figure 3 Another variant of this design shows how to manage without a requirement for minimal reverse current in D_1.

Cascade two decade counters to obtain 19-step sequential counter

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This Design Idea offers a practical approach to cascading two or more Johnson counters together with a bare minimum of parts. The CD4017 Johnson decade counter finds use in simple circuits ranging from sound effects to LED displays. The counter's outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. The dc-supply voltage can range from approximately 3 to 18V dc. The dc-current drain per each output pin (Q0 to Q9) is 10 mA. The circuit has passed tests at 12V dc at 0 to 150°F without anomalies.

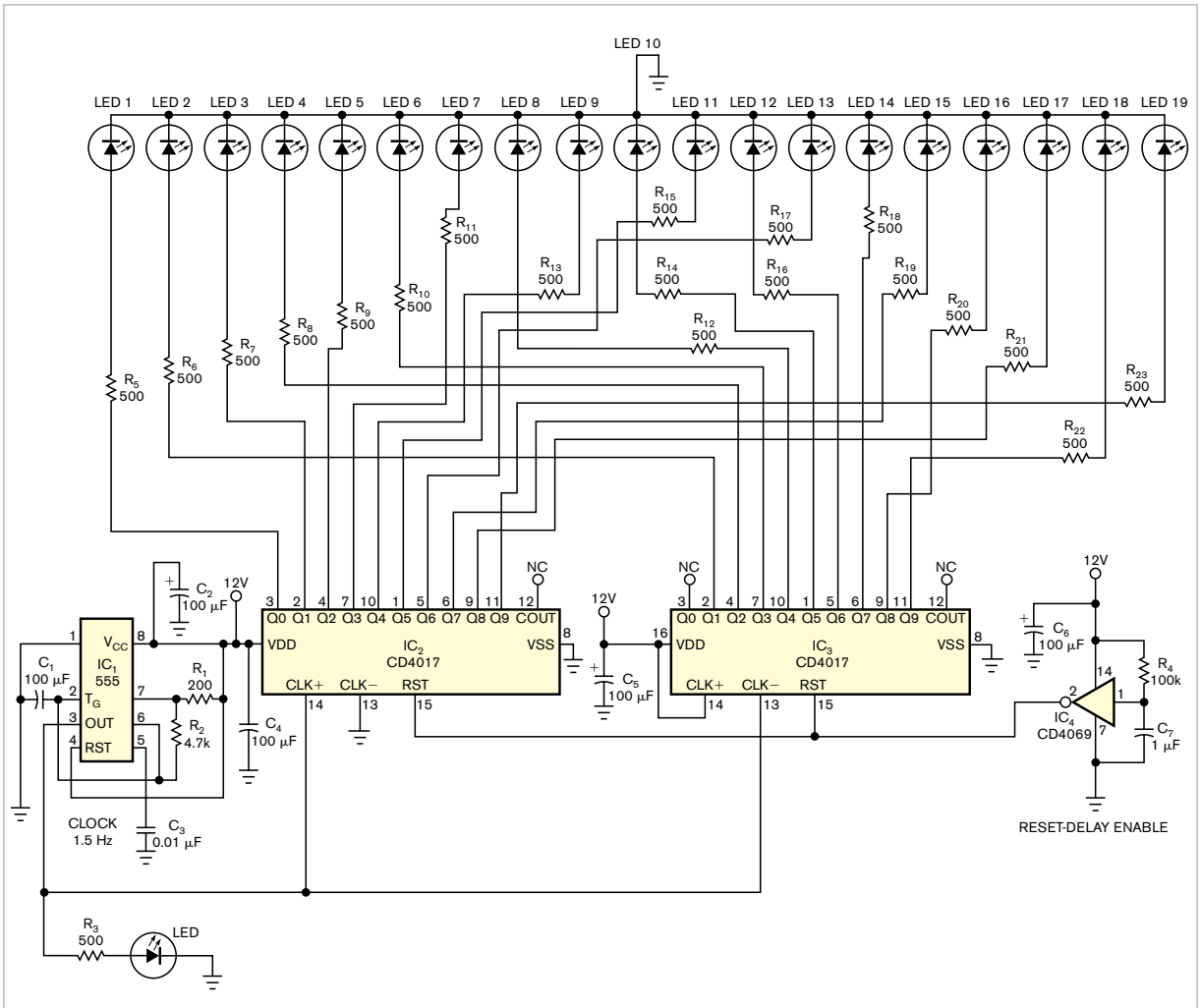

Figure 1 By interleaving the outputs of two cascaded CD4017 Johnson counters, you can obtain a 19-step sequential output.

The circuit in **Figure 1** uses only four ICs and yields a 19-step sequential count. You cannot get 20 outputs without adding more hardware because of the fact that, upon powering up, each CD4017 counter displays output Q0 as being on. Therefore, the circuit does not use output Q0 of IC_3 and can use only 19 of the 20 outputs.

At first blush, you might think that you could simply cascade two counters together using the carry-out pin, Pin 12, from one counter to feed the clock-input pin, Pin 14, of a second counter. But the problem with this configuration is that it does not provide sequential count from 1 to 20 because the first counter begins to count over again once it has reached 10. Such a configuration is a zero-to-99 counter because every 10 counts on the first IC counter causes one count on the second IC counter.

By hooking together two counters, you can obtain a sequential count from 1 to 19. The circuit uses IC_4, a CD4069 inverter, as a reset-delay enable to cause a few milliseconds of delay before each counter can begin to count. A high signal on the Pin 15 Reset clears the counter to its zero count.

Without the delay time, each counter powers up with a random output count such that several LEDs may be on. The circuit uses IC_1, a 555 timer, as the clock to generate a 1.5-Hz square wave. You can change the frequency by changing the RC time constant comprising R_1, R_2, and C_1. Keep in mind that, to obtain a 50% output duty cycle, make R_2 much larger than R_1. Pin 14 of IC_2 has a positive-edge clock trigger. Pin 13 of IC_3 has a negative-edge clock trigger. Therefore, when the clock goes high, IC_2 produces an output count. When the clock goes low, IC_3 produces an output count. By interleaving the outputs, you obtain a sequential count from 1 to 19. Because each clock cycle has both a high and a low state, after the first clock pulse, two LEDs will always be on—that is, LED 1, LED 1 and 2, LED 2 and 3, LED 3 and 4, and so on. Go to www.edn.com/071214di1 to see a short video clip of the finished circuit in action. EDN

Dual-input sample-and-hold amplifier uses no external resistors

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At least two classic ways exist to address applications requiring sampling of a sum of analog voltages. The most common way is to cascade a classic analog adder and a sample-and-hold amplifier. A classic analog adder is an op amp plus at least three precision resistors. The values of these resistors should be as low as possible so as not to deteriorate the bandwidth of the adder. On the other hand, such low-value resistors dissipate power. Further, the configuration of an adder-sample-and-hold amplifier suffers also from another drawback, which manifests itself when the two input voltages are close in magnitude but of opposite polarity. In this case, even if the magnitude of the input voltages is high, the resulting sum is low or no voltage if the magnitudes of input voltages are equal. Sampling a low voltage usually involves a high relative error of the output voltage because each amplifier has some dynamic errors, such as residual parasitic transfer of charge into the storing capacitor.

Another possibility is to use one amplifier per channel and add their outputs in a classic analog adder. Although this configuration avoids the problem with the high relative error of output voltage when input voltages are similar in magnitude and opposite in polarity, precision resistors in the adder still dissipate power.

You can avoid these problems by using the circuit configuration in **Figure 1**, which uses no external resistors. In the steady state, the internal-tracking interval, the $\overline{Q}_D$ internal-logic signal is at an active-high level, enabling the A_1, B_1, and A_2 followers. Thus, the ground-referenced capacitor, C_2, charges to the V_{INA} voltage. The lower node of capacitor C_1 at Pin 2 of IC_2 gets temporarily grounded through the out-

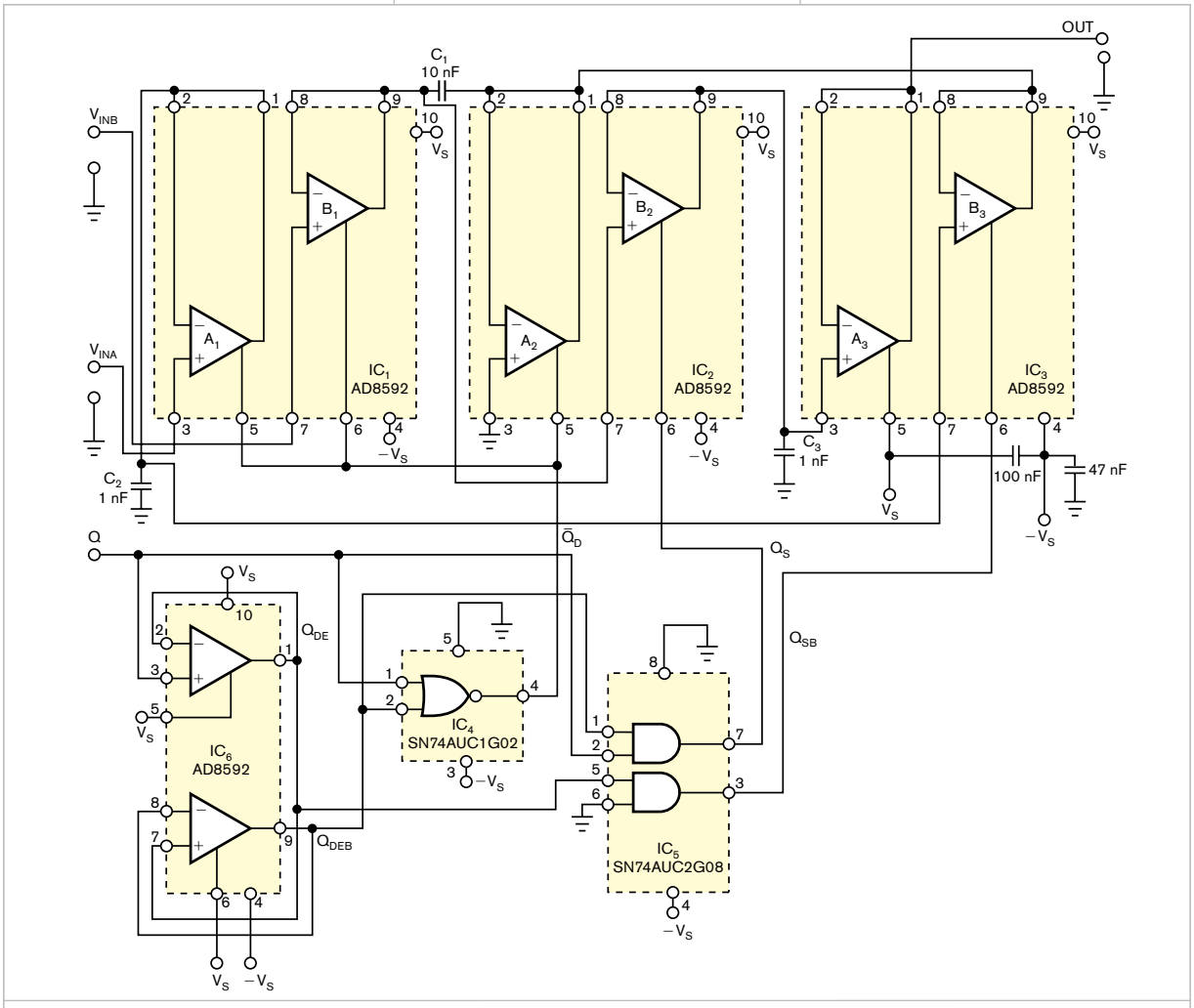

Figure 1 The basis of the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on the C_2 and C_1 capacitors, stacking these capacitors within the sample interval, and storing the value of stack's voltage on the C_3 capacitor.

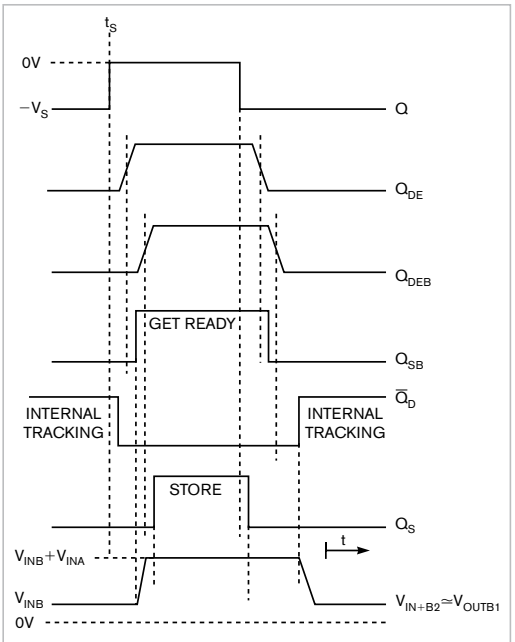

Figure 2 The bottom waveform shows that, at the upper node of the C_1 capacitor, the V_{INB} voltage appears within the tracking interval, and it rises to the value of the sum of both input voltages within the get-ready interval.

put of the A_2 follower while it charges to the V_{INB} voltage at its upper node at Pin 9 of IC_1. V_{INA} and V_{INB} are the input voltages at the A and B inputs, respectively.

After a settling period, when all internal logic-control signals are low and all controlled followers are disabled, the Q_{SB} control-logic signal goes high. The potential at the lower node of C_1 goes from 0V to $V_{C2}(t_S)=V_{INA}(t_S)$ because of the enabled B_3 follower. $V_{C2}(t_S)$ is the value of voltage stored on the C_2 capacitor before the transition of the $\overline{Q}_D$ signal to an inactive-low level. The potential at the upper node of C_1 consequently rises to the value of $V_{C2}(t_S)+V_{C1}(t_S)=V_{INA}(t_S)+V_{INB}(t_S)$, as the bottom waveform in **Figure 2** shows. This trace is the only analog waveform in this **figure**. The active-low-to-high transition of the sampling-command logic signal, Q_S, gets slightly delayed with respect to that of the Q_{SB} logic signal, suppressing glitches in the output voltage. When Q_S is high, the sampled voltage of $V_{INA}(t_S)+V_{INB}(t_S)$, which is present at Pin 7 of IC_2, passes through the enabled B_2 follower to the C_3 capacitor and gets stored there until the next sampling command. The A_3 follower serves as an impedance converter. Dual op amp IC_6 serves as a tapped delay line, which, in conjunction with one single-NOR gate and one dual-AND gate, derives properly timed internal logic-control signals from the single external logic-control signal, Q.EDN

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1 "AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ±250 mA Output Current and a Power-Saving Shutdown Mode," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.