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READERS SOLVE DESIGN PROBLEMS

Use the MCLR pin as an output with PIC microcontrollers

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Although microcontroller manufacturers try to offer designers products that almost exactly fit the needs of their designs, another output pin is often necessary. This situation is particularly true in small designs using microcontrollers with eight pins or fewer. This Design Idea employs the Microchip (www.microchip.com) PIC10F222. The PIC10F222 comes in an SOT23-6 package and offers three I/O pins, one input pin, RAM, flash, and an ADC module. You must program these tiny microcontrollers, just as you do with their big brothers. To program these microcontrollers, you need the MCLR, two I/O pins (data and clock), and supply pins (V_{CC} and GND). To enter programming mode, you need MCLR and supply. Because the microcontroller must differentiate between normal and programming mode, the MCLR pin usually reaches a voltage of approximately 12V to enter programming mode. Thereafter, in normal operation, you can configure the MCLR pin either as an external reset or as an input-only pin.

This design uses one pin for analog input and the other three as outputs. The design thus requires an additional output. For that reason, this circuit uses the MCLR pin as an output. For simplicity, **Figure 1** shows only the GP3/MCLR output circuit. To allow the GP3/MCLR pin to act as an output, the circuit uses the configurable weak pullups that this microcontroller offers. The selected function for the GP3/MCLR pin is input, and you must enable the global weak-pullup bit in the microcontroller's configuration word. Although you cannot individually configure weak pullups, this inability is not a problem because you configure all other pins as analog inputs or digital outputs.

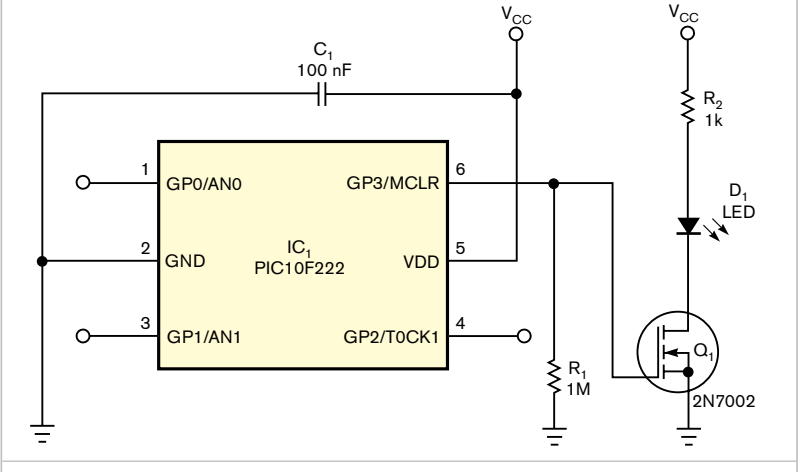

Figure 1 Adding a MOSFET and associated circuitry to a PIC microcontroller's MCLR input pin transforms the pin into an output.

The weak pullups have a resistance of 20 to 150 kΩ, depending on supply voltages, so this circuit uses transistor Q_1 to drive higher loads, such as the depicted LED. R_1 drives the transistor off when you deactivate the pullups. Because the transistor's gate is resistance-driven, the maximum toggle frequency depends on the chosen transistor. The worst-case scenario occurs when you need to switch off Q_1. R_1 and Q_1's gate-to-source capacitance determine the transistor's switch-off time.

Programming voltages for the MCLR pin are about 12V. Therefore, Q_1 must withstand a gate-to-source voltage higher than this value. This design uses a MOSFET having a ±18V withstand voltage. For this reason, you should not use digital MOSFETs. You can use this circuit with other PIC microcontrollers and with most RS08KA family microcontrollers from Freescale. EDN

DIs Inside

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High-speed clamp functions as pulse-forming circuit

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Amplifiers with positive feedback are the bases of signal-grade pulse-forming circuits. This setup ensures a triggerlike operation in which the input signal crosses the input-threshold level; in most cases, the input signal is a voltage signal. The most well-known of these triggers is the Schmitt trigger, which, by the way, will this year celebrate its 70th birthday. British scientist OH Schmitt in 1938 originated the Schmitt trigger in the form of a two-stage amplifier with current feedback. The two active devices were vacuum tubes.

The operation of a Schmitt trigger has the advantage of fast, almost-constant transition times of the output regardless of the slope of the input signal. One consequence of this type of operation is the hysteresis in the I/O characteristic. In other words, the threshold shifts to a higher value before the positive-output transition, and it shifts to a lower value after switching to the positive-output level. You can set the amount of hysteresis—from zero to latch-up—for Schmitt-trigger circuits comprising discrete parts. Schmitt circuits find wide use in logic ICs, in which the hysteresis is rather high and fixed.

As an alternative, you can use a circuit—a fast-response voltage limiter, or clamper—as a pulse-forming circuit. The input-voltage range is narrower than that of Schmitt-trigger circuits, because, at low input voltages, the voltage limitation becomes inactive, and the circuit operates as a linear amplifier. On the other hand, because of its nonhysteretic behavior, the decision threshold of the input voltage is precise and equal for both directions of output-level transitions. **Figure 1** shows one example of such as circuit. The voltage limiter in **Figure 1** is an inverting amplifier with a highly nonlinear negative feedback. For output voltages ranging from −0.3 to +0.6V, the feedback impedance is high because each of the diodes is nonconducting. The forward-voltage drop of the selected Schottky-barrier diodes determines these voltage limits (**Reference 1**). The voltage gain of the inverting amplifier is thus almost that of the op amp's open-loop gain.

Whenever the output voltage exceeds these limits, diode D_1, D_2, or D_3—depending on the polarity of the output voltage—starts to conduct. The differential gain of the amplifier then drops to the value of $-R_I/2R_D$ and $-R_I/R_D$, respectively, where R_D is the equivalent-series resistance of a single diode. The action clamps the output voltage to approximately 0.8V and to −0.4V even for large input voltages. The **figure** uses an Analog Devices (www.analog.com) AD8045 VHSIC (very-high-speed integrated-circuit) op amp because its slew rate exceeds the value of 1V/nsec (**Reference 2**).

Figure 1's circuit has an asymmetrical-limiting configuration to compare the single feedback diode with two series-connected diodes having a transverse resistor, R_{T1}, between their midpoints and ground. The clamping circuitry comprising D_1, D_2, and R_{T1} offers higher off-isolation between the output and the input of the op amp than that of the single diode, D_3. When D_3 is on, you can observe small, weakly damped oscillations at approximately 200 MHz in the output waveform. Oscillations manifest themselves less at the beginning of turn-on of the D_1 and D_2 diodes. EDN

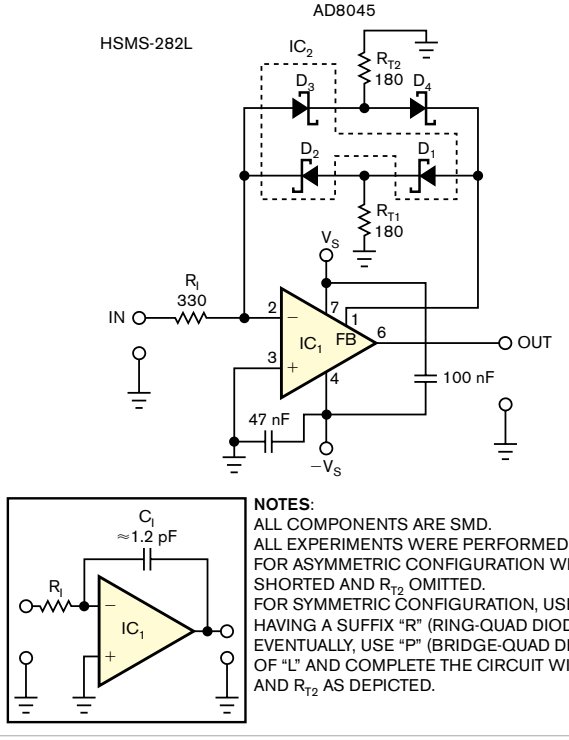

Figure 1 This clamping circuit uses diodes to achieve nonlinear feedback. The circuit employs a single diode in one feedback path and two diodes in the other. The dual-diode configuration offers cleaner switching.

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1 "Surface Mount RF Schottky Barrier Diodes," Avago Technologies, www.avagotech.com/.
2 "AD8045 3 nV/√Hz Ultralow Distortion Voltage Feedback High Speed Amplifier," Analog Devices, 2004, www.analog.com/en/prod/0,,ad8045,00.html.

Depletion-mode MOSFET kick-starts power supply

Gregory Mirsky, Milavia International, Buffalo Grove, IL

Many switch-mode power supplies use "kick-start" circuits to initialize their offline operation. These circuits may be simple resistors, such as International Rectifier's (www.irf.com) IRIS4015, or more complicated arrangements built with bipolar transistors or MOSFETs (**Reference 1**). These transistors provide the initial current for the flyback or PFC (power-factor-correction) IC. When such a power supply starts operating in normal mode, a supply voltage from a dedicated winding keeps supplying the PFC IC, thus reducing power consumption of the kick-start circuitry.

Such schemes reduce—but do not eliminate—the power consumption of the kick-start circuitry, because the active component is usually a high-voltage bipolar transistor or high-voltage enhancement-mode MOSFET. These transistors' base or gate requires forward-biasing with respect to the emitter or the source for normal operation. Therefore, a power loss always occurs in the circuits that keep the transistors in the off state. Unfortunately, engineers pay too little attention to depletion-mode MOSFETs, which require no forward-biasing for normal operation and, moreover, require gate potentials below the source. These valuable properties of depletion-mode MOSFETs suit them for a role in no-loss kick-start circuits for power supplies.

Figure 1 shows a conventional PFC circuit whose IC initially receives power from the output through a depletion-mode MOSFET, Q_2, a DN2470 from Supertex (www.supertex.com, **Reference 2**). Q_2's source feeds PFC IC_1 with an initial supply current of approximately 10 to 15 mA or less depending on the IC model. A brief power dissipation of approximately 4 to 6W can do no harm to the MOSFET soldered to a copper pour. If you have concerns about the MOSFET's health, you can use an IXTY02N50D from Ixys (www.ixys.com, **Reference 3**). Resistors R_3 and R_4 set up Q_2's working point to obtain the minimum required current. Zener diode D_5 limits its voltage across IC_1 to approximately 15V for an input voltage of 18V, which is usually necessary for most PFC ICs and is less than the maximum for MOSFET Q_2.

When IC_1 starts working normally, the secondary winding of the PFC inductor, L, generates the IC's supply voltage, which diodes D_1 and D_3 and capacitors C_1 and C_2 condition. Transistor Q_2 keeps feeding zener diode D_5 and IC_1 for a short interval. Eventually, bipolar transistor Q_3 gets its base supply through resistor R_5 from diode D_2, turning on and clamping Q_2's gate to ground. Q_3's power source is the IC's positive-supply potential of approximately 15V, which is more than enough to shut off Q_2. The residual thermal current of 10 to 20 µA produces no substantial power loss. EDN

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1. "IRIS4015(K) Integrated Switcher," Data Sheet No. PD60190-C, International Rectifier, www.irf.com/product-info/datasheets/data/iris4015.pdf.
2. "DN2470 N-Channel Depletion-Mode Vertical DMOS FET," Supertex Inc, www.supertex.com/pdf/datasheets/DN2470.pdf.
3. "High Voltage MOSFET: IXTP 02N50D, IXTU 02N50D, IXTY 02N50D," Ixys, http://ixdev.ixys.com/DataSheet/98861.pdf.

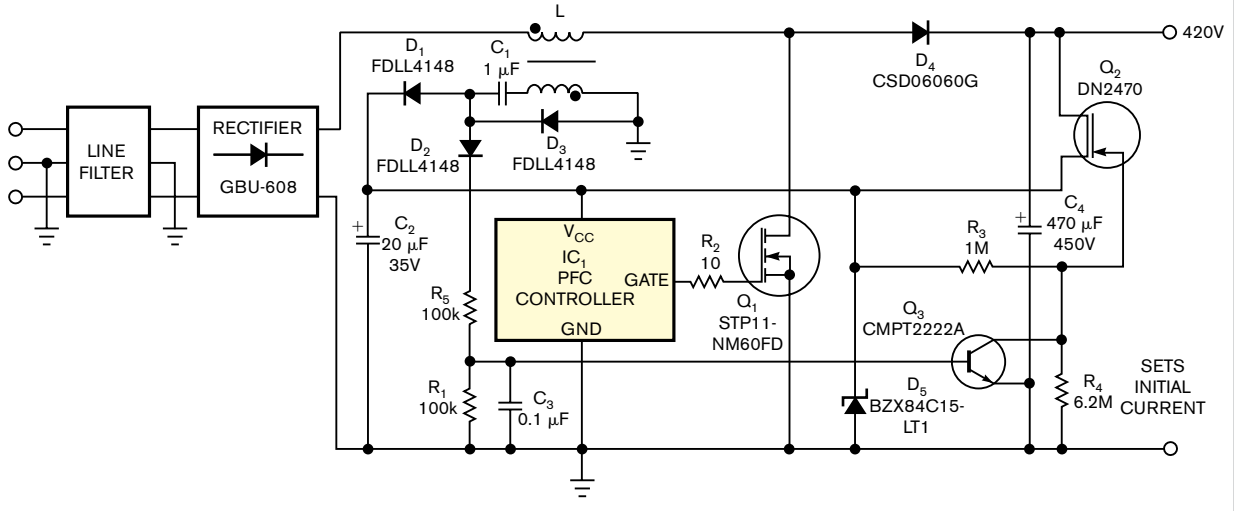

Figure 1 A depletion-mode, high-voltage MOSFET provides a kick-start for a PFC IC. During normal operation, the MOSFET switches off and dissipates negligible power.

Simple continuity tester fits into shirt pocket

Tom Wason, Phoenixville, PA

This Design Idea describes a handy continuity tester with two modes of operation: It may sound if it detects continuity between its two probes, or it may sound when it detects no continuity. The second option permits testing for intermittent cable breaks. Response must be sufficiently fast to permit swiping a probe across perhaps 100 pins to instantly find a connected pin. The tester may also identify microfarad or larger capacitance between two conductors.

To properly test for continuity, the tester's voltage and current are limited so that low-power semiconductors do not suffer overstress or appear as a connection between two conductors. The tester must protect itself if you accidentally connect it across an energized circuit or a charged capacitor. Power consumption must be low so that if you accidentally leave the tester on overnight, it will not discharge the battery. The tester must operate even with low battery voltage.

Continuity requires a threshold of less than 200Ω. Depending on battery voltage, that threshold may even be 80Ω. The tester's open-circuit voltage is less than 0.5V. Its short-circuit current is approximately 1 mA. Values are low so that the tester doesn't mistake a Schottky-barrier rectifier for continuity. When the tester is silent, it draws slightly more than 1 mA of current from a 9V battery. You can connect the probes for a few seconds across any voltage from −50 to +200V without damage.

A feedback circuit comprising Q_1 PNP and Q_2 NPN transistors maintains voltage on the gate of IGFET (insulated-gate field-effect transistor) Q_3 at less than 1.4V despite a 680-kΩ pullup resistor, R_4, and current from D_2 (**Figure 1**). When you short the probes, you divert more Q_1 base current to the probes, and less current flows through D_2. Eventually, Q_2 can no longer maintain a low Q_3 gate voltage. As the gate voltage exceeds 1.8V, Q_3's drain-to-source current causes Q_4 to become nonconductive. A 1-MΩ pullup resistor, R_6, then applies 9V to Q_5's gate, causing the tester to sound, announcing continuity.

Without a conducting Q_2 collector, Q_3's gate voltage approaches 9V. Current would then leak through Q_1's collector-to-base path. Diode D_2 blocks Q_3's gate voltage from leaking to the shorted probes.

The tester detects instantaneous continuity even when you quickly swipe a probe across 100 pins. Capacitor C_1 and pullup resistor R_5 extend Q_5's low gate-voltage response by 20 msec. Thus, the tester sounds slightly longer to indicate that it has established connectivity and does not miss a conductive pin during a fast swipe.

Probe current charging a capacitor may also create a short beep. The 20-msec extended beep means that the tester detects even 10-μF or smaller capacitors. With practice, you can estimate capacitance within decades from the beep's period.

Diodes D_3 through D_5 block destructive currents if probes touch an energized circuit. Resistor R_3 must be at least ½W to withstand current from an energized circuit for a few seconds without damage.

To test for cable continuity, the tester sounds only during a broken connection. In this case, firmly connect the probes to both ends of the cable. Switching S_2 changes the tester's function so that Q_4 drives the buzzer during a cable break.

You can modify the circuit to be a better cable tester by reducing the value of resistor R_1 to 4.7 kΩ and omitting capacitor C_1. With these modifications, detecting loss of continuity occurs at a threshold resistance of less than 100Ω.

Unfortunately, a continuity tester may create noise currents that feed back into the sensitive Q_1/Q_2 detector. Three circuit features minimize that noise. First, capacitor C_2 connects across the buzzer. Second, IGFET Q_3 acts as a buffer. Last, diode D_5 grounds Q_4 and Q_5 separately from ground for Q_2 and Q_3.

The circuit performs even when a battery voltage is less than 6.5V. However, lower battery voltage means that the tester detects continuity at a higher threshold resistance. You may install the entire tester in a plastic case smaller than a pack of cigarettes. EDN

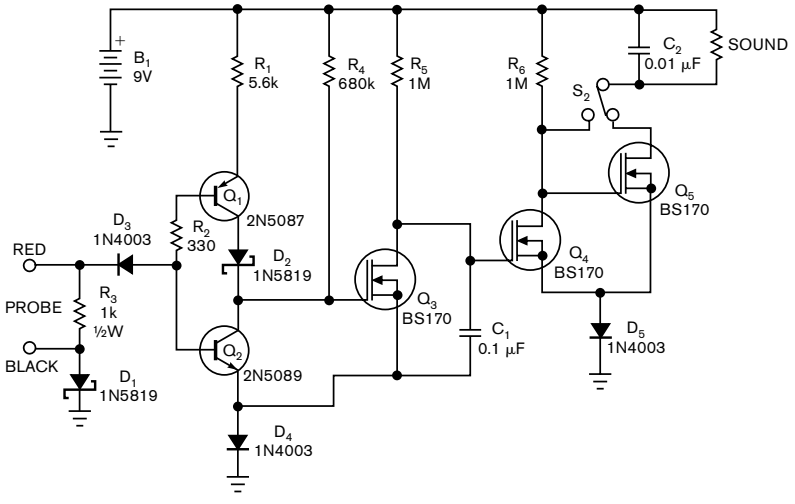

Figure 1 This simple continuity tester is switch-selectable to sound on either shorts or opens. It prevents a user from accidentally connecting it across live circuits.

White LED shines from piezoelectric-oscillator supply

TA Babu, Chennai, India

LED drivers that receive their power from a single cell are receiving a great deal of attention. To generate the high voltage for illuminating a white LED from a low-voltage power supply basically requires some form of an electronic oscillator, and one of the simplest is a piezoelectric buzzer. An unusual application of a piezoelectric transducer serves as an oscillator and drives a white LED (**Figure 1**). The piezoelectric diaphragm, or bender plate, comprises a piezoelectric ceramic plate, with electrodes on both sides, attached to a metal plate made of brass, stainless steel, or a similar material with conductive adhesive. The circuit uses a three-terminal piezoelectric transducer. In this transducer, the diaphragm has a feedback tab on one of its electrodes. The oscillation is a result of the resonance between the inductor and the element, which is capacitive. The frequency of operation is: $f_{OSC}=1/(2\pi\sqrt{LC})$, where L is the value of the inductor and C is the capacitance of the piezoelectric element.

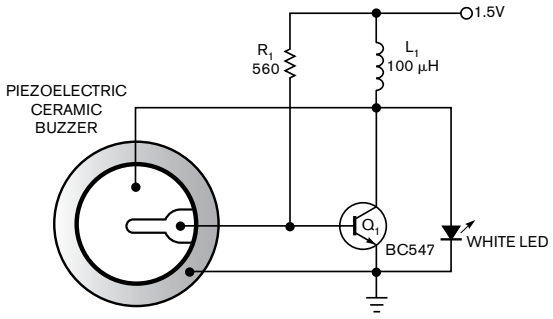

Figure 1 A piezoelectric ceramic buzzer serves as the oscillator in this flyback supply that lights a white LED using a single cell (not shown).

With the initial application of potential to the circuit in **Figure 1**, transistor Q_1 turns on. When the transistor conducts, the current through inductor L_1 increases gradually, and the potential across the plates flexes the piezoelectric ceramic. This flexing generates a negative potential at the feedback tab, which feeds back to the base of the transistor. The transistor then switches off. When turn-off occurs, the stored energy in the inductor dumps into the LED. This flyback voltage is sufficient to light the LED. EDN

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READERS SOLVE DESIGN PROBLEMS

Flexible Hopfield neural-network ADCs quash noise

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A Hopfield network can convert analog signals into digital format and can perform associative recalling, signal estimation, and combinatorial optimization similar to the way a human retina performs first-level signal processing. This Design Idea explores the Hopfield-neural-network paradigm for ADCs.

Simple converters comprise one-layer neurons that accept analog inputs and generate digital-bit outputs; such neurons make up one form of adaptive- and distributive-processing networks. These neurons comprise voltage comparators driving either analog inverters or followers and fully connected feedback resistors from the analog outputs of the inverters or followers to the comparators (**figures 1** and **2**). Reference and analog-input voltages drive the neural networks, and digital outputs come from the comparators in the networks. Hopfield networks have learning capabilities; the circuit in this Design Idea can apply different adaptive-learning rules by using alternative comparator-inverter/comparator-follower schemes, conductance-node-layout schemes—reciprocals of the feedback resistances—between the input comparators, and bit-order readouts.

As the analog-input voltage increases, the circuit can produce either monotonically increasing (from a comparator-inverter scheme) or decreasing (from a comparator-follower scheme) bit-word outputs. Decreasing outputs are the complements of increasing outputs and suggest subtractive-bit operations. Further, you can shape the digital responses of the converters to analog-input voltages in varying degrees using different conductance-node layouts as part of rule adaptation. For further flexibility, reversing bit order for digital readouts allows for reflection of circuit responses about analog-input/digital-output characteristics.

You can simply state a few symbols and their meanings to construct the two converters. For energy functions, the resistive network conductances—synapse weightings (S) in the form of reciprocal resistances (R)—have the designations $S_{IJ}=1/R_{IJ}$, where I is the Ith input comparator, J is the Jth feedback path to the Ith comparator, and I does not equal J—that is, there is no self-feedback path of the comparator to itself. The conductance between the input terminal of the Ith comparator and the reference voltage, V_R, has the designation $S_{IR}=1/R_{IR}$. The conductance between the input terminal of the Ith comparator and the analog-input-signal voltage, V_S, has the designation $S_{IS}=1/R_{IS}$.

For graphical curve fittings, Y is the normalized output-bit variable, and X is the normalized input analog voltage from a nonzero average value (less than one) to one. A, B, and C are curve-fitting constants in the curve equation $Y=1-A\times(1-X)^C$ and the complementary-curve equation $Y=A\times(1-X)^C$, where A is a coefficient, B is the lower limit for X and is less than one, and C is a power con-

TABLE 1 INPUT VOLTAGE VERSUS OUTPUT WORD

Input analog voltage (V)			Output binary word	
Raw range	Normalized range	Average normalized range	Raw	Normalized
0 to 0.189	0 to 0.2855	0.1427	0	0
0.189 to 0.265	0.2855 to 0.4003	0.3429	1000	0.5333
0.265 to 0.378	0.4003 to 0.571	0.4856	1100	0.8
0.378 to 0.662	0.571 to 1	0.7855	1110	0.933
More than 0.662	1	1	1111	1

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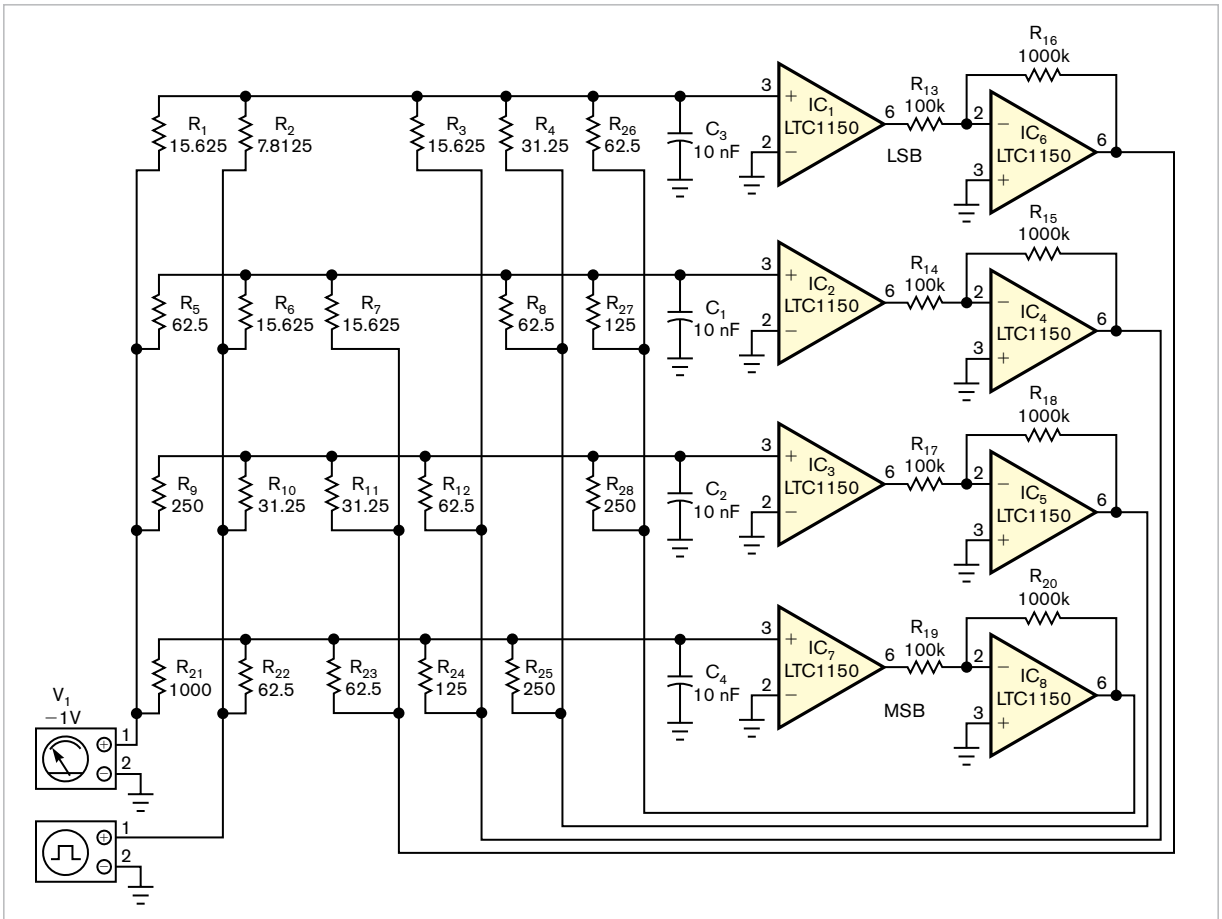

Figure 1 This Hopfield neural ADC provides a robust output in the presence of noise.

stant. For bit-pattern readout reversals, you can have the curve equation $Y=A\times(X-B)^C$ and the complementary-curve equation $Y=1-A\times(X-B)^C$.

Figure 1 shows a 4-bit neural ADC employing voltage inverters that comparators feed. The comparators connect with their positive terminals joined to input nodes and with their negative terminals grounded. The bases of this network are inverse factors of one-half—that is, reciprocal factors of two—input-node conductances $S_{IJ}=-1\times2^{(2-I-J)}$, where the −1 factor comes from negative feedback through the related resistor; $S_{IR}=2^{(1-2\times I)}$; and $S_{IS}=2^{(1-I)}$. To determine node resistances, choose a maximum node resistance of 1000Ω corresponding to a minimum conductance of 0.0078125, and a minimum node resistance of 7.8125Ω corresponding to a maximum conductance of one. Calculate all other resistances from the ratios between the extremes of conductances. Using these values, you can construct **Table 1**. The **table** lists bits ranging from the most significant bit to the least significant. The **table** shows that the digitization process is inaccurate in that it is not linear with input voltage and with many intermediate bit words missing. But the process is precise because it is repeatable over sizable input-voltage ranges. From the **table**, you can derive the following curve-fitting **equation**: $Y=1-1.6243\times(1-X)^{3.1508}$. When X is over the normalized range of 0.1427 to 1, A=1.6243, B=0.1427, and C=3.1508. The Y **equation** is essentially cubic, and it quantitatively shows the highly nonlinear nature of the digitization process. You can obtain a "flipped" mirror—that is, not a true mirror, or pseudoscopic—version of the curve of the straight line on a normalized graph by reversing the bit-order readout from the circuit so that the resulting curve equation would be: $Y=1.6243\times(X-0.1427)^{3.1508}$.

Without analog-input-voltage transformation, such as the use of look-up tables or logarithmic amplifiers to process the input voltage, or digital corrective logic, digital responses from simple Hopfield neural converters are nonlinear and crude. However, these responses are still possibly useful for such applications as associative memory and pattern classification because of robustness in output precision.

Indeed, because of output digital stability, the Hopfield neural converter can allow for unwanted analog-input-signal noisiness or variations. This scenario is in strong contrast to conventional interface circuits between analog-transmission media and digital-

computing machines. This Design Idea shows that flexible circuit adaptability can exist in producing various forms of stable digital outputs from neural ADCs depending on a designer's needs for neural-network-signal processing. This adaptability can be in the forms of various input-node-conductance layouts; comparator/inverter and comparator/follower combinations; and the selected order of bit-readout patterns from the comparators.EDN

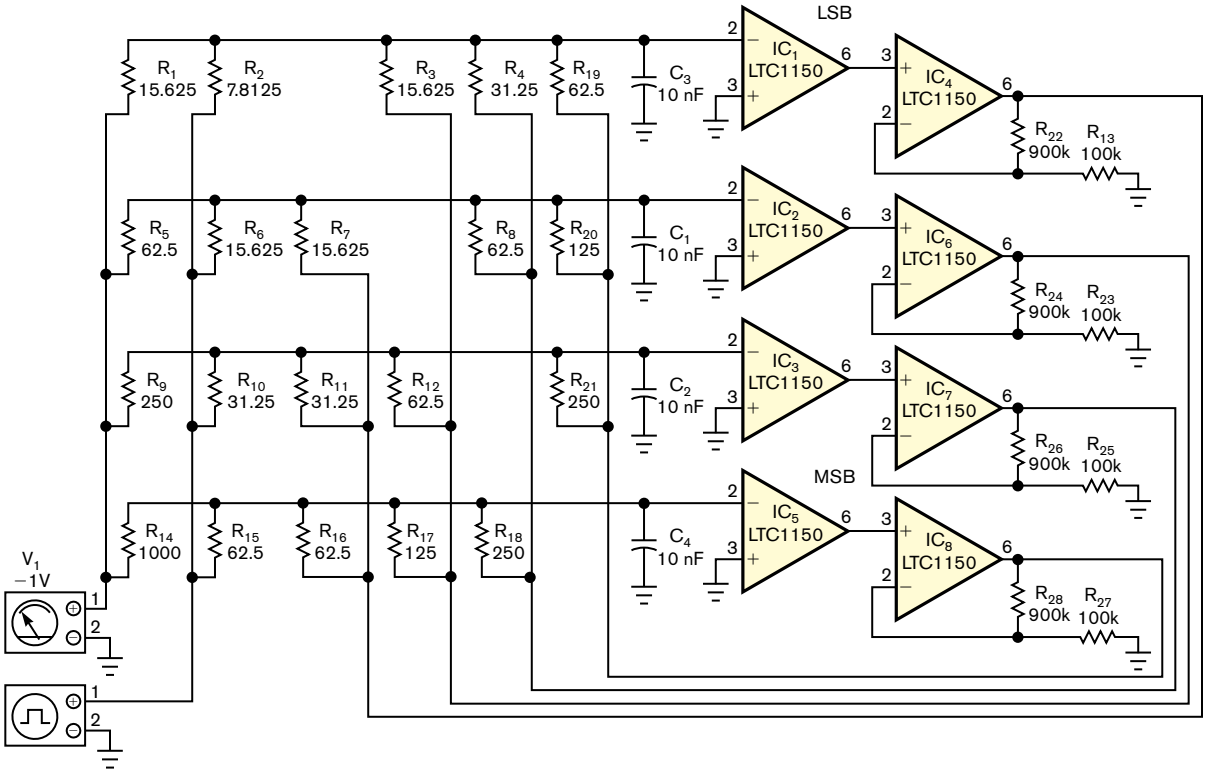

Figure 2 This version of the Hopfield neural ADC features inverted bit outputs.

8-bit microcontroller implements digital lowpass filter

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Filtering occurs frequently in the analog world. Unfortunately, in the digital world, engineers apply it mainly to the DSPs (digital-signal processors) and not to the small 8-bit microcontrollers that designers commonly use. This situation occurs because the math for the filter design is more complicated than most engineers are willing to deal with. Moreover, digital filtering requires calculations on integers instead of on floating-point numbers. This scenario causes two problems. First, the rounding-off error from the limited number of bits can degrade the filter response or even make it unstable. Second, you must handle the fractional values with integer math.

Several ways exist to solve these issues. For example, you can use operations with 16-, 32-, and 64-bit numbers, or you can scale for better accuracy. These and other methods usually require more memory, and, as a result, the program often does not fit into a small microcontroller. A literature search shows that published digital-filter firmware is written in C. Programs in C need more memory than those written in assembler. This situation often makes them unacceptable for small microcontrollers with limited memory resources.

Listing 1, available at the Web version of this Design Idea at www.edn.com/080124di1, shows a simple engineering method to design single-pole, lowpass-digital-filter firmware for 8-bit microcontrollers. The low-end Freescale (www.freescale.com) MC68HC908QT2 is the target of the assembler program, but you can apply this Design Idea to any type of microcontroller because it uses only standard assembler instructions.

Leaving aside the sophisticated design methods based on Z transformation with its extensive math, this idea uses another approach based on a recursive equation. You calculate each output-signal sample as the sum of the input signal and the previous output signal with corresponding coefficients. A recursive equation defines a single-pole lowpass filter as: $Y[n]=X[n]\times a0+Y[n-1]\times b1$, where X[n] and Y[n] are input and output values of sample [n], Y[n-1] is an output value of the previous sample [n−1], and a0 and b1 are weight coefficients that decrement δ controls. The coefficients have the value of $0<\delta<1$, $a0=1-\delta$, and $b1=\delta$. Physically, δ is the amount of decay between adjacent output samples when the input signal drops from a high level to a low level. You can directly specify the value of δ or find it from the desired time constant of the filter, d, which is the number of samples it takes the output to rise to 63.2% of the steady-state level for a lowpass filter. A fixed relationship exists between d and δ: $\delta=e^{-1/d}$, where e is the base of natural logarithms. The preceding **equations** yield $Y[n]=Y[n-1]+(1-\delta)\times(X[n]-Y[n-1])$.

NUMERICALLY PERFORMING THE FILTERING FUNCTION PROVIDES THE BENEFIT OF CONSISTENCY BECAUSE COMPONENT TOLERANCES, TEMPERATURE DRIFT, AND AGING DO NOT AFFECT THE FILTER'S ALGORITHM.

Instead of multiplying a decimal-point number, $1-\delta$, it is more convenient for assembler programming to divide by the reciprocal integer, $F=1/(1-\delta)$: $Y[n]=Y[n-1]+(X[n]-Y[n-1])/F$. Thus, you can determine the digital filter's parameters using the following steps:

1. Choose the parameter F. For assembler, it is convenient to perform division as right shifts. For right shifts, the value of F should be 2S, where S is the number of shifts. Let F equal 8, which you reach after three right shifts.

2. Calculate the decrement: $\delta=1-1/F=1-1/8=0.875$.

3. Calculate the time constant as $d=-1/\ln\delta=-1/\ln 0.875=7.49$ samples.

The **equation** $Y[n]=Y[n-1]+(X[n]-Y[n-1])/F$ determines the design of the microcontroller's algorithm for the filter. The algorithm needs three registers: input for X[n], output for Y[n], and an increment register to keep the $(X[n]-Y[n-1])/F$ term. The size of these registers depends on the inputs. In this application, the signals from the built-in 8-bit ADC range from 00 to $FF and must go through the lowpass filter. So, the input and the output registers are 1 byte in size. To increase the accuracy of division, add half the divisor to the dividend. This action increases the increment register to 2 bytes.

Numerically performing the filtering function provides the benefit of consistency because component tolerances, temperature drift, and aging do not affect the filter's algorithm. The implementation of the digital filter in the microcontroller gives the additional benefit of flexibility to adjust the filter's parameters, because this flexibility depends only on the firmware. EDN

Automotive switching regulators get input-transient-voltage protection

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Engineers often face difficult trade-offs when voltage regulators can encounter high-voltage transients that are well above normal input-supply operating ranges. This situation is common in automotive applications in which high-voltage transients from an alternator load dump can produce transients of 36 to 75V for durations as long as 400 msec. Designers must choose between a regulator that can withstand such maximum input voltage or use an input-protection scheme. The simple circuit in this Design Idea provides a highly cost-effective method for clamping an input voltage from a battery input with transients as high as 50V to take advantage of a 20V, 3-MHz regulator. With this circuit, your design can achieve a small total footprint with relatively low cost because of the 3-MHz operation along with lower voltage components than might otherwise be necessary to withstand 50V.

Input-protection components consist of Q_1, R_1, D_1, C_5, and one-half of D_2 (**Figure 1**). At start-up, N-channel MOSFET Q_1's source is at ground potential and turns on when R_1 applies the battery voltage to the gate. Once the input voltage is above the minimum of 2.74V on IC_1, the LM2734Z regulator starts switching, which charges the bootstrap circuit comprising D_3, D_4, and C_B. This bootstrap voltage of approximately $V_{OUT}-V_{FD}$ (forward-voltage drop) of D_3 then transfers to the gate source of Q_1. Capacitor C_5 then maintains gate drive during the bootstrap diode's off times.

Under normal operating conditions, for example, the battery voltage is 8 to 18V, D_1 does not limit conduction of Q_1, and the gate voltage tracks approximately 2.5V above the input-supply voltage for a low voltage drop from the battery voltage to the input voltage of the LM2734Z. However, when the input voltage increases above the threshold that D_1 sets, the input voltage to the LM2734Z regulates to the zener voltage (V_Z) of D_1 minus the threshold voltage of Q_1, or approximately $20-2V=18V$, well below the 24V absolute maximum of the LM2734Z. Selecting Q_1 requires careful consideration of maximum input voltage, gate-to-source-voltage threshold, and power dissipation under both steady-state and thermal-transient conditions.

Q_1, the SI1470DN N-channel MOSFET, provides 50V protection

with a drain-to-source voltage (V_{DS}) of 30V+20V (zener diode D_1 voltage), has an on-resistance of 95 mΩ at a gate-to-source voltage of 2.5V, and comes in a thermally efficient SC70-6 package. For some applications, the regulator's output voltage may be insufficient to fully turn on the selected protection MOSFET, so you can increase the bootstrap voltage with a separate zener reference, as the LM2734Z's data sheet shows (**Reference 1**). EDN

REFERENCE

1 "LM2734Z Thin SOT23 1A Load Step-Down DC-DC Regulator," National Semiconductor, www.national.com/pf/LM/LM2734Z.html.

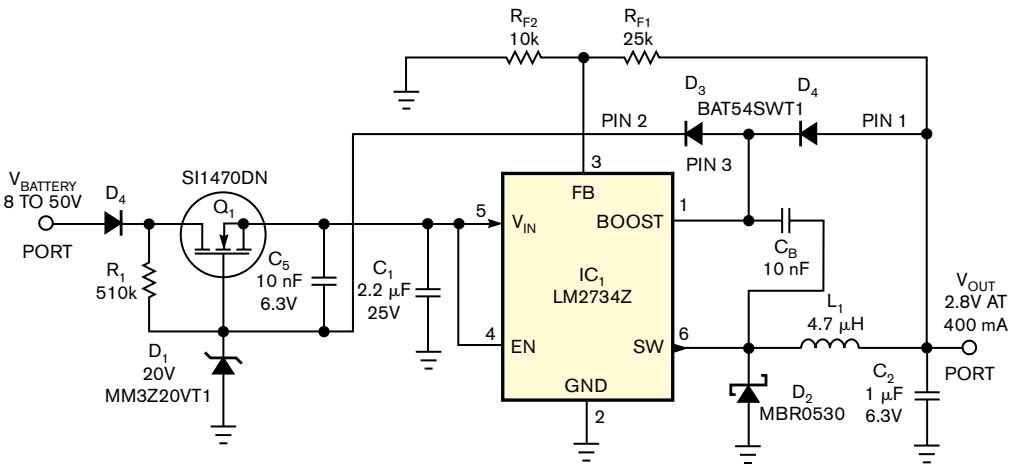

Figure 1 The N-channel MOSFET and zener diode protect the switching regulator against transient voltages as high as 50V in automotive applications.

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READERS SOLVE DESIGN PROBLEMS

Design an RTD interface with a spreadsheet

Robert S Villanucci, Wentworth Institute of Technology, Boston

RTDs (resistance-temperature detectors) are the preferred sensor choices for designs requiring precision. Although RTDs are approximately linear over the limited temperature range of 0 to 100°C, these sensors exhibit a slight but progressively more nonlinear temperature-versus-resistance characteristic as the measurement range widens. Consequently, over an extended span, curve fitting is necessary if the system is to achieve a high level of precision. One way to obviate the nonlinear characteristic of an RTD sensor is to design analog hardware to perform the curve-fitting mathematics before any additional signal processing occurs. This approach is especially attractive if you can keep both cost and component count low and if a microprocessor-driven design is not feasible. With low component count comes the added benefit of a small PCB (printed-circuit-board) footprint.

The most popular RTDs are made from platinum with a resistance value of 100Ω at 0°C and a metal purity that allows them to follow a standard European curve with a positive-temperature coefficient, α, equal to 0.00385Ω/Ω/°C. Less popular but still common are RTDs with a slightly higher metal purity. These RTDs have α of

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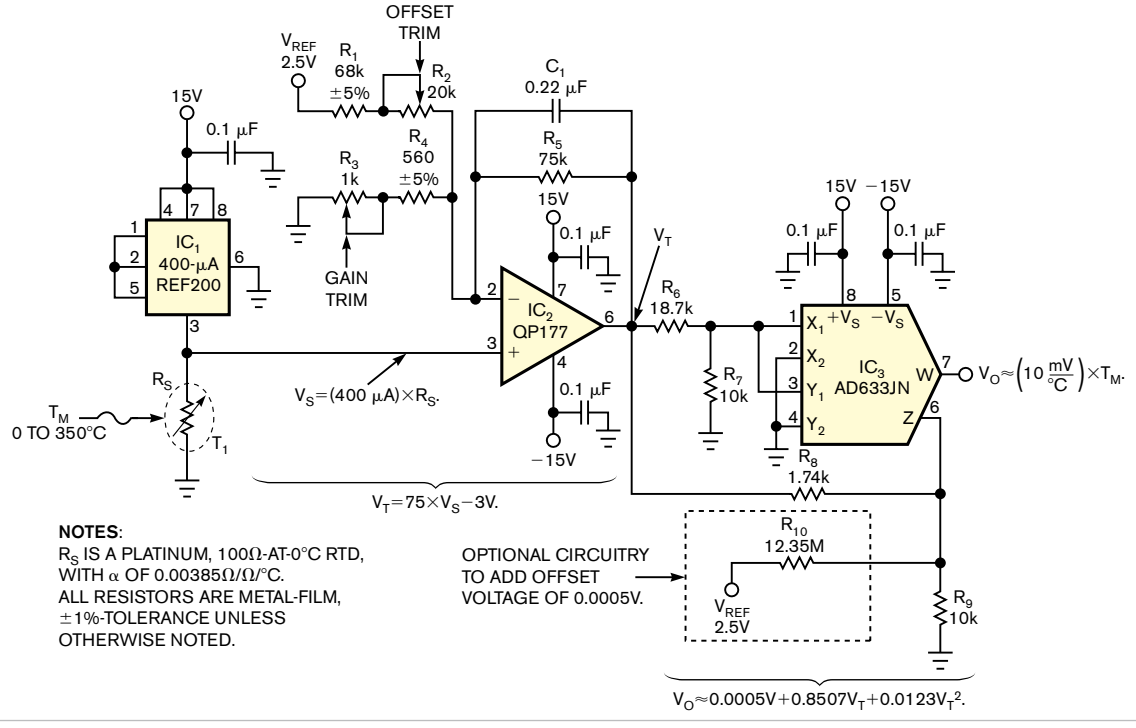

Figure 1 This RTD circuit uses a second-order polynomial to linearize the output of the sensor.

0.00392Ω/Ω/°C and follow the US curve. The circuit in **Figure 1** uses a standard RTD to measure temperature over the extended range of 0 to 350°C, an output voltage of 0 to 3.5V, and overall system accuracy greater than 0.5°C. The following linear **equation** expresses this sensor system:

$$V_O \approx \left(\frac{10\ mV}{°C}\right) T_M.$$

IC_1 is pin-configured to drive a constant current of 400 µA through the grounded sensor, T_1. Driving T_1 with this level of current—"zero-power" operation—keeps the worst-case power that the circuit dissipates in the sensor to less than 40 µW and reduces the self-heating errors to a second-order effect (**Reference 1**). Also, driving the RTD with a current source preserves its intrinsic nonlinearity and allows you to express the sensor's output voltage, V_S, as: 400 µA×R_S, where R_S is the resistance of the sensor.

IC_2 initially signal-conditions the sensor's output by first scaling the output voltage and then offsetting the result so that V_T is slightly larger than the 3.5V output at 350°C and that V_T equals 0V at 0°C. Adding gain and offset before linearization places less of a burden on the curve-fitting circuitry and helps to meet the system's precision specification. The combination of C_1 and R_5 implements a lowpass filter with a pole at approximately 10 Hz to remove power-supply noise. The following term describes the performance of IC_2 and its accompanying circuitry: $V_T = 75V_S - 3V$.

Next, an Excel spreadsheet creates the nonlinear-mathematical relationship between the voltage, V_T, and the system output, V_O (**Table 1**). The spreadsheet features 17 temperature entries—starting at 0°C, increasing in increments of 25°C, and ending at 400°C—for the measured temperature. Using a data set that extends beyond the intended measurement range of 350°C can reduce end errors in nonlinear systems. Values for R_S—which you derive from a standard RTD-resistance-versus-temperature table—and the **equations** allow you to compute V_S and V_T. The V_T and V_O columns are the input and output signals, respectively, for the linearization circuitry; you chart them using Excel's XY-scatter feature. You can use Excel's Trendline feature to create the following **equation**, the mathematical representation of the curve-fitting circuitry you need to linearize the sensor's output: $V_O = 0.0005V + 0.8597V_T + 0.0123V_T^2$. IC_3 and four 1%-tolerant resistors or, optionally, five resistors implement a second-order polynomial: $V_O = a + bV_T + cV_T^2$, where a is the offset term, b is the linear coefficient, and c is the square-term coefficient.

TABLE 1 EXCEL-SPREADSHEET DATA

Measured temperature (°C)	R_S (Ω)	V_S (V)	V_T (V)	V_O (V)
0	100	0.04	0	0
25	109.73	0.0439	0.292	0.25
50	119.4	0.0479	0.582	0.5
75	128.99	0.0516	0.87	0.75
100	138.51	0.0554	1.155	1
125	147.95	0.0592	1.439	1.25
150	157.33	0.0629	1.72	1.5
175	166.62	0.0666	1.999	1.75
200	175.86	0.0703	2.276	2
225	185.01	0.074	2.55	2.25
250	194.1	0.0776	2.823	2.5
275	203.1	0.0812	3.093	2.75
300	212.05	0.0848	3.362	3
325	220.91	0.0884	3.627	3.25
350	229.72	0.0919	3.892	3.5
375	238.88	0.0956	4.166	3.75
400	247.09	0.0988	4.413	4

The curve-fitting-circuit design begins by first wiring the four inputs of IC_3 to create a positive square term that is scaled at the chip's output by an internal scale factor of 1/10 V. Then, comparing terms, you find that the coefficient, c, must equal 0.0123. Because R_6 and R_7 form a voltage divider that attenuates the signal, V_T, you can express the coefficient with the following **equation**:

$$c = \frac{1}{10}\left(\frac{R_7}{R_6 + R_7}\right)^2.$$

Select a value for R_7—10 kΩ for this design—and then use the preceding **equation** to find the value for R_6.

Resistors R_8, R_9, and, optionally, R_{10} form a passive adder to create the offset term, a, and the linear coefficient, b. You apply the output of the passive adder directly to the Z input, Pin 6 of IC_3, which adds the offset and linear terms to the square term to form the system response at Pin 7. Again comparing these terms, note that the offset term must equal 0.0005V. The offset term is only 0.5 mV, and eliminating it would add an error of approximately 0.05°C, so you can initially neglect it. Then, because the linear term's coefficient, b, must equal 0.8507, you first select a suitable value for R_9 and use the following **equation** to solve for R_8: $b = R_9/(R_8 + R_9)$.

If you wish to design the optional circuitry and include the offset term, which is part of the passive adder, choose a stable 2.5V reference for V_{REF}, calculate the parallel combination of $R_8//R_9 = R_{EQ}$ (the equivalent resistance of R_8 in parallel with R_9), and solve for R_{10} using the following voltage-divider **equation**: $a = (R_{EQ}/(R_9 + R_{EQ}))V_{REF}$.

To calibrate this circuit, replace the sensor with a precision decade box. Set the decade box to simulate 0°C and adjust the offset trim of R_2 for an output of 0V at Pin 7 of IC_3. Next, set the decade box to simulate 350°C and adjust the gain trim of R_3 for an output of 3.5V. Repeat this sequence of trim steps until both points are fixed. The circuit in **Figure 1**—which includes optional circuitry—exhibits a worst-case measurement error at 250°C and 2.504V of 0.16%, or 0.4°C. Testing the circuit without the optional circuitry—the reference voltage and R_{10}—shows no discernible improvement in precision. EDN

REFERENCE

1 "IC Generates Second-Order Polynomial," *Electronic Design*, Aug 5, 1993, www.elecdesign.com/Articles/Index.cfm?AD=1&ArticleID=11502.

Isolated supply powers DVM module

Richard Dunipace, Fairchild Semiconductor, Irving, TX

Low-cost DVM (digital-voltmeter) modules are economical and can significantly reduce design time for instrumentation. Yet, these modules also involve a significant number of design challenges. For example, their inputs are not isolated from the power supply, so you must add an isolated power supply. This task can both consume critical design time and add to system costs. Additionally, many uses for the modules require one- to four-cell-battery operation, and the modules require approximately 9V, translating to operation from 0.7 to 6V if you use new batteries until they are fully discharged. This wide input range also means that you should regulate the power-supply output.

DVM modules also have low parts count, and you can implement them using off-the-shelf components. Optionally, the modules can operate with input voltages as low as 0.25V if you replace the silicon transistors with germanium devices. However, germanium transistors are relatively expensive, so use them only in applications requiring low-input-voltage operation.

The power-supply design in **Figure 1** is a blocking oscillator that operates as a flyback converter with fixed on-time and variable off-time. The variable off-time regulates how often the transformer charges and delivers power to the load. The blocking oscillator consists of NPN transistor Q_2, transformer T_1, and capacitor C_2. The conductance of PNP transistor Q_1 controls the off-time of the oscillator in conjunction with C_2. The output of the transformer conducts to the energy-storage capacitor, C_3, through diode D_2 during transformer flyback. The error amplifier and optocoupler, IC_1, monitors the voltage across C_3. When the voltage at resistive divider R_4-R_5 exceeds 2.5V, the optocoupler conducts more and reduces the conduction of transistor Q_1, increasing the time required for the next power cycle. EDN

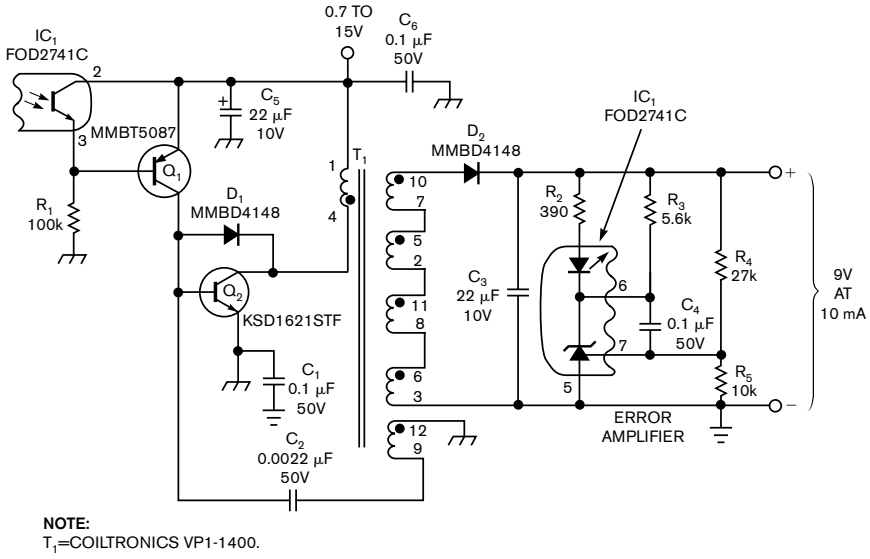

Figure 1 This isolated flyback supply powers a digital-voltmeter module from 0.7 to 15V.

IC performs delayed system reset upon power-up

Goh Ban Hok, Infineon Technologies Asia Pacific Ltd, Singapore

In most applications, the $\overline{MR}$ (manual-reset) pin usually connects to a switch to create a manual-reset signal to the supervisory chip. Subsequently, after a predetermined time-out-active period, it goes back to the high state in an active-low reset. A manual reset is a good feature for most applications; however, it requires human intervention to create the reset. In some applications, a manual reset could be a hassle because you must perform it each time the system powers up.

Further, applications involving embedded microprocessors can require the reset output to hold high—that is, inactive—for a certain period of time before you can apply the reset, or active low. The circuit in **Figure 1** proves useful during power-up when there is no need to press the reset button once the device powers up, because reset occurs automatically with the predetermined hold time before you apply the reset-low signal.

The circuit employs a reset-supervisory chip with the $\overline{MR}$ pin and active-low output, $\overline{RESET}$. Normally, the $\overline{MR}$ input has an internal pullup resistor with a value of 20 to 50 kΩ. During power-up, this $\overline{MR}$ internal resistor charges up capacitor C_1 to the maxi-

mum value to V_{DD} at the positive side. To create an $\overline{MR}$ reset input to the supervisory chip, its $\overline{MR}$ input must receive an active-low ground signal, requiring transistor Q_1 to turn on. The turn-on-time period depends on the RC-time constant of R_1 and C_2. These two components determine when Q_1 turns on and thus provide an adjustable hold time for the $\overline{RESET}$ output to hold high. To increase the hold time, simply increase the RC-time constant of R_1 and C_2.

The supervisory reset chip asserts its $\overline{RESET}$ output only when the voltage at the $\overline{MR}$ pin exceeds the threshold-trigger voltage and the supervisor's internal reset period has elapsed. This time-out period filters any short input-voltage transients. Because of Q_1's turn-on, the negative side of C_1 becomes grounded. Because the positive side of C_1 cannot instantly change its polarity, it pulls low and slowly charges up again through the internal pullup resistor of the $\overline{MR}$ input. When it reaches the threshold voltage of the reset chip, it then asserts the reset once it reaches the time-out period of the chip. The selection of C_1 is not critical. However, its value should be sufficiently large—0.1 to 10 µF, for example—that the RC time constant for C_1 and the internal pullup resistor are large enough. This value ensures that C_1 holds the voltage low at $\overline{MR}$ for at least 1 µsec.

The transistor remains on after C_2 charges toward the biased voltage of Q_1. At the next power-up or when you manually reset the circuit by pressing the pushbutton switch, the transistor discharges C_2. Once this action happens, Q_1 turns off. R_1 charges up the negative side of C_1 to the supply voltage, V_{DD}. Because the positive side of capacitor C_1 cannot change instantly, it appears to be charged to $2V_{DD}$. However, the protection diode, D_1, clamps C_1's voltage to just V_{DD} plus the diode's turn-on voltage. The cycle repeats once C_2 charges enough to again turn on Q_1. EDN

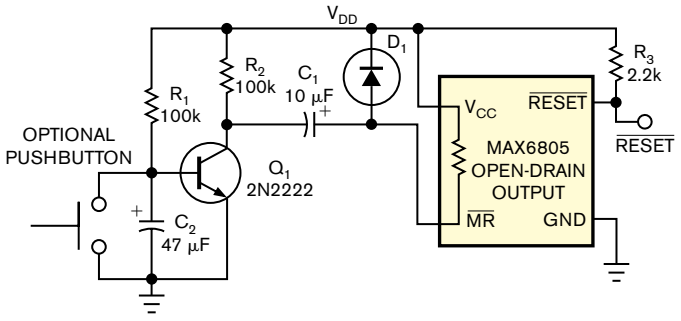

Figure 1 This simple circuit automatically resets a microcontroller upon power-up.

One microcontroller pin drives two LEDs with low quiescent current

Antonio Muñoz, Laboratorios Avanzados de Investigación del I3A, Zaragoza, Spain, and Arturo Mediano, PhD, GEPM University of Zaragoza, Zaragoza, Spain

The basis for this Design Idea is a circuit that uses three resistors and a microcontroller-I/O pin to work as input high impedance or output to independently drive two LEDs (**Reference 1**). The idea sounded good for this design, mainly because of the lack of spare I/O pins in the microcontroller and the simplicity of the implementation. Unfortunately, you cannot use the circuit in battery-powered designs because it exhibits a current leakage on the order of 2 mA even with both LEDs off. This Design Idea modifies that circuit, using only one I/O pin to drive the two LEDs but with a low current drain (**Figure 1**). Although the circuit uses a couple of diodes and a resistor, the price and the component count are low.

THE LEDs START DIMMING AT APPROXIMATELY 4V WITH A CURRENT OF 80 µA AND ARE FULLY ON WITH 4.4V AT A CURRENT OF 1 mA.

The basis for the operation of both circuits is the nonlinear characteristic of a diode, in which current grows exponentially with the voltage applied across it. To describe the operation, suppose that the microcontroller pin is configured as an input, leaving the pin in high impedance. In the first circuit, assume that LEDs need a voltage of approximately 1.5V to turn on and that the small-signal-diode voltage drop is approximately 0.6V (**Figure 1a**). So, to turn on both LEDs, you theoretically need 4.2V. In practice, the LEDs start dimming at approximately 4V with a current of 80 µA and are fully on with 4.4V at a current of 1 mA. With 3.3V, leakage current is merely 2.41 µA. The nominal voltage for this circuit can be slightly lower than 3.3V, but, in that case, you should use Schottky diodes.

The second circuit is for supply voltages greater than 5V (**Figure 1b**). Using the values in the **figure**, the LEDs start

dimming with 7V at 74-µA current and are fully on with 8.5V at 1 mA, remaining off for a 5V supply at 1.53 µA.

To turn on the LEDs, you must configure the microcontroller's I/O pin as an output; an output value of one turns on the lower LED, and a value of zero turns on the upper LED. If both LEDs must appear to be on, your program can cycle the port pin between one and zero with a frequency greater than 50 Hz. To calculate the value of the resistor in both cases, the following formulas apply: $R=(3.3V-V_D-V_{LED})/I_{LED}$ (**Figure 1a**), and $R=(V_{CC}-V_Z-V_{LED})/I_{LED}$ (**Figure 1b**), where I_{LED} is the desired LED-on current, V_D is the voltage across the diode when an I_{LED} current flows through it, V_Z is the zener-diode voltage, and V_{LED} is the forward voltage across the LED when an I_{LED} current flows through it. You should use a Schmitt trigger or an analog input for the I/O pin to avoid excessive current draw. EDN

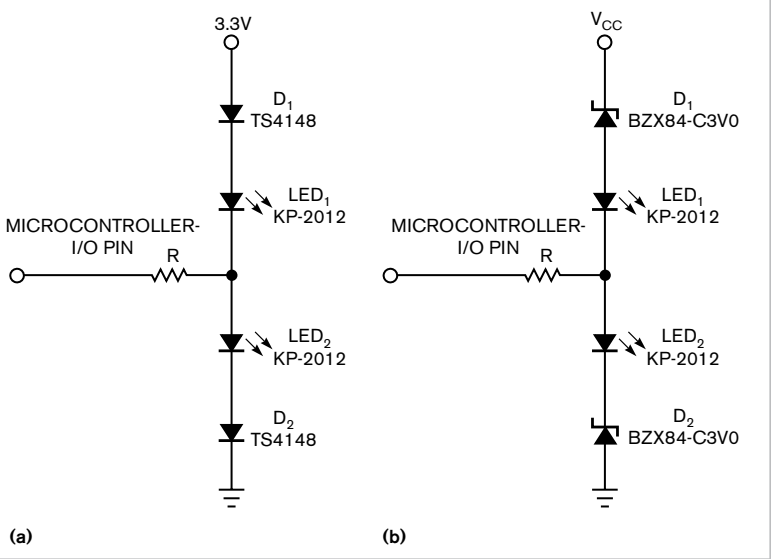

Figure 1 In these simple circuits, the LEDs need a voltage of approximately 1.5V (a) or more than 5V (b) to turn on. The circuits allow a battery-powered microcontroller to control two LEDs with only one I/O pin.

REFERENCE

1 Pefhany, Spehro, "Circuit Controls Two LEDs With One Microcontroller Port Pin," *Electronic Design*, April 1, 2002, http://electronicdesign.com/Articles/Index.cfm?AD=1&ArticleID=1683.

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NE555 timer sparks low-cost voltage-to-frequency converter

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In 1971, Signetics—later Philips (www.philips.com)—introduced the NE555 timer, and manufacturers are still producing more than 1 billion of them a year. By adding a few components to the NE555, you can build a simple voltage-to-frequency converter for less than 50 cents. The circuit contains a Miller integrator based on a TL071 along with an NE555 timer (**Figure 1**). The input voltage in this application ranges from 0 to −10V, yielding an output-frequency range of 0 to 1000 Hz. The current of C_1 is the function of input voltage: $I_C=-V_{IN}/(P_1+R_1)$.

As the voltage on C_1 reaches two-thirds of V_{CC}, the 555's internal discharge transistor opens, and the voltage on C_1 returns to one-third the voltage of V_{CC}, the lower comparator threshold. At one-third this voltage, the discharge transistor switches off, and C_1 again starts charging. The NE555's output is high while C_1 is charging and low while C_1 is discharging. The product of the input voltage and the charging time of C_1 is constant. Because the discharge time is shorter than the charging time, the following **equation** results for the output frequency: $f_{OUT}\sim V_{IN}/(P_1+R_1)\times C_1\times 1/3V_{CC}$.

P_1 calibrates the relationship between the output frequency and the input voltage. Because the discharge interval is approximately 30 µsec, the accuracy of the voltage-to-frequency conversion decreases as the frequency increases. If you assign 100 Hz to −1V and 1000 Hz to −10V, the error of conversion ranges from 0.3 to 3%. If you use P_1 to calibrate the output frequency in the middle of the input-voltage range at −5V, then the conversion error will be less than 1.3% over the entire range. To improve performance, C_1 should have a low dissipation factor. You can diminish temperature dependence if R_1 has a low temperature coefficient and P_1 is a multiturn, ceramic-metal potentiometer. EDN

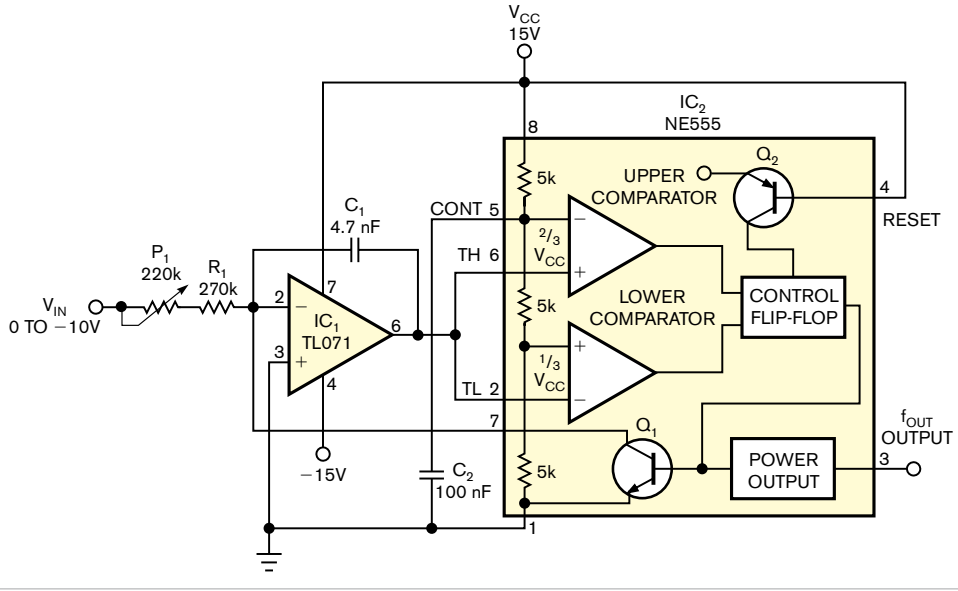

Figure 1 Preceding an NE555 timer with a Miller integrator yields a voltage-to-frequency converter that costs less than 50 cents.

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Optoisolators compute watts and volt-amperes

W Stephen Woodward, Chapel Hill, NC

A decade or so ago, I designed a simple circuit that included a quad optoisolator arranged in a full-wave analog-multiplier bridge (**Figure 1**). It sensed and calculated watts of ac-power consumption and ignored any reactive component in the load. The circuit's principle of operation relies on the fact that the LEDs of the bridge, like any other device with a semiconductor junction, have a dynamic conductance that's directly proportional to current: approximately 19 mS (millisiemens)/A at 25°C. Both the line voltage and load-current-proportional sense voltage, which the 0.001Ω copper shunt develops, modulate this current. The approximately 0.4%/°C temperature coefficient of the copper compensates most of the temperature dependence of the LEDs' conductances.

The circuit in this Design Idea is an elaboration on that older circuit. It acquires not only watts, but also volt-amperes and so makes possible an estimation of power factor—watts divided by volt-amperes. The right-hand side of the circuit in **Figure 2** is simply a half-wave version of the older circuit. The left-hand side is similar but substitutes rectified-dc excitation of its half-wave bridge for the ac excitation of the left-hand side. The analog product of instantaneous load current times the average voltage optically couples to phototransistor Q_4/D_4, which A_2 amplifies and the Q_5 through Q_8 transistor array rectifies to provide an analog voltage proportional to load volt-amperes. EDN

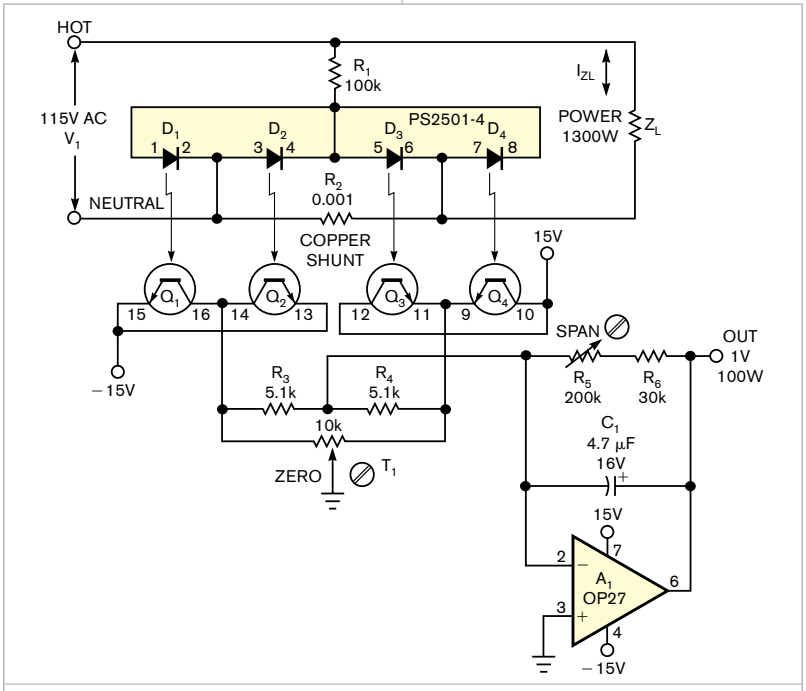

Figure 1 A quad optoisolator arranged in a full-wave analog-multiplier bridge senses and calculates watts of ac-power consumption and ignores any reactive component in the load.

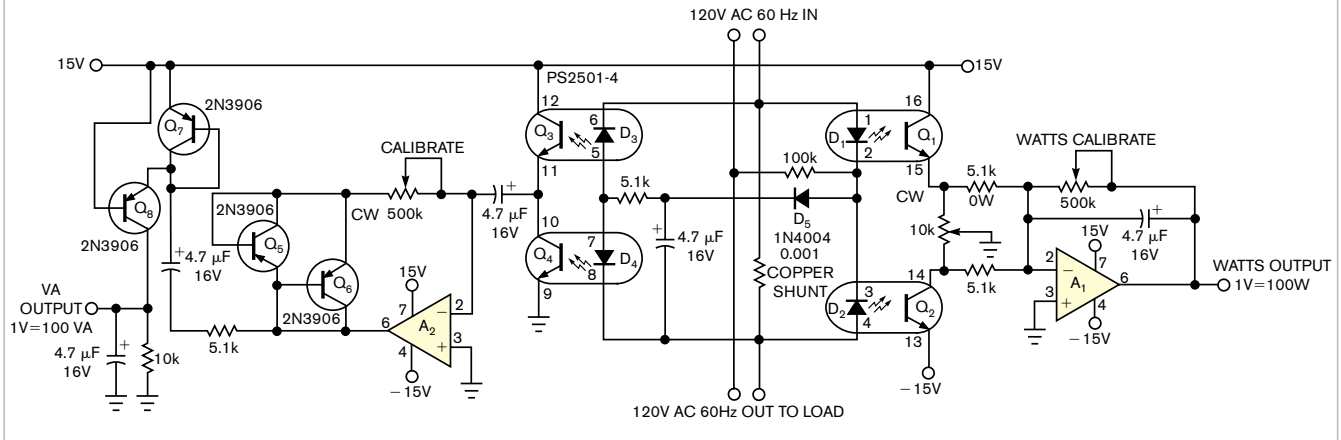

Figure 2 The right-hand side of this circuit is simply a half-wave version of the circuit in Figure 1. The left-hand side is similar but substitutes rectified-dc excitation of its half-wave bridge for the ac excitation of the right-hand circuit.

Single-supply circuit measures −48V high-side current

Wenshuai Liao, Analog Devices, Beijing, China;
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The nominal −48V rail, which finds wide use in wireless base stations and other telecommunications equipment in network central offices, can vary from −48 to −60V. Measuring its current draw typically requires components that operate on ±15V dual supplies. Eliminating the negative supply would reduce system complexity and cost. This Design Idea uses an AD629 difference amplifier and an AD8603 operational amplifier, both from Analog Devices (www.analog.com), to measure current at −48 to −60V and operates from a single positive-power supply (**references 1** and **2**).

Figure 1 shows how the AD629 and AD8603 measure current in the presence of a −48V common-mode voltage. The following **equations** demonstrate how the AD629 difference amplifier can condition voltages beyond its supply ranges: $V_{COM\_MAX}=20\times(V_S-1.2)-19\times V_{REF}$, and $V_{COM\_MIN}=20\times(-V_S+1.2)-19\times V_{REF}$. With a 5V reference, the common-mode input range is −71 to +121V. The current, I, flows through the shunt resistor, R_S, causing a differential voltage, which the difference amplifier senses. The AD629 has a fixed gain of one, so the output voltage is $I\times R_S+V_{REF}$. The AD8603 functions as a subtractor so that it can reject the common-mode voltage, V_{REF}, and apply gain to the signal of interest, $I\times R_S$. A factor of 20 amplifies the signal to span the 2.5V full-scale range of the ADC.

This Design Idea uses the AD8603 because it has low input-bias current and low offset drift. In addition, the rail-to-rail output allows it to share the same supply as the ADC. In this stage, the subtractor rejects the 5V common-mode signal from the voltage reference. The four resistors that form the subtractor must have matched ratios to obtain maximum common-mode rejection. If you cannot obtain tightly matched resistors, you can use an AD623 single-supply instrumentation amplifier in place of the AD8603, ensuring high common-mode rejection.

Offset, input-bias-current, and common-mode-rejection errors from both amplifiers result in a 163-mV maximum error at the output of the AD8603. This calculation assumes resistors with a 0.01% ratio match. The circuit was verified on the bench using 50-, 100-, and 200-mΩ shunts for R_S. EDN

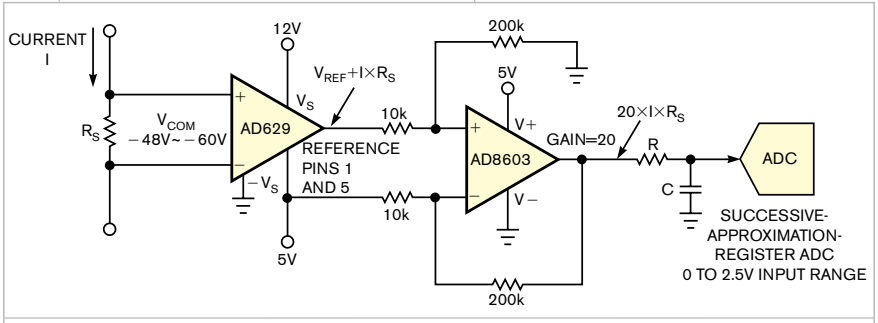

Figure 1 The AD629 and AD8603 measure current in the presence of −48V common-mode voltages.

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Three-state switch interface uses one microcontroller pin

Kartik Joshi, Netaji Subhas Institute of Technology, New Delhi, India

Human interfaces for electronic gadgets sometimes require three states for control. A single-axis joystick has states to define motions to the right, to the left, and with no motion. Similarly, a timer has control buttons that allow the timer to increment, decrement, and remain untouched. Engineers usually create these interfaces by using two independent pushbuttons, requiring two microcontroller pins. This Design Idea presents a way to sense three states of an SPDT (single-pole/double-throw) switch with a center-off state, using only a single pin of

TABLE 1 STATUS OF THE PIN FOR VALUES OF THE PORT AND THE DDR REGISTERS

	DDR bit=0 Port bit=0	DDR bit=0 Port bit=1
Pin connects to V_{DD} through a resistor	Pin bit=1	Pin bit=1
Pin connects directly to ground	Pin bit=0	Pin bit=0
Pin connects to ground through a very-high-resistance path	Pin bit=0	Pin bit=1

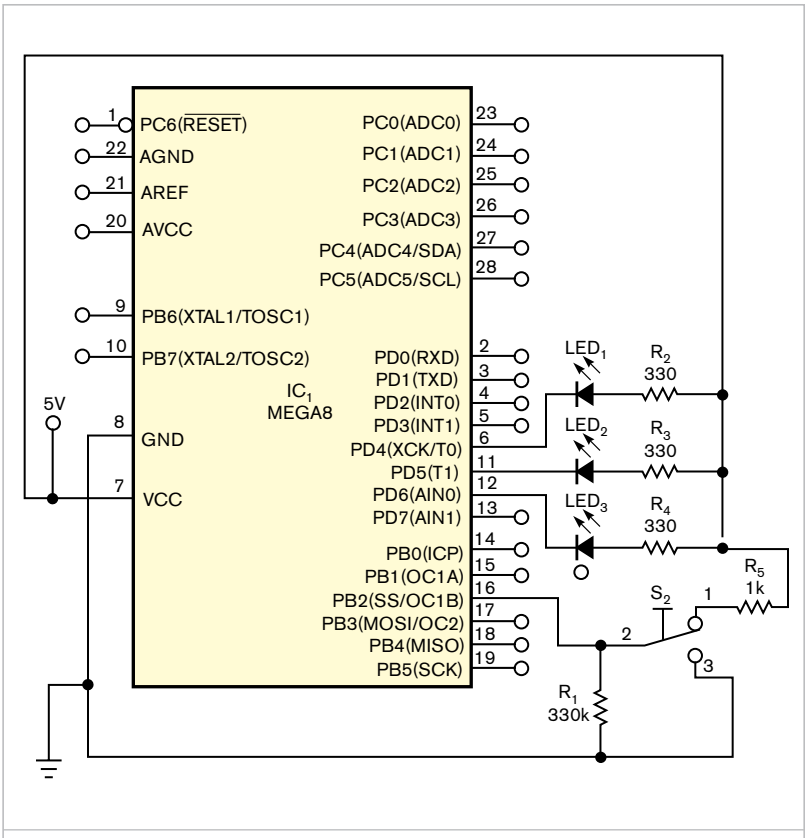

Figure 1 Using only one I/O pin, this circuit and a simple program can sense the state of a three-position switch.

Atmel's (www.atmel.com) ATmega8 microcontroller (**Reference 1** and **Figure 1**). **Listing 1**, which is available at the Web version of this Design Idea at www.edn.com/080221di1, is a simple program for the circuit.

The status of the pin of the microcontroller depends upon values of the DDR bit, the port bit, and its external connection. The microcontroller's pin connects to ground using pulldown resistor R_1 with resistance, typically, of a few hundred kilohms to impress the high-impedance state on the pin. You set the DDR register to zero. When the user toggles the switch to Position 1, the pin connects to V_{DD} through resistor R_5, and the pin bit is one, regardless of the value of the port bit. When the user toggles the switch to Position 3, the pin is grounded, and the pin bit is zero, regardless of the value of the port bit. In the center-off state, the pin bit follows the port bit. **Table 1** summarizes the states of the pin for different values of the port and the external input. EDN

REFERENCE

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AC-continuity tester finds single-ended faults in cables

Kevin Bilke, Maxim Integrated Products, Fleet, Hants, UK

An ac-based continuity tester for front-line test-and-repair jobs provides a simple go/no-go test for localizing faults in multiconductor cables (**Figure 1**). Open circuits are more likely to occur at the connector ends. This tool helps to identify the faulty end, thereby avoiding the risk of damaging a good connector by opening it. It's also useful for testing an installed cable for which both ends are in different locations. The circuit injects an ac signal on one wire of a cable and then looks for an absence of capacitive coupling to the other wires. After locating this fault, the circuit identifies the open wire and allows you to open and repair the correct cable end.

One end of a bad cable typically shows good ac continuity, and the other end typically has one or more connector pins with no ac continuity. Because a short in the cable appears as a good connection, the operator can easily confirm that the tester is operating correctly by simply shorting its test leads together. The first section of IC_1, a Maxim (www.maxim-ic.com) MAX9022 low-power dual comparator, forms a relaxation oscillator operating at approximately 155 kHz. It produces a peak-to-peak output signal approximately equal to the supply voltage, which feeds to a connector of the cable under test. The second section of the circuit processes any ac signal that the interlead capacitance picks up. A pair of silicon diodes first rectifies that signal and then integrates the rectified signal on storage capacitor C_5. Bleed resistor R_5 provides some noise immunity and helps to reset the capacitor between tests.

Output resistor R_4 and input capacitor C_4 provide limited circuit protection. The circuit indicates open for any test-cable capacitance below 100

pF. Thus, a standard mains-test lead, whose typical lead-to-lead capacitance is 200 pF, would test OK. The circuit is also immune to false triggering that the 60-Hz pickup from the power lines causes. Because the typical current draw of this low-power circuit is less than 40 µA, the circuit can usually operate from battery power in the form of three 1.5V AA or AAA cells. Many low-cost alternatives are available for the output device—for example, you could use a dc-activated piezoelectric buzzer—and most feature a suitably wide range of operating voltages. The 100-nF capacitors are standard ceramic decoupling capacitors, and the circuit contains no critical passive components. The comparator's high-side drive is somewhat better than its low-side drive, so it should source rather than sink current to the indicator device. D_1, D_2, and D_3 are silicon diodes. EDN

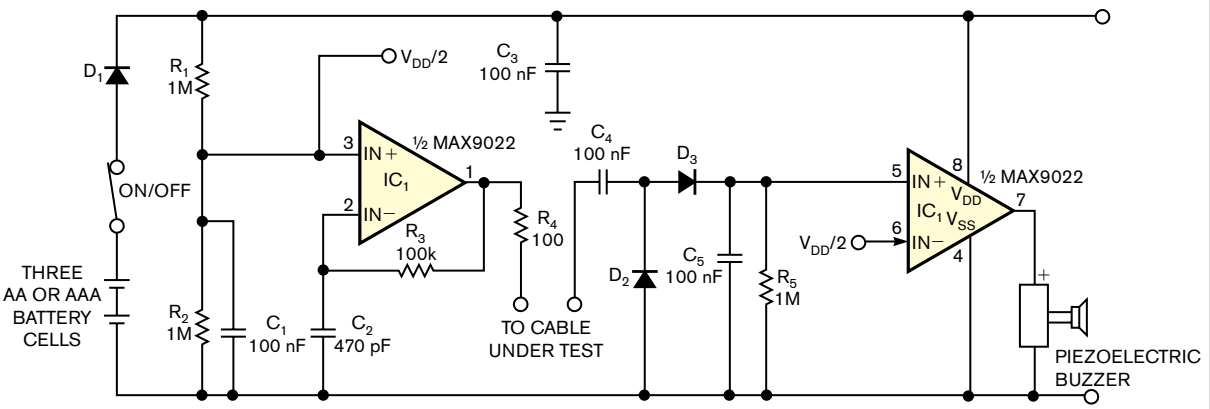

Figure 1 Based on a low-power dual comparator, this ac-continuity tester locates open-circuit pins in a cable.

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Audio equalizer features transimpedance Q-enhancement topology

Herminio Martínez, Encarna García, and Eva Vidal,
Technical University of Catalonia, Barcelona, Spain

In general, audio equalizers need second-order bandpass filters. Such cells require an easy and independent tuning of their parameters: the natural or central frequency, ω_0; the quality factor, Q; and the maximum bandpass gain, k. The use of cells with independent adjustments could require state-variable topologies. Unfortunately, this sort of structure usually needs at least three operational amplifiers. The basis for an alternative uses SAB (single-amplifier-biquadratic) filters. These cells allow obtaining second-order bandpass filters, but they have two main drawbacks: The quality factors that you can obtain with these cells have a practical maximum limit, and you cannot independently tune the three characteristic parameters.

This Design Idea instead uses the TQE (transimpedance-Q-enhancement) structure in an audio-equalizer (**Figure 1**). This cell has two advantages when you use it in equalizer circuits: You can adjust the three characteristic parameters in an independent way, but it uses only two operational amplifiers per cell. **Reference 1** presents the generic TQE topology. **Figure 1** shows the configuration that implements a bandpass filter based on the generic structure. This structure, which processes current-input signals, shows low-impedance input without the resistor R_{IN}. Considering that R_1 and R_3 are equal in value and that all the capacitors are equal to C, the transimpedance, Z(s), is:

$$Z(s)=\frac{V_{BP}(s)}{I_{IN}(s)}=\frac{R_1^2C_s}{R_1^2C^2s^2+(2-R_1/R_2)R_1Cs+1}.$$

However, by adding R_{IN}, the input has high impedance, allowing the processing of voltage input signals because R_{IN} provides the required voltage-to-current conversion. In this way, the input-to-output transfer function, H(s), is:

$$H(s)=\frac{V_{BP}(s)}{V_I(s)}=\frac{R_1}{R_{IN}}\frac{s/R_1C}{s^2+s(2-R_1/R_2)/R_1C+1/R_1^2C^2}.$$

Thus, the circuit implements a second-order bandpass-transfer function; the following **equations** yield the central frequency, ω_0, and the quality factor, Q:

$$\omega_0=1/R_1C;\ Q=\frac{R_2}{2R_2-R_1},$$

and the value of the gain, k, is:

$$k=\frac{R_1}{R_{IN}}Q=\frac{R_1}{R_{IN}}\left(\frac{R_2}{2R_2-R_1}\right).$$

Thus, you can make the adjustments of ω_0, Q, and k with R_1, R_2, and R_{IN}, respectively.

You can use the bandpass cell in **Figure 1** in an audio equalizer. **Figure 2** shows a possible implementation of a

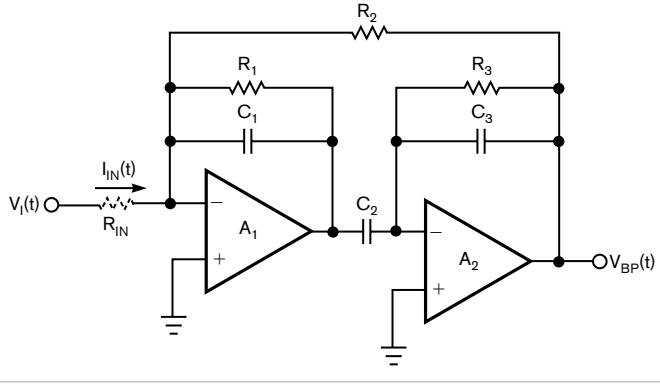

Figure 1 Adding R_{IN} to this bandpass filter based on a TQE structure causes the circuit to show high input impedance.

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graphic equalizer. The basis for the circuit is a bank of bandpass TQE cells. Note that the cells are TQE with low-impedance input. Thus, the input network's R_{IN} converts $V_{IN}(t)$ and $V_{OUT}(t)$ to the corresponding input current, $I_{IN}(t)$. Adjusting potentiometer R_{IN} with its wiper to the far left ($X_I \rightarrow 0$) accentuates the frequency band that the corresponding cell covers in the overall circuit output. On the other hand, positioning the wiper of R_{IN} to the far right ($X_I \rightarrow 1$) causes a large amount of negative feedback to occur at this same frequency, thus causing attenuation in the forward-signal path. In each case, the remaining filters' TQE_I receives percentages of both the input signal, $V_{IN}(t)$, and the output signal, $V_{OUT}(t)$, in ratios that their respective potentiometer settings determine.

You can derive the overall transfer function from **Figure 2**. The output voltage, $V_{OUT}(s)$, of the equalizer is:

$$V_{OUT}(s) = -\left\{V_{IN}(s) + A\sum_{I=1}^{N} Z_I(s)\left[\frac{V_{IN}(s)}{X_I R_{IN}} + \frac{V_{OUT}(s)}{(1-X_I)R_{IN}}\right]\right\},$$

where $Z_I(s)$ are the cells' transimpedances, and

$$A = \frac{R_B}{R_A}.$$

If you define

$$H_I(s) = Z_I(s)/R_{IN},$$

then the transfer function of the equalizer becomes

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{1 + A\sum_{I=1}^{N}\frac{H_I(s)}{X_I}}{1 + A\sum_{I=1}^{N}\frac{H_I(s)}{1-X_I}}.$$

Now, you can investigate the effect of various settings of the potentiometers. For example, in the case with all of the controls centered, X_I equals 0.5 for each band. Then, $V_{OUT}(s)/V_{IN}(s) = -1$, as you would expect in a typical equalizer's response. Setting band I=1 to a value of X_I and all other bands flat—that is, $X_I = 0.5$ for I=2, 3, ... n), you obtain:

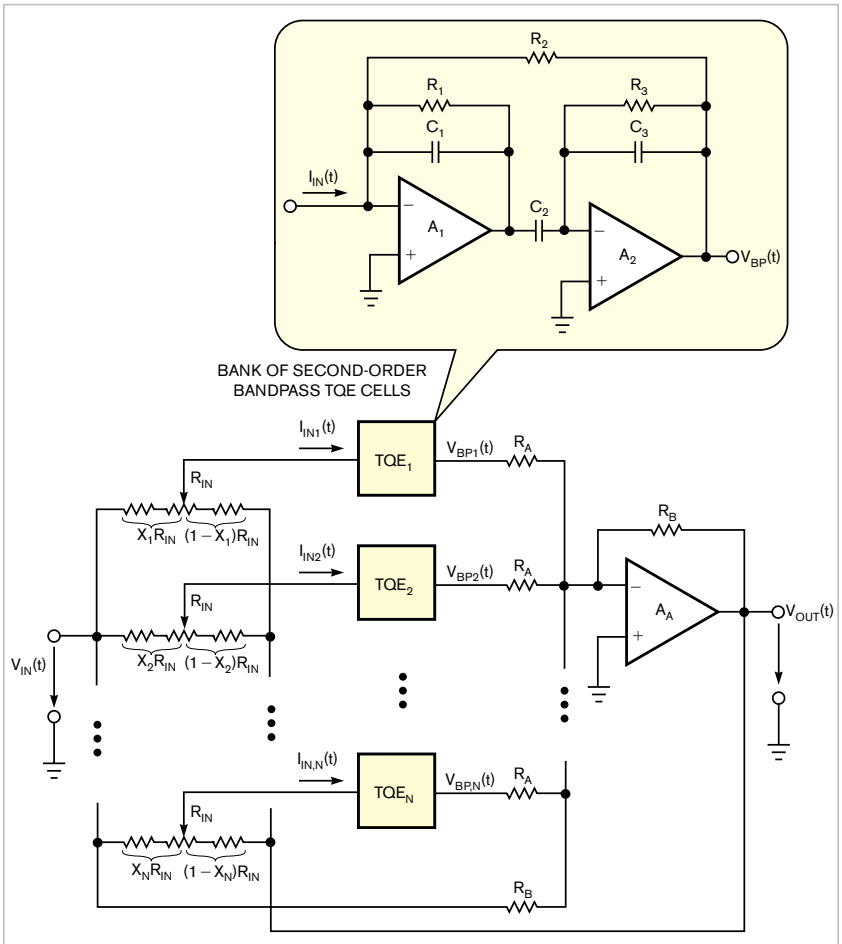

Figure 2 The TQE cells in this graphic equalizer have low-impedance inputs.

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{s^2 + \left(\frac{\omega_{01}}{Q_1}\right)\left[1 + \frac{1}{1+2AM}\left(\frac{A}{X_1} - 2A\right)k\right]s + \omega_{01}^2}{s^2 + \left(\frac{\omega_{01}}{Q_1}\right)\left[1 + \frac{1}{1+2AM}\left(\frac{A}{1-X_1} - 2A\right)k\right]s + \omega_{01}^2},$$

which represents a bandpass filter with unity gain, or 0 dB, in the stopband and a gain of A_O at resonance, and M is a constant representing the average value of the complete summation. M is approximately 1.3, or approximately 2.3 dB (**Reference 2**). Note that this gain can be higher—that is, boost—or lower than one. Considering as typical values M=1.3, A=1, and k=1, you can simplify the **equation** for passband gain A_O, which is equal to the ratio of the s term coefficients, as:

$$A_O = \frac{3.6 + \left(\frac{1-2X_1}{X_1}\right)}{3.6 + \left[\frac{1-2(1-X_1)}{1-X_1}\right]}.$$

As an example, consider the case of an octave-band equalizer with 10 bands. In this case, the value of the quality factor for each band is about 1.42 (**Reference 3**), and the typical central frequencies of the 10 sections are 32 Hz to 16 kHz. Adjusting R_{IN} in the input of the cell TQE with its wiper to the left boosts the frequency band that the corresponding cell covers in the overall circuit output. For instance, if X_I is 0.1, then A_O is approximately 13 dB. On the other hand, positioning the wiper of R_{IN} to the right causes attenuation in the forward-signal path. So, if X_I is 0.9, then A_O is

approximately −13 dB. You must have a minimum input impedance in each cell for the input voltage, $V_{IN}(t)$, and the feedback voltage, $V_{OUT}(t)$. Thus, the inclusion of two resistors in series with each potentiometer R_{IN} in **Figure 2** guarantees this resistance. EDN

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AMI-to-NRZI-direct-conversion circuit tolerates unequalized pulse tails

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

AMI (alternate-mark inversion) is a three-level—positive, zero, negative—copper-cable transmission code with the useful property of having no dc component for ease of ac coupling using capacitors or line-coupling transformers and a spectral peak at one-half the symbol rate. The zeros symbols transmit as 0V; the ones symbols transmit at half-unit intervals with alternating-line polarity to maintain the dc balance.

An interesting feature of the three-level AMI code is that you can easily translate it directly from and to the two-level NRZI (non-return-to-zero-inverted) code. The basis for NRZI is a transition, not a level; an NRZI edge in either the rising or the falling direction signifies a logic one. A lack of transition in a given symbol interval signifies a logic zero. Thus, the NRZI code is invertible without destroying the logic sense. Absolute level is meaningless. The only information content is the change or no change of level at the expected transition time. Likewise, the AMI code is invertible; you need not worry about the twisted-pair polarity. **Figure 1** shows the relationships between NRZ (non-return-to-zero), NRZI, and AMI codes.

The usual received-data-recovery method for AMI comprises a pair of voltage-level slicers, or comparators, that combine the transmission-line-positive and -negative marking symbols into a two-level RZ code (**Figure 2a** through **d**). The symbols are then further changed into the standard NRZ-logic representation (not shown), typically with a D-type sampling flip-flop or similar circuitry.

One impediment to successful AMI transmission over distance is the "pulse-tail"-cable artifact. When you do not drive the cable to a positive- or a negative-marking pulse, such as in a zero following a one, the last transmitted marking pulse extends in time and slowly decays to zero. This effect becomes more pronounced as the cable gets longer, and, unless you eliminate it through the use of a frequency-equalization network that matches the cable-length and -attenuation characteristics, it will wreak havoc on the data-recovery slicers (**Figure 2e** and **f**).

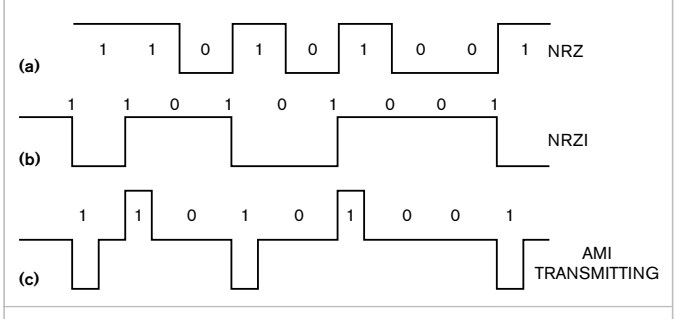

Figure 1 These waveforms illustrate an NRZ-to-NRZI-to-AMI conversion. Only when NRZ (a) is at logic one does NRZI (b) change at bit boundaries. AMI marks at the polarity of the NRZI transition (c).

You can easily convert two-level NRZI to three-level AMI through a straightforward algorithm that you can implement with a few gates and line drivers, a transformer, and a delay line if the system clock is unavailable. If no NRZI transition exists, transmit nothing for that symbol interval. For every rising NRZI edge, transmit a marking pulse, usually with a duration of one-half-symbol interval. For convenience, assign this pulse polarity as positive. For every falling NRZI edge, transmit a similar marking pulse of the opposite polarity to that of the rising edge. This step automatically creates the alternate marking polarities. Again for convenience, assign this pulse polarity as negative.

Recovering the NRZI directly from the AMI is likewise a straightforward algorithm (**Figure 3a** and **b**). If there is no received-voltage-threshold crossing of opposite polarity to that of the previous marking-threshold crossing, retain the last received-marking state at logic high or logic low. If the received-AMI voltage crosses a threshold at a polarity opposite to the current state of the detector output, toggle the detector output to the state associated with that new polarity. Again, for convenience, if the AMI-pulse-threshold crossing is positive above the midlevel, or zero, toggle the detector output to a rising edge; if the AMI-pulse-threshold crossing is negative below the midlevel, or zero, toggle the detector output to a falling edge.

From these algorithms, you can see that this receiving method directly translates the AMI code into the NRZI code. Also, by its requirement for alternate marks to cross the zero level and the subsequent opposite threshold to cause an output toggle, this method is immune to the marking-pulse tails that poorly or nonequalized lengths of transmission line cause (**Figure 3c** and **d**). This effect gives rise to the possibility of eliminating the amplitude/frequency-equalizer portion of the receiver for high-bit-rate data transmission on medium-length copper cables.

A circuit that fulfills the receiver algorithm is a Schmitt trigger with an upper trip point and a lower trip point that are above and below the midlevel of the AMI three-level signal. You can easily set this point as a hardware bias with ac coupling of the dc-balanced AMI signal because there is virtually no baseline wander with AMI (**Figure 4**). Gain and drive level are not critical as long as sufficient pulse amplitude exists to cross the trip thresholds. If the signal is excessively strong or the trip thresholds are close to the midsignal level, the circuit still correctly translates data as long as no end-of-pulse ringing crossing into the opposite trip thresholds occurs. If this scenario occurs, pulse tails are beneficial, and you can artificially introduce them for the minimum operational cable length if necessary. For some oscilloscope-photo waveforms using the ECL Schmitt trigger of **Figure 4**, go to www.edn.com/080306di.EDN

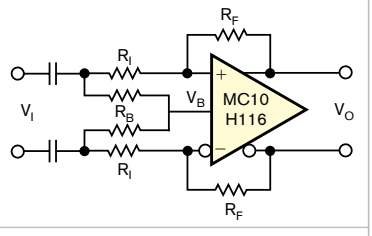

Figure 4 An MC10 H116 configured as a Schmitt-trigger circuit uses an ECL-amplifier stage. R_F supplies the positive feedback; the ratios of R_F to R_I set the hysteresis and thus the upper- and lower-trip-point-voltage levels. To remain within the linear region of the MC10 H116 transfer function, ±100 to 200 mV from center zero level is suggested.

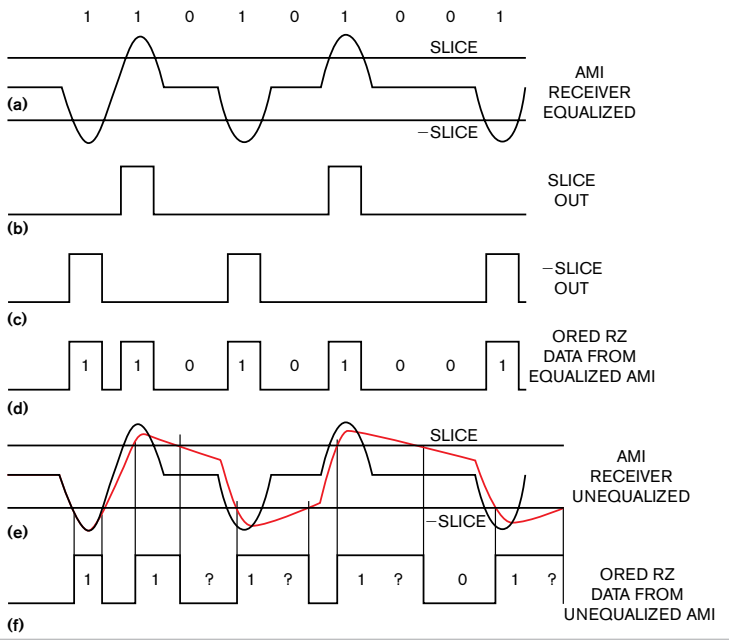

Figure 2 These waveforms show the usual transcoding of AMI to RZ. Two digital comparators slice bandlimited, equalized AMI (a). ORing the comparators, one for positive polarity (b) and one for negative polarity (c) produces RZ data (d). The digital comparators may themselves be Schmitt triggers for clean switching and immunity to small noise levels riding on the analog AMI. Unequalized AMI, superimposed on equalized AMI (e) causes the marking pulse tails, resulting in a highly distorted and error-filled RZ data waveform (f).

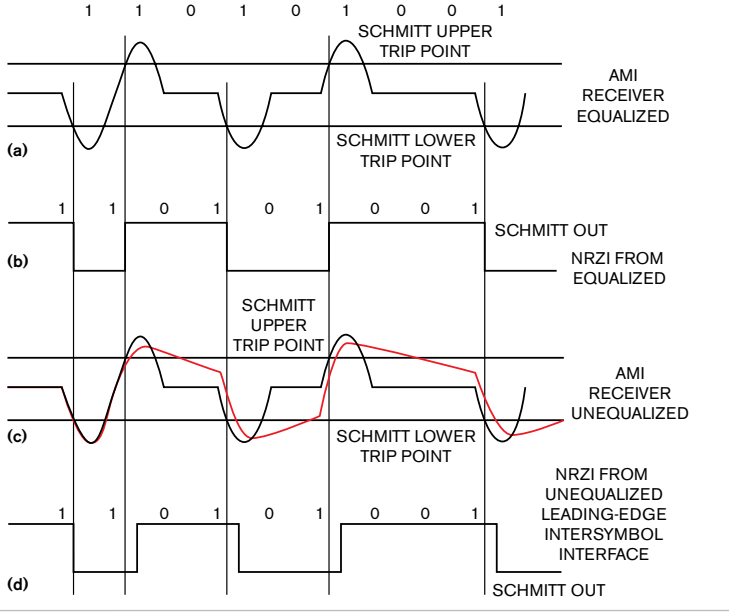

Figure 3 A Schmitt trigger directly converts bandlimited, equalized AMI (a) into the original NRZI (b). Once AMI crosses a trip point, no further transition at Schmitt output (c) is possible until the AMI crosses the opposite trip point. Unequalized AMI, superimposed on equalized AMI, cause marking pulse tails, resulting in little waveform distortion (d). Some data-dependent timing jitter occurs because of leading-edge intersymbol interference.

Virtual RF generator measures load impedance and power

Michael Nasab, Circuit Mentor, Boulder Creek, CA

Calculating the load impedance and power consumption at high frequencies in RF circuits is a tedious task. This Design Idea describes a VI (virtual instrument) that provides an easy way to quickly and effectively measure these parameters. You can measure and display the power and impedance of various types of loads, such as resistive or series/parallel tank circuits, at any given frequency. Using National Instruments (www.ni.com) LabView, you can easily modify the VI to accommodate any type of load having any complexity. The virtual RF generator comprises power-supply, amplifier, and load-select/measurement-display modules.

The amplifier module, with as much as 90% efficiency, provides frequencies of 100 kHz to 1 MHz with adjustable ac power applied to the load. The load-select-and-display module provides a sine or square waveform, load-selection type, and adjustment.

Figure 1 shows the VI driving a resistive load. Adjusting the frequency from minimum to maximum has no effect on the output impedance and power. You can download the VI and watch a flash movie describing three examples at www.circuitmentor.com. EDN

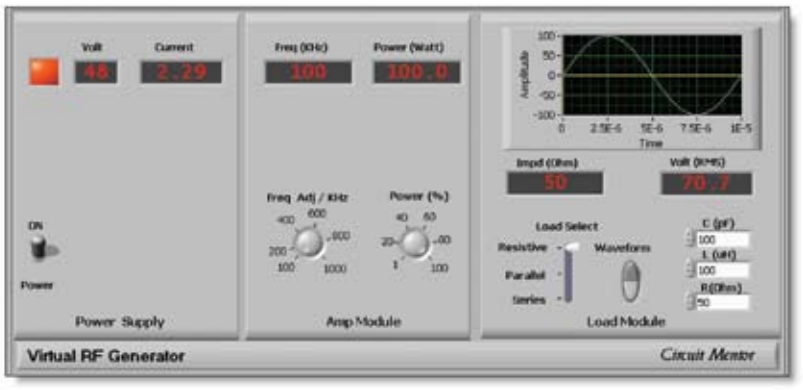

Figure 1 These settings on the virtual instrument measure the impedance and power of a resistive load.

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Precision voltage-controlled current sink tests power supplies

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

To discover potential power-supply problems, you must run dynamic and static tests. This simple current sink tests low- to medium-power supplies and voltage sources. In this application, the current sink can draw current of 0 to 1.5A for an input-voltage range of 0 to 5V with a supply voltage as high as 20V. The basis of the circuit is precision op-amp IC_1, an OPA277 from Texas Instruments (www.ti.com), which features a maximum input-offset voltage of only 100 µV, maximum input-bias current of 4 nA, and low drift over the temperature range of −40 to +85°C (**Figure 1**). The op-amp IC compares its positive input voltage with the voltage across sense resistor R_{SENSE}.

IC_1's output drives an enhancement-mode N-channel power-MOSFET, Q_1, an STMicroelectronics (www.st.com) IRF530, such that the voltage across the sense resistor equals the positive-input voltage. The voltage across the sense resistor is proportional to the load current from the power supply under test and is independent of its output voltage. Q_1 features a maximum current of 14A at a case temperature of 25°C with drain-to-source voltage of 100V, low gate charge, and maximum on-resistance of 0.16Ω at a gate-to-source voltage of 10V and a drain current of 7A.

The MOSFET can dissipate a finite amount of maximum power—to 30W with the heat sink's thermal resistance of 1°C/W or less and an ambient temperature of 40°C or less in still air. The maximum power depends on the thermal resistance of the heat sink you use and the ambient temperature, so, when you increase the supply voltage, you must accordingly reduce the load current. By pulsing the input voltage, you can increase the supply voltage to several 10s of volts because the average power dissipation is lower and depends on the average load.

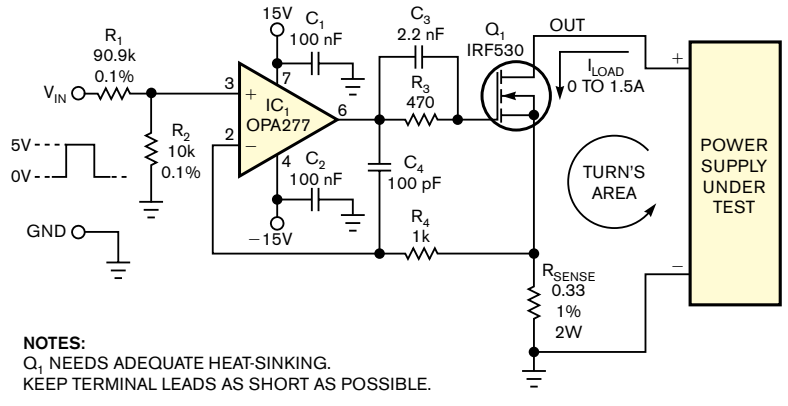

Figure 1 This simple current sink allows you to test both the static and the dynamic behavior of power supplies.

The precision resistive divider, R_1 and R_2, allows you to convert the input-voltage range of 0 to 5V into 0 to 0.495V at the positive input of IC_1, resulting in an output-current range of 0 to 1.5A. In addition, the values of resistors R_1 and R_2 provide 100 kΩ of input resistance, which is adequate for most voltage-function generators having a source impedance of 50 or 75Ω, allowing them to drive the circuit's input without using an input-op-amp buffer.

Analyzing the circuit yields the following relationships: $I_{LOAD}=GV_{IN}$, with $G=1/(\alpha R_{SENSE})=0.3A/V$, where G is the conductance, α is the attenuation factor, and $\alpha=1+R_1/R_2=10.09$. You can change the attenuation factor of the input-voltage divider to adjust

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the upper limit of the output current to several amperes, which allow you to test low-voltage power supplies with high output current.

Capacitors C_3 and C_4 and resistors R_3 and R_4 ensure loop stability, yielding a circuit with a rise time of 1.4 µsec for an input step voltage of 0 to 5V. So, you can test power supplies in either static conditions, applying a dc input voltage, or dynamic conditions, applying, for example, a pulsed input voltage to simulate fast load transients. Also, you can test power supplies or voltage sources as low as 1V because of the low channel resistance of Q_1 and the R_{SENSE} resistor; the lower limit is $1.5A(R_{SENSE}+R_{DS(ON)})=735$ mV, where $R_{DS(ON)}$ is the on-resistance.

You can also test multiple regulated outputs of power supplies such as a −5 or a −12V supply voltage. In this case, you must connect the ground of the power supply to the output of the current sink—that is, the drain terminal—and the negative output with the ground of the circuit. For accuracy, when you perform dynamic tests, such as load regulation, recovery time, and transient response, you must take care when connecting the power supply under test with the circuit to reduce the turn's area. The pulsed load current produces radiated emissions, which are proportional to this area, to the value of the current, and to the square of the current frequency, and they may disturb the circuit itself and the measuring equipment. EDN

Red LEDs function as light sensors

Geoff Nicholls, Glinde, Germany

Ordinary red LEDs normally function as light emitters, but they can also function as photosensors. A single LED can even function as both a light emitter and a light detector in the same circuit (**Reference 1**). The basic idea is to pulse the LED, using the on-time to light it and the off-time to sense the photovoltaic current from the ambient light that the LED sees.

Figure 1's circuit functions as a night-light. The LED stays off during daylight and turns on when the ambient-light level drops. The 7555 CMOS timer is a monostable one-shot, which triggers when Pin 2's voltage is less than one-third of the supply voltage. R_1 and R_2 form a voltage divider, which keeps the cathode of the LED just below the trigger voltage. When the ambient-light level is sufficient, the LED develops several hundred millivolts, which add to the R_1/R_2-junction voltage and keep Pin 2 above the one-third-trigger level. In this state, the Pin 3 output of the 7555 approaches 0V, and the 1N914 diode becomes reverse-biased, allowing the LED's photovoltaic current to flow into Pin 2's trigger input.

When the ambient-light level drops low enough, the LED voltage falls, and Pin 2 goes below the trigger level. The 7555 then generates a one-shot pulse, the 1N914 becomes forward-biased, and the LED lights up. At the end of the timing period, which R_3 and C_1 set, the monostable resets and discharges C_1. The monostable is then ready for another cycle. The LED then briefly turns off during this interval, which allows it to again sense the ambient light.

The circuit in **Figure 2** functions as a day-light; the LED flashes in bright light and stays off in low ambient light. The 7555 provides astable operation and slowly flashes the LED through the 1N914 diode as long as Pin 4's reset input is greater than approximately 600 mV. If the ambient light is too low, the LED cannot generate enough voltage at Pin 4, and the 7555 output remains near 0V, preventing the LED from turning on. The LED operates as a light emitter when Pin 3's output is high and as a sensor when Pin 3's out-

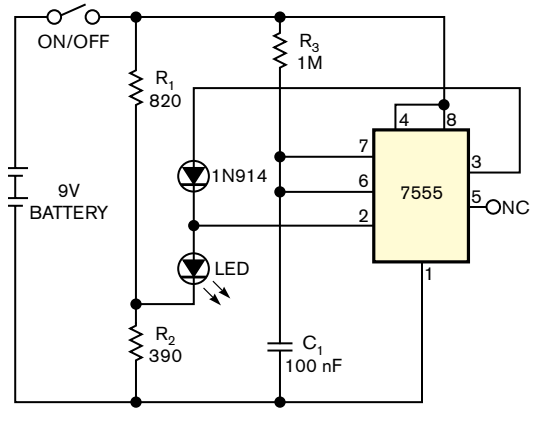

Figure 1 This circuit functions as a night-light. The LED stays off during daylight and turns on when the ambient light level drops.

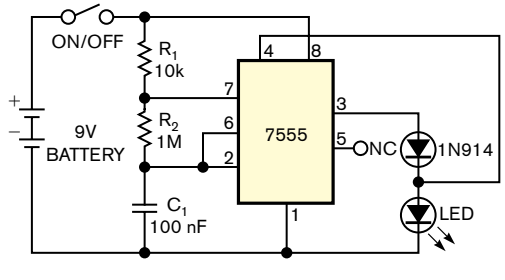

Figure 2 The LED in this circuit flashes slowly when the ambient-light level is high and turns off when the light level drops.

put is low.

These circuits require no current-limiting resistor. The timer IC must be a CMOS type because, to operate correctly, the circuit design requires low input currents. The prototypes use Intersil's (www.intersil.com) ICM7555 devices.EDN

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White-noise generator has no flicker-noise component

Alfredo Saab and Randall White,
Maxim Integrated Products, Sunnyvale, CA

White-noise generators generate a flat graph of output-power density versus frequency. These generators are useful for testing circuits that have an extended low-frequency or dc response. However, the presence of pink, or flicker, noise complicates the design of white-noise generators for frequency ranges that extend to a few hertz or below. A semiconductor device generates noise that always has the characteristic signature of pink noise: Its output-power-density amplitude increases as frequency decreases, with a corner frequency of 10s of hertz to a few kilohertz. A high-value resistor generates noise with its own flicker-noise component, whose value and characteristics vary with the resistor's technology. If, on the other hand, the resistor has a low value and the device uses low-noise technology, then the noise is almost completely white with power density that is constant with frequency. Unfortunately, a low-value resistor also yields a low value of noise-power-density amplitude, and any device you introduce to amplify that level adds pink noise of its own.

You can find amplifiers whose input-voltage noise includes no pink-noise component, but their input-current noise has a flicker-noise component, which appears at the amplifier output if the resistance that any amplifier input encounters has a significant value.

In the noise-generator circuit of **Figure 1**, IC_1, a MAX4238 amplifier from Maxim (www.maxim-ic.com) has no flicker-noise component in its input-voltage noise. It amplifies its own input-voltage noise with a feedback network comprising low-value resistors to avoid adding noticeable flicker-component noise from either the resistors or the amplifier's input-noise current.

A plot of the circuit's output voltage as a function of frequency is almost flat from 0.01 Hz to 3 kHz (**Figure 2**). The voltage-density amplitude is 4 to 5 $\mu V/\sqrt{Hz}$. The noise-density amplitude also depends on temperature, so you should keep the circuit at constant temperature while making measurements.EDN

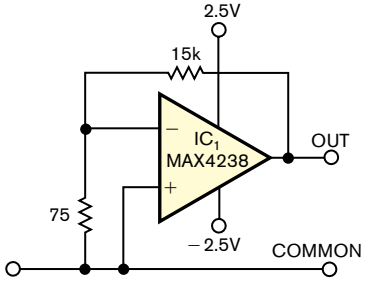

Figure 1 Built with an amplifier whose input voltage noise has no flicker-noise component, this white-noise generator produces an output with no flicker-noise component.

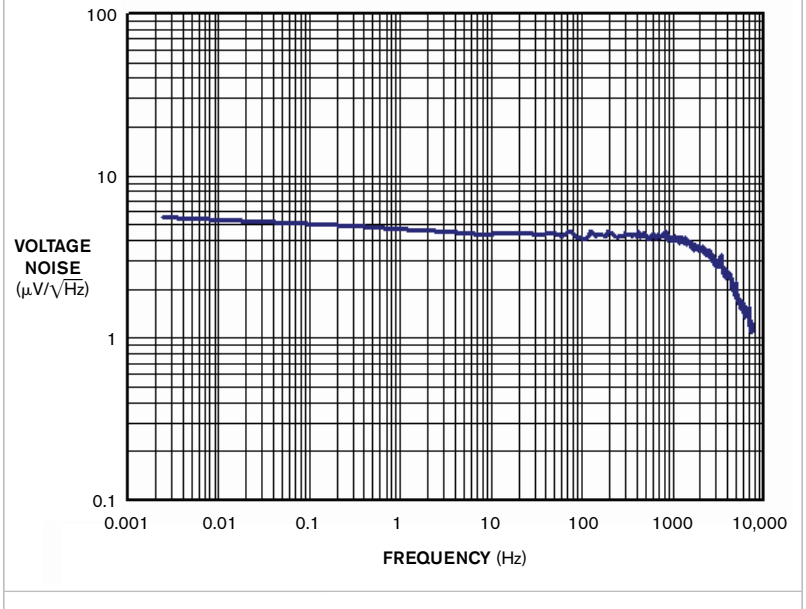

Figure 2 The circuit's output voltage as a function of frequency is almost flat from 0.01 Hz to 3 kHz.

Analog voltage controls digital potentiometer

Hrishikesh Shinde, Maxim Integrated Products, Dallas, TX

This Design Idea describes an analog voltage that controls a digital potentiometer through the device's I²C interface. An ADC in the Microchip (www.microchip.com) PIC12F683 microcontroller converts the analog voltage to the I²C stream that controls the Maxim (www.maxim-ic.com) DS1803 digital potentiometer (**Reference 1**). Of the microcontroller's six general-purpose I/O pins, two control the SDA (system-data) and SCL (system-clock-line) output signals, one controls an LED, and one accepts the analog input. SDA and SCL connect directly to the digital potentiometer's SDA and SCL pins with 4.7-kΩ pull-up resistors to V_{DD}. By adding or removing jumpers, you can separate the shared V_C and V_{DD} and isolate SDA and SCL.

The firmware is in assembly language, which was assembled using Version 7.40 of the MPLab IDE (integrated development environment), which is currently available free from Microchip at www.maxim-ic.com/tools/other/appnotes/4051/AN4051.zip. The program comprises fewer than 450 bytes in flash memory and 8 bytes in RAM. The program first initializes various configuration bits in the PIC, including the ADC and the internal oscillator. It configures the ADC to accept input from the analog input and sets the conversion clock to use the internal oscillator at 125 kHz.

The firmware runs in a loop, causing the 10-bit ADC to continuously convert the analog-input voltage. When a conversion is complete, the 8 MSBs form a data byte that transmists over the I²C bus, and this I²C-signal stream controls the digital potentiometer. The program controls both potentiometers in this dual device. With a change in firmware, however, you can independently control the potentiometers, using separate analog inputs on the PIC12F683. The program enables you to control the potentiometer by varying a voltage at the GP1 input of the PIC12F683. A change at GP1 causes a corresponding change in the potentiometer's resistance: $R_{OUT}=((\text{Input Voltage})/V_{CC})\times 50\ k\Omega$, where the end-to-end resistance of the digital potentiometer is 50 kΩ, the allowable V_{CC} range is 2.7 to 5V, and the input-voltage range is 0 to V_{CC}. You can troubleshoot an application by checking that the device's address is correct and that the I²C bus is connected. The LED blinks constantly while the ADC is running, but remains on when an I²C error occurs. After you correct the error, the LED resumes its normal function.

You can extend this design approach to other applications for which an analog voltage must control a device with an I²C interface. You can, for example, implement a nonlinear-transfer function, such as gamma correction, using the DS3906 variable resistor, and implement the transfer function in embedded look-up tables (**Reference 2**). Or, by connecting a thermistor at the input, you can vary the output of an I²C-controlled current DAC in response to changes in the ambient temperature. EDN

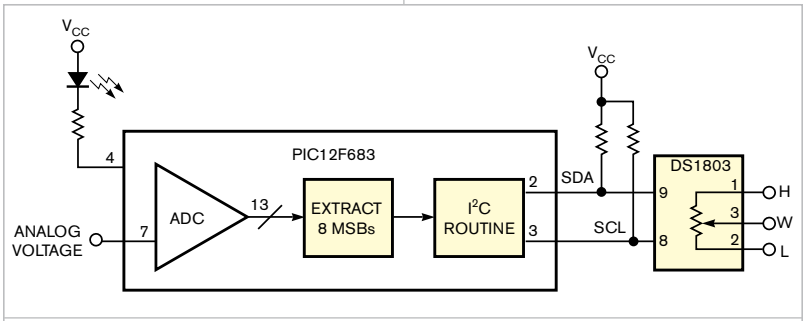

Figure 1 This circuit allows an analog-voltage input to select the digital potentiometer's resistance.

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Harvest energy using a piezoelectric buzzer

Carlos Cossio, Santander, Spain

Energy-harvesting, or "scavenging," systems extract energy from the ambient environment. Unfortunately, these power generators supply much less energy than do standard batteries. However, thanks to the decreasing size and low-power requirements of today's wearable devices, it is feasible to replace batteries in some low-power systems with power generators that capture energy from the user's environment, such as the vibration energy a user produces during walking or running. This Design Idea uses the piezoelectric effect of a standard and easy-to-find piezoelectric buzzer to turn mechanical vibrations into electrical energy. Although piezoelectric buzzers generate sound waves when you apply an ac voltage,

you can use them in the opposite way: You obtain the maximum ac peak voltage that the piezoelectric buzzer generates when the vibration frequency matches the resonant frequency of the piezoelectric buzzer.

The power generator in **Figure 1** is a simple circuit. The piezoelectric buzzer produces an ac voltage when it is under vibration; therefore, you must convert this voltage to a dc voltage before charging the capacitor. The four Schottky diodes form a bridge rectifier to perform this task. For a reliable and efficient operation, select Schottky diodes, such as the 1N5820 rectifier diode from On Semiconductor (www.onsemi.com), that exhibit low forward-voltage drop and low reverse leakage.

Energy harvesters typically capture small amounts of energy over long periods, so harvesters usually contain an energy-storage subsystem in the form of a supercapacitor, such as the PowerStor 0.47F, 2.5V capacitor from Cooper Busmann (www.bussmann.com). The larger the capacitor, the longer it takes to charge it. On the other hand, a larger capacitor provides power for a longer time for the same load. Because a supercapacitor often has a much lower voltage than standard electrolytic capacitors, you must connect a zener diode, such as the BZX85-C2V7, to prevent the voltage across the supercapacitor from increasing beyond its maximum voltage rating. As soon as you apply a load, the supercapacitor starts discharging, and the voltage across the supercapacitor starts dropping. To guarantee a fixed voltage at the output, you must use a dc/dc-voltage-converter IC, such as the MAX1675 from Maxim (www.maxim-ic.com) as a step-up converter working at 3.3V.

As an additional benefit, if the supercapacitor's voltage drops below the required voltage of operation, the circuit continues to provide regulated output voltage as long as the supercapacitor voltage does not drop below the lower limit of the dc/dc converter. This limit is 0.7V for the MAX1675. EDN

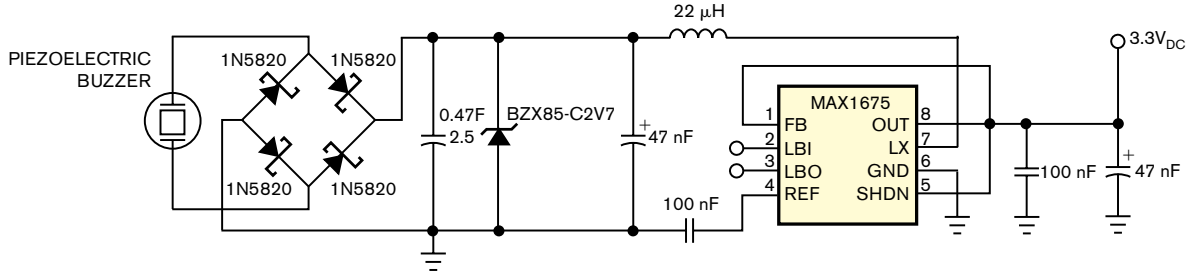

Figure 1 A simple vibrational-energy-harvesting circuit using an off-the-shelf piezoelectric buzzer as the power generator turns mechanical energy into electrical energy.

Retriggerable monostable multivibrator quickly discharges power-supply capacitor

Jordan Dimitrov, Tradeport Electronics, Vaughan, ON, Canada

Universal power supplies must work from mains power lines ranging from 90 to 264V ac at 50 or 60 Hz. Directly rectifying the input voltage charges the filter capacitor to 120 to 370V dc. Such voltages present a serious threat to personnel who are prototyping or repairing the power supply. It is desirable to discharge the filter capacitor when mains power is off so workers can safely deal with the power supply. An intuitive solution is to use an ac relay. However, relays cannot operate in a wide range of input voltages, they consume significant power and space, and they have a limited number of cycles. **Figure 1** shows an alternative circuit, which you can apply to a filter capacitor of almost any value. It uses a MOSFET, Q_1, and a current-limiting resistor, R_D, to discharge the high-voltage filter capacitor, C_P, within one second after you switch off the mains power. The trick is to use a retriggerable monostable multivibrator to control the MOSFET.

THE TRICK IS TO USE A RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TO CONTROL THE MOSFET.

While the mains power is on, optocoupler IC_1 and the associated passive components continue to generate symmetrical square pulses that they apply to the A input of multivibrator IC_2. Each pulse triggers the circuit, forcing the $\overline{Q}$ output to the low level. The multivibrator generates a 100-msec negative pulse; then, $\overline{Q}$ should turn high. However, because triggering pulses arrive before the multivibrator's pulse is complete, the $\overline{Q}$ output never turns high, the MOSFET is always off, and the rectifier works as usual. When you turn off mains power, the $\overline{Q}$ output stays low for 100 msec after the last triggering pulse;

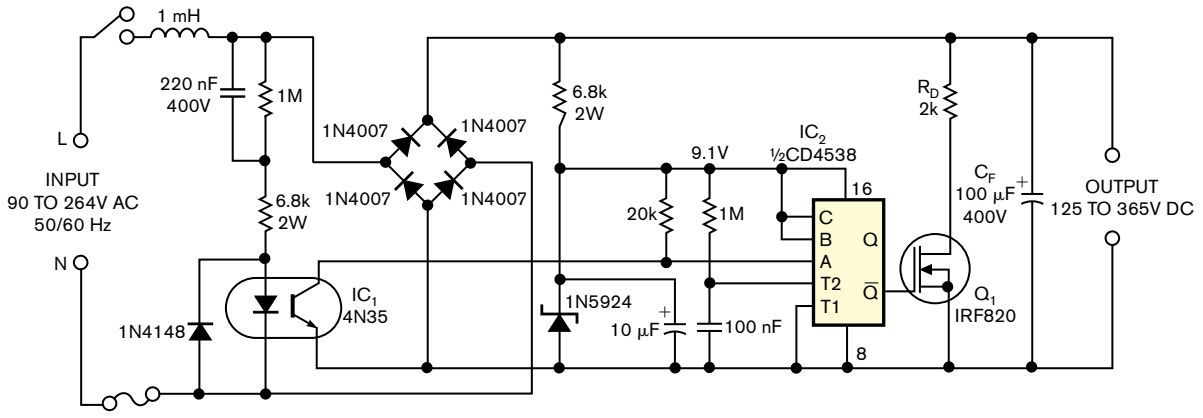

Figure 1 Because of the retriggerable feature of the CD4538 IC, the discharge network, Q_1 and R_D, remains off when mains power is present; otherwise, it turns on and quickly discharges high-voltage filter capacitor, C_F.

it then turns high. The MOSFET turns on and quickly discharges the output capacitor to a safe level.

The circuit underwent testing at both limits of the input voltage: 90 and 264V ac. The filter capacitor is of moderate value, 100 µF, and so is the peak-discharge current of 0.06 to 0.18A. The MOSFET's peak current is 8A; hence, the circuit can readily work with much larger-value capacitors. If this current is still not enough, you must use a MOSFET with a higher peak current rate. You need to change only R_D to fit the desired discharge time, t_D. The $t_D=3\times R_D\times C_F$ relationship is a good guideline. It ensures that the output voltage drops to 95% of its initial value, which is well below the user-touchable safety limit for any value of the output voltage. EDN

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Chop the noise gain to measure an op amp's real-time offset voltage

Glen Brisebois, Linear Technology, San Jose, CA

One of the most important specifications of an op amp is its input-offset voltage. You can null out this voltage on many op amps, but the problem with determining the input-offset voltage is that the offset voltage varies with temperature, flicker noise, and long-term drift. Chopping and autozeroing techniques have been around for several years, reducing achievable input offset to microvolts or less. The accuracy is so good that other minuscule effects, such as copper-solder thermocouple junctions, dominate the errors, until, with some effort, you can overcome them, as well. This Design Idea introduces a new type of chopping. "Chopping the noise gain" is a simple way to measure the offset voltage in real time, so that you can subtract it and enhance dc precision.

Figure 1 shows an LTC6240HV op amp in an inverting gain-of-10 configuration, along with several of its pertinent specifications. All of the input offset arrives at the output with a gain of 11 (called the "noise gain") as an output error. Any downstream circuitry or observer looking at the output voltage cannot distinguish the output error from the desired output signal.

Figure 2 shows the chop-the-noise-gain method. S_1 switches the additional shunt resistor, R_3, in and out, changing the noise gain without affecting the signal gain or bandwidth. There would normally be some degradation of bandwidth, but C_1 dominates the bandwidth limitation whether the switch is open or closed. Now, you impose a small square wave on the output with an amplitude that is equal to the present dc errors. You can demodulate out the error as with a conventional chopper, or you can subtract it in software in a modern ADC-based system.

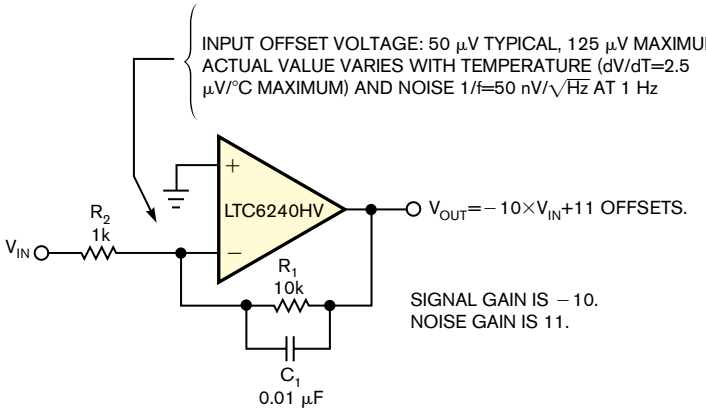

Figure 1 An op amp has a conventional gain of −10. The noise gain is 11, so all of the input errors appear at the output with a gain of 11. You cannot distinguish the signal from noise just by looking at the output.

The circuit in **Figure 2** is much like a simple summing amplifier, with one input both connected and disconnected. It is, in that sense, much like a true chopper amplifier. But, in this case, the input voltage being chopped is the amplifier offset, rather than the input signal. Why disconnect your input signal if you don't have to? Also, there is no need for continuous chopping; you need apply it only when you require an offset measurement.

Note that, although this Design Idea shows the inverting case for ease of understanding, the noninverting case is also practicable with a good analog switch for S_1. Also, as with any sampled system, frequencies at or greater than the clock rate alias into baseband, and you should therefore filter them out before the chopping. Finally, this method does not correct for bias- or leakage-current-induced errors.

Switch S_1 opens and closes, increasing the noise gain and imposing the input errors onto the output with alternating noise gains of 11 and 22. The

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resultant square wave now represents an easily measurable "11 errors," which you can then subtract from the output. This technique is similar to that of conventional chopper amplifiers, except that, in this case, you are chopping the error rather than the signal.

Figure 3 shows the oscillogram of the output of the circuit of **Figure 2**, with an input voltage of 0V (grounded). The top trace is "S," the control signal applied to S_1 at 750 Hz. The bottom trace is the output error alternating between 1 and 2 mV, indicating 90 µV of op-amp offset. The output "sees" the effect of doubling the noise gain of the output offset. The difference between the two noise gains is 11, and this difference dictates the amplitude of the square wave that S_1 causes, independently of the input voltage.

Figure 4 is similar to **Figure 3**, but zoomed out and with a 2-mV-p-p slow-moving sine wave signal at the input voltage—that is, 20-mV-p-p output. The 1-mV square wave of **Figure 3** is superimposed upon the slow-moving output signal and still contains the real-time dc-error information. Just by looking at the output, you can discern that the true value of the signal is 1 mV below the measured value. EDN

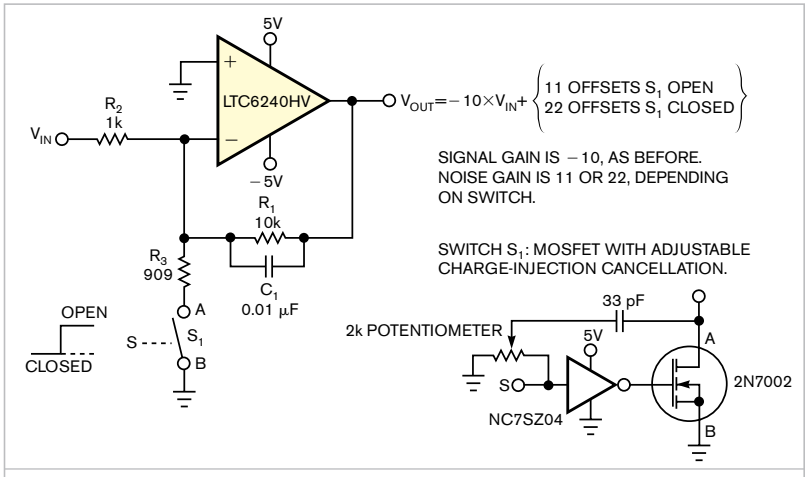
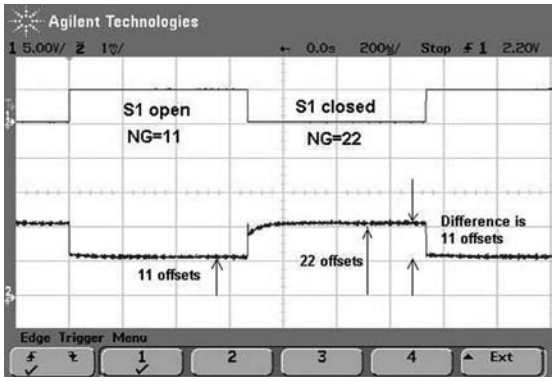


Figure 2 S_1 switches the additional shunt resistor, R_3, in and out, changing the noise gain without affecting the signal gain or bandwidth.



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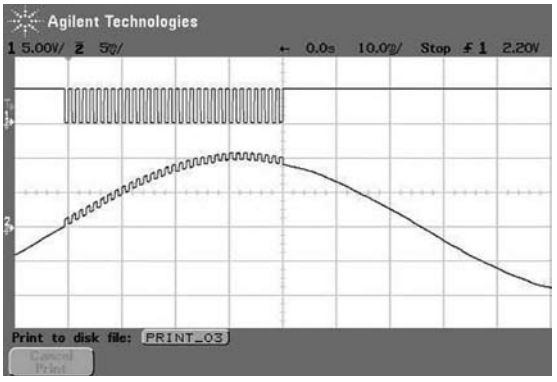

Figure 4 The oscillogram is similar to that in Figure 3, but with a 2-mV-p-p slow-moving sine wave signal applied at the input voltage.

Simple analog circuit provides voltage clipping and dc shifting for flash ADC

Alfredo del Rio, University of Vigo, Spain

Many flash ADCs, such as National Semiconductor's (www.national.com) ADC1175, have a recommended operating input-voltage range of 0.6 to 2.6V (**Reference 1**). However, in some applications, you must convert a symmetrical analog-input signal. The circuit in this Design Idea converts a symmetrical input-voltage range of −0.2 to +0.2V into the recommended 0.6 to 2.6V range (**Figure 1**).The circuit also prevents the output voltage from going below –0.3V, which would probably damage the ADC.

The circuit uses an Analog Devices (www.analog.com) AD8002 dual-current-feedback operational amplifier to obtain a high bandwidth (**Reference 2**). The first block, noninverting am-

plifier IC_{1A} has a voltage gain of five. This block also provides high input impedance and low output impedance, so that the second block, IC_{1B}, operates properly. The second block does most of the work. Starting from a basic inverting amplifier comprising IC_{1B}, R_4, and R_5, you obtain the clipping effect by adding R_3 and D_1. R_3, D_1, R_4, and R_5 determine the clipping level. In addition, adding the I_{DC} current dc-shifts the output voltage. You can trim adjustable potentiometer resistor P_1 to obtain the desired output voltage shift—that is, 1.6V.

If diode D_1's current is negligible, the output voltage, V_O, is $-(1+R_2/R_1)\times(R_5/(R_3+R_4))\times V_I+V_{CC}\times R_5/(R_6+P_1+R_7)=1.6-5\times V_I$. Given that the diode voltage, V_{DIODE}, is $0.6V_S$, $V_O=-(R_5/R_4)\times V_{DIODE}+V_{CC}\times R_5/(R_6+P_1+R_7)=1.6-1.65=-0.05V$.

The clipping takes place near 0V, protecting the ADC. Raising the clipping level makes the circuit less linear in the nonclipping range. In other words, a design trade-off exists between clipping level and linearity. Resistor R_8 limits the current through the ADC's input pin. Capacitor C_2 is optional; it limits the V_{ADC}/V_I bandwidth. Capacitor C_1 helps to reduce the voltage noise that might come from the $-V_{CC}$ power supply. EDN

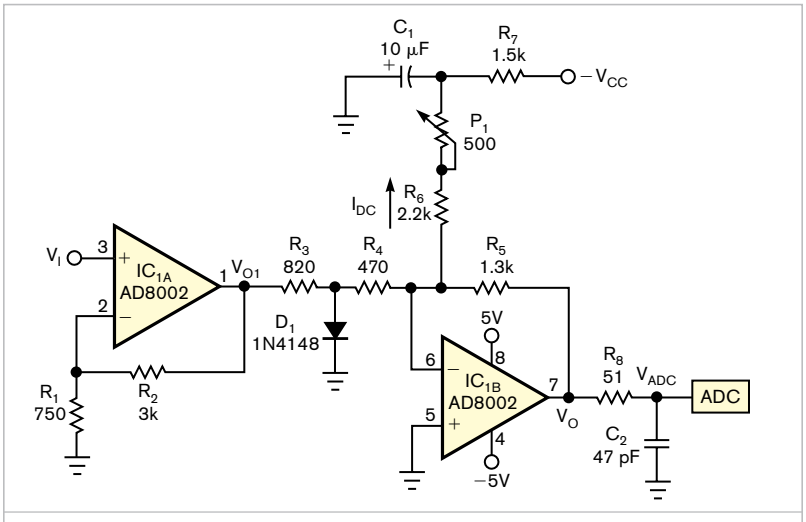

Figure 1 Adding R_3 and D_1 to a conventional op-amp circuit provides clipping. R_3, D_1, R_4, and R_5 determine the clipping level. In addition, adding the IDC current causes dc-shifting of the output voltage.

REFERENCES

1 "ADC1175 - 8-Bit, 20MHz, 60mW A/D Converter," National Semiconductor, www.national.com/mpf/DC/ADC1175.html

2 "AD8002 Dual 600 MHz, 50 mW Current Feedback Amplifier," Analog Devices, www.analog.com/en/prod/0%2C2877%2CAD8002%2C00.html.

Compact laser-diode driver provides protection for precision-instrument use

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University of Shanghai for Science & Technology, Shanghai, China

Continuous-wave laser diodes in precision-instrument applications require constant-current sources to drive them. Proper design of such a driver must involve careful tackling of robustness, stability, noise, and other issues and is consequently costly and complicated (**Reference 1**). **Figure 1** shows a compact, cathode-grounded laser-diode driver with protection against ESD (electrostatic-discharge) damage, start-up spikes, overshoot, and possible fluctuation arising from external optical feedback. An op amp, IC_4, with an enable input drives PMOS FET Q_1 and controls the output current. R_S sets the current to the rated value for a 35-mW HL6738MG laser diode from Opnext (www.opnext.com). To prevent output from Q_1 during start-up, comparator IC_{5A} keeps IC_4 off, and a 10-kΩ pullup resistor keeps Q_1 off by linking Q_1's gate to the supply of IC_4 until the terminal supply, V_B, reaches the designed value, approximately 6.5V, and opens Q_1 via IC_4.

The key point for protection against ESD damage and overshoot lies in the use of Q_2, a depletion-mode NMOS FET. With power off, Q_2 conducts, shunting any harmful ESD to ground. With power on, comparator IC_{5B} outputs a negative voltage far below the gate-to-source off-state voltage. Hence, Q_2 is off and has little effect upon the drive current unless the operating voltage at the laser's anode exceeds the maximum rating of 2.8V in the **figure**. In this case, the operating voltage triggers IC_{5B} to output high and thus turns on Q_2, shunting the drive current to ground, as well. The circuit now introduces significant hysteresis to latch off the state of emergency. Considering the low on-resistance of Q_2, this circuit provides better protection than the common method of relying on a paralleled zener diode for overshoot suppression (**Reference 2**).

Despite employing a split supply, this design requires no particular supply sequencing. You must cut off Q_2 only at the beginning of start-up, so it would be better to turn on the −9V external supply before enabling the driver. Despite the availability of substitutes for some ICs in this design, selection

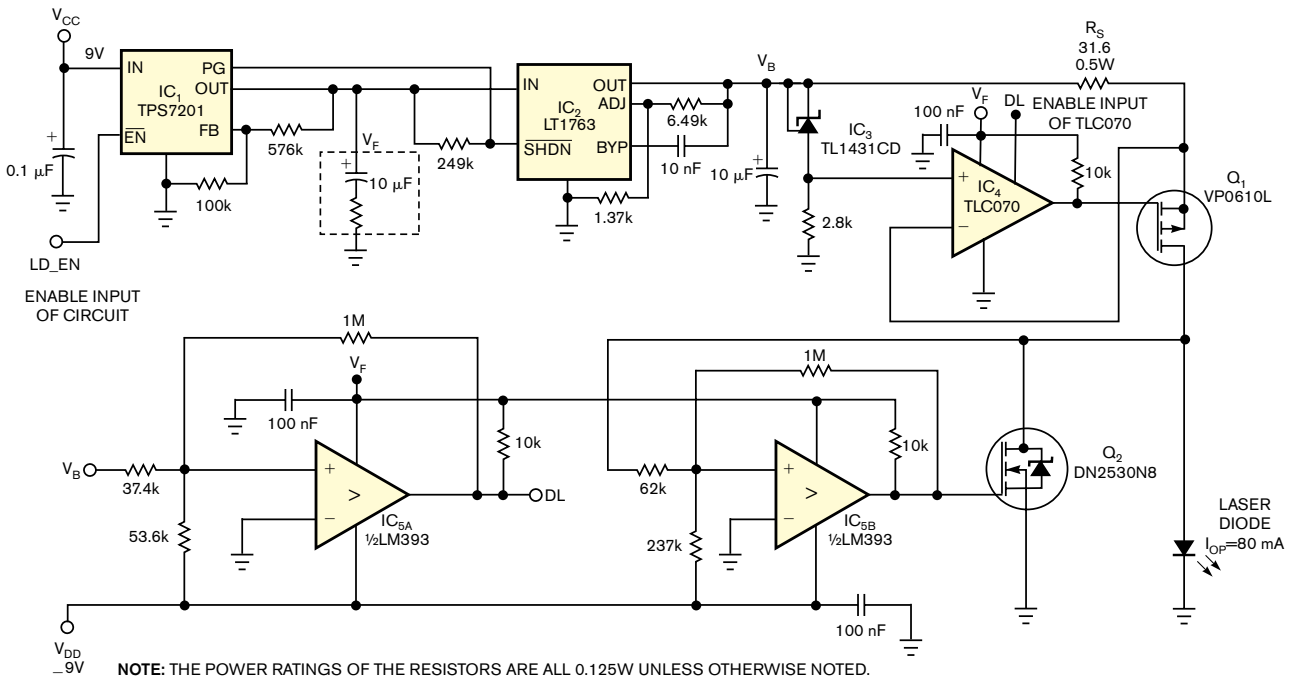

Figure 1 This laser-diode-drive circuit provides a constant current and protection against input overvoltages and start-up transients.

of the proper devices may be troublesome. For example, you can with slight modifications replace the Texas Instruments (www.ti.com) TLC070 with a Linear Technology (www.linear.com) LT1637; the two devices are not pin-compatible. However, the TLC070's superior ac performance, especially higher CMRR (common-mode-rejection ratio) over a wider bandwidth permits more effective protection against fluctuations in the operating voltage because of external optical feedback under some desired or undesired circumstances (**Reference 3**).EDN

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1 Williams Jim, "Current sources for fiber-optic lasers: a compendium of pleasant current events," *EDN*, Aug 22, 2002, pg. 69, www.edn.com/article/CA238417.

2 "DN2530: N-Channel Depletion-Mode Vertical DMOS FETs," Supertex, 2001, www.supertex.com/pdf/datasheets/DN2530.pdf.

3 "TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA: family of wide-bandwidth high-output-drive single supply operational amplifiers," Texas Instruments, September 2006, http://focus.ti.com/lit/ds/symlink/tlc074.pdf.

Current source makes novel Class A buffer

Horst Koelzow, Winnipeg, MB, Canada

The basis for this Design Idea is a classic two-transistor current source (**Figure 1**). Current through R_1 depends only on the V_{BE} (base-emitter voltage) of Q_2 and on the value of R_1 itself. The V_{BE} of Q_1 has no impact on the output current. Typically, this circuit finds use as a steady current source or as a limiter. The circuit forms the amplifier for the upper, positive half of the signal. Adding a complementary stage for the lower, negative half of the signal completes the buffer (**Figure 2**). The emitters of Q_2 and Q_3 become the input for the circuit, and the junction of sensing resistors R_1 and R_2 is the output. R_3 is an input-termination resistor that sets the output quiescent voltage. You can replace the bias sources (current

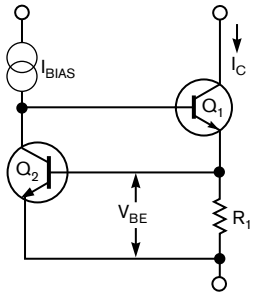

Figure 1 This classic two-transistor current source commonly finds use as a steady source of current or as a limiter.

sources in the **figures**) with resistors.

At the quiescent, 0V-input-voltage operating point, both halves of the circuit run at maximum current, and both the input and the output are at the same potential. When you impress a voltage on the input, you inject current into the Q_2-Q_3 emitter node. From there, current can go up into base of Q_1 or down into base of Q_4. The output voltage relative to the input voltage determines the direction of the injected current. If the input voltage is positive, it has no effect on the upper half because it is already limiting. It can, however, reduce drive current in the lower half, resulting in a reduction of lower output-drive current. Reduction of lower side output current results in a rise in output voltage. In short, an injected signal current "unlimits" the stage of opposite polarity.

At first glance, the circuit appears to have unity gain. But, because Q_2 and Q_3 sense the tops of R_2 and R_3 and not circuit output, R_1 and R_2 are effectively in series with the output load. If the load's impedance, R_{LOAD}, is small, the circuit gets significantly loaded down. However, as long as the input stage does not clip, the circuit does not become distorted. The source driving the buffer stage sets $h_{FE}(Q_1)\times(R_1+R_{LOAD})\Omega$, where h_{FE} is forward-current gain.

AN INJECTED SIGNAL CURRENT "UNLIMITS" THE STAGE OF OPPOSITE POLARITY.

Q_2 and Q_3 are common-base stages. Their purpose is to translate input voltage to the bias voltage that Q_1 and Q_4 require. This voltage-translation action allows direct substitution of other devices, such as MOSFETs or Darlington transistors. EDN

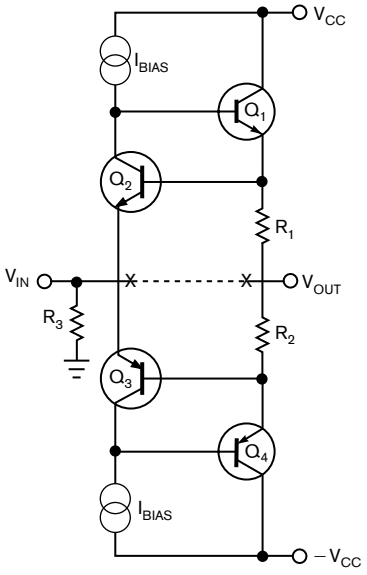

Figure 2 Adding another stage to the current source allows the circuit to function as a buffer.

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READERS SOLVE DESIGN PROBLEMS

Use thermoelectric coolers with real-world heat sinks

W Stephen Woodward, Chapel Hill, NC

Peltier devices, also known as solid-state refrigerators, or TECs (thermoelectric coolers), actively cool temperature-sensitive electronic components, such as optical detectors and solid-state lasers. A glance at any TEC data sheet reveals that some primary and fairly easily understood parameters characterize a TEC: The maximum current is the TEC's current drive for maximum cooling, the maximum differential temperature is the no-load cooling temperature at maximum current and with no heat load. The maximum voltage is the TEC's voltage drop at the maximum-current drive, and the maximum heat transfer (Q_{MAX}) is the maximum cooling-heat load at a maximum current and differential temperature of zero.

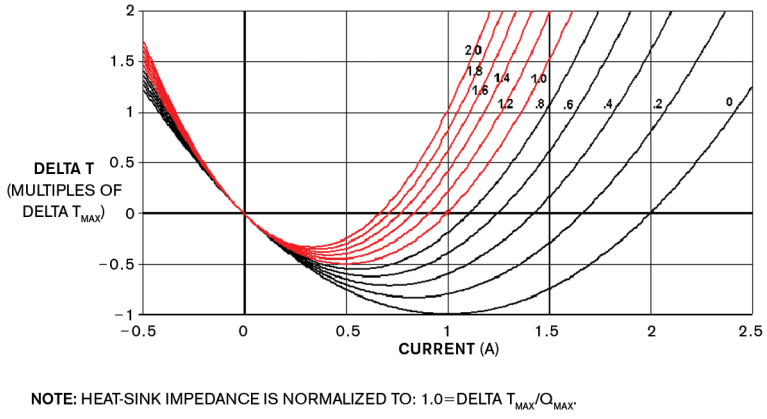

Figure 1 This family of curves shows that a thermoelectric cooler may actually heat rather than cool at the maximum drive current if the heat sink the cooler is mounted on is less than perfect.

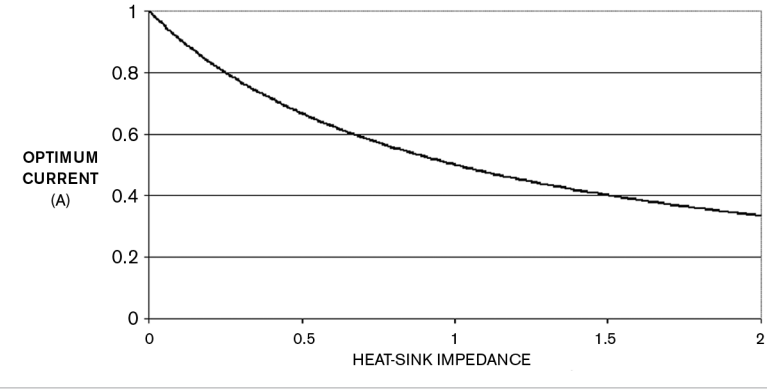

Figure 2 A derating factor for maximum voltage and current is based on the real-world thermal impedance of the TEC's heat sink.

However, one TEC data sheet proviso that designers sometimes miss is that you always measure these parameters with the TEC mounted on an effectively zero-thermal-impedance—that is, perfect—heat sink. This point is an important one and deserving of the designer's rapt attention because heat sinks always have at least some thermal impedance, and all the primary TEC parameters change—sometimes dramatically—when the TEC must make do with an imperfect sink.

The family of impedance-versus-current curves in **Figure 1** illustrates this effect. Each curve corresponds to a different heat-sink thermal impedance, normalized to one for 11 values from zero to two.

Although the maximum current is, by definition, the optimal current for

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maximum cooling at a heat-sink impedance of zero, the situation changes radically with increasing impedance until there's no net cooling whatsoever. Further, for impedance greater than one, instead of cooling, the maximum TEC drive actually heats rather than cools. **Figure 2** shows the simple solution for this problem: You must replace the data sheet's maximum current and voltage values with new, lower maximum-drive values corresponding to the optimal numbers you need to achieve maximum cooling whenever impedance is greater than zero. EDN

Interface MIDI instruments to a PC through a USB port

Stefano Palazzolo, Senago, Milan, Italy

This Design Idea uses the FT-232BM from Future Technology Devices International (www.ftdichip.com), a USB-to-UART interface IC that you need not program, to interface a USB port to the MIDI (musical-instrument-digital-interface) bus (**Figure 1**). The USB signals directly interface to IC_1, an FT232BM. The serial-transmitter and -receiver signals pass through IC_2 and IC_3 to transform the RS-232 signals to the MIDI's loop current. You can use an EEPROM, IC_4, if you want to add a serial-number interface or use more than one interface.

This hardware doesn't require you to write any software. However, you must install two drivers. First, you need the free VCP driver from FTDI at www.ftdichip.com/Drivers/VCP.htm. It allows you to use this interface as a common serial-port interface. Before you install it, you must change a string in the file FTDIPORT.INF (**Reference 1**) to set up the 31,250-baud rate for FT232BM. Then, you can configure VCP to run at 38,400 baud. (The real baud rate will be 31,250 as preset in FTDIPORT.INI.)

Then, you must install another driver that permits you to see your VCP serial port as a MIDI port for addressing all MIDI messages. You can find a lot of similar drivers on the Internet. For example, the Roland serial MIDI driver is available at: http://www.roland.it/dow_drivers/for_win/serial32_wxp2k.exe. You can enable this driver on the COM1 or the COM3 port.

Listing 1, at www.edn.com/080417di1, shows the changes to add to the FTDIPORT.INF file that change the baud rate from 38,400 to 31,250 baud. Change this file before installation. EDN

REFERENCE

1 "FT232BM Designers Guide, Version 2," FTDI, 2002/2003, www.ftdichip.com/Documents/AppNotes/DF232_20.pdf.

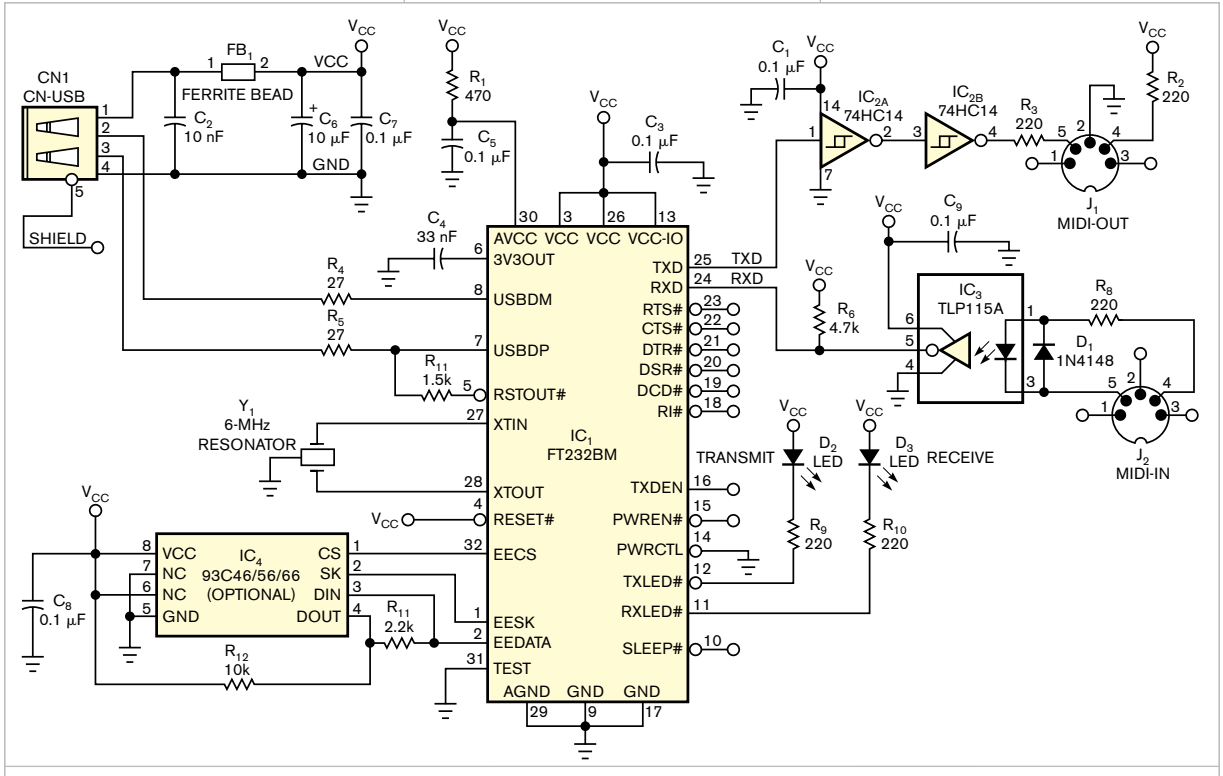

Figure 1 This USB-to-MIDI interface uses the FT232BM, a USB-to-UART interface chip that you need not program.

Transmission lines simulate digital filters in PSpice

David Báez-López, Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada

Designers use PSpice mainly to simulate analog circuits. However, you can also simulate digital filters with it. The main components in a digital filter are delay elements, adders, and multipliers. Although you can implement adders and multipliers using operational amplifiers, you can simulate a delay element with a transmission line. The transmission line in PSpice is a long-forgotten element that can realize a delay of seconds.

For example, **Figure 1** shows a second-order recursive digital filter. The transfer function for this filter is:

$$H(z)=\frac{B_0z^2+B_1z+B_2}{z^2+A_1z+A_2},$$

where H(z) is the digital-filter-transfer function, z is the z-transform variable, the As are the coeffieients of the denominator polynomial of the transfer function, and the Bs are the coefficients of the numerator polynomial of the transfer function. You can obtain the coefficient values with software available for filter design (**Reference 1**). The sampling frequency, f_S, relates to the transmission-line delay as $t=1/f_S$. For example, a bandpass digital filter with a 3-dB passband from 900 Hz to 1 kHz, a sampling frequency of 6 kHz, and a Butterworth characteristic yields the following transfer function:

$$H(z)=\frac{z^2-1}{z^2-0.9096707z+0.809374}.$$

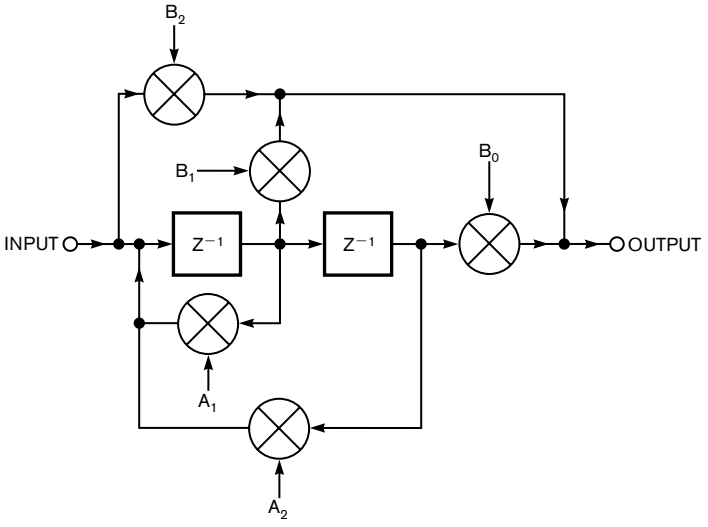

Figure 1 The transfer function for a second-order recursive digital filter has coefficient values that yield a lowpass, highpass, band-reject, or bandpass-transfer function.

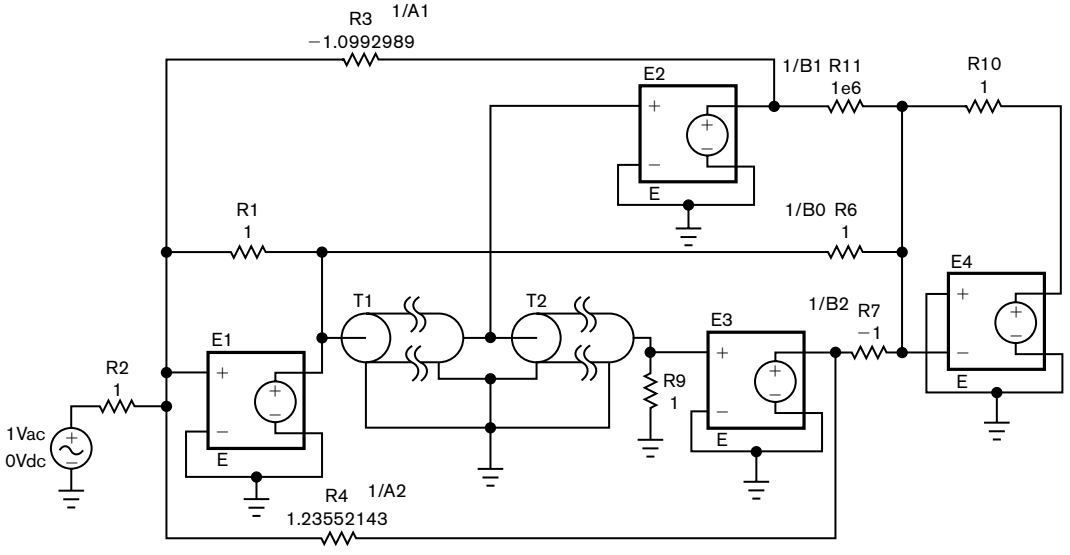

Figure 2 In the PSpice circuit, the VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers.

In this case, the transmission-line delay is 1/6000=166.67 µsec. If you additionally specify an impedance, Z, of 1Ω for the transmission line, then the parameters for the transmission line are Z_0=1Ω, and t=166.67 µsec. **Figure 2** shows the PSpice circuit. The VCVSs (voltage-controlled voltage sources), E1 and E2, simulate voltage followers, and VCVSs E3 and E4 and the resistors that connect to them simulate summers. **Figure 3** shows the results of the simulation. EDN

REFERENCE

1 López, David Báez, "Windows Based Filter Design with Winfilters," *IEEE Circuits and Devices*, Volume 13, 1997, pg 3.

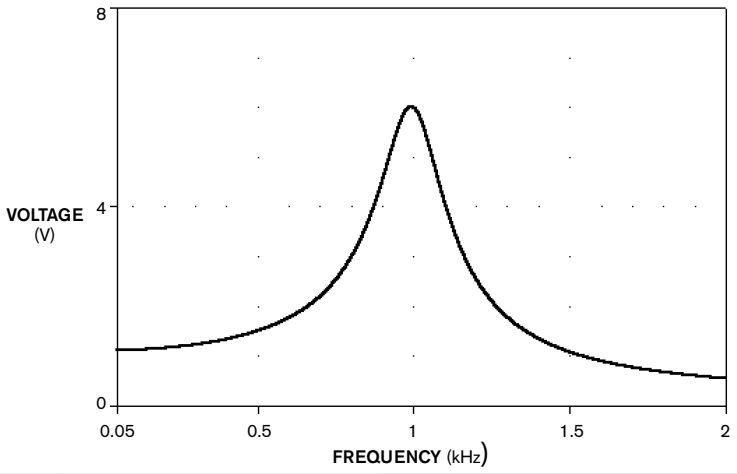

Figure 3 In this PSpice simulation, the digital bandpass filter uses transmission lines as delay lines.

Dual flip-flop forms simple delayed-pulse generator

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

Some applications require clock-timing adjustments, such as generating precision clocks for time-interleaved ADCs, or delay adjustments in a variety of precision-timing and pulse-delay applications. This Design Idea describes a delayed-pulse generator using a dual-CMOS D-type flip-flop (**Figure 1**). The circuit provides precision time delays of a trigger-input pulse. A dc-control voltage selects a time delay within the full-scale range. When the rising edge of a pulse triggers the input, the circuit's output generates a pulse with its rising edge delayed by an amount equal to the selected time delay, T_D, plus a fixed inherent propagation delay T_{PD}. Also, a time constant, R_4C_2, determines the output pulse's width.

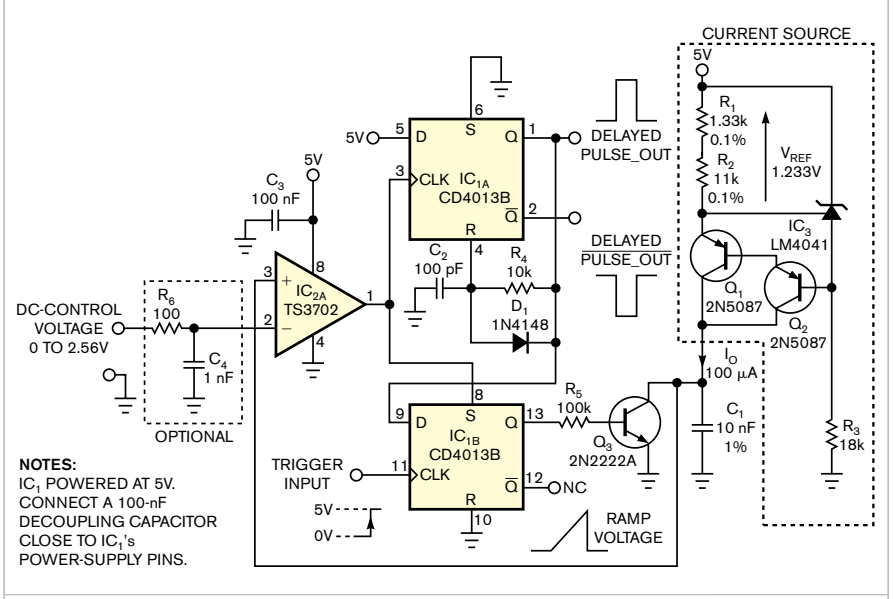

Figure 1 The rising edge of a trigger input starts a precision ramp voltage that compares with a control voltage, generating a precise delay.

A precision dc source, I_O, and capacitor C_1 set the full-scale delay range. When Q_3 is off, the current source charges capacitor C_1, generating a linear-ramp voltage with slope equal to I_O/C_1. The delay is the time it takes for the ramp to rise from its initial voltage to the control-voltage value.

In this application, the ramp slope is 10 mV/1 µsec, so that the full-scale delay range is 256 µsec for a control voltage of 0 to 2.56V. You can set the full-scale delay by changing I_O through either R_1+R_2 or capacitor C_1. For best accuracy, the current source can range from 10 µA to 1 mA, the capacitor's value can range from 1 nF to 1 µF, and the corresponding full-scale delay can range from 2.56 µsec to 256 msec. Use a precision film capacitor for C_1.

The basis of the current source is a shunt precision-micropower-voltage-reference, IC_3, producing a reference voltage of 1.233V with an initial ac-

curacy of 0.2%. A Texas Instruments (www.ti.com) LM4041, through precision resistors R_1 and R_2, biases the Darlington-coupled transistors Q_1 and Q_2 with a reference current $I_Q=V_{REF}/(R_1+R_2)=100\ \mu A$. The Darlington configuration ensures that base current is negligible and that the output collector current can achieve a worst-case accuracy of 0.3%. You can use any small-signal transistor, but, for best accuracy, use high-gain, low-level, low-noise BJTs, (bipolar-junction transistors) such as a 2N5087 or a BC557C.

IC_{1A} is a one-shot circuit (**Reference 1**). The output pulse's width, T_W, is $R_4C_2\times\ln(V_{DD}/V_{TH})$, where V_{TH} is the threshold voltage of the digital CMOS. Because $V_{TH}\approx V_{DD}/2$, then $T_W\approx R_4C_2\times 0.69$. Diode D_1 reduces recovery time. After power-up, Q_3 is in saturation, absorbing the current source's output, and, as soon as an input pulse triggers the circuit, IC_{1B}'s Q output goes low, switching off Q_3, starting a ramp. When the ramp exceeds the control voltage, then the IC_{2A} comparator's output goes high, and the rising edge triggers one-shot IC_{1A} and switches on Q_3 through IC_{1B}, allowing the discharge of the capacitor C_1. When an input pulse triggers the circuit, any other trigger pulse that occurs before the falling edge of the delayed output pulse does not produce an output pulse; in other words, the circuit is not retriggerable. This feature permits you, at the same time, to divide and delay an input-trigger clock.

Although IC_1 and IC_2 can operate from a 3 to 16V supply, the minimum supply voltage of the circuit is 5V; otherwise, Q_1 and Q_2 approach saturation, generating to a less linear ramp voltage. Voltage comparator IC_{2A}, an STMicroelectronics (www.st.com) TS3702, has an input-common-mode-voltage range that includes ground, permitting you to monitor input voltages as low as 0V.

However, for correct operation of the circuit, the minimum control voltage must be greater than the saturation voltage of Q_3. For the components in **Figure 1**, the measured value is 12 mV. If you want to reduce this voltage, you can use a digital N-channel MOSFET with low on-resistance. The optional input lowpass filter, comprising R_6 and C_4, helps to clean noise from the dc-control voltage.

If a DAC drives the control input, you can build a digitally programmable delay generator. A suitable low-cost, 8-bit DAC is the AD558 from Analog Devices (www.analog.com), which features an internal precision bandgap reference to provide an output voltage of 0 to 2.56V, making 1 LSB equal to 1 μsec. It operates from 5 to 16V, with a 1-μsec settling time. The circuit's quiescent current, I_{DD}, is less than 300 μA because all ICs are micropower. EDN

REFERENCE

1 Bhandarkar, Santosh, "Single-IC-based electronic circuit replaces mechanical switch" *EDN*, March 15, 2007, pg 76, www.edn.com/article/CA6421439.

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READERS SOLVE DESIGN PROBLEMS

Circuit and software provide accurate recalibration for baseline PIC microcontroller's internal oscillator

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

All of Microchip's (www.microchip.com) baseline PIC microcontrollers have internal 4-MHz oscillators, which are useful for freeing up one or two pins for I/O use and allowing you to build minimal-component-count designs using these devices. You must calibrate the internal oscillator by reading a factory-programmed calibration setting that resides at the last address in the user-program memory and then writing that setting into the microcontroller's oscillation-calibration register during the application software's initialization of the device. Because the calibration value is unique to each microcontroller, problems arise for time-sensitive applications if you erase or overwrite the last address.

The circuit in **Figure 1** recovers the calibration value by recalibrating against a reference clock, the 4-MHz crystal. The frequency looks for the best calibration value to ensure that the microcontroller's internal oscillator runs within 1% accuracy at 4 MHz. You can download the microcontroller's program and a flow chart

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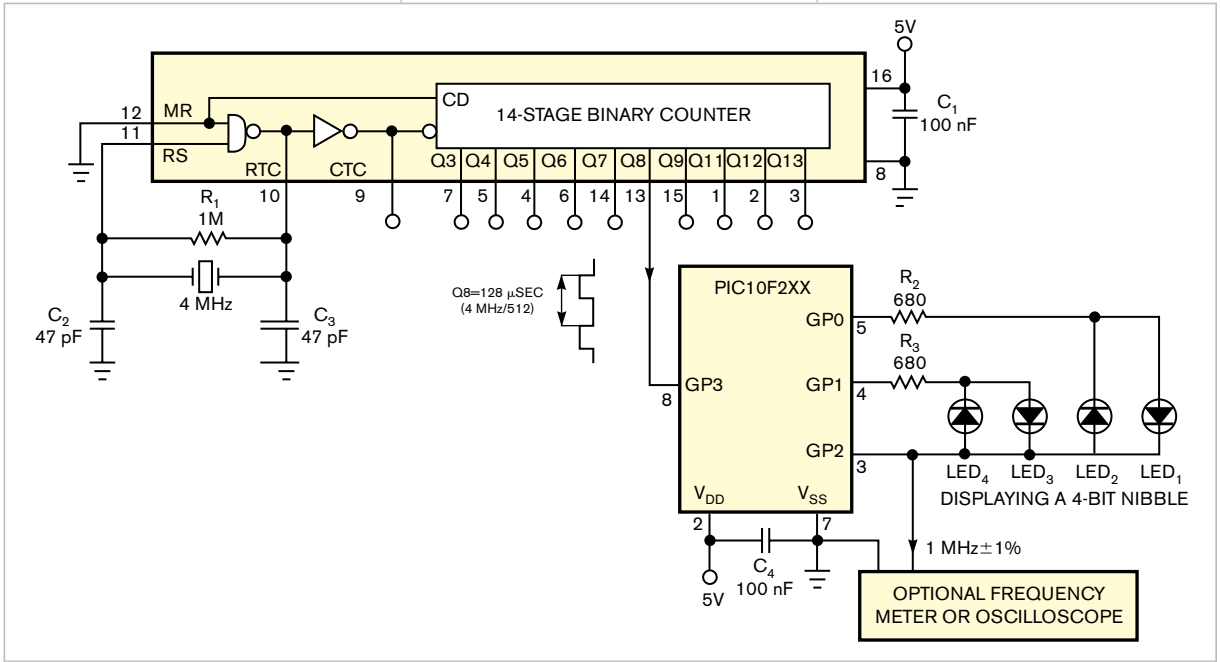

Figure 1 This circuit and an assembly-language program that occupies less than 250 bytes allow you to calibrate a PIC10F2xx microcontroller against a 4-MHz reference clock.

in a compressed zip file from www.edn.com/080501di1.

The baseline PIC microcontroller, which includes the PIC10F, PIC12C508/509/510, or PIC16F505/506 series, uses its internal timer, Timer 0, to count the number of instruction cycles that execute in one period from output Q8 of a Fairchild Semiconductor (www.fairchildsemi.com) CD4060 oscillator/divider to the only input, GP3, of the PIC microcontroller. The 4-MHz crystal drives the CD4060, which yields a period of 128 µsec from the output Q8.

The four LEDs display the two 4-bits nibbles of the 8-bit oscillation-calibration register's best value. Output GP2 acts as a multiplexing line to drive these LEDs for 8 to 10 sec and then as the oscillator output to yield a 1-MHz signal, which you can measure with a frequency meter or an oscilloscope. EDN

Microcontroller moving-dot display interface uses three I/O lines

Abel Raynus, Armatron International, Malden, MA

The moving-dot display has some benefits over the bar-graph display: It better indicates the location of a detected object in sonar and radar applications; it needs only one LED's current-limiting resistor instead of several; and it provides the same current for all LEDs, thus providing even brightness. When a new design required adding a seven-LED moving-dot display to an 8-bit, low-end microcontroller, a question arose about the corresponding interface. Of course, the most cost-effective approach is to directly connect the LEDs without any extra parts. But this approach needs seven vacant microcontroller-output pins, which microcontrollers with limited I/Os often cannot afford.

A previous Design Idea describes a one-wire interface that applies only to a bar-graph display, not to a dot display (**Reference 1**). Another tack would be interfacing using serial-to-parallel shift registers or a serial-input Johnson counter. But small microcontrollers often lack a SPI (serial-peripheral interface), and you must use firmware to re-create it (**Reference 2**). The method in this Design Idea needs three output lines—data, clock, and latch—and requires some firmware and hardware. Exploiting the fact that only one LED in a dot display should light at a time, you can use National Semiconductor's (www.national.com) CD4051 1-to-8 analog demultiplexer (**Figure 1**). This circuit needs three microcontroller outputs, and the firmware is simple and straightforward. The additional benefit is that the microcontroller now does not limit the LED current and voltage; you can choose them independently.

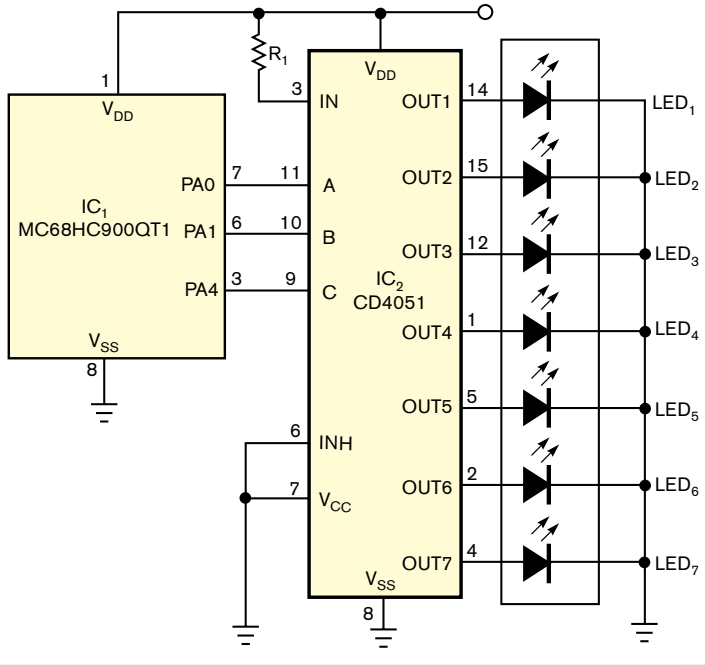

Figure 1 Using the 1-to-8 CD4051 analog demultiplexer you can interface a moving-dot LED display to a low-end microcontroller using just three outputs.

Listing 1, which you can download from the Web version of this Design Idea at www.edn.com/080501di2, provides demo firmware illustrating this design. The demo program automatically moves the lit dot back and forth by incrementing and decrementing a modulo-7 counter. Ideally, any three adjacent microcontroller outputs, such as pA0, pA1, and pA2, are available for the A, B, and C inputs of the CD4051. But, this scenario is not always possible. In this application of a low-end, eight-pin MC68HC908QT1 microcontroller, you can use pins pA2 and pA3 only as inputs. You can easily overcome this problem by programming, as **Listing 1** shows. This Design Idea applies to any small microcontroller because it uses only a standard instruction set. EDN

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Microcontroller displays multiple chart or oscilloscope timing ticks

William Grill, Honeywell, Lenexa, KS

While working with a 10-bit DI-184 module from Dataq to monitor and display vibration-sensor data, I found that, although the chart displays a time index, this time reference is not visible in the saved file. You can add time ticks, representing seconds or minutes, to a chart graphic by using a simple and inexpensive crystal-based microcontroller to generate a sequence of tags on a dedicated chart channel. **Figure 1** shows a small, eight-pin 12F508 microcontroller from Microchip Technology (www.microchip.com) that provides multiple timing ticks. **Listing 1**, the microcontroller's program is available in the Web version of this Design Idea at www.edn.com/080501di3. It offers four timing sequences. You can select a timing sequence by strapping pins 4 and 6 (**Table 1**, also at www.edn.com/080501di3).

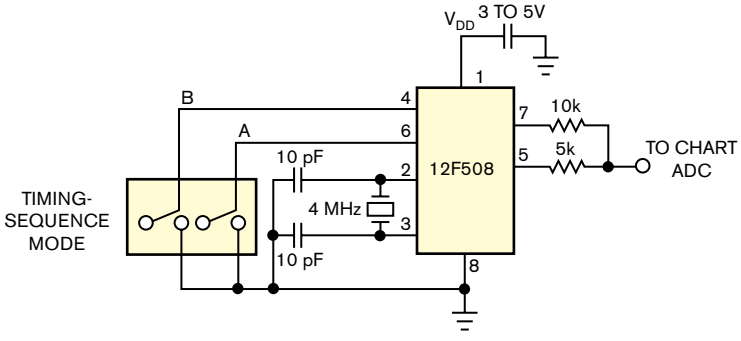

Figure 1 An 8-bit microcontroller with output pins 5 and 7 configured as a 2-bit DAC provides precise timing ticks to annotate captured data.

The 4-MHz crystal maintains a solid instruction-timing reference, and equalized coded branches in the **listing** maintain accurate timing ticks. You can also configure the 12F508 with an internal, 4-MHz RC oscillator. You base the coded loops on a sequence of exactly 25 instructions, and they provide a fundamental, base-reference loop that is exactly 100 instructions. A 16-bit register counter serves as the multiplier to produce the base timing. For use with scopes, you can recode the **listing** with minor changes to use 50 instructions or a 50-µsec base-timing-tick minimum. The 8-bit registers in the equalized loop provide multipliers to produce the additionally tiered output. The microcontroller uses two output pins, 5 and 7, as a pseudo 2-bit DAC. This configuration generates one of four voltage levels for timing ticks that display continuously, and you can record them along with application data. EDN

Fast-settling synchronous-PWM-DAC filter has almost no ripple

W Stephen Woodward,
Chapel Hill, NC

An inexpensive way to implement high-resolution digital-to-analog conversion is to combine microcontroller-PWM (pulse-width-modulated) outputs with precision analog-voltage references, CMOS switches, and analog filtering (**Reference 1**). However, PWM-DAC design presents a big design problem: How do you adequately suppress the large ac-ripple component inevitably present in the switch's outputs? The ripple problem becomes especially severe when you use typical 16-bit microcontroller-PWM peripherals for DAC control; such high-resolution PWM functions usually have long cycles because of the large 2^{16} countdown modulus of 16-bit

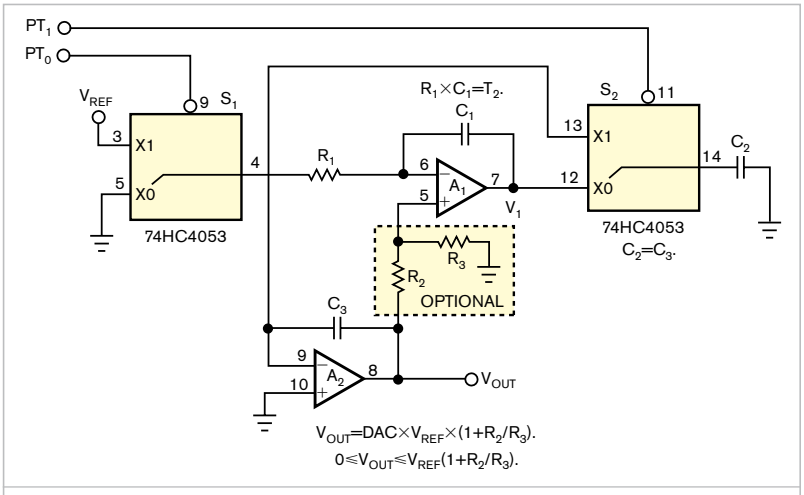

Figure 1 This DAC ripple filter combines a differential integrator, A_1, with a sample-and-hold amplifier, A_2, in a feedback loop operating synchronously with the PWM.

timers and comparators. This situation results in ac-frequency components as inconveniently slow as 100 or 200 Hz. With such low ripple frequencies, if you employ enough ordinary analog lowpass filtering to suppress ripple to 16-bit—that is, −96-dB—noise levels, DAC settling can become a full second or more.

The circuit in **Figure 1** avoids most of the problems of lowpass filtering by combining a differential integrator, A_1, with a sample-and-hold amplifier, A_2, in a feedback loop operating synchronously with the PWM cycle, T_2 in **Figure 2**. If you make the integrator time constant equal to the PWM cycle time—that is, $R_1 \times C_1 = T_2$—and, if the sample capacitor, C_2, is equal to the hold capacitor, C_3, then the filter can acquire and settle to a new DAC value in exactly one PWM-cycle time. Although this approach hardly makes the resulting DAC exactly "high speed," 0.01-sec settling is still 100 times better than 1-second settling. Just as important as speed, this improvement in settling time comes without compromising ripple attenuation. Ripple suppression of the synchronous filter is, in theory, infinite, and the only limit in practice is nonzero-charge injection from S_2 into C_3. The choice of a low-injected-charge switch for S_2 and an approximately 1-μF capacitance for C_3 can easily result in ripple amplitudes of microvolts.

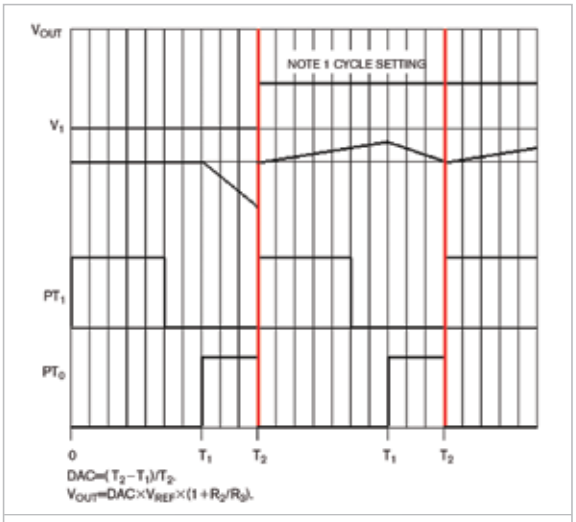

Figure 2 The DAC output settles within one cycle.

Optional feedback-voltage divider R_2/R_3 provides flexibility in a DAC-output span with common voltage references. For example, if $R_2 = R_3$, then a 0 to 10V output span will result from a 5V reference. An additional advantage of this method of span adjustment is that output ripple remains independent of reference amplification. EDN

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Switched-gain op amp serves as phase detector or mixer

W Bruce Warren, Marietta, GA

Some op amps, such as the AD8041 from Analog Devices (www.analog.com) and the EL5100 from Intersil (www.intersil.com), provide a disable pin, which allows you to parallel the outputs of several op amps for video multiplexing. In addition to this multiplexing, you can also use the disable function to configure the op amp as a phase detector or a frequency mixer. **Figure 1** shows how the disable function can implement a low-frequency phase detector. You can switch the gain of this circuit's amplifier on and off at the rate of the phase-reference signal. Doing so produces a dc component at the output of the op amp. This component is proportional to the cosine of the phase difference between the phase of the input signal and the phase of the reference signal.

In the circuit, the output of the op amp is: $V_{OUT}(t) = V_{IN}(t) \times G(t)$, where $V_{IN}(t) = A\cos(\omega_{REF}t + \theta)$, and G(t) is the time-varying gain of the op amp. G(t) is a 50%-duty-cycle square wave that switches from zero to G_0 at the frequency of the phase-reference signal. G_0 is the gain of the op amp when the op amp is enabled. Because G(t) is a time-varying periodic function expand it in a Fourier series: $G(t) = G_0[1/2 + 2/\pi\{\cos(\omega_{REF}t) - 1/3\cos(3\omega_{REF}t) + 1/5\cos(5\omega_{REF}t) + \ldots\}]$.

Multiplying $V_{IN}(t)$ by G(t) and retaining only the dc terms, the dc component of the output is $V_{OUT}(dc) = (AG_0/\pi)\cos(\theta)$.

The EL5100 op amp in **Figure 1** has a 200-MHz unity-gain bandwidth, and you can turn its output on and off by applying a square wave of at least 0 to 4V to the output-disable terminal, Pin 8. Using the feedback resistances shown and with $G_0 = 3$, the peak output voltage of the phase detector is approximately equal to the peak value of the input signal. The EL5100 has a disable time of 180 nsec and an enable time of 650 nsec, which allows you to gain-switch the device to approximately 250 kHz. At higher frequencies, the gain of the phase detector falls off because the gain-switching no longer has a 50% duty cycle.

The lowpass filter following the op amp extracts the dc component of $V_{OUT}(t)$ and has a 3-dB point at 800 Hz. A 100Ω resistor in series with the 0.1-μF shunt capacitor limits the phase lag of the filter when the phase detector is inside a PLL (phase-locked loop). The values in **Figure 1** provide a maximum phase lag of approximately 65°. Using 5 and −5V power sup-

plies allows the output swing of the phase detector to be symmetric at approximately 0V. If your design doesn't require this symmetry, you can use a single 5V supply with 2.5V positive offset-biasing of the op amp. In this case, the output swing is symmetric with respect to 2.5V. As with all wide-bandwidth-op-amp circuits, you should take care to connect the power-supply bypass capacitors to ground with short connections and as close to the op amp's power-supply pins as possible to avoid instability.

This same gain-switching scheme also works as a frequency mixer. If the input signal is at frequency ω_S and the reference-square-wave input is at frequency ω_{lo}, the IF output signal is $(\omega_{lo}-\omega_S)$ or $(\omega_{lo}+\omega_S)$. You obtain the desired IF signal by replacing the output lowpass filter in **Figure 1** with a bandpass filter tuned to the desired IF frequency of $\omega_{lo}\pm\omega_S$. If the switching rate for the reference signal is higher than the disable function can provide, then you can use the harmonic mixing using the odd-order harmonics of the reference signal. This approach reduces the gain of the mixer by a factor of 1/N, where N is the number of the harmonic you are using. EDN

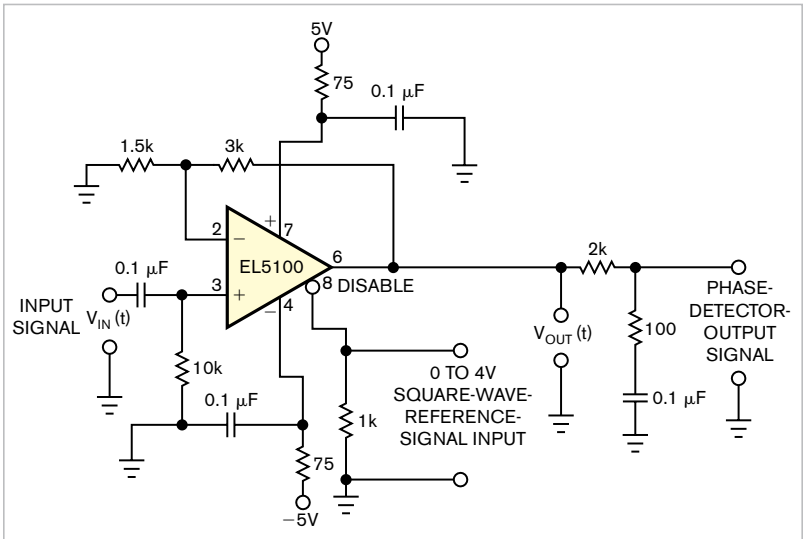

Figure 1 By switching the disable input of the op amp at a reference frequency and lowpass-filtering its output, you can obtain a dc voltage proportional to the phase difference of the switching frequency and the input frequency.

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READERS SOLVE DESIGN PROBLEMS

Small capacitor supports telecom power supply during brownouts

Samuel Kerem, Rockville, MD

This Design Idea shows how to keep telecom equipment operational during a short brownout. You must first understand a few details regarding the power supply for telecom equipment. The common voltage of the power source that feeds telecom equipment is −48V, although the actual voltage can range from −42.5 to −56V, −40 to −60V, or even beyond. The common power-"brick" dc/dc converter operates over the −36 to −75V range. A brownout occurs when the −48V source drops to 0V and stays there as long as 10 msec.

Using capacitive storage that connects to the brick's input is an obvious approach to overcoming this problem, but a shortcoming becomes apparent when you understand the reality of the −48V supply. For example the energy in a capacitor charged to voltage is $(C \times V^2)/2$, where C is the capacitance and V is the voltage. The brick stops its operation when the capacitor discharges to 36V. In general, the energy available to support the brick's operation is, therefore:

$$U = C \times \frac{\left(V_1^2 - V_2^2\right)}{2},$$

where V_1 and V_2 are the beginning and final −36V voltages, respectively, and U is the energy. Also, $U = P \times t$, where P is power and t is time. Using these equations, you can find the time that the equipment will stay operational:

$$t = C \times \frac{\left(V_1^2 - V_2^2\right)}{2 \times P},$$

or, to define the capacitor's value:

$$C = \frac{2 \times P \times t}{V_1^2 - V_2^2}.$$

Assume that the brownout occurs when the voltage at the brick's input is −39V, which is the case when −48V is −40V but the brick loses at least 1V because of protective ORed diodes in a hot-swap configuration. Also, assume that the storage capacitor charges to −39V. The equipment operates until this storage capacitor discharges to −36V. Assume that the equipment consumes 100W. To store enough energy for 5 msec, the capacitor's value would have to be approximately 4500 µF. The capacitor must be rated for the maximum possible incoming voltage, which can be more than 75V, so the minimum rating of 100V is a must. The 4500-µF, 100V capacitor is a sizable part. If the design requires twice as much operational time at a power consumption of 300W, the capacitor must have a value of 27,000 µF and 100V.

This Design Idea still requires a capacitor, but the capacitor has a lower value—that is, 200 µF versus 4500 µF—and sustains 100W during a 5-msec brownout. This approach increases reliability and reduces cost and size. The hidden feature is the power brick's ability to stay operational over the input range of −36 to −75V and even to operate under surges greater than

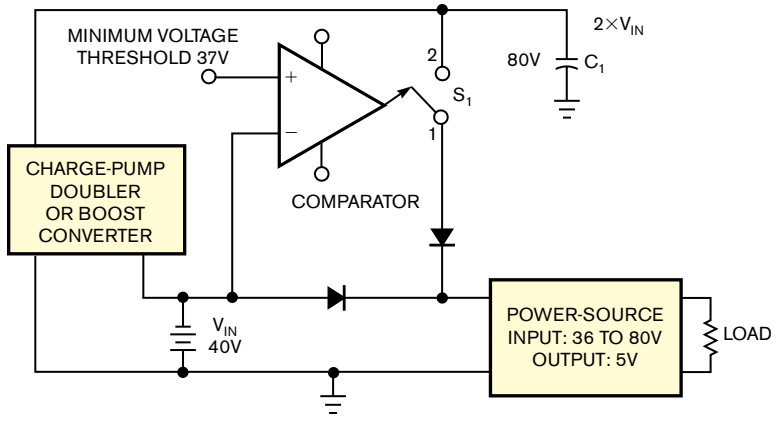

Figure 1 Charged to double the input voltage, the energy stored in capacitor C_1 dumps into the input of the "brick" power supply during brownouts when the input voltage drops to less than −37V.

DIs Inside

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−80V. **Figure 1** shows how you can use this feature. The **figure** depicts a positive input voltage. The brick is isolated, so polarity is irrelevant, but positive interpretation is easier to illustrate.

Remember that the stored energy in the capacitor grows exponentially, whereas the capacitor's voltage increases linearly. The doubler charges C_1 to twice the input voltage or at least to 80V. Even if, hypothetically, you expect a 5-msec brownout as often as 10 sec, the current to charge 200 µF is still only approximately 3 mA. The comparator watches the input voltage, and, as soon as it drops below 37V, switch S_1 closes, and the energy from C_1 discharges to the power brick. EDN

Tiny microcontroller hosts dual dc/dc-boost converters

Dhananjay V Gadre, Netaji Subhas Institute of Technology, New Delhi, India

Batteries are the typical power sources for portable-system applications, and it is not unusual these days to find microcontroller-based portable systems. A variety of microcontrollers operates at low power-supply voltages, such as 1.8V. Thus you can employ two AA or AAA cells to power the circuit. However, if the circuit requires higher voltage—for LED backlighting for an LCD, for example, which requires approximately 7.5V dc—you must employ a suitable dc/dc converter to boost the power-supply voltage from, for example, 3V to the required voltage. However, you can also employ a microcontroller to develop a suitable dc/dc-boost-voltage converter (**Reference 1**) with the help of a few additional discrete components.

This Design Idea shows how to create not just one, but two dc/dc converters with just a tiny eight-pin microcontroller and a few discrete components. The design is scalable, and you can adapt it for a wide range of output-voltage requirements just by changing the control software for the microcontroller. You can even program the microcontroller to generate any required output-voltage start-up rate. **Figure 1** shows the basic topology of a boost switching regulator. The output voltage in such a regulator is more than the input voltage. The boost switching regulator operates in either CCM (continuous-conduction mode) or DCM (discontinuous-conduction mode). It is easier to set up a circuit for DCM operation (**Reference 2**). The name comes from the fact that the inductor current falls to 0A for some time during each PWM period in DCM; in CCM, the inductor current is never 0A. The maximum current passes through the inductor at the end of high period of the PWM output (when the switch is on) and is:

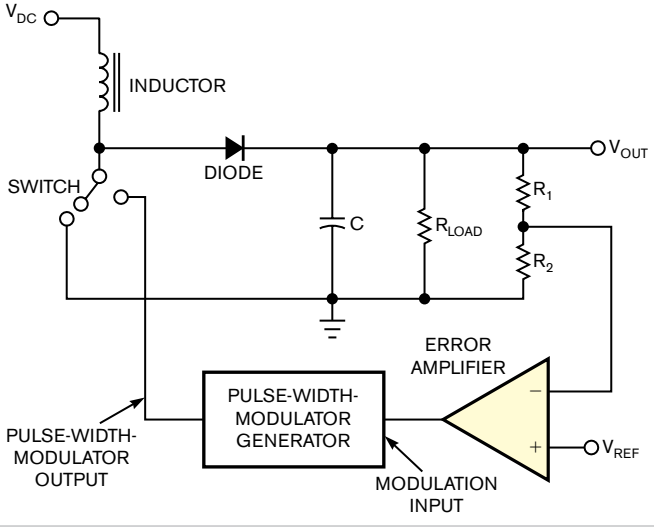

Figure 1 The output voltage in a boost switching regulator is more than the input voltage. The boost switching regulator operates in either CCM (continuous-conduction mode) or DCM (discontinuous-conduction mode)

$$I_{L_{MAX}} = \frac{V_{DC} \times D \times T}{L}, \quad (1)$$

where V_{DC} is the input voltage, D is the duty cycle, T is the total cycle time, and L is the inductance of the inductor. The current through the diode falls to zero in time T_R.

$$T_R = \frac{V_{DC} \times D \times T}{(V_{OUT} - V_{DC})}, \quad (2)$$

The load current is the average diode current,

$$I_{LOAD} = \frac{I_{L_{MAX}} \times T_R}{2 \times T}, \quad (3)$$

from **equations 1** and **2** and simplifies to:

$$I_{LOAD} = \frac{V^2_{DC} \times D^2 \times T}{2 \times L \times (V_{OUT} - V_{DC})}. \quad (4)$$

The output voltage, V_{OUT}, is:

$$V_{OUT} = V_{DC} \times \left(1 + \frac{V_{DC} \times D^2 \times T}{2 \times L \times I_{LOAD}}\right), \quad (5)$$

The value of the output capacitor, which determines the ripple voltage, is:

$$\frac{dV}{dt} = \frac{I}{C}. \quad (6)$$

where dV/dt represents the drop in the output voltage during the period of the PWM signal, I is the load current, and C is the required output capacitor.

The total period of the PWM wave

is T and is a system constant. D is the duty cycle of the PWM wave, and T_R is the time during which the diode conducts. At the end of T_R, the diode current falls to 0A. The period of the wave is $T>D\times T+T_R$ for DCM. The difference of the PWM period, T, and $(D\times T+T_R)$ is the dead time.

The switch that operates the inductor is usually a BJT (bipolar-junction transistor) or a MOSFET. A MOSFET is preferable because of its ability to handle large current, better efficiency, and higher switching speed. However, at low voltages, a suitable MOSFET with low enough gate-to-source threshold voltage is hard to find and can be expensive. So, this design uses a BJT (**Figure 2**).

Microcontrollers offer PWM frequencies of 10 kHz to more than 200 kHz. A high PWM frequency is desirable because it leads to a lower inductor value, which translates to a small inductor. The Tiny13 AVR microcontroller from Atmel (www.atmel.com) has a "fast" PWM mode with a frequency of approximately 37.5 kHz and a resolution of 8 bits. A higher PWM resolution offers the ability to more closely track the desired output voltage. The maximum inductor current from **Equation 1** is 0.81A for a 20-µH inductor. The transistor that switches the inductor should have a maximum collector current greater than this value. A 2SD789 NPN transistor has a 1A collector-current limit, so it is suitable for this dc/dc converter. The maximum load current achievable with these values, from **Equation 4**, is 54 mA and thus meets the requirement of maximum required load current for an output voltage of 7.5V.

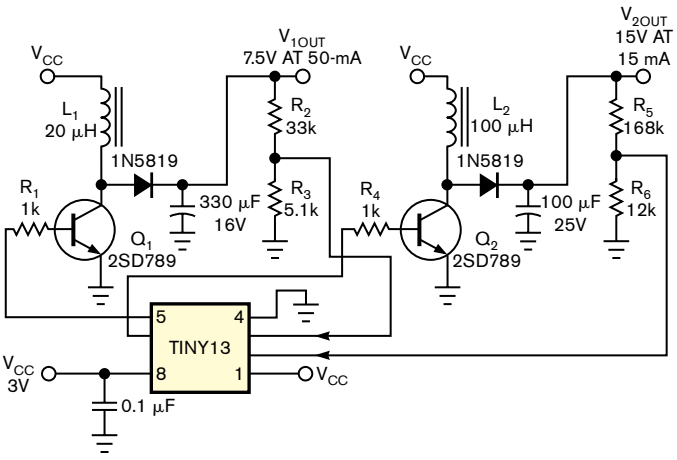

Figure 2 An Atmel Tiny13 AVR microcontroller regulates two boost-dc/dc-converter outputs using its internal ADCs and PWMs.

The Tiny13 microcontroller boasts two high-speed PWM channels and four 10-bit ADC channels. Another PWM channel and an ADC channel create the second dc/dc converter for an output voltage of 15V and a maximum load current of 15 mA. The inductor for this converter has a value of 100 µH. To calculate the output-capacitor value, use **Equation 6**. For a 5-mV ripple, the value of the capacitor for 7.5V output voltage is 270 µF, because the output current is 50 mA and the PWM-time period is 27 µsec, so this circuit uses the nearest larger value of 330 µF. Similarly, for the 15V output voltage, the required capacitor value is 81 µF, so the design uses a 100-µF capacitor.

The programs for the microcontroller are in C and use the open-source AVR GCC compiler (www.avrfreaks.net). They are available in the Web version of this Design Idea at www.edn.com/080515di1. The AVR Tiny13 microcontroller operates at an internal clock frequency of 9.6 MHz without an internal-clock-frequency divider, so the PWM frequency is 9.6 MHz/256=37.5 kHz. The internal reference voltage is 1.1V. The main program alternately reads two channels of ADCs that monitor the output voltages in an interrupt subroutine. The main program executes an endless loop, monitoring the output voltage by reading the ADC values and adjusting the PWM values accordingly. EDN

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Cross-coupled gates prevent push-pull-driver overlap

Richard Rice, Oconomowoc, WI

Overlap—the short period during which a push-pull drive's two transistors are both simultaneously on—is a common problem with these drives in a center-tapped transformer's primary. Overlap causes a large current spike and increased switching losses. The fact that saturated transistors turn off more slowly than they turn on causes the problem. One method of preventing overlap is to provide a time delay after turning off one transistor and before turning on the other one. This method requires several extra components and must include enough delay for a worst-case scenario. This Design Idea uses cross-coupled gates to prevent one transistor from turning

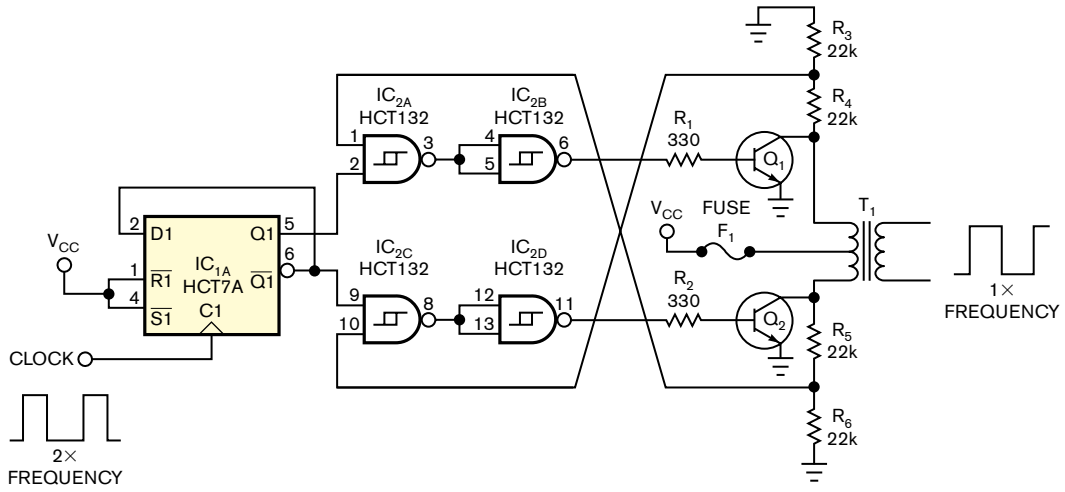

Figure 1 Cross-coupled gates prevent one transistor from turning on before the other turns off. Fuse F_1 protects against catastrophic failures.

on before the other turns off (**Figure 1**). For simplicity, the **figure** omits the depiction of bypass capacitors, snubber networks, and other components unnecessary for illustrating the method.

Gate IC_{2A} prevents Q_1 from turning on until Q_2 turns off. Likewise, gate IC_{2C} prevents Q_2 from turning on until Q_1 turns off. Gates IC_{2B} and IC_{2D} function as inverters to provide the correct polarity to drive the switching transistors. Monitoring the transistors' collector voltages senses the turn-off of each transistor using the voltage dividers R_3/R_4 and R_5/R_6. Because the collector voltage swings to twice the supply voltage, the voltage dividers halve the voltage. The impedance of the voltage dividers also limits the gates' input current to a safe level during overshoot. The switching frequency is one-half the input-clock frequency. D-type flip-flop IC_{1A} divides the input-clock frequency by two and provides complementary outputs with a 50% duty cycle. The complementary outputs drive the switching transistors in an alternating sequence. The secondary of transformer T_1 provides an isolated square-wave output. EDN

Save valuable picoseconds using ECL-wired OR

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

Often, when you are designing with high-speed ECL (emitter-coupled logic), you have too little time between clock cycles to implement logic functions using gates between flip-flops. In these cases, you can derive equivalent-logic functions using the wired-OR and flip-flop complementary inverted outputs (**references 1**, **2**, and **3**). You can parallel the emitter-follower outputs of ECL with a pulldown resistor to implement the OR function with almost no time-delay penalty. Complementary outputs—one inverted—provide delay-free logic inversions.

This Design Idea uses the older Motorola (www.motorola.com) 10H ECL logic family, the fastest available when I was building the design (**Figure 1**). Newer ECL families are much faster, but the same wired-OR principle applies. For clarity, the **figure** omits power and 50Ω pulldown resistors. This design needed an XOR comparison between a PRBS (pseudorandom-binary-sequence) data stream and a local PRBS reference for a BER (bit-error-rate) counter running at 250 Mbps (**Figure 1a**). A problem occurred with the design, however: The clock period at 250 Mbps is 4 nsec, whereas the 10H107 XOR/XNOR gate's maximum propagation delay is 1.7 nsec. In addition, the 10H131 flip-flop's maximum propagation delay is 1.8 nsec, and the required input-setup time is 0.7 nsec. All these delays total 4.2 nsec, which exceeds the 4-nsec clock period by 200 psec. Adding a fourth flip-flop with wired-OR outputs to replace the 10H107 XOR/XNOR solves the problem (**Figure 1d**).

The XNOR-equivalent function uses NOR, AND, and OR functions (**Figure 1b**). The circuit in **Figure 1c** separates the NOR into the equivalent OR with an output inverter and converts the AND into the equivalent OR with inverted inputs and output. Now, the circuit uses only ORs and inverters. This form is necessary for implementing the wired-OR equivalent (**Figure 1d**). In this case, the inverted-complementary outputs of the flip-flops replace the

inverters, and a parallel electrical connection between the flip-flops' outputs replaces the OR gates. EDN

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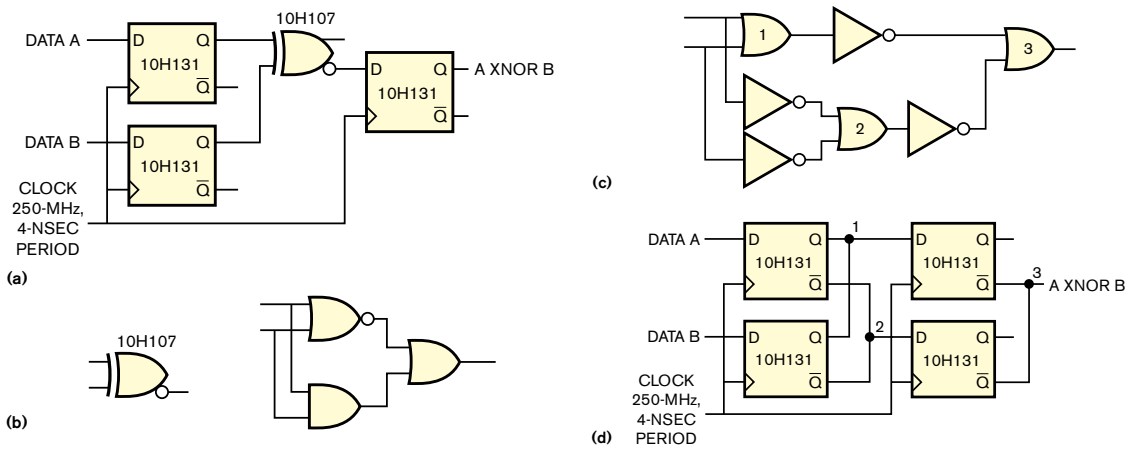

Figure 1 The XNOR comparison of inputs A and B results in too much propagation delay to guarantee setup at the final flip-flop's input (a). The equivalent XNOR circuit uses NOR, AND, and OR gates (b), and OR gates and inverters realize the XNOR function (c). You can also implement the circuit using wired ORs (d) to eliminate the interflop XNOR-gate delay and almost double the usable clocking speed.

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READERS SOLVE DESIGN PROBLEMS

Capacitive touch switch uses CPLD

Rafael Camarota, Altera, San Jose, CA

Capacitive touch switches work by measuring the change in capacitance of a PCB (printed-circuit-board) pattern depending on the placement of a user's finger over a sensing pad. Capacitive switches are becoming popular because they are less expensive than mechanical switches. Using the features of an Altera (www.altera.com) MAX IIZ CPLD (complex-programmable-logic device), you can implement a touch-switch decoder with no external components. The touch sensor employs an 8-mm-diameter sensing pad on the PCB using the solder mask as a dielectric. The circuit decodes a single switch, but you could use the approach for multiple switches, and it has programmable sensing thresholds that allow for different PCB layouts and dielectrics.

Figure 1 shows a simple circuit with no external components other than the capacitive-switch layout on the PCB. A basic touch-switch PCB layout is on the left. It comprises only an 8-mm copper circle surrounded by copper that connects to ground. The dashed line shows that the center sensor connects to the CPLD using a via and a backside copper trace. A solder mask acting as a dielectric covers the center sensor and ground. The PCB touch sensor becomes a variable capacitor, C_{TOUCH}.

The variable capacitor is part of a relaxation oscillator. The CPLD has a built-in weak pullup resistor on each I/O pin. C_{TOUCH} and the weak pullup resistor create an RC circuit. If the PINOSC (pin-oscillator) signal is low, the I/O pin will be low, making the D input to the PINOSC LPM (library-of-parameterized-modules) register low. LPM blocks come from the Quartus II LPM.

The register and other logic in the circuit use a free-running, 4.4-MHz internal oscillator, ALTUFM oscillator, as a clock. On the rising edge of the clock, PINOSC goes low, making the buffer-driving pin go to a high-impedance state. The weak pullup resistor slowly makes the pin voltage rise based on an RC time constant. Not touching the switch causes it to have the lowest capacitance and fastest rise time. Touching the switch causes it to have the highest capacitance and the slowest rise time. The pin-I/O buffer uses the Schmitt-trigger option of the CPLD to reduce the noise sensitivity of

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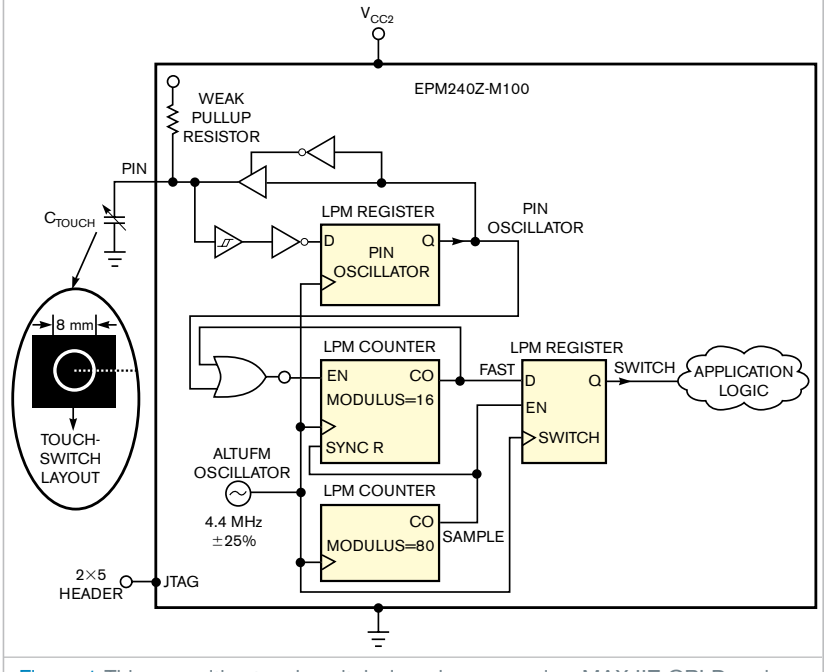

Figure 1 This capacitive-touch-switch decoder uses only a MAX IIZ CPLD and no external components other than the capacitive switch.

the slow-rising pin signal. Once the pin node reaches the high-voltage threshold, the D input of the PINOSC registers a zero. On the next clock edge, the PINOSC signal goes low, driving the pin node low for one full clock cycle. This PINOSC circuit oscillates at two fundamental frequencies, depending on the state of the touch capacitor. Putting the register into the oscillator loop reduces noise and makes the oscillator stable and synchronous with the decoding logic. The PINOSC period is always a multiple of 1/4.4 MHz or the frequency of the internal oscillator.

The switch decoder counts the period of 16 PINOSC cycles and compares it with a known time period. If 16 or more cycles happen in less than the sample period, it means that no one is touching the switch. If fewer than 16 cycles happen in the sample period, it means that someone is touching the switch, and the PINOSC oscillation becomes slower. The lower LPM counter sets the sample period.

For example, the sample signal was active once every 80 clock cycles in a prototype (**Figure 2**). The upper LPM counter measures the period of 16 PINOSC cycles. After 16 cycles, the fast signal goes high and stays high until the sample signal resets it. The fast signal is a one in the prototype when 16 cycles occur in fewer than 80 cycles, making the fast signal a one when the sample signal is a one. When the sample signal is a one, the fast value clocks into the switch-LPM register. The switch-signal value updates every sample cycle with the current capacitive switch state. When you touch the switch, PINOSC is slow, and the fast signal remains a zero when the sample signal is a one, making the switch output zero. In the prototype design, the PINOSC period was three clock cycles when someone touched it and nine cycles when no one touched it. The switch threshold was five cycles. Therefore, the lower LPM-counter modulus was 5×16=80. You can use any value from four to eight, but four is too sensitive, and eight does not work for small fingers; hence, five is the best value. The upper LPM-counter modulus affects noise sensitivity. The larger the count, the more the circuit averages the period of oscillation. A low modulus makes the circuit more sensitive to random system noise. The five-cycle sensing point also allows margin for the ±25% variation among parts of the internal oscillator frequency. EDN

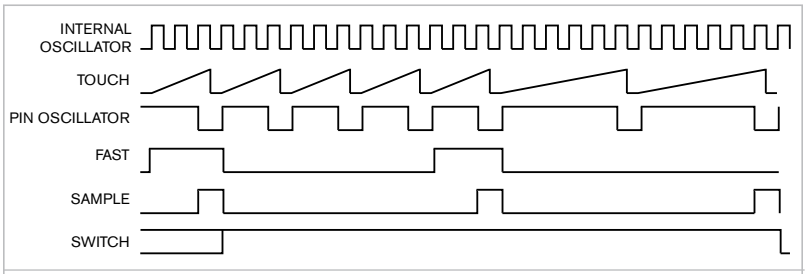

Figure 2 Representative waveforms that Figure 1 illustrates have a top-counter modulus of 3; a bottom-counter modulus of 12; and pin-oscillator periods of 3 and 6, respectively.

Bit-shifting method performs fast integer multiplying by fractions in C

Aaron Lager, Panamax Furman, Santa Rosa, CA

This Design Idea presents a method for fast integer multiplying and multiplying by fractions. What can you do when you lack access to a hardware multiplier or MAC (multiply/accumulate) function and you need to multiply by something other than a power of two? One option is to include the math.h function and just sling around the multiplication operator and watch your code bloat and slow to a crawl. Option two is to get fancy with bit shifting. The general idea is to find powers of two, including zero, that you can add to achieve the multiplier you need. This method works because of the distributive properties of multiplication. Using the distributive properties of multiplication, you can, for example, rearrange the problem of: 12×12=144→(4+8)×12=144→(12×4)+(12×8)=144. This version is amenable to implementation in C code because four and eight are powers of two. To implement the multiplications, you use the exponent of the power-of-two representation for your code as an integer shift. Because $4=2^2$ and $8=2^3$, you use two and three as your shift factors.

For example, multiply the variable foo by 12 to get 144: BYTE foo=12: foo=((foo<<3)+(foo<<2)). Left-shifting by three is the same as multiplying by eight, and left-shifting by two is the same as multiplying by four. Another example is multiplying by six: 6×10=60→(2+4)×10=60→(2×10)+(4×10)=60. BYTE foo=10; foo=((foo<<1)+(foo<<2)). Left-shifting by one is the same as multiplying by two, and left-shifting by two is the same as multiplying by four.

Using this same theory of distribution, you can also perform fractional multiplication or division. This method creates rounding errors just like dividing integers by values that are not powers of two does with math.h functions and the division operator.

One example is 2.5×10=25→(2+0.5)×10=25→(2×10)+(0.5×10)=25. The result is ((foo<<1)+(foo>>1)). Left-shifting by one is the same as multiplying by two, and right-shifting by one is the same as dividing by two or multiplying by 0.5. Another example is

3.125×80=250→(2+1+0.125)×80=250→(2×80)+(1×80)+(0.125×80)=250. The result is ((foo<<1)+foo+(foo>>3)). Left-shifting by one is the same as multiplying by two, multiplying by one is the same as adding the multiplicand once to the result, and right-shifting by three is the same as dividing by eight or multiplying by 0.125. A third example is 2.625×80=210→(2+0.5+0.125)×80=210→(2×80)+(0.5×80)+(0.125×80)=210. The result is ((foo<<1)+(foo>>1)+(foo>>3)). Left-shifting by one is the same as multiplying by two, right-shifting by one is the same as dividing by two or multiplying by 0.5, and right-shifting by three is the same as dividing by eight or multiplying by 0.125.

All of these examples take up less space and are faster than calling the standard 8×8-multiply function or division function from most standard math libraries. Also, you should note that, if the result of the variable you are multiplying can ever exceed 8 bits, then you should use a word function that can store 16 bits of your result, and you should use casting on the outer parentheses. The result is (word)((foo<<1)+(foo>>1)+(foo>>3)).EDN

RS-232-to-TTL converter tests UARTs with a PC

Matthieu Bienvenüe, Malissard, France

You often need an RS-232-to-TTL adapter for debugging or testing UARTs using a computer. But most of these adapters require an external power-supply adapter to power up the RS-232 transceiver. This external adapter increases the number of cables on your desk and uses no flow-control signals. This Design Idea describes how you can use these signals as power sources. It uses the RTS (request-to-send) and DTR (data-terminal-ready) signals, which provide a positive voltage when you open the PC's COM port (**Figure 1**). The voltage on those pins can differ from one computer to another but is generally higher than 6V, which is sufficient to power the adapter.

A standard RS-232 MAX3232 line driver from Maxim (www.maxim-ic.com) performs the TTL-to-RS-232 conversion. The MAX3232 accepts a 5 or 3.3V supply voltage, which is switch-selectable using S_1. D_1 and D_2 block the negative voltage that occurs when the COM port is closed. Q_1, R_3, S_1, and zener diodes D_3 and D_4 form a simple voltage regulator. LED_1 signals that the COM port is open. R_1, R_5, and R_6 protect the circuit under test and the line driver. The use of a pull-up resistor for R_2 avoids the need for an open input. This circuit has successfully undergone testing with a laptop computer, which provides a 6V power supply. The circuit works well at speeds as high as 115,200 bps.EDN

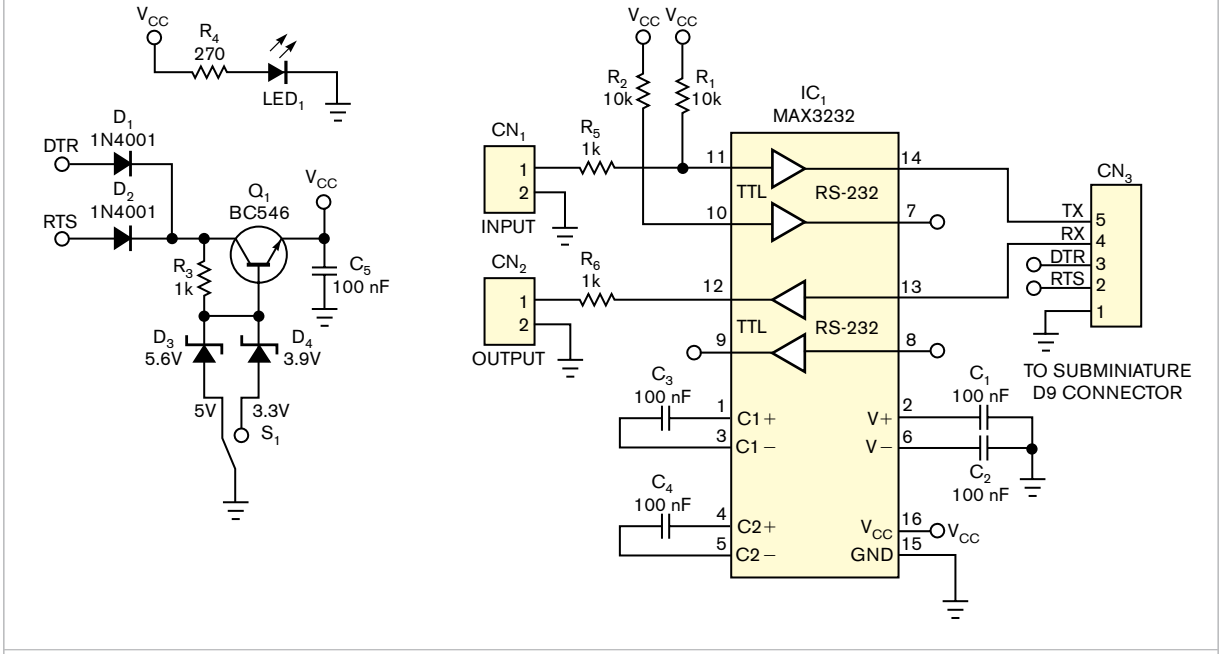

Figure 1 An RS-232-to-TTL converter uses the unused DTR and RTS outputs of a PC's COM port to self-power the circuit.

Hot-swap circuit allows two computers to monitor an RS-232 channel

Jeff Patterson, All Weather Inc, Sacramento, CA

The hot-swap serial-interface circuit in **Figure 1** allows two computers to see all of the communication between each computer and each device on the communication network for that serial port. This circuit allows each computer to determine what the other is doing and receive all of the data from the peripheral device. Only one device can transmit at a time; otherwise, the transmitted data becomes corrupted. This circuit allows two computers in a hot-swap configuration to know when to become the master computer. When the master computer fails, the slave computer stops receiving the data requests that the master supplies, and the slave then becomes the master. This approach allows for computer redundancy in applications in which a master computer that is communicating with an RS-232 device must always be operating. When you replace the failed computer, it "hears" that a master computer is communicating with the device and operates in slave mode while waiting for the current master to fail.

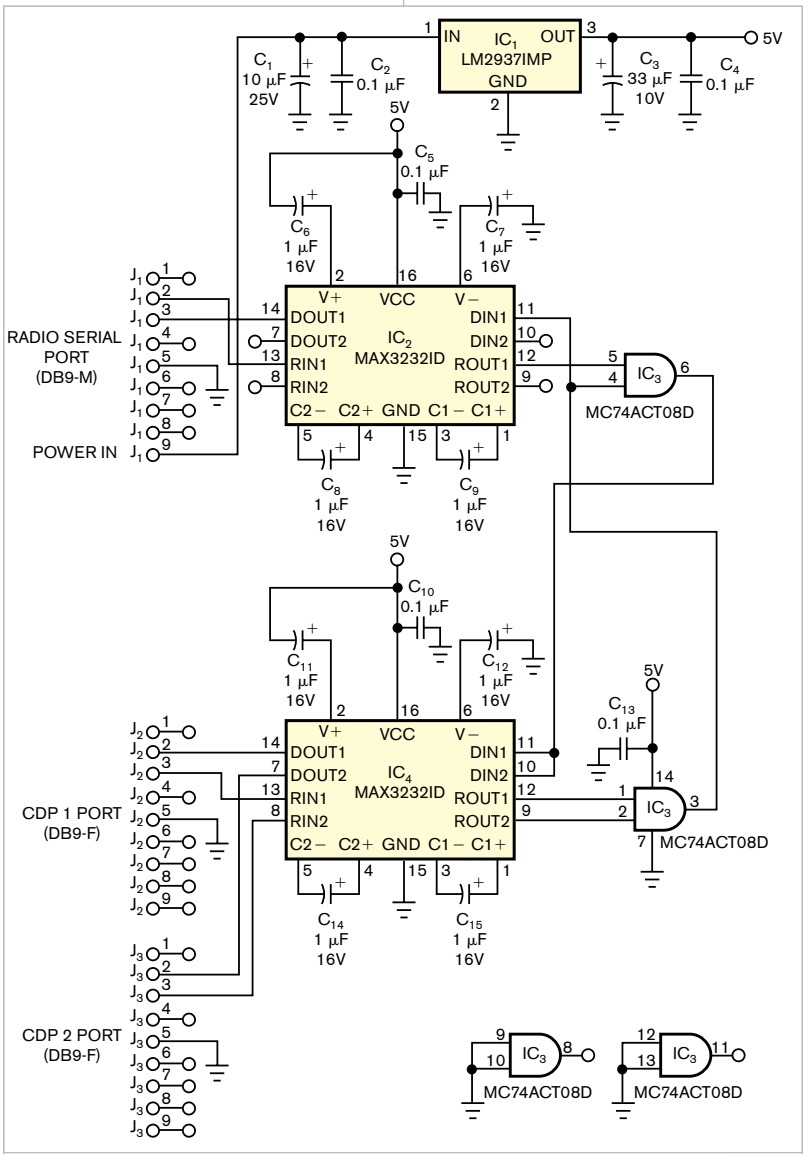

Figure 1 This hot-swap RS-232 interface allows two computers to monitor traffic on a computer's RS-232 port.

This circuit allows two DTE (data-terminal-equipment) computers to use one DCE (data-communications-equipment) RS-232 peripheral device. This device is usually a communication interface, such as a UHF radio or an RS-232-to-RS-485 converter. The board requires 9 to 15V dc to operate. You must provide this voltage on Pin 9 of the peripheral RS-232 device.

The transmitted RS-232 signal from the peripheral device converts to a TTL signal through level converter IC_2 and feeds into an AND gate. The output of this AND gate feeds into two inputs of another level converter, IC_4. These RS-232 outputs travel to the input lines (Pin 2) of the two monitoring computers. When one of the computers transmits on Pin 3 of its serial port, its output converts to TTL levels with IC_4. The TTL-converted outputs of both computer serial ports feed into an AND gate. The default, or off, level for a computer serial port is −12V dc. The level converter inverts the signal as part of the conversion to TTL levels. This action makes the default a high level going to the AND gate, allowing the data on the other input of the AND gate to pass to the output of the AND gate.

The output of this AND gate goes to the second input of the AND gate that receives the output of the peripheral device as well as the input into the level converter going to the input of the peripheral device at Pin 3. This action enables the output of one of the two computers to return to the computer that transmitted the data as well as to the other computer and the peripheral device. EDN

Improved laser-diode-clamp circuit protects against overvoltages

James Zannis, Baulne-en-Brie, France

Expensive semiconductor laser diodes have no tolerance for fast voltage or current transients. To minimize the risk of damage, a standard JFET-clamp circuit shorts the laser when there is no supply voltage, thus protecting it against such transients (**Figure 1**). When the negative supply rail comes up, the JFET turns off. This circuit is effective for low-power laser diodes but may not be so for diodes with power dissipation greater than 150 mA. The maximum cutoff current of the JFET sets this limit. If it becomes necessary in an emergency to clamp the laser during normal operation, the selected JFET might not adequately shunt the current. Higher-current JFETs are available but are more expensive and difficult to procure.

The circuit in **Figure 2** avoids these deficiencies. It is similar to the standard JFET circuit but has a supplementary bipolar transistor that shunts most negative-going currents when the JFET is on. R_2 prevents the gate of Q_1 from floating, and R_3 ensures rapid turn-off of Q_2. The 1N914 diode bypasses any positive-going transients. The RC circuit ensures an adequately slow response; therefore, the transition between on and off is smooth. EDN

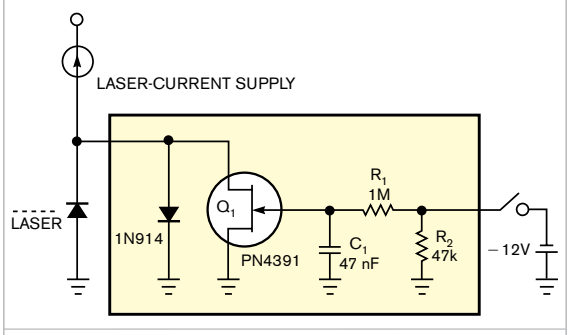

Figure 1 This circuit protects low-power laser diodes but is not suitable for higher-power laser diodes.

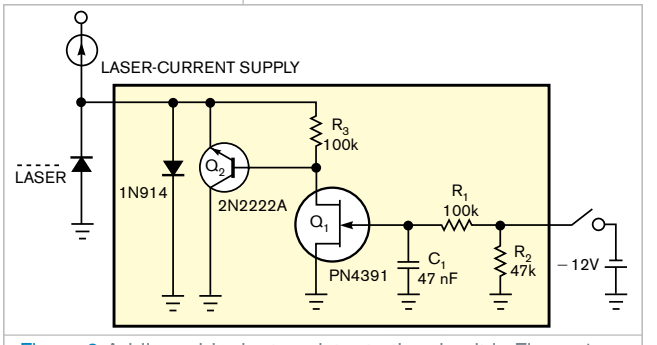

Figure 2 Adding a bipolar transistor to the circuit in Figure 1 allows the circuit to protect higher-power laser diodes.

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READERS SOLVE DESIGN PROBLEMS

Precision temperature controller has thermal-gradient compensation

W Stephen Woodward, Chapel Hill, NC

Accurate and stable temperature control is necessary for effectively using many thermally sensitive components and sensors, such as semiconductor lasers and optical detectors. An industry has grown up in response to provide thermal-control devices, such as TECs (thermoelectric coolers), temperature sensors, and both monolithic and hybrid application-specific driver ICs, to facilitate the associated designs. This availability eases the implementation of high-performance thermostasis electronics with good dynamic behavior, because it allows you to assemble feedback loops with flexible and sophisticated control characteristics—PID (proportional-integral-differential) feedback loops, for example—with nothing more than appropriate choices of shunt resistance and capacitance. Unfortunately, achieving good static stability is sometimes more difficult because the thermal properties of a system, rather than the electronics, often cause limited temperature-control-loop static stability.

Every thermal-control system incurs nonzero thermal impedances in the heat-transfer paths between the source of heating, cooling, or both. These paths include the thermal load, which is the object of thermostasis; the temperature sensor—the thermistor, for example; and the ambient temperature. If the ratios of these impedances don't balance well, which, unfortunately, is usually the case, then

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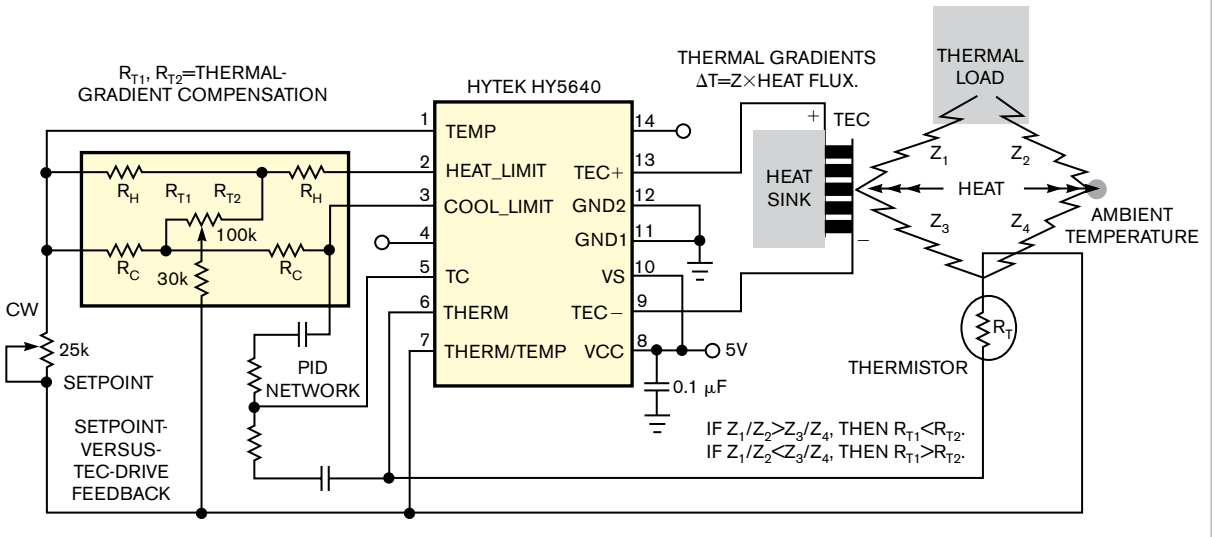

Figure 1 This circuit partially cancels the effects of thermal gradients in the load's thermal impedances. It works by providing an adjustable positive- or negative-feedback path from the TEC-drive level that couples changes in ambient temperature into compensating changes in the thermistor setpoint.

even perfect thermostasis of the sensor doesn't equate to adequate stability of the load's temperature (**Figure 1**).

For example, if Z_1/Z_2 is greater than Z_3/Z_4, where Z is the impedance, then rising ambient temperatures will cause the temperature of the load to rise, whereas falling ambient temperatures will cool the load. By contrast, if Z_1/Z_2 is less than Z_3/Z_4, then rising ambient temperatures will cause the temperature of the load to fall and vice versa (**Figure 2**). Reducing the parasitic impedances with tighter thermal coupling and better insulation can reduce but seldom eliminate the gradient and magnitude of the error.

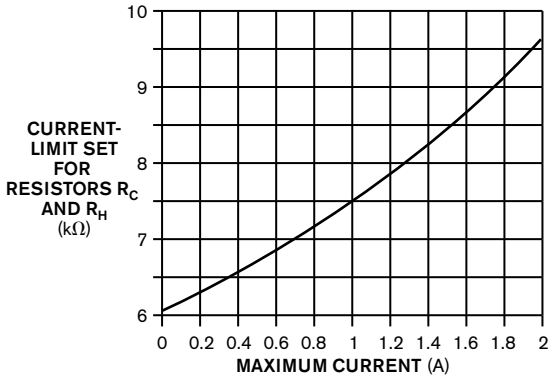

Figure 2 The TEC's maximum-drive heat- and cool-current ratings determine the selection of current-sampling resistors R_C and R_H.

The circuit in **Figure 1** provides a different solution: an electronic workaround to at least partially cancel the effects of thermal gradients in the impedances. It works by providing an adjustable positive- or negative-feedback path from the TEC-drive level that couples changes in ambient temperature and, therefore, in TEC drive into compensating changes in the thermistor-setpoint temperature. The implementation in **Figure 1** uses a popular hybrid TEC controller. Two signal nodes that track TEC drive, COOL_LIMIT and HEAT_LIMIT, are inputs to an adjustable bridge circuit that comprises R_{T1}, R_{T2}, the potentiometer, and associated circuitry. With correct adjustment of R_{T1} and R_{T2}, a test determined that the thermistor setpoint must move either with or in opposition to ambient temperature, so that net stability of the load results. A version of this concept flew as part of two tunable-diode laser spectrometers in the science package of the 1999 Mars Polar Lander (**Reference 1**). EDN

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Programmable current source requires no power supply

John Guy, National Semiconductor, Santa Clara, CA

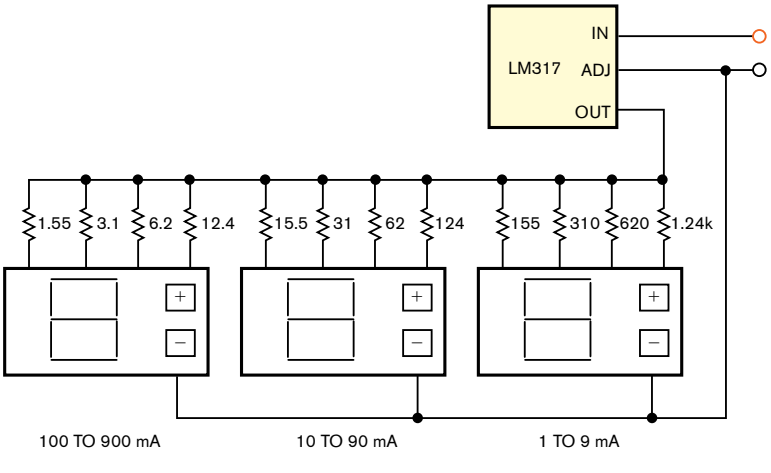

Figure 1 This programmable current source uses BCD switches to set the current limit.

Engineering labs are usually equipped with various power supplies, voltmeters, function generators, and oscilloscopes. One piece of equipment missing from many such labs, however, is a current source. This omission is unfortunate, because a current source is useful for creating I-V (current-versus-voltage) curves, charging and discharging batteries, preloading power supplies, and many other applications.

The circuit in **Figure 1** is an easy-to-build, easy-to-use, low-cost current source. It comprises three sections of BCD (binary-coded-decimal) switches, a three-terminal adjustable regulator, a handful of 1%-tolerant resistors, and a National Semiconductor (www.national.com) LM317 three-terminal adjustable regulator. All newer National Semiconductor regulators are of the low-dropout type, which is unsuitable for this application. The switches short their four outputs to a common terminal based

on the digit setting of the switch.

The circuit operates as follows: Assume that the red terminal in **Figure 1** connects to a 5V power supply and that the black terminal connects to the power supply's ground. Assume that the middle digit (labeled 10 to 90 mA) gets set to two and that the other two digits get set to zero. The BCD switch connects a 62Ω resistor from the LM317's output to adjust pins. The LM317 forces 1.25V across the 62Ω resistor, causing 20 mA to flow from the output pin through the resistor, and to the black terminal of the current source. The circuit maintains this regulation provided that the input voltage remains 3 to 40V.

To construct the current source, you should either use a heat sink for the LM317 or build the circuit into a die-cast aluminum housing, which acts as the heat sink. Isolate the LM317 from the heat sink using a thermally conductive isolation pad and a shoulder washer. You determine the resistors' values by starting with the base-resistance value, 1.24 kΩ. Then, simply use parallel values to determine the successive resistors' values. For example, two 1.24-kΩ resistors in parallel yield 620Ω, four 1.24-kΩ resistors in parallel yield 310Ω, and so on. Using this approach with ¼W resistors ensures that the highest current resistors do not overheat. For example, eight 12.4Ω, ¼W resistors yield 1.55Ω resistance and dissipate only 1W with a peak capability of 2W.

The performance of the circuit is about 2% accurate. You can achieve higher accuracy with hand-selected resistors. The output impedance for lower currents is more than 1 MΩ but drops to approximately 250 kΩ at 200 mA. EDN

Pulse-width modulator has digital control

S Vinay Kumar, Mysore, India

In this Design Idea, the total time period of an output pulse's width is 16 times the pulse width of the input clock. The input clock connects to a binary counter (**Figure 1**). The output of the binary counter then goes to a decoder. The decoder scans the signal such that the first output of the decoder goes to an inverter gate and then to the counter. The output of the counter then goes to one as soon as the signal to the counter goes from zero to one and then from one to zero.

The multiplexer decodes the output pulse width's time to be in the on state. The first output of the demultiplexer sets the output of the counter, and the next outputs clear the output of the counter. The multiplexer, a 14067, selects the clearing signal. Upon the 0th input of the multiplexer, the PWM (pulse-width-modulator) output becomes zero because the setting time and clearing time become nearly zero. The last input of the multiplexer does not connect, so the final input selection becomes independent of the PWM output. The design uses all the intermediate input selections of the multiplexer. EDN

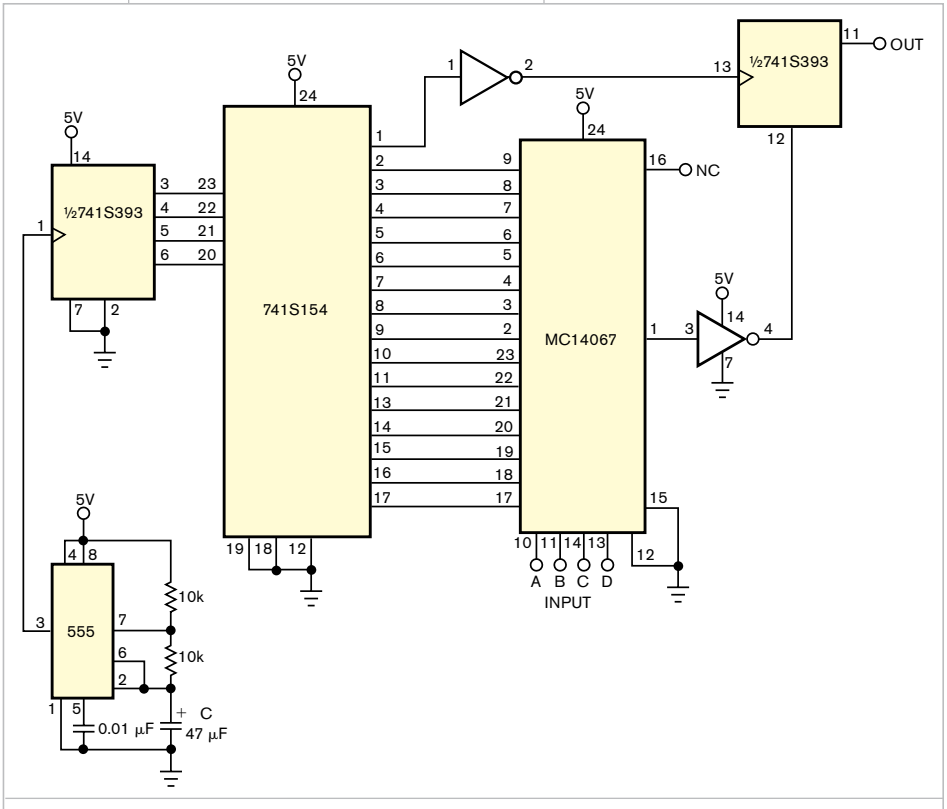

Figure 1 In this digitally controlled pulse-width modulator, the period of the output is 16 times the pulse width of the input clock.

Microcontroller controls analog phase shifter

Nick Ierfino, IGS Technologies, Montreal, PQ, Canada

Phase shifters find use in a variety of circuits, but variation in amplifier and capacitance tolerances usually makes it difficult to control the exact phase shift that precise control circuitry requires. The circuit in **Figure 1** can control the phase shift from input to output by using IC_3, an AD5227 64-step-up/step-down control digital potentiometer, to replace the value for the resistance. The formula of the center frequency of the output is $1/(2\times\pi\times R\times C)$. Different ranges of resistance are available for the AD5227. This example uses a 10-kΩ value. By stepping through the 64 points, the 720-kHz input sine wave rotates several times from 0 to 360°. The AD5227 acts as a potentiometer, in which A and B are the extremes and W is the wiper.

This example uses IC_2, a PIC16F84 microcontroller with a crystal frequency of 20 MHz. This microcontroller has a theoretical potential performance of 5 MIPS and should serve many purposes in PLL (phase-locked-loop) circuitry. You could use any microcontroller or even an FPGA to control the AD5227.EDN

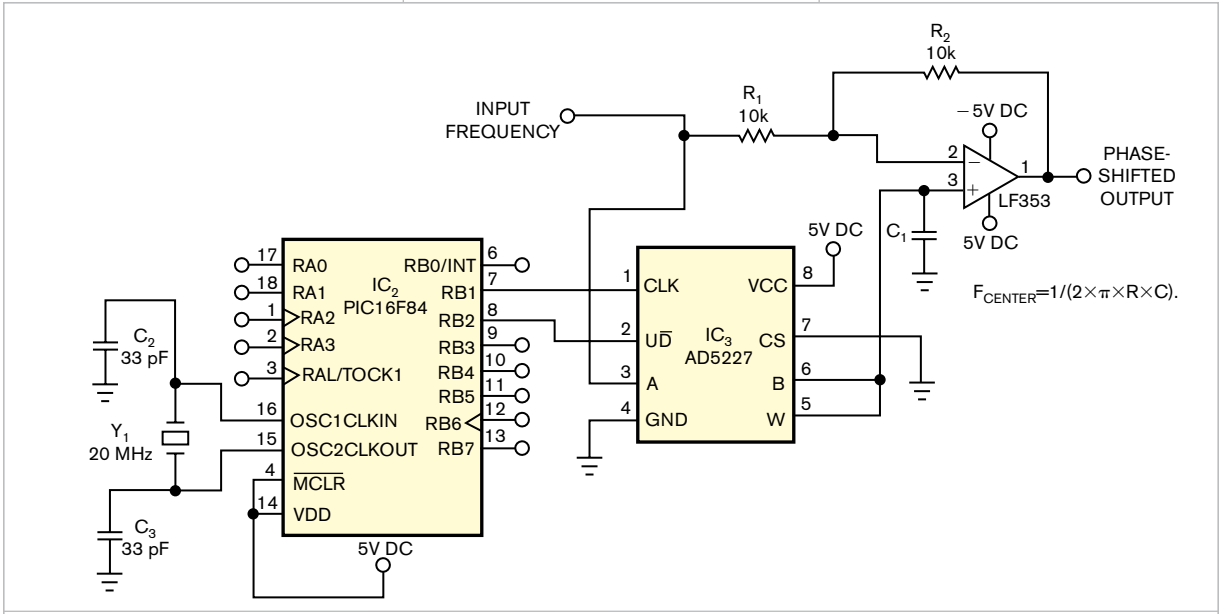

Figure 1 A PIC16F84 sets the resistance of the AD5227 digital potentiometer, precisely controlling the phase shift of the output with respect to the analog input.

Composite instrumentation amplifier challenges single-chip device for bandwidth, offset, and noise

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Although the prevailing number set in electronics is binary, human-machine interaction uses a decimal-number set. For this reason, designs often require the use of amplifiers with gain programmable in steps in the power of 10. Currently, Analog Devices' (www.analog.com)AD8253 monolithic instrumentation amplifier is digitally programmable with voltage gains of one, 10, 100, and 1000 (**Reference 1**). This IC has high bandwidth at lower gains, but you inevitably sacrifice this bandwidth when the amplifier has a gain of 1000. If your application's demands for bandwidth reach the megahertz range at a gain of 1000 and if offset and noise performance prevail over circuit complexity, then a composite amplifier may fill the bill (**Figure 1**).

The composite amplifier is a cascade of three Analog Devices' AD8250 digitally gain-programmable amplifiers IC_1, IC_2, and IC_3 (**Reference 2**). The AD8250 is programmable for voltage gains of one, two, five, and 10. Because the gains of one and 10 are the only

ones of interest in this case, the 2-bit words corresponding to these two values of gain are the zero and three in binary code, and the two logic pins of each of these three ICs connect. The AD8250 has a typical bandwidth of 3.8 MHz and a guaranteed bandwidth of 3 MHz at a gain of 10. The net result is that the bandwidth of the amplifier is 1.9 MHz at a gain of 1000, which is more than six times that of the single-chip AD8253. The low-frequency noise is less than 40% of that of the single-chip device. EDN

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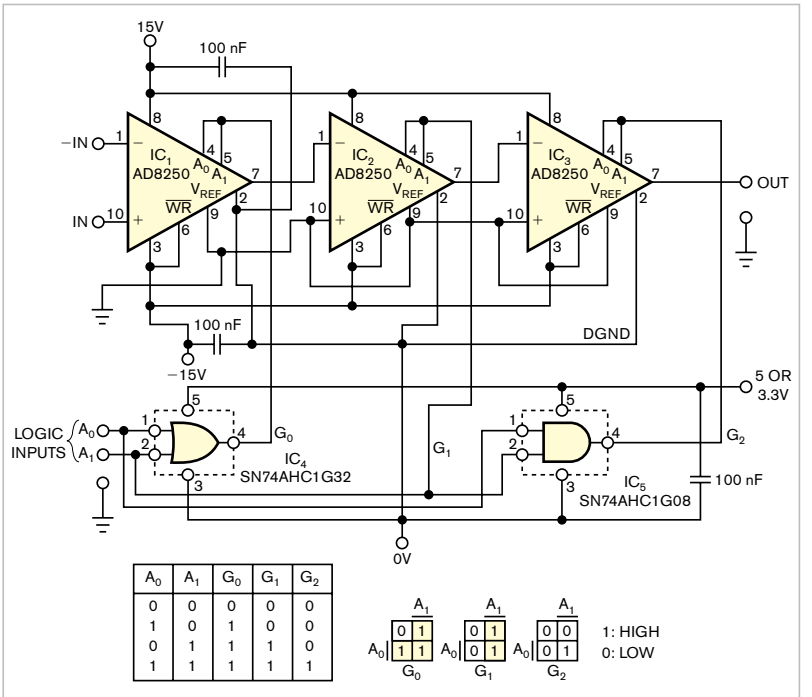
1 "AD8253 10 MHz, 20V/µs, G=1, 10, 100, 1000 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, 2007, www.analog.com/pr/AD8253.

2 "AD8250 10 MHz, 20V/µs, G=1, 2, 5, 10 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, 2007, www.analog.com/pr/AD8250.



A_0	A_1	G_0	G_1	G_2
0	0	0	0	0
1	0	1	0	0
0	1	1	1	0
1	1	1	1	1

Figure 1 Although comprising five IC packages, this digitally gain-programmable instrumentation amplifier reaches a typical bandwidth of 1.9 MHz at a gain of 1000 and thus covers the megahertz range at any of the programmable gains of one, 10, 100, and 1000.

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READERS SOLVE DESIGN PROBLEMS

Simple fixture statically tests programmable-gain amplifiers

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The advent of instrumentation amplifiers with digital gain switching offers obvious advantages, such as board-space saving, higher reliability because of fewer solder joints, and lower total cost. These valuable features stem from the fact that the gain-setting networks are integral parts of the monolithic ICs. This feature makes these IC amplifiers much less sensitive to stray electromagnetic fields because the area of internal resistors is a negligible fraction of the previously used discrete gain-setting resistors. Moreover, the value of the relative permittivity of the plastic package and that of the silicon chip are higher than that of the air. As a consequence, the field strength of the electrical component of any stray field penetrating into the chip is lower than that in the surroundings.

Because the gain-setting circuitry is inaccessible directly, a digitally gain-programmable amplifier is a black box. However, the simple fixture in **Figure 1** can help to evaluate some of the static characteristics of these ICs. The fixture comprises Analog Devices' (www.analog.com) 10V REF01 voltage-reference cell, IC_1, the elderly but still excellent industry standard, and a high-precision fixed resistive divider. These components provide a millivolt-range output voltage.

Multiplying the ratio of the resistive divider by the maximum voltage gain of the tested programmable-gain amplifier should give a value of one. The circuit uses tablet-type film resistors having tolerances of 0.1% maximum, yielding a voltage of 10.02 mV at the output of the divider. The two gain-setting logic inputs of the DUT (device under test), an Analog Devices AD8253, connect to short-stranded conductors, which gold-plated pins terminate. Resistors R_{F1} and R_{F2} force the logic level at gain-programming inputs A_0 and A_1 to be low when you disconnect these pins. To set a high level on either or both pins, insert them into the gold-plated counterparts. Two such counterparts interconnect mechanically and elec-

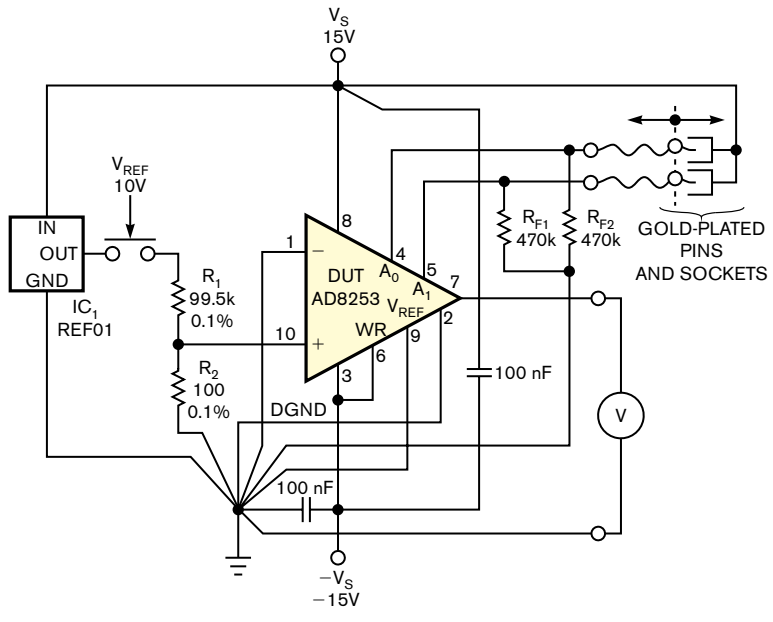

Figure 1 Comprising a handful of components, this circuit allows you to perform your own, independent testing of basic static properties of digitally gain-programmable amplifiers.

DIs Inside

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trically and remain at the V_S potential. The DUT uses all permutations of the binary values at A_0 and A_1 logic (**Reference 1**). The corresponding voltage gains are one, 10, 100, and 1000.

The evaluation procedure involves measuring the output voltage of the DUT with resistor R_1 both connecting to and disconnecting from the output of IC_1. Thus, you obtain an output voltage of the gain times 10.02 mV and 0V for all voltage gains. The 0V output voltage has a nonzero value because of the input-voltage offset; this voltage might seem high at first glance. However, any fraction of a millivolt of the input-voltage offset times a gain of 1000 yields a fraction of a volt at the output.

When you calculate the differences of the 10.02-mV and 0V output voltages for the respective values of gain, you get a pleasant surprise: These values differ from the ideal values of 10.02 mV times the gain by less than 0.05%. Using this test, you can confirm the precision of the laser-trimmed gain settings. The relatively low value of R_2 ensures that the additional input-offset error arising from input bias current of the DUT has a value of less than 3 µV, whereas the typical value is 0.5 µV. Because proper grounding is an absolute necessity when dealing with tens-of-millivolts scale and high-voltage gains, you must connect supply grounds, digital ground, and other rough grounds with the fine signal grounds in one common junction. **Figure 1** illustrates this approach by using unusual slanted lines for grounding leads. EDN

REFERENCE

1 "AD8253 10 MHz, 20V/µs, G=1, 10, 100, 1000 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, www.analog.com/pr/AD8253.

Control system uses LabView and a PC's parallel port

Carlos Alberto Aguilar Sández, Centro de Estudios Superiores del Estado de Sonora, Unidad sede San Luis Rio Colorado, Sonora, Mexico

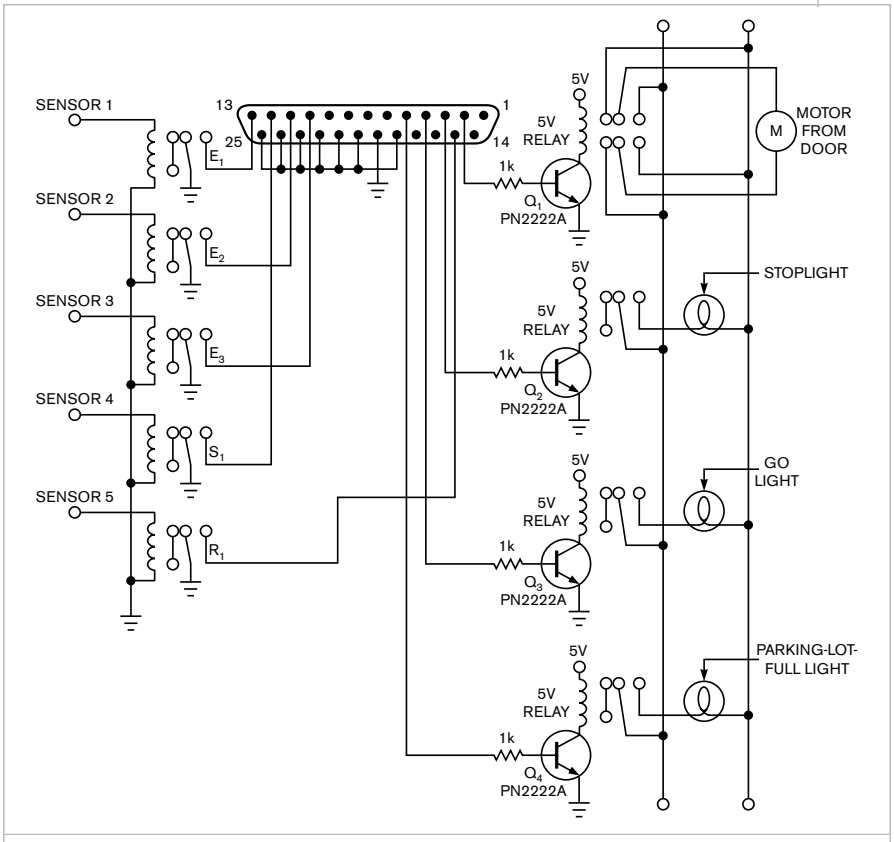

Figure 1 The sensors, indicator lights, and door motor of a parking lot connect through relays to the parallel port of a PC.

The circuit in this Design Idea controls the inbound and outbound traffic of cars in a parking lot. This project uses National Instruments (www.ni.com) LabView as the main programming tool and a PC's parallel port for I/O. Basically, the circuit uses the PC's status port, 379h, as an input for sensors, which a relay isolates to prevent damage on the PC (**Figure 1**). At the data port, 378h, the D0 bit controls a door, D1 is a stop signal, D2 is the go signal, and D3 is an indicator of when the parking lot reaches its limit. All the signals drive PN2222A transistors having an external power supply—in this case, the PC's power supply. In this way, you can use relays as loads and control ac voltage for the traffic lights and door motor. The transistor, which D0 drives, controls a DPDT (double-pole/double-throw) relay to invert the motor's polarity.

Figure 2 shows the LabView diagrammatic program for controlling the parking lot. The VI (virtual instrument) in **Figure 3a** changes the inputs to a low state because all inputs are high by default inside the status register. All inputs have a low state when you do not ac-

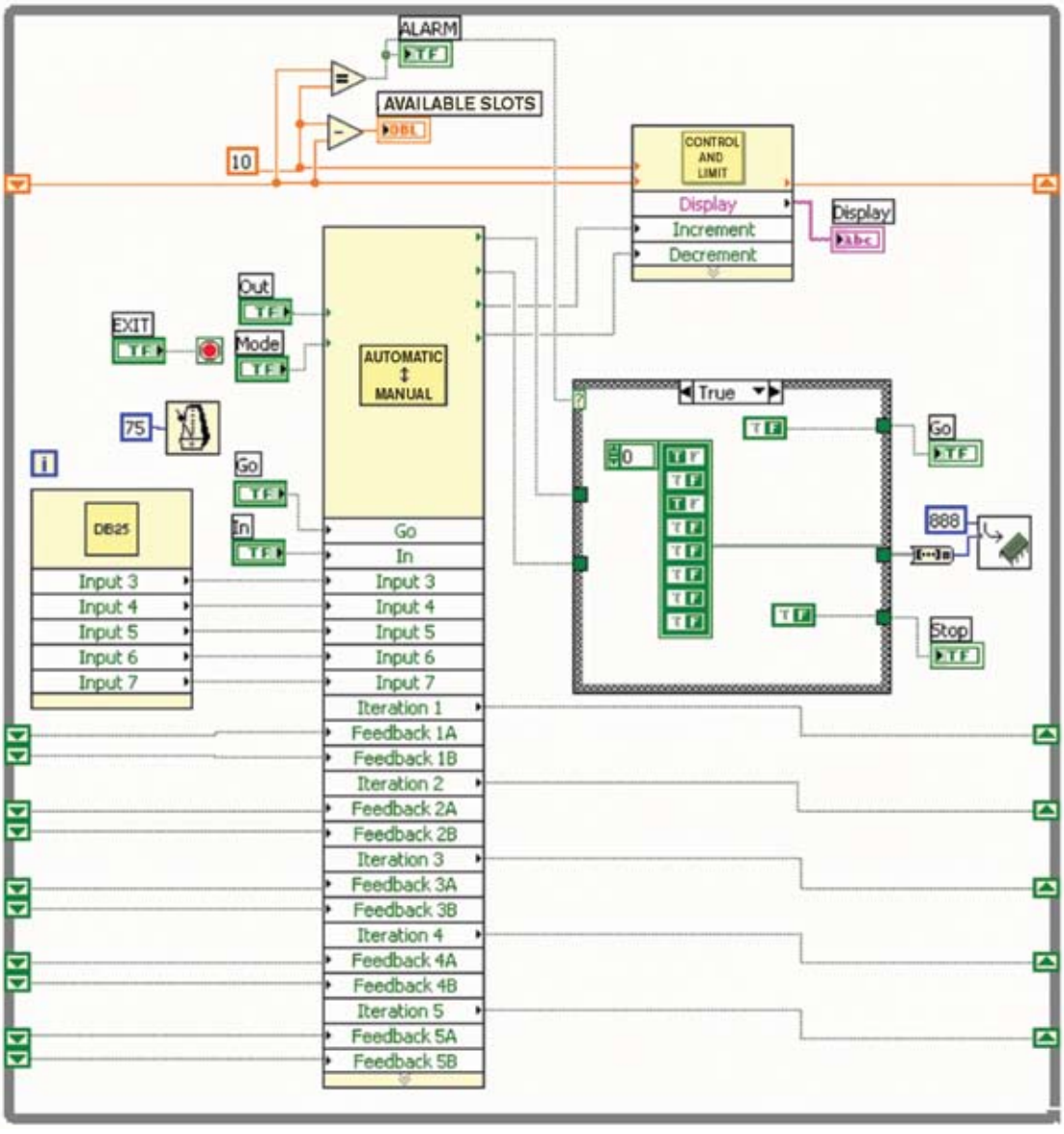

Figure 2 This LabView VI (virtual instrument) controls the operation of a parking lot.

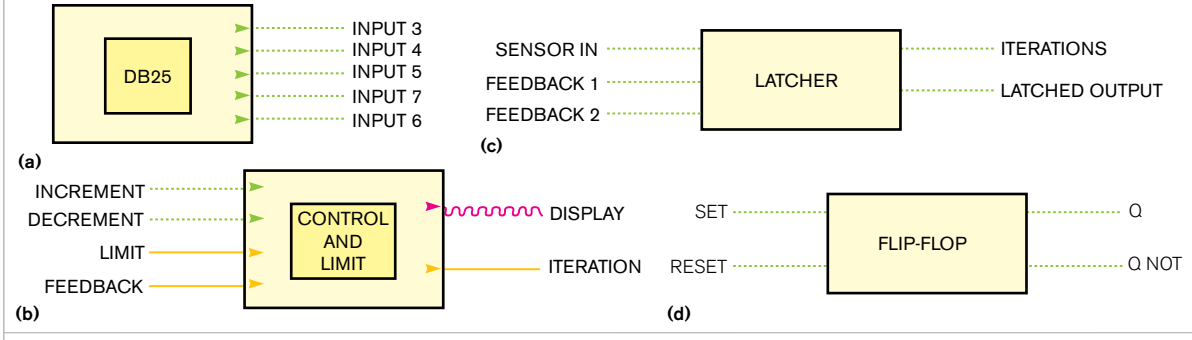

Figure 3 These VIs change the inputs to a low state (a), determine a limit for the number of cars in the parking lot (b), work as a latch-on-release circuit (c), and act as a flip-flop (d).

tivate the sensors. The VI in **Figure 3b** determines a limit for the parking lot, allowing incrementing and decrementing the number of cars parked. This VI also drives a user-oriented display and the shift-register connectors, feedback and iteration, on a "while" loop. The VI in **Figure 3c** works as a latch-on-release circuit; it generates a pulse upon an iteration when the circuit releases the high state on any of the input signals. The VI in **Figure 3d** works as a flip-flop. The VI in **Figure 4** allows switching from automatic to manual mode. Feedback and iteration terminals connect to shift registers, so the latches and the flip-flops inside the VI work correctly. EDN

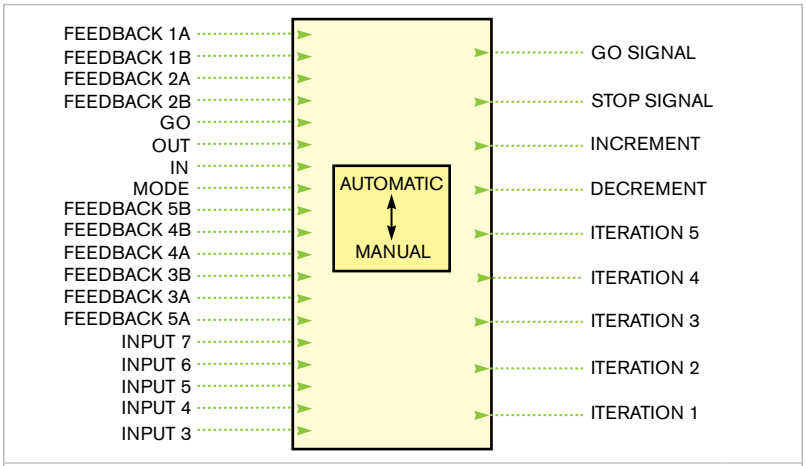

Figure 4 This VI allows switching from automatic to manual mode.

General-purpose components implement USB-based data-acquisition system

V Gopalakrishnan,
Indira Gandhi Centre for Atomic Research, Kalpakkam, India

Figure 1 presents a Design Idea for a USB-based data-acquisition system that uses a serial ADC employing general-purpose components, such as D flip-flops, a binary counter, and a shift register. Using the DLP-USB245M FIFO-to-USB-converter module from DLP Design (www.

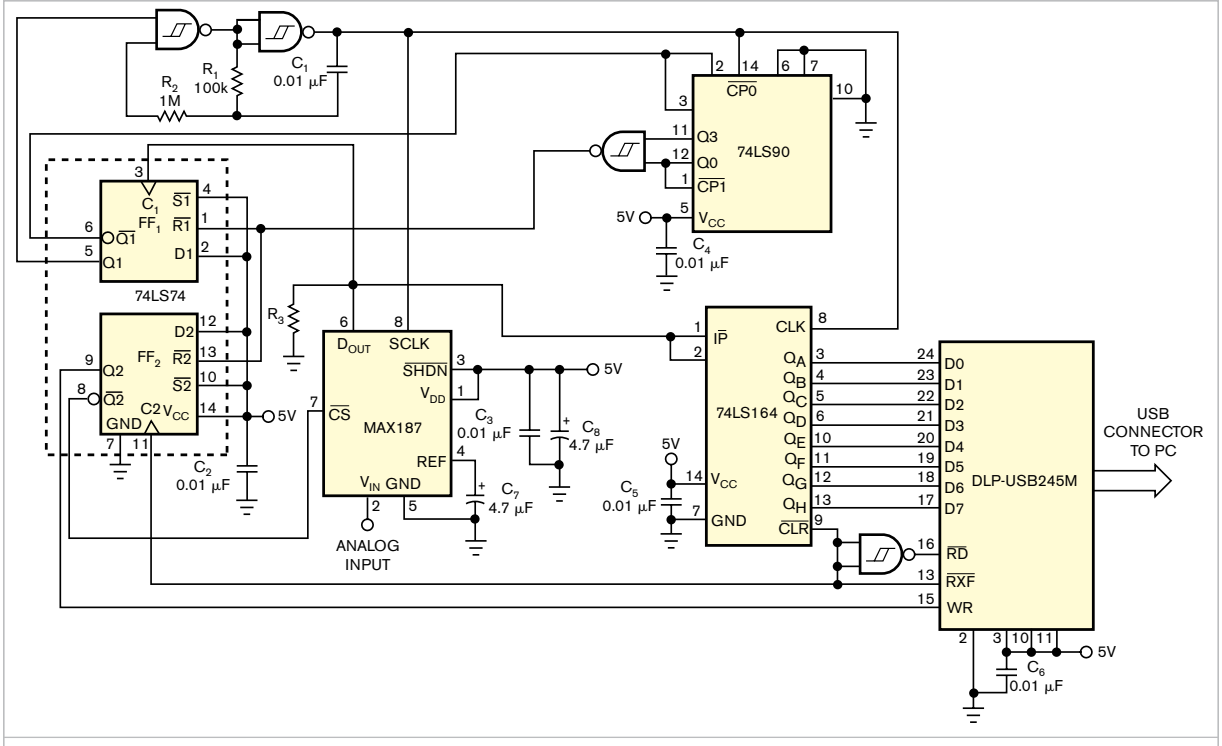

Figure 1 This circuit performs a serial-to-parallel conversion of serial-ADC data and transfers the data to the USB port of a PC.

dlpdesign.com), you can communicate with the peripheral device through the USB port of a host computer. You can write your own program to read and write the data through this module or simply download free test-application software available from DLP's Web site. Additionally, you could download National Instruments' (www.ni.com) LabView serial-read and-write VIs (virtual instruments).

Writing a dummy block of data from the host computer to the buffer of the DLP-USB245M generates a spike at the module's $\overline{RXF}$ pin, which triggers the D flip-flop, FF_2 of the 74LS74. The flip-flop's $\overline{Q2}$ pin initiates the conversion cycle of the MAX187 serial ADC from Maxim (www.maxim-ic.com) by pulling down its chip-select pin. The ADC's end-of-conversion cycle causes a low-to-high transition from its D_{OUT} pin, which triggers the other D flip-flop, FF_1 of the 74LS74, to generate a gating pulse, Q1, for the serial-clock pulses that read the data from the same D_{OUT} pin of the ADC. The 74LS90 binary counter counts the serial-clock pulses. When the count reaches nine, the counter resets the gating pulse for the serial clock and pushes back the chip-select signal to a high level by resetting both FF_1 and FF_2, ending the ADC's acquisition cycle.

YOU CAN WRITE YOUR OWN PROGRAM TO READ AND WRITE THE DATA THROUGH THIS MODULE.

The system acquires the data at the falling edge of the MAX187's SCLK pin and shifts it into the 74LS164 serial-to-parallel shift register at the rising edge of the next SCLK. The MAX187 needs nine serial-clock pulses to shift valid 8-bit data. This circuit uses only 8 bits of the 12-bit ADC. If the circuit requires all 12 bits, then you must connect all NAND gates at the appropriate outputs of the binary counter to generate a reset signal by its 13th clock pulse, and you must make the shift register larger.

The serial data from the ADC converts to parallel data in the serial-to-parallel shift register; a WR (write) signal to the DLP-USB245M then transfers this data to the PC. This action is a complement of the $\overline{CS}$ signal from Q2 of the 74LS74. The DLP-USB245M's $\overline{RXF}$ pin generates a trigger to initiate the conversion cycle and clears the previous data of the shift register. EDN

Small, simple, high-voltage supply features single IC

Alfredo H Saab and Tina Alikahi,
Maxim Integrated Products, Sunnyvale, CA

Sensors, electrostatic traps, and other applications require regulated, high-voltage power supplies that deliver modest amounts of output current. Simplicity, low quiescent current, and compactness are desirable in such supplies. The circuit of **Figure 1** meets these requirements, and its magnetically isolated output allows you to configure a positive, negative, or floating output. A separate winding that generates a feedback voltage proportional to the output voltage, but lower, enables the floating output. This arrangement eliminates the need for high-value resistors in a resistive-feedback divider, which the circuit would otherwise require for direct sampling of the high-voltage output. This low-voltage divider contains resistors with much lower values, which dissipate much less power.

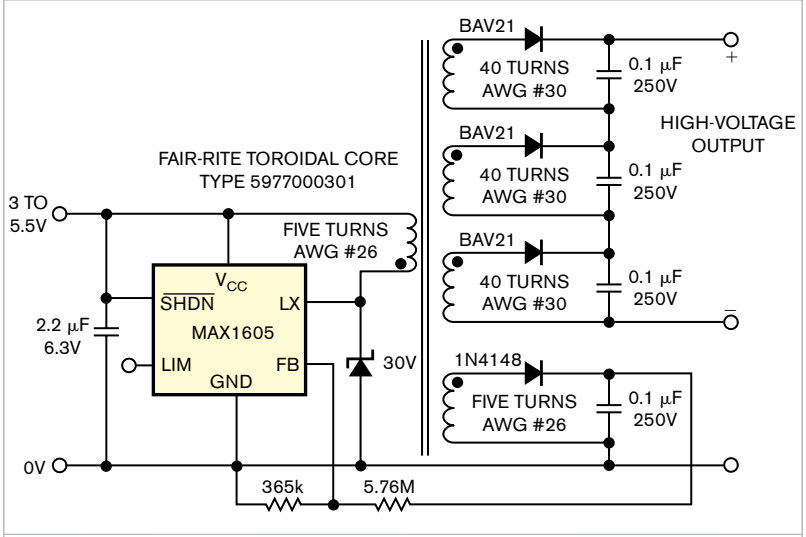

Figure 1 Obtaining feedback from a low-voltage secondary winding, this high-voltage supply generates 500V with low quiescent current.

The MAX1605 IC from Maxim (www.maxim-ic.com) contains the necessary switching regulator, modulator, error amplifier, and power switches (**Reference 1**). It drives the primary of a toroidal transformer that includes a feedback secondary and several output windings. With the component values in the **figure**, the circuit can generate 500V (**figures 2** and **3**). You can vary the output voltage ±30% by adjust-

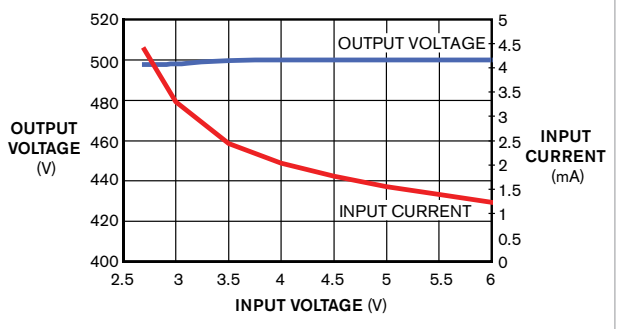

Figure 2 The graph shows output voltage and input current versus input voltage.

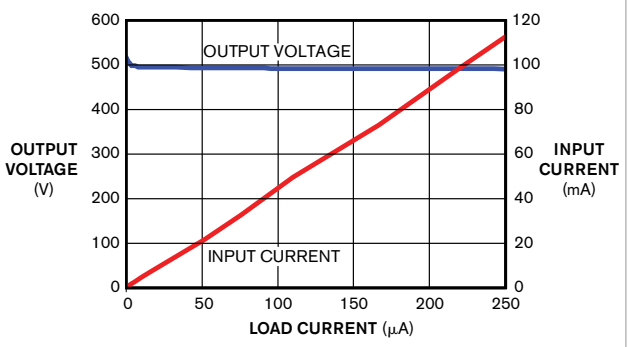

Figure 3 The graph shows output voltage and input current versus load current.

ing the ratio of the resistive-feedback divider. You can also increase or decrease the output voltage in steps by adding or removing the rectifier/capacitor/output-winding modules. The BAV21 is a high-voltage, low-reverse-current, general-purpose diode.

As with all switching converters, EMI (electromagnetic interference) and circuit parasitics can present problems. The circuit needs careful PCB (printed-circuit-board) layout, along with filtering, decoupling, and shielding. The high-voltage output has approximately 1% ripple. You can add an RC or an LC filter in series with the output to achieve lower output ripple. EDN

REFERENCE

1 "30V Internal Switch LCD Bias Supply," MAX1605 data sheet, Maxim, October 2003, http://datasheets.maxim-ic.com/en/ds/MAX1605.pdf.

CMOS DACs act as digitally controlled voltage dividers

John Wynne and Liam Riordan, Analog Devices, Limerick, Ireland

Digital potentiometers, such as Analog Devices' (www.analog.com) AD5160, make excellent digitally controlled voltage dividers in applications in which 8-bit resolution is acceptable. This Design Idea shows how to use a CMOS DAC as a voltage divider in applications requiring higher resolution.

Millions of CMOS R2R (resistor/two-resistor)-ladder DACs have found use in attenuator applications in which an external op amp acting as a current-to-voltage converter forces one current-output terminal to a virtual ground. The reference input to the DAC can be ac or dc as long as the op amp can produce the desired output voltage. A phase inversion is normal between input and output, so the circuit requires dual power supplies.

Figure 1 shows a way to rewire this simple circuit to avoid the phase inversion and to operate with a single supply. In this configuration, the DAC acts as a digitally programmable resistor, and the DAC's code changes the effective resistance between the input voltage and the I_{OUT1} output-current terminal of the DAC. **Figure 2** shows a practical implementation using one-half of an Analog Devices AD5415 dual 12-bit current-output DAC operating as a voltage divider. This **figure** omits the DAC's control lines for clarity. Op amp A_1 forces the voltage on the I_{OUT2A} output-current terminal to follow the voltage on the I_{OUT1A} output-current terminal. This approach prevents a voltage differential from developing between these two bus lines, which would result in the application of different gate-source voltages across the internal DAC switches and a deterioration in the DAC linearity.

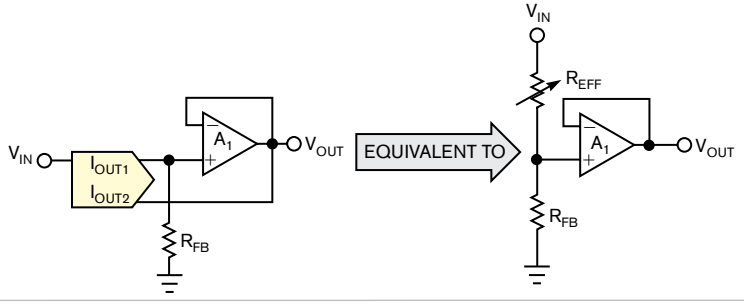

Figure 1 This simple circuit avoids a phase inversion and operates with a single supply. In this configuration, the DAC acts as a digitally programmable resistor.

Wire the split-feedback resistors, R_{FB} and R_1, to produce a composite-feedback resistor equal in value to the DAC's ladder impedance, R. For this arrangement the circuit-transfer function is $V_{OUT}/V_{IN}=(R)/(R_{EFF}+R)$, where R_{EFF} is the effective DAC resistance that is under digital control. Its value is $R(2^n)/N$, where n is the resolution of the DAC and N is the binary equivalent of the digital-input code. Substituting the second **equation** into the first and assuming zero DAC gain error, the circuit-transfer function for a 12-bit DAC reduces to $V_{OUT}/V_{IN}=1/(1+4096/N)$. With all switches off, the effective impedance between the reference voltage and the I_{OUT1A} terminal is infinite, so the output voltage starts at 0V when you load zeros into the DAC. The output voltage increases linearly with increasing code, ideally to approximately half the input with all ones applied to the DAC.

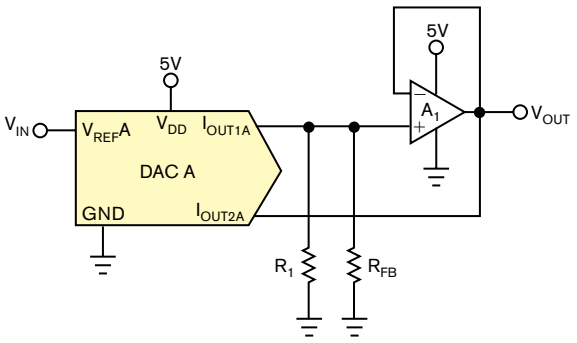

Figure 2 This practical implementation of the circuit in Figure 1 uses one-half of a 12-bit-current-output AD5415 dual DAC that operates as a voltage divider.

The threshold voltage of the DAC's internal N-channel-CMOS switches limits the maximum value of the output voltage, so not all configurations can achieve the full code range. The switch-gate voltage remains at the V_{DD} voltage, and the switch-source voltage rises with the voltage on I_{OUT1A}. As this voltage increases, the on-resistance of the switches becomes large and indeterminate, leading to a flattening of the output voltage and the cessation of the circuit as a predictable voltage divider. For proper operation, the V_{DD} voltage must be a few volts higher than the maximum output voltage—that is, half the input voltage. Otherwise, the input voltage must be less than two times the V_{DD} voltage minus 3V. With a V_{DD} voltage of 5V, the AD5415 operates linearly to approximately a 3.33V output but then flattens. If a wider output-voltage range is necessary, you could use Analog Devices' AD7541A, which uses a 15V power supply, in place of the AD5415. This substitution extends the usable output-signal range to approximately 7V. EDN

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Low-cost circuit incorporates mixing and amplifying functions

Guus Colman, Guy Torfs, Johan Bauwelinck, and Jan Vandewege,
INTEC/IMEC, Ghent University, Ghent, Belgium

In many applications, the frequency-conversion steps comprise a buffer, preferably with some extra voltage gain; a mixer; and some filtering. Instead of including an amplifier in front of the mixer, you can easily integrate the mixer function with the amplifier. A low-cost implementation uses an amplifier with a power-down-disable feature. When a square-wave local oscillator drives the disable pin, a square wave at the oscillator's frequency multiplies the input signal, and frequency conversion takes place.

The circuit in **Figure 1** uses an Analog Devices (www.analog.com) low-cost, 300-MHz, rail-to-rail AD8063 amplifier. The test circuit comprises a noninverting-op-amp circuit, which drives a load of 4 kΩ. The two resistors in the feedback loop regulate the voltage-conversion gain. In the test circuit, the voltage gain is 20 dB. However, you must consider the switching loss, which is about 10 dB when using an ideal switch and a 50%-duty-cycle clock. This scenario results in a 10-dB voltage-conversion gain.

Because the switching interrupts the power-supply current, the device's turn-on and turn-off times have a nonnegligible influence on conversion gain and nonlinearities. The AD8063's turn-on time, at 40 nsec, is less than the turn-off time of 300 nsec. In these cases, more signal power passes to the output, which results in an increase in voltage-conversion gain. **Figure 2** shows the voltage-conversion gain of the test circuit when downconverting an input signal to 12 kHz with a local-oscillator duty cycle of 50%. You can easily adjust this conversion gain by changing the two resistors in the feedback loop.

Another aspect of a mixer's ac performance is distortion. The test circuit maintains a second-order harmonic distortion of 35 dB and a third-order harmonic distortion of 43 dB when mixing a 5-MHz signal to a 12-kHz, 1V-p-p output signal. The circuit can downconvert two sine waves of identical power at 5 and 5.002 MHz to 12 and 14 kHz, respectively, with an intermodulation distortion of 47 dB. EDN

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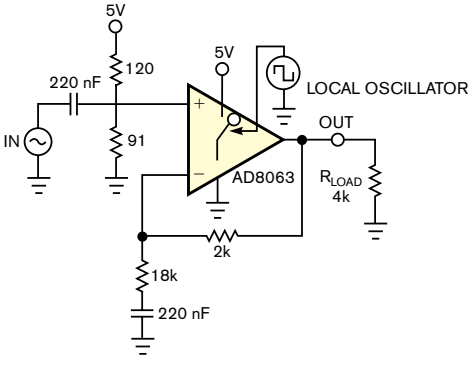

Figure 1 This circuit integrates the mixer function with a noninverting amplifier. The two resistors in the feedback loop set the voltage-conversion gain.

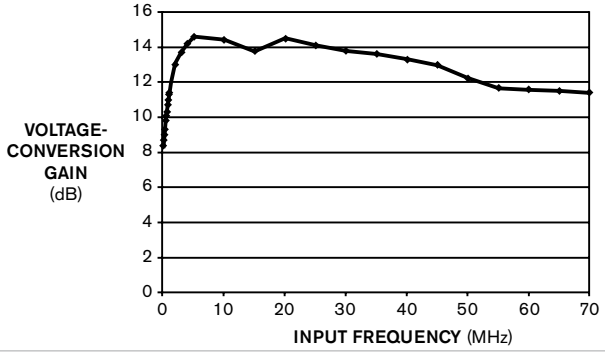

Figure 2 This graph shows the voltage-conversion gain of the test circuit when downconverting an input signal to 12 kHz with a local-oscillator duty cycle of 50%. You can easily adjust this conversion gain by changing the two resistors in the feedback loop.

Simple blown-fuse indicator sounds an alarm

Vladimir Oleynik, Moscow, Russia

Safety fuses or fusible links see wide use in modern electronic equipment to protect the load and the power supply—especially batteries—against short circuits and excessive load current. Fuses are inexpensive and simple, and a wide range of parts is available. However, you must replace them when they blow, and, when they do, you need an indicating circuit that warns you about its failure, especially when the fuse body is ceramic or sand-filled for improved protection against arcing.

The circuit in **Figure 1** signals that a fuse has blown. Input voltage ranges from 4 to 30V dc. The input range of the 78L05 voltage regulator determines the high limit; the lower one is less than the input range of the voltage regulator, but 4V dc is sufficient for the indicator to operate.

When fuse F_1 is in good order, diode D_1 is forward-biased, but its forward voltage is insufficient to bias forward-flashing diode D_2 and the Q_1's base-emitter junction. The self-driven HCM1206X buzzer is off, and the flashing diode does not flash. So, the alarm circuit is in standby mode. When F_1 blows, it no longer bridges the base-emitter-flashing-LED network. The 1-kΩ resistor forward biases D_2 and Q_1's base-emitter junction, forcing the buzzer to sound at a low frequency equal to the flashing frequency of D_2. During circuit operation, the 0.1-µF capacitor eliminates the buzzer's "tinkling" when the flashing LED is in the off state. EDN

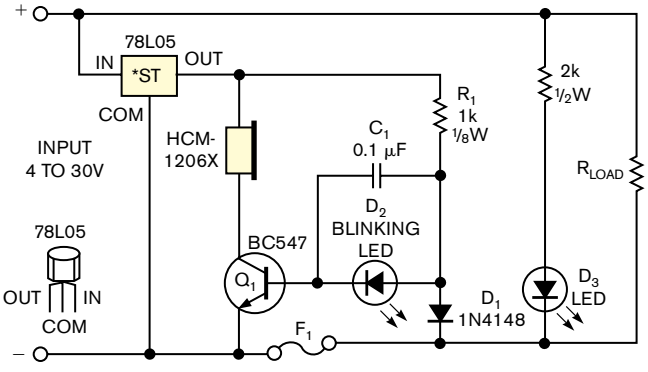

Figure 1 When fuse F_1 blows, the transistor biases on, sounding the buzzer and powering D_2.

Tester cycles system-power supplies

Goh Ban Hok, Infineon Technologies Asia Pacific Ltd, Singapore

Power-cycle testing is important because it tests the user environment. A poorly designed system board or chip can cause the power-cycle testing to fail, however. What's more, the power-cycle-test setup for system-board bench testing could require the use of a bulky and expensive commercial power supply. The situation gets worse when you need to simultaneously test several system boards.

This Design Idea describes a simple and inexpensive power-cycle circuit using just a few components (**Figure 1**). The power-supply input voltage is a dc supply from an inexpensive switching-power-supply adapter. This type of power adapter normally provides power for the system board. The circuit uses a 12V supply. You plug the power jack of the power unit into power socket J_1. The output voltage of this circuit from socket J_2 then connects to the system board to perform the power cycling. The 12V supply passes through resistors R_5 and R_6, which limit the current flowing through relay switches S_1 and S_2.

During start-up, the contact of relay S_2 is normally closed, allowing the 12V supply coming from R_6 to pass to resistors R_1 and R_2 and charge up capacitor C_1. Resistor R_8 in series with transistor Q_2 increases the charging and discharging duration of capacitor C_1. Transistor Q_2 turns on once capacitor C_1 charges toward 2V. This action impresses approximately 0.7V across the base-emitter voltage of transistor Q_2, which turns on Q_2. When transistor Q_2 turns on, it provides a low-resistance path for the coil of S_2 and thus energizes the relay, causing S_2's contact, 2_B, to close.

THIS DESIGN IDEA DESCRIBES A SIMPLE AND INEXPENSIVE POWER-CYCLE CIRCUIT USING JUST A FEW COMPONENTS.

When this scenario occurs, the 12V power supply switches its path to contact 2_B and enables the optocoupler's diode to conduct, turning on its internal transistor. The optocoupler then drives transistor Q_1. When Q_1 turns on, it provides a path for the coil of S_1, which energizes and thus connects the 12V supply to the output voltage. The circuit connects the output voltage to the power supply of the system board, thus powering up the board.

The system board remains powered up for approximately 45 sec. During the on time, capacitor C_1 discharges slowly through R_2, Q_2, and R_8. C_1 turns off transistor Q_2 once the voltage across the base of the transistor is below the transistor's turn-on voltage. Then, contact 2_B connects to contact 2_A, and the cycle repeats.

The off time for this circuit should be approximately 17 sec. Freewheeling diodes D_1 and D_2 reduce the large transient voltages that occur when the currents through the relay coils change quickly. EDN

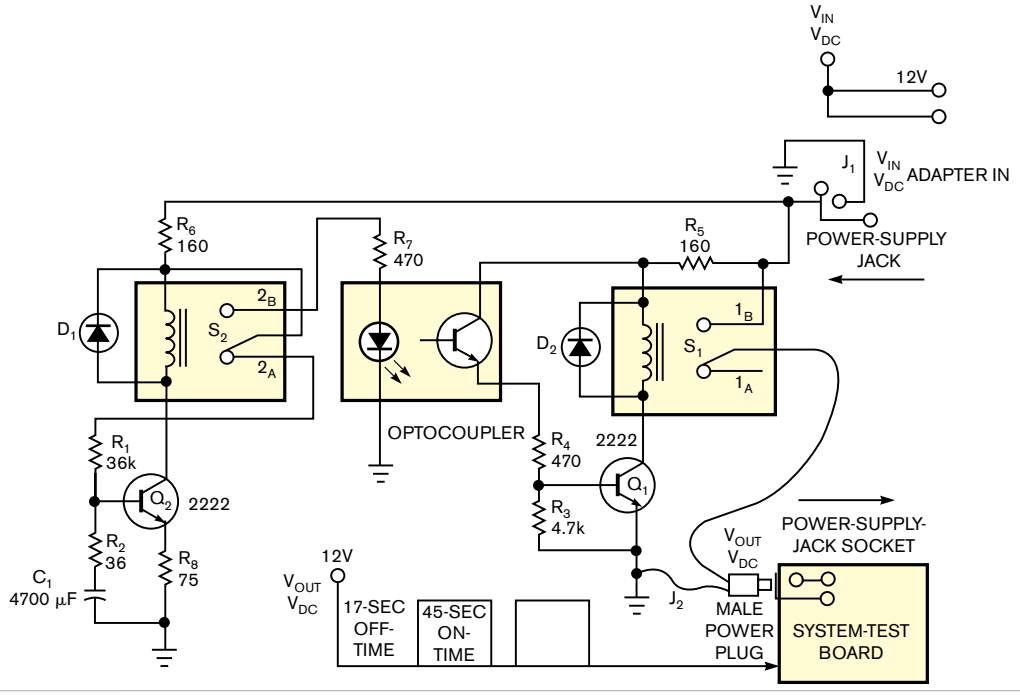

Figure 1 This simple and inexpensive power-cycle circuit uses just a few components.

Touch-activated timer switch extends battery life

Israel Schleicher, Prescott Valley, AZ

A certain type of cordless optical computer mouse operates on two AA alkaline cells. It has no power on/off switch. When not in use, it automatically reduces power consumption by switching its light source on and off at a low duty cycle. Nevertheless, this function unnecessarily drains the battery, and it is annoying to often find the device inoperable. The solution to the problem is to add a battery switch that automatically disconnects the battery after a preset time. This approach requires no disassembly or other kind of tampering. This Design Idea describes two distinct implementations of a touch-activated timer switch that you can add to many battery-operated gadgets that you might inadvertently leave on.

The circuit in **Figure 1** illustrates an analog implementation of the switch. **Figures 2** and **3** show digital implementations. The idea is to insert a 30-mil-wide strip of dual-sided PCB (printed-circuit board) between the negative pole of the battery and the spring contact of the battery holder (Item A in the **figures**). Q_3 is a low-threshold MOS transistor that connects between the two sides of the strip and serves as the switching element (**Figure 1**). C_1 is a 0603 X7R ceramic-chip capacitor, and R_1 is a 0603 chip resistor. You mount Q_3 and all associated components near the upper edge of Item A. You insert a narrow strip of thin brass, Item B, in series with the positive pole of the second cell. You connect it to the circuit with a piece of thin, flexible wire. Touch contacts C and D comprise short strips of self-adhesive copper tape that you attach outside the battery compartment. Thin and flexible wires connect C and D to the circuit.

THIS DESIGN IDEA DESCRIBES A TOUCH-ACTIVATED TIMER SWITCH THAT YOU CAN ADD TO MANY BATTERY-OPERATED GADGETS.

Q_1, Q_2, and C_1 form a monostable flip-flop. When the switch is off, C_1

does not charge, and both Q_1 and Q_2 are off. When you momentarily touch both C and D with bare fingers, current through your hand charges C_1 to the threshold level of Q_2. Both Q_2 and Q_1 turn on, discharging C_1 through Q_1 and your conductive fingers. The voltage level at the gate of Q_2 is then close to the battery voltage. After you remove your fingers, the leakage through the internal gate protection of Q_2—the zener diode in the **figures**—causes the voltage at the gate of Q_2 to slowly drift lower until it reaches the threshold level of approximately 1.3V. Q_2 exits conduction and, with Q_1, causes a regenerative action to quickly turn off Q_3.

The switch remains off until you again touch C and D. Item E is an optional contact similar to C and D. If you touch E and D, the switch turns off. Using a value of 0.01 µF for C_1, you obtain a delay of approximately one hour. Because the gate leakage is on the order of a few picoamperes, you must clean the circuit with a flux solvent and then coat it with a drop of wax or epoxy resin.

In some cases, you might want to be able to adjust the timing of the switch. The circuit in **Figure 2** provides that option. It uses a tiny microcontroller in an SOT-23 package. **Listing 1**, which is available in the Web version of this Design Idea at www.edn.com/080710di1, contains the touch-activated timer switch. Items A, B, C, and D are the same as those in **Figure 1**. When the switch is off, the PIC10F200T microcontroller is in sleep mode and consumes practically no power. When you simultaneously touch contacts C and D, the level at Pin 1 of IC_1 goes high, and the microcontroller starts to tally the time that Pin 1 remains high. After 0.5 sec, the buzzer sounds a short beep. The buzzer then sounds two, three, and four fast beeps in 0.5-sec intervals. By immediately releasing contacts C and D after hearing any number of beeps, you can set the switch for 30 seconds, 30 minutes, four hours, and eight hours of operation, respectively. The choices of operating times are arbitrary; you can modify the code in **Listing 1** to whatever fits your application. Jump-

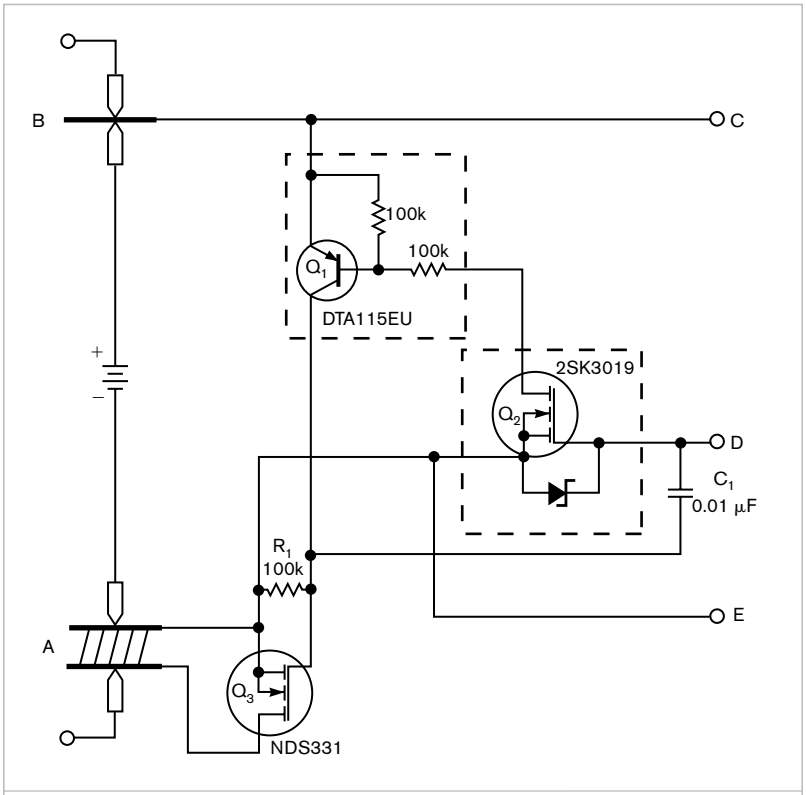

Figure 1 In parallel with the cells of a battery-powered device, this analog circuit disconnects the battery after a delay. Touching contacts C and D with a finger turns on the switch, connecting the cells to the load. The components fit inside the battery compartment.

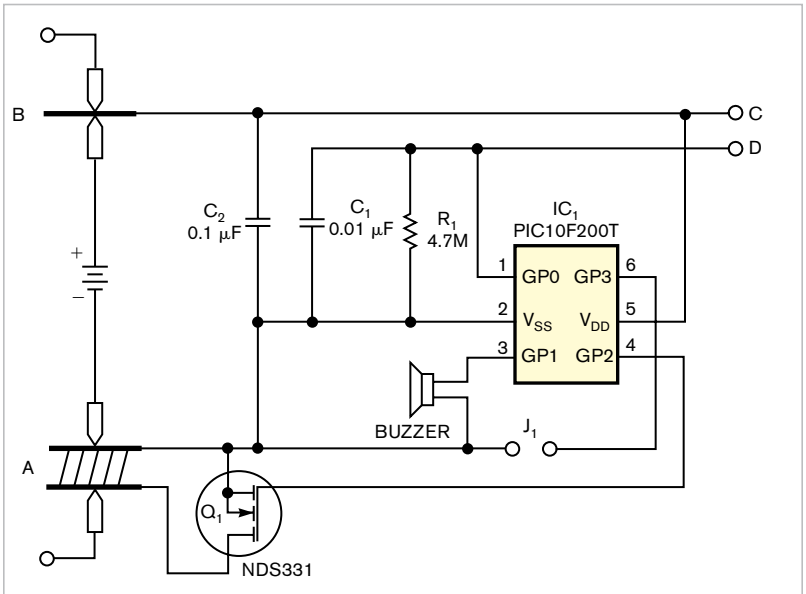

Figure 2 This digital implementation of the battery-disconnect switch uses a PIC10F200T microcontroller to control the disconnect switch.

er switch J_1 is optional. If you leave it open, touching C and D turns it off. Short-circuiting J_1 disables this option, and the switch will turn off only at the end of the programmed time. As is the case with the analog implementation, you mount all components except the buzzer at the edge of Item A. The buzzer is a small piezoelectric element with a resonant frequency of 4 kHz and can easily fit inside the battery compartment.

In some cases, you may not have access to the negative contact of the battery holder. The circuit in **Figure 3** addresses this situation. It is essentially the same as the circuit in **Figure 2**, except that you place Item A in series with the positive pole and attach B to the negative pole of the battery. A P-channel MOS transistor acts as a switch, and you modify the microcontroller's program to provide a low level to drive Q_1. A comment in **Listing 1** indicates the proper line of code for the options in either **Figure 2** or **Figure 3**.EDN

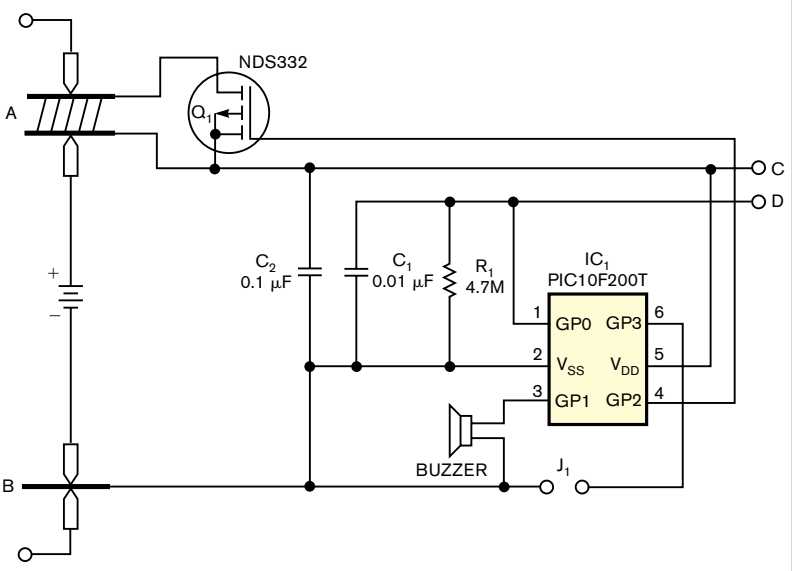

Figure 3 This circuit addresses the problem of a lack of access to the negative contact of the battery holder. It is essentially the same as the circuit in Figure 2, except that you place Item A in series with the positive pole and attach B to the negative pole of the battery.

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READERS SOLVE DESIGN PROBLEMS

High-voltage, high-frequency amplifier drives piezoelectric PVDF transducer

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Universidad Católica Nuestra Señora de la Asunción,
Itapúa Antequera, Paraguay

Piezoelectric transducers find use in NDE (nondestructive-evaluation) applications. The PVDF (polyvinylidene-fluoride) transducer has many advantages, including a wide bandwidth and high sensitivity. These transducers require high-voltage and wide-bandwidth amplifiers. The basis of the circuit in **Figure 1** is an earlier Design Idea (**Reference 1**). The operation of the circuits is basically the same, but this one can drive a 2.3-nF capacitive load at frequencies as high as 500 kHz.

In this circuit, an LM7171 op amp from National Semiconductor (www.national.com) replaces the LF411, also from National Semiconductor, of the earlier design. The LM7171 op amp has a unity-gain bandwidth of 200 MHz. To further improve the bandwidth, this design's mirror circuit uses lower-value resistors to increase the current in the transistors, thus increasing the bias current and the power dissipation of Q_3 and Q_4. To improve thermal stability, this design adds resistors R_{16} and R_{17}, and, to increase the current to drive the transducer's capacitive load, this design adds a current driver to the circuit's output. V_{CC} and V_{EE} are 15 and −15V, respectively, and V_{H+} and V_{H-} are a maximum of 150 and −150V, respectively. EDN

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Duggal, Bipin, "High-voltage amplifier drives piezo tubes," *EDN*, Dec 7, 2004, pg 100, www.edn.com/article/CA484492.

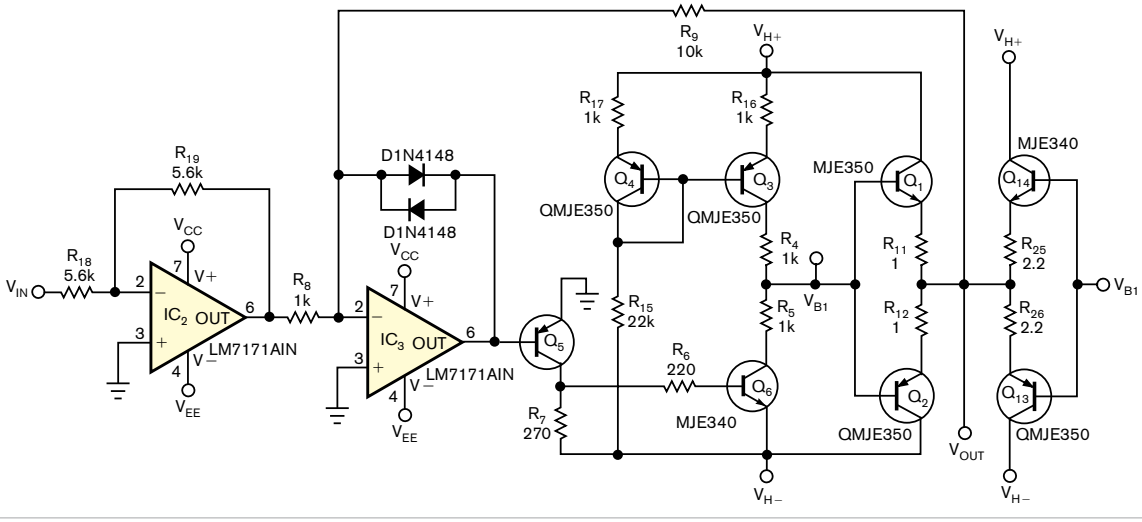

Figure 1 This high-frequency, high-voltage amplifier can drive the capacitive load from a PVDF (polyvinylidene-fluoride) piezoelectric transducer.

Microcontroller detects pulses

Abel Raynus, Armatron International, Malden, MA

While recently designing an automatic test station employing a microcontroller, I faced a nonstandard task: Detect the presence or the absence of output pulses in the DUT (device under test). You might think this task is easy to accomplish by connecting an LED to the DUT output. The blinking LED provides evidence of the pulse's presence. That approach would work if that test were the only one you needed to perform. In this station, however, the pulse test is just one of more than a dozen tests and measurements. The test station should display the final result—pass or fail—only after completing all the tests. So, it should represent the result of each test in binary format—that is, yes for pass or no for fail. This Design Idea describes a simple way of solving this problem.

The pulses for detection enter the $\overline{IRQ}$ (interrupt-request) pin of the Freescale (www.freescale.com) MC68HRC908JK1 microcontroller (**Figure 1**). Each pulse period is 500 msec, causing an external interrupt. At least three interrupts should occur within 2 seconds. The program waits for 2 seconds, and, if no external interrupts occur during that time, it declares that the pulse test has failed. The red LED on the PB1 pin then switches on, and the test stops. Otherwise, after three interrupts, the program starts the next test. To evaluate the pulse test separately from the rest of the tests, this demo program ends in an indefinite loop instead of starting the next test. When the green LED on the PB0 pin lights up, it indicates that the pulse test has successfully completed. The LEDs work with built-in current-limiting resistors, such as W934GD5V and W934ID5V devices from Kingbright (www.kingbright.com).

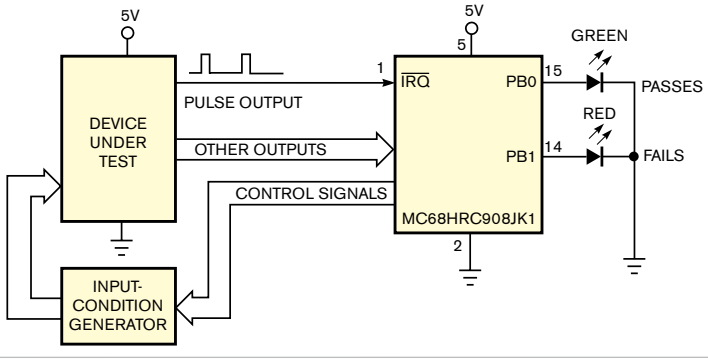

Figure 1 This 8-bit, low-end microcontroller detects pulses from LEDs, yielding a simple tester.

This design uses the low-end, 8-bit MC68HRC908JK1 microcontroller because of its low cost and ability to have 10 8-bit ADC channels. You can find **Listing 1**, the firmware-assembly code for the device, at the Web version of this Design Idea at www.edn.com/080724di1. You calculate the time delay for the oscillation frequency at approximately 4 MHz, which a 20-kΩ resistor and a 10-pF capacitor determine. This approach is applicable to any type of microcontroller because it uses standard assembly instructions. You need to recalculate the time delay only in case of different oscillation frequencies. EDN

Sample-and-hold amplifier holds the difference of two inputs

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

You can fulfill a requirement for sampling the difference of two signals in two classic ways. You can subtract the two input signals with an instrumentation amplifier whose output connects to an input of a classic sample-and-hold amplifier. Despite the positive feature of needing no external resistors for a gain-of-one differencing instrumentation amplifier, this approach suffers from high relative output distortion when the inputs are of the same polarity and close in magnitude. In such a case, the difference of two input signals is close to 0V, and the amplifier is therefore more vulnerable to residual dynamic imperfections of the sample-and-hold amp. The other approach is to separately sample the two input voltages in two sample-and-hold amps and subtract the outputs of these amps in an instrumentation amp. Here, the relative error of output signal with similar input waveforms is lower than in the first approach.

If you like all-in-one solutions, you can use the circuit configuration in **Figure 1**. This circuit simultaneously tracks both input voltages, V_{INA} and V_{INB}, at an active-high level of the internal logic-control signal, which enables the A_1, B_1, and A_2 voltage followers. V_{INA} thus appears on capacitor C_2, which is ground-referenced. Capacitor C_1, which is temporarily grounded at its upper node, Pin 9 of IC_1, tracks the V_{INB} voltage. After a settling interval when all of the internal logic-control signals go inactive low, the Q_{SB} logic-control signal goes high. The voltage of $V_{C2}(TS)=V_{INA}(TS)$ shifts the potential at the lower node of capacitor C_1 because of the enabled B_3 follower. Upon the sample command, Q_S is high, and the upper node of C_1 is grounded within the tracking interval. Storage capacitor C_3 therefore charges through the B_2 follower to a voltage of $V_{C2}(TS)-V_{C1}(TS)=V_{INA}(TS)-V_{INB}(TS)$. The A_3 follower serves as an impedance converter.

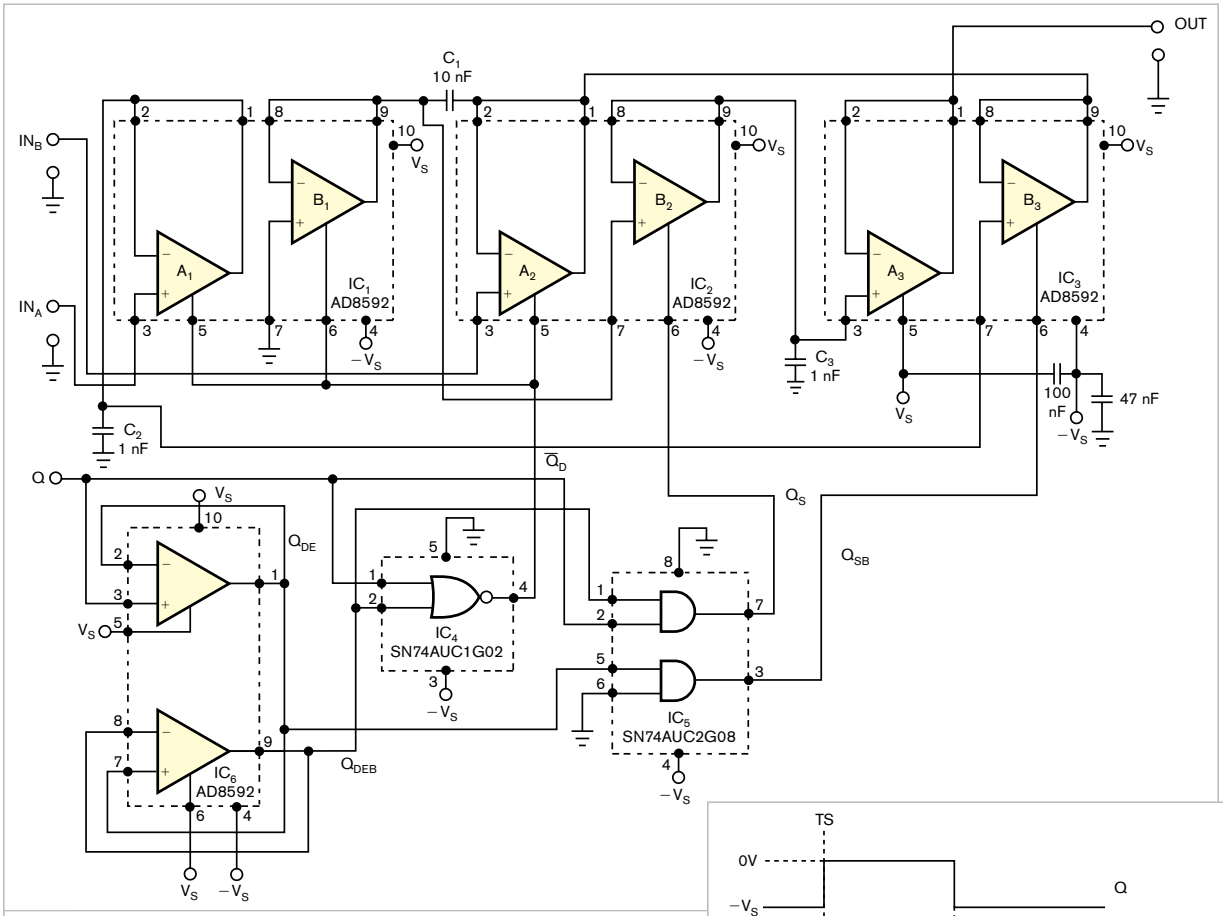

Figure 1 The basis for the operation of this circuit is the simultaneous tracking of the V_{INA} and V_{INB} input voltages on capacitors C_1 and C_2 and a stacking of these capacitors within the sample interval on capacitor C_3.

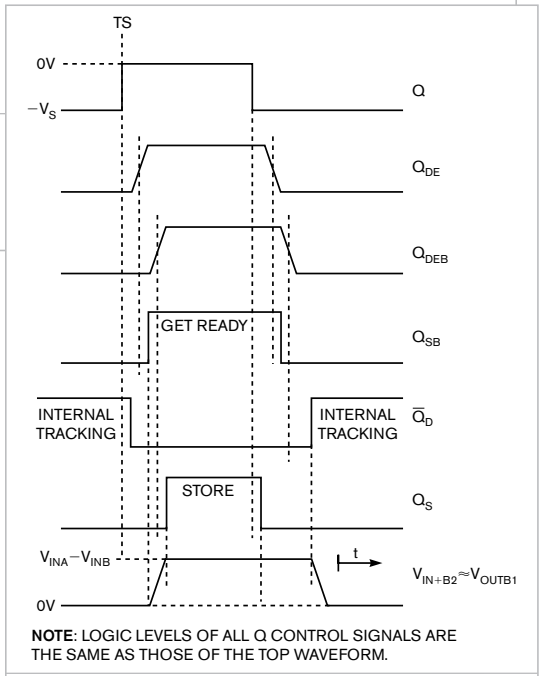

Figure 2 The bottom waveform shows that, at the upper node of capacitor C_1, 0V appears within the tracking interval, and it rises to the value of a difference between both input voltages within the get-ready interval when Q_{SB} is high. The difference of input voltages of $V_{INA}(TS)-V_{INB}(TS)$ resides within the store interval when Q_S is high.

The voltage gains of both the A and the B channels are slightly lower than ideal. This slight gain decrease has approximately the same value for both channels: $\delta_{GAINA}=\delta_{GAINB}\sim(C_{OUTB1}/C_1)$. The equality of gain decrements on both channels stems from the fact that the upper node of the storage capacitor, C_1, connects at the instant that Q_{SB} goes high to the output capacitor, C_{OUTB1}, of the disabled follower, B_1. Follower B_1 always discharges to 0V within the tracking interval without regard to the voltages at the A and B inputs. For Analog Devices' (www.analog.com) AD8592 op amps, the output capacitance, C_{OUT}, in the disabled state is approximately 26.2 pF.

Note, however, that if V_{INA} and V_{INB} are of opposite polarity and of equal magnitude, almost reaching the value of $V_S/2$, the output voltage approaches either the positive- or the negative-supply rail. In this case, the relative output error is about twice that given in the previous **equation**. The op amps' capacitance rises as the output voltage approaches any of the supply rails, reaching the value of 55 pF. This increasing output capacitance arises from one of the complementary power transistors in the AD8592's output stage as its drain-to-source voltage approaches 0V at the output voltage close to the positive-supply rail. The increasing drain-to-source capacitance with decreasing drain-to-source voltage is an inherent

property of MOSFET transistors. The same situation holds true for the bottom power transistor of the AD8592's output stage, when the output voltage approaches the negative-supply rail.

The turn-on time of the AD8592 is much longer than the turn-off time. Although the device's data sheet does not directly specify these times, you can see from the internal structure of the IC that the on/off control enters almost all of the IC's stages (**Reference 1**). Thus, turn-off is fast because the turn-off of the output stage occurs without regard for the states of the preceding stages. Within one period of operation of the circuit in **Figure 1**, a sequence of two turn-ons (T_{ON}) plus four intentionally added delays (T_{DE}) determines the shortest sampling period: $T_{MIN} \sim T_{ONB3} + 4T_{DE} + T_{ONA1B1A2}$. Here, $T_{ONA1B1A2}$ is the largest from among the values of turn-on times of followers A_1, B_1, and A_2, which depend on the actual values of V_{INA} and V_{INB}. The maximum sampling frequency is then $1/2(T_{ON}+2T_{DE})$.

If you assume that the maximum turn-on time can reach the value of the overvoltage-recovery time of approximately 3 µsec and that the delay time is approximately 0.35 µsec, then it follows that the maximum sampling frequency is approximately 135 kHz. The duty-factor of the external logic-control signal, Q, for sampling frequencies near the value of the maximum sampling frequency should be about 0.5 (**Figure 2**). EDN

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Precision capacitive-sensor interface suits miniature instruments

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University of Shanghai for Science and Technology, Shanghai, China

In some applications of capacitive sensors, the instrument's front end must be small enough to fit into a narrow space. **Figure 1** shows a precision capacitive-sensor interface for such use. The square-wave output from a low-voltage 555 timer, IC_1, constantly triggers the precision one-shot, IC_2, to produce quasistable outputs for time periods T_1 and T_2, which are proportional to external timing capacitance: $T_1 = KR_0(C_S + C_0)$, and $T_2 = KR_0C_S$, where K is the multiplier factor. K is nearly independent of the external timing capacitance when that capacitance is more than 100 pF (**Reference 1**). So, a 150-pF capacitor, C_0, in shunt with the capacitive sensor, C_S, supplies an offset so that operation of the one-shot remains within a linear range even if the value of C_S is less than 100 pF.

To achieve good measurement accuracy, connect a reference channel with a fixed 150-pF capacitor. This method cancels the effects of both stray capacitance and transition time. A single 3.3V supply powers this interface circuit. The circuit's compact design permits flexibility, and you can easily

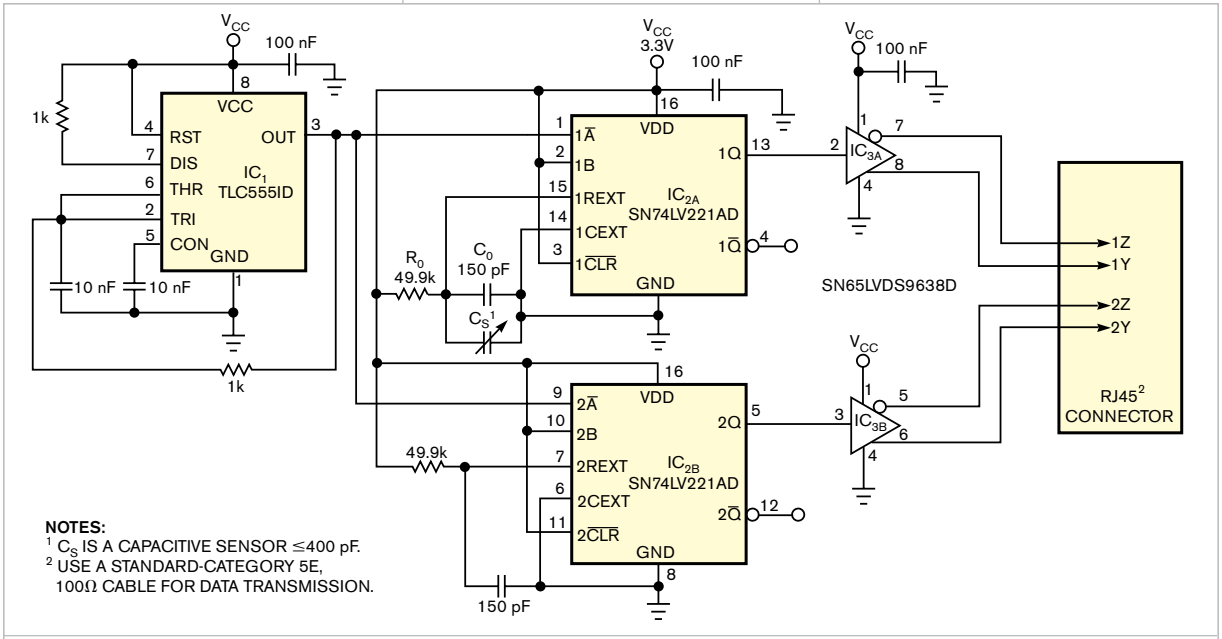

Figure 1 This compact capacitive-sensor-interface-circuit design permits great flexibility; you can easily integrate it into a miniature sensor head near the measurement point.

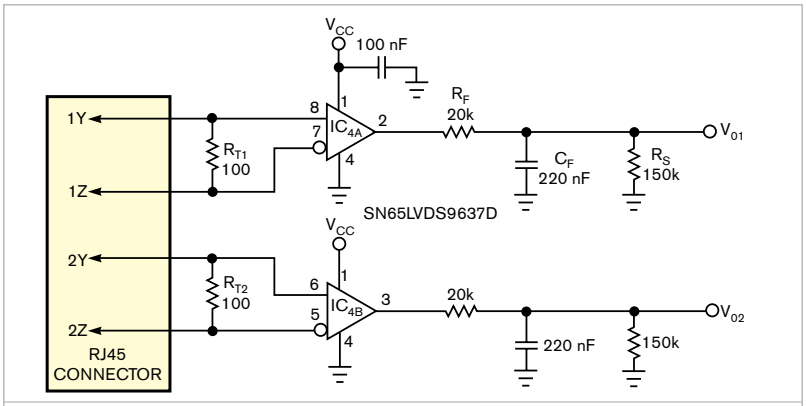

Figure 2 At the terminal, IC_4 converts the signals it receives from the interface to LVTTL levels and then feeds them to a set of passive filters.

integrate the circuit into a miniature sensor head near the measuring point. IC_3 converts the outputs to LVDS (low-voltage-differential-signaling) levels and then transmits these outputs using a standard Category 5e cable to the terminal, which may be some distance away. As long as the cable is shorter than 10m, the transmission bandwidth is adequate for ensuring acceptable measurement accuracy within several picofarads to hundreds of picofarads (**Reference 2**). In **Figure 2**, the terminal at IC_4 converts the signals it receives from the interface to LVTTL (low-voltage-transistor-to-transistor-logic) levels and then feeds them to a set of passive filters. Each dc output is proportional to the signal's duty cycle:

$$V_{O1} = V_H \times \frac{T_1}{T_P} \times \frac{R_s}{R_f + R_s},$$

and

$$V_{O2} = V_H \times \frac{T_2}{T_P} \times \frac{R_s}{R_f + R_s},$$

where V_H is the high-level output voltage of IC_4 and T_P is IC_1's oscillation period. By digitizing the two outputs, you can obtain a reading proportional to the sensor's capacitance, $V_{O1} - V_{O2}$. Be sure that $T_1 < T_P$—that is, $C_S < T_P/(K \times R_0) - C_0$; otherwise, the final output will be erroneous. For the sake of a wide measurement range, keep T_P as long as the target application permits. **EDN**

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2. High-performance linear products technical staff, *LVDS Application and Data Handbook*, Texas Instruments, November 2002, http://focus.ti.com/lit/ug/slld009/slld009.pdf.

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Simple toggle circuits illustrate low power-MOSFET leakage

Tom Bruhns, Mukilteo, WA

The novelty circuit in **Figure 1** illustrates the extremely low gate-leakage current typical of modern power MOSFETs. You can find parts that, in a moderately dry environment, will hold their state for days at a time. In operation, if MOSFET Q_1 is off, the load—perhaps a lamp or a buzzer—pulls Q_1's drain to nearly the 12V-dc power-supply voltage. R_2 charges C_1 to practically the same voltage. If you tap momentary-contact switch S_1, C_2 and the gate of Q_1 charge to about 99% of C_1's initial voltage, assuming that the tap is short enough that C_1 doesn't discharge significantly back through R_2 to the drain of Q_1, which is now at a low voltage. During the next couple of seconds, C_1 discharges through R_2 toward the new drain voltage of Q_1, which now conducts current through load resistor R_1.

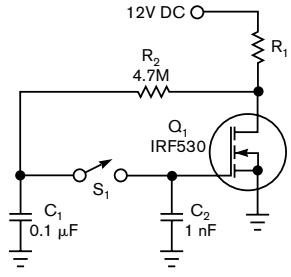


Figure 1 This "toggle" circuit demonstrates the low gate leakage of modern power MOSFETs.

In the construction of the circuit, you must ensure extremely low leakage from the MOSFET's gate node. You can omit C_2 if you use a switch with essentially no leakage, and you may find that the gate capacitance of Q_1 is enough and that the leakage is low enough that days pass before the output changes significantly. If you'd like to ensure a longer hold time, you can increase the value of C_2. A modern polypropylene capacitor should have a self-discharge time constant measured in years if you keep it clean, dry, and not too far above room temperature. If you increase C_2, proportionately increase C_1 and decrease R_2 to maintain an R_2C_1 time constant of about half a second.

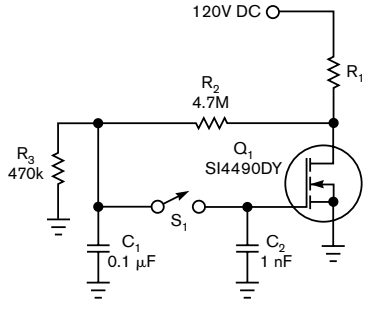
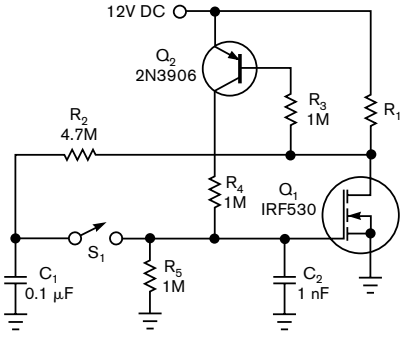


Figure 2 This circuit can control higher voltages because it supplements R_2 with a resistor to ground to form a voltage divider, ensuring that C_1 doesn't charge to a voltage that would destroy the gate of Q_1.



NOTE: LOADS AS LARGE AS A FEW AMPS ARE POSSIBLE WITH THE RIGHT POWER MOSFET.

Figure 3 This version of the toggle circuit indefinitely holds a state.

Another curious behavior of this novelty circuit occurs if you hold down S_1 for a few seconds. The gate of Q_1 then goes to a voltage slightly higher than the gate's threshold voltage for Q_1. If, for example, the power supply is 6V and the load is a 6V incandescent lamp and Q_1's gate threshold is approximately 3V, the lamp will light dimly. When you release the switch, because a typical power MOSFET has a high rate of drain-current change with gate-voltage change—that is, transconductance—you can observe

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the slow change in gate voltage as a change in lamp brightness. Any leakage is inside and external to Q_1. You may be able to detect a change in lamp brightness within a few seconds. But, even if you don't notice it, some change of voltage will occur. If you tap S_1 several times at intervals of a few seconds, the lamp will soon toggle between full brightness and fully off.

To use the circuit to control higher voltages, you can supplement R_2 with a resistor to ground to form a voltage divider to ensure that C_1 doesn't charge to a voltage that would destroy the gate of Q_1 (**Figure 2**). For a more practical toggle circuit that will indefinitely hold a state, you can add a transistor and some resistors (**Figure 3**).

If Q_1 is on and powers the load, then Q_2 is also on, holding Q_1's gate on at about half the power-supply voltage because of the voltage-divider action of R_4 and R_5. Tapping S_1 toggles the output as before, and, with Q_1 off, Q_2 is also off, allowing R_5 to hold Q_1's gate near ground potential. EDN

Circuit adds functions to a monostable multivibrator

PM Ishtiaq, S Mufti, MA Darzi, and GN Shah,
Nuclear Research Laboratory, Bhabha Atomic Research Centre,
Kashmir, India

Gate generation is often an inevitable step in digital-signal processing. Invariably, the gate generation during event processing in a digital system uses the input trigger of a monostable multivibrator. The values of the RC (resistance-capacitance) components within the manufacturer-supplied parameters determine the gate width of the output pulse of the monostable multivibrator. The monostable multivibrator generates only one-shots for each input trigger during event processing.

However, you can enhance the functional capability of gate generation of a monostable multivibrator with modifications in its input-trigger circuitry to generate any number of output-gate pulses for each single-input triggering. You can exploit the resultant circuit to generate a fixed number of repetitive gate pulses with a single-input trigger by incorporating a counter with the circuit to keep track of the gate generation. The monostable multivibrator becomes inactive as soon as it generates the requisite number of gates.

Figure 1 shows modifications to a monostable multivibrator that allow it to repetitively generate 63 gate pulses with one trigger. The RC components determine a gate width of 5 to 75 µsec. However, this design has a preset gate width of 20 µsec to give a total time

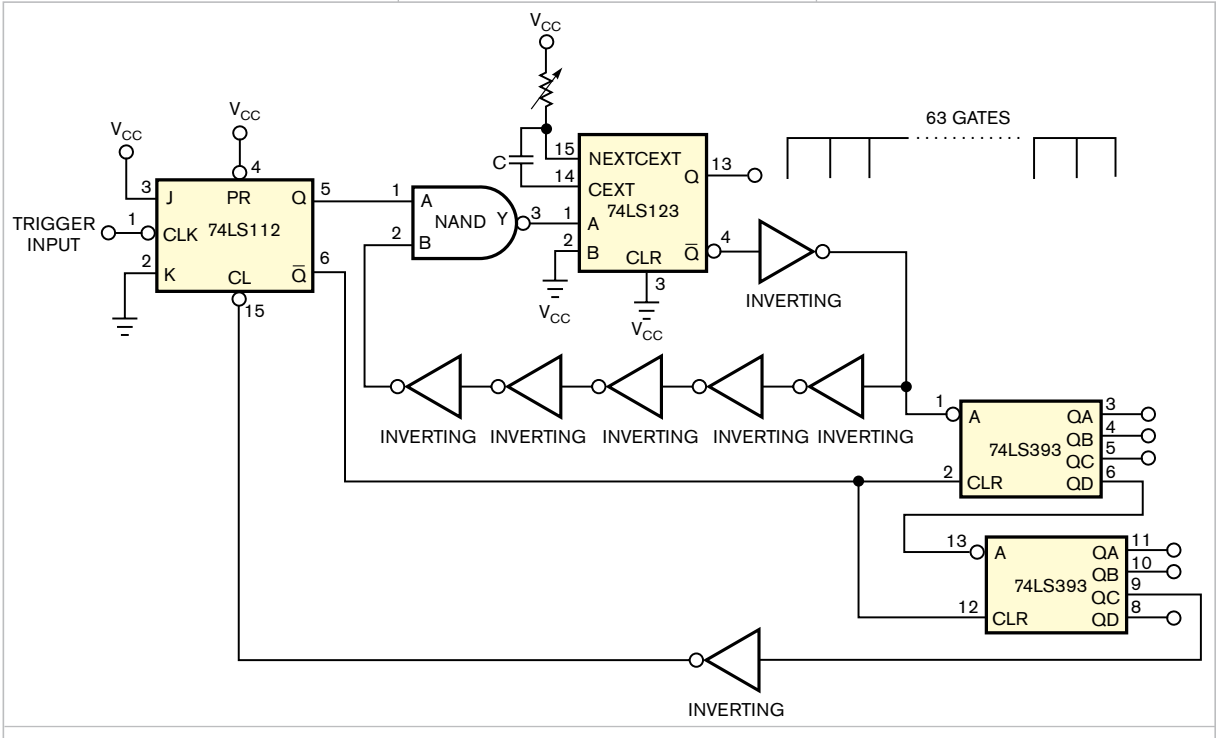

Figure 1 By adding counters and an oscillator to the output of a monostable multivibrator, you can generate any number of output-gate pulses.

interval of 1260 µsec. When the input-trigger pulse goes to the active low, Pin 1, of the JK 74LS112 flip-flop, the falling edge of the input-trigger pulse activates the flip-flop to set Q. Because the default condition of Pin 2 of the NAND gate is at a high level, the transition at the output pin, Pin 3, of the NAND gate passes on to the active-low input of the monostable multivibrator at Pin 1. The falling edge of the output pulse of the NAND gate triggers the monostable multivibrator to generate the first gate pulse of predefined gate width.

Subsequently, when the Q output pulse of the monostable multivibrator makes a transition from high to low, the rising edge of the complementary output pulse of the monostable multivibrator at $\overline{Q}$, Pin 4, connects back to the two-input NAND gate. Through a series of inverter retriggers, the monostable multivibrator again generates the next gate pulse. The gate generation can continue indefinitely. However, the $\overline{Q}$ output after inversion also feeds into two 74LS393 hex counters. The two hex counters cascade together to count the 63 gate pulses. As soon as the circuit counts the requisite number of gate pulses, Pin 9 of the hex counter goes high and, after inversion, clears the active state of the JK flip-flop.

The two-input NAND gate's Pin 1 also goes to a low level and disables the flip-flop, preventing the feedback rising-edge transition of the $\overline{Q}$ of the monostable multivibrator from again passing on to the trigger input—Pin 1 of the monostable multivibrator. So, the trigger to the monostable multivibrator and further gate generation stop (**references 1** and **2**).EDN

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2. Shah, GN; H Razdan; CL Bhat; and QM Ali, "Neutron generation in lightning bolts," *Nature*, Volume 313, Feb 28, 1985, pg 773, www.nature.com/nature/journal/v313/n6005/abs/313773a0.html.

Piezoelectric driver finds buzzer's resonant frequency

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Piezoelectric buzzers find wide use as audible-signal generators because of their low power consumption and clear, penetrating sound. An external driver or a self-driven circuit that oscillates at the resonant frequency of the piezoelectric element can drive these buzzers. A piezoelectric element produces the maximum sound output at its resonant frequency. However, the resonant frequency of a piezoelectric element can have a tolerance as great as ±15%. An external driver tuned to the nominal resonant frequency is therefore likely to miss the actual resonance point. This Design Idea externally drives a piezoelectric element and automatically finds its actual resonant frequency.

The basis for operation is the following principle: When you apply an alternating voltage to the terminals of a piezoelectric element, the element will begin to vibrate. If you remove the excitation, vibrations will continue in a damped manner before they cease altogether. These residual vibrations will cause damped oscillations at the terminals of the piezoelectric element. If the excitation is close to the resonant frequency, the vibrations will be stronger and the residual oscillations will last

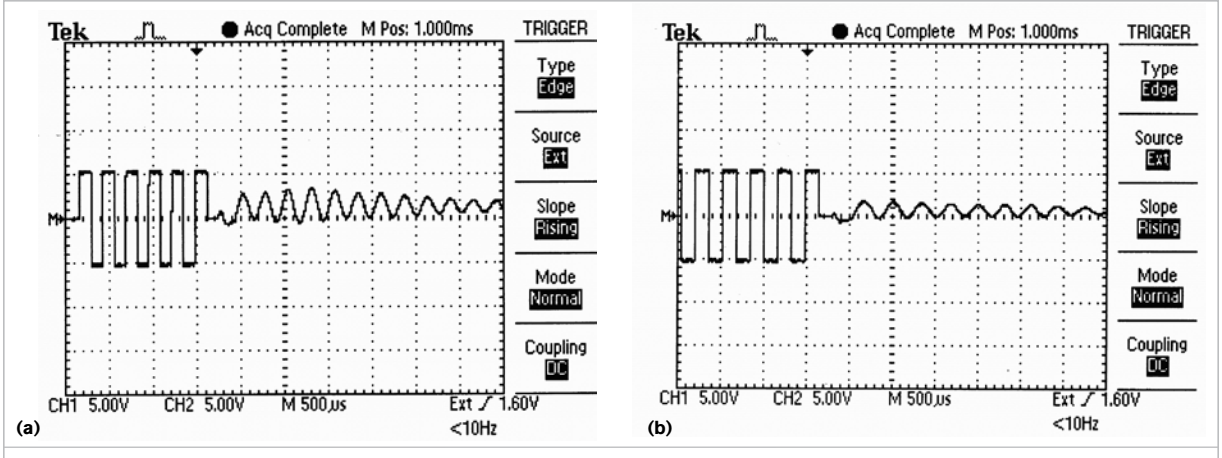

Figure1 At a frequency of 4 kHz, which is closer to the resonant frequency, residual oscillations last longer (a) than the resonant frequency with 3.2 kHz (b).

longer (**Figure 1**). You can determine the actual resonant frequency by trying all the frequencies around the nominal resonant frequency and comparing the duration of residual oscillations.

In this design, a Microchip (www.microchip.com) PIC18F452 microcontroller drives a piezoelectric element through its I/O pins, RB4 and RB3 (**Figure 2**). Initially setting RB3 to zero and RB4 to one and toggling them after each half-period generates an alternating piezoelectric voltage (V_p) with a 0V-dc bias. After applying 10 cycles, RB3 is kept low, and

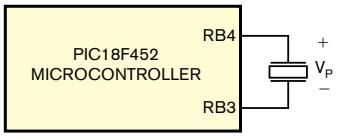

Figure 2 A PIC18F452 microcontroller first drives the piezoelectric buzzer at a programmed frequency and then configures one of its pins as an input to count the residual oscillations.

RB4 is made an input to count the low-to-high and high-to-low transitions of V_p. Enabling the "interrupt-on-port-change" feature of Port B for 10 msec and incrementing a counter in the interrupt-service routine counts the transition of the piezoelectric voltage. **Listing 1**, which is available in the Web version of this Design Idea at www.edn.com/080807di1, demonstrates this feature. The program repeats these steps for all frequencies of interest and identifies the frequency corresponding to the maximum number of transitions at the resonant frequency. You can easily expand the idea for the case of multiple resonant frequencies. EDN

Low-cost digital DAC provides digital three-phase-waveform synthesis

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and R García-Gil, J Castelló, and JM Espí, Universidad de Valencia, Spain

Many applications involve the digital synthesis of three-phase sinusoidal waveforms, such as ac-motor drives, active power filters, and grid-voltage synchronizers, that use a microcontroller or a DSP for digital control. You can perform this synthesis by using conventional analog techniques (**Reference 1**) or DDS (direct digital synthesis). Digital techniques provide higher stability and the ability to incorporate frequency, phase, and amplitude adjustments. For applications requiring 16-bit or higher-resolution, three-phase-signal synthesis, DDS involves the use of a microprocessor or a DSP to interface multiple DACs. This approach uses not only a lot of devices, but also supporting components and board space. Although one device can have multiple-output serial-controlled DACs with four, eight, 32, or more

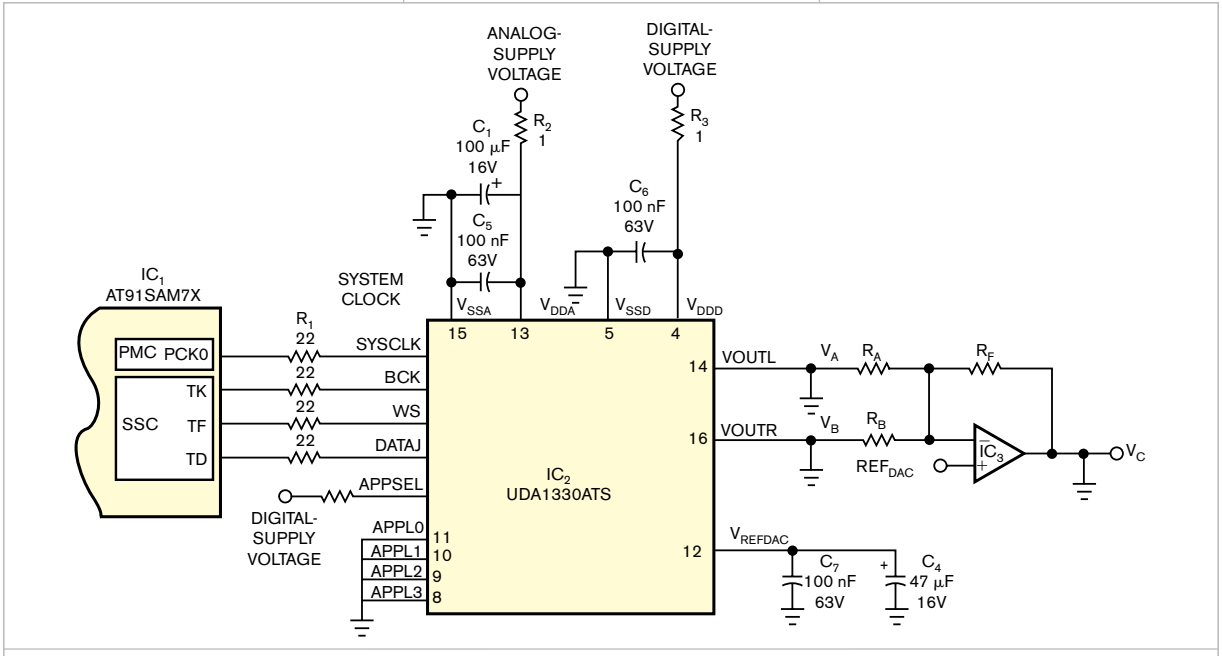

Figure 1 This scheme implements three-phase DDS (direct digital synthesis) with few components. The code in the ARM processor provides the ability to incorporate arbitrary frequency, phase, and amplitude adjustments with 16-, 18-, or 20-bit resolution.

channels, the DACs provide few bits at the expense of the number of channels. Hence, using multiple-output DACs is an unappealing approach.

Alternatively, you can use shift registers or switched-capacitor filters, but this approach also involves a high parts count, and the lack of phase and amplitude adjustment makes this method inappropriate for high-resolution DDS (**Reference 2**). In contrast, stereo DACs are readily available. Their widespread use has produced low-cost, high-quality components. For example, the NXP UDA1330ATS has an I^2S-serial data-format interface; word lengths of 16, 18, and 20 bits; and sampling frequencies of 8 to 55 kHz (**Reference 3**). These features make the DACs attractive for three-phase DDS with few components.

This Design Idea implements DDS techniques using an ARM microcontroller, IC_1; one stereo-DAC, IC_2; and one op amp, IC_3 (**Figure 1**). The ARM AT91SAM7X256 code in **Listing 1**, available in the Web version of this Design Idea at www.edn.com/080807di2, generates a table containing the cosine function of the desired resolution and length. The table produces $\cos(\alpha+2/3\pi)$ and $\cos(\alpha-2/3\pi)$. The ARM microcontroller sends the data using I^2S-serial format by using interrupts attaching the ISR (interrupt-service routine) whenever the output buffer is empty. **Listing 2**, also in the Web version of this article, shows how to achieve an ISR to send the data. IC_2 provides voltage outputs V_A and V_B, which are two of the three signals for a maximum amplitude of 5V p-p, but with an offset of 2.5V. You can derive the third channel as a function of the other channels. You can easily implement this operation using a single inverting, summing op amp, IC_3, and the 2.5V DAC reference for canceling the offset. In this case, $R_F=R_A=R_B=10\,k\Omega$ for obtaining unity gain, and you could add a potentiometer in the inverting pin for an exact offset cancellation if the resistors don't match exactly.

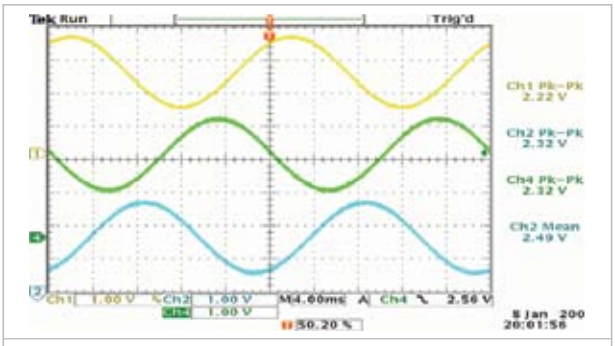

Figure 2 Traces 1 and 2 show the voltage outputs from the DAC. Trace 4 is the third channel that an inverting, summing op amp provides.

Figure 2 shows the synthesis of the three-phase waveforms. For further explanation and to access the **references** to this article, go to www.edn.com/080807di2.EDN

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Astable multivibrator lights LED from a single cell

Luca Bruno, ITIS Hensemberger, Monza, Lissone, Italy

Lighting LEDs from a single 1.5V cell poses a problem because their forward voltages are higher than the cell's. The simplest way to light the LED is to use a step-up dc/dc converter. This Design Idea offers a simple and reliable alternative for applications in which low cost is of primary concern. The circuit in **Figure 1** employs a classic astable oscillator, which transistors Q_1 and Q_2 form. The square-wave drive signal at Q_2's collector turns a PNP switching transistor, Q_3, on and off. When Q_3 turns on, it charges inductor L_1, and, when it turns off, inductor L_1 discharges its stored energy through the LED during flyback, allowing you to light any type or color of LED.

The astable circuit oscillates at a frequency of $1/T_O$, where $T_O=T_L+T_H$ with $T_L \simeq 0.76R_2C_2$ and $T_H \simeq 0.76R_1C_1$ when the cell voltage is 1.5V, where T_O is the time, T_L is the on-time, and T_H is the off-time. With the component values in **Figure 1**, the frequency and the duty cycle are about 28.5 kHz and 50%, respectively. During the on-time, transistor Q_3 is on, and inductor L_1 starts to charge with constant voltage so its current ramps up linearly to a peak value, as the following **equation** describes: $I_{L1PEAK}=[(V_{BAT}-V_{CESATQ3})/L_1]\times T_L$, where I_{L1PEAK} is the peak current of L_1, V_{BAT} is the battery voltage, and $V_{CESATQ3}$ is the collector-to-emitter saturation voltage of Q_3. During the off-time, Q_3 is off, and the inductor's voltage reverses polarity, forward-biasing the LED and discharging through it at a constant voltage roughly equal to the forward voltage of the LED while its current ramps down to zero.

Because this cycle repeats at a high rate, the LED appears always on. The LED's brightness depends on its own average current, which is proportional to the peak value. Because the LED current is roughly a triangular pulse with a peak current approximately equal to the inductor's current because of the finite turn-off time of Q_3, you can easily estimate the average current: $I_{LEDAVG} \simeq (½)\times I_{L1PEAK}\times(T_{DIS}/T_O)$, where T_{DIS} is the discharge time of inductor L_1 through the LED, which you can roughly estimate from the slope of L_1's discharge, which is V_{LED}/L_1, where V_{LED} is the LED's voltage.

To control the LED's brightness, you may increase or decrease the inductor's peak current by varying its inductance from 100 to 330 µH to achieve the optimal brightness for the type of LED you are using. However, L_1's charge slope is always smaller than its discharge slope, and, because T_L and T_H are equal, L_1 has enough time to discharge completely. When it recharges on its next cycle, its current

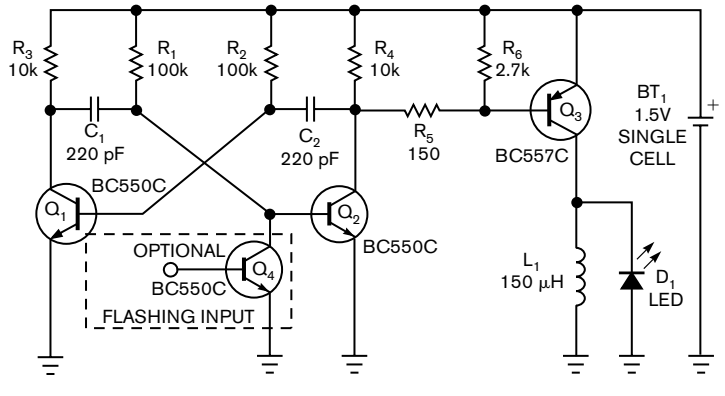

Figure 1 This simple astable multivibrator provides a low-cost way to drive an LED from a single cell.

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cycle always starts from zero. If this is not the case—if you reduce T_H too much, for example—the inductor current increases on each cycle until Q_3 goes out of saturation, and the final current value becomes unpredictable because it depends on Q_3's dc gain. Optional transistor Q_4 allows the circuit to flash the LED when a low-frequency gating signal drives its base.

No one component is critical; for example, any small-signal transistor is suitable. But, if possible, choose a PNP transistor for Q_3 with high dc-current gain and low collector-to-emitter saturation voltage for best efficiency. Also, take care that the peak current does not saturate L_1 and does not exceed the maximum peak-current rating of Q_3 and the LED. The astable circuit starts to operate with a supply voltage as low as 0.6V, but the LED is off and begins to light dimly when the supply voltage exceeds 0.9V. When the supply voltage exceeds 1V, the LED's brightness is adequate, even if it depends slightly on the forward voltage of the LED. EDN

IC provides versatile toggle functions

Louis Vlemincq,
Belgacom, Evere, Belgium

The circuit in **Figure 1** offers not only as many as six channels in a single IC package, but also a high level of additional flexibility. The configuration of Output 1 is a "plain-vanilla" toggle. A resistive divider comprising R_1 and R_2 provides a midsupply bias to all the channels through resistors R_3, R_6, R_7, R_{10}, and R_{12}. Because the bias voltage of R_1/R_2 is within the hysteresis range of the gates, they behave as flip-flops, retaining their high or low state in a stable manner.

Debouncing capacitors C_2, C_3, C_4, and C_5 charge to the level of the output. Pushing switch S_1 inverts the output state because of the inverting action of the gate. This state remains stable because, in the first gate's circuit, for example, R_4's value is larger than that of R_3, and R_4 cannot overcome the hysteresis threshold of the gate. Only the discharge of C_2 can accomplish that task. When you release the pushbutton, C_2 fully charges after the debouncing delay, and the circuit is ready for another inversion. C_1 provides a general power-on-reset feature to all the channels. If your circuit requires only one channel, you can directly connect R_1 and R_2 to the input of the gate, omitting R_3.

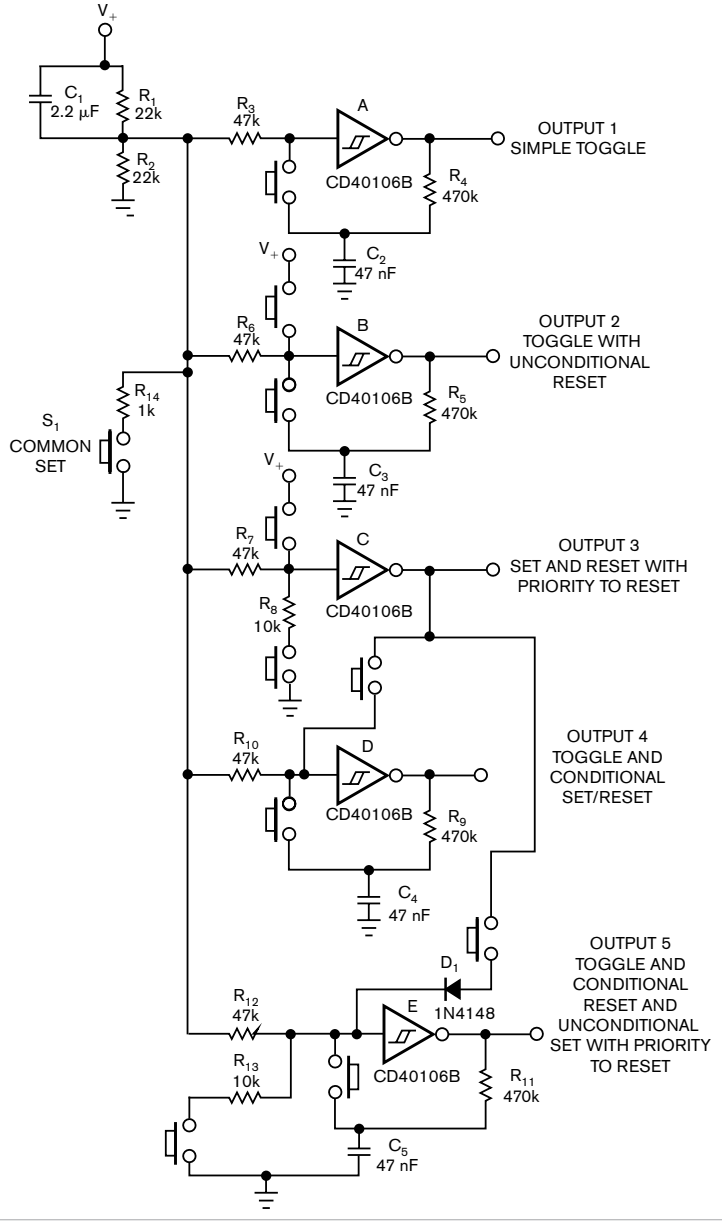

Figure 1 This circuit shows multiple Schmitt-trigger inverters functioning as a variety of set/reset toggles.

Output 2 has the same toggle function as Output 1 but also includes a direct reset. Output 3 works only in a set/reset mode; the position of R_8 determines the priority state. Output 4 also has a toggle action, but you can set or reset it to a state opposite that of Output 3. Output 5 works in a similar manner, except it allows only a conditional reset because of the position of D_1. Output 5 also includes a forced, nonpriority set. You can mix and match all these functions, providing almost unlimited versatility.

The IC in **Figure 1** is a Fairchild Semiconductor (www.fairchildsemi.com) CD4000-series circuit, suitable for supplies of 3 to 15V, but it could also be a 74AC14 or 74HC14 from NXP (www.nxp.com), for example. Any CMOS-input gate having a Schmitt-trigger action is suitable. You must take care to bias the inputs in the middle of their hysteresis range. HCMOS circuits would require an average bias of approximately 1.2V for a 5V supply, for example. EDN

Instrumentation amp has low offset, drift, and low-frequency noise

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Analog Devices' (www.analog.com) digitally gain-programmable AD8231 instrumentation amplifier exhibits zero offset. It has programmable voltage gains, which are successive powers of two, from $2^0=1$ to $2^7=128$ (**references 1** and **2**). The AD825x family also includes some digitally gain-programmable instrumentation amplifiers, which have gain expressed as powers of 10. These amplifiers contain no internal autozero circuitry, however. The composite instrumentation amplifier in **Figure 1** suits applications requiring instrumentation amplifiers having voltage gains of a multiple of 10 and requiring low voltage offset, drift, and low-frequency noise.

The design exploits the fact that the gain is 10^M, where M is an integer, which you can express as $10^M=2^M\times5^M$. The circuit in **Figure 1** employs a cascade of the autozeroed AD8231 instrumentation amp, IC_1, with a preset voltage gain of eight, IC_2, and IC_3. The net result is that the input-voltage offset of IC_2 causes an RTI (referred-to-input) voltage offset, which decreases by a factor of eight compared with an offset of a stand-alone circuit, IC_2. The same holds also for the offset-voltage drift. The auto-zeroing circuitry of the IC_1 decimates the low-frequency noise. EDN

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1 "Zero Drift, Digitally Programmable Instrumentation Amplifier, AD8231," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8231,00.html.

2 "10 MHz, 20V/s, G=1, 2, 5, 10 iCMOSR Programmable Gain Instrumentation Amplifier, AD8250," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8250,00.html.

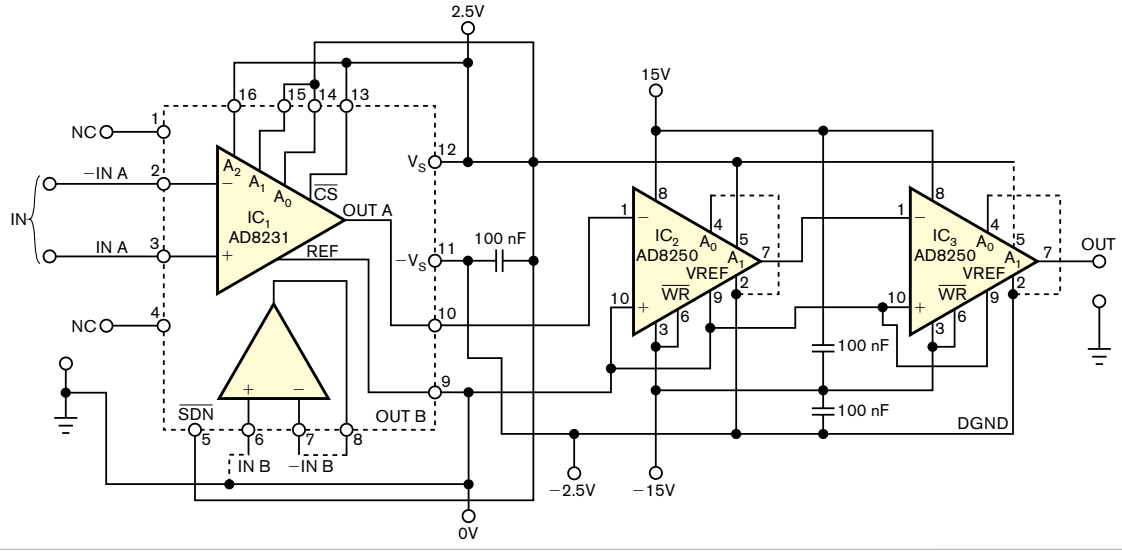


Figure 1 By cascading an autozeroed instrumentation amplifier having a gain of 2^3 and instrumentation amplifiers having gains of five, you get a decade-gain instrumentation amp whose dc performance is much better than that of monolithic decade-gain instrumentation amps.

Four DIPs provide as many as 80 sequential-LED outputs

Greg Carkner, Cobourg, ON, Canada

A previous Design Idea makes clever use of the ability of the 4017 CMOS counters to accept either positive or negative edge-clock signals, even though it leaves two LEDs on at once (**Reference 1**). But what happens if you want more than 19 counts? A quick check in some old CMOS data books uncovered a circuit for using 4017 counters to make sequential displays. However, this approach sacrifices some outputs and yields nine outputs for the first counter and only eight for each subsequent one. It also requires you to add an AND gate between each successive counter stage.

The circuit in **Figure 1** differs from the one in the earlier Design Idea in that it uses HCMOS parts and adds one 74HC540 to facilitate a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs. The 74HC540 is a convenient pinout version of the venerable 74HC240-series bus drivers. By including a DIP-resistor network, you can also reduce the discrete-component count for the design. The recommended current-sourcing capability of the HC-series parts at 6V supply is slightly lower than that of the 4000-series parts at 15V, but the reduced resistor losses provide a more energy-efficient circuit if you use better LEDs.

The **figure** omits the necessary supply-bypassing capacitors or a clock or power-on-reset circuit. D_1, D_2, and R_1 form a simple AND gate, which you might use instead of an external reset input to form a continuous ring counter, at which the cathodes connect to selected outputs of each of the counters, IC_1 and IC_2. EDN

REFERENCE

1 Tregre, Jeff, "Cascade two decade counters to obtain 19 sequential outputs," *EDN*, Dec 14, 2007, pg 62, www.edn.com/article/CA6512153.

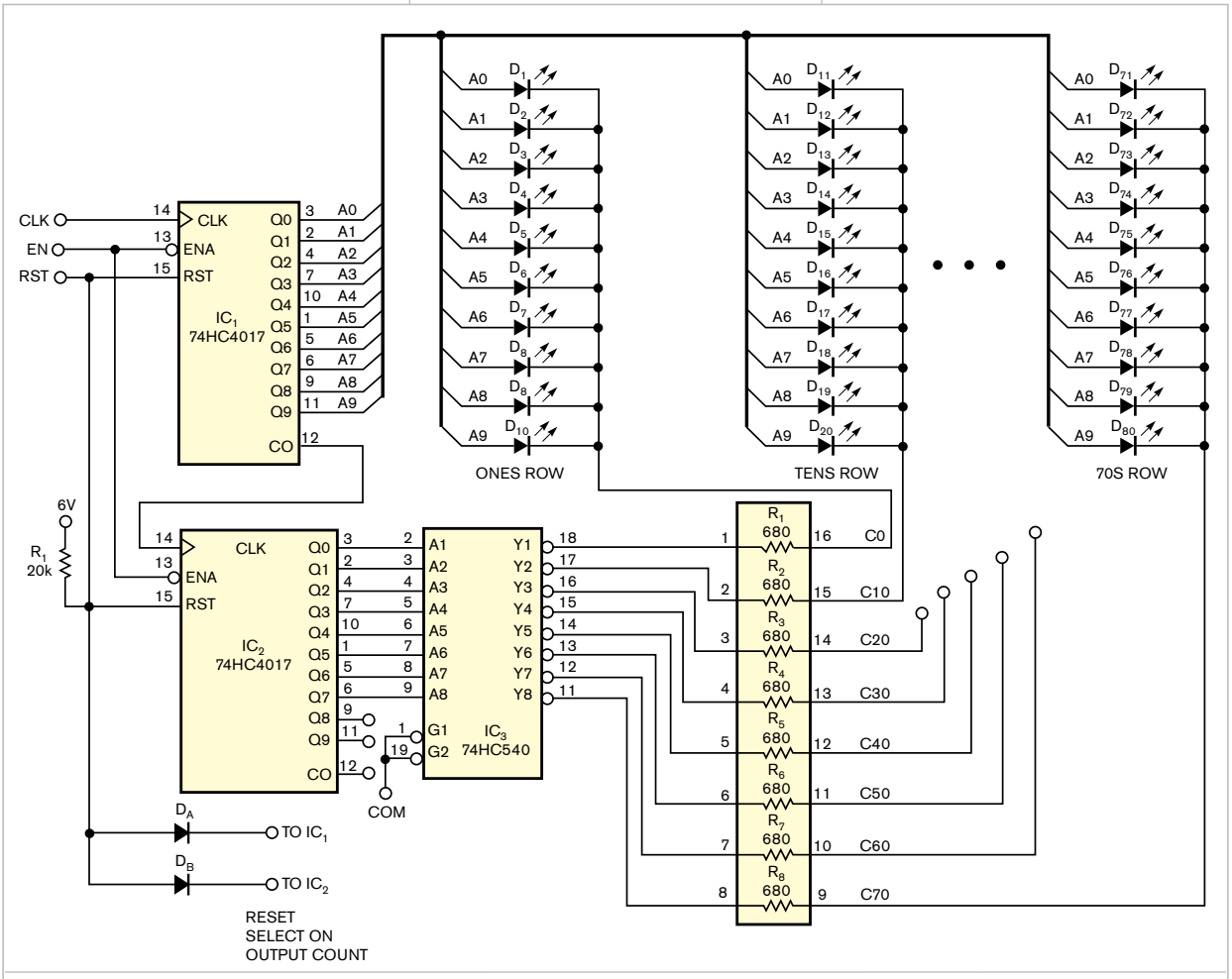


Figure 1 This circuit provides a simple means of multiplexing the outputs of two 4017 counters for as many as 80 outputs.

Program an op-amp gain block with a limited-adjustability, monolithic, solid-state resistor

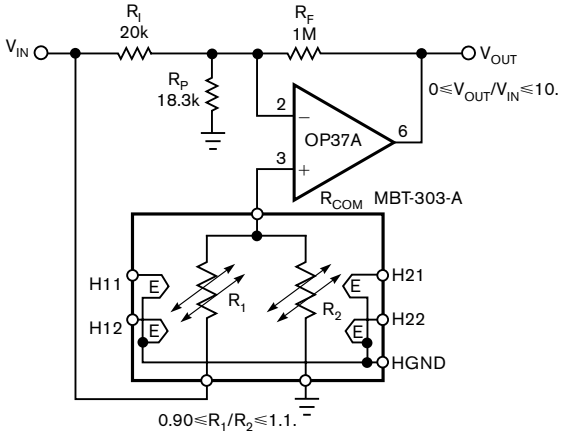
W Stephen Woodward, Chapel Hill, NC

Solid-state replacements for traditional electromechanical trimmer potentiometers are increasingly available in a variety of technologies from a variety of vendors. These replacements have many obvious advantages, such as automatic adjustability, miniaturization, and immunity to vibration. Some of these devices have only limited programmable spans, however. This limitation can sometimes be problematic and may preclude the use of a solid-state option in some design applications. An example of this shortcoming is the Rejustor family of devices, which Microbridge (www.mbridgetech.com) recently introduced. The MBT-303-A Rejustor voltage divider is programmable over a span of only ±10%. When such a limited-capability device sets the gain of a typical amplifier circuit, the correspondingly narrow range of accessible gains may be woefully inadequate.

Figure 1 suggests a generally applicable workaround that works not only with rejustors, but also with all limited-adjustability, programmable dividers with a ±10%-ratio-adjustment range. It uses a single op amp in a differential topology that, in effect, subtracts the minimum programmable-divider ratio from the maximum and amplifies the difference. This approach expands the programmable-gain span to include zero and any desired figure. Potential applications for this trick include any design situation requiring a wide range of inverting and noninverting programmable-gain factors.

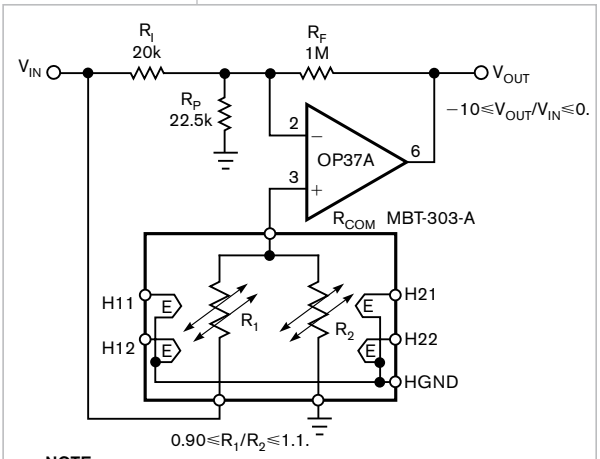
Although the circuit in **Figure 1** implements a programmable gain of zero to 10, you can implement almost any range with a suitable choice of resistors and op amps. **Figure 2** illustrates a gain of zero to −10 for the inverting case. The design equations are R_F/R_I, which is five times the maximum desired gain; $R_P=1/((1/0.9/R_I)-(1/R_F))$ for noninverting gain; and $R_P=1/((1/1.1/R_I)-(1/R_F))$ for inverting gain. The availability of stock resistances sometimes determines a starting value for R_I or R_F. For example, the circuit in **Figure 1**, where R_F has a value of 1 MΩ, accommodates the fact that many inexpensive precision-resistor families, such as those made of metal film, have maximum resistances of 1 MΩ. However, if resistor availability isn't a factor, then choosing R_I to have the same value as R_I minimizes sensitivity to op-amp bias-current errors. Choosing R_P midway between the resistances for the noninverting- and inverting-gain equations reveals an additional flexibility of the circuit. That variation results in a bipolar—that is, both inverting and noninverting—gain range, with a gain of zero at midspan.

This topology eliminates the inflexibility penalty that limited divider programmability imposes. This benefit, however, incurs a price in the op amp's performance. Because of the partial cancellation of amplifier gain, the gain-bandwidth product and dc accuracy of the op amp must surpass the overall maximum gain and offset requirements of the gain block by at least a factor of five. One way to accommodate this requirement is to incorporate a decompensated, precision op amp, such as the classic OP37, which is stable only for closed-loop gains higher than five. EDN



NOTES:
Set R_P=20.4 kΩ FOR A PROGRAMMABLE-GAIN RANGE OF −5≤GAIN≤+5.
$V_{OUT}/V_{IN}=50(R_2/R_1-0.9)=0$ IF $R_2/R_1=0.9$ AND $=10$ IF $R_2/R_1=1.1$.

Figure 1 Adding an op amp and associated components to a Rejustor solid-state resistor allows you to trim the output over the full input-voltage range.



NOTE:
$V_{OUT}/V_{IN}=50(R_2/R_1-1.1)=0$ IF $R_2/R_1=1.1$ AND $=-10$ IF $R_2/R_1=0.9$.

Figure 2 Adjusting the value of R_P allows the circuit to function as an inverting trimmer.

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Platinum-RTD-based circuit provides high performance with few components

Jordan Dimitrov, Toronto, ON, Canada

The standard way of using an RTD (resistance-temperature-detector) sensor is to include it in a bridge followed by a differential amplifier. The problem is that two nonlinearities—one from the sensor and another from the bridge—affect the transfer function. Some approaches are available that attempt to avoid the problem, but they tend to be bulky and expensive (**references 1**, **2**, and **3**). An alternative circuit proposes adding only one extra resistor to the differential amplifier but provides neither design guidelines nor results (**Reference 4**). This Design Idea fills the gap. Although circuit analysis is somewhat complex, performance is good, and the circuit uses few components.

Besides the platinum RTD, R_Θ, the circuit features only six precision resistors, an op amp, and a voltage reference (**Figure 1**). R_4, the extra resistor for the differential amplifier, delivers additional current to the sensor that relates to the temperature you are measuring. With proper design, the circuit can provide good linearity and stability over a wide range of input temperatures. The output voltage, V_O, depends on circuit components in the following way:

$$V_O = V_{REF} \times \frac{Y_1}{Y_2} \times \frac{R_\Theta(Y_0 + Y_2 - Y_3 - Y_4) - 1}{R_\Theta[Y_1 + Y_3 - R_2 Y_4(Y_0 + Y_1)] + 1},$$

where $Y_I = 1/R_I$ and I=0 to 4.

For positive temperatures, a second-degree polynomial of the following form can approximate RTD characteristics:

$$R_\Theta = R_0(1 + \alpha \times \Theta + \beta \times \Theta^2),$$

where R_0 is sensor resistance at 0°C, α and β are coefficients, and Θ is the measured temperature.

After replacing the second **equation** in the first and doing some rearrangements, you get:

$$V_0 = \frac{\Theta - B}{\Theta^2 - B\Theta - C} \times K \times \Theta = f(\Theta)K\Theta,$$

where B, C, and K are constants and f(Θ) is a function of temperature. **Figure 2** shows the general shape of f(Θ). The output voltage depends linearly on temperature when f(Θ) is as close as possible to a constant. This situation is most true around the minimum point of f(Θ).

Some additional relations provide that the output voltage is 0V at temperature 0°C, the conversion coefficient is 10 mV/°C, the minimum of function f(Θ) is in the middle of the measurement span, and

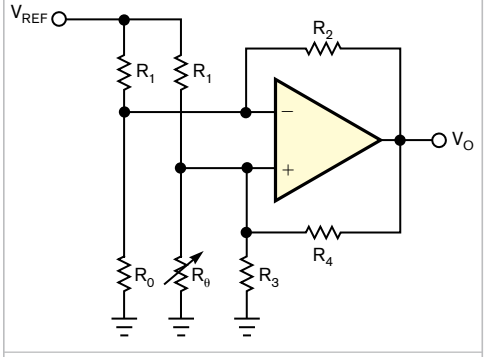

Figure 1 This generic RTD circuit needs few components.

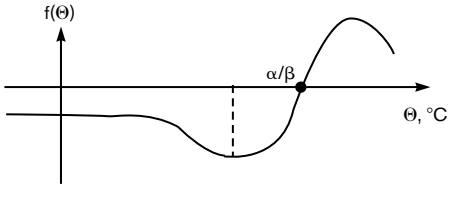

Figure 2 The general shape of function f(Θ) varies with temperature.

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the current through R_θ causes negligible self-heating of the sensor.

Figure 3 shows the circuit that meets these requirements. The sensor is a DIN-IEC 751 platinum RTD. Microsoft (www.microsoft.com) Excel software fits 13 points of 0 to 600°C in steps of 50° from the RTD's calibration table. The spreadsheet software determined R_0 to have a value of 100Ω, α to have a value of 3.908×10^{-3}°C^{-1}, and β to have a value of -5.801×10^{-7}°C^{-2} with an R^2 factor of one.

All the circuit's resistors have tolerances of 0.02%, and the temperature coefficient is 50 ppm/°C. You can use two trimming potentiometers, V_{R1} and V_{R2}, to independently adjust zero and span readings. You should perform span adjustment at 550°C to match the magnitudes of the positive and the negative errors. You can also extend the temperature range to start from −100°C instead of 0°C without exceeding the basic nonlinearity. The three-lead connection to the sensor significantly reduces the influence of connection-cable resistance, R_C, on accuracy.

Table 1 shows the results of evaluating this circuit's performance with a calibrated, precision-decade resistance and a calibrated, 4.5-digit multimeter with readings at ambient temperatures of 24 and 68°C; power supplies of ±12, ±15, and ±18V; and cable resistances of 0 and 5Ω. EDN

TABLE 1 EXPERIMENTAL RESULTS

Measurement range	−100 to +600°C
Nominal sensitivity	10 mV/°C
Basic accuracy (nonlinearity)	Well below ±1°C
Ambient-temperature effect	0.05°C/10°C
Power-supply effect	0.1°C/V
Cable effect (three-lead connection)	0.7°C/Ω
Power-supply range	±12 to ±18V
Consumption (600°C input)	9 and −3 mA
Operating temperature	−40 to +85°C

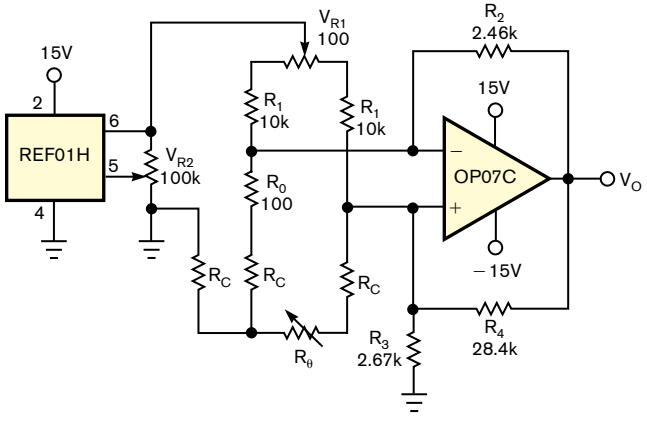

Figure 3 The full circuit needs trimming potentiometers V_{R1} and V_{R2} to adjust zero and span, respectively, and a three-lead cable for sensor connection. R_C is the cable's resistance.

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Proportional-ac-power controller doles out whole cycles of ac line

Richard Rice, Oconomowoc, WI

In industrial and process control, it is often necessary to accurately control the temperature of a process. You control most heating elements using the "bang-bang" method—turning the power to them on and off at a predetermined setpoint. The temperature of the heated substance constantly hunts back and forth around the setpoint. You can achieve much greater temperature precision using proportional power control. With this method, the controller monitors the temperature, proportionally varying the heater power to keep the temperature as close as possible to the setpoint. A PID (proportional-integral-derivative) control loop usually accomplishes this function. Varying the ac power to the heating element in a linear-proportional manner is neither easy nor simple.

This Design Idea borrows from the delta-sigma-modulator concept. The controller sends cycles of the ac line to the load as the delta-sigma modulator determines. For example, when the input-control voltage is 15% of full-scale, only 15 of 100 ac cycles arrive at the load. Likewise, at 85%, 85 of 100 arrive (**Figure 1**). The control-voltage-input stage, IC_{1A}, is an inverting amplifier with a gain of negative one. This stage makes the control-voltage range over the positive side of 0V. In this example, the control-voltage input ranges from 0 to 2V full-scale. The control

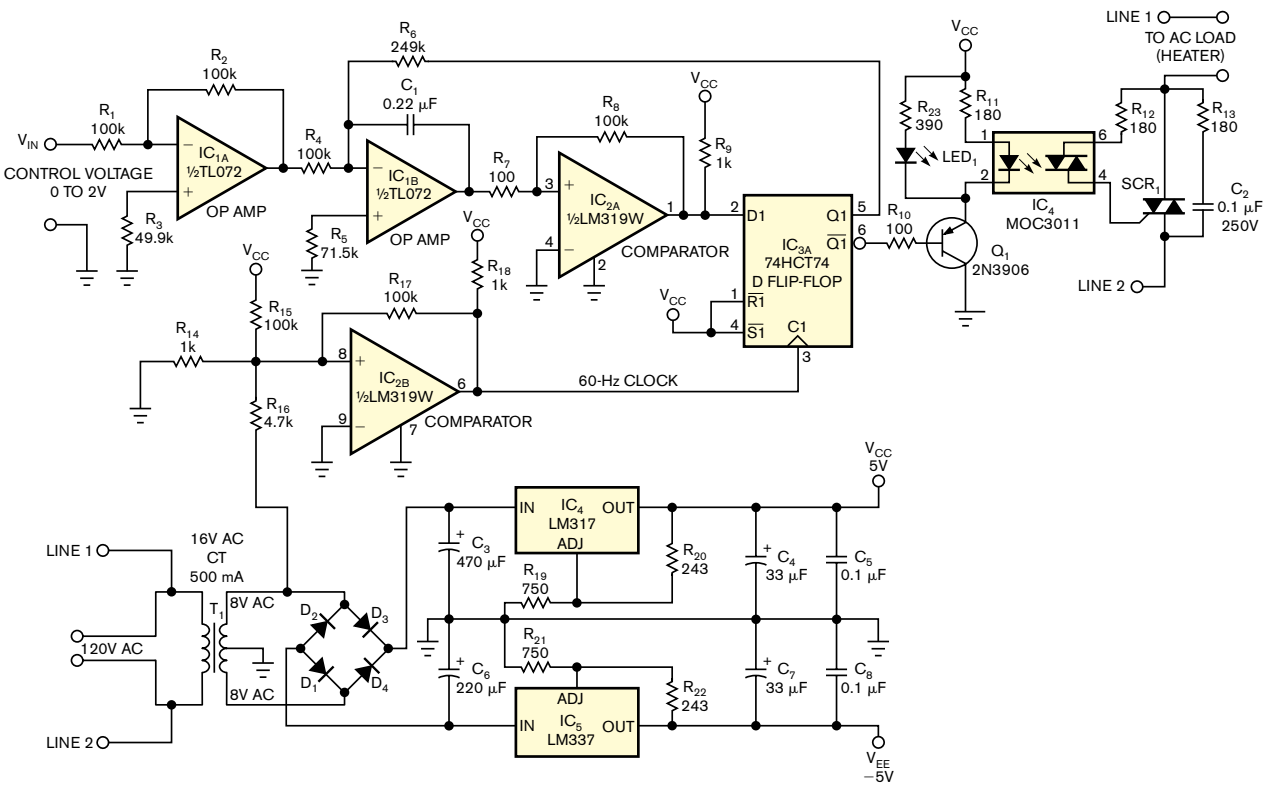

Figure 1 This ac controller borrows from a sigma-delta converter to output a number of whole cycles of ac-line power according to an input-control voltage.

voltage's input impedance is 100 kΩ.

The next stage, IC_{1B}, is an integrator. The integrator output ramps either up or down depending on the polarity of the input current. The speed at which it ramps depends on the magnitude of the input current. The integrator is the heart of the delta-sigma modulator. It forces a balance, on the average, between the control-voltage current in R_4 and the feedback current in R_6. In other words, the duty cycle of the output of IC_{3A}, a CMOS D-type flip-flop, must match the control-voltage percentage of full-scale.

Comparator IC_{2A} detects whether the integrator's output is positive, thus requiring more feedback current, or negative, thus requiring less feedback to maintain the balance. The output of the comparator switches between 0 and 5V. The flip-flop latches the comparator's decision on the next rising edge of the 60-Hz clock.

PNP transistor Q_1 and optoisolated SCR (silicon-controlled rectifier) IC_4 drive load-switching SCR_1 into conduction whenever the flip-flop provides feedback current to the integrator. Indicator LED_1 lights when the load SCR is on. The secondary of transformer T_1 detects the zero crossings of the ac-power line; these crossings provide the 60-Hz clock. The output of comparator IC_{2B} switches high during the positive half-cycles of the ac line and low during the negative half-cycles. Resistor R_{15} provides a small positive bias, causing the edges of the 60-Hz clock to occur slightly early—which is better than late in this case. If you turn off the SCR too late, its self-latching nature may cause it to stay on for an extra half-cycle when it should have been off.

IF YOU TURN OFF THE SCR TOO LATE, ITS SELF-LATCHING NATURE MAY CAUSE IT TO STAY ON FOR AN EXTRA HALF-CYCLE WHEN IT SHOULD HAVE BEEN OFF.

Both comparators IC_{2A} and IC_{2B} use a small amount of hysteresis to promote fast, clean switching. The remaining components generate the regulated 5 and −5V power supplies. Transformer T_1 and optoisolator IC_4 provide isolation from the ac-power line.

This Design Idea works well for an application such as a spa-heater control but does not work for light-dimming or motor-speed control because the output power is pulsating in nature. You can easily adapt the design for 240V-ac or 50-Hz operation. EDN

Extend monolithic programmable-resistor-adjustment range with active negative resistance

W Stephen Woodward, Chapel Hill, NC

A variety of solid-state, in-circuit-programmable replacements exist for the traditional electromechanical trimmer potentiometer. These replacements have many obvious advantages, such as automatic adjustability, miniaturization, and immunity to vibration. But these devices, unlike humble mechanical potentiometers, have relatively large minimum programmable resistance. Although you can adjust a typical trimming potentiometer down to a fraction of 1Ω, solid-state-potentiometer substitutes usually bottom out at 10s, 100s, or even 1000s of ohms. This limitation can sometimes be problematic and frequently precludes use of the solid-state option in some design applications.

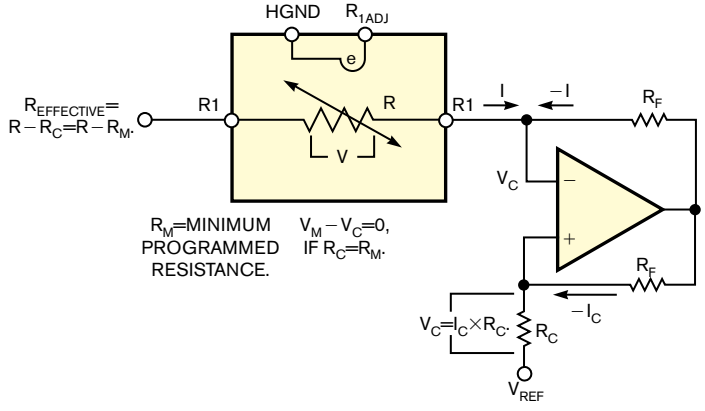

Figure 1 This circuit uses an op amp in a negative-resistance topology that, in effect, subtracts the minimum programmable resistance from the total programmed resistance.

The Rejustor family of devices, which Microbridge (www.mbridgetech.com) recently introduced, provides an extreme example of this effect. You can program a typical Rejustor over only a narrow span of 30%. For example, you can program a 10-kΩ Rejustor to no lower than 7 kΩ, imposing a serious and obvious obstacle to general-purpose application of these devices. **Figure 1** suggests a generally applicable workaround that works not only with Rejustors, but also with all adjustable resistances. It uses an op amp in a negative-resistance topology that, in effect, subtracts R_{MIN} (minimum programmable resistance) from the total programmed resistance. EDN

1-Wire network controls remote SPI peripherals

Michael Petersen, Maxim Integrated Products, Colorado Springs, CO

Many 1-Wire-compatible peripherals are available, but, for those that lack the 1-Wire capability, the circuit in **Figure 1**, pg 80, illustrates one way to implement it. The example controls a remote LED display by the 1-Wire network through an SPI (serial-peripheral-interface)-compatible display controller.

To produce the three-wire SPI that a MAX7221 display controller requires for the $\overline{CS}$ (chip-select), DIN (serial-data), and CLK (clock) signals, the 1-Wire network serially addresses three DS2405 1-Wire switches. The first switch directly creates $\overline{CS}$; the second switch directly creates DIN; and the third switch, aided by three exclusive-OR gates, creates CLK.

The edge detector and one-shot IC_{4A}, IC_{4B}, and IC_{4C} combine the outputs of IC_2 and IC_3—Data 1 and Data 0—to create a clock signal for the SPI. This one-shot clock-generation circuit improves the data rate by requiring only a single 1-Wire transaction per SPI bit, instead of the three transactions—data, clock low, and clock high—that would be necessary if you directly use the IC_3 output as a clock signal.

To transmit data to the SPI inputs, first set the output of IC_1 low. Then, transmit the data bits using the following rules: If the current data bit differs from the previous bit, set IC_2's Data 1 output accordingly. If the current data bit is the same as the previous bit, toggle IC_3's Data 0 output. The circuit automatically generates a clock pulse each time and requires only one 1-Wire command for each data bit sent. When data transmission is complete, send a final 1-Wire command to set the IC_1 output high.

This circuit allows a 1-Wire network to control a remote temperature display, but similar techniques can provide an interface to I^2C (inter-integrated-circuit)-compatible devices and to other SPI peripherals, such as ADCs and DACs. You can also produce a bidirectional-data capability by adding a fourth DS2405. Note that the SPI data rate and updates to the peripheral are relatively slow, but speed is not an issue for many remote-monitoring applications. EDN

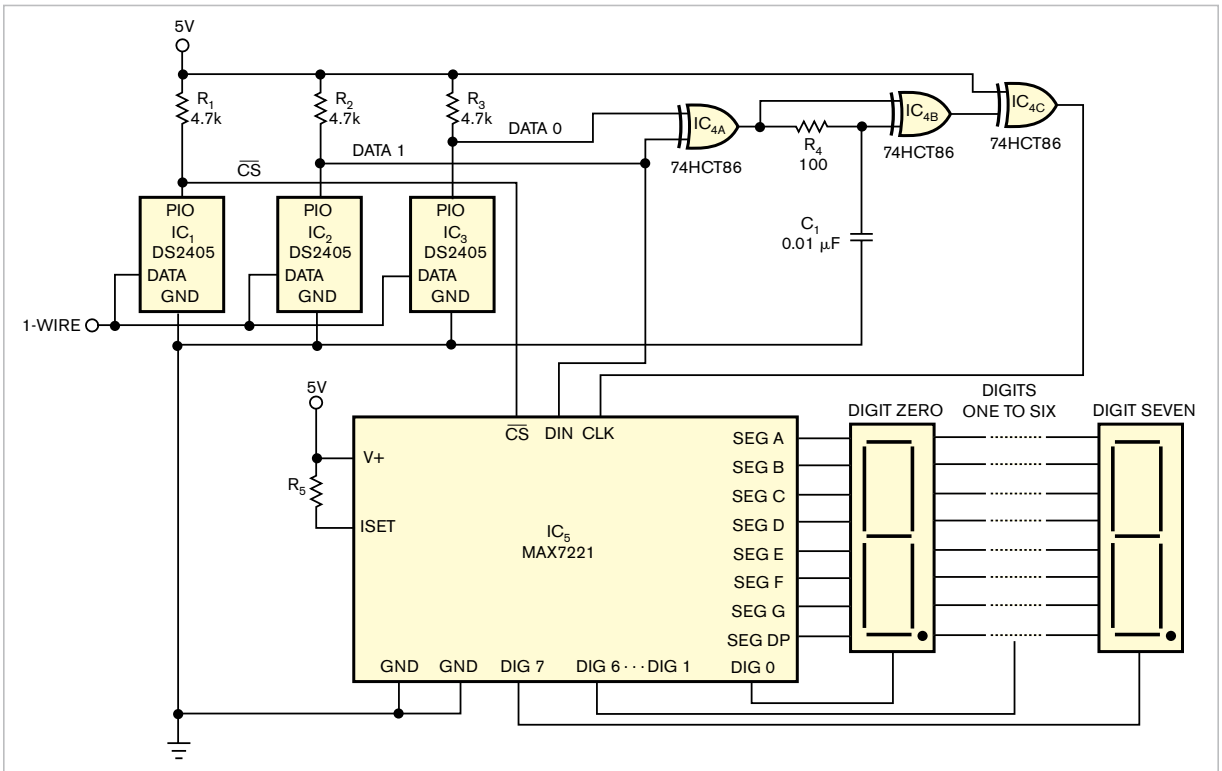

Figure 1 Three 1-Wire switches–IC_1, IC_2, IC_3; three XOR gates, IC_4; and the associated components enable a 1-Wire network to control this display through the SPI peripheral IC_5.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Add margining capability to a dc/dc converter

Brian Vasquez, Maxim Integrated Products, Dallas, TX

You can easily add margining capability—that is, the ability to digitally adjust the output voltage—to a dc/dc converter by making a single connection to the circuit (**Figure 1**). The dashed line in the **figure** shows the connection. The extra IC is a two- or four-channel, I²C (inter-integrated-circuit)-adjustable-current DS4402 or DS4404 DAC. Because each DAC output is 0 mA at power-up, the extra circuitry is essentially transparent to the system until you write a command using the I²C bus.

For example, assume that the input voltage is 3 to 5.5V; the output voltage is 1.8V, which is the desired nominal output voltage; and the feedback voltage is 0.6V. You can obtain the feedback voltage from the dc/dc converter's data sheet; be sure to verify that it is within the output-voltage range that the current DAC's data sheet specifies as sinking or sourcing voltage depending on whether you are sinking or sourcing current. You should also verify the input impedance of the dc/dc converter's feedback pin. The circuit in **Figure 1** assumes a high impedance.

Assume that you want to add a ±20% margining capability to the dc/dc converter's output so that the maximum, nominal, and minimum output voltages would be 2.16, 1.8, and 1.44V, respectively. First, determine the necessary relationship between R_1 and R_2, which yields the nominal output when the current of the DS4404 DAC is 0 mA:

$$V_{FB} = V_{OUTNOM}\left(\frac{R_2}{R_2+R_1}\right), \quad (1)$$

where V_{FB} is the feedback voltage and V_{OUTNOM} is the nominal output voltage. Solving for R_1,

$$R_1 = R_2\left(\frac{V_{OUTNOM}}{V_{FB}}-1\right). \quad (2)$$

For this example,

$$R_1 = R_2\left(\frac{1.8V}{0.6V}-1\right)=2\times R_2. \quad (3)$$

Summing the currents at the feedback node derives the current to make the output voltage increase to the maximum output voltage:

$$I_{R1} = I_{R2} + I_{DS4404}, \quad (4)$$

where I_{R1} is the current through R_1, I_{R2} is the current through R_2, and I_{DS4404} is the current into the DAC.

$$I_{DS4404} = I_{R1} - I_{R2}. \quad (5)$$

$$I_{R1} = \left(\frac{V_{OUTMAX}-V_{FB}}{R_1}\right); I_{R2} = \left(\frac{V_{FB}}{R_2}\right), \quad (6)$$

where V_{OUTMAX} is the maximum output voltage.

$$I_{DS4404} = \left(\frac{V_{OUTMAX}-V_{FB}}{R_1}\right) - \left(\frac{V_{FB}}{R_2}\right). \quad (7)$$

You can simplify **Equation 7** by solving **Equation 1** for R_2 and then substituting, which yields:

$$I_{DS4404} = \frac{V_{OUTMAX}-V_{OUTNOM}}{R_1}. \quad (8)$$

In margin percentage, you can express **Equation 8** as:

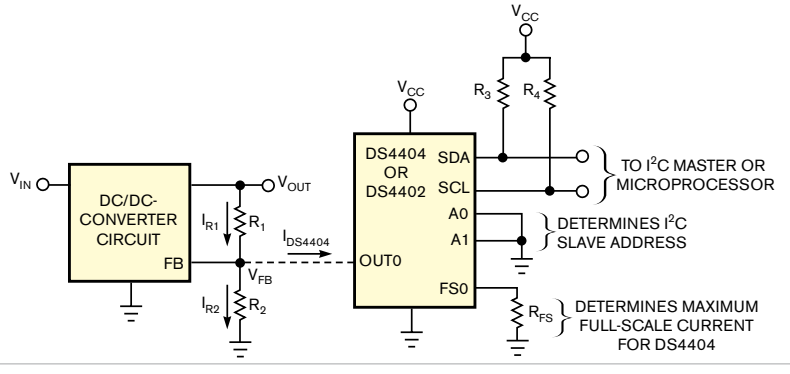

Figure 1 The circuitry to the right of the dashed line adds margining capability.

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$$I_{DS4404} = \frac{V_{OUTNOM} \times MARGIN}{R_1}, \quad (9)$$

where the margin is 0.2 to implement ±20% margining in this case. Before you can use this relationship to calculate R_1 and R_2, you must select the full-scale current.

According to the DS4404's data sheet, the full-scale current must be 0.5 to 2 mA to guarantee the specifications for accuracy and linearity. Unfortunately, no formula is available for calculating the ideal full-scale current. The desired number of steps, the step size, and the values for R_1 and R_2 influence that value. Another factor affecting the full-scale current value is whether there is a requirement that a particular register setting corresponds to a particular margin percentage.

In any case, your selection of a full-scale current will likely require several iterations, in which you select an arbitrary value within the range and then calculate R_1, R_2, R_{FS} (full-scale resistance), and step size. When you've determined an acceptable full-scale-current value, you may want to further adjust it or some of the resistor values to ensure that the resistor values you finally specify are commonly available.

To calculate R_1 for the original example, make the full-scale current equal to the current of the DS4404. This step gives you 31 equal increments, or steps, from the nominal output voltage to the maximum output voltage, as well as 31 steps from the nominal output voltage to the minimum output voltage. This resolution is more than adequate for this example.

You could, for instance, begin by arbitrarily choosing the full-scale current in the center, or 1.25 mA, of the specified range and then performing all the calculations. Instead, for illustrative purposes, the calculations are shown for the endpoints of the range: 0.5 and 2 mA. Analyzing the 0.5-mA case first, you perform the following calculations and then repeat for the 2-mA case.

Using **Equation 9** and solving for R_1 yields:

$$R_1 = \frac{V_{OUTNOM} \times MARGIN}{I_{DS4404}} = \frac{1.8 \times 0.2}{0.5 \times 10^{-3}} = 720\Omega. \quad (10)$$

$$R_2 = \frac{R_1}{2} = \frac{720}{2} = 360\Omega. \quad (11)$$

To calculate the full-scale resistance, use the formula and the reference voltage in the DS4404's data sheet:

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{0.5 \times 10^{-3}} \times \frac{31}{4} = 19{,}065\Omega \approx 19\ k\Omega. \quad (12)$$

$$STEP\ SIZE = \frac{I_{FS}}{NO.\ OF\ STEPS} = \frac{0.5 \times 10^{-3}}{31} = 16.1\ \mu A/STEP, \quad (13)$$

where R_{FS} is the full-scale resistance, V_{REF} is the reference voltage, and I_{FS} is the full-scale current.

Finally, for completeness, you determine the DS4404's output current as a function of register setting:

$$I_{OUT}(REGISTER\ SETTING) = STEP\ SIZE \times REGISTER\ SETTING. \quad (14)$$

Note that this register setting does not include the sign bit, which selects sink or source. The DS4404 sinks current when the sign bit is zero, making the output voltage increase to the maximum output voltage. It sources current when the sign bit is one, making the output voltage decrease toward the minimum output voltage.

Now, you can repeat the calculations for the 2-mA case.

$$R_1 = \frac{V_{OUTNOM} \times MARGIN}{I_{DS4404}} = \frac{1.8 \times 0.2}{2 \times 10^{-3}} = 180\Omega. \quad (15)$$

$$R_2 = \frac{R_1}{2} = \frac{180}{2} = 90\Omega. \quad (16)$$

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{2 \times 10^{-3}} \times \frac{31}{4} = 4766\Omega \approx 4.7\ k\Omega. \quad (17)$$

$$STEP\ SIZE = \frac{I_{FS}}{NO.\ OF\ STEPS} = \frac{2 \times 10^{-3}}{31} = 64.5\ \mu A/STEP. \quad (18)$$

Comparing R_1 and R_2 for the two cases—with a full-scale current of 0.5 or 2 mA—0.5 mA is the more attractive value because the resistances are higher. EDN

A better approach to designing an RTD interface with a spreadsheet

Aubrey Kagan, Emphatec, Markham, ON, Canada

An earlier Design Idea described how to linearize the output of an RTD (resistance-temperature-detector) sensor and how to calculate the resistor values using a spreadsheet (**Reference 1**). That idea limited the use of Microsoft (www.microsoft.com) Excel to calculating the coefficients you need for the polynomial expression and stopped short of using Excel to calculate the resistor values. You can generalize this proposed approach such that you can select any type of RTD and any temperature range, but this Design Idea limits the details to the following example.

You can download the worksheet (**Figure 1**) from the Web version of this Design Idea at www.edn.com/080918di1. You plot the chart as an XY diagram, and you create the trend line on the chart using a second-order polynomial, which will appear on the chart. The original Design Idea included this information. Unfortunately, you cannot access the coefficients you generate in this way from the worksheet, so you cannot directly calculate the resistor values.

To access the polynomial coefficients, you can use Excel's LINEST

array formula. It prescribes a specific way of entering data; without that protocol, Excel will not provide the desired results. LINEST returns a number of regression statistics; to allow for these statistics, you must first highlight the range on the worksheet on which you want the regression results. Only the polynomial coefficients are important in this example, so this Design Idea limits the returned results by selecting block B24:D24 for those three values. You then enter the following line into the formula bar at the top of the worksheet:=LINEST(G5:G21,E5:F21,,TRUE).

Simultaneously press the Control, Shift, and Enter keys rather than just Enter to terminate this command. The coefficients will then drop into the selected range. Excel will add the braces, { }, to indicate the array formula. The input range of the function in the formula above includes the Vt^2 column, allowing LINEST to create a second-order polynomial equation.

You can enter user-selected values as set numbers, providing easy and quick modification and an immediate update of the calculated values. These values include the current source through the RTD, the reference voltage, and the value of R_7 and R_9, all of which are "named" cells that the formulas refer to. The idea rewrites the original formulas to isolate the desired variable. You will find each in the associated cells for R_6, R_8, and R_{10} on the worksheet. You could also complete the model by creating an automatic look-up of standard resistor values (**Reference 2**).EDN

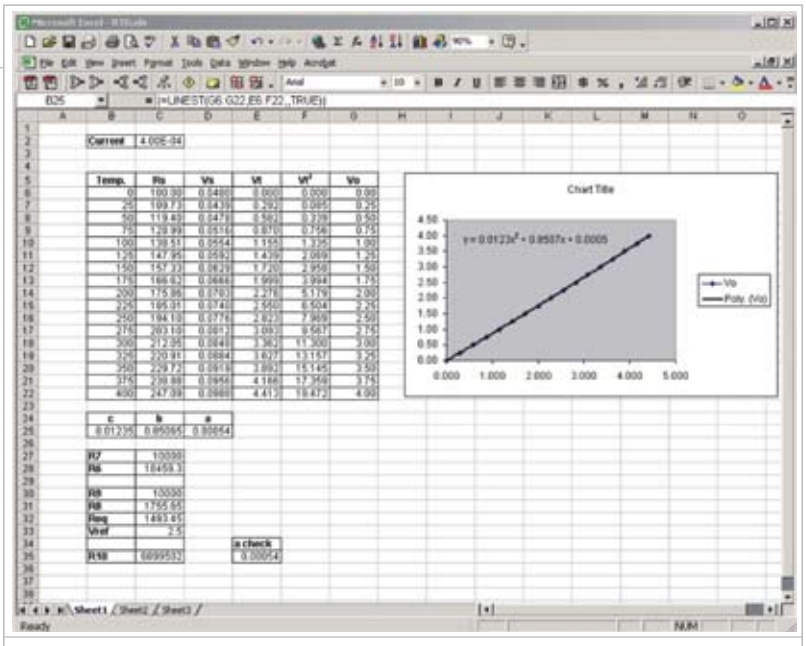

Figure 1 The linearizing values of an RTD circuit accompany a graph of the output voltage.

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2 Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Elsevier/Newnes, May 2004, ISBN 0750677562.

Shunt regulator monitors battery voltage

Vladimir Rentyuk, Modul-98 Ltd, Zaporozhye, Ukraine

A TL431 shunt regulator is a perfect choice for many applications. You can use it as a comparator with hysteresis by taking advantage of its inner voltage reference along with few additional components. You can use this comparator with hysteresis, like a Schmitt trigger, as a simple battery monitor (**Figure 1**). You calculate the threshold voltage, V_{T+}, of this comparator as $V_{T+}=V_{REF}\times(1+R_1/R_3)$, where V_{REF}, the internal reference voltage of shunt-regulator TL431, is 2.5V.

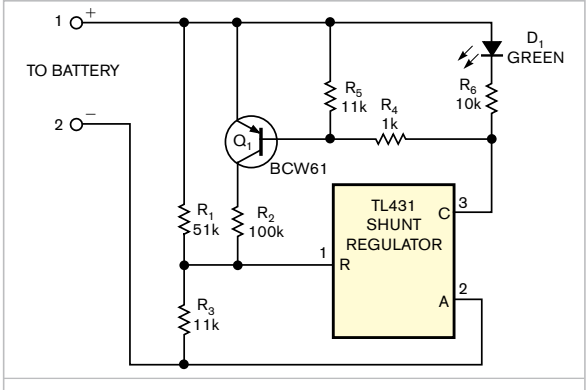

Figure 1 A shunt regulator and associated circuitry function as a Schmitt trigger, lighting LED_1 when the battery is fully charged.

When the battery voltage is higher than the threshold voltage, the cathode voltage of the TL431 is at its low level of approximately 2V, and transistor Q_1 turns on, lighting LED_1. You calculate the release voltage, V_{T-}, of the trigger as $V_{T-}=V_{REF}\times(1+R_1\times R_2/(R_1+R_2)\times 1/R_3)$.

When the battery voltage is less than the release voltage, the cathode voltage of the TL431 goes to its high level—to the battery voltage. Transistor Q_1 turns off, and LED_1 does not shine. LED_1 turns on again when the battery voltage, after recharging, exceeds the threshold voltage.EDN

Power supply meets automotive-transient-voltage specs

Francesc Casanellas, Aiguafreda, Spain

Figure 1 shows a power supply that delivers 5V from a 12V battery. With only a few components, the supply copes with all the automotive transients that ISO (International Organization for Standardization) 7637-1 lists without the need for a bulky transient-voltage suppressor. In normal operation, R_3 connects to the common through a microcontroller port. In standby mode, R_3 stays open, and the quiescent current of the supply decreases from approximately 2.8 mA to approximately 160 µA, and the output voltage then drops to approximately 3.5V. If your application doesn't require a standby mode, suppress R_3 and set R_5 to 220Ω. With most common zener diodes, you would then set R_5 to 120Ω and D_1 to 4.3V. You can use the circuit in 24V systems if D_2 is 36V.

If the voltage increases, the current through D_1 and the base of Q_3 increases, so Q_3 increases the current of Q_2, which lowers the gate-to-source voltage of Q_1. If the input voltage surpasses 19V, D_2 starts to conduct and makes Q_2 switch off Q_1, so permanent overvoltages as high as 200V cannot damage the circuit. The Miller capacitance of Q_1 makes it act as a fast integrator, which keeps the system stable. If you remove D_2, you must replace Q_3 with a high-voltage transistor, such as an MMBTA42.

If you omit D_2, the circuit cannot withstand permanent overvoltages without Q_1's overheating. In this case, however, the circuit can cope with all the impulses, including the load-dump pulse, of ISO 7637-1. You should remove D_2 only if C_1 cannot maintain the voltage during long overvoltages, such as the load-dump pulse, and keeping the voltage is critical.

An added advantage of this circuit over most IC-voltage regulators is that it can sink current through D_1 and Q_3. This feature allows the use of diodes to fully protect the microprocessor's inputs. Soldering the D-Pack package to a couple of 1-cm^2 copper pads allows the circuit to source 300 mA at 10 to 16V or 150 mA at 20 to 32V. More dissipation area allows for higher currents. EDN

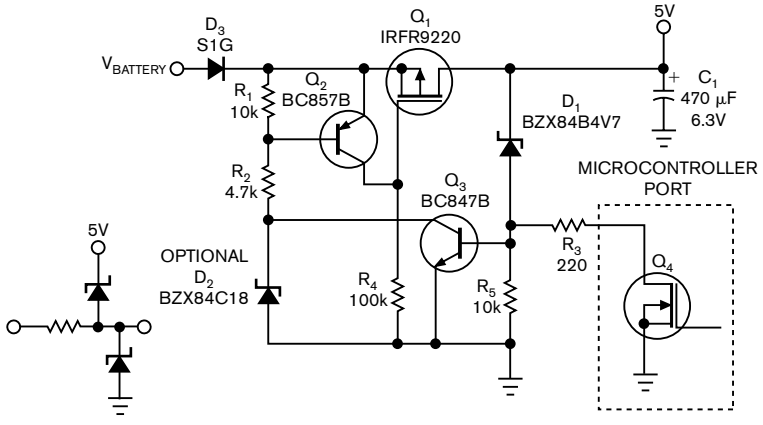

Figure 1 This automotive regulator withstands overvoltages that ISO 7637-1 specifies.

Locked-sync sine generator covers three decades with low distortion

Alfredo H Saab and Tina Alikahi, Maxim Integrated Products, Sunnyvale, CA

Analog applications, such as testing, calibration, and general system operation, often require a sine waveform of accurate amplitude and frequency, with low THD (total harmonic distortion). Some applications demand that the generator of such waveforms have the ability to accurately synchronize the output with an external timing signal. Simple sine-wave generators can offer various degrees of this performance, but maintaining low THD with constant amplitude is a problem, particularly if the output and the synchronization signal must remain locked through an extended range of frequencies.

The circuit in **Figure 1** can synchronize a sine-wave output through three decades of frequency—20 Hz to 20 kHz—and maintain low THD and constant amplitude (**Table 1**). The synchronizer IC, an NXP Semiconductors (www.nxp.com) 74HC4046, is a PLL (phase-locked loop) with a VCO (voltage-controlled oscillator) and a phase/frequency detector. It has three internal phase detectors, but this design uses the one with a frequency-capture range equal to that of the VCO-frequency range (the maximum frequency minus the minimum frequency).

The circuit's general-purpose binary frequency divider, the 74HC4060, connects between the VCO output and the 74HC4046 feedback (phase/frequency-comparator) input and has a division ratio of 64. When the PLL is locked, therefore, the Q6 output of the 74HC4060 generates a square wave equal to 1/64th of the VCO-output frequency. The components

that determine the 74HC4046 center frequency, C_1 and R_1, determine the VCO-frequency range from 20×64 to 20,000×64 from the minimum to the maximum level of the VCO's input-voltage range.

A switched-capacitor lowpass filter, the Maxim (www.maxim-ic.com) MAX297, whose cut-off frequency by design equals 1/50th of the clock frequency you apply to it, has for signal input the same square wave it uses for the PLL feedback, and its clock input attaches to the VCO output. Because the clock and signal inputs always have a frequency ratio of 64, the input signal always falls within the filter bandpass. No input harmonics fall within this bandpass because the ratio of the clock frequency to frequency is less than 50 for all of them. (For the lowest second harmonic, the ratio is 32.) The THD, up to the 32nd harmonic, is lower than 0.1%.

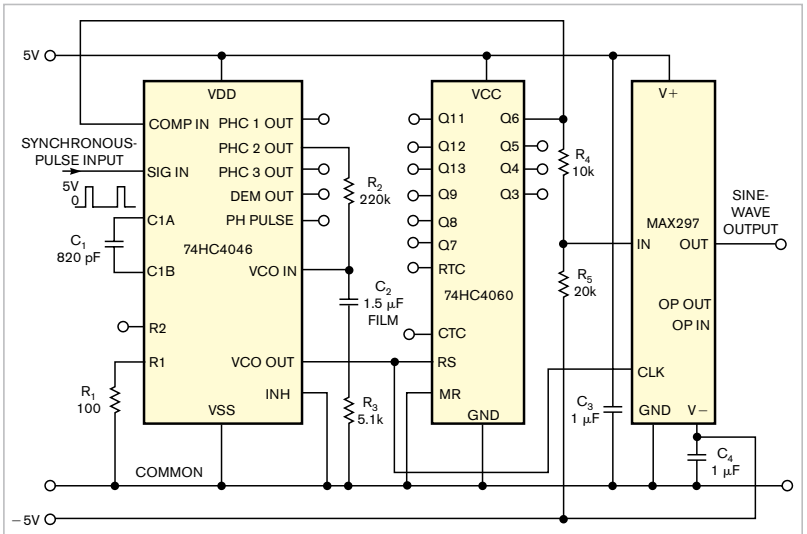

Figure 1 This three-IC sine-wave generator covers three frequency decades, provides low distortion, and allows you to synchronize it with an external signal.

The fact that the filter's input signal is a square wave with a 50% duty cycle helps in this application because a square wave contains only odd harmonics of the fundamental, and the lowest-frequency harmonic is the third, which is well within the filter's deep-attenuation range.

You can frequency-modulate the synchronization signal, but that task entails a compromise between the synchronization-tracking speed (or maximum modulation frequency and depth) and the frequency-locking range, which the PLL's lowpass filter components, R_2, R_3, and C_2, set. Modulation speed is limited for the values the **figure** shows because those values are optimized for an extended-frequency locking range. You can download more information, including a full data sheet for the MAX297, from www.maxim-ic.com **(Reference 1)**.EDN

TABLE 1 AMPLITUDE VERSUS FREQUENCY

Frequency (Hz)	Amplitude (V rms)
20	1.470
50	1.472
100	1.472
200	1.473
500	1.473
1000	1.473
2000	1.472
5000	1.473
10,000	1.473
20,000	1.472

REFERENCE

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READERS SOLVE DESIGN PROBLEMS

Use an LM317 as 0 to 3V adjustable regulator

Vladimir Rentyuk, Modul-98 Ltd, Zaporozhye, Ukraine

Most engineers know that they can use an inexpensive, three-terminal adjustable regulator, such as Fairchild Semiconductor's (www.fairchildsemi.com) LM317, as an adjustable regulator to only some necessary value of voltage, such as 36 or 3V. This value cannot be less than 1.25V without employing other approaches, however. The devices' inner reference voltage is 1.25V, and their output voltage accordingly cannot be less than this value without potential bias (**Reference 1**). One way to solve this problem is to use a reference-voltage source based on two diodes (**Reference 2**). Although this approach is suitable for a 1.2 to 15V or higher-voltage regulator, it is not appropriate for an extra-low-voltage fixed- or adjustable-voltage regulator. The two 1N4001 diodes it employs do not provide the needed potential bias of 1.2V, and they have additional temperature instability of approximately 2.5 mV/K (**Reference 3**). Hence, additional temperature drifting of the output voltage is approximately 100 mV; it is more than 6% for a 1.5V output voltage and 10% for a 1V output voltage if you adjust the temperature to 20°C—a typical indoor situation. You can solve these problems by using a Fairchild Semiconductor LM185 or an Analog Devices (www.analog.com) AD589 adjustable-voltage-reference IC. These devices are expensive, however, and, in this case, they require not only additional zero adjustment but also matching. These adjustments at their reference voltages are 1.215 to 1.255V and 1.2 to 1.25V for the LM185 and AD589, respectively. Note that the reference voltage of the LM317 is 1.2 to 1.3V.

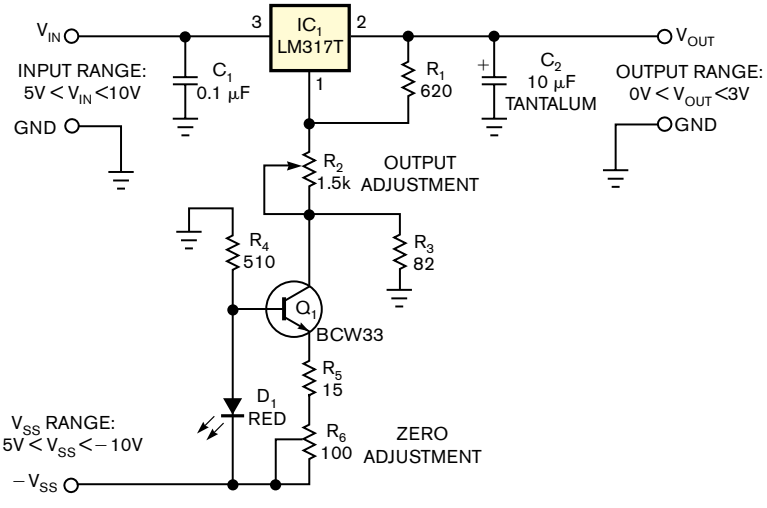

Figure 1 This circuit is an inexpensive approach using a simple 0 to 3V adjustable regulator.

Figure 1 shows an inexpensive approach using a simple 0 to 3V adjustable regulator. You implement the necessary potential bias using a simple temperature-stabilized constant-current source (**Reference 4**). You calculate this current source using the following **equation**: $I=(V_F-V_{EBO})/(R_5+R_6)$, where V_F is D_1's forward voltage of approximately 2V and V_{EBO} is Q_1's emitter-base voltage of approximately 0.68V. The current is approximately $1.32/(R_5+R_6)$. The constant-current source creates a bias voltage of approximately −1.25V on resistor R_3. You implement the zero adjustment using resistor R_6, which can change the current of the constant-current source. Resistor R_5 protects transistor Q_1. You can use D_1 as a light indicator. You can adjust the output voltage using resis-

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tor R_2. Calculate the output voltage as follows: $V_{OUT}=V_{REF}(1+R_2/R_1)-V_{R3}$, where V_{REF} is the reference voltage of IC_1 and V_{R3} is some compensative voltage of resistor R_3. You should establish this voltage to equal the reference voltage for its compensation. In this case, $V_{OUT}=V_{REF}(R_2/R_1)$. With R_2 having a value of 1.2 kΩ, this circuit found use as the equivalent of a typical battery with an output voltage of 1.56V for development projects. EDN

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Alarm monitors rotational speed of dc motor

Peter Demchenko, Vilnius, Lithuania

You can use the circuit in **Figure 1** to monitor the rotating speed of a dc fan motor and sound an alarm if the motor stalls. One potential application of the circuit is monitoring the CPU-fan speed in a PC in which overheating the CPU can ruin the whole system. A PC BIOS (basic input/output system) often has a limited capability for monitoring the speed of CPU or chassis fans during boot-up. Moreover, if you enable the CPU-fan-protection function of BIOS today, you can have a problem with it tomorrow: If the fan's starting acceleration slows down, the BIOS powers down the PC at the beginning of the boot sequence, not allowing you to go into BIOS settings to correct the situation. So, the manual often advises you to disable this fan function. The circuit in **Figure 1** shows how to implement continuous monitoring and sound an alarm and automatically power off the system if a fan problem occurs.

The impulses on R_1, arising from commutation in the fan's brushless motor, start up the Schmitt trigger, Q_1/Q_2, which controls transistor switch Q_3, commutating the sense pin of the fan's motherboard connector; the frequency of commutation is proportional to the rotation speed. Optionally, the output of the trigger resets the timer with two time-out periods; the expiration of the first time-out activates the alarm buzzer.

After the second time-out, transistor Q_5 powers down the PC with or without the relay switch. The relay switching is more consistent, is less prone to interference, and is preferable when the distance between this circuit and the power-switch connector on the motherboard exceeds 20 to 30 cm. You must connect the collector of Q_5 or the contacts of the relay in parallel with the power-switch button. The alarm circuit comprises Q_4 and a three-terminal piezoelectric buzzer. EDN

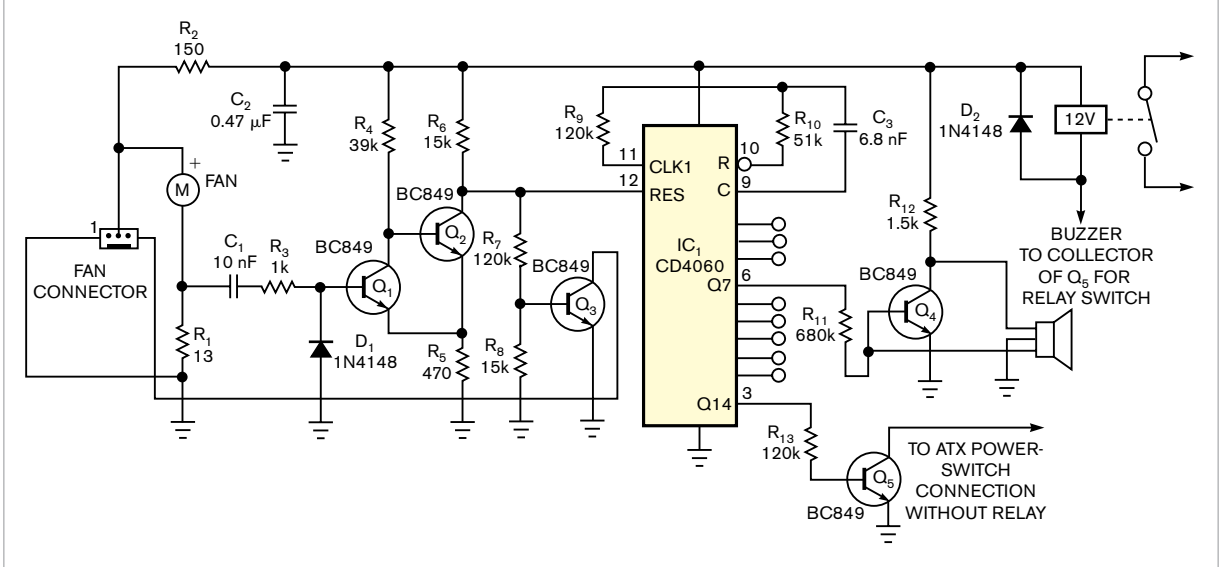

Figure 1 This circuit provides an optional audible alarm after a time-out when a brushless-dc fan motor slows down. Then, after a second time-out, the circuit powers down the PC.

Add charging status to simple lithium-ion charger

Peter T Miller, Applied Inspirations, Bethlehem, CT

Like other simple, single-cell lithium-ion battery chargers, Microchip's (www.microchip.com) MCP73812 provides no means of indicating the charging status. You can remedy this situation by adding four components (**Figure 1**). Add one more LED, and you also get a charging-complete indication. This two-LED configuration has the added benefit that one of the LEDs is always on, providing an indication that the charger is powered.

While the cell is in the constant-current charging mode, 401 mA flows through the 1N4001 diode, D_1. The additional 1 mA is the supply current of the control chip. Because the 1N4001 conducts before the base-emitter junction of Q_1, it prevents Q_1 from turning on until the forward voltage across it reaches about 450 mV. Q_1 then starts to conduct and turns on D_2, a red LED that indicates charging. Because the forward-voltage drop for a green LED is typically higher than that of a red LED—2.1 versus 1.7V—the voltage across D_2 and Q_1 is less than the turn-on voltage of the green LED, D_3, and it remains off.

For the last part of the charging cycle, the controller switches to constant-voltage mode. As the cell voltage gets closer to this 4.2V terminal voltage, the current through D_1 drops, and at 15 to 40 mA, both LEDs illuminate.

Tests measured this range for several 2N3904 transistors. Testing with 2N4401s gave a lower range of 4 to 18 mA. When the current drops below about 15 mA, Q_1 turns off D_2. The voltage across D_3 now rises above its forward-voltage threshold, and the green charging-completed LED lights. EDN

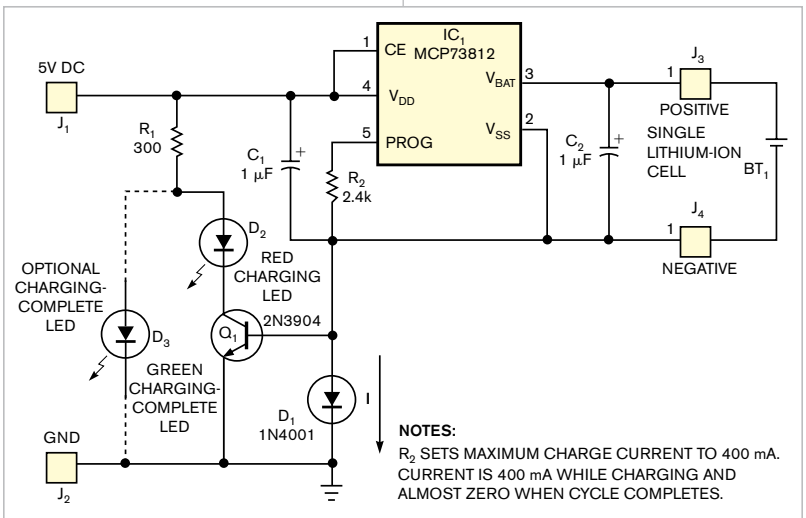

Figure 1 Adding a few components to a lithium-ion cell charger provides an indication of charging status.

555 timer drives multiple LEDs from one NiMH cell

Chuck Irwin, Hendersonville, NC

Using a CMOS 555 timer and a single NPN transistor, you can drive as many as seven LEDs using a minimal amount of voltage and power from a single NiMH (nickel-metal-hydride) AA cell. The circuit works by creating much higher-voltage pulses than the voltage for powering the circuit by pulsing a high-Q power inductor. The circuit

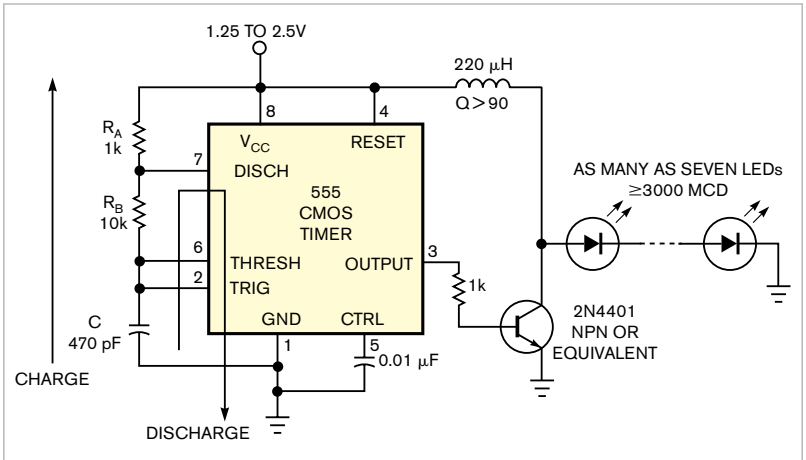

Figure 1 Using a CMOS 555 timer configured as a switching power supply, you can drive seven high-brightness LEDs from a single 1.25V cell.

creates voltage pulses of 23V using a 1.25V NiMH cell with seven connected LEDs.

The circuit uses a CMOS timer because it functions on low voltages—in this case, as low as 1V. A single white LED rated at 9300 mcd maintains its brilliance down to this low voltage. The circuit works for 192 hours using a 2000-mAHr-rated NiMH cell. The output of the timer is a 4.5-µsec pulse repeating at a 222-kHz rate. Although you can use the circuit to power any LED, it works best using high-brightness, high-power LEDs rated at 3000 mcd or higher. Obviously, the higher the millicandela rating, the brighter the LED will appear.

You can connect the LEDs in parallel if their forward voltages match; otherwise, the LED with the lowest forward voltage will dim out the other LEDs. Using the parallel connection, all LEDs will glow with equal brightness if their forward voltages match. Adding LEDs does not increase the current drawn from the battery but reduces the brilliance of all of the connected LEDs.

The advantage of connecting the LEDs in series—which is possible because of the high pulse voltage they produce—is equal brilliance of all LEDs, regardless of their individual forward-voltage drops and millicandela ratings. Each additional LED decreases additional voltage and lowers the resulting current into the series string of LEDs, lowering their brilliance. Using seven LEDs with a single 1.25V cell draws a current of only 8 mA. By adding a 1.25V cell to the power input, the LEDs become so brilliant that it is difficult to look at them. With a 2.5V supply, the peak voltage pulses increase to 70V with no connected LEDs. With the LEDs connected, the output voltage peaks at 25V. Current draw at 2.5V is 20 mA. EDN

Microcontroller inputs parallel data using one pin

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

Inputting multiple bits of information using a single entry pin of a microcontroller without the complexity of UARTs can prove useful. Such a scheme could allow scanning of a keyboard, mode switches, or any relatively slowly changing digital data. **Reference 1** details a technique for outputting signals with a single pin. The data from switch bank S_1 first presents itself to IC_3, a 74HC165 parallel-to-serial converter from NXP Semiconductors (www.nxp.com, **Figure 1**). Loading the data into the shift register requires a pulse on the PL line (Pin 1). Line CK accomplishes this pulse by sending as output a long pulse on the microcontroller-pin line. R_2 and C_2 introduce a delay, and, once the pulse exceeds that delay, the PL line goes low, and the data loads.

After the PL signal rises, shorter pulses on the microcontroller's I/O port generate pulses at the shift register's clock input, CP, but not at the PL input. The duration of these clock pulses must be long enough to exceed delay R_1C_1 but not R_2C_2. These clock

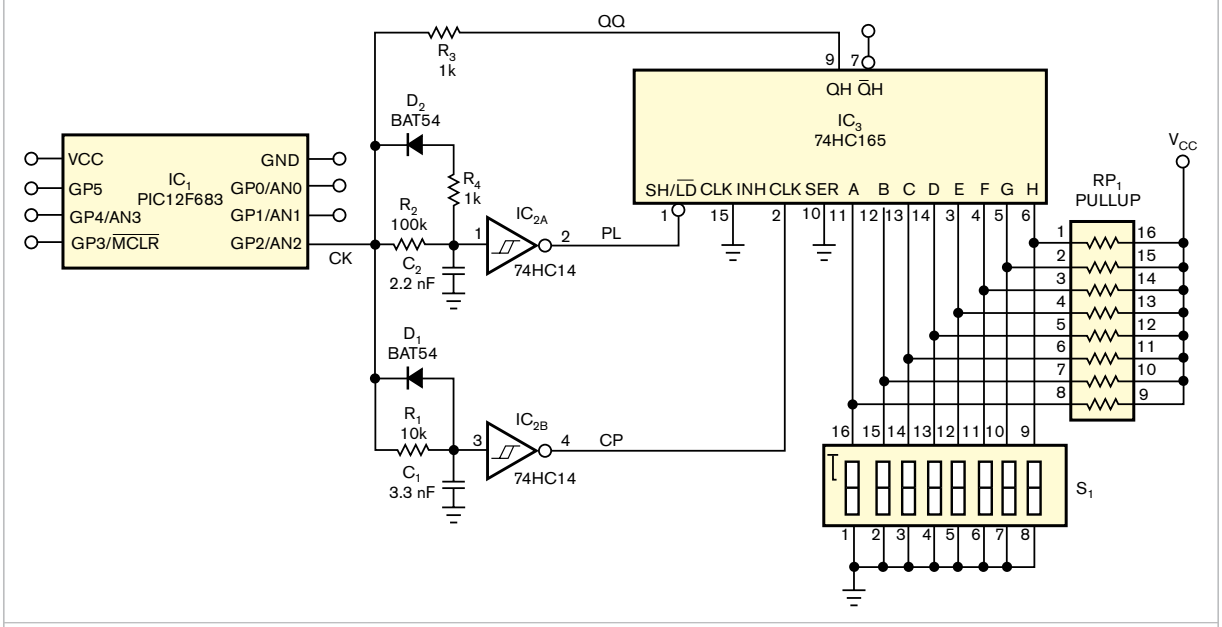

Figure 1 Careful adjustment of the RC time constants allows a microcontroller to input a serial-data stream using a single I/O pin.

pulses shift the data so that the 8 bits appear in sequence at the shift-register output, QQ.

If the microcontroller's data direction briefly changes to input with high impedance, this shift-register data dominates because of the relative values of R_1, R_2, and R_3, with R_3 being a much lower value. The high-impedance state must exist only for a time less than the R_1C_1 time constant (**Figure 2**). The microcontroller now reads the single bit of data. The action of three differing periods generates three functions: load, clock, and data read. The time the microcontrollers need to change port direction, read the pin data, and reset the pin's direction to output determines the timing. For example, a 1-µsec microcontroller requires 10 µsec.

To avoid spurious CP pulses, this time constant must be less than $0.33R_1C_1$, so R_1C_1 could be 30 µsec and R_2C_2 could be 200 µsec. These settings would allow a complete 8-bit read in about 1 msec. To achieve faster operation, replace the RC delays with a precision retriggerable monostable multivibrator, such as NXP's 74HC123, and logic gates. You can expand the scheme with more shift registers to read dozens of signals.

Note that internal logic in the 74HC165 shift register prevents the CP signal from shifting data when LD is active. Resistor R_4 ensures the correct sequencing of LD and CP. Diodes D_1 and D_2 quickly discharge the capacitors to "reset" the delay function of R_1C_1 and R_2C_2. EDN

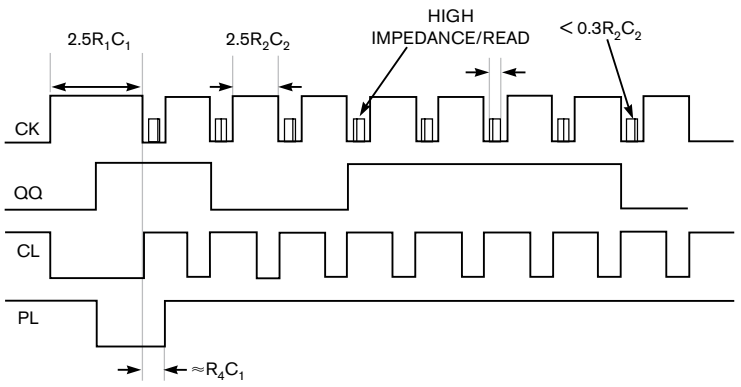

Figure 2 The high-impedance state must exist only for a time less than the R_1C_1 time constant.

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READERS SOLVE DESIGN PROBLEMS

Precision analog bests digital in speed, noise, simplicity, and ease of implementation

Paul Antonucci, Alberti's Window, Watertown, MA

Every once in a while, I read that analog is on the way out, and everything should be digital. Recently, I was involved in a design project that illustrates that this belief doesn't apply in many situations.

The problem was to put two new optical breaks into the drive mechanism of a group of robotically controlled, Internet-accessible telescopes in an education application. The drive mechanisms have been showing signs of wear from excess slipping at end of travel: The sensors would signal end of travel, so there would be no slipping. The fork arms and other locations enclosed the internal wiring harnesses of the telescopes so that rewiring the telescopes would have been awkward.

So, the best idea was to encode the signals from the new sensors into the current wiring. There was one digital signal available; the challenge was to encode the two new sensors onto that signal.

Using a digital approach would have involved adding a small microcontroller to the base and encoding a serial digital signal to send up the tube, with appropriate synchronous pulses, data, and check sums, which then would undergo decoding at the CPU. This approach would have required some sort of reset provision because the telescope needed to operate independently for months, and those serial digital signals would have undesirable switching noise on them. The CPU would also have had to spend time grabbing, decoding, and synchronizing the signals, taking up more time. In addition, we would have had to have written some messy bit-banging code: not a huge challenge—but not a simple or elegant one, either.

Instead, this approach uses a variation on a simple adder circuit in which each sensor contributes a different amount. Taking the basic binary idea that one sensor adds ±1; the next, ±2; and the last, ±4, the approach uniquely represents each state.

The basic requirements are a voltage reference, some op amps, and a summing junction. This application uses IC_4, a Texas Instruments (www.ti.com) REF3040 voltage reference, which has an output tolerance of 0.2% yet costs only approximately $1 (**Figure 1**). This reference generates a voltage of 4.096V and produces enough current to run the op amps, which run rail to rail to within a few millivolts. Be careful, however: Some "rail-to-rail" op amps have insufficient current drive near the rails. This circuit uses 0.1%-precision resistors, which cost only about 20 cents. Remember that you can use two 10-kΩ resistors in series and two in parallel to create the 20- and 5-kΩ resistances that you see in the **figure**. The assembly and bill of materials are simpler and precision is better because the distributions around the ideal resistor value tend to cancel out. **Table 1** lists the predicted output voltages.

TABLE 1 PREDICTED OUTPUT VOLTAGES

Sensor 1	Sensor 2	Sensor 3	Output
0	0	0	0.256
0	0	1	0.768
0	1	0	1.28
0	1	1	1.792
1	0	0	2.304
1	0	1	2.816
1	1	0	3.328
1	1	1	3.84

Tests with a voltmeter show that all output voltages were within 1 mV of the predicted output values. The error budget of less than 1% shows that you could use this method to encode several more sensors. In the telescope, the CPU's ADC reads the outputs. Read it twice to ensure that you aren't catching it at a transi-

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tion. The advantages of the circuit include the fact that its dc signals ensure that there's no noise and that the updates are nearly instantaneous. Also, because op amps are simple, virtually indestructible, and insensitive to noise, no reset circuits are necessary. Best of all, the design requires no programming. EDN

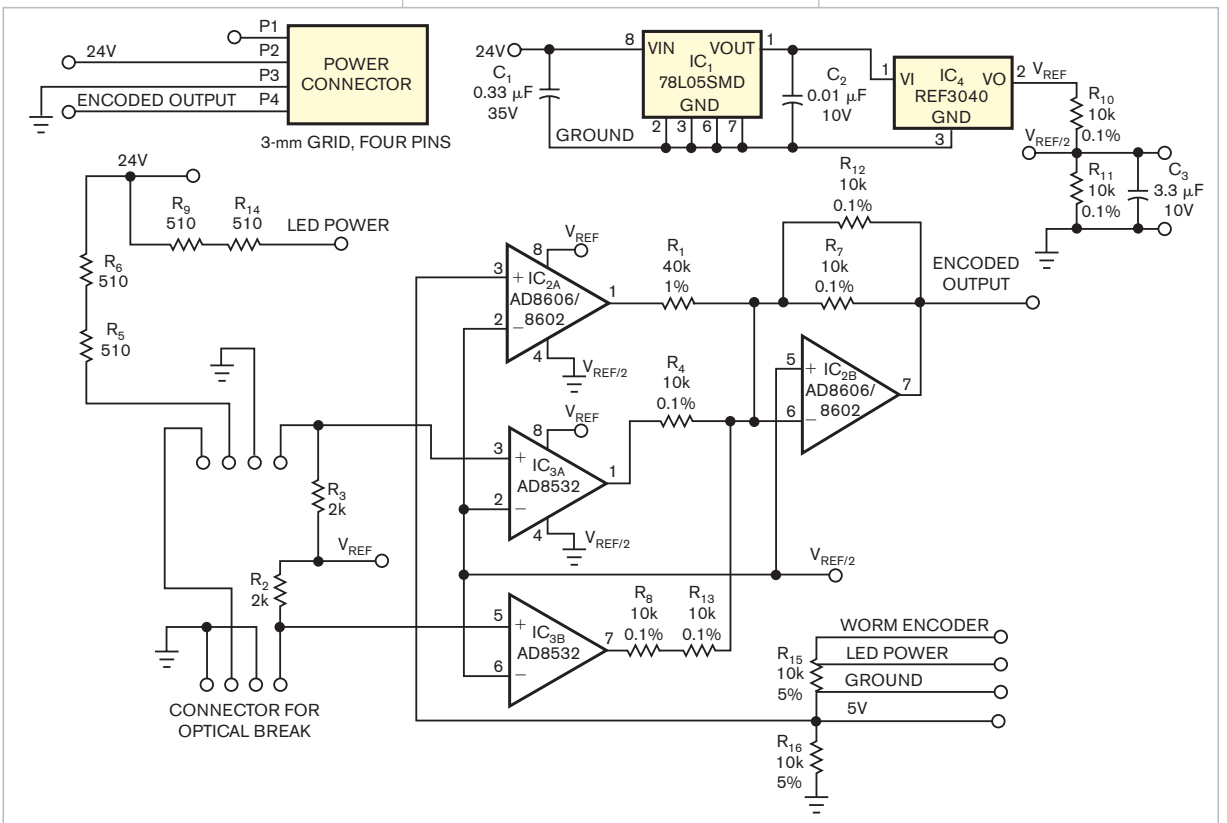

Figure 1 This application uses IC_4, a REF3040 voltage reference, which has an output tolerance of 0.2% yet costs only approximately $1.

Mutliplexing technique yields a reduced-pin-count LED display

Saurabh Gupta and Dhananjay V Gadre,
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"Charlieplexing" as a method of multiplexing LED displays has recently attracted a lot of attention because it allows you, with N I/O lines, to control N×(N−1) LEDs (**references 1** through **5**). On the other hand, the standard multiplexing technique manages to control far fewer LEDs. **Table 1** lists the number of LEDs that you can control using Charlieplexing and standard multiplexing by splitting the available number of N I/O lines into a suitable number of rows and columns. **Table 1** also shows the duty cycle of the current that flows through the LEDs when they are on.

Clearly, Charlieplexing allows you to control a much larger number of LEDs with a given number of I/O lines. However, the downside of this technique is the reduced duty cycle of the current that flows through the LEDs; thus, to maintain a given brightness, the peak current through the LEDs must increase proportionately. This current can quickly reach the peak-current limit of the LED. Nonetheless, Charlieplexing is a feasible technique for as many as 10 I/O lines, allowing you to control as many as 90 LEDs. To control an equivalent number of LEDs using the standard

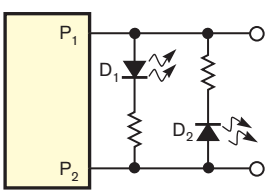

Figure 1 "Charlieplexing" with two I/O lines allows you to control two LEDs.

TABLE 1 NO. OF LEDs AND DUTY CYCLE

No. of I/O lines	Multiplexing-controlled LEDs	Duty cycle with multiplexing (%)	Charlieplexing-controlled LEDs	Duty cycle with Charlieplexing (%)
Two	Two	100	Two	50
Three	Three	100	Six	16.67
Four	Four	50	12	8.33
Five	Six	50	20	5
Six	Nine	33	30	3.33
Seven	12	33	42	2.4
Eight	16	25	56	1.78
Nine	20	25	72	1.38
10	25	20	90	1.11

TABLE 2 OUTPUT VOLTAGE

P_1	P_2	Voltage at node PR_1
0	0	V_{CC}
0	1	V_{CC}
0	Z	V_{CC}
1	0	0
1	1	0
1	Z	0
Z	0	$V_{CC}/2$
Z	1	$V_{CC}/2$
Z	Z	$V_{CC}/2$

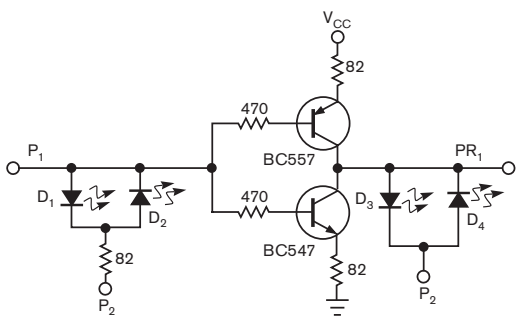

Figure 2 "GuGaplexing" with two I/O lines allows you to control four LEDs.

multiplexing technique would require 19 I/O lines.

This Design Idea proposes a modification to the Charlieplexing technique that allows you to control twice as many LEDs. Thus, the proposed method, "GuGaplexing," allows $2\times N\times(N-1)$ LEDs using only N I/O lines and a few additional discrete components (**Figure 1**). To turn on LED D_1 using the Charlieplexing method, set P_1 to logic one and P_2 to logic zero. To turn on LED D_2, set P_1 to logic zero and P_2 to logic one. **Figure 2** shows the proposed GuGaplexing scheme with two I/O lines controlling four LEDs. The

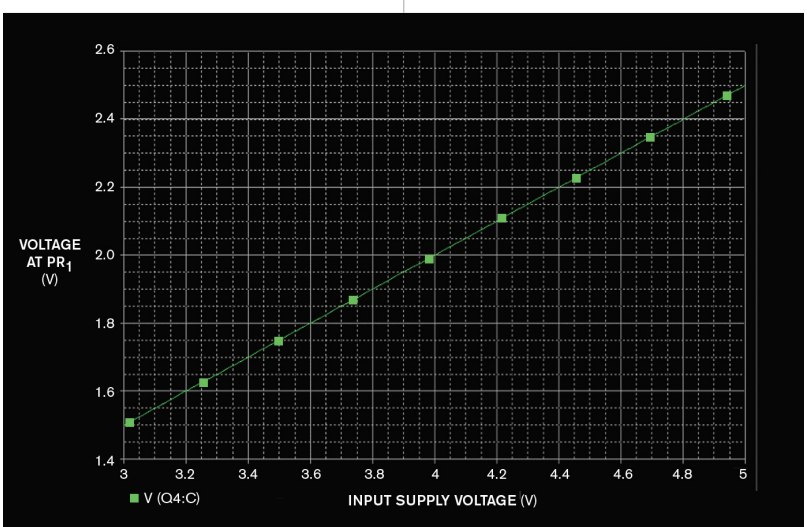

Figure 3 This graph plots the voltage at node PR_1 for various supply-voltage values when the input to the transistor pair is floating.

TABLE 3 I/O LINES AND PR_1 VOLTAGE

P_1	P_2	Voltage at node PR_1	LED that turns on
0	0	V_{CC}	L_3
0	1	V_{CC}	L_2
1	0	0	L_1
1	1	0	L_4
Z	Z	$V_{CC}/2$	None

GuGaplexing technique exploits the fact that each I/O line has three states: one, zero, and high impedance. Thus, with two I/O lines, states 00, 01, 10, and 11 of eight possible states control the LEDs.

Table 2 lists the voltage at the output of the transistor pair for various states of the two I/O lines, P_1 and P_2. The transistor pair comprises a BC547 NPN and a BC557 PNP transistor; matched transistor pairs are recommended. For N I/O lines, the GuGaplexing technique requires $N-1$ transistor pairs. **Table 3** shows the state of the I/O lines P_1 and P_2 and the voltage at node PR_1 to control the four LEDs. The circuit requires that the LED turn-on voltage should be slightly more than $V_{CC}/2$. Thus, for red LEDs with a turn-on voltage of approximately 1.8V, a suitable supply voltage is 2.4V. Similarly, for blue or white LEDs, you can use a 5V supply voltage. Modern microcontrollers, especially the AVR series of microcontrollers from Atmel (www.atmel.com), operate at a wide variety of supply voltages ranging from 1.8 to

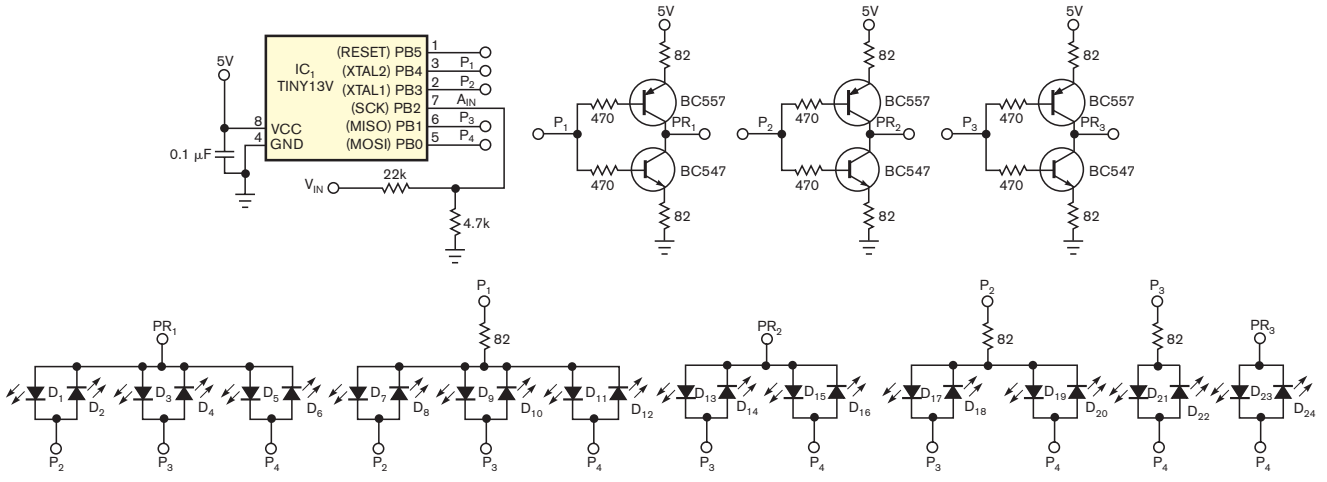

Figure 4 With the GuGaplexing technique, controlling 24 LEDs requires only four I/O lines and three sets of transistors.

5.5V, and this design uses a Tiny13 microcontroller to implement the GuGaplexing technique.

Figure 3 plots the voltage at node PR_1 for various supply-voltage values when the input to the transistor pair is floating. The Spice simulation ensures that the circuit would work properly to provide $V_{CC}/2$ at the PR_1 node for wide operating-supply-voltage values when the input is floating.

A 24-LED bar display validates the scheme in a real application (**Figure 4**). The display is programmable and uses a linear-display scheme for the input analog voltage. The input analog voltage displays in discrete steps on the 24-LED display. Controlling 24 LEDs requires only four I/O lines and three pairs of transistors. The system uses 5-mm, white LEDs in transparent packaging and a 5V supply voltage. The GuGaplexing implementation uses an AVR ATTiny13 microcontroller. The analog input voltage connects to Pin 7 of the ADC input of the Tiny13 microcontroller.

The control program for the ATTiny13 microcontroller is available with the Web version of this Design Idea at www.edn.com/081016di1. The source code is in C and was compiled using the AVRGCC freeware compiler. You can modify the source code to display only one range of input voltage between 0 and 5V. For example, it is possible to have a linear-display range of 1 to 3V or a logarithmic scale for input voltage of 2 to 3V. EDN

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Derive a simple high-current source from a lab supply

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Maxim Integrated Products, Sunnyvale, CA

When electronic testing requires an adjustable current source, you must often build that piece of test equipment in the lab. You can easily make such a current source from a standard force-sense lab power supply (**Figure 1**). The circuit requires an additional power supply for the ICs and a separate control voltage. The feedback signal to the force-sense supply comes from a MAX4172 high-side current monitor from Maxim (www.maxim-ic.com). In the configuration in **Figure 1**, the circuit offers a 1-to-1 ratio of control voltage to load current (1A/V). **Figure 2** shows load current as a function of load resistance.

To change the voltage-to-current ratio, simply change the value of R_{SHUNT}; a lower value of R_{SHUNT} gives higher current and vice versa. The

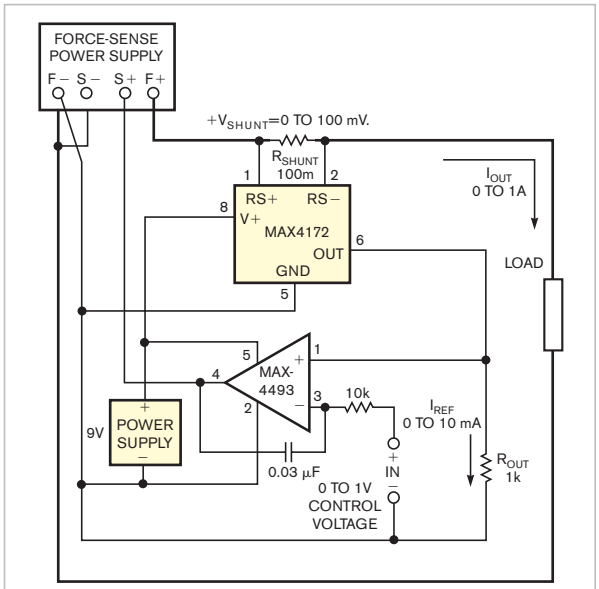

Figure 1 Adding these components to a standard force-sense lab supply makes a simple voltage-controlled current source. As configured, the circuit produces a control ratio of 1-to-1A/V.

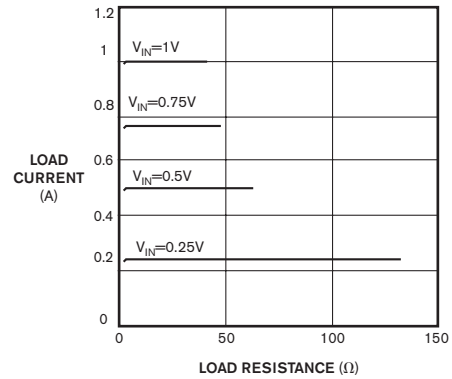

Figure 2 This graph shows load current versus load resistance for the circuit in **Figure 1**.

maximum allowed voltage of 150 mV between the RS+ and RS− terminals, the maximum positive RS voltage of 32V, and the maximum current capability of the force-sense supply all limit the output current of the supply.

Because voltage and current meters in the force-sense supply display inaccurate values while this circuit is operating, you should use external meters to monitor the load voltage and load current. Also, be aware that, if you remove the load so that the output current is 0A, the open-circuit voltage of the force-sense supply goes to the maximum value it can generate. EDN

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DC-accurate, 32-bit DAC achieves 32-bit resolution

W Stephen Woodward, Chapel Hill, NC

Some applications, such as ADC testing and calibration, require a DAC with extremely good resolution, monotonicity, accuracy, and resolution. In these categories of performance, the circuit in **Figure 1** is hard to beat. Its typical specifications follow:

- Resolution=32 bits=3×10^{-10}=1.2 nV=192 dB.
- DNL (differential nonlinearity)=27 bits=400 nV=162 dB.
- INL (integral nonlinearity)=22 bits=1.6 μV=130 dB.
- Full-scale accuracy (untrimmed)=11 bits=±2.5 mV=66 dB.
- Zero accuracy=23 bits=±500 nV±10 nV/°C=140 dB.
- Ripple and noise=21 bits=2 μV p-p=128 dB.

The basis of the DAC's 32-bit resolution is the summing of two 16-bit PWM signals by analog switches S_1 and S_2 and precision resistor network R_2 through R_6. The DAC's monotonicity and DNL are theoretically infinite, and, in practice, the only limit is the 1-to-2^{16} ratio of R_2: ($R_6+R_5+R_{S2\text{-}ON}$) and R_3: ($R_6+R_4+R_{S2\text{-}ON}$). Typical accuracy of 0.1% resistors yields a DNL of approximately 0.1 ppm=27 bits.

The less-than-0.1Ω output impedance of the AD586 reference and the 130-dB CMR (common-mode rejection) of chopper-stabilized "zero-drift" amplifier A_1 mostly limit INL. R_7 suppresses a potential contribution from asymmetry in $R_{S1\text{-}ON}$, yielding the typical INL of approximately 0.3 ppm=22 bits.

Zero-accuracy and output-noise specs are at the low-microvolt level because of the excellent specifications

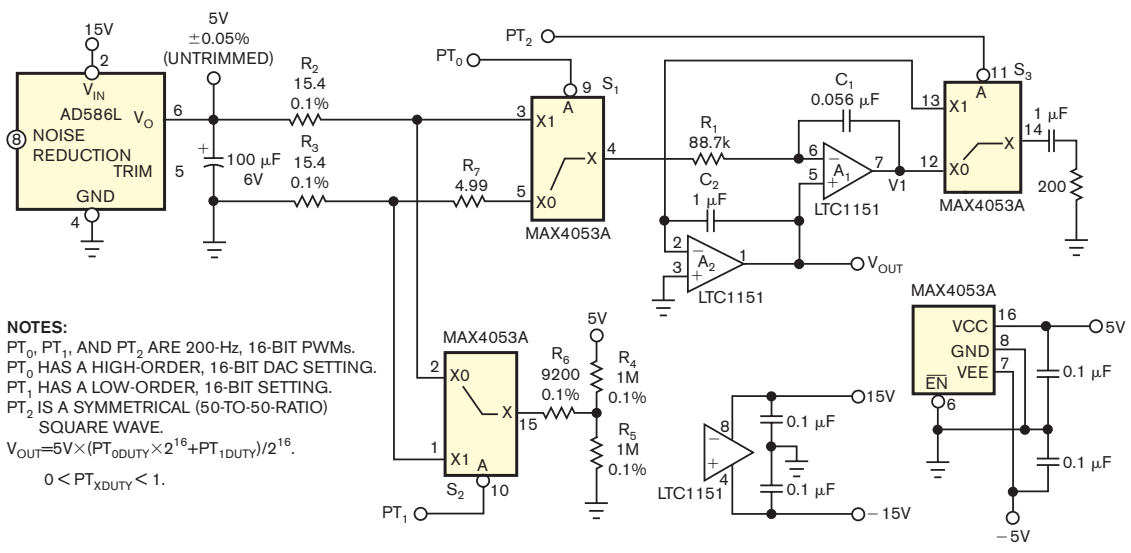

Figure 1 This DAC circuit sums two 16-bit PWM signals using precision analog switches to achieve 32-bit resolution.

of the LTC1151 A_1 and A_2 op amps and the charge-injection performance of the MAX4053A S_2: approximately 0.4 ppm, or 23 bits.

The precision of the AD586L 5V reference, which is ±500 ppm untrimmed, limits absolute accuracy. If your design requires greater accuracy, then you can use an Analog Devices (www.analog.com) simple trim circuit to further tweak it. There's nothing critical about the suggested 200-Hz PWM cycle. You need to change only R_1 and C_1 to accommodate any convenient frequency. How closely the R_1C_1 time constant matches the PWM-cycle time determines the settling time of the A_1-S_2-A_2 synchronous "zero-ripple" integrate-and-hold filter, and can be as fast as one cycle if the match is exact. EDN

Digitally programmable instrumentation amplifier offers autozeroing

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The current trend in advanced instrumentation amps is to use no external resistors. In these amplifiers, a gain-control word, comprising a binary-coded one, sets the voltage gain. Several integer gains within one to 1000 are currently available; however, this range does not yet include a gain of three. Although external-resistor-free amplifiers with a gain of three are available, they are neither instrumentation amps nor autozeroed devices (**Reference 1**). These features are essential in applications requiring accurate processing of low-level voltages. You can use the circuit in **Figure 1** for applications requiring instrumentation amps having voltage gains of three or 10 and the ability to process voltages as low as 1 mV.

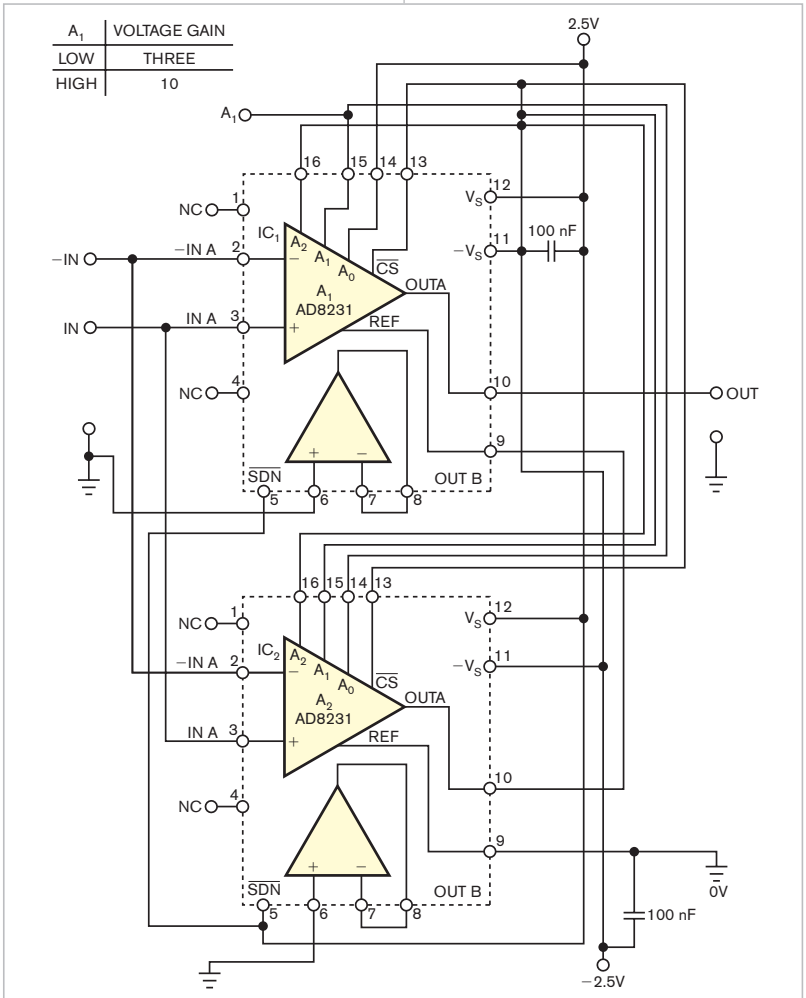

Figure 1 The autozeroed instrumentation amp, digitally programmable for voltage gains of three and 10, can help you to overcome the current inavailability of monolithic ICs for this task.

This design achieves a voltage gain of three by using the "algorithm" of 3=2+1. The circuit comprises two units of the Analog Devices (www.analog.com) digitally gain-programmable, autozeroed AD8231 instrumentation amp. These ICs have voltage gains that are programmable as powers of two—that is, one, two, four … 128 (**Reference 2**). Amplifier A_1 in IC_1 is preset to provide a gain of two, and auxiliary amp A_2 in IC_2 is preset to a gain of one. The noninverting and inverting inputs of A_1 and A_2 connect together. The output of A_2 connects with reference input REF_1, and reference input REF_2 serves as a freely usable reference. You can thus calculate the output voltage as $V_{OUT}=V_{OUT1}+V_{REF1}=V_{OUT1}+V_{OUT2}=2\Delta V_{IN}+\Delta V_{IN}=3\Delta V_{IN}$, where ΔV_{IN} is the input-difference voltage.

Similarly, you can achieve a voltage gain of 10 according to a symbolic formula of 10=8+2. This time, A_1 has a voltage gain of eight, and A_2 has a gain of two. Using **Reference 2**, you can derive that, for gains of both three and 10, $A_{1A1}=A_{0A2}$. Therefore, the gain-control pins connect and remain low for a gain of three, and the high at

these pins sets the gain to 10. Note that three approaches the square root of 10, or approximately 3.16. You can therefore consider it as roughly the geometric center of a decade. EDN

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2 "Zero Drift, Digitally Programmable Instrumentation Amplifier, AD8231," Analog Devices Inc, 2007, www.analog.com/en/prod/0,2877,AD8231,00.html.

C# application controls simple ADC

Yury Magda, Cherkassy, Ukraine

This Design Idea describes a simple and low-cost ADC that you control using the serial port of a PC running Windows XP/Vista. The hardware comprises Microchip's (www.microchip.com) 12-bit SAR (successive-approximation-register) MCP3201 ADC, which attaches to the serial port of the PC through the RTS, CTS, and DTR lines (**Figure 1**).

The circuit uses an SPI (serial-peripheral-interface)-compatible interface to communicate with the MCP3201. The MAX232 chip transforms the RS-232 levels into TTL-compatible levels that the MCP3201 converter requires to operate. The analog signal comes through the IN+ pin of the MCP3201. The output digital stream of bytes on the D_{OUT} pin goes through the CTS line to the serial port of the PC. The RTS line of the serial port provides clock pulses that go through the CLK pin of the converter. Each separate bit appears on D_{OUT} on the falling edge of CLK, and the application should latch the bit on the rising edge of the clock pulse.

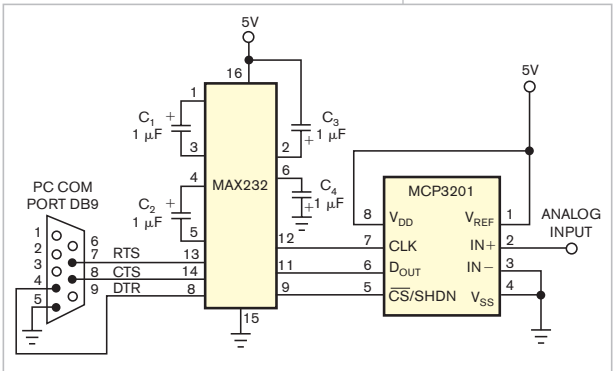

Figure 1 This simple, low-cost ADC comprises a 12-bit SAR ADC, which attaches to the serial port of the PC through the RTS, CTS, and DTR lines.

The DTR line produces the $\overline{CS}$ signal that frames the conversion process. The $\overline{CS}$ signal must be low while the conversion is in progress (**Figure 2**).

The meaningful bits, with MSB first, appear on D_{OUT} after the third CLK pulse goes low. It implies that, if you miss the first three data bits, the software would programmatically realize it. The software that controls the device is written in free Microsoft (www.microsoft.com) Visual C# 2008 Express Edition. It uses a built-in SerialPort component that allows you to get full control over the serial port of the PC. You implement the software as a simple console application containing **Listing 1**, which is available with the Web version of this Design Idea at www.edn.com/081030di1. The program is uncomplicated, so you can easily modify it. For instance, you could send the data from ADC over the Internet or pass it into Microsoft Excel or Microsoft Access for further processing.

You can improve the simplified circuit in **Figure 1** for higher accuracy by placing a lowpass filter in the analog-signal chain. You should also always use a bypass capacitor with the MCP3201. Place a capacitor with a recommended value of 1 µF as close as possible to the device's pin. You can also replace the MCP3201with a similar SAR ADC that works with an SPI-compatible interface. For instance, you may use an LTC1286 or an LTC1297 device from Linear Technology (www.linear.com). If you plan to use a different ADC, you must

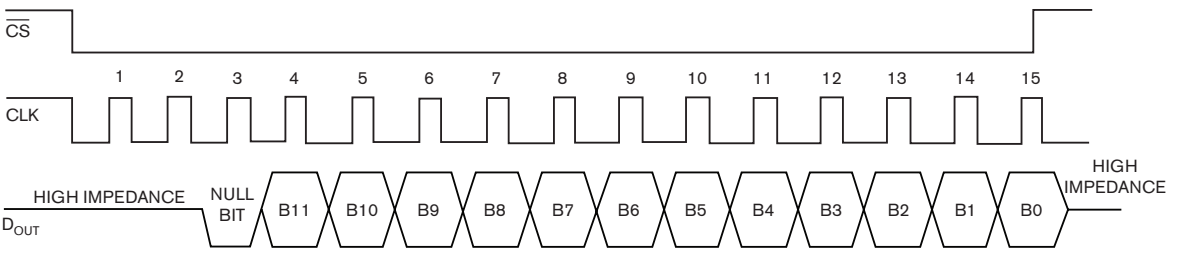

Figure 2 The DTR line produces the $\overline{CS}$ signal that frames the conversion process. The $\overline{CS}$ signal must be low while the conversion is in progress.

make some changes in the hardware and software. The changes necessary to the hardware are obvious, and you may need to change the software source code of the application to correct the *for (…)* loop statement according to the timing diagram of the selected part. EDN

Perform bitwise operation in Excel spreadsheets

Bruno Muswieck, Eletroeste, Uruguaiana, Brazil

Microsoft's (www.microsoft.com) Excel helps engineers with calculus and graphics to solve problems. But engineers often have to perform bitwise operations, too. **Figure 1** shows the bitwise operations' tables. The bitwise functions work for decimal values. If you need to use hexadecimal or binary values, you must use the Dec2Bin and Dec2Hex functions to convert all the decimal values for the desired format.

To install the add-in bitwise functions, you can download the ins.xla file from the Web version of this Design Idea at www.edn.com/081030di2. In Excel, go to Tools, then Add-Ins, and then Browser. Find the downloaded add-in xla file and click OK. Now, Excel can run the bitwise functions.

You can also download some examples from the *EDN* Web site at www.edn.com/081030di2 **(Reference 1)**. EDN

REFERENCE

1 Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Newnes Elsevier, 2004, ISBN 0-7506-7756-2.

AND		RESULT
0	0	0
1	0	0
0	1	0
1	1	1

OR		RESULT
0	0	0
1	0	1
0	1	1
1	1	1

XOR		RESULT
0	0	0
1	0	1
0	1	1
1	1	0

NOT	RESULT
0	255
1	254

SHIFT RIGHT		RESULT
BINARY	SHIFTED	BINARY
11010010	6	00000011

SHIFT LEFT		RESULT
BINARY	SHIFTED	BINARY
01100100	2	10010000

Figure 1 With the help of some new add-in functions, you can perform these bitwise operations in Excel.

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Linear wind-power meter compensates for temperature

W Stephen Woodward, Chapel Hill, NC

The rise of interest in renewable energy created by soaring fossil-fuel costs and global-warming fears has created a matching interest in associated support and demonstration instrumentation. This Design Idea hops on that bandwagon with the ability to directly and conveniently measure an important renewable-energy source: wind power. Handy for quick and easy preliminary evaluation of potential wind-turbine sites, it includes a wind-speed transducer, comprising an optically sensed vane anemometer, and a temperature sensor, comprising a diode-connected transistor. These components interface with a hybrid digital/analog-computation circuit. In combination, they provide a real-time, linear, temperature-compensated readout of wind-power density.

The power-generation potential of wind is ½×air density (kg/m^3)×air speed (m/sec)^3. To compute it, there-

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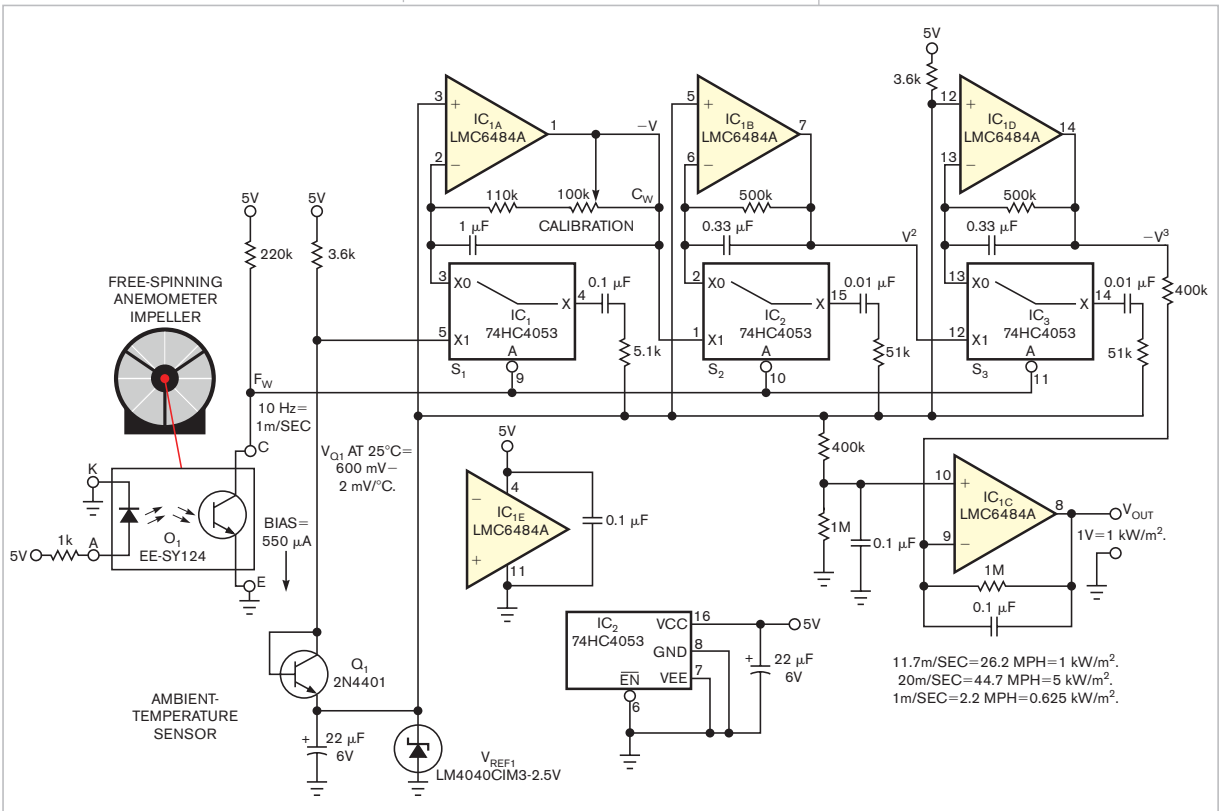

Figure 1 This meter circuit uses a free-spinning anemometer and a diode-connected transistor temperature sensor to measure the available wind power for "green" power generation.

fore, requires estimating air density, which is inversely proportional to absolute temperature; measuring air speed; and calculating a cube.

Here's how the wind-power meter does it. Diode-connected Q_1 has a bias of 550 µA for a 25°C (298K) base-to-emitter voltage of approximately 600 mV and a temperature coefficient of −2 mV/°C. Thus, Q_1 is a voltage reference that tracks the approximate ideal-gas-law temperature dependence of air density: −0.3%/°C. Meanwhile, optical sensor O_1 works with a free-spinning anemometer impeller to produce wind-speed-proportional frequency: F_W=10 Hz/m/sec. Conversion of V_{Q1} and F_W into a 1-mV=1W/m² output signal is then the function of the third-order X×Y×Z-multiplying behavior of three cascaded CMOS-switch FVC (frequency-to-voltage-converter) charge pumps: S_1, S_2, and S_3.

FVC S_1/IC_{1A} generates a negative voltage of $-0.17\times V_{Q1}\times F_W$; FVC S_2/IC_{1B} generates $V_2=-V\times F_W=0.17\times V_{Q1}\times F_W^2$; and FVC S_3/IC_{1D} generates $-V_3=-0.17\times V_{Q1}\times F_W^3$. Finally, differential inverter IC_{1C} shifts and scales $-V_3$ to output $V_{OUT}=0.42\times V_{Q1}\times F_W^3=1V/kW/m^2$.

You can conveniently calibrate the wind-power meter in an automobile being driven on a windless day at a constant speed of 18.6m/sec=41.5 mph=66.8 kph. With the anemometer exposed to the external slipstream, adjust the calibration trimming potentiometer for an output voltage of 4V or, for better accuracy, to the voltage that the following formula that accommodates true air density yields: V_{OUT}=1.14V×air-pressure millibar/(273+ambient temperature Celsius). EDN

Oscillator uses dual-output current-controlled conveyors

Abhirup Lahiri, Netaji Subhas Institute of Technology, New Delhi, India

In the last decade, engineers have done much work in designing and implementing current-mode circuits using second-generation current conveyors, which have higher signal bandwidth, greater linearity, larger dynamic range, simpler circuitry, and lower power consumption than their predecessors. Recently, a second-generation dual-output, current-controlled conveyor has emerged. The device is an active building block (**Figure 1**), and the following equations characterize it: $I_Y=0$, $V_X=V_Y+I_XR_X$, and $I_{Z+}=I_X$; $I_{Z-}=-I_X$. The parasitic resistance at terminal X is $R_X=(V_T/2I_B)$, where V_T is the thermal voltage and I_B is the bias current of the conveyor that is tunable over several decades.

Figure 2 shows current-controlled oscillators with few components, employing only two dual-output current-controlled conveyors and two grounded capacitors. The devices use no external resistors, and the parasitic resistance at terminal X realizes resistance. The proposed design for the circuit provides electronic controllability of frequency of oscillation.

The characteristic equation for both of the circuits in **Figure 2** is $s^2C_1C_2R_{X1}R_{X2}+sC_2R_{X1}-sC_1RX_1+1=0$. Satisfying Barkhausen's criteria—that the loop gain is unity or greater and that the feedback signal arriving back at the input is phase-shifted 360°—the required condition for oscillation is $C_1=C_2$, and the frequency of oscillation is $f=1/(2\pi\sqrt{C_1C_2R_{X1}R_{X2}})$.

Assuming that $C_1=C_2=C$ and taking $R_{X1}=R_{X2}=V_T/2I_B$ yield a frequency of oscillation: $f=(I_B/\pi CV_T)$. Clearly, the dc-bias current, I_B, can vary the frequency of the current conveyors, and the frequency is, therefore, electronically controllable. EDN

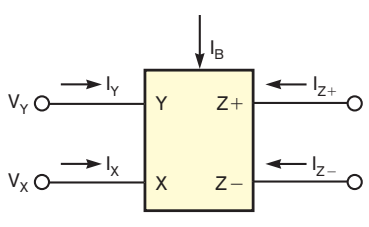

Figure 1 This dual-output current-controlled conveyor illustrates the quantities the equations use.

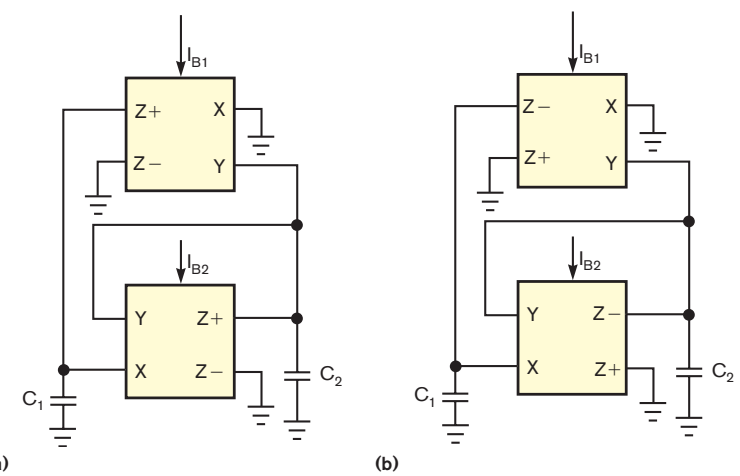

Figure 2 Varying the bias current, I_B, of the dual-output current-controlled conveyor (a) controls its frequency of oscillation versus another device (b).

Circuits drive single-coil latching relays

Alfredo H Saab and Tina Alikahi,
Maxim Integrated Products, Sunnyvale, CA

A single-coil latching relay is a relay with memory, usually with a magnetic structure that provides two stable positions for the armature that holds the movable contacts. A permanent magnet provides the force holding the armature in these stable positions. An application of electrical current to the relay coil moves the armature from one position to the other, which in turn changes the contact positions.

Applying to the coil a current pulse in one direction, of longer duration than the specified minimum for that relay type, sets the relay to the first of two stable positions, and it remains in that position after the current ceases to circulate. Current in the opposite direction resets the relay to the other position, which is also stable with no current. The relay then indefinitely remains in that position until a new current pulse toggles it to the other position.

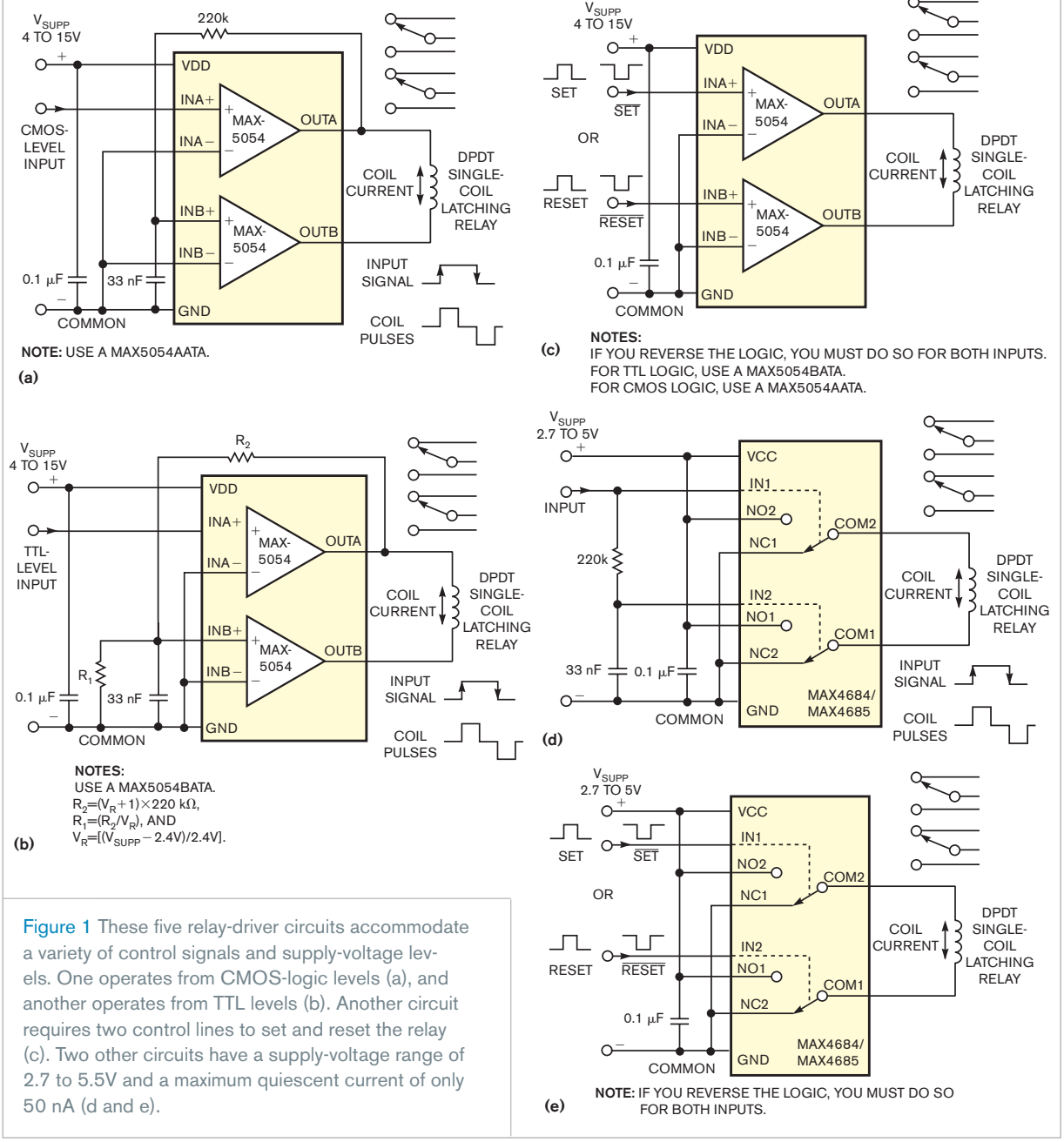

Figure 1 These five relay-driver circuits accommodate a variety of control signals and supply-voltage levels. One operates from CMOS-logic levels (a), and another operates from TTL levels (b). Another circuit requires two control lines to set and reset the relay (c). Two other circuits have a supply-voltage range of 2.7 to 5.5V and a maximum quiescent current of only 50 nA (d and e).

The electronic circuitry to drive one of these relays from logic signals can be a half-bridge if dual supply voltages are available or a full bridge—that is, an H-type power driver—if only a single supply voltage is available. The need to generate reversible-current pulses through the two-terminal coil imposes the use of these bridge topologies. Because the relay itself does not consume power under static conditions, the driving circuitry should also consume minimal power under the same conditions.

Figure 1 illustrates a variety of driving circuits, depending on the input-signal-logic levels, their coding, and the magnitude of the available supply voltages. The circuits in **figures 1a** through **c** drive relays for voltages of 4 to 15V. The circuit in **Figure 1c** requires two separate control lines: The set line sets the relay, and the reset line resets it. You can code the set and reset signals as positive (active high) or negative (active low). You must use the same logic convention for both inputs in this circuit.

The widths of the set and reset signals must be longer than the minimum time required for the relay to operate—typically, 3 to 5 msec. For proper operation, you should apply only one signal at a time; while applying one, the other should remain at the nonactive-logic value. Using positive logic, for example, the signal must go high for 3 to 5 msec, and the other input must remain low until the first signal pulse ends. The choice of IC determines the logic level: TTL (transistor-to-transistor logic) or power-supply-level CMOS (**Figure 1c**).

The circuits in **figures 1a** and **1b** operate from a single on/off-signal line, generating a coil-current pulse with each transition of the input signal. The polarity of the coil-current pulse depends on the polarity of the input-signal transition that generates it (**figures 1a**, **b**, and **d**). The circuit in **Figure 1a** operates from CMOS-logic levels, and the one in **Figure 1b** operates from TTL levels. After each transition, the signal must remain stable for longer than the relay's minimum operating time. The circuits in **figures 1a** and **c** typically draw quiescent currents of 40 μA, and the one in **Figure 1b** typically draws approximately 50 μA. The circuits in figures **1d** and **1e** are similar to those in **figures 1a**, **1b**, and **1c**, but their supply-voltage range is 2.7 to 5.5V, and their maximum quiescent current is only 50 nA.

Because the single-coil latching relay has a memory of its own, you must initialize its position after power-up to a known state, either by exercising the input logic or by analyzing and responding to a signal from the contacts' circuitry. Any of these circuits can deliver as much as several hundred milliamps in either polarity while pulse-driving a relay coil. You can find technical information and data sheets for the ICs in these circuits at www.maxim-ic.com. EDN

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"Chipiplexing" efficiently drives multiple LEDs using few microcontroller ports

Guillermo Jaquenod, La Plata, Argentina

Actual microcontrollers have powerful bidirectional I/O ports, and you can use different techniques to fully exploit such capabilities. Recent Design Ideas described the "Charlieplexing" method as an effective way to drive $M=N\times(N-1)$ LEDs using only N bidirectional I/O ports and N resistors (**references 1** and **2**). Unfortunately, using Charlieplexing allows you to drive only one LED at a time, so, when using a large number of LEDs, only a tiny slice of time is available to multiplex each LED: $T_{DRIVE}=T/M$, where T is the PWM excitation period. As a consequence, to obtain a given average current and bright LEDs, you must excite them with a current M times higher, and you can't usually obtain such peak currents from the microcontroller port.

This Design Idea describes "Chipiplexing," a method in which you need to add only N cheap, bipolar transistors. This circuit uses PNP types, but you can also use NPN devices. (The term *Chipiplexing* comes from my nickname, Chipi.) The benefits pay the additional cost because you can simultaneously drive N−1 LEDs, thereby reducing peak currents N−1 times.

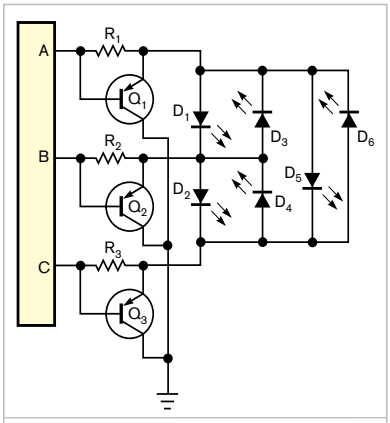

Figure 1 With Chipiplexing, you need to add only N cheap, bipolar transistors to simultaneously drive two LEDs.

Figure 1 shows the approach for N=3 and M=6, but you can use the same criteria for different values of N; in this case, you can simultaneously drive two LEDs. The current-limiting resistors connect in parallel with the base and emitter of the added PNP transistors, and all the collectors connect to ground. If you set one of the microcontroller ports to zero, or ground, the respective PNP transistor has a grounded base, and its emitter is at a fixed voltage—typically, 0.7V. You can excite every LED whose cathode connects to this emitter through the remaining ports. If you set the port to one, the battery voltage, the LED turns on; if you set the port to high impedance, the LED turns off.

Table 1 shows how there are now nine possible combinations of the

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TABLE 1 NINE POSSIBLE USEFUL PORT COMBINATIONS TO DRIVE LEDS

A	B	C	D_1	D_2	D_3	D_4	D_5	D_6
V_{BAT}	Ground	High impedance	Yes	No	No	No	No	No
High impedance	V_{BAT}	Ground	No	Yes	No	No	No	No
Ground	V_{BAT}	High impedance	No	No	Yes	No	No	No
High impedance	Ground	V_{BAT}	No	No	No	Yes	No	No
V_{BAT}	High impedance	Ground	No	No	No	No	Yes	No
Ground	High impedance	V_{BAT}	No	No	No	No	No	Yes
Ground	V_{BAT}	V_{BAT}	No	No	Yes	No	No	Yes
V_{BAT}	V_{BAT}	Ground	No	Yes	No	No	Yes	No
V_{BAT}	Ground	V_{BAT}	Yes	No	No	Yes	No	No

three microcontroller ports: the six available when using Charlieplexing to drive one LED at a time and three new combinations to drive two LEDs at a time. The microcontroller port grounds the transistor's base. This action fixes a junction-drop voltage at the emitter and collects and sinks all the LED currents to ground without overconstraining the microcontroller port, which has to sink only the transistor's base current plus 0.7V per resistor. Each of the other ports set to the battery voltage needs to source only one LED current.

With Charlieplexing, two resistors are in the LED-current path; in this case, however, you can easily compute the limiting resistors as $R=(V_{BAT}-V_{LED}-0.7)/I_{LED}$, where V_{BAT} is the battery voltage, V_{LED} is the LED voltage, and I_{LED} is the desired LED current. The benefits are more noticeable as the number of LEDs increases. For N=5, with 20 LEDs, this approach gives 20% of the total time to drive each LED, instead of only 5% of the time using Charlieplexing. EDN

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Achieve precision temperature control with TEC Seebeck-voltage sampling

W Stephen Woodward, Chapel Hill, NC

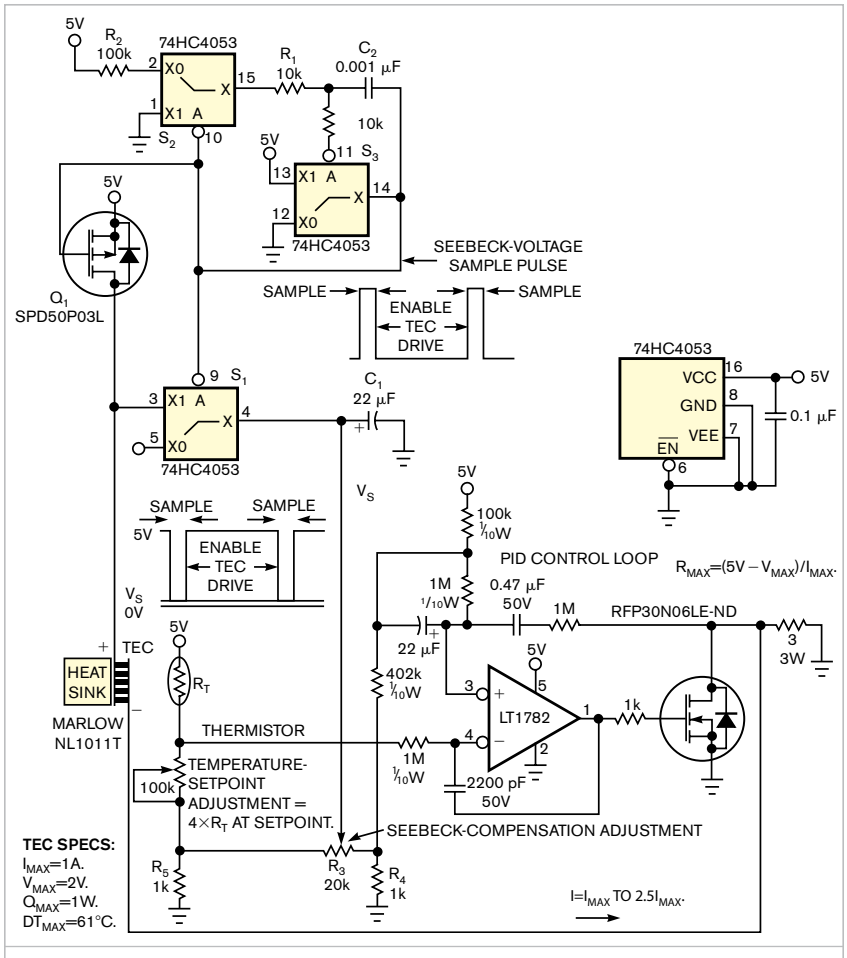

Figure 1 This circuit periodically sets the thermoelectric cooler's drive current to zero, sampling the Seebeck voltage and holding it in a storage capacitor to achieve stable temperature control with real-world heat sinks and thermocouples.

TEC (thermoelectric-cooler) temperature-control systems often have limited stability. The causes of these limitations are the thermal properties of the system, not the performance of the control electronics. Real-world thermal-control systems incur nonzero thermal impedances in the heat-transfer paths between the TEC; the thermal load, which is the object of thermostasis; the temperature sensor—for example, a thermistor; and the ambient temperature.

If the ratios of these impedances don't balance, then even perfect thermostasis of the sensor's temperature doesn't equate to adequate stability of the load's temperature. The circuit in **Figure 1** provides a thermoelectronic design that directly measures the heat flux through the TEC and then uses the measurement to better estimate and cancel the effects of thermal impedances. Its operation is based on the fact that the total voltage that every TEC develops is the sum of two components: an ohmic component proportional to drive current and the Seebeck voltage, V_S, which is proportional to the temperature difference across the TEC and, therefore, to heat flux.

In this circuit, however, the drive current switches to zero approximately every 100 µsec because of the asymmetrical sample-pulse waveform that multivibrator S_2/S_3 generates. Each sample pulse turns off 5V transistor Q_1, which isolates the Seebeck voltage and allows its sampling through S_1 and storage capacitor C_1 to hold it. The duty factor of the sampling pulse, which the

R_1-to-R_2 ratio sets, is less than 10% to avoid significantly reducing the TEC-drive capability of the circuit.

You apply the acquired Seebeck signal to the $R_3/R_4/R_5$ adjustable-bridge circuit, which empirically determines the feedback ratio for both polarity and amplitude to provide best stability. With proper bridge adjustment, you can make gradient cancellation nearly perfect over a wide range of ambient temperatures. The TEC-control circuit in **Figure 1** derives from a previous Design Idea because it eases the incorporation of Seebeck sampling (**Reference 1**). You can, however, adapt Seebeck sampling to virtually any TEC-drive topology. You can further enhance the circuit in **Figure 1** by using nonvolatile, in-circuit-programmable resistors for the $R_3/R_4/R_5$ bridge, automatically optimizing gradient cancellation. One attractive choice is the Rejustor family of monolithic resistors from Microbridge Technologies (www.mbridgetech.com). EDN

REFERENCE

1 Woodward, W Stephen, "Thermoelectric-cooler unipolar drive achieves stable temperatures," *EDN*, Dec 3, 2007, pg 98, www.edn.com/article/CA6505571.

Instrumentation-amplifier-based current shunt exhibits 0V drop

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Passive current shunts for measuring the value of current flowing through a relatively small-value resistor often have a full-scale voltage drop of 60 mV for higher-power equipment and 200 mV for electronic instruments. Similarly, simple current-to-voltage converters, in which the measured current flows through a sensing resistor, often have even higher voltage drops. In some cases, however, the voltage drop between the input terminal and the ground must be as low as possible; 0V—independent of the value of measured current—is ideal. If your application requires this feature, you can use the current-to-voltage converter in **Figure 1**. In this circuit, resistor R_1 serves as a classic current-sensing resistor, on which the instrumentation amplifier senses the measured current, resulting in the voltage drop. The instrumentation amplifier, along with R_1, not only serves as an inverting current-to-voltage converter, but also creates a voltage through a resistive network at Point B. This voltage is equal in magnitude to a voltage drop on R_1 and has the opposite polarity to ΔV_{R1}. The net result is that the value of voltage at Input A is theoretically 0V, regardless of the magnitude and polarity of the current flowing into the input.

The design uses the Analog Devices (www.analog.com) AD8223 instrumentation amplifier because it has a default voltage gain of five; this value remains close to the ideal one with high precision. The typical gain error at the default value of gain is 0.03%, and the worst-case error is 0.1% for the B-grade IC (**Reference 1**). For gain of five and R_1 and R_2 having the same value, you can derive that the value of R_3 is two times that of R_2 for a 0V drop at Input A (**Figure 2**). Resistors R_1, R_2, and R_3 in **Figure 1** should be high-precision, low-temperature-coefficient types. In the experimental circuit with a value of 20Ω for R_1 and R_2, there is an input-referred-current zero shift of 0.8 μA, and the voltage drop at Input A varies by 0.27 mV at a 1-mA input current. Similar slope of negative-voltage variations occurs at Input A for negative-input current. The transfer constant, or transresistance, of the circuit is: $(\Delta V_{OUT})/(\Delta I_{IN}) = -5R$.

Thus, for instance, an input current of 1 mA causes the voltage of −100 mV to appear at the output. Because the output-current capability of the AD8223 is approximately 2.5 times higher for sinking output current than for sourcing current, the input scale can be higher for positive currents by a factor of 2.5. You can further increase the scales for both positive and negative currents by increasing the supply voltages from ±5V to ±12V; you can also use 12V and −5V. If your design requires an even higher input current, place a precision voltage buffer, having appropriately high

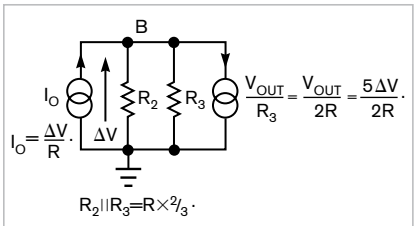

Figure 2 The value of R_3 is two times that of R_2 for a 0V drop at Input A in Figure 1.

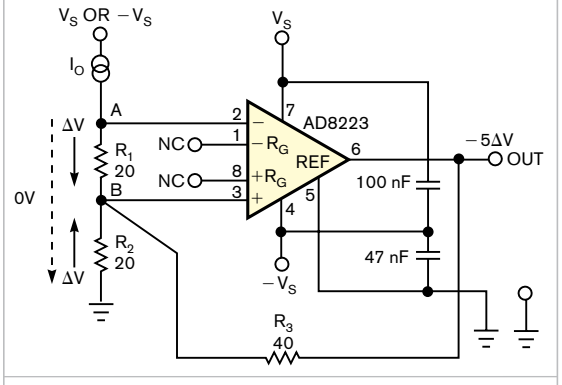

Figure 1 This instrumentation amplifier serves two purposes: It forms a current-to-voltage converter having a transresistance of −5R, and it exerts a voltage drop of opposite polarity at point B, resulting in a zero potential at Input A, regardless of input-current I/0.

output-current capability, between the output of the instrumentation amplifier and resistor R_3. EDN

REFERENCE

1 "Single-Supply, Low-Cost Instrumentation Amplifier, AD8223," Analog Devices Inc, 2008, www.analog.com/en/prod/0,2877,AD8223,00.html.

Spark detector uses proximity

Robert Most, Ferris State University, Big Rapids, MI

Hall-effect ICs find use as proximity sensors in applications such as proximity detection and angular-velocity measurement on rotating machinery. Hall-effect devices can detect mechanical motion without mechanical contact. This noninvasive detection is due to the magnetic nature of the Hall effect. A current flowing through a semiconductor in the Y direction produces a negligible potential difference in the X direction (**Figure 1**). In the presence of a magnetic field at a right angle to the current flow, the Z direction, a displacement voltage appears across the semiconductor in the X direction. This effect is the Hall voltage, V_H.

Hall-effect ICs detect, signal-condition, and add hysteresis to the electrical displacement. In essence, the devices measure the electric field, which the magnetic field causes, across the semiconductor in the X direction. Therefore, if you subject the semiconductor to an electric field of sufficient magnitude in the X direction, the Hall-effect device would detect the electric field, as well.

Internal-combustion-engine designs require precise control of spark timing. The microcontroller that controls engine parameters not only changes the spark relation relative to the piston position, but also, in more advanced engines, requires feedback for variable valve timing. In addition, diagnostic aids and engine-troubleshooting hardware can benefit from an easy way to measure spark timing using this novel approach. Even the most basic carburetor adjustments on a lawnmower require a method to measure an engine's revolutions per minute. Four-stroke small engines create a spark on every engine revolution. Therefore, the detection of this spark is a direct indication of engine revolutions per minute.

By simply placing the Hall-effect IC against the spark-plug wire using the correct orientation, you can detect a spark-plug pulse using its electric field. Simply attach the device with electrical tape to the spark-plug wire's insulation. Because the Hall-effect IC incorporates internal signal conditioning and hysteresis, no additional components are necessary to read a basic frequency from the device, unlike with the traditional current-transformer method.

The circuit in **Figure 2** converts the pulses from the Hall-effect IC into a dc voltage that the most basic voltmeter can read. The Hall-effect IC provides an open-collector output. You need only a pullup resistor. The sensor converts the series of generated pulses, which the LM2917 frequency-to-voltage converter from National Semiconductor (www.national.com) converts to a voltage. The selection of C_1 and R_1 scales the output voltage in relation to the range of frequencies that the charge-pump section of this device will encounter. In the case of a four-stroke, single-cylinder engine, a range to 5000 rpm is more than sufficient.

The circuit provides an output voltage as high as 5V and requires a battery-supply voltage of 9V. Operation is straightforward: By pressing the Hall-effect IC against the spark-plug wire, the voltage on the DVM (digital volt-

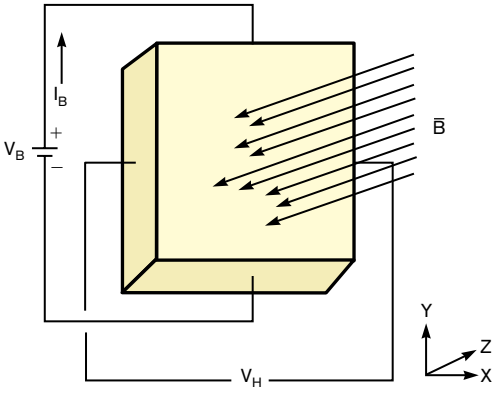

Figure 1 A current flowing through a semiconductor in the Y direction produces a negligible potential difference in the X direction.

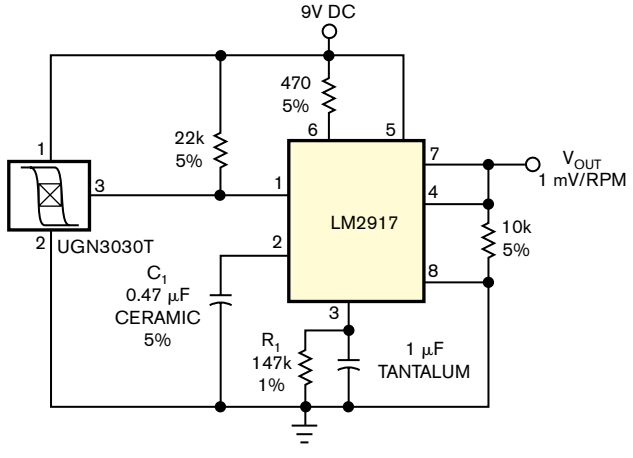

Figure 2 This circuit converts the pulses from the Hall-effect IC into a dc voltage that the most basic voltmeter can read.

meter) can readily interpret the revolutions per minute. Because the measurement is noninvasive, this method can easily perform repeated measurements or analysis of multicylinder engines. Measurement of automobile engines differs slightly. Automobile engines have mechanical distributors that spark on every other engine revolution. Ignition systems without distributors and with one ignition coil per cylinder also spark on every other engine revolution.

Because there is no electrical contact with the ignition system, this circuit intrinsically provides isolation from the high voltage. Interfacing to microprocessors and microcontrollers thus becomes a matter of compatible logic levels. The Hall-effect IC's power-supply voltage is 4.5 to 24V dc, which enables it to work with standard 5V processors as well as automotive voltages. You can interface multiple sensors to provide ignition diagnosis and timing analysis in automotive applications.EDN

Configure a low-cost, 9V battery-voltage monitor

Paul C Florian, McKinney, TX

This Design Idea describes a 9V battery-voltage monitor whose total parts cost less than 34 cents (**Figure 1**). You configure transistor Q_1 as a 10-mA current sink. LED_1, a Kingbright (www.kingbrightusa.com) WP7104IT, is on when the battery voltage is good. When the battery voltage nears the threshold voltage, the LED gradually dims. It goes out once it reaches the threshold voltage. The threshold voltage for this design is 7.2V, which the values of D_3, LED_1, and R_1 determine. If your application requires a different threshold voltage, you can change these three components' values. You can reduce the PCB (printed-circuit-board) space this circuit requires by using equivalent surface-mount components.EDN

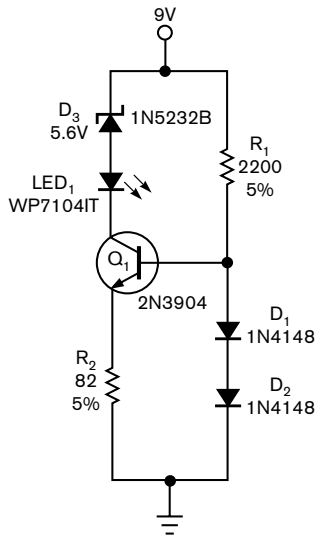

Figure 1 The parts for this 9V battery-voltage monitor cost less than 34 cents.

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Solar-array controller needs no multiplier to maximize power

W Stephen Woodward, Chapel Hill, NC

Solar-photovoltaic arrays are among the most efficient, cost-effective, and scalable "green" alternatives to fossil fuels, and researchers are almost daily announcing new advances in photovoltaic technology. But successful application of photovoltaics still depends on strict attention to power-conversion efficiency. **Figure 1** shows one reason for this attention.

A photovoltaic array's delivery of useful power to the load is a sensitive function of load-line voltage, which in turn depends on insolation—that is, sunlight intensity—and array temperature. Operation anywhere on the current/voltage curve except at the optimal maximum-power-point voltage results in lowered efficiency and a waste of valuable energy. Consequently, methods for maximum-power-point tracking are common features in advanced solar-power-management systems because they can boost practical power-usage efficiency—often by 30% or more.

Because of its generality, a popular maximum-power-point-tracking-control algorithm is perturb and observe, which periodically modulates, or perturbs, the load voltage; calculates, or observes, the instantaneous transferred power response; and uses the phase relationship between load modulation and calculated power as feedback to "climb the hill" of the current/voltage curve to the maximum-power-point optimum. The perturb-and-observe algorithm is the basis of the maximum-power-point-tracking-control circuit (**Figure 2**, in yellow) but with a twist (in blue), which achieves a feedback function equivalent to a current-times-voltage power calculation but without the complexity of a conventional multiplier. The idea relies on the well-known logarithmic behavior of transistor junctions, $V_{BE}=(kT/q)\log(I_C/I_S)=(kT/q)[\log(I_C)-\log(I_S)]$, where V_{BE} is the base-to-emitter voltage. It also relies on the fact that adding logarithms is mathematically equivalent to multiplication. Here's how.

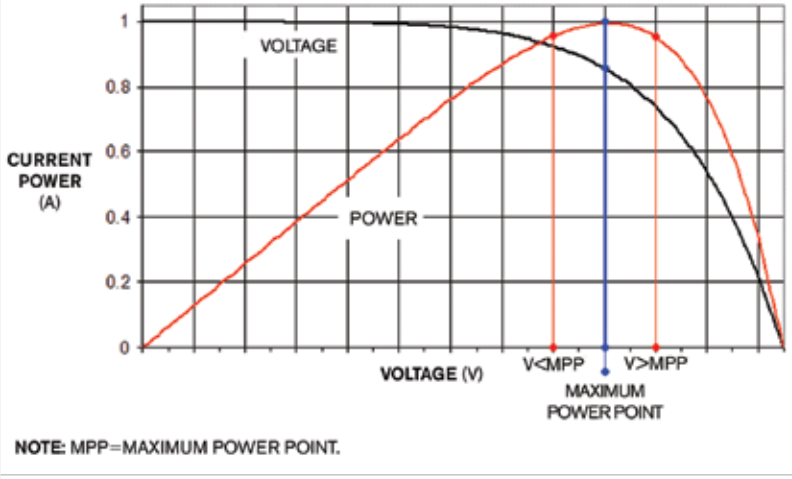

Figure 1 It is important to operate solar-photovoltaic arrays at their maximum power point.

Capacitor C_2 couples a 100-Hz, approximately 1V-p-p-modulation or 1V-p-p-perturbation square wave from the S_2/S_3 CMOS oscillator onto the photovoltaic-input voltage, V. The current/voltage curve of the array causes the input current, I, to reflect the V modulation with a corresponding voltage-times-current input-power modulation. IC_{1A} forces I_{Q1} to equal $I\times x_1$, where I is the solar-array current and x_1 is a gain constant. IC_{1B} forces I_{Q2} to equal V/499 kΩ, where V is the solar-array voltage. Thus, $V_{Q1}=(kT_1/q)1[\log(I)-\log(I_{S1})+\log(x_1)]$, and $V_{Q2}=(kT_2/q)[\log(V)-\log(I_{S2})-\log(499\ k\Omega)]$. V_{Q1} is the base-to-emitter voltage of Q_1; k is the Boltzman constant; T_1 is the temperature of Q_1; q is the elementary charge of the electron; I is the current input

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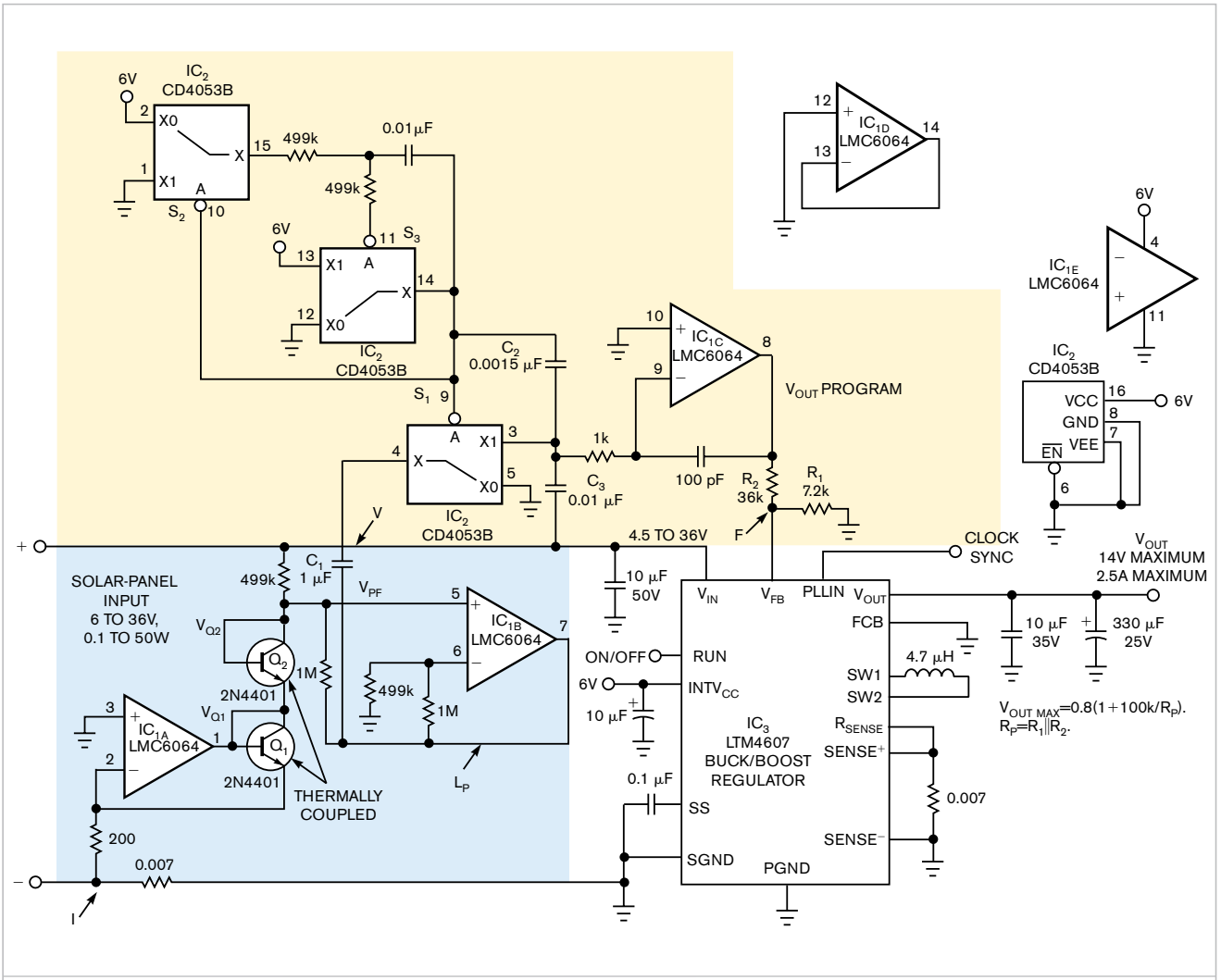

Figure 2 This maximum-power-point-tracking controller relies on the well-known logarithmic behavior of transistor junctions.

from the solar panel's negative terminal; I_{S1} is the saturation current of Q_1; x_1 is the arbitrary gain constant, which IC_3 determines; V is the voltage input from the solar panel's positive terminal; I_{S2} is the saturation current of Q_2; K is degrees Kelvin; V_{PF} is the power-feedback signal; and V_{IP} is the calculated power-input signal. Because k, q, I_{S1}, I_{S2}, x_1, and 499 kΩ are all constants and $T_1=T_2=T$, however, for the purposes of the perturb-and-observe algorithm, which is interested only in observing the variation of current and voltage with perturbation, effectively, $V_{Q1}=(kT/q)\log(I)$, and $V_{Q2}=(kT/q)\log(V)$.

The series connection of Q_1 and Q_2 yields $V_{PF}=V_{Q1}+V_{Q2}=(kT/q)[\log(I)+\log(V)]=(kT/q)\log(VI)$, and, because of IC_{1B}'s noninverting gain of three, $V_{IP}=3(kT/q)\log(V\,I)\simeq 765$ µV/% of change in watts. The V_{IP} log (power) signal couples through C_1 to synchronous demodulator S_1, and error integrator and control op amp IC_{1C} integrates the rectified S_1 output on C_3. The IC_{1C} integrated error signal closes the feedback loop around the IC_3 regulator and results in the desired maximum-power-point-tracking behavior.

Using micropower parts and design techniques holds the total power consumption of the maximum-power-point-tracking circuit to approximately 1 mW, which avoids significantly eroding the efficiency advantage—the point of the circuit in the first place. Meanwhile, simplifying the interface between the maximum-power-point-tracking circuit and the regulator to only three connection nodes—I, V, and F—means that you can easily adapt the universal maximum-power-point-tracking circuit to most switching regulators and controllers. Therefore, this Design Idea offers the efficiency advantages of a maximum-power-point-tracking circuit to small solar-powered systems in which more complex, costly, and power-hungry implementations would be difficult to justify. EDN

Simple microcontroller-temperature measurement uses only a diode and a capacitor

Andreas Grün, Wedemark, Germany

Using a PN-junction diode for temperature measurement usually depends on its 2-mV/K temperature coefficient. Conventionally, you must amplify and digitize this voltage with an ADC before you can use the value in a microcontroller. Less well-known is the fact that the *reverse* current of a PN-junction diode shows a good exponential dependency over temperature; increasing the temperature by approximately 12K doubles the leakage (**Figure 1**). An easy way to measure current over such a large range of two to three decades is to charge and discharge a capacitor and measure the time or frequency.

A general-purpose I/O pin of a microcontroller charges a capacitor either by using it temporally as an output or by enabling a pull-up resistor, which is available in some controllers (**Figure 2a**). After charging the pin, you configure it as a high-impedance input, and a capacitor discharges through the leakage current of the diode (**Figure 2b**). The discharge time then is proportional to the temperature of the diode; thus, the diode exhibits exponential behavior. Depending on the type of diode, the exponential behavior can be nearly ideal. Calibration of a base point is necessary because the absolute value of the current varies greatly at a given temperature.

Selecting the diode and the value of the capacitor requires some care. The smaller the PN junction, the smaller the reverse current and the longer the discharging time. Periods longer than a few seconds are usually unsuitable. Making the capacitor's value too low leads to errors because the capacitance of any cable and the capacitance of the PN-junction diode come into effect.

Typically, a power diode, such as a 1N4001 with a capacitance of 1 nF, gives suitable results. The discharge time is approximately 0.3 to 1 sec at room temperature, falling into the millisecond range at 100°C. The PN-junction diode of a power transistor should also work. EDN

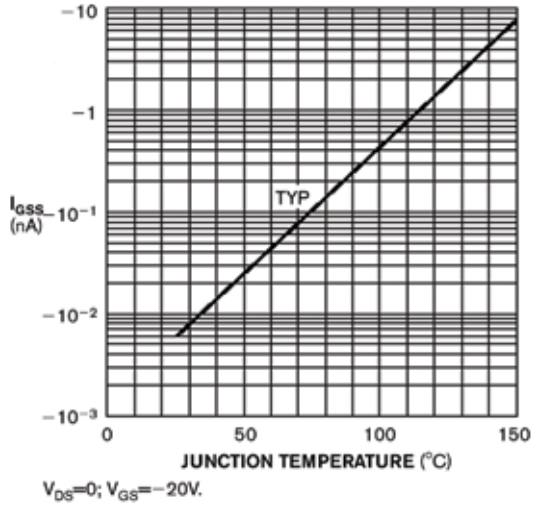

Figure 1 The reverse current of a PN-junction diode shows an exponential dependency over temperature; increasing the temperature by approximately 12K doubles the leakage.

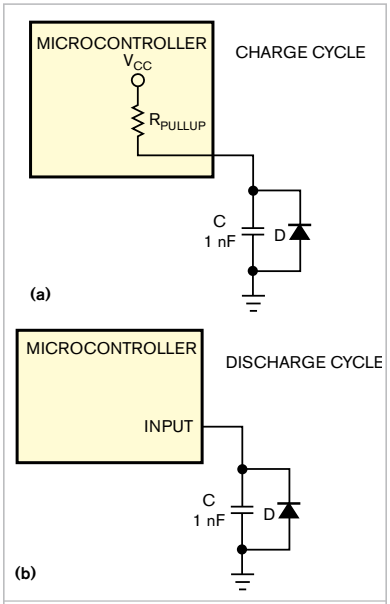

Figure 2 Capacitor C first charges through the pull-up resistance of the microcontroller's I/O pin configured as an output (a). The capacitor then discharges through the reverse leakage of diode D_1 (b).

Current mirror drives multiple LEDs from a low supply voltage

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

Driving LEDs at a regulated current from low supply voltages can be difficult because minimal overhead voltage is available for control circuits. A current-mirror architecture is suitable but usually works only with ICs with well-matched transistors and in which the silicon substrate holds them at one temperature. However, high currents—approximately 100 mA—are not normally possible. A thermal runaway can occur in circuits using unfavorable combinations of discrete bipolar transistors. In this scenario, one LED-driver transistor becomes

slightly hotter than the others, its gain increases, and it takes more current and gets even hotter until it self-destructs. This Design Idea shows how you can avoid this problem for pulsed-current-mirror applications.

The current mirror comprises Q_4 through Q_7 with connected bases and emitters, and the collector current of Q_3 is the control output (**Figure 1**). Resistor R_3 converts Q_3's collector current to a feedback voltage. Transistors Q_1 and Q_2 form a voltage-difference amplifier. The control-transistor current after feedback is $1.2V/R_3$, and the LEDs have a similar current. Because of the pulsed operation—say, 25% duty at 3 Hz—the transistor temperature does not reach a stable value and cools again toward the ambient temperature during the off period. The thermal-runaway effect does not have time to develop.

The capacitor prevents transient oscillations at switch-on or -off. Use the same transistor type for Q_4 through Q_7 and mount all of them on the same part of the PCB (printed-circuit board). The supply voltage can be as low as 2.5V for certain LEDs, especially infrared types, and the collector current can exceed 100 mA per LED. EDN

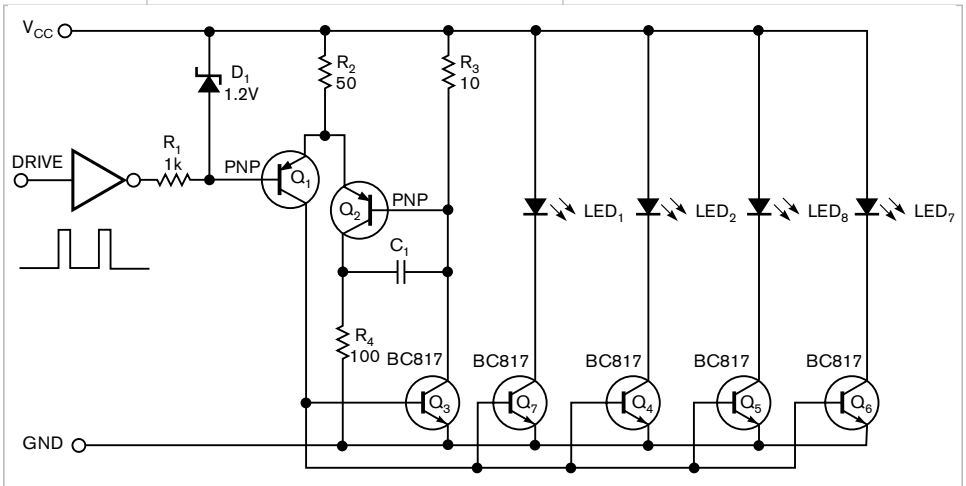

Figure 1 A pulsed-current mirror comprising transistors Q_4 through Q_7 drives multiple LEDs from a low supply voltage.

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READERS SOLVE DESIGN PROBLEMS

Program "excelerates" microcomputer-I/O allocation

Aubrey Kagan, Emphatec, Markham, ON, Canada

When I designed a system employing the LPC2138 ARM (www.arm.com)-based microcontroller, I quickly abandoned a pencil-and-paper approach to allocating the I/O. That method is tedious and error-prone because of the large number of pins on the microcontroller. Instead, I entered the data into Microsoft (www.microsoft.com) Excel (**Reference 1**). This approach let me assess the initial amount of I/O and any additional I/O that I would have to add. With the spreadsheet, I could create a rough bill of materials for a quote. Thereafter, it helped with the functional allocation and is an elegant and practical approach for almost any project. The online version of this article, at www.edn.com/081215dia, provides a sample spreadsheet that you can download.

First, you enter all the pins in ascending order (Column A in **Figure 1**). The LPC2138 can have as many as four functions per pin. Columns C to F show the functions and their corresponding pin numbers. Next, you insert the data-validation feature in each concomitant cell in Column B. When you click on a cell with this setup, a drop-down arrow appears, and a selection of the cells appears to the arrow's right. You click on any cell in Column B and then click on the "data" menu and then the "validation" menu to see the setup of data validation. You format cells for which no options are available, such as V_{SS}, with a black background because, at start-up, you can delete the whole column to initialize, but the color formatting will remain.

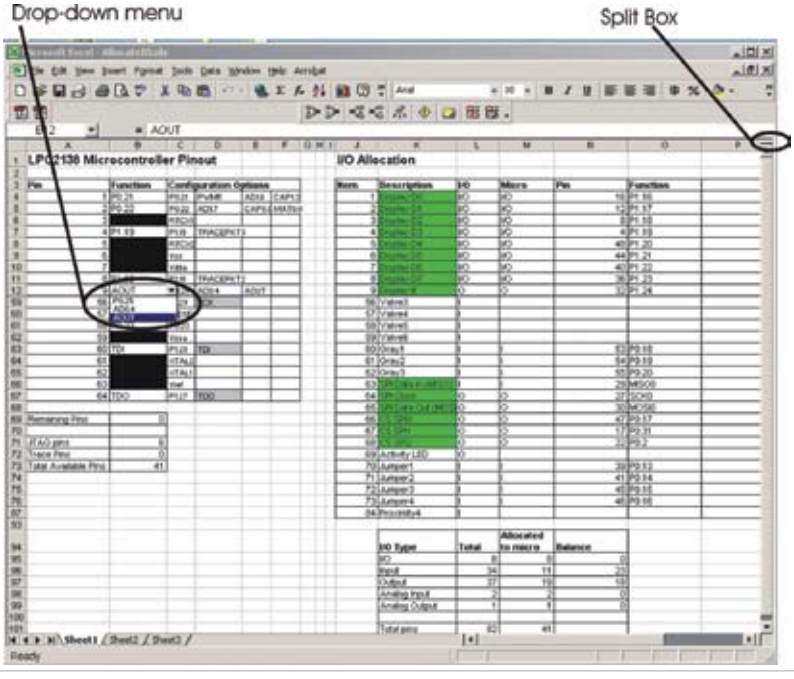

Figure 1 The completed worksheet has a large number of hidden rows to show the top and the bottom of the range.

You enter the project's I/O in the I/O-allocation table (columns J to O). You classify each pin as I (input), O (output), I/O (input/output), AI (analog input), or AO (analog output). You must allocate those pins to the microcontroller. Any I/O device that is not green is a direct user decision and not a function of anything else on the worksheet. Note that the information that appears in the pin column (Column N) is not the pin number but a reference to the pin number in Column A, so that, if you were allocating the function to Pin 8, the entry is "=A11," as it is in Cell N6. Column 12 contains a look-up formula that fetches the function name that appears in Column B to the right of the selected pin.

The bottom of each table (cells A69 to B73 and K94 to N101) includes

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some statistics on the usage and availability of pins based on the allocation to allow you to keep tabs on the allocation as it progresses. Cell M101 has conditional formatting, so it turns red if the pins you allocate to the microcontroller exceed the total number of pins available on the microcontroller as calculated in cell B73. You can add hardware I/O to the right of the table to ensure that you include all I/O.

The usage of the spreadsheet takes place as follows:

1. Delete cells B4 to B67.
2. Delete cells K4 to N87.
3. Create a list of project I/Os and fill in the I/O-allocation table. Insert rows for additional pins, remembering to update the entries in columns K and O.
4. Allocate those pins on the microcontroller that you cannot use for general I/O, such as the JTAG pins for emulation.
5. Drag down the split-box indicator so that the worksheet appears something like that in **Figure 2**.
6. In the upper pane, select the cell in Column B associated with the desired pin. Select the configuration from the drop-down box.
7. Go to the project-I/O function in Column N in the lower pane. Enter an equals sign and then click on the desired pin in Column A in the upper pane, scrolling up or down if necessary. The selected cell reference then fills into the formula. Complete the entry with the "enter" key.
8. Repeat for all the I/O.
9. Drag the split-box indicator back to the top to remove the screen split.

Some of the features in Excel can really make this model shine. For instance, the pin allocation of the LPC2138 does not follow the logical ordering of the pins. Perhaps it would help to see Port 0 listed in ascending order. You can use Excel's sort feature to group like functions together.

To see where the information comes from, click on any entry in Column N, select the "tools" menu item, then select "auditing" and "trace precedents." If you use this procedure with all the cells, you can visually trace unallocated or twice-allocated pins. A macro, "find all precedents," which is available in the Web version of this Design Idea at www.edn.com/081215dia, results in the screen in **Figure 3**. Another macro, "clear arrows," also available on the Web site, clears all these indicators. Unfortunately, because the look-up table in Column O includes a reference to Column A, you cannot use the antecedents' trace in the same manner. EDN

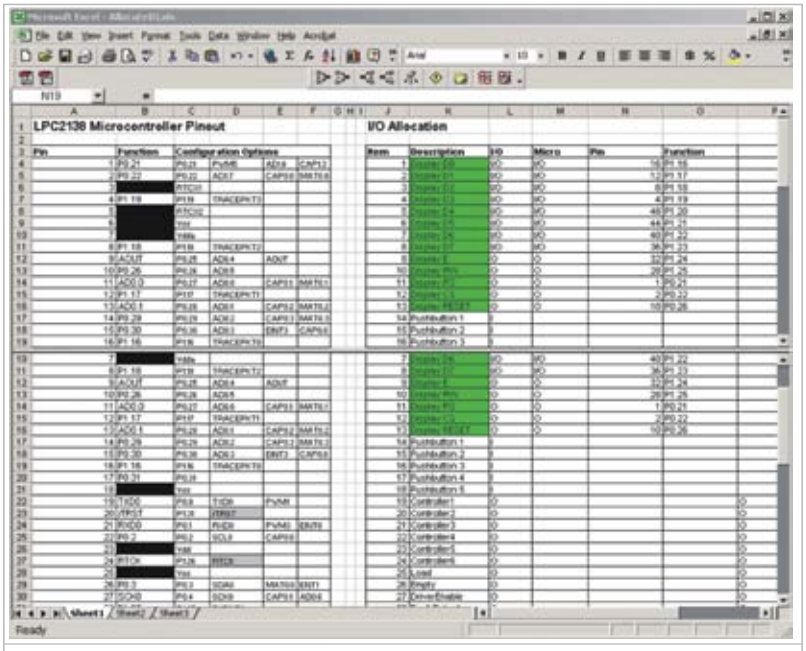

Figure 2 Two panes with the split box allow for easy pin allocation.

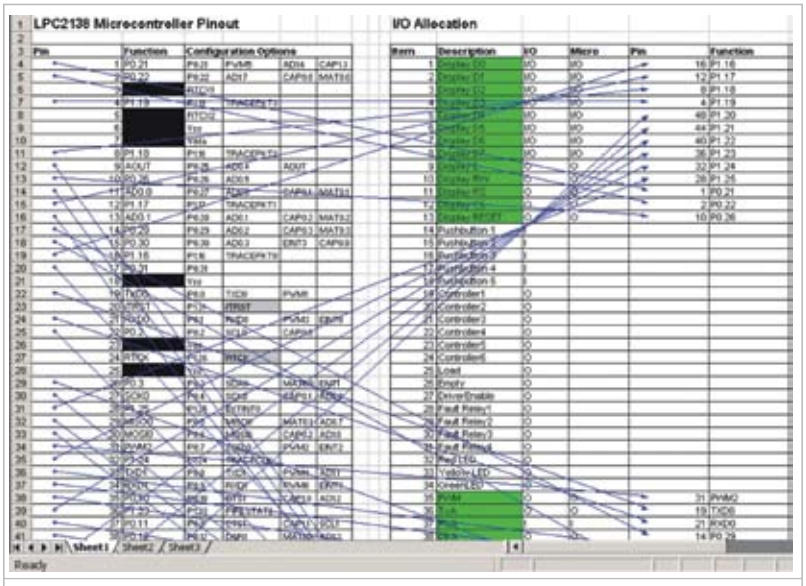

Figure 3 The precedent feature lets you verify that you have allocated all the pins and that each pin has a unique assignment.

REFERENCE

1 Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Elsevier/Newnes, May 2004, ISBN: 0750677562.

Microcontroller measures resistance without an ADC

Ashish Aggarwal, Netaji Subash Institute of Technology, Dwarka, India

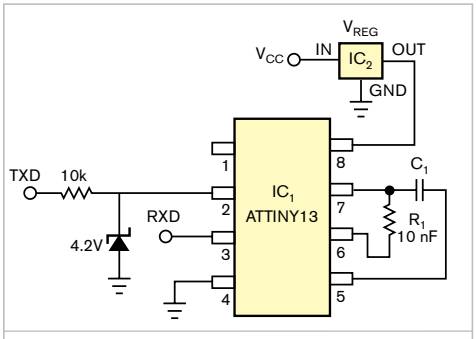

Figure 1 This circuit can measure resistance by measuring the frequency of a microcontroller configured as an astable multivibrator.

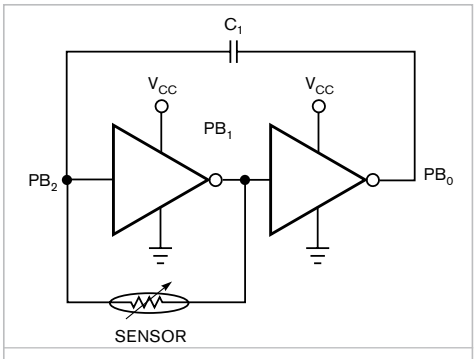

Figure 2 This design implements an equivalent oscillator based on the principle of an astable multivibrator in the Tiny13.

Sensors automate most of the processes in industry. Most of these sensors, such as those for ammonia gas, temperature, and the like, are resistive devices in which electrical resistance changes—mostly nonlinearly—as the surrounding conditions change. The sensors' resistances may vary from 1 mΩ to 10 MΩ. **Figure 1** illustrates a circuit for resistance measurement. The circuit uses an eight-pin AVR microcontroller, a Tiny13V from Atmel (www.atmel.com), for the controller. The Tiny13V works over a supply-voltage range of 1.8 to 5.5V.

This design implements an equivalent oscillator based on the principle of an astable multivibrator in the Tiny13 (**Figure 2**). The oscillator has no stable states, and the signal keeps oscillating between two quasistable states. This oscillator produces a frequency that depends on the value of the resistor. As resistance increases, frequency decreases, and you can easily measure this frequency to yield the value of the resistance.

The resistance you want to measure connects between any two general-purpose I/O pins of the microcontroller, and a capacitor, C_1, of known value connects across the other general-purpose I/O pin. Note that PB_0 and PB_1 are always in different states to implement a NOT gate. PB_2 measures a high or a low across resistor R_1.

Initially, PB_0 is high, PB_1 is low, and there is a high-impedance state at PB_2. As a result, the capacitor starts charging with time-constant RC. Note that the capacitor initially acts as a short, and PB_2 senses a high. As the capacitor charges, the voltage across the resistor decreases, and, when PB_2 detects a low, PB_1 goes high and PB_0 goes low.

Next, as the capacitor discharges, the potential across the resistor builds up, and, when PB_2 detects a high, PB_0 goes high and PB_1 goes low. In this fashion, measuring the frequency or half the number of toggles of PB_0 in a second gives an inverse relation of resistance, R_1 (in **Figure 1**), with frequency, f: $R_1=k/f$, where k is a proportionality constant. The result travels to a PC through a serial RS-232 interface. Because the Tiny13 has no UART, a software UART program and the program for measuring resistance are available with the Web version of this Design Idea at www.edn.com/081215dib.EDN

Five- to 10-LED flashlight circuit runs at 3V

GY Xu, XuMicro, Houston, TX

Almost all inexpensive commercial LED flashlights use a 4.5V power supply—three AA or AAA batteries—because white LEDs require 3.3 to 3.5V to fully turn on. Thus, there is a voltage gap between LEDs and traditional 3V incandescent-flashlight bulbs. The voltage difference makes for a difficult—but not impossible—transition from the old flashlight to an LED flashlight. The simple circuit in **Figure 1** solves this problem.

The circuit is just a typical voltage booster comprising six components that you can mount on a small PCB (printed-circuit board) measuring less than 1 in^2. Component selection and their values are, however, important. IC_1, an Atmel (www.atmel.com) ATtiny13 microcontroller, works as a charge pump for boost control. Its internal oscillator frequency is 1.2 MHz at 3.5V, and it can operate with voltages as low as 1.8V with low power consumption. The ATtiny13 has a small, eight-pin footprint.

Q_1 is a low-saturation-voltage ZTX618 NPN transistor that can handle more than 3A of collector current. D_1 is a Schottky diode with low forward-voltage drop to achieve high efficiency. When you apply the 3V supply-voltage power to IC_1, IC_1 outputs a high pulse that turns on Q_1. Its collector is effectively grounded. Inductor L_1 charges linearly from 0A to some peak current until IC_1 outputs a logic low, and Q_1 then turns off (**Figure 2**). This circuit works only when the inductor is not saturated, so choosing the right inductor is important. At that mo-

ment, the established magnetic field in L_1 collapses, causing a reverse induced voltage that makes D_1 conduct. The energy in L_1 transfers to C_2, which stores the energy until it is sufficient to light up the LEDs. The relationship between the supply voltage (V_{IN}), the inductor (L), its peak current (I_{PK}), and the microcontroller's on time (T_{ON}) is $V_{IN}=L\times I_{PK}/T_{ON}$.

For a supply voltage of 3V, you should select an inductor with a nominal value of 10 µH and a saturation current larger than 1.5A. You can calculate the microcontroller's on time as 5 µsec. **Listing 1**, which is available in the Web version of this Design Idea, at www.edn.com/081215dic, uses this value for the charge pump's on time. The program in **Listing 1** is so simple that it takes only 22 bytes of the 1-kbyte program memory. The charge-pump-control function is easy to understand. The instruction Sbi portb, 2 tells the microcontroller to output a logic high to turn on the charge pump. Because the microcontroller works at 1.2 MHz by its internal oscillator, each NOP (nonoperation) takes one clock cycle, or 0.83 µsec, to execute, so the on time is 5 µsec. Similarly, Cbi portb, 2 tells the microcontroller to output a logic low that turns off the charge pump.

Measurement shows that the circuit works at a 100-kHz switching frequency and that the actual output is 17V/35 mA for five LEDs and 32V/20 mA for 10 LEDs. Unlike the usual voltage-booster circuit, this circuit needs no resistor, which wastes energy and generates useless heat, as a voltage divider or a sensor.EDN

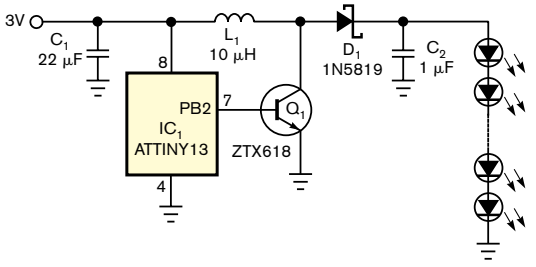

Figure 1 A charge-pump circuit creates the boosted voltage to light LEDs for a flashlight.

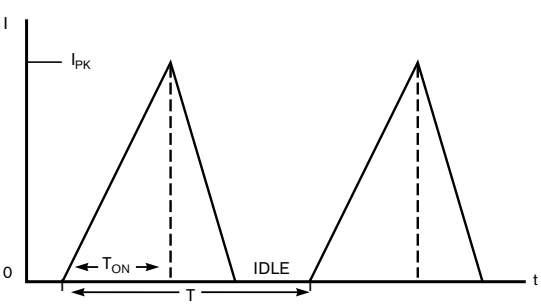

Figure 2 During the on time, current flows through the inductor and then charges the capacitor.