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OCTOBER

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Optically isolated overcurrent detector works from ac mains
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A diode ladder multiplies voltage under software control
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Mains-driven zero-crossing detector uses only a few high-voltage parts
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A few added components make a self-contained controller for 100A load
Simple night-light uses a photoresistor to detect dusk
Simple tester checks Christmas-tree lights

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READERS SOLVE DESIGN PROBLEMS

Test continuity with an LED

Raju R Baddi, Raman Research Institute, Bangalore, India

You sometimes need to know whether a resistance exceeds a preset limit. The continuity tester in **Figure 1** lets you determine that fact for resistances of 0.5Ω to 10 kΩ. The heart of the circuit is the transistor pair comprising Q_1 and Q_2, whose emitters draw current from a single source, R_E. Insert the circuit under test, R_{CY}, between Point A and Point B. To set the limit, use a known resistance for R_{CY} and set the trimming potentiometer until the LED begins to light.

The current through R_E divides between Q_1 and Q_2 in proportions based on the resistances of the two loops. The circuit lets you set the low limits to values as low as 0.5Ω because the emitter current in Q_2 can change rapidly with small changes in its V_{BE} (base-to-emitter voltage). The remaining current originating in R_E goes through the emitter of Q_1, whose collector then suffers voltage changes on the order of approximately 100 mV because most of a transistor's emitter current flows to its collector.

At extremely low limits, a large change in emitter current can easily accommodate the drop in voltage across R_{CY} in Loop 2. The extra current goes through Loop 1. At the critical value of R_{CY}, Loop 1 conducts a much higher current than Loop 2, which again means a much smaller V_{BE} change for Q_2.

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The online version of this Design Idea, available at www.edn.com/110106dia, includes an appendix that provides

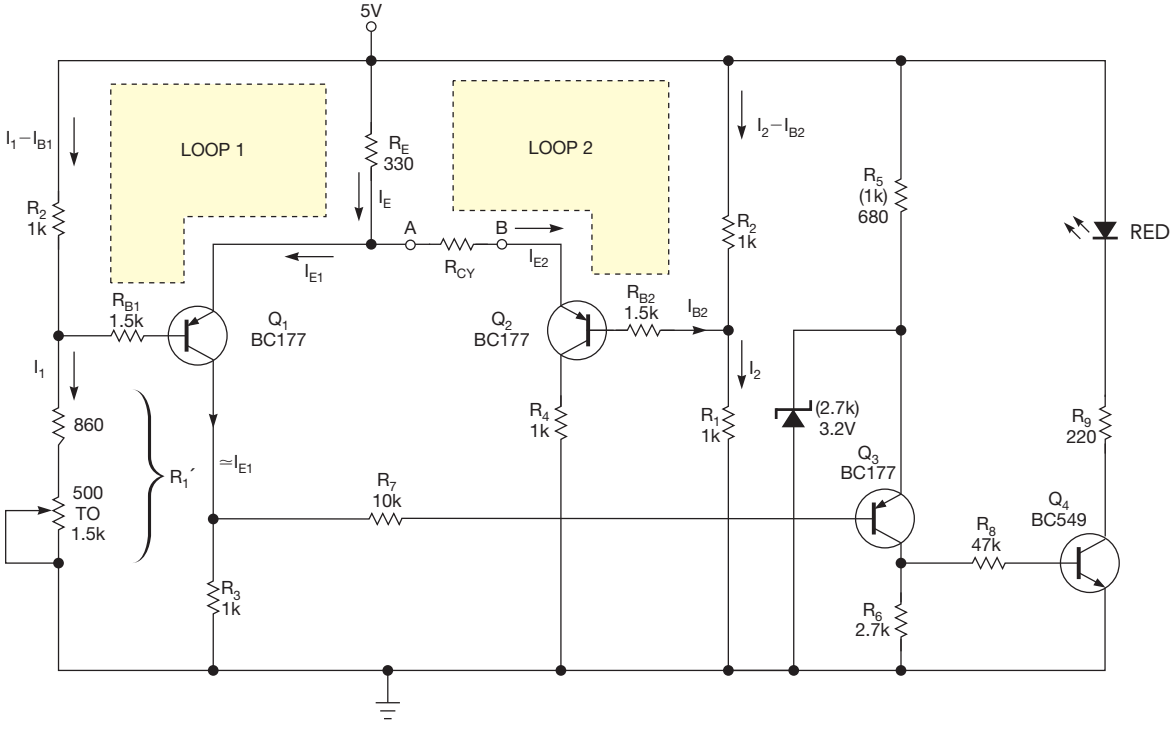

Figure 1 This continuity tester lets you know whether a resistance exceeds a preset limit.

a detailed analysis of the circuit's dc performance.

When R_{CY} is an open circuit or has a resistance above the set limit, a larger portion of the current through R_E flows to the emitter of Q_1, which produces a voltage across R_3. That voltage is close to the voltage at the emitter of Q_3. Thus, Q_3 doesn't have sufficient V_{BE} to turn on. In turn, Q_4 is off, and the LED doesn't illuminate.

When the resistance of R_{CY} is under the set limit, Q_2 begins to draw its share of current from R_E. This step reduces the current through the collector of Q_1, and the voltage drop across R_3 also decreases. The difference in voltages between the collector of Q_1 and the emitter of Q_3 exceeds V_{BE}. Q_3 then conducts, turns on Q_4, and lights the LED.

The tester's quiescent current is 10 mA, making the tester suitable for a bench instrument. If you need battery power, such as a 3.6V nickel-cadmium or lithium-ion battery, however, you can reduce the LED's series resistance by less than 47Ω and change Q_3's emitter voltage. (See the appendix, which is available online at www.edn.com/110106dia.)

Use two variable potentiometers in series whose values—1 kΩ and 100Ω, for example—differ by an order of magnitude. This approach allows you to make precise limit adjustments at lower limits.

The values in parentheses in **Figure 1** are substitute values. You can substitute five 1N4148 diodes for the 3.2V zener diode. Both arrangements perform well. The LED may go a bit dim toward the low limit, approximately 0.5Ω, so use one with a transparent lens. EDN

Flash an LED from ac-mains power

TA Babu, Chennai, India

LED technology is opening the door to a variety of high-power-illumination applications. The circuit in **Figure 1** can let you know when ac power is available. To drive a power LED from the ac line requires a converter or a similar arrangement. In this circuit, a passive dropper greatly simplifies the total design. You can also simplify the circuit to run on dc power, which lets you use it from automotive batteries to supply light at night.

The design comprises an inrush-limiting resistor, R_1; a half-wave rectifier with a filtering capacitor comprising D_2, D_3, D_4, and C_2; a relaxation oscillator; and two high-power LEDs. Because the circuit drives the LED with a constant current, you can use any LED color to suit the situation.

The circuit uses a simple DIAC (diode-alternating-current) relaxation oscillator, which activates a constant-current switching circuit comprising IC_2 and Q_1. The DIAC turns on when capacitor C_3 charges through diode D_1 and resistor R_2 from the mains voltage. After a number of half-cycles of the mains, the voltage on C_3 exceeds the break-over voltage of the DIAC, the DIAC conducts, and C_3 discharges through R_3 and optocoupler IC_1. The optocoupler activates the constant-current switching circuit, resulting in a brief, intense flash of light from the LEDs.

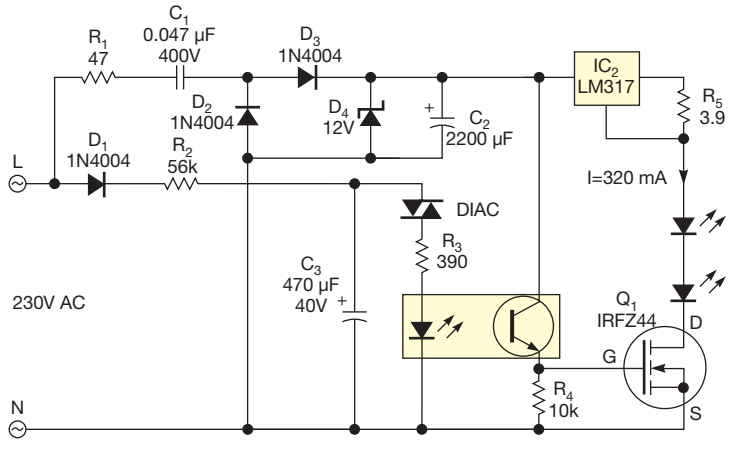

Figure 1 This circuit uses a simple DIAC relaxation oscillator, which activates a constant-current-switching circuit.

High-voltage capacitor C_1, part of the passive dropper, limits the current drawn from the power line, as the following **equation** shows:

$$I_{RMS} = \frac{V_{AC}}{X_{ACCAPACITOR}} = \frac{V_{AC}}{\frac{1}{2\pi FC}} = 2\pi FCV_{AC}.$$

A 47Ω metal-oxide resistor, R_1, acts as an inrush-current limiter. Because the LEDs require a lot of energy, it's not feasible to directly drive them using a small-value capacitive dropper. Instead, this circuit uses a 2200-µF capacitor, C_2, to collect and store energy from the power line between flashes. Zener diode D_4 limits the capacitor voltage to 12V.

The easiest constant-current approach is to use an adjustable linear regulator, such as Linear Technology's (www.linear.com) LM317. The regulator maintains a voltage of 1.25V across series resistor R_5. The 1.25V is the reference voltage of the regulator. Consequently, you can determine the load current with the following equation: $I_{LED}=1.25/R_5$. The active current limiting is 320 mA, which is sufficient to produce an intense light flash.

As a note of caution, this circuit has no galvanic isolation from the ac mains. Most nodes are, therefore, at mains potential and hence dangerous. You should not construct this circuit unless you have experience in handling high-voltage circuits. EDN

Reliable 555 timer doesn't falsely trigger

John Dawson, Opelika, AL

Circuits employing the popular 555 timer circuits are often reliable under many conditions. When you use them in electrically noisy environments, however, the timer can produce a false trigger, no matter how well you filter its power-supply lines. The circuit in **Figure 1** sends a pulse to an SCR (silicon-controlled-rectifier) crowbar circuit when the 555's input pulls low due to a fault-detection circuit. The 555 timer chip is unpowered until a crowbar fault signal occurs. The logic-low signal forces the 74LS02 NOR gate's output high, which provides enough power to operate to the 555 timer circuit. The timer triggers on power-up. Capacitor C_2 holds the trigger signal low until it charges to 5V. The 555 timer's output should drive a low-current device—in this case, a transistor switch. This circuit solves the problem of false triggers. The pulse transformers connect to two SCRs in series that pulse 1600 to 2000V dc to fire a crowbar for a 22-kV dc power supply. The SCR-controlled high-voltage power supplies are electrically noisy, causing many false triggers from the 555 timer circuit. EDN

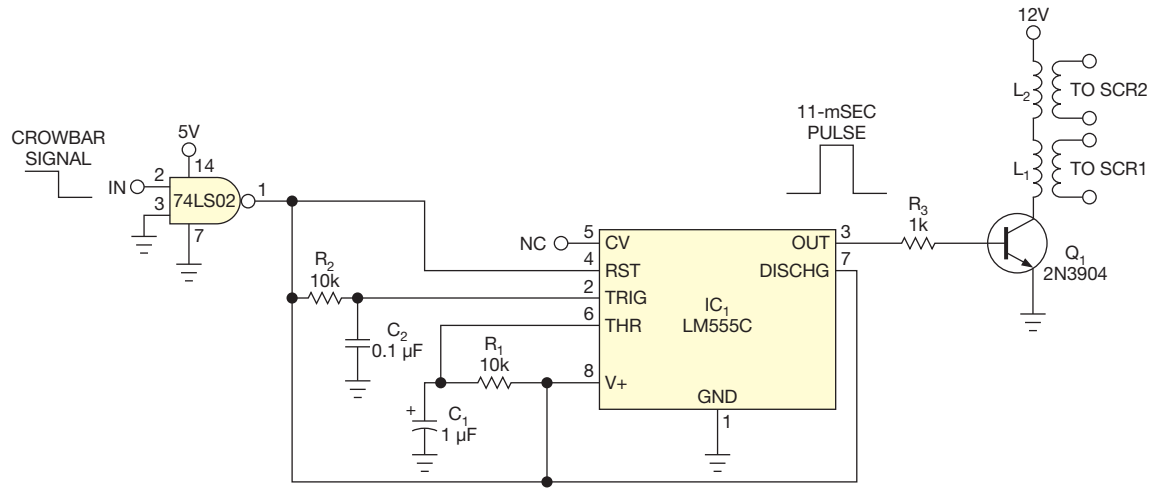

Figure 1 Powering the 555 timer from a NOR gate results in no false triggers from an electrically noisy environment.

Transistors drive LEDs to light the path

Eliot Johnston, Comnet International, Richardson, TX

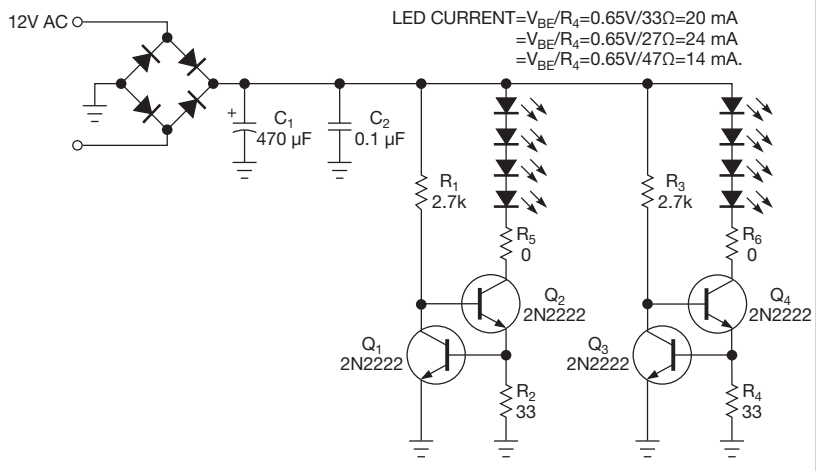

Figure 1 A simple two-transistor, two-resistor circuit is a good fit for outdoor-lighting applications.

Keeping low-voltage outdoor lights illuminated takes some effort. Bulbs burn out, and connections corrode. HB LEDs (high-brightness light-emitting diodes) seem like acceptable replacements, but most are available only in surface-mount packages, which aren't conducive to a backyard project. In addition, you must create a reflector for tiered lighting. Low-power LEDs, which come in finished packages, are more appealing, but you must have a way to drive them. Numerous driver ICs are available, but they, too, usually are available in surface-mount packages. Furthermore, the cost of the parts can add up to an expensive project. The simple two-transistor, two-resistor circuit in **Figure 1** provides a better fit for this application.

The two transistors and two resistors act as a simple current source. Q_1's base-emitter voltage, V_{BE}, combines with re-

Figure 2 Two identical circuits on a round PCB can drive eight LEDs, producing a relatively consistent light output.

sistor R_2 to set the LED current at approximately 20 mA. In this application, even a tolerance of ±10% doesn't significantly affect LED performance. Thus, only the value of R_2 is somewhat critical.

The 7 and 11W incandescent outdoor lights in this setup receive their power from a 12V-ac photoelectric timer. The bridge rectifier and filter capacitor produce approximately 15V dc—enough to drive four white LEDs, each with an approximately 3.2V forward-voltage drop. A small-value resistor, R_5, may be necessary to offload some of the power dissipation of the main pass transistor. In this setup, however, Q_2 dissipates only around 50 mW, so it can use just a jumper wire for R_5—hence, the schematic shows it with a value of 0Ω. Two identical circuits on a round PCB (printed-circuit board) can drive eight LEDs, producing a relatively consistent light output using Cree (www.cree.com) C535A-WJN series 110°-viewing-angle LEDs (**Figure 2**).

The lighting network uses two 144W transformers, which probably consume more energy than the new LED lamps. Once you replace all the bulbs with LEDs, power consumption should drop from approximately 200W to approximately 20W. You then connect the two strings together and remove one of the transformers. You could also build an efficient 120V-ac to 15V-dc power supply into the transformer housing and send dc down the wire rather than 12V ac.

SOLDER THE WIRES DIRECTLY TO THE PCB, LEAVING THE POTENTIAL FOR CORROSION AT THE CONNECTION TO THE MAIN WIRE.

You should use an automotive clear-coat spray to seal everything from moisture. This circuit should provide more than 10 years of service life. Contact corrosion causes reliability problems. Corrosion tends to set into the stab connection to the main wire and at the bulb itself. Instead of plugging in the replacement, you can solder the wires directly to the PCB, leaving the potential for corrosion at the connection to the main wire. Removing some insulation and soldering the wires makes for a more reliable connection. Remember to coat each splice with some silicon RTV (room-temperature-vulcanizing) sealant. EDN

Use an optocoupler to make a simple low-dropout regulator

Marc Ysebaert, De Pinte, Belgium

Although a monolithic low-dropout regulator has superior dynamic characteristics, the discrete regulator in this Design Idea is so simple that you can adapt it to many purposes. Using a common transistor, it has a dropout voltage of 0.1V. This dropout voltage can be even less if you use a FET. In the circuit in **Figure 1**, the optocoupler's LED determines the approximately 1V output voltage, which the circuit adds to the voltage of the zener diode. A low-current zener diode gives the best results because regulation occurs at less than 1 mA, depending on the current gain of the transistor. To regulate the voltage of one battery cell, you can omit the zener diode to a given output voltage of approximately 1V. You can also replace the zener diode with a potentiometer to obtain a variable output voltage. Another alternative is to use a combination of one or more LEDs or regular or Schottky diodes to obtain a fixed output voltage. You can insert a low-current LED as part of the voltage-reference branch to give an indication of the proper operation of the regulator.

The circuit in **Figure 1** consumes approximately 1 mA and starts to limit the current at currents higher than approximately 50 mA. With a lower value for the resistor, the LED glows brighter, the output voltage is slightly higher, and the current consumption and the current limit are proportionally high-

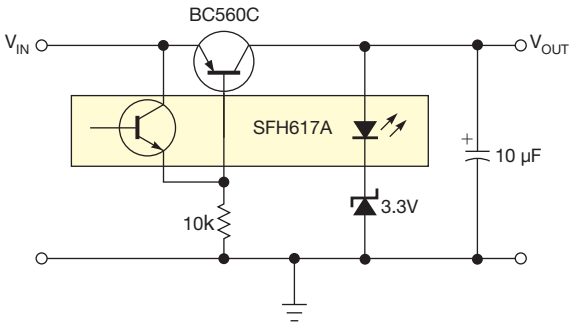

Figure 1 This simple low-dropout circuit is ideal for higher voltages that a zener diode sets.

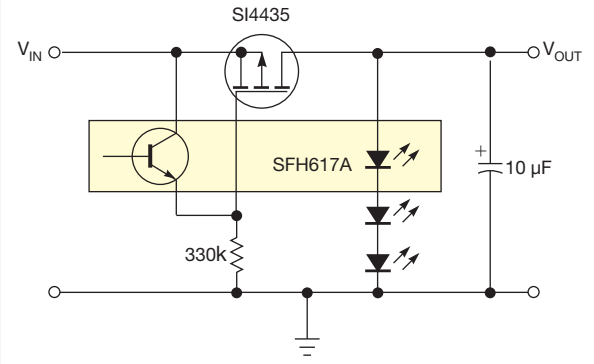

Figure 2 Using LEDs or diodes makes the circuit suited for lower regulation voltages.

er. You can replace the transistor and the optocoupler with almost any other type, but a high current gain and transfer ratio are preferable. When you use a high-voltage transistor, the input voltage can be much higher than is possible with common monolithic regulators. You can use a Darlington transistor for higher currents if your design can tolerate a dropout voltage of 0.7V. An output capacitor with a value of approximately 10 to 47 µF is necessary to avoid oscillation. Higher values are necessary for higher output currents. The circuit requires no input capacitor.

The circuit in **Figure 2** replaces the transistor with a P-channel FET and uses a 330-kΩ resistor. In this configuration, the circuit consumes about 50 µA and should suit many battery-powered devices. There is no inherent current limiting. You can reduce R_1 to 10 kΩ or lower to have a faster response to load change and to obtain a visual indication with the LEDs. EDN

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READERS SOLVE DESIGN PROBLEMS

Oscillator has voltage-controlled duty cycle

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

The classic Colpitts oscillator circuit in **Figure 1** generates a clock signal with a fixed duty cycle. By replacing CMOS inverter gate IC_{1A} with a voltage comparator (**Figure 2**), you can obtain a more versatile and more useful clock generator. You can set not only the oscillation frequency but also the duty cycle. You must use the comparator in an inverting configuration, which introduces a 180° phase shift. That shift, along with an additional phase shift of 180° from the capacitor-input network, lets the circuit oscillate. The circuit compares the sine wave at the output of the capacitor-filter network with the reference voltage, which drives the output of the threshold comparator high and low.

The network sets the oscillation frequency as follows:

$$f_O=\frac{1}{2\pi\sqrt{LC/2}},$$

where f_O is the oscillation frequency. With a suitable choice of the values of inductors and capacitors, the circuit can oscillate at frequencies as high as 10 MHz.

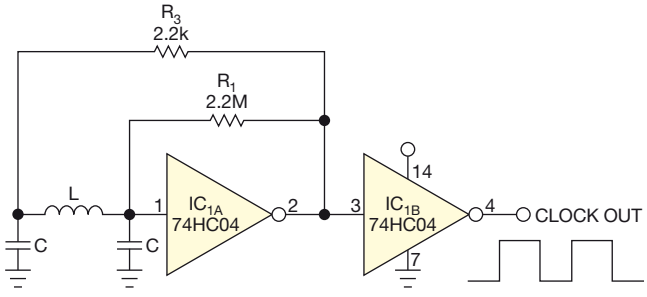

Figure 1 A typical Colpitts oscillator uses an inverter and has a fixed duty cycle.

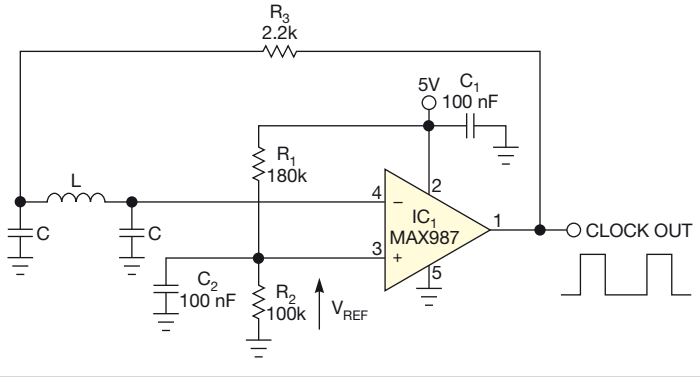

Figure 2 A comparator lets you vary the duty cycle based on resistors R_1 and R_2.

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The output clock's duty cycle depends on the reference voltage, which you can easily set through the voltage divider comprising R_1 and R_2. Unfortunately, the mathematical relationship between the reference voltage and the duty cycle is nonlinear because the sine wave at the output of the capacitor-input-filter network is not a linear function. Also, its amplitude is not constant but depends on the duty cycle of the output clock. You can easily obtain this mathematical relationship by testing the circuit with an inductance of 10 µH and a capacitance of 10 nF.

You can use any high-speed compara-

TABLE 1 OSCILLATOR DUTY CYCLE BASED ON REFERENCE VOLTAGE

Reference voltage (V)	Duty cycle (%)
0.5	15.2
1	28.3
1.5	37
2	43.5
2.5	50
3	56
3.5	62.6
4	71.5
4.5	85.4

tor with rail-to-rail inputs and outputs, such as the MAX987 from Maxim (www.maxim-ic.com), to achieve a wider input range for the reference voltage. That wider range gives you wider control of the duty cycle, although you can't reach the minimum duty cycle of 0% or the maximum duty cycle of 100%.

The propagation delay, T_{PD}, of the comparator introduces a further phase shift of value $\Delta\phi=2\pi f_O T_{PD}$, where $\Delta\phi$ is the phase shift. The capacitor-input network compensates for the phase shift, slightly reducing the oscillation frequency. For safe operation of the circuit, you should vary the reference voltage by 0.5 to 4.5V. The duty cycle varies from approximately 15 to 85% (**Table 1**). You can produce a bipolar output signal if you use a dual power supply. EDN

Generate noisy sine waves with a sound card

José M Miguel, RF-Electronics Ltd, Barcelona, Spain

Testing audio-noise-reduction circuits, PLLs (phase-locked loops), and audio-frequency filters may require a noisy sine wave, one that is summed with white noise. Using a typical computer sound card, free software, and an external amplifier circuit, you can create a noisy sine wave.

Free Generatosaur software from Wavosaur (www.wavosaur.com) turns your sound card into a low-frequency wave generator. It lets you independently choose amplitude, frequency, and waveform for the left and the right channels. The Generatosaur's user interface is a dialogue-box-style control panel (see **figure** at www.edn.com/110120dia). If you select a sine wave for the left channel and a white noise for the right channel, you then need only to use an amplifier to add the signals. **Figure 1** shows the complete circuit.

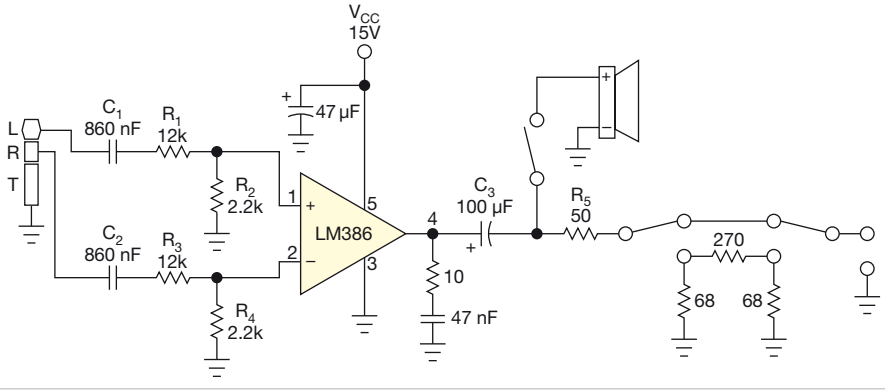

Figure 1 Generatosaur is free software that turns your sound card into a low-frequency wave generator.

The differential amplifier employs a National Semiconductor (www.national.com) LM386 audio power amplifier with a supply voltage of 15V. The output of the LM386 has a self-centered quiescent voltage that is half the power-supply voltage and that requires a blocking capacitor, C_3. Resistor R_5 sets the output impedance to 50Ω. You need the voltage dividers R_1/R_2 and R_3/R_4 because the output-voltage range for a standard sound card is 0 to 2V. Taking into account that the voltage gain of the LM386 amplifier is internally set to 20 and that its output voltage range is 7V, you need an attenuation factor, K, of 7/(2×20) in each amplifier input. The circuit also includes a selectable 20-dB attenuator that you can invoke with the two DPDT (double-pole/double-throw) switches.

Another **figure**, also available at www.edn.com/110120dia, shows a 450-Hz sine wave with a 10-dB SNR (signal-to-noise ratio). The root-mean-square noise voltage of this signal is 0.5V measured on an oscilloscope and following the tangential method. If you need to hear the generated noisy signal, connect a loudspeaker to the output of IC LM386. EDN

Decode a quadrature encoder in software

Sid Levingston, Gentec-EO, Lake Oswego, OR

Quadrature encoders work in many applications to determine displacement and direction of mechanical travel. They vary in design, but they all do the same thing: supply a set of square waves 90° out of phase. **Figure 1** shows the typical output signals.

The encoder rotates clockwise when Channel A leads Channel B. If Channel B leads Channel A, the encoder is rotating counter clockwise. By counting the pulses and the direction of rotation, you can find the position of the encoder. Although ICs can decode quadrature encoders, you can easily and less expensively have the processor decode the signal. The signals from Channel A and Channel B go through a Schmitt trigger if necessary, but many encoders and processors include this trigger internally. The signals are then applied to two I/O pins on the processor that support edge-triggered inter-

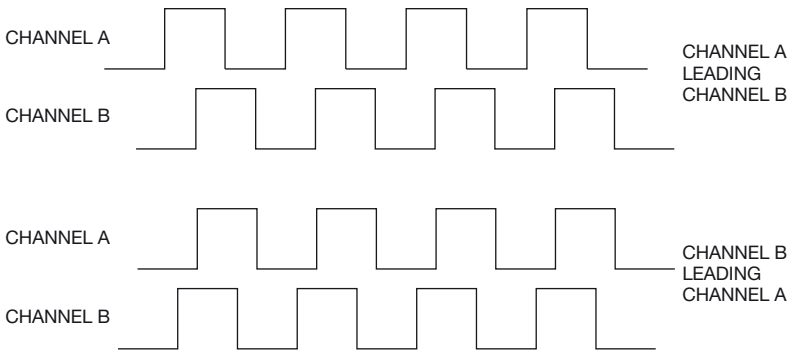

Figure 1 A quadrature encoder produces pulses that are 90° out of phase.

rupts. The code in the interrupt handler implements a standard decoder algorithm, but all algorithms typically follow these steps:

1. Set up a state table like the one in **Table 1**. The table wraps around from State 3 to State 0.
2. Initialize a counter.
3. Measure the current state of Channel A and Channel B. Find that state in the table and set a pointer to it.
4. Enable the interrupts.

In the interrupt handler, use the following steps:

1. Read the state of Channel A and Channel B.
2. If the state is the one preceding the pointer, decrement the counter.
3. If the state is the one following the pointer, increment the counter.
4. Set the pointer to the new state.
5. Clear the interrupt.

This method requires that a state table exists, that the previous state remain, and that the handler determine on each interrupt which of four states exists and then make a decision based on two possible conditions. The handler accomplishes this task with a four-case switch, in which each case has two if conditions.

Now, consider what happens in the real world. If the I/O pin generates an interrupt on a rising edge, then when the interrupt happens, that channel goes from low to high. Therefore, there's no reason to read the state of the pin that interrupted. The other channel did not interrupt because the signals are 90° out of phase. So, to determine the current state, you need only to read the state of the pin that didn't initiate the interrupt. The state of the unchanged low or high signal tells which way the encoder rotated. If it is low, then the interrupting pin is leading. If it is high, then the interrupting pin is trailing. You can use these facts to implement an efficient interrupt handler with no state table and no memory of a previous state.

The code in **Listing 1** was tested on an MSP430F processor connected to an Encoder Products (www.encoder.com) model 15T. The encoder monitored the position of a linear stage. The stage traveled 85 mm and could be tracked with resolution of 5 microns.

The define statements (highlighted in red) make the code more readable. The initPort() function (highlighted in blue) sets up the rising-edge interrupt on channels A and B. The final piece is the interrupt handler (highlighted in green). Note that it contains only six lines of code compared with the 20 or 30 lines it would take to implement the traditional method of decoding the channels. EDN

TABLE 1 LOGIC STATES OF QUADRATURE ENCODER

	Channel A	Channel B
State 0	0	0
State 1	1	0
State 2	1	1
State 3	0	1

LISTING 1 QUADRATURE-ENCODER CODE

```
#define CHA BIT0
#define CHB BIT1

initPort()
{
  P1SEL = 0;
  P1DIR = 0;
  P1OUT = 0;
  P1IES = 0;    // rising edge.
  P1IE = CHA + CHB;    // interrupt on CH A or CH B rising edge
}

#pragma vector = PORT1_VECTOR
__interrupt void port1_ISR (void)
{

  if(P1IFG & CHA )  // who interrupted? If A then A is high
   {
    (P1IN & CHB) ? gStepCount--  : gStepCount++ ;   // test B
     P1IFG &= ~CHA;    // clear interrupt
   }

  if(P1IFG & CHB ) // who interrupted? If B then B is high

   {
    (P1IN & CHA) ? gStepCount++  : gStepCount-- ;  // test A
     P1IFG &= ~CHB;     // clear  interrupt
   }
}
```

Power an LED driver using off-the-shelf components

TA Babu, Chennai, India

High-power LEDs challenge electronics engineers to design accurate and efficient, yet simple, driver circuits. Conventionally, driving high-power strings with accurate current requires dedicated switching regulators. Choosing a discrete driver circuit requires an understanding of LED lighting to make the best trade-off. This Design Idea describes a simpler and equally good way to employ the ubiquitous 555 IC.

In the converter circuit in **Figure 1**, IC_1's pins 2 and 6 connect together, which lets the device retrigger itself on each cycle. Thus, it operates as a free-running oscillator. During each cycle, capacitor C_2 charges up through timing resistor R_1 and discharges through resistor R_2. The capacitor charges up to two-thirds of the power-supply voltage, the upper comparator limit, which $0.693(R_1C_2)$ determines, and discharges itself down to one-third the power-supply voltage, the lower comparator limit, which $0.693(R_2C_2)$ determines. The total time period, T, is $0.693(R_1+R_2)C_2$.

ONCE THE VOLTAGE DROP REACHES THE BASE-EMITTER THRESHOLD OF TRANSISTOR Q_2, IT STARTS CONDUCTING.

During the on time, transistor Q_1 conducts and stores the energy in inductor L_1. When it stops conduction, the stored energy transfers to capacitor C_3 through Schottky diode D_1.

You can use the following **equations** to calculate the inductor value. The selection of an inductor depends on input voltage, output voltage, maximum current, switching frequency, and availability of standard inductor values. Once you know the inductance, you can choose the diode and the capacitor.

MOSFET Q_1 determines the duty cycle, according to the following **equation**:

$$D=1-\frac{V_{INMIN}\times\eta}{V_{OUT}},$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the desired output voltage, and η is the efficiency of the converter, estimated at 80%.

The average inductor current is

$$I_{LAVG}=\frac{I_O}{1-D},$$

where I_{LAVG} is the average inductor current and I_O is the output current.

The peak inductor current is

$$I_{LPEAK}=I_{LAVG}+\frac{\Delta I_L}{2},$$

where I_{LPEAK} is the peak inductor current and ΔI_L is the change in inductor current.

Assume that the change in inductor current is 25% over the average current. You can compute inductor L_1 as

$$L=(V_{IN}\times D)/(F_{OSC}\times\Delta I_L),$$

where F_{OSC} is the oscillator frequency. The inductor's saturation-current rating should be greater than the peak current.

To ensure constant illumination, you must monitor the current through the LED. Resistor R_3 senses the output current. Once the voltage drop across this resistor reaches the base-emitter threshold of transistor Q_2, it starts conducting, and this conduction reduces the on time of the 555 timer.

The following **equation** thus sets the LED current:

$$I_{LED}=\frac{0.6V}{R_{SENSE}},$$

where I_{LED} is the LED's current and R_{SENSE} is the sense resistance.

The minimum and maximum input and output voltages for this circuit are 10.5 and 15V, respectively. The LED string's voltage and current are 21V and 350 mA, respectively. The 6W LED driver can find numerous applications, including battery-operated portable lighting, solar-operated garden lighting, automotive lighting, bike headlights, and underwater lights. Driving high-power LED strings with standard off-the-shelf components simplifies your design without sacrificing performance. EDN

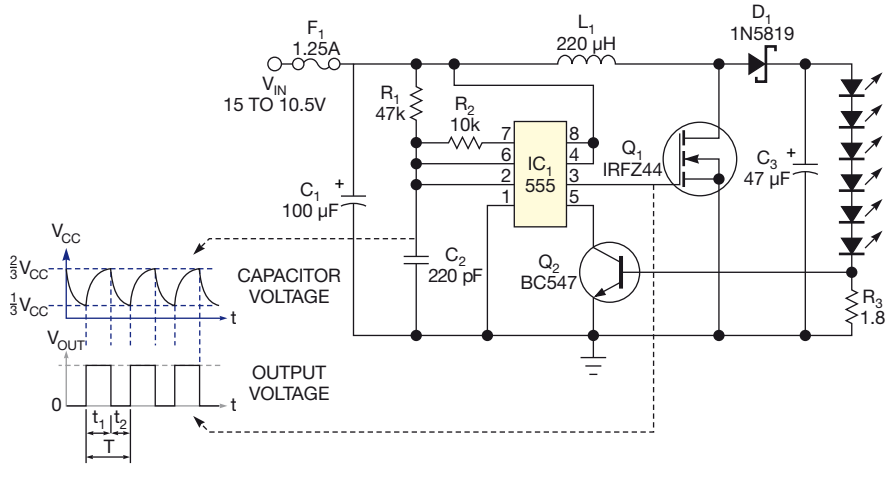

Figure 1 A free-running 555 timer provides the stimulus for driving a series of LEDs.

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READERS SOLVE DESIGN PROBLEMS

Compute a histogram in an FPGA with one clock

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Histograms are often useful tools for analyzing digital data. To get reliable results from a histogram, though, you must collect large amounts of data, often with 100,000 to 1 million points. If you need to collect an ADC's digital outputs for analysis, you can use an FPGA (**Figure 1**).

The **figure** shows the histogram, RAM, and pulse-generator blocks, which let you capture and display the histogram computation based on 14-bit data. The RAM block is the FPGA's built-in RAM, and the histogram block is the VHDL (very-high-level-design-language) code to compute the histogram. You can also download the VHDL code for this application from the online version of this Design Idea at www.edn.com/110203dia.

The 14-bit parallel data, Device_Data[13..0], from an ADC goes to the histogram block and to the RAM Rd_Addr input. The RAM provides the data at its address location, RAM-DataOut[15..0]. This data loops back to the histogram block, which increments it by one and sends it to output pin DataOut[15..0], a 16-bit data output. When the WREN (write-enable) pin is at logic level one, the data is written at the address at pin Wr_Addr[13..0]. That approach is the same as if the data were coming from Device_Data[13..0].

The RAM has a fixed delay from its input to its output. That is, when the input is at Rd_Addr, data becomes available at its output pin, RAM-DataOut, after a fixed delay. This delay might vary across the FPGA. To take care of this delay, allow a two-clock delay to Device_Data before calculating the histogram. The delay in RAM should be less than two clock periods; otherwise, there could be data loss. This constraint limits the maximum frequency of Device_Clk.

The Cntr_Value gives the number of input data for which the histogram block computes the histogram. To reset the

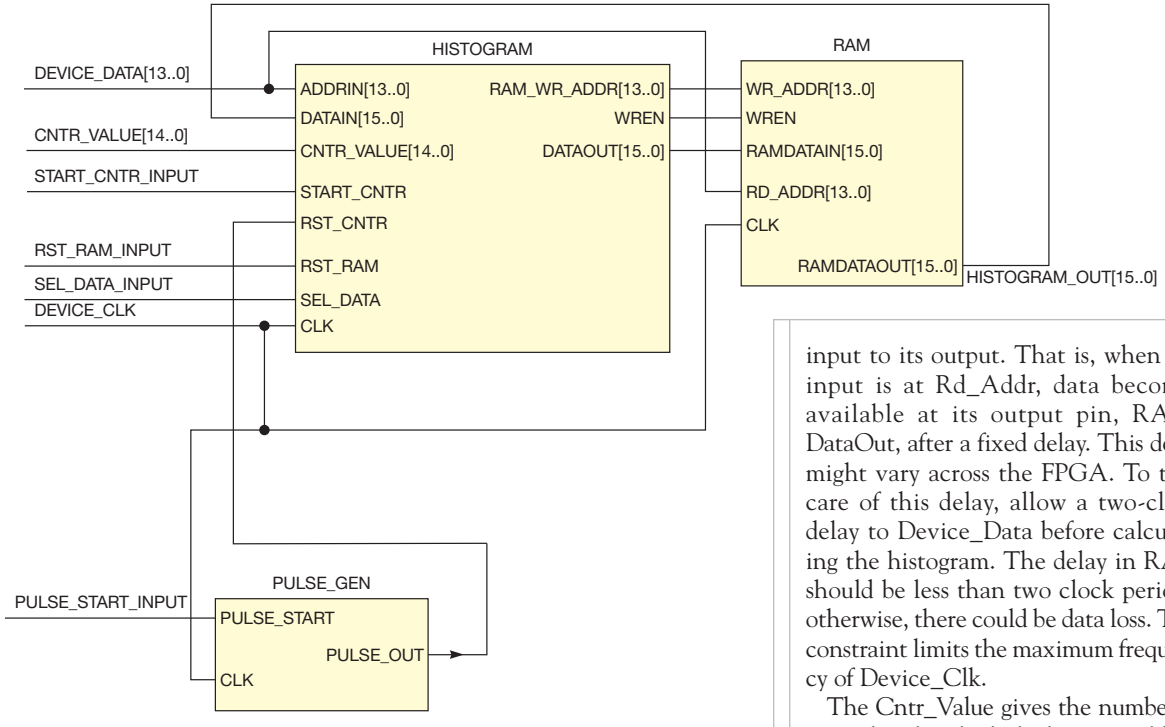

Figure 1 A histogram computational circuit retrieves data from an FPGA's RAM block.

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counter, the Pulse_Gen block generates a pulse, which enters at input Rst_Cntr. At this point, the histogram again computes the histogram for the next set of input data from Cntr_Value. The Cntr_Value is 15 bits, but you can increase it to collect more histogram data.

The signals Sel_Data and Rst_RAM reset the data stored in the FPGA's RAM. Whenever the high signal is at the Rst_RAM pin, the DataOut pin of the histogram block gives all bits as 0. When the high signal is at the Sel_Data input pin of the histogram block, the output from RAM_Wr_Addr is not the Device_Data but an internally generated ramp that ramps up from 0 to 16,384. The histogram block does no computation because doing so would reset the address of the RAM.

When the FPGA completes the histogram computation, the RAM can read the histogram data by selecting Sel_Data as logic high and keeping Rst_RAM as logic low. The data in the RAM address sequentially exits the output pin, and you can transfer the data to a PC. Because all the blocks run on a single clock, Device_Clk, the design is simple and helps you meet timing constraints. You can easily modify the design to accommodate 16- or 12-bit data histograms. EDN

Protect MOSFETs in heavy-duty inductive switched-mode circuits

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The MOSFET power switch is commonly the most vulnerable part of a new switched-mode high-power circuit. One threat for this device is exceeding the value of the maximum allowed pulse current. You cannot exceed this limit, even for pulse durations as short as 10 nsec. You could still thermally damage the MOSFET with a high duty cycle even when the drain-to-source current has a value between the peak and the dc ratings. The FET might eventually enter self-oscillations at a frequency, which might be an order of magnitude higher than your planned operating repetition rate. To protect the FET, you can limit the duty cycle by ac coupling the FET-driver circuit. If you further limit the repetition rate to tens of kilohertz, you needn't worry about thermal considerations.

To limit the duty cycle of the pulses, use the Schmitt-trigger input of IC_1 (**Figure 1**). You pass the input-voltage waveform through a derivative circuit comprising C_D, R_D, and R_S. The low-to-high transition of the clock causes an abrupt rise of voltage at resistor R_D. The output of the noninverting driver therefore goes high. Immediately after this transition, the voltage on R_D starts to decrease exponentially. When it falls below V_{TL}, the lower threshold of input IN_A, output OUT_A abruptly falls to 0V. The time constant $(R_D+R_S+R_{GEN})\times C_D$ yields the rate of exponential decrease. R_{GEN} is the output resistance of the generator of the input clock. You can calculate the value of capacitor C_D using the desired pulse width, T_P:

$$C_D=\frac{T_P}{R_D+R_S+R_{GEN}}\times\frac{1}{\ln\left[\frac{V_{DD}}{V_{TL}}\times\frac{R_D}{R_D+R_S+R_{GEN}}\right]}.$$

The **equation** employs an estimate of

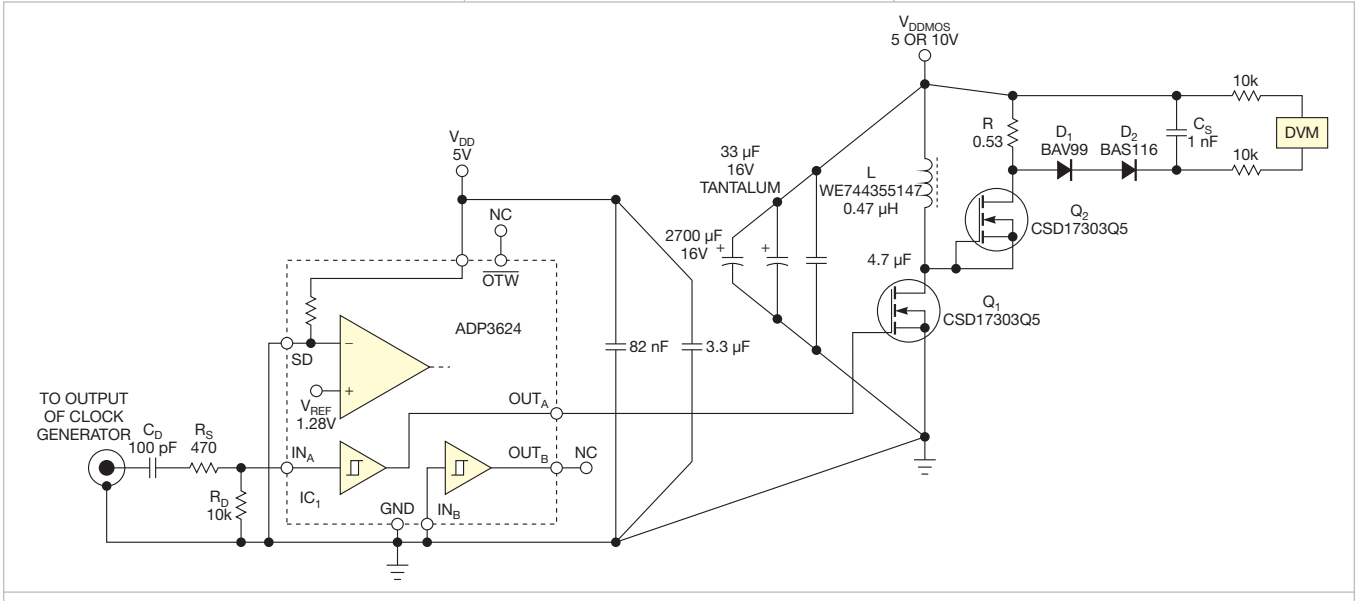

Figure 1 The test setup allows you to operate a MOSFET power switch at a fixed turn-on time. The power circuit remains cool with a 10-kHz repetition rate, even at peak inductor currents of tens of amperes.

the value of V_{TL}:

$$V_{TL} \simeq \sqrt{V_{INL} \times V_{INH}} - 0.1V = 1.165V.$$

The IC's data sheet gives the values of 0.8 and 2V as the limits of the low and high input voltages, respectively. The high-to-low transition of the clock has no effect. This transition causes a sharp negative exponential pulse, which an internal Schottky diode at input IN_A suppresses. The anode of this internal diode connects to ground, and its cathode connects to input IN_A. Resistor R_S limits the peak current flowing through the protective diode to about 10 mA.

The IC has an output current of ±4A. The typical on-resistance of Q_1 is 2 mΩ. You interconnect Q_2's gate and source pins to create a freewheeling diode. This diode has a typical reverse-recovery time of 33 nsec at a 25A forward current. When Q_1 turns off, the peak inductor current flows through Q_2. Voltage V_R occurs on power resistor R and is superimposed onto the supply voltage, V_{DDMOS}. The sum of these voltages must be lower than or equal to the manufacturer's specified value of the drain-to-source voltage of transistors Q_1 and Q_2.

When testing the circuit, you should monitor the dc-supply current. You can calculate the ideal-case supply current as a function of supply voltage on the power section and the pulse period as follows:

$$I_{SID} = \frac{1}{2} \times \frac{V_{DDMOS} T_{PON}^2}{L} \times f_{REP} = \frac{1}{2} I_{LPEAK} T_{PON} f_{REP}.$$

You calculate the pulse width of a single interval when the channel of Q_1 is conductive as an approximation relating the rise, fall, on, and off times of the FET:

$$T_{PON} \simeq T_P + t_{DOFF} - t_{DON} + t_{DMOSOFF} - t_{DMOSON} + (t_R + t_F) \times \left(\frac{1}{2} - \frac{V_T}{V_{DD}} \right).$$

The sum of differences in the propagation delays of IC_1 and Q_1 is positive and totals 32.1 nsec. V_T is the gate-to-source threshold voltage of Q_1. The data sheet gives a typical V_T of 1.1V, and the supply voltage, V_{DD}, has a value of 5V. These values yield 9.8 nsec for the last term of the preceding **equation**. T_{PON} is thus larger by 41.9 nsec. For a good design, an ammeter will indicates a supply current one to 1.5 times the ideal value of the current.

You can check the peak voltage at load resistor R. D_1 and D_2 and storage capacitor C_S function as a peak detector. The peak-voltage pulses at resistor R cause a dc voltage at C_S of roughly the same value as the peak voltage. You can determine the peak current flowing through the inductor from the voltage at the peak detector using the following **equation**:

$$I_{LPEAK} \simeq \frac{V_{RPEAK}}{R}.$$

Set the auxiliary supply voltage at 5.078V, the supply voltage at 10V, and the clock-pulse repetition frequency to 11,387 Hz. This approach causes the supply's current to be 0.327A and the peak voltage to be 16.4V. The peak current of the inductor reaches 30.94A. The experimentally determined turn-on time is approximately 1.502 µsec.

The IC driver contributes to the protection of the MOSFETs with an undervoltage lockout. If the supply voltage is on, but the auxiliary supply voltage is off, a voltage could get from the IN_A pin through internal protective diodes to the V_{DD} pin. The undervoltage lockout disables the control outputs until the auxiliary supply's voltage reaches a typical value of at least 4.2V.

The 0.65-mΩ dc resistance of ferrite-core inductor L might seem to be overrated for the circuit. However, the slope of current pulses in the inductor represents a megahertz-range equivalent frequency. The effective resistance at these slopes increases due to the skin effect and the proximity effect. This effective resistance can be many times the dc value. EDN

Control an LM317T with a PWM signal

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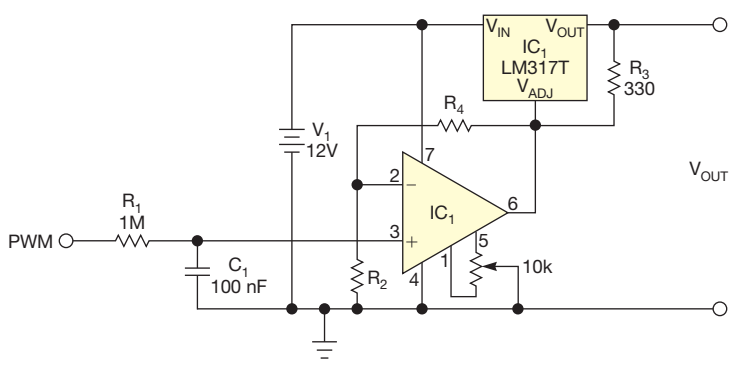

Figure 1 This circuit replaces a potentiometer with an analog voltage that you can control from a PWM signal.

The LM317T from National Semiconductor (www.national.com) is a popular adjustable-voltage regulator that provides output voltages of 1.25 to 37V with maximum 1.5A current. You can adjust the output voltage with a potentiometer. The circuit in **Figure 1** replaces the potentiometer with an analog voltage that you can control from a PWM (pulse-width-modulation) signal. You control this signal with a microcontroller or any other digital circuit. You can use the same microcontroller to dynamically monitor the output and adjust the LM317T.

Using an RC lowpass filter and an op amp, you can convert the PWM signal to a dc level that can adjust the

LM317T's voltage output. Varying the pulse width of the input signal lets you generate an analog voltage of 0 to 5V at the output of the lowpass filter. The op amp multiplies the voltage to achieve the desired voltage range.

For scenarios in which you must multiply the input voltage by two, the LM317T's adjustment pin receives 0 to 10V. Its output-voltage range is 1.25 to 11.25V. The **equation** $V_{OUT}=V_{ADJ}+1.25V$ governs the LM3175T's output voltage. You can change the op amp's gain by choosing proper values for R_4 and R_2. You must be able to remove offset voltages from the op amp. Use an op amp, such as a National Semiconductor LM741, with null adjustment. The selection of values for the capacitor and resistor for the RC lowpass filter depends on the PWM signal's frequency. This circuit uses values for a 1-kHz PWM signal.

YOU CAN IMPROVE THE CIRCUIT BY REPLACING THE RC LOWPASS FILTER WITH AN ACTIVE FILTER.

You can improve the circuit by replacing the RC lowpass filter with an active filter and then feeding a feedback signal from the circuit's output into the microcontroller for dynamic adjustments. EDN

High-speed buffer comprises discrete transistors

Lyle Russell Williams, St Charles, MO

Circuits sometimes need a gain-of-one buffer to lower output impedance and prevent the load from interfering with the previous stage. For an application involving a 1.5-MHz, low-power transmitter and antenna, a Burr Brown (www.ti.com) BUF634 buffer IC would work, but a discrete transistor buffer may be more convenient and less expensive than the IC.

Figure 1 shows the classic design of such a buffer. This circuit can drive a load as low as 200Ω with a peak output voltage of 2V. The maximum collector current of the transistors limits the output. You can use larger output transistors if your application requires more output current. Trimmer resistor R_4 across the diodes is, however, a relatively expensive part, and you must adjust it to produce the correct bias current for Class

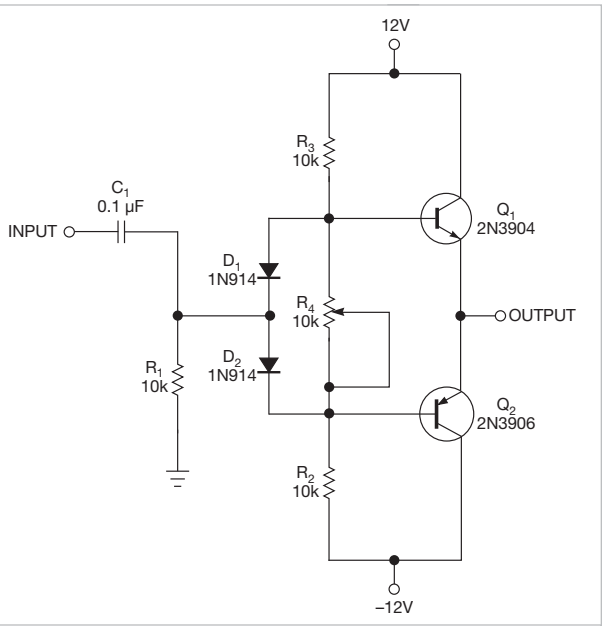

Figure 1 A typical buffer can drive loads as low as 200Ω.

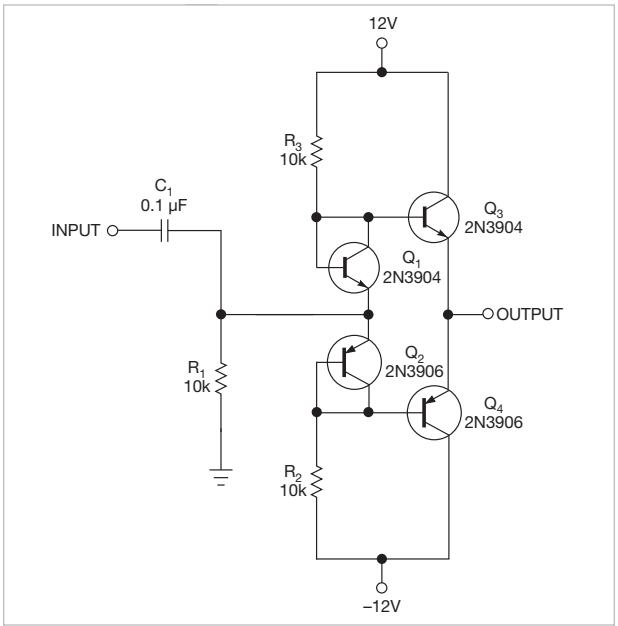

Figure 2 Current-mirror transistors replace the diodes in Figure 1.

AB operation. The adjustment is likely to drift over time.

A simpler circuit, such as the one in **Figure 2**, uses current-mirror transistors Q_1 and Q_2 instead of diodes. Resistors R_2 and R_3 set the zero-signal bias current in the bias-transistor circuits. The current-mirror effect causes the current in the output transistors to be nearly equal to the current in the bias transistors—approximately 1.2 mA in this case.

Because the current-gain-bandwidth product of the 2N3904 and 2N3906 transistors is 300 MHz, this circuit should work at 100 MHz or higher frequencies. At these frequencies, however, the circuit layout may be critical, and the slew rate, which is unknown, may limit usefulness. The offset of the circuit is approximately 0.1V, which is not a problem for this application because the circuit uses capacitive coupling through C_1. If you use the buffer in the feedback loop of an op amp, the op amp can null the offset.

You may want to monitor the current in the output transistors, so the circuit in **Figure 3** adds 100Ω resistors R_3 and R_4 and 10-µF bypass capacitors C_2 and C_3 in the collectors of output transistors Q_3 and Q_4. The voltage across these resistors reveals the collector currents, which are nearly equal in the two output transistors, and is close to the value that the values of R_1 and R_2 predicted. EDN

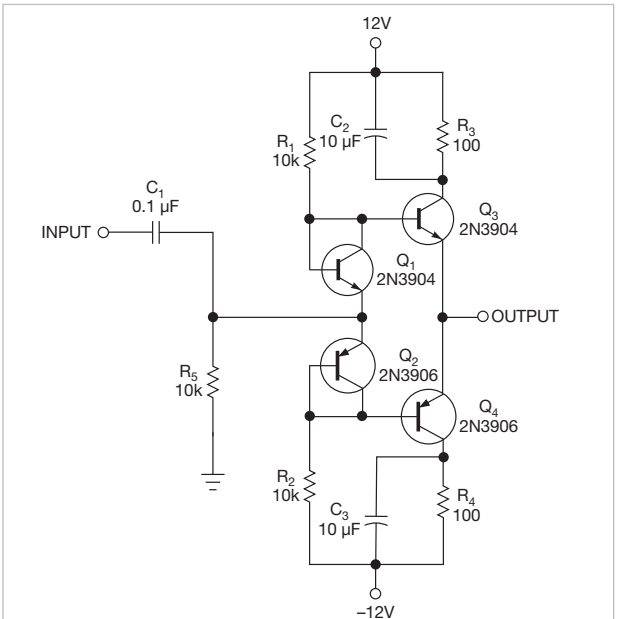

Figure 3 Resistors R_3 and R_4 limit the output current.

Limit inrush current in high-power applications

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C Castro-Miguens, University of Vigo, Vigo, Spain

A high-power offline supply is nothing more than a half- or full-bridge dc/dc converter. Rectifying the ac line yields a dc voltage that feeds the converter. At power-supply turn-on, the bulk capacitor of the uncontrolled rectifier is completely discharged. It results in a huge charging current for a high instantaneous line voltage because the discharged bulk capacitor temporarily short-circuits the diodes of the rectifier stage. The high inrush current can trigger a mains circuit breaker, burn a fuse,

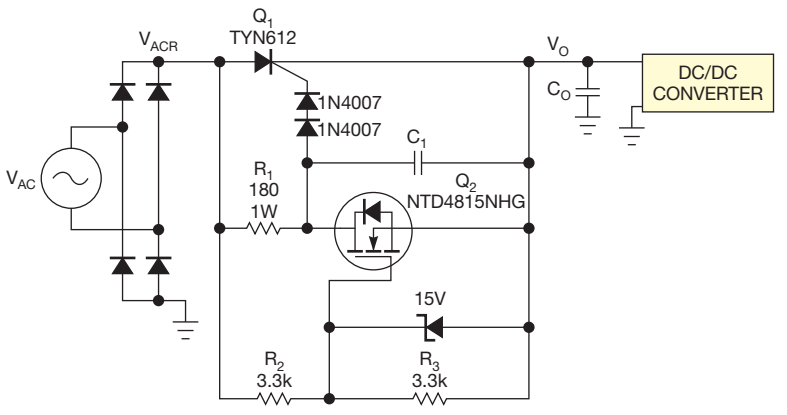
or even destroy a power supply's rectifier diodes unless you take precautions. The circuit in **Figure 1** limits the inrush current.

At turn-on, if the instantaneous rectified ac-line voltage, V_{ACR}, is greater than approximately 10V, Point A in **Figure 2**, MOSFET Q_2 turns on, forcing thyristor Q_1 off. In this situation, a little current flows through R_1 and Q_2, injecting a small charge into bulk capacitor C_O, Path A to B in **Figure 2**.

When $V_{ACR}-V_O \leq 8V$ or so, where V_O is the output voltage, Q_2 is off, letting Q_1 conduct. In this situation, the bulk capacitor receives the necessary charge through Q_1, Path B to C in **Figure 2**, to match V_O to V_{ACR}. After this point, V_{ACR} falls below V_O, and the bulk capacitor alone must support any power the dc/dc converter demands until $V_{ACR}-V_O \geq 5V$ or so, Path C to D in **Figure 2**. At Point D, $V_{ACR}-V_O \approx 5V$ and thyristor Q_1 triggers, which conducts the capacitor's charge current and the current the dc/dc converter demands until V_{ACR} matches the sinusoidal peak at Point E.

When V_{ACR} falls, thyristor Q_1 cuts off, and the bulk capacitor alone feeds the dc/dc converter. The thyristor conducts again when V_{ACR} matches V_O to the sinusoidal peak. This process then repeats. Use a nonsensitive gate thyristor with a breakdown voltage of at least 400V for an ac voltage of 220V rms (root mean square) and with twice the rms-current rating of the rectifier diodes.

This circuit uses a TYN610 thyristor. You can calculate the value of R_1 using $R_1=(6.8-V_{GT})/I_{GT-20°}$, where V_{GT} is the minimum gate-cathode voltage necessary to produce the gate-trigger current for Q_1 and I_{GT} is the minimum gate current to trigger Q_1 down to –20°C. The NTD4815NHG MOSFET is suitable for this circuit. A MOSFET with a different threshold voltage may require different values for R_2 and R_3. EDN



NOTE: 15 nF IS AN OPTIONAL VALUE FOR C_1.

Figure 1 A thyristor and a MOSFET control current to bulk capacitor C_O. This circuit limits the inrush current.

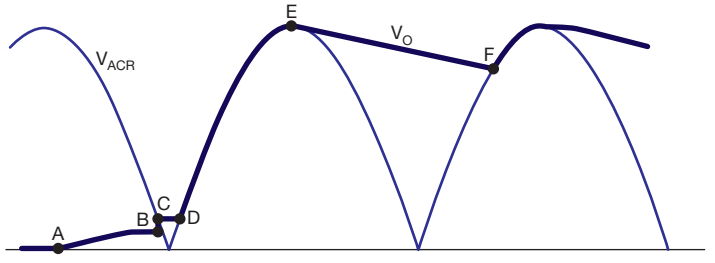


Figure 2 if V_{ACR} is greater than approximately 10V, MOSFET Q_2 turns on; current flows through R_1 and Q_2, injecting a small charge into bulk capacitor C_O.

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READERS SOLVE DESIGN PROBLEMS

Reduce acoustic noise from capacitors

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Some surface-mount capacitors exhibit acoustic noise when operated at frequencies in the audio range. A recent design uses 10-µF, 35V X5R 1206 ceramic capacitors that produce noticeable acoustic noise. To quiet such a board, you can use acoustically quiet capacitors from manufacturers such as Murata (www.murata.com) and Kemet (www.kemet.com). Unfortunately, they tend to cost more than standard parts. Another option is to use capacitors with a higher voltage rating, which could reduce the noise. Those parts may also be more expensive than standard capacitors. A third path is to make a physical change to the PCB (printed-circuit board).

A ceramic capacitor expands when you apply a voltage and contracts when you reduce the voltage. The PCB flexes as the capacitor changes size because the ends of the capacitor mechanically couple to the PCB through solder (**Reference 1**).

Figure 1a shows a capacitor with no applied voltage, and **Figure 1b** shows an exaggerated condition of PCB flexing when you apply voltage to a capacitor. Applying the voltage makes the PCB operate as a speaker. Keeping that fact in mind, consider two methods for improving the situation. The first technique is relatively simple: If your circuit uses one capacitor, replace it with two in parallel, each with half the capacitance of the noisy capacitor. This approach lets you place a capacitor on top of the board and the other on the bottom of the board; the capacitors lie directly above each other, and their orientations are the same. As the upper capacitor tries to flex the board down, the lower capacitor tries to flex the board up. These two stresses tend to cancel each other, and the PCB generates little sound.

Adding a second capacitor increases cost but not as much as replacing the noisy capacitor with one that might not create noise. A ceramic capacitor from Digi-Key (www.digikey.com) sells for approximately 27 cents (1000). A quieter KPS-series part from Kemet costs approximately $1.50. The second method involves making a slot in the PCB near each end of the capacitor (**Figure 2**). When the capacitor expands and contracts, it flexes only a small portion of the PCB, which should reduce the noise.

A test with five 10-µF, 25V ceramic capacitors connected in parallel showed that putting three capacitors on top of the PCB and two on the bottom reduces the noise by 14 dBA (acoustic decibels). Routing a slot on both sides of the five capacitors reduces the noise by 15 dBA. Both are substantial noise reductions. A Murata JG8-series capacitor reduces the noise by 9.5 dBA. Combining these techniques should further reduce the noise. EDN

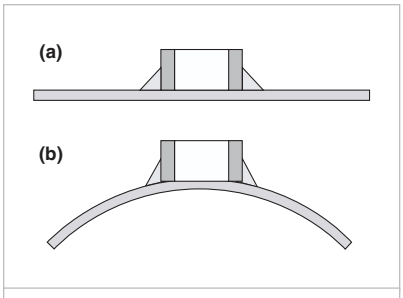

Figure 1 A ceramic capacitor expands when you apply a voltage (a) and contracts when you reduce the voltage (b).

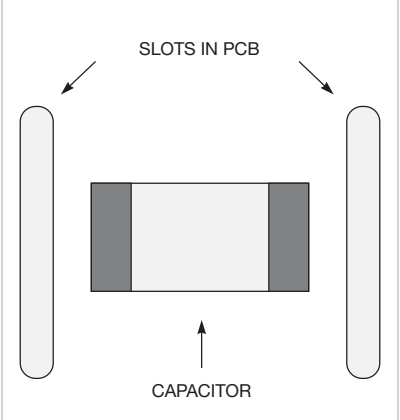

Figure 2 Adding a second capacitor increases cost but not as much as replacing the noisy capacitor with one that might not create noise.

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Function generator has variable frequency

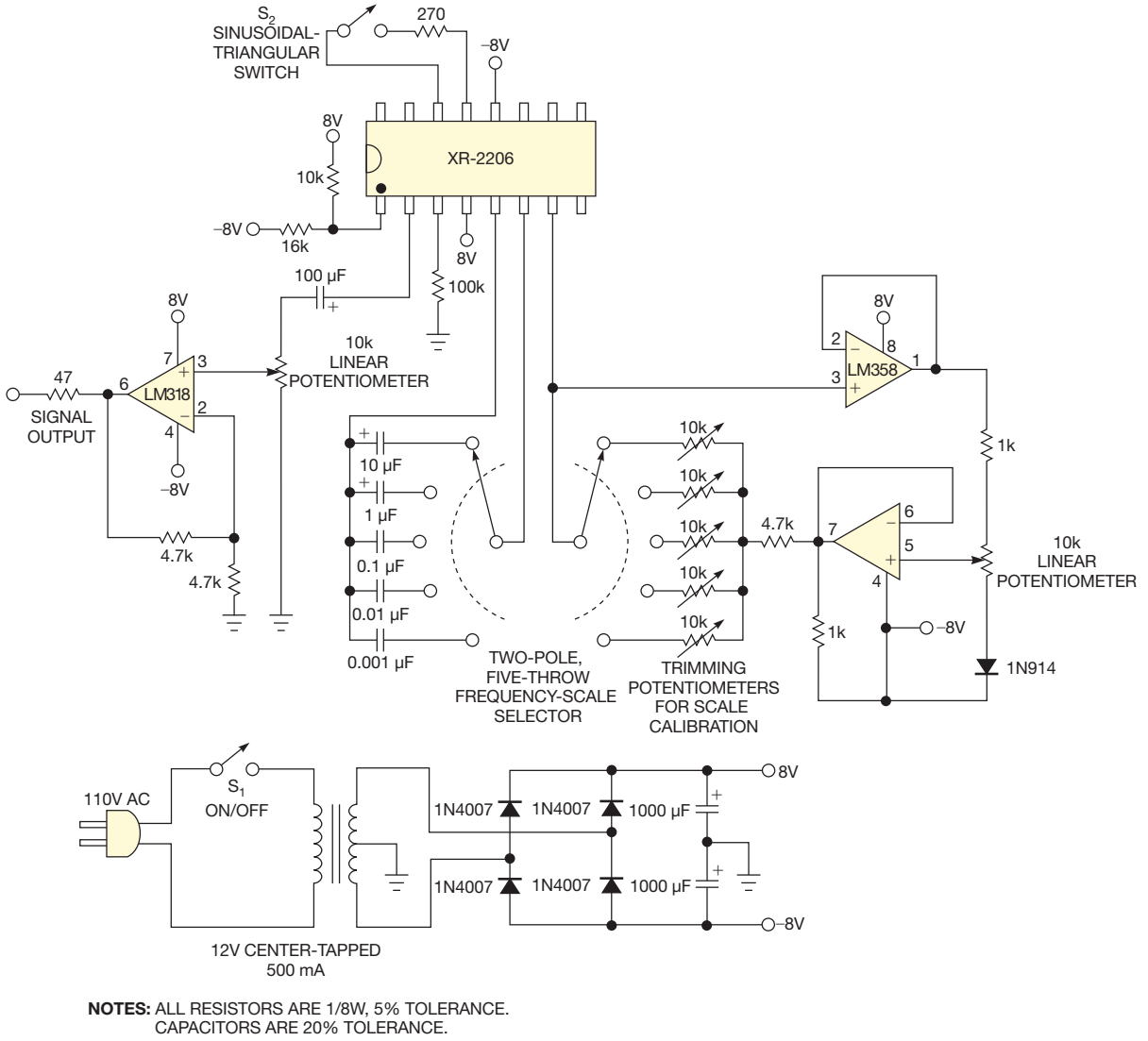
Adolfo Mondragon, Electrolux Products, Juarez, Mexico

The Exar (www.exar.com) XR-2206 function-generator IC can generate square, triangular, and sinusoidal signals with low distortion. Its output frequency is inversely proportional to the components in an RC network, according to the formula F=1/RC.

Use a potentiometer as the resistor component to provide a frequency variation similar to a logarithmic scale. To change this behavior, the manufacturer's data sheet recommends connecting a resistor network to a variable external voltage source. The voltage should be stable and vary from 0 to almost 3V.

Instead of using an external voltage, the circuit described here uses an internal reference voltage of approximately 3V at Pin 7 of the XR-2206. With this internal reference, the circuit requires no voltage regulators—not even in the power supply. The circuit requires a power supply with only a 12V, 500-mA center-tapped transformer, a bridge rectifier, and two filter capacitors (**Figure 1**). You can define the frequency **equations** using **Figure 2** as a reference.

When V_X is 0V, you determine the frequency using F=1/RC. The current trough, I_R, equals 3/R, where 3 is the voltage reference in Pin 7. From this **equation** and resolving the recipro-



NOTES: ALL RESISTORS ARE 1/8W, 5% TOLERANCE.
CAPACITORS ARE 20% TOLERANCE.

Figure 1 The waveform-generation circuit has a frequency of 1 Hz to 100 kHz in five scales.

cal of R, you define the frequency as $I_R/3R=1/R$, as a function of the current, $F=I_R/3C$.

When $V_X>0V$, you define the current as $I_R=(3-V_X)/R$. Replacing I_R from the previous **equation**, you can define the frequency as a direct function of the voltage: $F=(1/3RC)(3-V_X)$.

Figure 1 shows the final circuit to generate the waveforms. The circuit's frequency ranges from 1 Hz to 100 kHz in five scales. The rotary switch lets you select the scale by switching in a set of capacitors. EDN

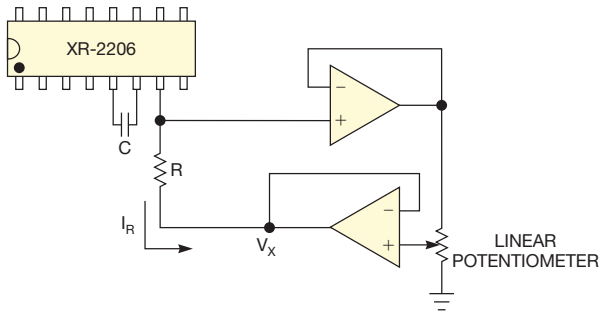


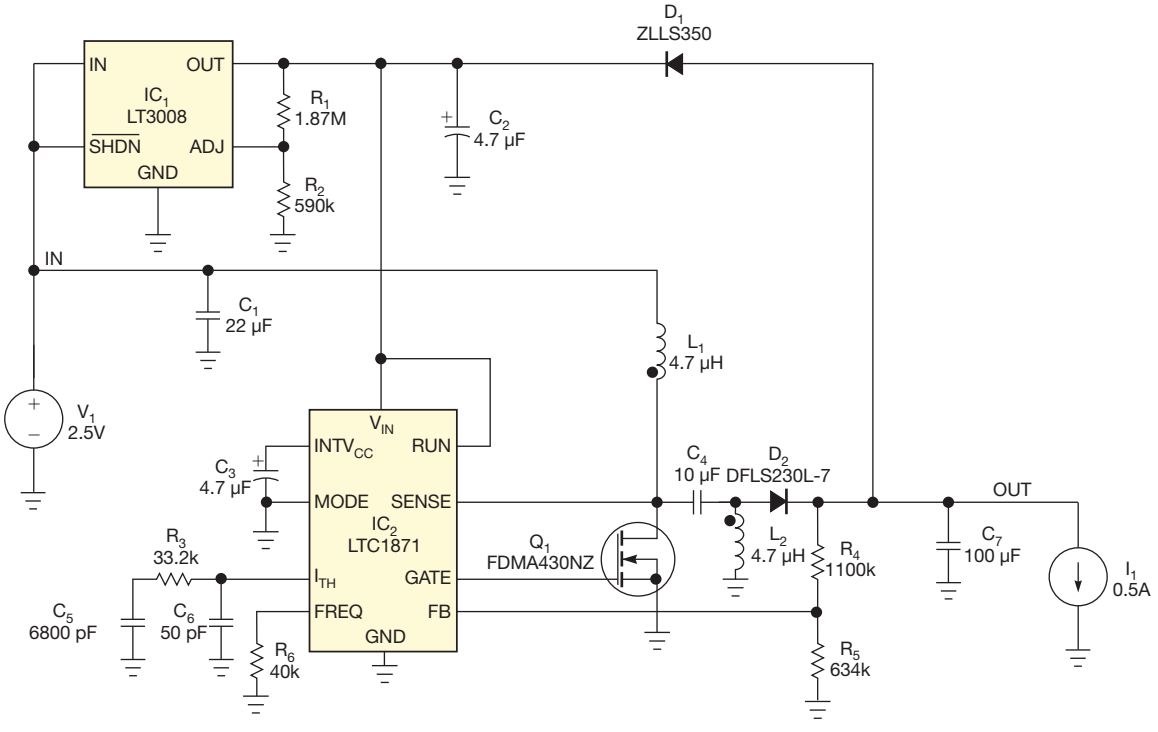
Figure 2 With an internal reference, this circuit requires no voltage regulators—not even in the power supply.

Power supply accepts wide input-voltage range

Jim Windgassen, Northrop Grumman Undersea Systems, Annapolis, MD

The switching power supply in **Figure 1** produces 3.3V dc from an input voltage of 2.5 to 20V dc with high efficiency. The circuit operates at an input voltage as low as 1.5V once it starts from a minimum of 2.5V dc, allowing the switcher to fully discharge a pair of alkaline cell batteries nearing end of life. The power supply can also run efficiently off higher input voltages, such as 12V automotive power. The heart of the circuit is a SEPIC (single-ended-primary-inductance-converter)-based switching power supply, which provides an output voltage greater than or less than the input voltage (**Reference 1**).

This power supply includes bootstrap circuitry comprising IC_1, an LT3008



NOTES: INDUCTOR MODEL IS BASED ON 4.7-µH WÜRTH 744878004 DUAL INDUCTOR FOR 600 kHz.
L_1 AND L_2 ARE WOUND ON A COMMON CORE.

Figure 1 The power supply can provide a 3.3V output from 2.5 to 20V input voltages. It needs 2.5V to start.

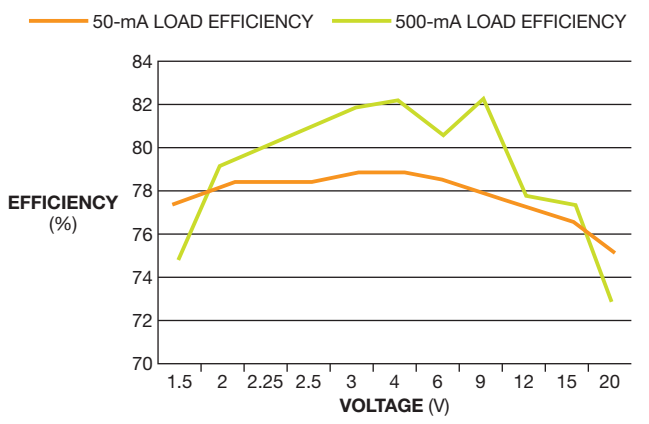


Figure 2 The power supply's efficiency is consistent over 50- and 500-mA loads.

voltage regulator; Schottky diode D_1; and capacitor C_2. It needs a minimum of 2.5V to start. Voltage regulator IC_1 provides 2.5V to start SEPIC controller IC_2. Once the output voltage of the SEPIC power supply reaches its normal output voltage of 3.3V, D_1 lets the output power of the switcher flow back to power IC_2. Once this action occurs, IC_1 drops out of the circuit because the voltage at its output is above its setpoint voltage. The converter's own output now powers IC_2, and the regulator's internal circuitry prevents backflow of power through IC_1. MOSFET Q_1 has low threshold voltage, appropriate on-resistance to provide current feedback to IC_2, and a maximum drain-to-source voltage of 30V to allow for operation up to a 20V input.

The bootstrap circuit allows the converter to run from very low input voltages by maintaining the input voltage to IC_2, and it increases efficiency at high input voltages by eliminating the use of IC_2's internal linear voltage regulator. **Figure 2** shows the efficiency of the prototype power supply at both 50- and 500-mA loads. The power supply's efficiency is consistent over a range of operating voltages because of the bootstrapping circuit.

Because the circuit uses a low-threshold-voltage MOSFET, the switch, keeping the gate drive voltage low, reduces the total charge that must go into and out of the MOSFET gate, further improving efficiency. SEPIC controller IC_2 normally uses its internal low-dropout capability to generate an operating voltage of 5V from the input. Running IC_2 from the bootstrapped output reduces IC_2's operating voltage to approximately 3V, which also limits the drive voltage to Q_1's gate.

Table 1 lists the key components for the power supply, including an appropriate commercially available coupled inductor. The PCB (printed-circuit-board) design and the choice of coupled inductors for this power supply are critical for good performance. For the power supply to achieve high efficiency at low input voltages and high output current, the coupled inductor must have low-resistance windings, and the high current tracks should use wide copper pours to minimize resistance

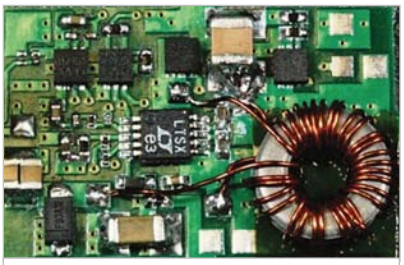


Figure 3 The complete power supply fits onto a 23×15×3.5-mm PCB.

TABLE 1 KEY PARTS FOR POWER SUPPLY

Component	Description	Manufacturer	Part
Input capacitor	22-µF, 25V, 10%-tolerance, 1210-size X5R ceramic capacitor	AVX	12063D106KAT2A
Output capacitor	100-µF, 6.3V, 1206-size X5R ceramic capacitor	Kemet	C1206C107M9PACTU
Coupled inductor	4.7-µH coupled-inductor Cuk SEPIC	Würth	744878004
Bootstrap low-dropout regulator	Regulated-low-dropout-adjustment, 20-mA, 6-DFN-packaged IC	Linear Technology	LT3008EDC#TRMPBF
SEPIC controller	10-MSOP-packaged current-mode-IC controller	Linear Technology	LTC1871EMS#PBF
MOSFET	30V, 5A, N-channel microMOSFET	Fairchild Semiconductor	FDMA430NZ
Bootstrap diode	SOD-523-packaged, 40V Schottky diode	Diodes Inc	ZLLS350TA
SEPIC diode	2A, 30V Schottky power diode	Diodes Inc	DFLS230L-7

losses and unwanted inductance.

A prototype of the power supply measures 23×15×3.5 mm (**Figure 3**). It uses a custom coupled inductor, but you can choose from many off-the-shelf coupled inductors available from BH Electronics (www.bhelectronics.com), Coilcraft (www.coilcraft.com), and Würth Elektronik (www.we-online.com). You can download the Linear Technology LTSpice code for this circuit from the online version of this Design Idea at www.edn.com/110217dia. EDN

REFERENCE

1 "Designing a SEPIC Converter," Application Note 1484, National Semiconductor, April 30, 2008, http://bit.ly/ich5pf.

Circuit lets you test capacitors

Raju R Baddi,
Tata Institute of Fundamental Research, Maharashtra, India

Electrolytic capacitors tend to leak with time. The circuit in **Figure 1** lets you test capacitors and decide whether they're worth using. You can set the constraint on the leakiness through the values of C_{REF}/R_{REF}. The values in the **figure** are typical for general testing of all capacitors, from 1-nF ceramic versions to 1000-µF electrolytic types. The value of C_{REF} in the circuit is near the value of the test capacitor, C_X. You can also choose R_{REF}, by a rotary-switching arrangement, to be greater than or less than 22 MΩ.

When the pushbutton switch closes, capacitors C_{REF} and C_X charge through their respective PNP transistors. When the switch opens, the capacitors begin to discharge. C_{REF}, assuming that it is in good condition, has an additional discharge external resistance, R_{REF}. The capacitor under test, C_X, discharges through its internal resistance. If the leakage in C_X is greater than that of C_{REF} through R_{REF}, then its voltage will fall faster. Thus, the voltage at the op amp's noninverting input will be lower than at its inverting input, forcing the op amp's output low and lighting the red LED. This LED indicates that the test capacitor leaks. Testing of the circuit reveals that even a 1-nF ceramic capacitor holds against the reference. Check the voltage rating on the test capacitor to make sure that it is higher than the voltage to which it will be charged—in this case, V_{SUPPLY} is –1.8V.

The LF357 has a minimum supply voltage of 10V, but the testing took place at only 6V to allow a low upper-limit voltage for the test capacitor. Make sure the capacitor has a FET or a MOSFET input stage. EDN

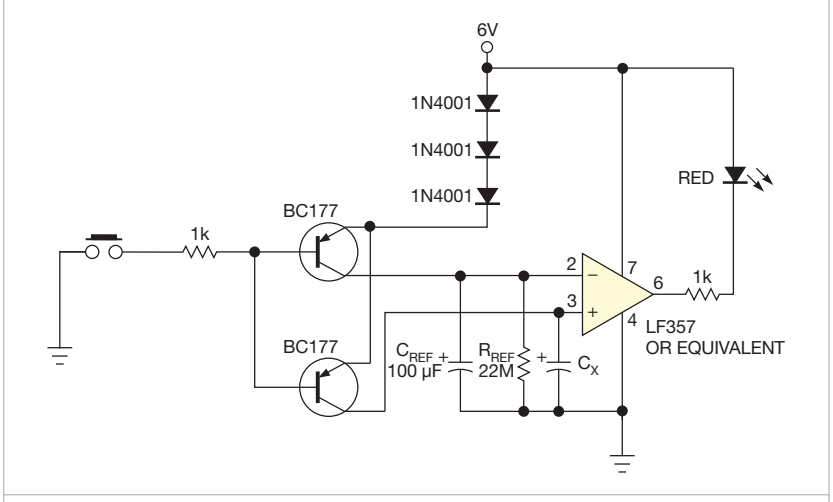


Figure 1 Electrolytic capacitors tend to leak over time, but this circuit lets you test them and decide whether they're worth using.

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designideas

READERS SOLVE DESIGN PROBLEMS

Design provides single-port-to-dual-port SDRAM converter

Yu-Chieh Chen, Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan

In multimedia and video applications, DRAM buffers large frames in the image coding and decoding between an image-sensing device and an image-display device (**references 1** and **2**). It also plays a key role in image-frame-rate converters by matching the displaying format of the monitor (**Reference 3**). Accessing dual-port SDRAM is a complex task, especially when two data read or write operations are occurring simultaneously into a single-port SDRAM during high-speed operation.

SDRAM supports asynchronous control, performs reading and writing operations, and allows multiple CPUs to read or write in parallel. To reduce production costs and avoid complexity, engineers typically prefer conventional one-port SDRAM. You can, however, use an FPGA to convert a single-port SDRAM to function as a dual-port SDRAM.

The single-port-to-dual-port SDRAM converter comprises two read-FIFO (first-in/first-out) and write-FIFO memory blocks. A pair of read and write controllers each control a read-and-write data bus. **Figure 1** shows the architecture of the proposed converter, and **Figure 2** shows the operating flow of the read-and-write controller. The write controller first stores the writing data in write-FIFO and executes the SDRAM write command when the WKO (write-keep-out) signal falls to a low level, which means that the read operation is complete. Meanwhile, the RKO (read-keep-out) signal goes high until the write operation is complete. The procedure prevents the read signal from occurring during the writing operation.

The read-data operation is similar to the write-data operation. The read controller first waits for the RKO signal to fall low if it is high when the read operation starts. The read controller then executes the read command and stores the data from SDRAM to read-FIFO memory. The read controller simultaneously pulls the WKO signal high until the read operation is complete. **Figure 3** shows the hardware logic of the smart controlling strategy, which the following **equation** also describes:

$$F_{COM} = [MUX_{READCOM,WRITECOM} \times \overline{RKO} \times \overline{WKO}],$$

where MUX is the multiplexer. For the read example, the SEL (select) signal switches to the read mode and then waits for the RKO signal to fall low if the RKO signal is at a high level when the read command executes (**Reference 1**).

This strategy doubles the high-level period of both the read operation, or RKO signal, and write operation, or WKO signal. These signals rise to logic high before executing each read or write operation. This step ensures that the read operation does not interrupt the write operation and that the write operation does not interrupt the read operation.

Figure 4, available with the Web version of this Design Idea at www.edn.com/110303dia, shows the simulation waveform of the converter, which is a part of the image-sensing and -displaying sequence. The iSDRAM_Read signal is high, indicating that the SDRAM is performing a read operation. At the same time, the iSDRAM_Write signal is high during the SDRAM-writing op-

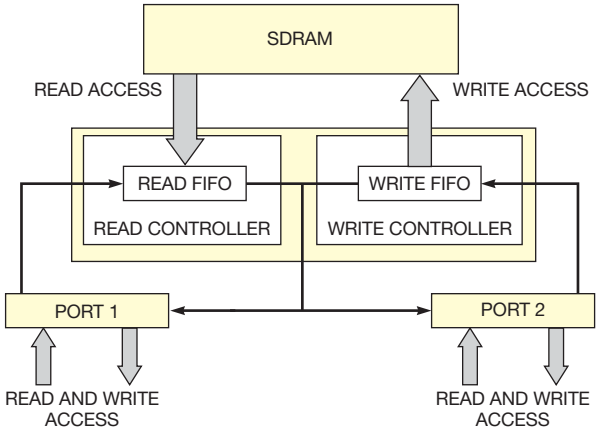

Figure 1 The converter architecture uses two ports for separate read and write operations.

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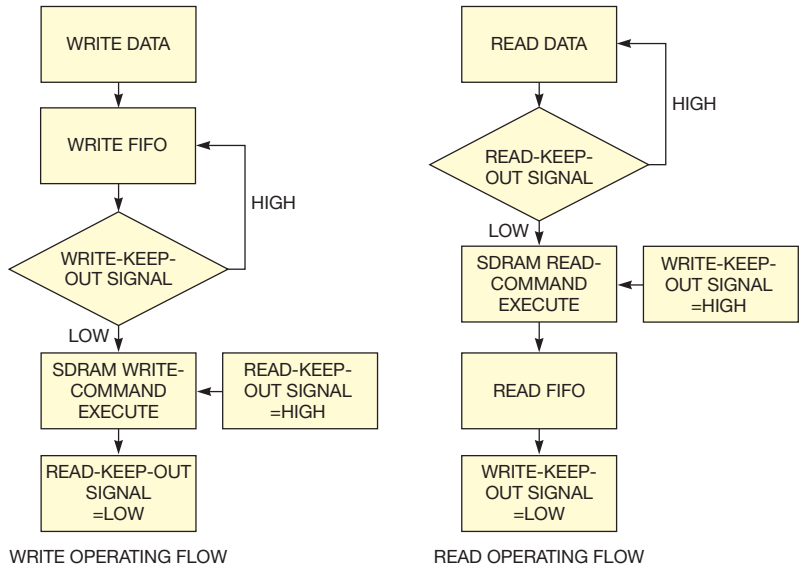

Figure 2 Read and write operations occur when the RKO and WKO signals are at logic-low states.

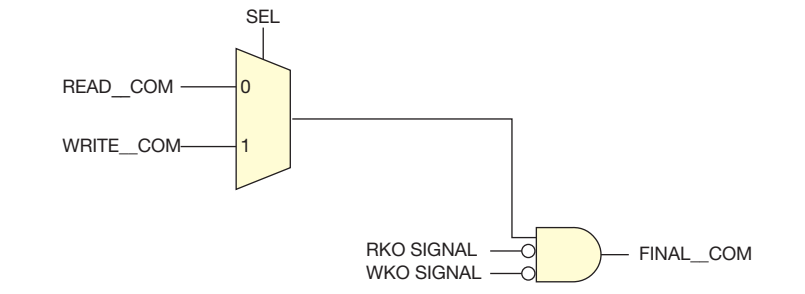

Figure 3 The hardware logic uses a multiplexer to select write or read signals.

eration. The iSDRAM_ReadKeepOut signal goes high before each iSDRAM_Write signal and lasts two times longer than each iSDRAM_Write signal. This setup ensures that the writing command does not execute during the read operation. For the same reason, the read command doesn't execute during the writing operation.

The write-clock operation is initially ahead of the read-clock operation. After several time delays, however, the write-clock operation catches up with the read-clock operation. At this point, the controller holds the data and waits until the iSDRAM_ReadKeepOut command falls to a low level before executing the read command. Using this read-and-write strategy, the controller resolves the conflict of executing read and write commands during write or read operations. EDN

REFERENCES

1 Zhu, Jiayi; Peilin Liu; and Dajiang Zhou, "An SDRAM controller optimized for high definition video coding application," *Proceedings of the IEEE 2008 International Symposium on Circuits and Systems*, May 2008, pg 3518, http://bit.ly/h6xaz0.
2 Jack, Keith, *Video Demystified*, Fifth Edition, Newnes Publishers, 2007, ISBN: 0750683953.
3 Yim, Myung-Sik, "Image decoding apparatus having frame rate transformation function," US Patent No. 5917950, June 29, 1999, http://bit.ly/i4GR98.

Zener diode protects FPGA inputs

Rick Collins, Arius, Frederick, MD

Although 5V-powered logic is still common in many applications, most FPGAs support interface levels of 3.3V and lower. When you connect an FPGA to higher voltage levels, the FPGA's application notes commonly suggest that you use the PCI (Peripheral Component Interconnect)-bus clamp diodes in the FPGA's I/O blocks with an external series-limiting resistor to prevent damage to the FPGA (**Figure 1**). The PCI clamp diode limits the voltage to a level that doesn't harm the input, and the resistance value limits the current to a safe level that doesn't harm the PCI clamp diode. This approach works well in designs with low-speed signals.

However, when you use this approach with a higher-rate signal, the effects of the parasitic RC filter distort the signal

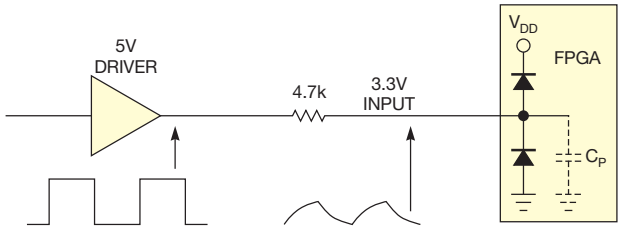

Figure 1 Engineers often use a series resistor to interface 5V logic levels to FPGAs.

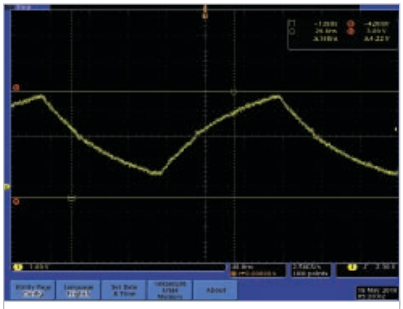

Figure 2 A parasitic RC filter slows the signal's edges.

(**Figure 2**). The circuit from the FPGA's application notes requires a change, which you can accomplish without redesigning the PCB (printed-circuit board). In this case, substituting a zener diode for the resistor shifts the signal level without causing excessive distortion (**Figure 3**). The zener diode works with the PCI clamp diode and the internal pulldown resistor to set the voltage level at the input pin.

To set the static level at the input pin, you must enable the FPGA's internal pulldown resistor to prevent the PCI clamp diodes from being driven too hard when the input is continuously high. The current from the pulldown resistor is smaller than the rating current of the zener diode. Low-voltage zener diodes also have round "knees" in the avalanche IV (current-to-voltage) curve. This curve results in a zener voltage that's lower than the rated value, so you need to use a higher-voltage zener diode. The diode should also have a low capacitance. The CZRU52C3, a 3V zener diode from Comchip (www.comchip.tw.com), works well, reducing the circuit's voltage by 2V (**Figure 4**).

Some parasitic effects in the zener diode will create other distortion to the waveform. The parasitic capacitance of the diode causes the diode to initially look like a short to the signal edges from the 5V driver. The FPGA pin will see a high-voltage overshoot for approximately 10 nsec, quickly decaying to the rated level of the input pin. The RC time constant of the pin capacitance and the pulldown resistance result in a slower drop to the final value, which the zener diode and the pulldown resistance determine. **Figure 5** shows a detailed view of the leading edge. EDN

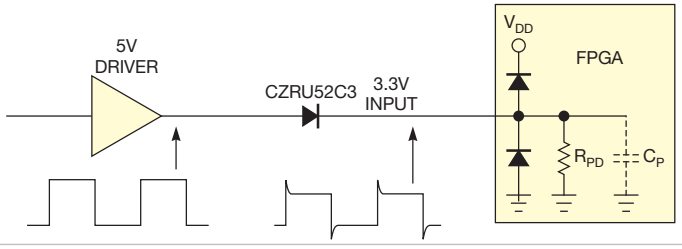

Figure 3 Replacing the resistor with a zener diode shifts the voltage level with little distortion.

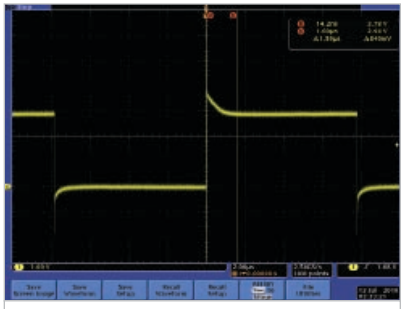

Figure 4 An oscilloscope trace shows the signal with overshoot.

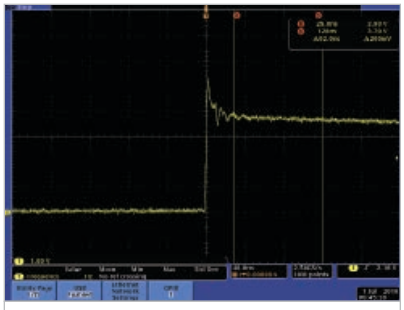

Figure 5 The brief overshoot of the leading edge of the pulse does not damage the FPGA inputs.

Bicolor LED indicates 10 states

Abel Raynus, Armatron International, Malden, MA

Most microcontroller-based devices have several states of operation. Pushbutton switches often control these states. To minimize costs, many designs use only one switch; the number of presses sets the microcontroller's state. In the circuit in this Design Idea, lighting an LED indicates the chosen state.

A large selection of bicolor LEDs is on the market in various shapes and colors from Kingbright (www.kingbrightusa.com), Optosupply (www.optosupply.com), and other suppliers. These LEDs provide new opportunities to use just one LED to indicate 10 states. You set the states by pressing a pushbutton switch that connects to a microcontroller's external interrupt pin (**Figure 1**). After each push, the interrupt subroutine sets the device to the next state (**Figure 2**).

State 0 is standby mode with the LED off. The device waits for you to press a switch. The LED's color indicates the next three states. For example, a Kingbright WP5A9EGW12.3SF LED yields red, green, and orange. Add

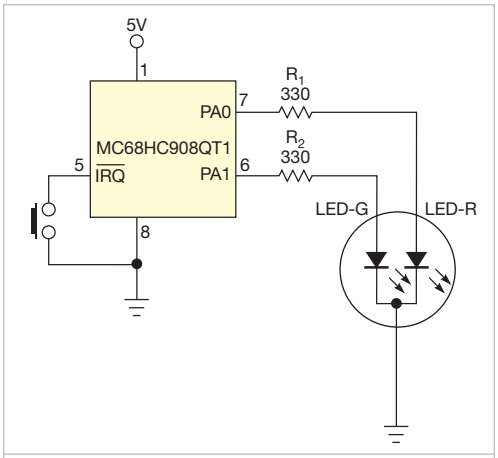

Figure 1 A bicolor LED and a pushbutton switch are all you need to set and indicate a microcontroller's state.

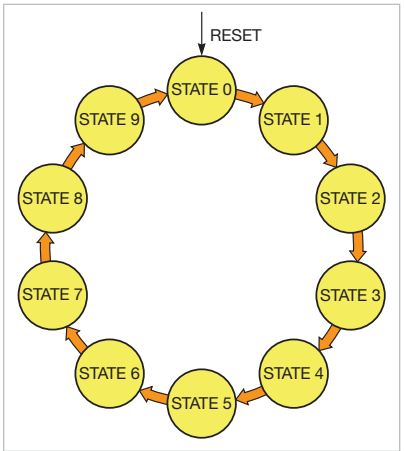

Figure 2 Pressing the switch advances the microcontroller's state.

TABLE 1 COLOR AND BLINKING PATTERNS FOR 10 STATES

State	Red LED	Green LED	Indication
0	Off	Off	No light (standby)
1	On	Off	Red
2	Off	On	Green
3	On	On	Orange
4	Blinks	Off	Red blinks
5	Off	Blinks	Green blinks
6	Blinks	Blinks	Orange blinks
7	On	Blinks	Red and orange blink
8	Blinks	On	Green and orange blink
9	Blinks	Blinks	Red and green blink

blinking to indicate the remaining states. You can independently control the red and the green LEDs, yielding six more combinations of indication (**Table 1**).

Using the microcontroller's internal oscillator as a clock source simplifies the circuit because the oscillator needs no external components and its 5% tolerance is sufficient for this application. Firmware sets the built-in pullup resistor for external interrupt input.

The clock speed and the values of the prescaler and time-counter-modulo registers determine the rate of LED blinking. The internal oscillator generates a 12.8-MHz clock, resulting in a 3.2-MHz bus frequency, with one cycle equal to 0.3125 μsec. By choosing a prescaler value of 64, a time-counter-modulo register can calculate a cycle of 50 times the timer period in milliseconds. For example, for 1 second of blinking, you should set the time-counter modulo to 50,000, or $C350 in hexadecimal.

Using tables rather than polling in programming allows you to significantly reduce the size of firmware (**Reference 1**).You can download firmware assembly code from the online version of this Design Idea at www.edn.com/110303dib. This method is applicable to any microcontroller. You can even increase the number of indicated states by using different blinking rates. EDN

REFERENCE

1 Raynus, Abel, "Tables ease microcontroller programming," *EDN*, April 22, 2010, pg 76, http://bit.ly/brXaq7.

Relay driver switches two relays with one pin

Gunther Kraut, PhD, Egmating, Germany

Independently switching two loads, such as relays, usually requires two microcontroller-I/O ports. Two ports let you control the loads so that you can switch them both off, switch them both on, or switch one on and the other off. If you don't need both relays on at once, you can control the remaining three states using only one port. You can also use a port's high-impedance state to control the relays.

You can, for example, use this application to control a motor. The motor's rotational direction depends on which of its two phase lines you select. This approach works with either classic electromechanical relays or SSRs (solid-state relays). If both relays are open, the motor is off. For electromechanical relays, you can use the driver circuit in **Figure 1**. Setting the microcontroller pin to logic one causes Q_1 to turn on relay REL_1, and the motor runs forward. Setting the pin to a logic zero turns on Q_2, which turns on Q_3. This action closes the switch of REL_2 and causes the motor to run in the opposite direction. If the microcontroller port is in a high-impedance state, Q_1, Q_2, and Q_3 cannot deliver current because the constant voltage of 1V at the base of Q_2 is too low to reach the threshold of the base-emitter junctions of Q_1 and Q_2 plus the diode drop of D_1. Both relays are off, and the motor is off. The supply voltage through a voltage divider or an emitter-follower circuit can provide the constant voltage of 1V. Free-wheeling diodes D_2 and D_3 prevent the collectors of Q_1 and Q_2 from overvoltage when the relay's coils are off. You can use almost any small-signal NPN and PNP transistors in this circuit. The selection of diode D_1 is also not critical.

The circuit is simpler for SSRs because virtually all microcontroller ports directly drive the LEDs (**Figure 2**). A logic one supplies the LED in S_1, whereas a logic zero supplies the LED in S_2, making the corresponding TRIAC (triode-alternating-current) switches conductive. If the port is in the high-impedance state, no current can flow through the LEDs because the constant dc voltage of 1.2V is below the sum of the threshold voltages of the LEDs. Voltage-dependent resistors R_3 and R_5 and snubber circuits C_1, R_4, C_2, and R_6 protect the SSRs. These protection circuits' values depend on the respective load. EDN

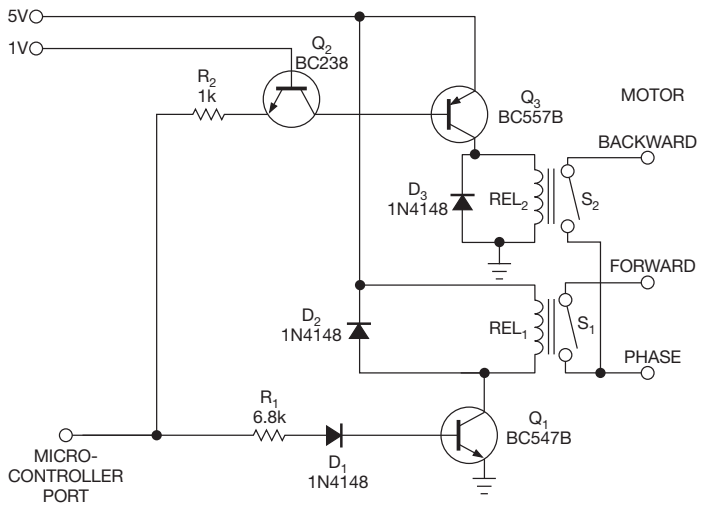

Figure 1 Relays respond to logic one, logic zero, and the high-impedance states of the microcontroller port.

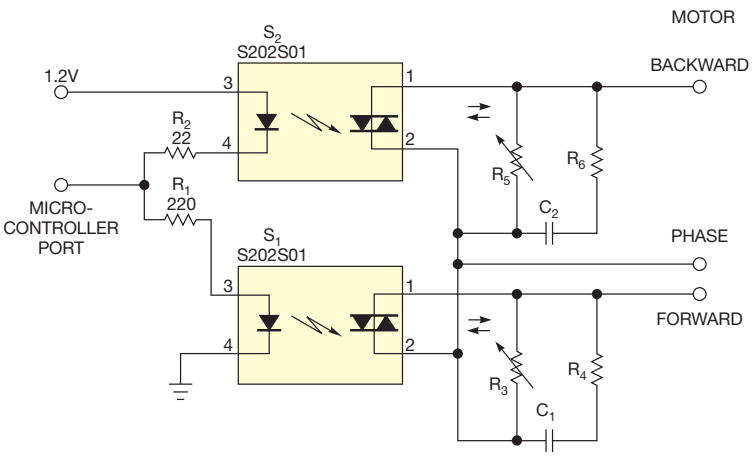

Figure 2 The circuit is simpler for SSRs because virtually all microcontroller ports directly drive the LEDs.

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READERS SOLVE DESIGN PROBLEMS

Anticipator circuit speeds signal settling to a final value

Tim Regan, Linear Technology, San Jose, CA

The circuit in this Design Idea anticipates, or jumps instantly to, the final voltage of an input-signal change. It relies on the fact that the intended input signal changes exponentially with a known time constant. This circuit was adapted from a 1970s-era instant-reading electronic thermometer, which displayed a patient's body temperature within seconds after a thermometer probe was placed under the patient's tongue. It exploits the fact that the temperature probe's exponential thermal response-time characteristic is known.

The circuit uses a quad rail-to-rail amplifier to perform a mathematical operation (**Figure 1**). The input to the circuit is at Node X. At that node, a filter with a 500-msec RC time constant averages a 1-kHz PWM (pulse-width-modulated) signal. The desired output is a dc voltage proportional to the PWM duty cycle. A long time constant is required to reduce ripple. You obtain an instant output response by differentiating this input signal with the same time constant. The input signal is the voltage on capacitor C_1 as it moves from initial voltage V_I to final voltage V_F. R_1 and C_1 set the time constant, as the following **equation** shows:

$$V_{IN}=V_F-(V_F-V_I)\times e^{-\frac{t}{R_1 C_1}}=V_A,$$

where e is an irrational constant approximately equal to 2.718281828. You then buffer this signal with an inverting gain of one-half to prevent clipping. Ignoring dc biasing for clarity, the ac output at Node V_B is a function of the RC time constant, as the following **equation** shows:

$$V_B=-0.5V_F+0.5(V_F-V_I)\times e^{-\frac{t}{R_1 C_1}}.$$

You then differentiate the inverted signal with amplifier IC_1. You set the differentiator time constant with R_2 and C_2. The gain of a differentiator circuit increases with frequency, making these circuits prone to instability. You use R_5 and C_8 to keep the circuit stable. At the low frequencies of interest, R_2 and C_2 dictate the function of the circuit, as the following **equation** shows:

$$V_C=-\tau\times\frac{dV_B}{dt}=$$

$$-R_2C_2\times0.5(V_F-V_I)\times e^{-\frac{t}{R_1 C_1}}\times\left(\frac{-1}{R_1C_1}\right).$$

R_1 and C_1 set the time constant of the input, so you can match it by making the differentiator time constant, $R_2\times C_2$, the same. This step cancels terms in the **equation** and simplifies the expression for output voltage, as the following **equation** shows:

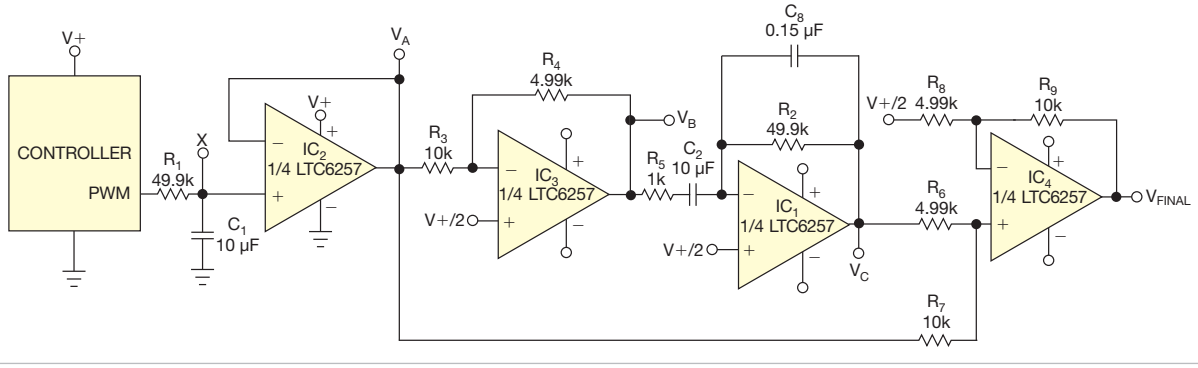

Figure 1 The output of this anticipator circuit instantly jumps to the final voltage of an exponential input signal.

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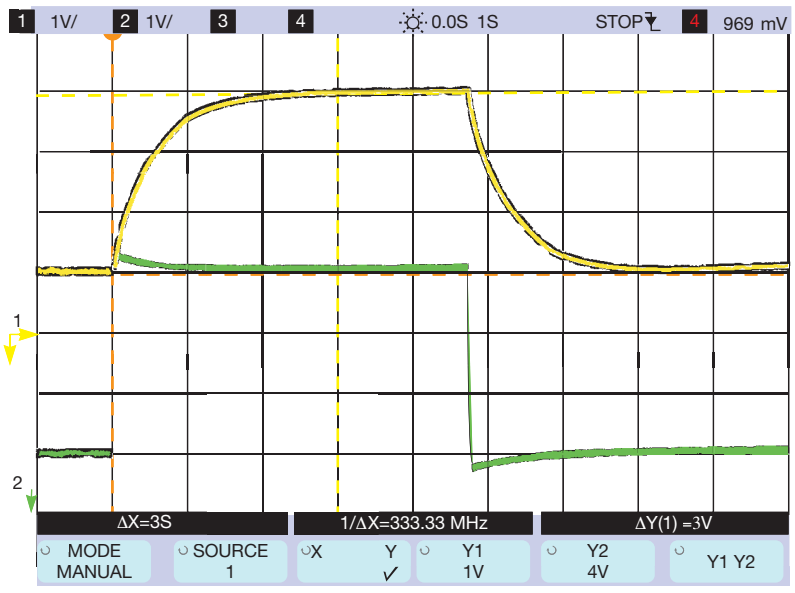


Figure 2 The anticipator circuit speeds the response of a slow exponential waveform (yellow) and results in nearly instant response to the final value, with only a small amount of overshoot (green).

$$V_C = 0.5(V_F - V_I) \times e^{-\frac{t}{R_1 C_1}}.$$

Due to scaling to prevent clipping, you sum this signal with the input signal in a weighted manner and present this voltage at the positive input of IC_4, as the following **equation** shows.

$$V_{IC4+IN} = \frac{2}{3}V_C + \frac{1}{3}V_A = \frac{(V_F - V_I) \times e^{-\frac{t}{R_1 C_1}}}{3} + \frac{V_F}{3} - \frac{(V_F - V_I) \times e^{-\frac{t}{R_1 C_1}}}{3}.$$

Note that the first and last terms of the preceding **equation** cancel out. You then set a gain of three for amplifier IC_4, as the following **equation** shows:

$$V_{OUT} = 3 \times \frac{V_F}{3} = V_{FINAL}.$$

When the input starts to move with a known exponential rate, the output anticipates the result and jumps instantly to what will be the final voltage (**Figure 2**). You can use this circuit in many applications that have a fixed input time constant. EDN

Schmitt trigger provides toggle function

Vladimir Oleynik, Moscow, Russia

D-type flip-flops, with the inverted output connected to the D input, can toggle a clock signal. If your circuit has an extra Schmitt-trigger inverter gate, you can use it to accomplish the same thing. Every time you press and release the momentary pushbutton switch in **Figure 1**, the circuit reverses to the opposite of what it was before you pressed it.

You can use a Schmitt trigger because it has hysteresis that positions roughly symmetrically around half of the power-supply voltage, $V_{CC}/2$. If a signal rises from 0V to $V_{CC}/2$, the output will be logic zero, so the inverter output is at logic one. If the signal drops from V_{CC} to $V_{CC}/2$, it will be at logic one, so the inverter output is at logic zero. At power-up, voltage at Point A rises from 0V to $V_{CC}/2$ because R_1=R_2, and the inverter's output will be high as V_{CC}. Capacitor C charges to $V_{CC}/2$. The momentary pushbutton switch in the circuit has NO (normally open) and NC (normally closed) states.

When you first press the button, capacitor C quickly charges to V_{CC} because the inverter output is high. When you release the button, high logic voltage appears across the capacitor on the inverter input. Thus, its output goes low. The capacitor discharges through resistor R_2 down to $V_{CC}/2$. When you press the button for the second time, capacitor C quickly discharges from $V_{CC}/2$ to 0V because the inverter's output is low. When you release the button again, the discharged capacitor shunts the inverter input, thus forcing its output high. The capacitor charges up through resistor R_1 to $V_{CC}/2$. **Figure 2** shows the waveforms.

The circuit is insensitive to contact bounce. Because the 40106 contains six Schmitt-trigger inverters, one IC can support as many as six momentary switches. You can substitute a two-input NAND Schmitt trigger CD4093 for the 40106. If you need to change the output when you press the button, reverse the connection of the NO and the NC contacts of the switch. EDN

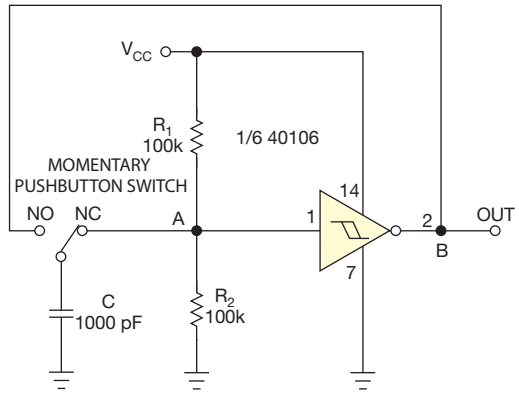


Figure 1 A single Schmitt trigger provides a toggle function.

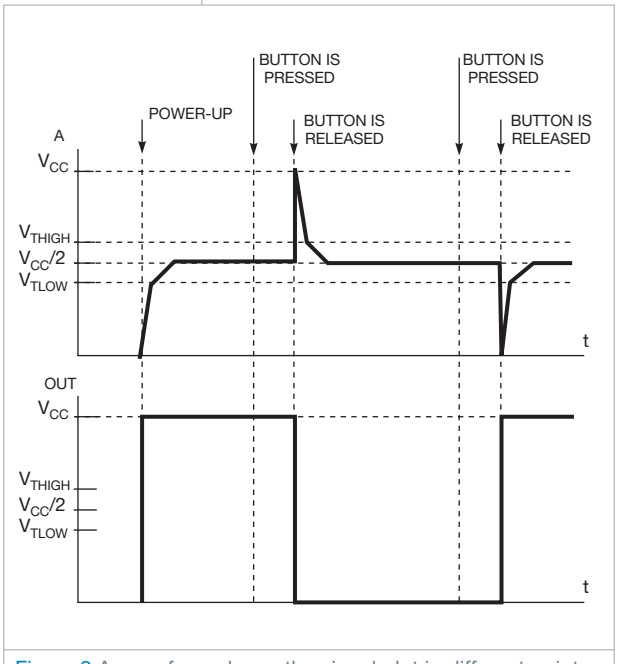


Figure 2 A waveform shows the signal plot in different points of the circuit.

Active multiplexing saves inputs

JB Guiot, Mulhouse, France

Microcontrollers must often read the status of switches in control applications. A typical switch configuration uses pullup resistors on both of the switches to pull the signals high or low for the microcontroller to read. The controlling output in the circuit in **Figure 1** uses two switches. When both switches are open, resistors R_1 and R_2 keep the input at an undetermined value between low and high, which is 1.5V if the supply voltage is 5V. Thus, an analog input would be preferable to a digital input. With the values in the figure, 0.5 mA of current flows through the resistors, even when both switches

AN INVERTER GATE HAS CLEARLY DEFINED LEVELS OF INPUTS. THUS, YOU CAN USE NORMAL LOGIC INPUTS RATHER THAN ANALOG INPUTS.

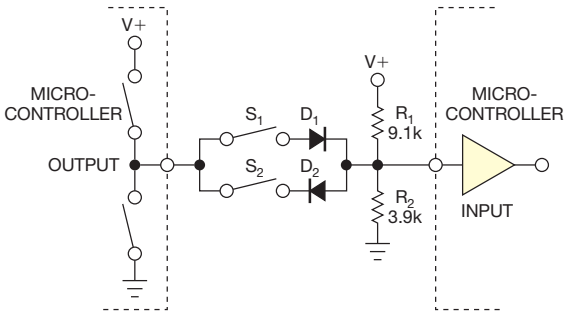


Figure 1 The controlling output in this circuit uses two switches.

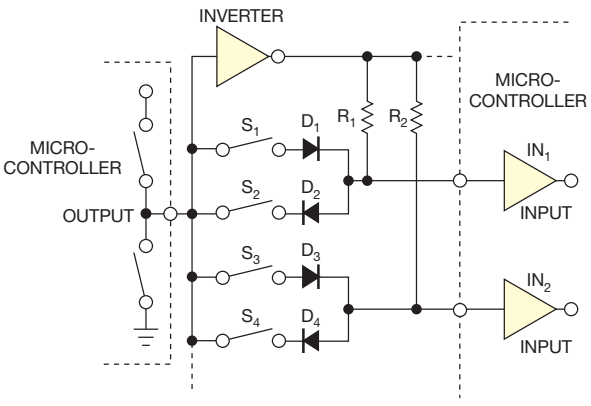


Figure 2 An inverter gate pulls the microcontroller's inputs to the opposite state of the driving output.

are open. You must multiply that value by the number of inputs used to get the total current.

Figure 2 shows an alternative circuit. It adds an inverter gate that pulls the microcontroller inputs to the opposite state of the driving output. An inverter gate has clearly defined levels of inputs. Thus, you can use normal logic inputs rather than analog inputs. You can choose a resistor value as high as the input characteristics allow yet low enough to minimize noise immunity. When both switches are open or the controlling output is in a high-impedance state, the current flowing through the resistor is only the current that flows into the microcontroller's input.

Switching a signal's state uses energy, so change states only when reading the switches. Otherwise, leave the input and output pins in a high-impedance state. If your design has position-cam switches that never close

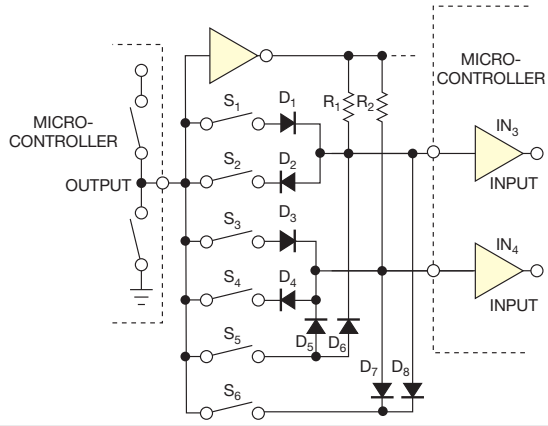


Figure 3 You can use this circuit to reduce the number of inputs coding the switches.

simultaneously, you can refer to the circuit in **Figure 3** to reduce the number of inputs coding the switches. **Table 1**, a truth table, provides the possible states.

You can expand this scheme to any number of switches and inputs. You can read 12 inputs with three switches. You can also mix the circuits in **figures 2** and **3** on the same microcontroller, separating independent switches (**Figure 2**) and "interlocked" switches (**Figure 3**) on different inputs. EDN

TABLE 1 TRUTH TABLE OF POSSIBLE STATES

Out	In_3	In_4	Switch
1	1	0	1
0	0	1	2
1	0	1	3
0	1	0	4
1	1	1	5
0	0	0	6

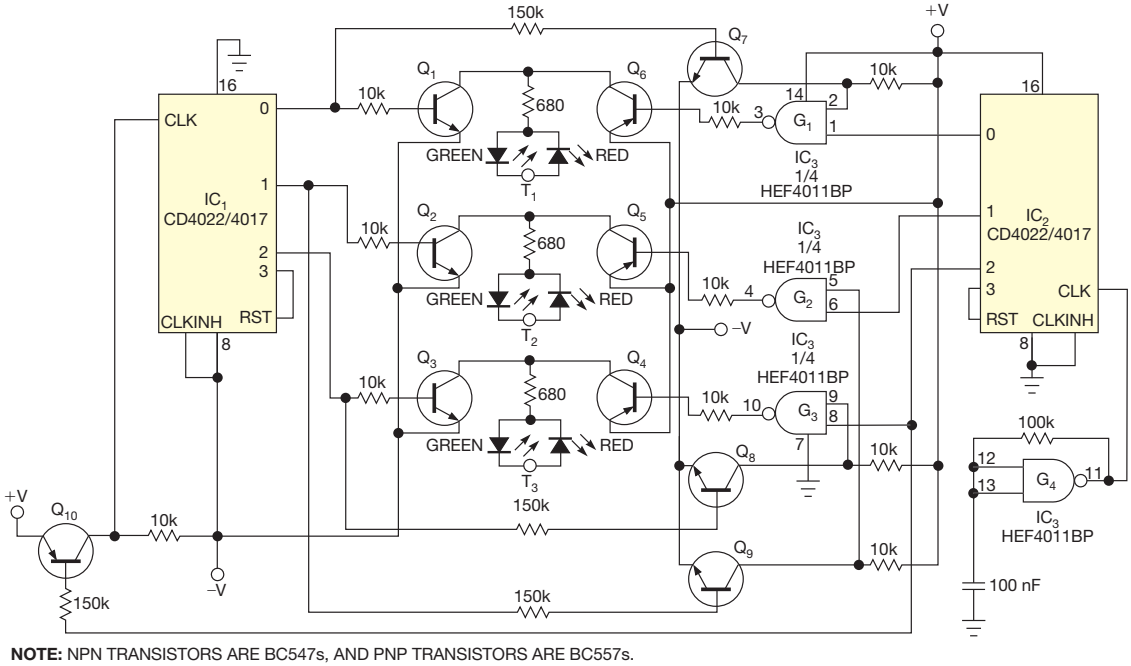
Transistor tester identifies terminals

Raju R Baddi, Tata Institute of Fundamental Research, Maharashtra, India

The simple transistor tester in **Figure 1** lets you identify the type of transistor, and it helps in detecting a transistor's emitter, collector, and base. It checks all possible combinations of directions of current flow between the test transistor's three terminals, T_1, T_2, and T_3.

The circuit uses two CD4022 or CD4017 counters, IC_1 and IC_2; a single-gate square-wave oscillator, G_4; and a CD4011 quad NAND gate, G_1 through G_3. A pair of LEDs connects in series to each test terminal to indicate the direction of current flow. The color of the LEDs directly reveals the junction side of the transistor.

Figure 2 provides an easy reference for understanding the test procedure. A pair of NPN transistors, Q_1 and Q_3, and PNP transistors, Q_4 and Q_6, for each terminal connects the terminals to either –V or +V, which sets up the required potential difference between the terminals. The circuit generates all of the possible or required combinations of +V and –V between the terminals to establish the junction relations. Q_7 and Q_8 act as voltage



NOTE: NPN TRANSISTORS ARE BC547s, AND PNP TRANSISTORS ARE BC557s.

Figure 1 Counters and transistors let you detect a transistor's terminals and determine whether the transistor under test is working.

translators, whereas G_1 to G_3 are inhibitors, which prevent T_1 to T_3 from clashing by being at +V and –V at the same time.

When you plug a functioning transistor into the test terminals, it restricts current flow in certain directions only. The series LEDs reveal these directions and, hence, indicate the type of transistor—for example, the LEDs glow red-green-red for an NPN transistor and glow green-red-green for a PNP transistor.

With this knowledge, you can easily choose the base of the transistor. To differentiate between emitter and collector you must understand the property that, under reverse bias, base-emitter junction breaks down more easily than does the base-collector junction, which is reverse-biased for normal operation.

Because transistors have different base-emitter reverse-breakdown voltages, the circuit provides a way to easily change the supply voltage (**Figure 3**). Under increased voltage, both LEDs connected with the emitter glow brightly, whereas only one LED glows for the collector (**Figure 2b** and **d**). A basic voltage of ±4V seems sufficient for detecting the base or type of transistor. By gradually increasing the supply voltage from ±4 to ±15V, you can test a variety of transistors for the emitter. This range provides a maximum reverse-breakdown voltage of greater than 26V for the base-emitter junction, taking into account the voltage drop of the series LEDs.

This circuit underwent testing and works. However, the testing employed CD4520 counters and CD4028 decoders because the CD4022/CD4017 ICs were unavailable. This replacement shouldn't cause problems. Only the voltage levels matter, which for CMOS devices is more or less the same for logic one or logic zero. You can also use only two supply voltages: ±5V for detecting the base and ±15V for detecting the emitter. EDN

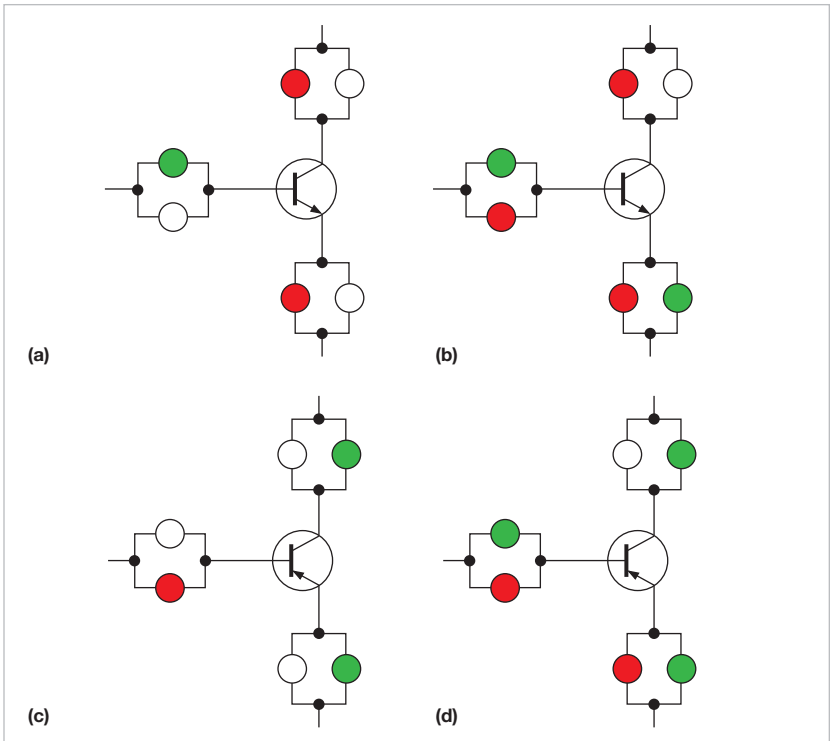


Figure 2 A reference indicates the health of a transistor under test for an NPN with normal supply voltage (a), an NPN with increased supply voltage (b), a PNP with normal supply voltage (c), and a PNP with increased supply voltage (d).

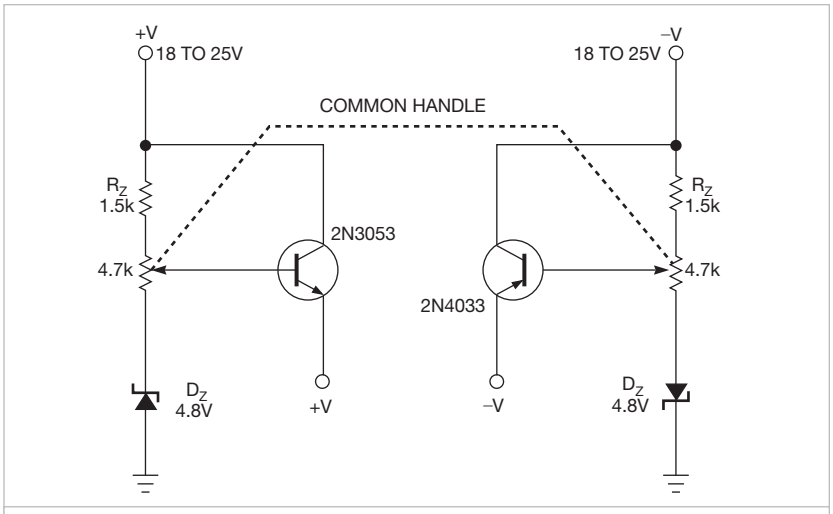


Figure 3 A common handle ensures symmetric variation of supply voltage about the ground.

Finely tune the hue of blue-light sources

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When coach cars of long-range trains comprised compartments for six to eight passengers, the passengers could choose either "white" or deep-blue light. The blue light helped passengers sleep, even when they were not in full darkness. The circuit in **Figure 1** lets you set a hue of blue light that can match your favorite blue color. Although you can accomplish this task

with another circuit (**Reference 1**), this circuit provides a finer adjustment of color and uses a narrower range from cyan to royal blue. The light is a mixture from two power LEDs, both from Avago Technologies (www.avagotech.com). LED_1, the ASMT-JC11, is a recently introduced, high-performance, thermally ruggedized, miniature, 1W cyan unit, and LED_2 is the 3W ASMT-JL31.

Two coupled current sources drive the LEDs. IC_{3A}, with a cascade of two NPN transistors, Q_1 and Q_2, forms a sink-current source that drives LED_2. IC_{3B}, a current source with a cascade of two PNP transistors, Q_3 and Q_4, drives LED_1. This PNP current source is feed-forward-operated and is controlled by the output current of the sink-current NPN source. The circuit achieves this task by routing the output sink current through feedback resistor R_{E2} of the PNP current source. If the output sink current is at full-scale, then the feedback signal for the PNP current source is also at maximum. Thus, the actual sourced current has a theoretical value of 0 mA. In contrast, if the sink current is 0 mA, then the source current reaches the full-scale value. Therefore, the sink and the source currents are complementary; their sum is a constant. The sum of the output currents is $I_O=(R_B \times I_T)/R_E$, where I_T is the value of the reference current that flows through IC_1, an Analog Devices (www.analog.com) AD590. IC_1 is a two-pole source of proportional-to-absolute-temperature current, whose value is typically 298.2 μA at room temperature. IC_1 creates the high- and low-side reference voltages, V_{REF}, which are both 400 mV and which serve as references for the two power-current sources. I_O has a value of approximately 80 mA.

With values for R_{E2} and R_{E1} tightly matched and equal to R_E, the sums of the currents flowing through the LEDs are independent upon setting IC_2, an Analog Devices AD5228, which acts as a digitally controlled potentiometer. The sum of emitted light from the two LEDs remains roughly constant as they change the final hue from cyan to royal blue.

You can interchange the position of LEDs in the circuit, but using them as the **figure** shows offers optimum voltage headroom for both power-current sources, even though the forward-voltage drop of the cyan LED is higher. The wiper positions of the DAC have margins that are typically 0.9% for zero and −2.4% for full-scale. With the Preset input high, you set the midscale setting of the wiper, W, at power-up; thus, the output light is a 50/50 mixture of both colors. For a low Preset, you reach a zero setting, resulting in full-cyan light at power-on. IC_2's internal 100-kΩ resistors force the $\overline{PU}$ and $\overline{PD}$ control pins to inactive high. As I_T's value rises linearly with absolute temperature, the circuit roughly compensates the decreasing of radiance of the LEDs.

In advertising or toys, this circuit can also provide a periodic change of the hue. If you set the Preset high and hold the $\overline{PU}$ pin low while feeding a 50%-duty-cycle, 0.05-Hz-frequency logic waveform to the $\overline{PD}$ pin, you get a slow, periodic, quasicontinuous "waving" of the color from cyan to royal blue and back. EDN

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1 Štofka, Marián, "Electronically tinge white-light source," *EDN*, Nov 4, 2010, pg 46, http://bit.ly/eQhzR5.

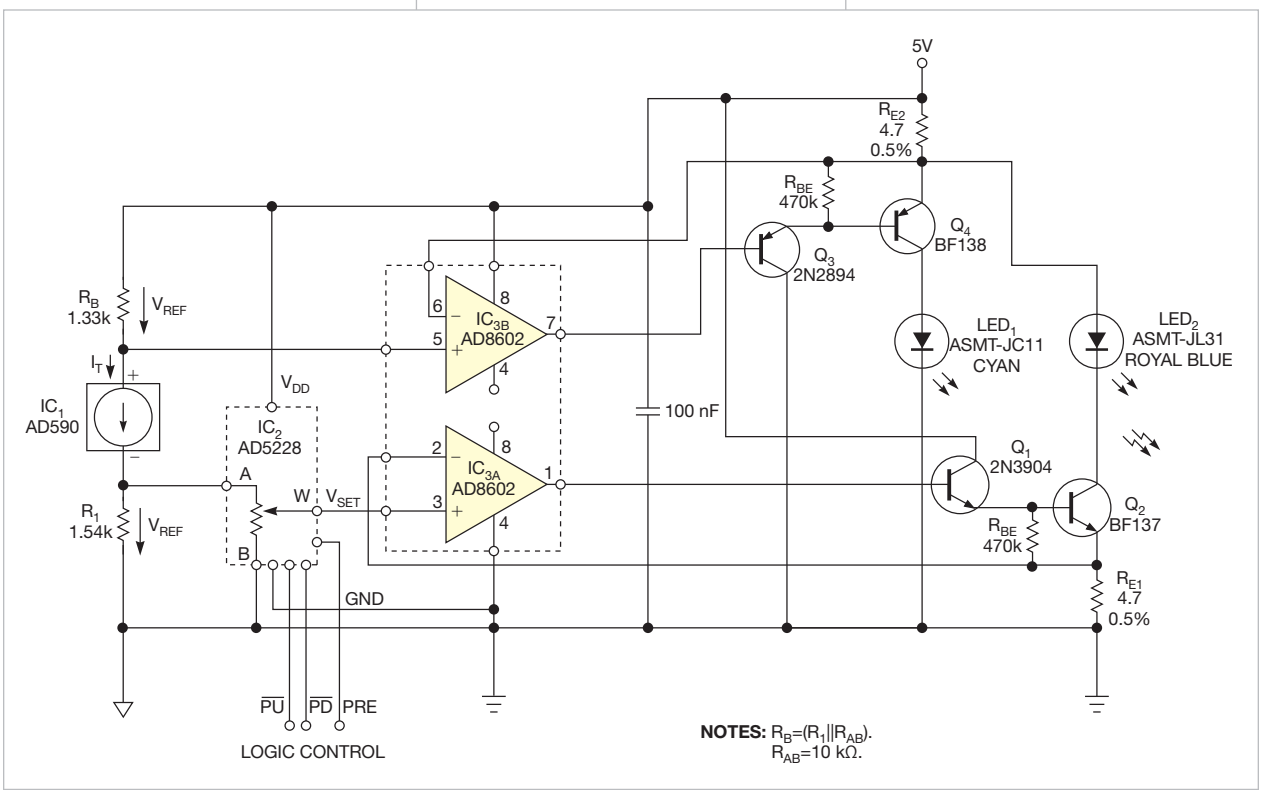

Figure 1 A current source and a current sink drive two LEDs. The balance of current sets the hue.

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READERS SOLVE DESIGN PROBLEMS

Low-component-count logic probe works with TTL and CMOS logic

Aruna Rubasinghe, University of Moratuwa, Sri Lanka

The circuit in **Figure 1** uses the LM358 dual op amp running as a comparator, plus a few other inexpensive components, to make a TTL (transistor-transistor-logic)/CMOS-logic probe. The circuit gets its power from the circuit under test, which lets it work with TTL or CMOS logic. The IC_{1A} and IC_{1B} op amps come in an LM358 package. Switch S_1 selects the TTL or the CMOS mode of operation. The green LED shows logic low, and the red LED shows logic high.

The noninverting input of IC_{1A} and the inverting input of IC_{1B} connect to the test probe. The circuit uses 90% of the power-supply voltage as CMOS-logic high and 2.7V as TTL high. It uses 0.7V as logic low for both TTL and CMOS because their logic-low levels approach 0.7V. Voltage divider R_3/R_4 divides voltage from 2.7V zener diode D_1, providing 1.35V at IC_{1A}'s noninverting input and IC_{1B}'s inverting input. Diode D_2 is forward-biased, and the 0.7V voltage across D_2 becomes the lower limit, which represents logic low. You set this voltage on the noninverting input of IC_{1B}.

In TTL mode, the voltage at the inverting input of IC_{1A} is 2V. In CMOS mode, the voltage at the inverting input of IC_{1A} is nearly 90% of the input voltage through voltage divider R_6/R_7. When the probe is in its high-impedance state in either CMOS or the TTL mode, IC_{1A}'s inverting input voltage is greater than its 1.3V noninverting input voltage. IC_{1A}'s output is low. IC_{1B}'s 1.3V inverting input voltage is greater than its 0.7V noninverting input voltage. The output of IC_{1B} is also low, and both LEDs are off.

In TTL mode, when measuring logic high, IC_{1A}'s 2.7V inverting input voltage is less than its noninverting input voltage, which is the probe voltage. IC_{1A}'s output is high. IC_{1B}'s inverting input voltage, which is the probe voltage, is greater than its 0.7V noninverting input voltage. IC_{1B}'s output is, therefore, low. The red LED turns on, indicating logic high.

When measuring logic low, IC_{1A}'s 2.7V inverting input voltage is greater than the voltage at its noninverting input, which is the probe voltage. Thus, IC_{1A}'s output is low. IC_{1B}'s inverting input voltage, which is the probe voltage, is greater than its 0.7V noninverting input voltage. Thus, IC_{1B}'s output is high. The green LED turns on, indicating a logic low.

In CMOS mode, when measuring logic high, IC_{1A}'s inverting input voltage, which is 90% of the supply voltage, is greater than the voltage at its noninverting input. The output is thus high. IC_{1B}'s inverting input voltage, which is the probe voltage, exceeds that of its 0.7V noninverting input voltage, and IC_{1B}'s output is low. The red LED turns on, indicating logic high.

When measuring logic low, IC_{1A}'s inverting input voltage, which is 90% of the supply voltage, exceeds the voltage at its noninverting input. IC_{1A}'s output is low, and IC_{1B}'s output is high because its inverting input voltage is higher than 0.7V at its noninverting input voltage. The green LED turns on, indicating logic low. When the probe's pin is pulsing, both LEDs alternately turn on and off at the pulse frequency. EDN

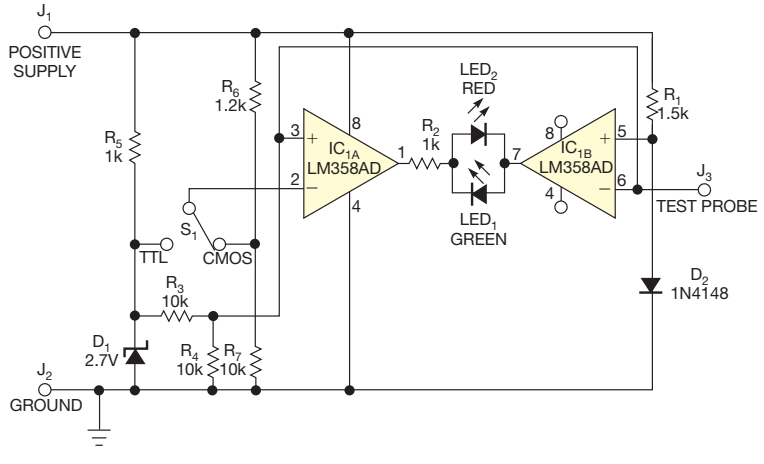

Figure 1 Two comparators and some voltage dividers determine the status of a TTL or a CMOS-logic signal.

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Circuit implements photovoltaic-module simulator

José M Blanes and Ausiàs Garrigós, University Miguel Hernández, Elche, Spain

Electronics engineers often use photovoltaic-module simulators to test dc/dc-power converters, inverters, or MPPT (maximum-power-point-tracking)-control techniques. The use of these simulators lets you work in the laboratory with predefined photovoltaic conditions, thus avoiding the drawbacks of real photovoltaic modules. Various commercial simulators are available, but they are often expensive.

This Design Idea presents a simple circuit that works as a photovoltaic-module simulator using a dc-voltage source as its input. The circuit employs the simplest equivalent circuit of a photovoltaic module: a current source in parallel with a diode. The output of the current source is directly proportional to the irradiance, and the characteristics of the parallel diode change with temperature.

The current source in **Figure 1** operates at a short-circuit current as high as 2A and employs two MJ15023 power bipolar transistors, Q_2 and Q_3, working in the linear region. The value of the current is proportional to the transistor's base current. You can control the short-circuit current with potentiometer R_2, whose change in value forces a variation in Q_1's collector current and, thus, the base current of Q_2 and Q_3.

The circuit has 50 MUR1520 diodes that connect in series and are in parallel with the current source. You can short-circuit these diodes in groups of 10, so you can choose the number of series diodes: 10, 20, 30, 40, or 50. If you need more precision, you can increase the number of diode groups in the simulator, providing more output curves.

Figures 2 and **3** show the current- and power-voltage characteristics of

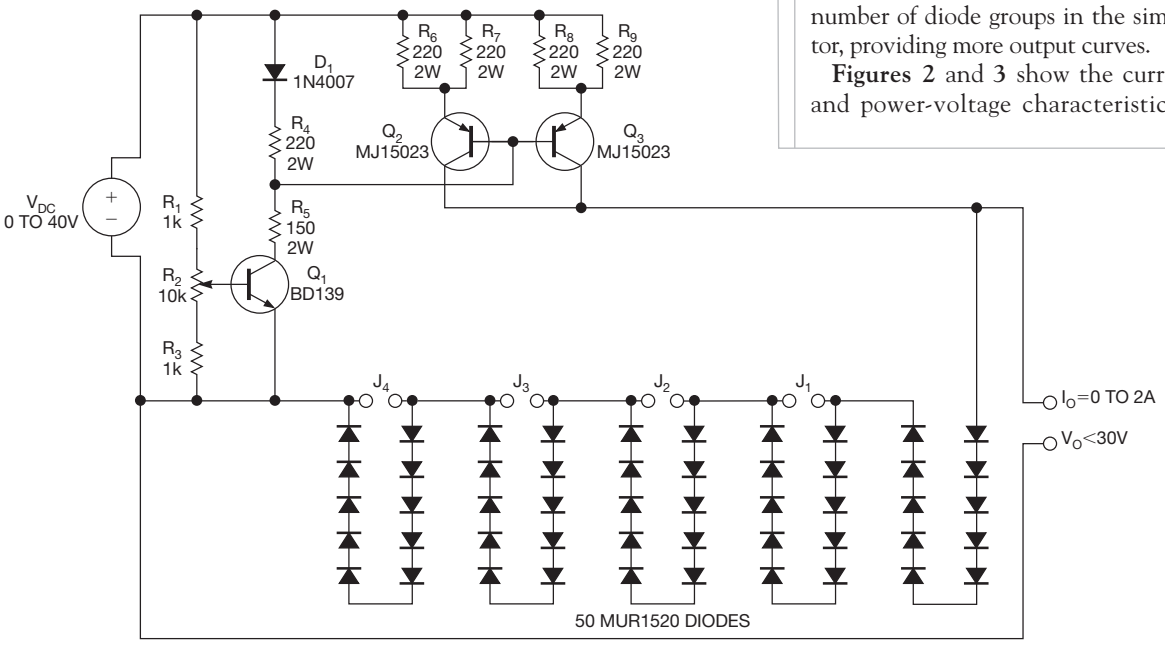

Figure 1 You can change the photovoltaic characteristics of this simulator by modifying the current-source output value or connecting 10 to 50 diodes in series. You can short-circuit these diodes in groups of 10.

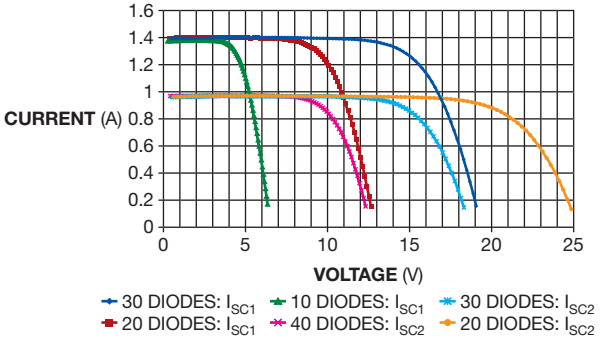

Figure 2 Modifying the current-source output value also modifies the short-circuit current.

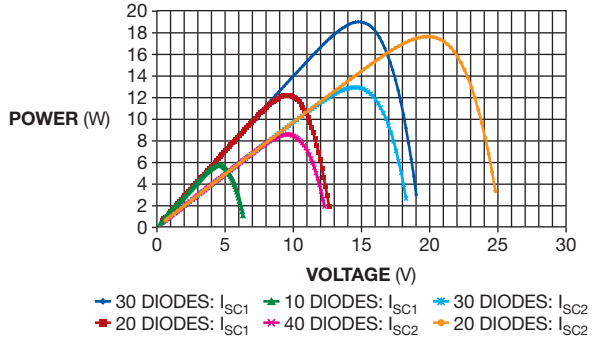

Figure 3 For each combination of diodes, the maximum power-point voltage changes.

the photovoltaic-module simulator for two current-source values and a different number of diodes. Extracting these curves required the use of an electronic load (**Reference 1**). The short-circuit current of the simulated module changes, modifying the current-source output value, and, when you connect or disconnect diodes, it varies the open-circuit voltage of the module. You can use digital circuits to control the simulator to create photovoltaic patterns. EDN

REFERENCE

1 Ausiàs Garrigós and José M Blanes, "Power MOSFET is core of regulated-dc electronic load," *EDN*, March 17, 2005, pg 92, http://bit.ly/fz8geK.

Switch circuit controls lights

C Castro-Miguens, University of Vigo, Spain,
and JB Castro-Miguens, Cesinel, Madrid, Spain

Cities and towns worldwide are considering and installing LED streetlights to help save electric energy, reduce costs, protect the environment, and improve lighting for their citizens. Despite this trend, the lamps' turn-on/turn-off time control is receiving little attention.

A suitable control can achieve an important energy saving because lights can operate too late, too early, or both, wasting energy or providing insufficient light. Using a twilight switch can significantly reduce energy consumption in all types of lamps (**Figure 1**). It offers a cost-effective, compact, and reliable way of providing lighting time control.

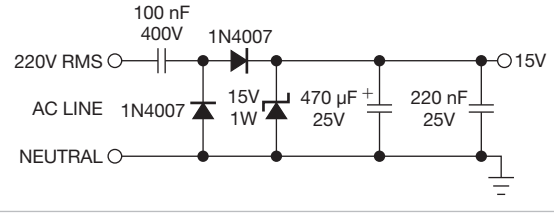

Figure 1 This charge pump feeds the twilight switch from the ac line with high efficiency.

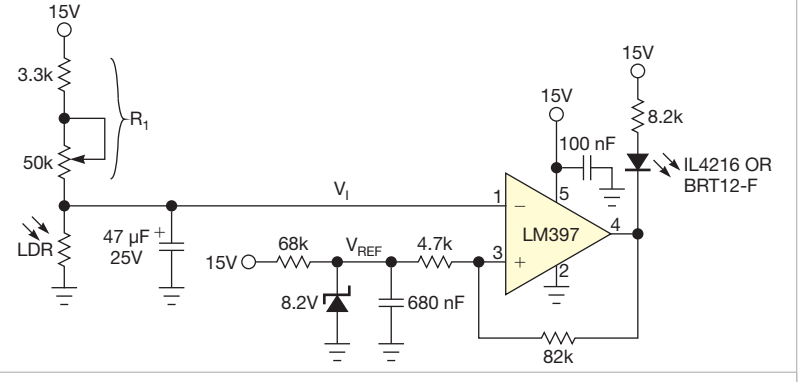

Figure 2 The circuit uses a light-dependent resistor to measure the ambient-light level.

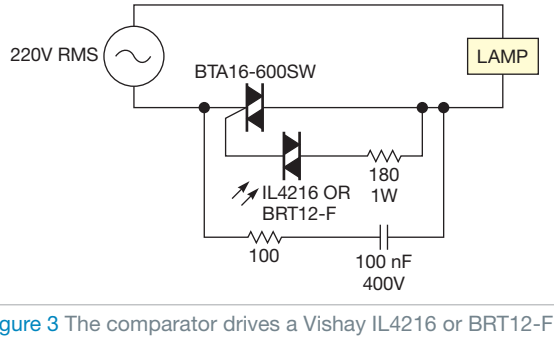

Figure 3 The comparator drives a Vishay IL4216 or BRT12-F optocoupler with a TRIAC output.

The circuit does not use a relay. Therefore, it has no moving parts, and it is not prone to contact oxidation. It uses a TRIAC (triode alternating current) that can switch hundreds of watts.

The circuit requires little power. It uses a charge pump to feed the circuit from the ac line, drawing less than 37 mW for a 220V-rms ac line. It uses just a few low-cost components.

You can adjust the circuit's darkness and illuminance level that switches the light on and off using only onboard potentiometer R_1. The circuit automatically turns on the lamps at nightfall and turns them off at daybreak. You can use it with incandescent lights, fluorescent lights, or LEDs.

The circuit uses an LDR (light-dependent resistor) to measure the ambient-light level (**Figure 2**). Be sure that the LDR you use has a spectral response similar to that of the human eye to achieve good performance. It uses a hysteresis comparator because a basic comparator configuration oscillates or produces a noisy output when the illumination level is close to the edge between natural light and darkness. Hysteresis creates two switching thresholds in the circuit: The upper threshold voltage is 8.47V for the rising input-voltage change from natural light to darkness, and the lower threshold voltage is 7.75V for the falling input-voltage change from darkness to natural light. The relationship between the 82-kΩ and the 4.7-kΩ resistors controls the 0.72V hysteresis. This value is adequate to avoid the false triggering that light noise can cause.

THE CIRCUIT DOES NOT USE A RELAY, AND SO IT HAS NO MOVING PARTS.

When the ambient light falls below the level that R_1 sets, the input volt-

age, V_1, rises above the upper threshold voltage and the output of the comparator decreases, switching on the TRIAC. When the ambient light rises above the level that R_1 sets, the input voltage decreases below the lower threshold voltage and the output of the comparator increases, switching off the TRIAC.

You must provide a mechanical isolation between the LDR and the lamp light to prevent the formation of a feedback path to the LDR. Otherwise, the lamp light will cause an oscillation at the comparator's output and then in the lamp's state. The BTA16-600SW, which is available from many sources, is suitable for switch lamps operating at more than 2000W.

The comparator drives a Vishay (www.vishay.com) IL4216 or BRT12-F optocoupler with a TRIAC output (**Figure 3**). The optocoupler, in turn, drives the BTA16-600SW TRIAC that controls the lamp. EDN

Isolated PWM suits low frequencies

Tim Regan, Linear Technology, San Jose, CA

Many industrial- and medical-system circuits require isolation from the mains-ac power. You can often send a signal across the isolation barrier using a small transformer; transformers do not pass low-frequency signals well. The circuit in this Design Idea converts a low-frequency PWM (pulse-width-modulated) signal to a higher frequency, which you pass across the transformer, and retains the duty cycle. Once the frequency is on the other side, you can then convert the PWM signal back to an analog voltage.

The circuit converts a 1-kHz PWM signal to a 100-kHz signal with the same duty cycle (**Figure 1**). This 100-kHz signal easily couples across an isolation transformer. You then filter it to provide a dc control voltage on the isolated side. IC_2, an LTC6992-2, is a voltage-controlled PWM IC. A voltage ranging from 0 to 1V on the MOD input pin varies the duty cycle of the output from 5 to 95%. The duty cycle does not reach 0 or 100%, which would not pass through the transformer. Resistor R_{SET} fixes an internal master-oscillator frequency of 100 kHz. The voltage on the DIV pin sets a divider ratio. An internal 4-bit ADC translates the analog voltage to a digital-divider value. With the input shored to ground, the divider ratio is one, and the circuit outputs the oscillator frequency.

R_2 and C_2 make amplifier IC_1 a voltage integrator. It servo-controls the voltage at the MOD pin of IC_2. R_1 and C_1 filter the input signal to an average dc value. The integrator compares this value with the average dc value of the IC_2 output that you filter with R_3 and C_3. This step forces the 100-kHz output signal to the same duty cycle as the 1-kHz input signal. The time constants of these filters should be much longer than the clock period to minimize duty-cycle jitter. You use a 500-msec time-constant network for the 1-kHz PWM signal and a 1-msec time-constant network with the 100-kHz PWM signal. The amplitude of each signal must be the same for an accurate match of the two duty cycles. For this reason, IC_2's power-supply voltage is the same supply the PWM controller uses. Any supply-voltage variation affects each signal in the same way, providing insensitivity to power-supply variation.

IC_2 has 20 mA of output current to drive the primary of the isolation transformer, and comparator IC_3 squares up the 100-kHz PWM signal on the isolated side of T_1. You can use this output directly as a digital-control signal if necessary. In this circuit, you filter the signal with a 1-msec RC lowpass network and then buffer the signal with voltage-follower amplifier IC_4, yielding a dc analog-control voltage.

The circuit accurately replicates a stepped increase in the input PWM duty cycle (**Figure 2**). The circuit operates from a 5V supply. The average voltage changes from 1 to 4V when you change the input duty cycle from 20 to 80%. The slow change is due to the 500-msec time-constant filter, an acceptable scenario in cases in which a gradual change in the isolated control signal is acceptable. You can circumvent the slow response at the expense of some overshoot if you need a faster response. For this task, you use an anticipator circuit, as a previous Design

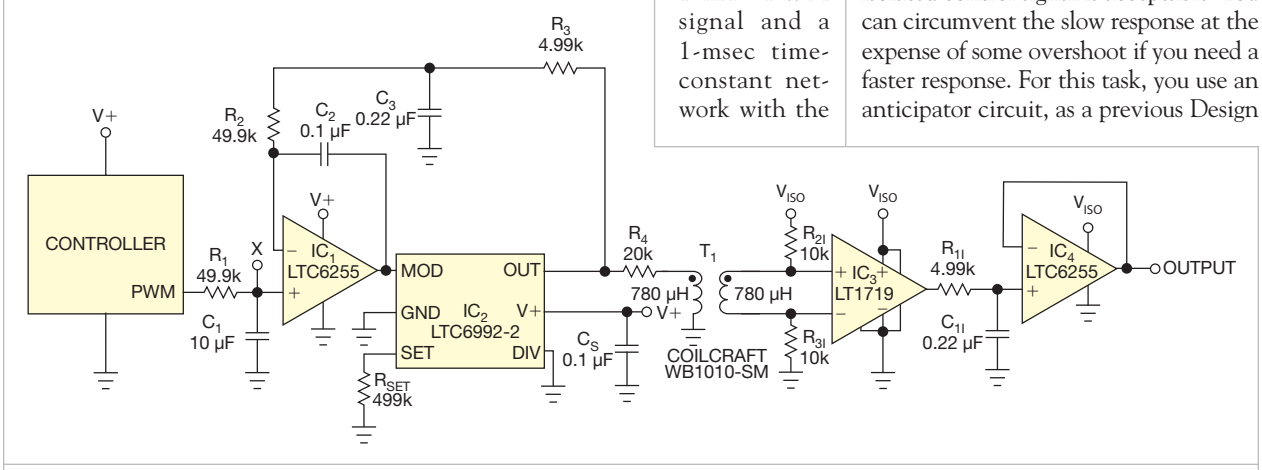

Figure 1 This circuit creates a 100-kHz PWM signal from a 1-kHz PWM signal to send it across an isolation transformer. The output is an integrated dc control voltage.

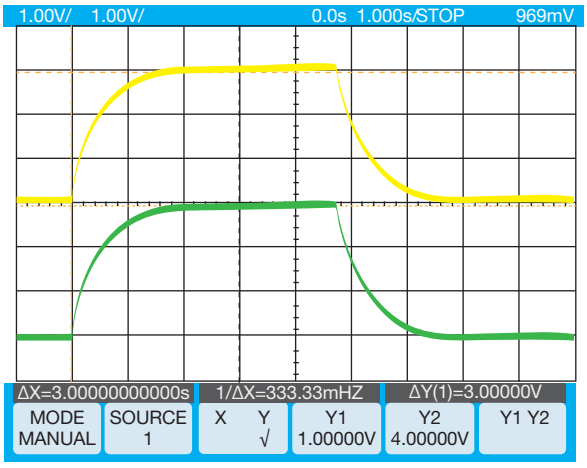

Figure 2 The circuit gives a gradual exponential response to a 20 to 80% step change in duty cycle. A 500-msec time constant filters the input PWM (yellow). The filtered, 100-kHz isolated signal closely matches the input (green).

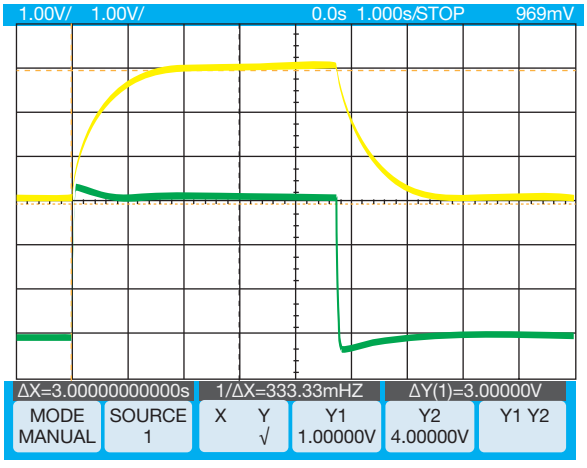

Figure 3 An anticipator circuit speeds the output response (green).

Idea describes (**Reference 1**). Adding the anticipator circuit at the X node of **Figure 1** results in a faster response to a final value (**Figure 3**).

You add another voltage-controlled PWM IC to re-create the 1-kHz PWM signal on the isolated side (**Figure 4**). You use amplifier-integrator circuit IC_6 to servo-control the duty cycle of IC_7. Resistor R_{SETI} programs IC_7 for 1-kHz, 5- to 95%-duty-cycle operation. The circuit forces the 1-kHz output duty cycle to equal the 100-kHz input-signal duty cycle. Again, the supply voltage for comparator IC_5 and the PWM device must be the same. If you want minimum duty-cycle ripple, set filter R_{2I} and C_{2I} to have a 500-msec time constant. Unfortunately, this approach would make the response time of the reconstructed output slow. You cannot use the anticipator circuit when you re-create the slow PWM signal because the slow signal is now the dependent variable in the circuit, and fast jumps in the feedback voltage would result in the loop's continuously hunting and never settling to a final value. Use instead a 10-msec time-constant filter on the 1-kHz output to obtain a reasonable response time and then minimize duty-cycle ripple with an additional lowpass network comprising R_{4I} and C_{4I}.

Note that the feedback signal for integrator IC_1 in **Figure 1** is on the negative pin and that the feedback signal to re-creation integrator IC_6 is on the positive pin. If you connect the fast-responding input signal to the positive input of IC_6, it would cause a large overshoot in the duty cycle of the output signal and a long recovery time. You compensate for the polarity reversal by biasing the DIV pin of IC_2.

Setting the DIV pin above $V_{SUPPLY}/2$ programs the output-control polarity to change from 95 to 5% duty cycle with an increasing voltage applied to the MOD pin. An increase in the 100-kHz signal's duty cycle now ramps down the MOD pin and increases the 1-kHz output signal's duty cycle to match it. EDN

REFERENCE

1 "Anticipator circuit speeds signal settling to a final value," *EDN*, March 17, 2011, pg 58, http://bit.ly/h7qZPo.

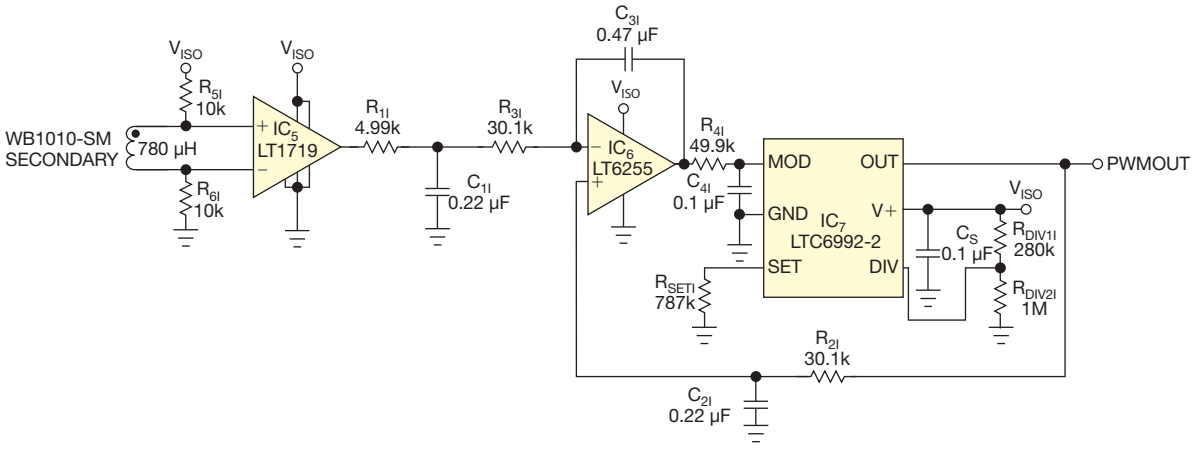

Figure 4 This circuit re-creates the 1-kHz PWM control signal on the isolated side. It cannot use the anticipator circuit, but R_{4I} and C_{4I} provide extra lowpass filtering, helping to reduce output jitter.

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READERS SOLVE DESIGN PROBLEMS

Increase efficiency in embedded digital-I/O lines

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Digital-I/O-multiplexing techniques, such as "Charlieplexing" or "Gugaplexing," let an eight-digit, seven-segment LED display connect to nine I/O pins of a microcontroller (**references 1** and **2**). These methods use lower-duty-cycle timing, which requires a driver between the microcontroller's I/O lines and the display to achieve good visibility. The circuit in **Figure 1** uses an 8+N/2 I/O bus for interfacing an N-digit display and as many as eight buttons on the same bus. This method needs no driver. You can apply it to any programmable device with LED-driving capabilities, such as small PIC (www.microchip.com) or Atmel (www.atmel.com) microcontrollers.

In **Figure 1**, R_8 is a segment current-limiting network resistor for the IC_1 common-anode LED display and the IC_2 common-cathode LED display. Any combination of standard and superbright displays for this IC_1/IC_2 pair is acceptable with proper duty-cycle timing adjustment in firmware. The R_7 network and D_1 to D_8 switching diodes act as antighosting devices. "Ghosting," or faint illumination, is the partial illumination of the segments, which should be in an off state, as a result of switching glitches or unsuitable voltage levels on the driving pins when those pins are in a high-impedance

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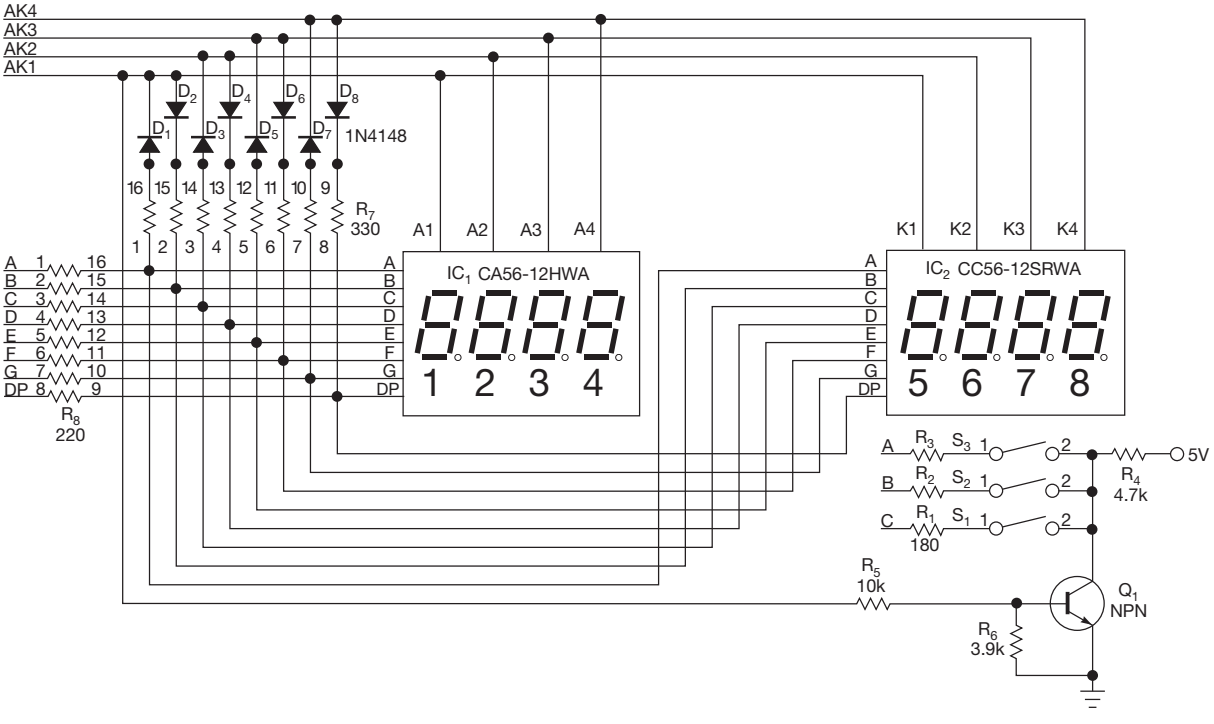

Figure 1 Common-anode and common-cathode LED displays and buttons can connect to the same bus.

state. Ghosting results from using all the microcontroller's I/O: output-high, output-low, and high-impedance logic levels, switching between them in an infinite-loop sequence (**Table 1**).

The following **equation** calculates the value of R_7: $R_7=(V_{SAFE}–0.6V)/10I_{GHOST}$, where 0.6V is the voltage drop of diodes D_1 through D_8 at 25°C, I_{GHOST} is the threshold value of the static-leakage current for which the ghosting effect is visible but minimal, and V_{SAFE} is the voltage potential value that may appear on any segment when the segment is not illuminated.

You can experimentally find I_{GHOST} at an ambient-light level of less than 10 lux by injecting a small current into a separately powered digit segment and observing the current value and segment voltage drop at the moment when the segment begins to light up. For a superbright display, I_{GHOST} should be approximately 70 µA. The I_{GHOST} current creates an unwanted voltage drop on the segment LED, V_{GHOST}: $V_{GHOST}=1.54V$ and $V_{SAFE}\leq kV_{GHOST}$, where k, a factor of confidence, ranges from 0.5 to 0.7, compensating the V_{GHOST} dispersion of displays. In this example, V_{SAFE} is 0.7V for a superbright LED display and 1V for a standard display. If you combine normal and superbright display types, choose the smallest V_{SAFE} for the computed value of R_7.

Figure 2 Without R_7, ghosting is visible (left). With R_7, the display is clean (right), even when you push buttons S_1 through S_3.

Reading electrode buttons is an asynchronous procedure, unlike digital multiplexing; thus, any combination of button presses must not turn on any segment of IC_1's or IC_2's digit group. R_1, R_2, and R_3 limit the current through IC_1 segments below I_{GHOST} when Q_1 is on and AK1 is at an output-high level. R_4, R_5, and R_6 polarize Q_1; R_6 keeps Q_1 off even when AK1 is in a high-impedance state; and R_4 limits the Q_1 collector current. Note that the weak pullup of the A, B, and C microcontroller inputs is on during the button-reading sequence. You can download the firmware source for the PIC16F886 driving the display in **Figure 1** from http://bit.ly/e1cwCu. Adding R_7 and D_1 through D_8 eliminates ghosting (**Figure 2**). EDN

REFERENCES

1 Sangalli, Luke, "Charlieplexing at high duty cycle," *EDN*, June 25, 2009, pg 44, http://bit.ly/ehxi3w.

2 Gupta, Saurabh, and Dhananjay V Gadre, "Multiplexing technique yields a reduced-pin-count LED display," *EDN*, Oct 16, 2008, pg 58, http://bit.ly/fJhrE8.

TABLE 1 SWITCHING SEQUENCE FOR LED DISPLAYS

Sequence	Display on digit	Read buttons	Common electrode buttons				Segments bus
			AK1	AK2	AK3	AK4	A, B, … D_P
1	IC_1-1	X	High impedance	High impedance	High impedance	High impedance	Output low=data
2	IC_1-2	X	High impedance	High	High impedance	High impedance	Output low=data
3	IC_1-3	X	High impedance	High impedance	High	High impedance	Output low=data
4	IC_1-4	X	High impedance	High impedance	High impedance	High	Output low=data
5	X	Yes	High	X	X	X	Input
6	IC_2-5	X	Low	High impedance	High impedance	High impedance	Output high=! data
7	IC_2-6	X	High impedance	Low	High impedance	High impedance	Output high=! data
8	IC_2-7	X	High impedance	High impedance	Low	High impedance	Output high=! data
9	IC_2-8	X	High impedance	High impedance	High impedance	Low	Output high=! data

Modulating a reference allows maximum-value search for phase detection

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A lock-in amplifier is a useful tool for measuring a signal's amplitude and phase. A data-acquisition card can digitize the amplifier's output signal, and software can calculate amplitude and phase. A DSP or a general-purpose processor can also calculate amplitude and phase. The circuit in this Design Idea integrates two Analog Devices (www.analog.com) AD9954 DDS (direct digital synthesizers) and an AD630 balanced modulator/demodulator into a low-cost lock-in amplifier (**Figure 1**).

One AD9954 generates a reference signal and a measurement signal for the target. The AD630 then modulates the reference signal and the target signal. A lowpass filter removes the $2\omega t$ component that you calculate from the signal modulation. When the modulator function of the AD630 operates at frequencies higher than 50 kHz, however, the output waveform of the AD630 causes a measurement error and thus a signal-analysis error in the phase measurement.

When the reference and measurement signals are in phase, the result of

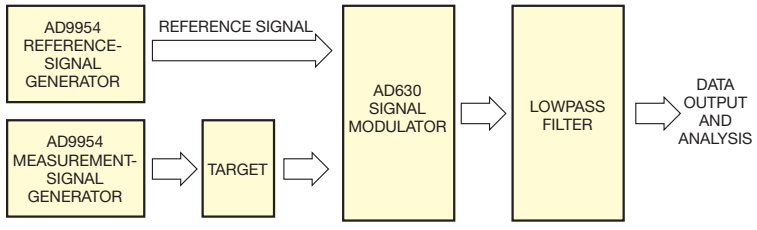

Figure 1 A lock-in amplifier comprises two signal generators, a modulator, and a lowpass filter.

modulation is at its maximum. A maximum-value-search method improves the operating frequency of the AD630's modulation function. Using a flow chart, you can control two AD9954s to generate the reference and target signals (**Figure 2**). The AD630 then modulates the two signals, digitizes the results, and stores them in registers. Later, you shift the phase of the reference signal and repeat the procedure until the circuit sweeps through all possible differences in phase.

You then search for the maximum value in the data set. When you modulate the signal at different phases, the phase shift of the reference signal indicates the phase shift of the target. **Table 1** represents the real case with 30° phase shift between the reference and the target signals. At 50 kHz, the error of lock-in calculation is 19%, which is larger than the 5% phase shift at 10 kHz. Those results indicate weak performance at high frequencies. Using the search results, you can increase the accuracy to 3% at 10 kHz and 7% at 50 kHz. EDN

TABLE 1 ERROR AS A FUNCTION OF FREQUENCY

Operation frequency (kHz)	Lock-in calculation error	Maximum-value-search error
1	29.669° (1%)	29.669° (1%)
10	28.451° (5%)	29.201° (2%)
50	24.275° (19%)	26.338° (12%)

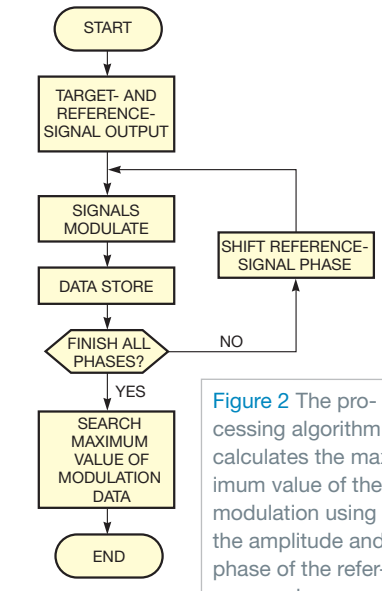

Figure 2 The processing algorithm calculates the maximum value of the modulation using the amplitude and phase of the reference and measurement signals.

Offline supply drives LEDs

TA Babu, Chennai, India

LEDs need power when rectified ac-mains voltage drops during its cycle. The circuit in **Figure 1** lets you use an inductor-less, switching, offline power supply as an LED driver for emergency-exit signs and neon-light replacements. The design uses off-the-shelf components, offers efficient operation without an inductor in the dc side of the circuit, has no high-voltage capacitors, operates directly from either 120 or 230V ac, has minimal power dissipation, and has adjustable output voltage.

The circuit operates by controlling the conduction angle of MOSFET Q_2. When the rectified ac voltage is below the high-voltage threshold, V_{TH}, which D_1 sets, the series pass transistor turns on. The series pass transistor turns off when the output storage capacitor, C_2, charges up to the regulation point.

The circuit's output voltage decays when Q_2 is off and when the rectified ac is below the output voltage (**Figure 2**). The load and the value of C_2 determine the amount of decay. The switch conducts only when it has low voltages across it, minimizing power dissipation.

The output capacitor charges on the rising edge of a sine wave, which achieves reasonable efficiencies. Fusible resistor R_1 provides catastrophic-failure protection and limits input inrush when you first apply ac power. A 15V diode, D_2, limits the voltage to the gate of Q_2 and limits the voltage across transistor Q_1.

The current interruption in the MOSFET causes ringing on the drain-to-source voltage of Q_2, creating conducted EMI (electromagnetic interference). The 2.2-mH choke, L_1, and capacitor C_1 suppress EMI. This design maintains a fairly constant illumination over

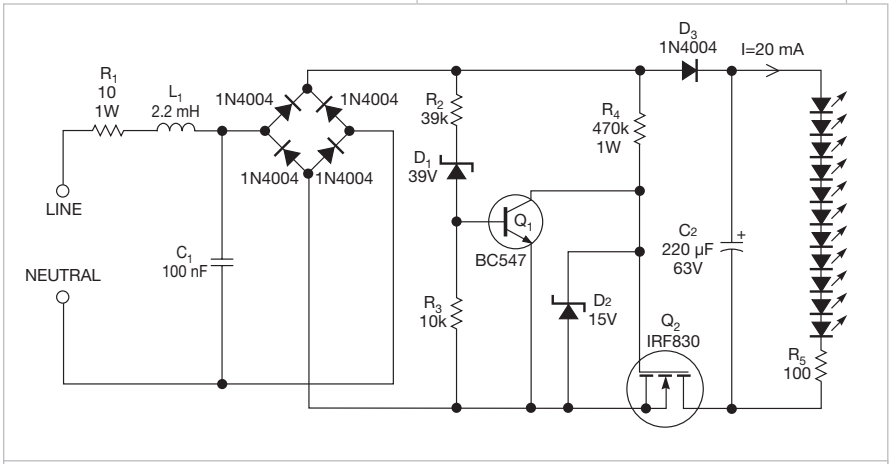

Figure 1 The transistor and MOSFET provide current to keep the LEDs lit.

a wide voltage variation in the input. If necessary, you can add a few more such strings to suit your requirements.

Note that this circuit does not provide galvanic isolation. Touching any part of the circuit during operation can give you an electric shock. EDN

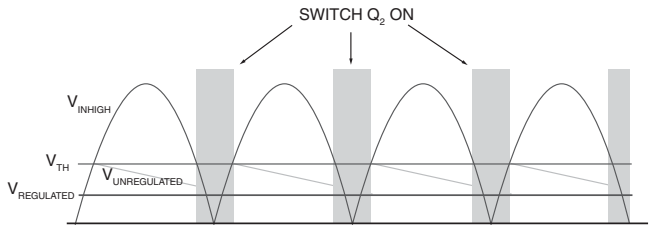

Figure 2 Switch Q_2 turns on when the rectified ac input voltage drops below a threshold.

Light an LED without wasting energy

Raju R Baddi, Tata Institute of Fundamental Research, Maharashtra, India

LEDs need current to illuminate, and current usually flows through a power supply to an LED. A typical LED-driver circuit uses a transistor to provide current and a series resistor to decrease the voltage you apply to the LED. Unfortunately, the energy $(V_{SOURCE}–V_{DIODE})×I_{DIODE}$ in a transistor/resistor combination goes to waste, giving off heat.

The circuit in **Figure 1** can minimize this waste by using an inductor and an oscillating circuit to control the current through the LED—energy that would otherwise go to waste. Inductor L_1 stores power and channels it back into the LED.

You might think to put two or more LEDs in series instead, but that configuration doesn't let you change the intensity and still save power. This circuit provides a general way of saving power without worrying about the intensity issues or operating voltage of the device. Transistors Q_1 and Q_2 alternately turn on and off. Q_1 increases the current through the LED from a certain minimum value when it connects the L_1/LED combination to a voltage source. Transistor Q_2 discharges stored energy in inductor L_1 through the LED. The current falls between a maximum and a minimum. Assume that transistors Q_1 and Q_2 are lossless switches in the analysis of this circuit.

Because the inductor doesn't let the current grow suddenly, it controls the average current through the LED to a desired value. The inductor also stores energy, which also powers the LED. You can obtain details, the average current through white LED D_3 as a function of inductance, and other parameters in the online version of this Design Idea at www.edn.com/110421dia. The following **equations**, which apply to the output of G_2, set the on- and off-times:

$$t_{OFF} \simeq R_1 C \ln\left(\frac{V+V_T-0.6}{V_T-0.6}\right);$$

$$t_{ON} \simeq R_2 C \ln\left(\frac{2V-V_T-0.6}{V-V_T-0.6}\right),$$

where V is the supply voltage and V_T is the input threshold voltage of the CMOS gates at supply-voltage V.

You can expect efficiencies as high as 80% with this circuit. Simulation results produce values of average current approximately the same as those in the Web version of this Design Idea. In this circuit, the supply current is less than the current through the LED because of the stored energy.

The current through the LED has a maximum and a minimum, which the on- and off-times of Q_1 and Q_2 set, along with other parameters, such as the value of L_1. You can use a 5- to 10-mH ferrite-core inductor for L_1 with a white LED with a forward-voltage drop of approximately 3V. For supply voltages of 7 to 15V, use a better transistor than Q_2, such as the 2SC3134, because of the reverse breakdown voltage of the base-emitter junction. The C1364 transistor in the **figure** works well at voltages as high as 9V. The **equations** apply to the CD4011BP, although you can substitute the HEF4011BP, which consumes less power. EDN

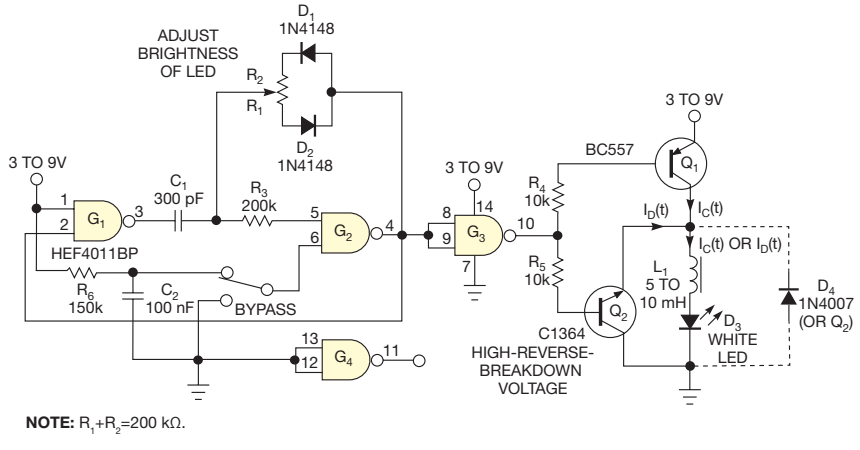

Figure 1 This circuit lights an LED without wasting power when the source voltage is much higher than the LED's operating voltage.

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READERS SOLVE DESIGN PROBLEMS

Circuit secures bootstrap operation under light load

Chee H How, Kuala Lumpur, Malaysia

A previous Design Idea highlights a potential issue of a bootstrap IC under light-load or precharged-load operation (**Reference 1**). The circuit in **Figure 1**, with the additional circuit in the green box, fixes the problem of a voltage dip in the bus-voltage signal. The waveforms in **Figure 2** demonstrate how this problem takes place in buck converter IC_{1B} when its output voltage, V_{BUS}, dips below the regulation point at a fixed rate under no load. By inspecting the other traces in **Figure 2**, you can conclude that the dip of V_{BUS} occurs when the bootstrap voltage falls below its threshold of 8.66V (Trace 3), causing the buck converter's switching action to cease. This situation intensifies when the bus voltage approaches the input voltage.

During freewheeling operation of DCM (discontinuous-conduction mode), the output signal (**Figure 3**, Trace 4) tends to settle at the bus voltage after inductor L_1 completely discharges. This action prevents bootstrap

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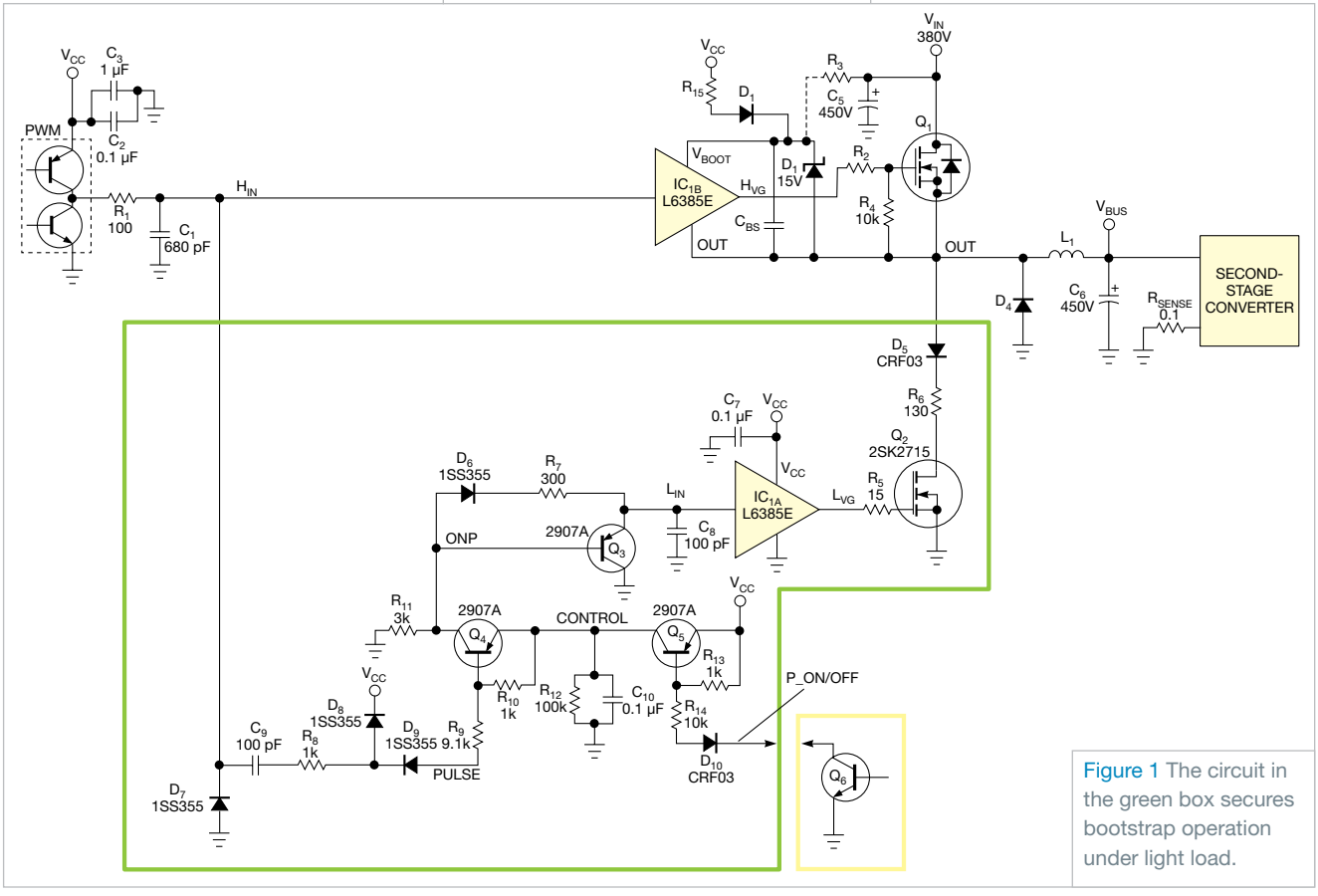

Figure 1 The circuit in the green box secures bootstrap operation under light load.

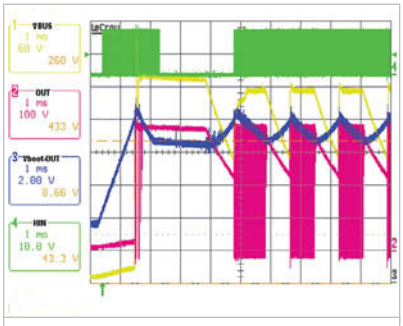

Figure 2 A 380V-dc buck converter suffers from output dipping under no-load conditions. Trace 1 is the buck converter's output voltage; Trace 2 is the switching-node voltage; Trace 3 is the voltage across the bootstrap capacitor, V_{BS}; and Trace 4 is the input signal to the bootstrap's high-side driver, H_{IN}.

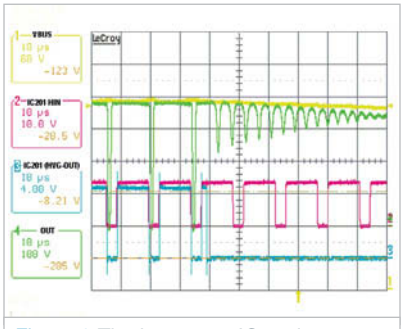

Figure 3 The bootstrap IC undergoes premature termination under no-load conditions. Trace 1 is the buck converter's output voltage, V_{BUS}; Trace 2 is the input signal to the bootstrap's high-side driver, H_{IN}; Trace 3 is the high-side output of the bootstrap driver, V_{OH}; and Trace 4 is the switching-node voltage, OUT.

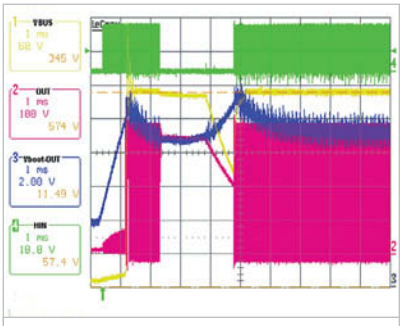

Figure 4 With Figure 1's subcircuit at a no-load condition, Trace 1 is the buck converter's output voltage, V_{BUS}; Trace 2 is the switching-node voltage, OUT; Trace 3 is the voltage across the bootstrap capacitor, V_{BS}; and Trace 4 is the input signal to the bootstrap's high-side driver, H_{IN}.

capacitor C_{BS} from charging, which eventually causes the bootstrap voltage in **Figure 2** to fall below 8.66V. Hence, the buck converter stops switching.

The circuit in **Figure 1**'s green box aims to solve the problem. It starts by tapping the input signal to the bootstrap's high-side driver to generate an inverted and delayed short pulse to control Q_2. Upon activation, Q_2 forces the output signal momentarily low, which provides an opportunity for C_{BS} to charge. R_8, R_9, R_{10}, R_{11}, and C_9 set the turn-on period of Q_2. This period must not exceed the dead time of the PWM (pulse-width-modulated) signal. If Q_2's turn-on time is too long, the converter's efficiency will degrade, or the C_{BS} might not sufficiently charge. Inadequate charging of Q_2 involves multiple component values and operating parameters, such as Q_2's turn-on time, and you might have to empirically tune the delay time to accommodate for these effects. The values in **Figure 1** produce a Q_2-turn-on time of 1 µsec and delay time of 450 nsec in a 70-kHz switching frequency.

The Q_5 network is optional. It lets you disable operation of Q_2 when it is not necessary by linking the P_on/off signal to an open collector, Q_6. The low section of IC_{1A} drives Q_2. You must experimentally select the value of R_6. A resistance value that is too low induces larger current spikes upon activation of Q_2. On the other hand, a resistance value that is too high causes C_{BS} to insufficiently charge.

Resistor R_7 and capacitor C_8 control the delay time between the falling edge of the input signal to the bootstrap's high-side driver and the rising edge of IC_{1A}'s LVG (low-voltage) pulse. **Figure 4** displays the waveform of the same converter after the inclusion of the additional circuit. In this case, V_{BUS} (Trace 1) remains stable and the output signal from the buck regulator switches continuously, lacking the gaps with switching that the waveforms of **Figure 2** show. EDN

REFERENCE

1 Larson, Justin, and Frank Kolanko, "Buck regulator handles light loads," *EDN*, Sept 9, 2010, pg 48, http://bit.ly/eVbMdP.

Build an accurate bipolar voltage reference

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Pulse generators often need voltage comparators with accurately defined hysteresis, and such comparators need bipolar voltage references. Most voltage-reference-cell ICs are referenced to their low-side supply rail. If your circuit needs both positive and negative voltages, you could create the negative reference voltage by connecting a –1 gain inverter to the output of an IC reference cell. If your analog circuit runs from a single power supply, however, you must shift the common-mode voltage to a specific level. You can use the circuit in **Figure 1** for that task.

Reference cell IC_1's output voltage, V_{REF}, connects to the noninverting input of amplifier IC_2, an AD8475. This high-precision, differential-output, ×0.4/×0.8 amplifier in this case connects as an ×0.8 amplifier (**Reference 1**). The negative input, –IN, of IC_2 is grounded. Voltages at its positive and negative outputs form the positive- and negative-output reference voltage, referenced to common-mode voltage V_{COM}. The magnitude of the generated reference voltages is $(1/2)\times0.8\times V_{REF}=1V$.

The AD8475's gains of 0.4 and 0.8 have a tolerance of no more than 0.05%

because of the device's laser-trimmed internal gain-setting resistors. This circuit takes advantage of the AD8475's gain-setting options. Typical use of the device as a ×0.8 amplifier keeps the +VIN0.4× and –VIN0.4× unconnected. In the circuit in **Figure 1**, however, these inputs interconnect, forming a high-precision 1-to-1 voltage divider of V_{REF}.

The V_{COM} input of the AD8475 connects to this node, and the common-mode voltage of the generated reference voltages becomes $V_{REF}/2$. Case A in **Table 1** shows that the measured common-mode voltage is approximately 0.6% lower than $V_{REF}/2$. This difference stems from the fact that the V_{COM} input connects within the AD8475 through one 200-kΩ resistor to the V_S pin and through another 200-kΩ resistor to ground. You can, therefore, model the V_{COM} input as a source of $V_S/2$=2.5V with a series resistance of 100 kΩ. This series resistance acts as if it connects in parallel to the $R_{+VIN0.4×}$ resistor, which results in a slight imbalance in the 1-to-1 divider ratio. In cases B and C, the V_{COM} pin connects to Point A. The compensation resistor connects only in Case C. You can prove from the V_{GND} values in cases B and C that R_{COMP} pushes the relative error of voltage at the COM output from 0.632% to –0.032%.

In many applications, the magnitude of difference of bipolar reference voltages is important, and this imbalance has no effect on it. If, however, your application requires a high-accuracy common-mode voltage, you can connect a 100-kΩ compensation resistor between the V_{COM} pin and ground, and the circuit thus operates as in Case C. This approach almost fully retains the accuracy of the 1-to-1 divider ratio. EDN

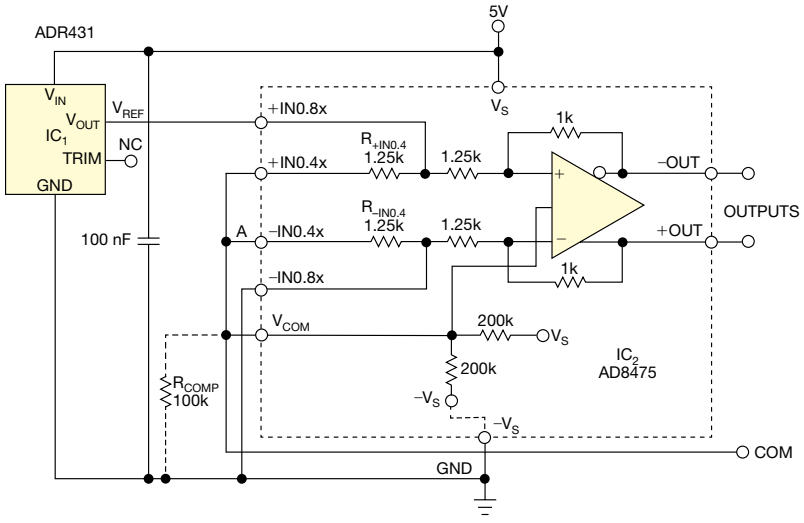

Figure 1 You can use this circuit to generate precision reference voltages of 1, –1, 1.25, and –1.25V.

TABLE 1 OUTPUT VOLTAGES AND VOLTAGE AT V_{COM} PIN

	Case A	Case B	Case C
Positive-output voltage (V)	2.2525	0.9981	0.9986
Negative-output voltage (V)	0.2525	–1.0019	–1.0011
Ground voltage (V)	–1.25	–1.2579	–1.2496
Common-mode voltage at V_{COM} pin (V)	1.239	0	0

REFERENCE

1 "AD8475 Precision, Selectable Gain, Fully Differential Funnel Amplifier," Analog Devices, http://bit.ly/gOtm7G.

Send MIDI signals over long distances

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The MIDI (Musical Instrument Digital Interface) protocol transfers digital control messages among synthesizers, audio equipment, and computers. A consortium of hardware and software manufacturers in 1983 developed the MIDI standard, which defines the use of microphone cables to link devices at a maximum distance of approximately 20m. That length may be insufficient for controlling distant devices. For example, in some venues, the equipment is on stage and you may want to send control messages from a remote mixing board.

The circuit in **figures 1** and **2** uses line drivers and receivers that let you transfer MIDI data signals over a common Category 5 LAN cable. MIDI data comes from the MIDI transmitter device and passes through optocoupler IC_1, conforming with the MIDI standard because it provides isolation between the devices.

Figure 1 You can test the completed MIDI drivers with a 100m Category 5 cross cable.

The MIDI signal then goes to the UA9638C line driver, which transforms

the data from a single-ended signal to a differential signal suitable for transmission over the Category 5 cable. The transmission passes through one of the pairs of a cross cable, reaching the UA9637C line receiver in an equal circuit on the other end. The signal then reformats to TTL (transistor-transistor-logic) level and travels through a MIDI output to reach a MIDI receiver device. LEDs D_2 and D_3 show the transmitter/receiver activity. Tests prove that this circuit can transfer messages over distances of more than 100m without losing data. EDN

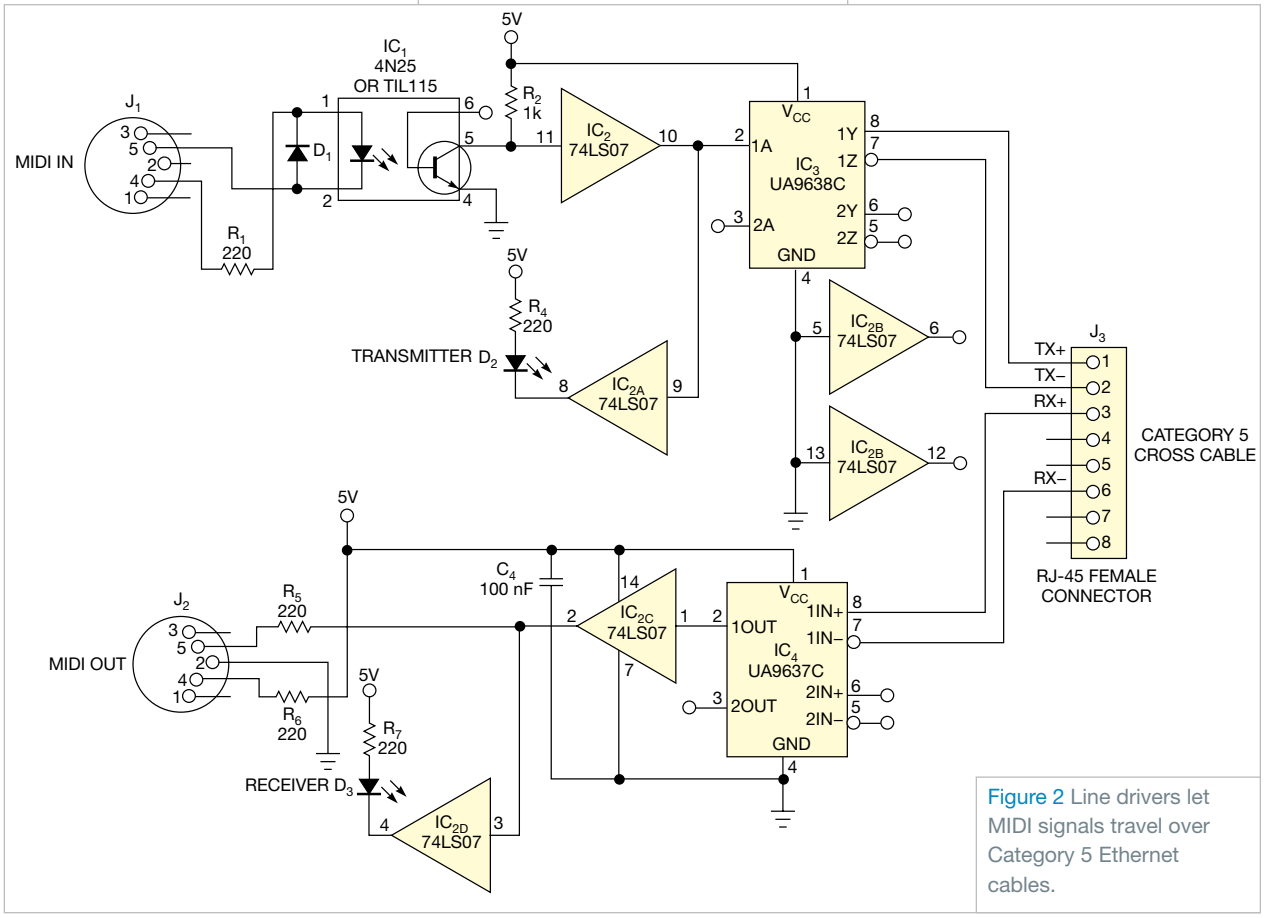

Figure 2 Line drivers let MIDI signals travel over Category 5 Ethernet cables.

MOSFET provides high power at low loss

Camilo Quintáns Graña and Jorge Marcos Acevedo, Vigo University, Vigo, Spain

PN-junction diodes often have a dropout voltage of approximately 1.2V for silicon power diodes. That voltage drop causes power diodes to dissipate considerable power, resulting in a loss of efficiency in a power supply. In a photovoltaic panel with 120W of power and 24V nominal voltage, an antireturn diode may cause a power loss of 6W, or 5% of the managed energy. Moreover, the cost of developing a cooling system for dissipating the heat diodes may pose a problem.

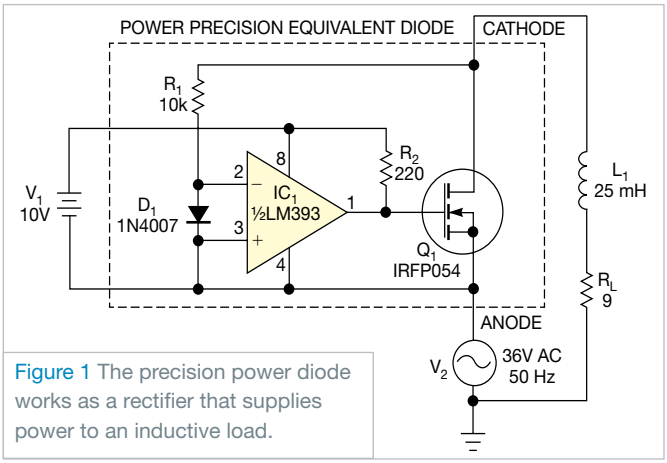

Figure 1 The precision power diode works as a rectifier that supplies power to an inductive load.

This Design Idea shows a more efficient approach that replaces a conventional power diode with a MOSFET transistor operating in on/off mode. **Figure 1** shows the rectifier circuit with a MOSFET transistor, Q_1, which has a low drain-to-source resistance in the

THIS APPROACH REPLACES A POWER DIODE WITH A MOSFET TRANSISTOR OPERATING IN ON/OFF MODE.

on state. In the circuit, V_2 represents an ac power source of 36V. The load comprises 9Ω resistor R_L and 25-mH coil L_1. Comparator IC_1 generates the gate voltage for Q_1 when the voltage-

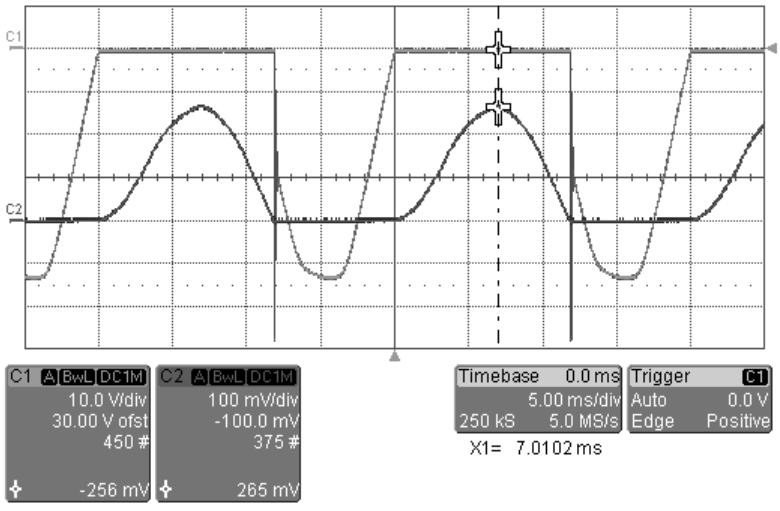

Figure 2 These traces show the rectifier's waveforms for an inductive load that comprises 9Ω resistor R_L and 25-mH coil L_1. Trace C2 shows a maximum load current of 2.65A. (The probe is 100 mV/A.) Trace C1 shows the anode-to-cathode voltage drop.

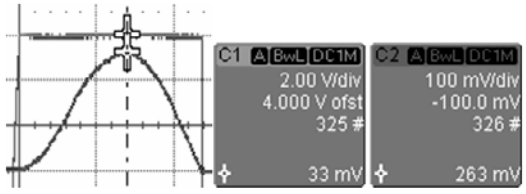

Figure 3 These traces show the condition of the rectifier with gate control. The MOSFET's parasitic diode is off, and the maximum voltage drop across the MOSFET is only 33 mV (Trace C1). Trace C2 shows the current through the rectifier.

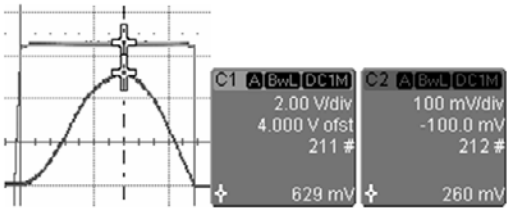

Figure 4 These traces show the condition of the rectifier without gate control. The MOSFET's parasitic diode is on, and the voltage drop across the MOSFET is 629 mV (Trace C1). Trace C2 shows the current through the rectifier.

supply anode is higher than the drain-voltage cathode. Thus, the source works as the anode of the rectifier, and the drain functions as a cathode. The circuit exploits the capability of the transistor in conducting currents in the source-to-drain direction. Turning on Q_1 effectively shorts its parasitic diode between the substrate and the drain, minimizing power loss. When the gate-to-source voltage is low, both Q_1 and its parasitic diode are off. Diode D_1 and resistor R_1 limit the voltage across the comparator inputs.

Figure 2 shows the load voltage and the voltage drop on rectifier Q_1. **Figure 3** shows the normal operation of the rectifier, in which, for a maximum load current of 2.65A, the voltage drop is 33 mV; Q_1 is working in the ohmic region. On the contrary, if you use the MOSFET, the voltage drop becomes 629 mV, yielding a maximum instantaneous power of 1.66W (**Figure 4**).

This approach is valid for any type of rectifier with any number of diodes. Moreover, you can use this circuit in dc/dc and dc/ac converters because, when you use power MOSFETs in bridge circuits, they can conduct both active and reactive currents. This approach avoids the need to use substrate-drain parasitic diodes in the MOSFET. EDN

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designideas

READERS SOLVE DESIGN PROBLEMS

Waveform generator minimizes amplitude dependency

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Engineers have long used function-generator circuits employing analog integrators and high-hysteresis comparators. The outputs of these circuits often depend on variations in temperature, power-supply voltage, load, and parts. However, you can pump new life into the classic triangular/rectangular-waveform generator using the circuit in **Figure 1**. This circuit uses a precision reference-voltage source and the diode network comprising IC_1, IC_2, and IC_6; dual analog SPDT (single-pole/double-throw) switch IC_3; integrator IC_4; and comparator IC_5. The result is a ramp- and square-wave generator that holds its output stable in the face of those variations. Comparator IC_5 uses a switching technique to achieve its stable high hysteresis. **References 1** and **2** provide more details, including how the Schottky-barrier diodes of IC_6 suppress charge injection.

The output of IC_5, an ADCMP601 comparator, is initially low, forcing the ADG736 analog switch, IC_3, to connect a positive reference voltage, V_{REF+}, to IC_5's inverting input. Simultaneously, the S_2 switch connects a negative reference voltage, V_{REF-}, to the integrator's R_1 resistor. As long as the comparator's output is low, the integrator's output, V_{INT}, increases linearly until it reaches V_{REF+}, the comparator's positive-threshold level. At that point, the output of the comparator changes to high, which turns on the B channels of both multiplexers as their A channels turn off.

When the switch positions change, the integrator integrates positive reference-voltage V_{REF+}, and V_{INT} decreases linearly until it reaches the negative threshold V_{REF-}, which the comparator sets. The cycle then repeats. A bipolar reference source comprising IC_1 and IC_2 creates V_{REF+} and V_{REF-}. This part

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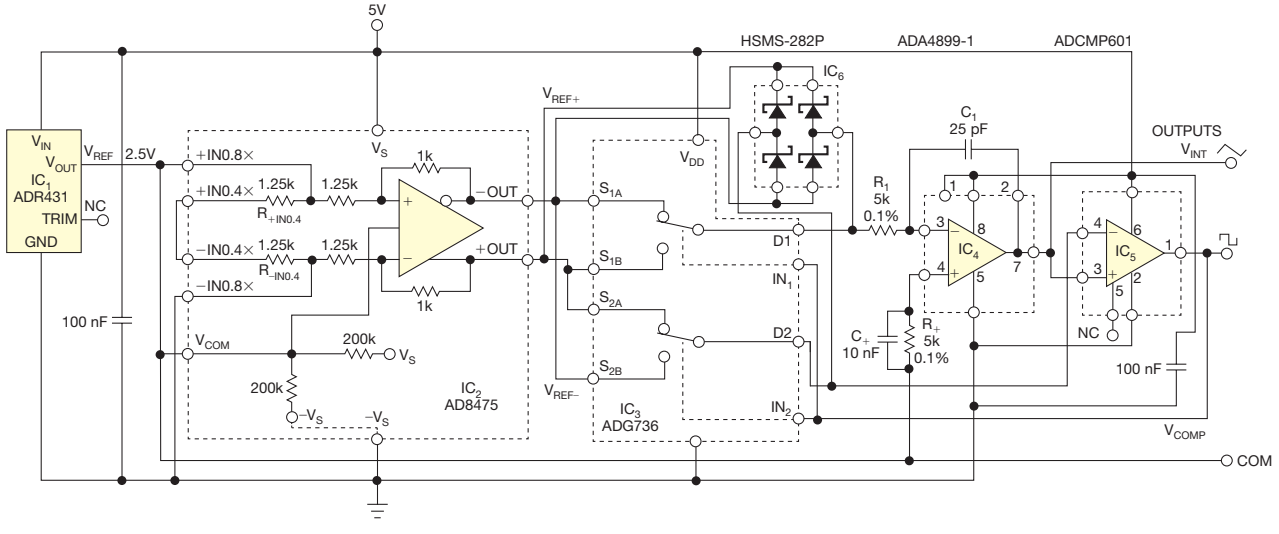


Figure 1 Creating hysteresis by switching precision reference voltages within the waveform generator ensures high insensitivity of the amplitude of triangular waveforms on supply-voltage variations.

of the circuit is a slight modification of the circuit in an earlier Design Idea (**Reference 3**).

As the ramp-up/ramp-down cycle repeats, the integrator produces a symmetrical, triangular waveform of V_{INT}, and a rectangular waveform, V_{COMP}, appears at the output of the comparator. The amplitude of V_{INT} is approximately $(V_{REF+}–V_{REF–})/2$. The duty cycle of the rectangular waveform is close to 50%. The thresholds of the comparator are independent of the output load, and you derive them from a precision source of reference voltages. Thus, the circuit has low sensitivity of the repetition frequency of its output to supply-voltage variations and to load variations. In a simplistic model of the generator, the amplitude of the triangular waveform at the output of the integrator no longer depends on variations of supply voltage.

Experimentally, increasing supply voltage V_S from 5.0365 to 5.437V increases the amplitude of the triangular waveform by 2.85 mV, representing 0.285% of full-scale. Under the same conditions, a classic triangular/rectangular-waveform generator typically shows an 8% increase in amplitude. Thus, this circuit reduces the dependence of amplitude on supply-voltage variation by a factor of about 28.

In testing this circuit, you can expect an output frequency of 1.366 MHz with a supply voltage of 5.0365V. When the supply voltage is 5.437V, the output frequency will be 1.368 MHz. The time constant sets the repetition rate. In this case, the repetition rate is one divided by four times the time constant for an ideal comparator and ideal switches. The comparator's propagation delay and the on/off times of the switches lower the repetition rate to lower than the ideal value. EDN

REFERENCES

1 Štofka, Marián, "Circuit uses two reference voltages to improve hysteresis accuracy," *EDN*, Jan 7, 2010, pg 43, http://bit.ly/g9GmAc.

2 Štofka, Marián, "Schottky diodes improve comparator's transient response," *EDN*, Jan 21, 2010, pg 32, http://bit.ly/el3N0d.

3 Štofka, Marián, "Build an accurate bipolar reference," *EDN*, May 12, 2011, pg 42, http://bit.ly/knjieC.

Produce current from positive or negative high-voltage supplies

Kurt Nell, Sankt Pölten, Austria

You sometimes need a current source for supply voltages as high as 1000V or more. This current source can be useful for ripple-voltage reduction when the current source's high-impedance node feeds an electrolytic capacitor to effectively short the ripple voltage. The circuit in **Figure 1** does the job with a temperature-stable and exact-output current. The circuit uses N-channel MOSFET Q_1, which has a drain-to-source voltage of 1000V. Zener diode D_2, a ZR431LF01 shunt regulator, stabilizes and regulates the output current. The threshold voltage of Q_1 must be higher than D_2's 1.25V reference voltage.

R_1 and the voltage across it determine the output current. In this case, 1.25V/220Ω=5.6 mA. D_2 regulates the MOSFET's gate-to-source voltage until the voltage across R_1 equals D_2's reference voltage, which is temperature stable and accurate, making the current source stable and accurate, as well. Zener diode D_1 protects Q_1's gate and limits the gate-to-source voltage if no load connects to the current source.

You can use a similar circuit to get constant current from negative high-voltage supplies even if a P-channel MOSFET with a high drain-to-source voltage is unavailable. To make the circuit work with negative supplies with an N-channel MOSFET, you must modify the circuit in **Figure 1**. You can use the N-channel MOSFET by changing the source and drain connections of MOSFET Q_1 in **Figure 2** (pg 55). The function of the current regulation with zener diode D_2 is the same as for positive voltages. EDN

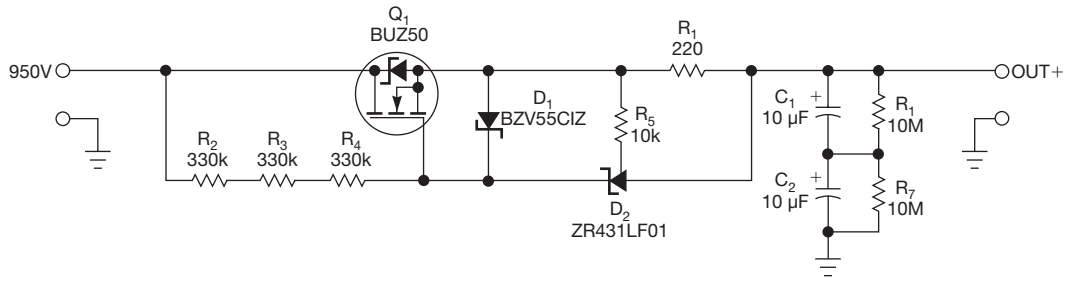
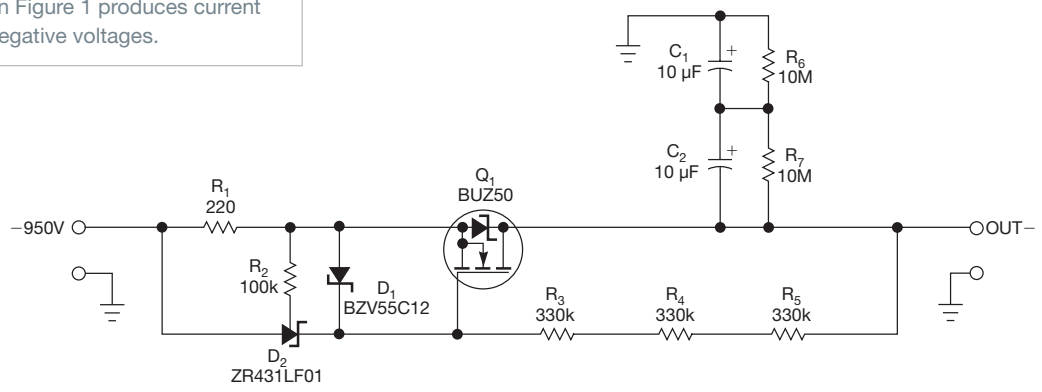


Figure 1 This circuit produces current using positive voltages.

Figure 2 This modified version of the circuit in Figure 1 produces current using negative voltages.



Arrange LEDs as seven-segment displays

Charaf Laissoub, Valeo Engine and Electrical Systems, Créteil, France

When you need to drive three seven-segment LED displays, you typically need 10 I/O lines—and that's without a decimal point. You might think that you cannot accomplish that task without a binary-to-seven-segment decoder or a serial-to-parallel shift register (**Reference 1**). Many previous Design Ideas have shown how to maximize the number of LEDs you drive with a minimum number of I/O lines (**references 2** through **5**). This Design Idea shows how you can build a circuit that drives 21 LEDs, thus forming three pseudo-seven-segment displays.

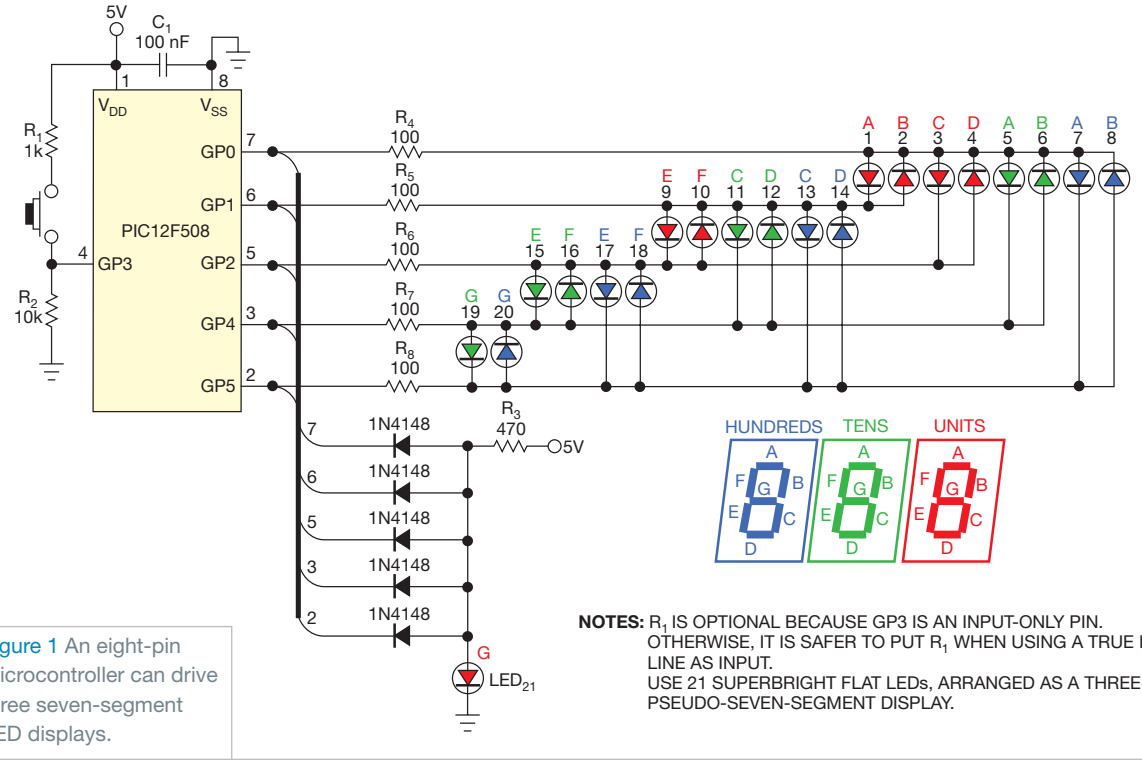


Figure 1 An eight-pin microcontroller can drive three seven-segment LED displays.

The circuit in **Figure 1** modifies the circuit in a previous Design Idea (**Reference 6**). It adds the 21st LED, but it modifies the assembler code to use just 98 words without the main routine. **Listing 1**, the assembler code, is available with the online version of this Design Idea at www.edn.com/110526dia. It can also suit any of a Microchip (www.microchip.com) baseline or midrange PIC microcontroller's eight pins.

THE CIRCUIT ADDS THE 21st LED, BUT IT MODIFIES THE ASSEMBLER CODE TO USE JUST 98 WORDS WITHOUT THE MAIN ROUTINE.

You can adapt this code for another type of microcontroller, such as those from Atmel (www.atmel.com) or STMicroelectronics (www.st.com), using the following steps:

1. Build a look-up table of 10 values for seven-segment coding (see **table** "Code7Segment" in **Listing 1**).

2. Build a look-up table of 3×7 values to store the successive configurations for I/O lines, each configuration containing only one high output and one low output to drive one LED at a time, for each digit (see **table** "Cfg2LinesOut" in **Listing 1**).

3. Build a look-up table of 3×7 values to store the successive high and low state for the I/O lines that are acting as outputs to light only one LED at a time for each digit (see **table** "Light1LED" in **Listing 1**).

4. The subroutine DispDigit rotates to the right seven times, through Carry flag, and the seven-segment code of a digit. It then calls the subroutine LEDon each time you set Carry.

5. The subroutine LEDon activates the LED related to the I/O configuration code, which you can extract from **table** "Cfg2LinesOut," and lights it according to the high or low state code, which you extract from **table** "Light1LED." The subroutine ends by a jump to a critical 1- to 3-msec delay subroutine. Increasing this delay increases the flicker effect, and decreasing this delay dims the LED.

6. Cycle digits of units, tens, and hundreds through steps 4 and 5.

For the PIC10F2xx series, which contains only three I/O lines, **Figure 2** shows an example of driving one digit, and **Listing 2** shows the corresponding assembler code. You can access **Listing 2** from the Web version of this Design Idea at www.edn.com/110526dia. EDN

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2 Raynus, Abel, "Squeeze extra outputs from a pin-limited microcontroller," *EDN*, Aug 4, 2005, pg 96, http://bit.ly/gX723N.

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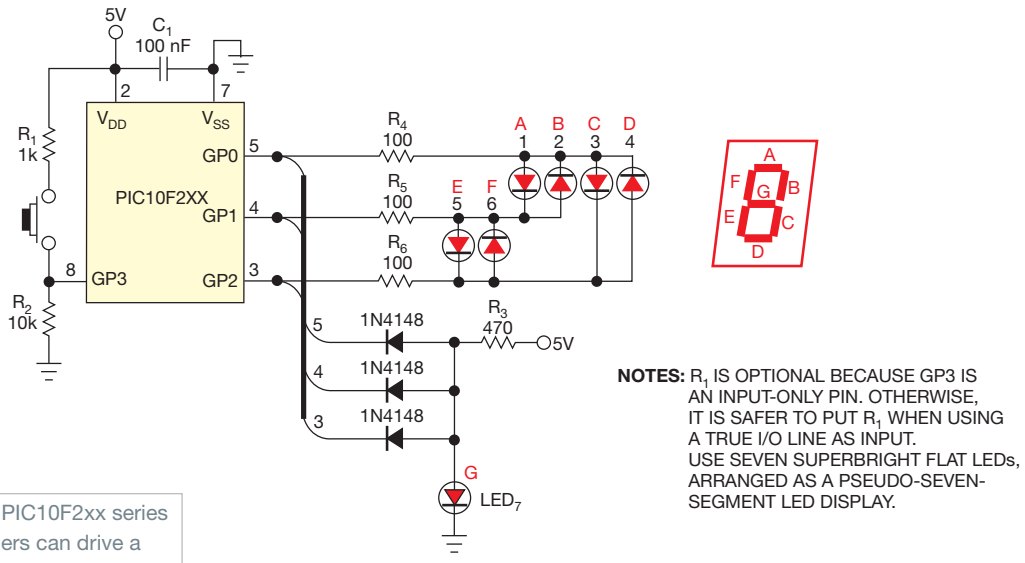
5 Gadre, Dhananjay V, and Anurag Chugh, "Microcontroller drives logarithmic/linear dot/bar 20-LED display," *EDN*, Jan 18, 2007, pg 83, http://bit.ly/hJCs3j.

6 Benabadji, Noureddine, "PIC microprocessor drives 20-LED dot- or bar-graph display," *EDN*, Sept 1, 2006, pg 71, http://bit.ly/g7ZIQY.



NOTES: R_1 IS OPTIONAL BECAUSE GP3 IS AN INPUT-ONLY PIN. OTHERWISE, IT IS SAFER TO PUT R_1 WHEN USING A TRUE I/O LINE AS INPUT. USE SEVEN SUPERBRIGHT FLAT LEDs, ARRANGED AS A PSEUDO-SEVEN-SEGMENT LED DISPLAY.

Figure 2 The PIC10F2xx series microcontrollers can drive a seven-segment display with three pins.

Logic gates form high-impedance voltmeter

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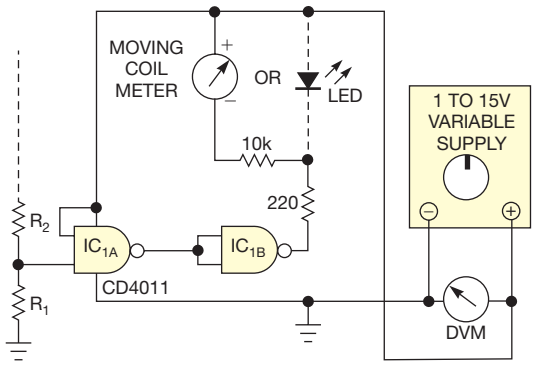
You can use the circuit described in this Design Idea to estimate voltages across 10- to 100-MΩ resistances. It also works for reverse-biased diodes.

The common CMOS gates in **Figure 1** have an input threshold voltage in which the output swings from logic zero to logic one, and vice versa. The threshold voltage depends on the supply voltage (**Figure 2**). Because of each CMOS gate's high input impedance, input currents are approximately 0.01 nA. If you apply 5V to 100 MΩ, you get 50 nA. Thus, you can connect the gate input at a point at which it draws a negligible amount of current.

You can vary the CMOS gate's supply voltage to attain the desired threshold voltage for the gate input. If you apply the unknown voltage to one of the gate's inputs and then connect the other input to the positive-voltage supply, you can vary the supply voltage, V_S, until you reach a point at which the threshold voltage at the input becomes equal to the unknown voltage.



NOTE: R_1 AND R_2 ARE IN TENS OR HUNDREDS OF MEGOHMS.

Figure 1 Use CMOS gates and a variable power supply to find an unknown voltage.

At this point, the output of the sense gate, IC_{1A}, changes from logic zero to logic one. When this event happens, the threshold of the gate passes the unknown voltage. You can estimate the unknown voltage using a graph of threshold voltage versus supply voltage,

ESTIMATE THE UNKNOWN VOLTAGE USING A GRAPH OF THRESHOLD VERSUS SUPPLY VOLTAGE.

such as the one in **Figure 2**. By fitting a parabola or a polynomial to the experimentally obtained points—say, some 20 points lying in the supply-voltage range of 2 to 15V—you can estimate the threshold voltage, V_T, for any supply voltage. This circuit has been built and tested. The online version of this Design Idea includes Octave/Matlab code that you can view at www.edn.com/110526dib. EDN

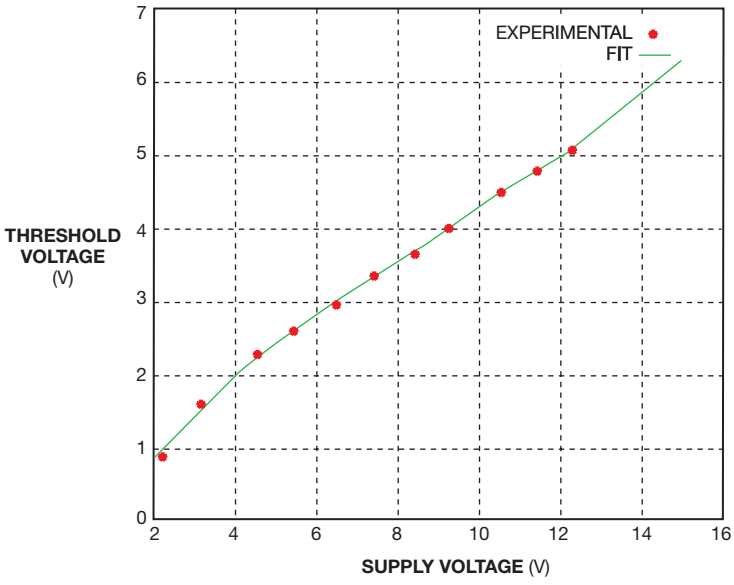


Figure 2 The gate's threshold voltage is nearly linear with respect to the power-supply voltage. You can download this plot at www.edn.com/110526dib.

Measure resistance and temperature with a sound card

Zoltan Gingl and Peter Kocsis, University of Szeged, Szeged, Hungary

Unless you add a measurement instrument to your computer, you have only the sound card as an analog I/O port. You can use the sound card to digitize ac analog voltages but only within a limited range. You can, however, add some signal processing and measure a wider variety of signals, even those that produce dc or low-frequency outputs. For example, you can directly connect a thermistor to make a sound-card thermometer to monitor or record the temperature on PCBs (printed-circuit boards), circuits, heat sinks, and more.

Thermistors are popular temperature sensors because they allow easy detection of changes in resistance. Once you measure a thermistor's resistance, you can apply the following **equation** to find the temperature:

$$T = \frac{1}{\frac{1}{T_O} + \frac{1}{\beta}\ln\left(\frac{R_T}{R_O}\right)},$$

where R_T is the thermistor resistance and T_O is the temperature in Kelvins at which the thermistor's resistance is R_O. You can find the value of β in a thermistor's data sheet.

Figure 1 shows the easiest way to interface a thermistor to a sound card. The microphone input has an internal bias resistor, R, with a typical value of 2 to 5 kΩ. A dc bias voltage drives this resistor. The bias resistor connects the thermistor between the line or the headphone output and the microphone input, which forms a voltage divider with the internal bias resistor. Those components are all the circuit needs. Note that some microphone inputs may have different internal connections, so check yours before use.

You also need a sinusoidal signal because the sound card's inputs are ac-coupled. The sound card's audio output can produce an ac voltage at the microphone input, whose amplitude is proportional to $R/(R+R_T)$. You can do a simple calibration to find the output signal's amplitude and the value of R by replacing R_T with known values, such as 0 and 10 kΩ.

A sound card's measurement accuracy is worse than what you could achieve using a commercial data-acquisition card, but this ratiometric arrangement and calibration keep errors to approximately 1% for resistor values of 1 to 100 kΩ. Even without

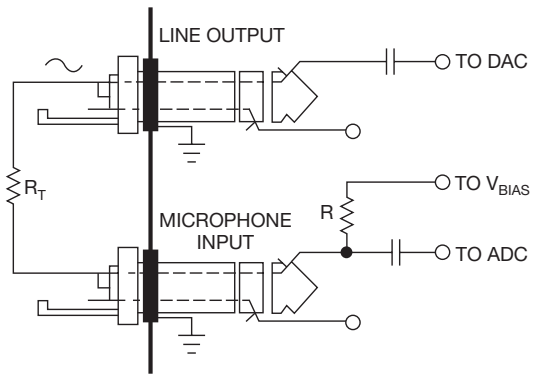


Figure 1 The internal microphone bias resistor and the externally connected thermistor form a voltage divider.

temperature calibration, you should get temperature errors of 1 to 2K with a 10-kΩ thermistor at room temperature. Accuracy degrades to 3 to 5K over the thermistor's operating temperature.

You can download simple, free, and open-source software in Java that you can use as a simple ohmmeter, thermometer, or chart recorder under Windows or Linux. You can download a Java executable or the Java source code (**Reference 1**).

You should consider adding protection to the sound card's audio I/O ports by inserting series resistors. Typically, a few kilohms is all the circuit needs. You can also use an inexpensive USB (Universal Serial Bus) sound card to spare and protect your PC sound card's inputs.

You can add second and third thermistors to your system by adding an external resistor divider (**Figure 2**). This approach lets you use both audio channels and a third thermistor at the microphone input. In addition to using thermistors, you can use the sound card with other resistive sensors, such as photoresistors or potentiometric displacement sensors. You can even connect capacitive sensors if you add some more components and signal processing (**Reference 2**). EDN

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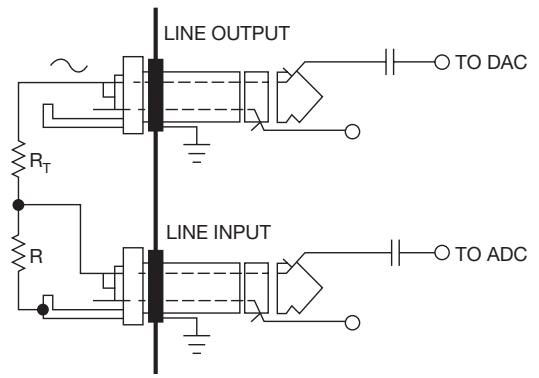

Figure 2 You can add second and third thermistors to your system by adding an external resistor divider.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Potentiometer calibrates photodiode amplifier

Michael J Gambuzza, General Electric Energy, Billerica, MA

One of the nagging problems with optocouplers is that their light output varies with temperature, age, and CTR (current-transfer ratio). Thus, you may need to calibrate optocouplers to compensate for those variations. Using the circuit in **Figure 1**, you can calibrate an optocoupler's output using an up/down digital potentiometer. The amplifier circuit, a typical photovoltaic-mode device, uses IC_3, an Analog Devices (www.analog.com) AD5227 up/down potentiometer, which has 64 steps and powers up at midscale resistance. When a microcontroller output pin or another digital signal selects the device, the device's resistance changes with every clock pulse until the output voltage of the amplifier equals the maximum set reference voltage. The completion of the calibration cycle optimizes the amplifier's output for the optocoupler's CTR.

Driving the optocoupler's LED at a maximum dc current for a full-scale amplifier output puts the incident light at a maximum level. The circuit then asserts the calibration pulse for a time that depends on the AD5227's external clock rate. If the output of the amplifier is lower than the maximum reference

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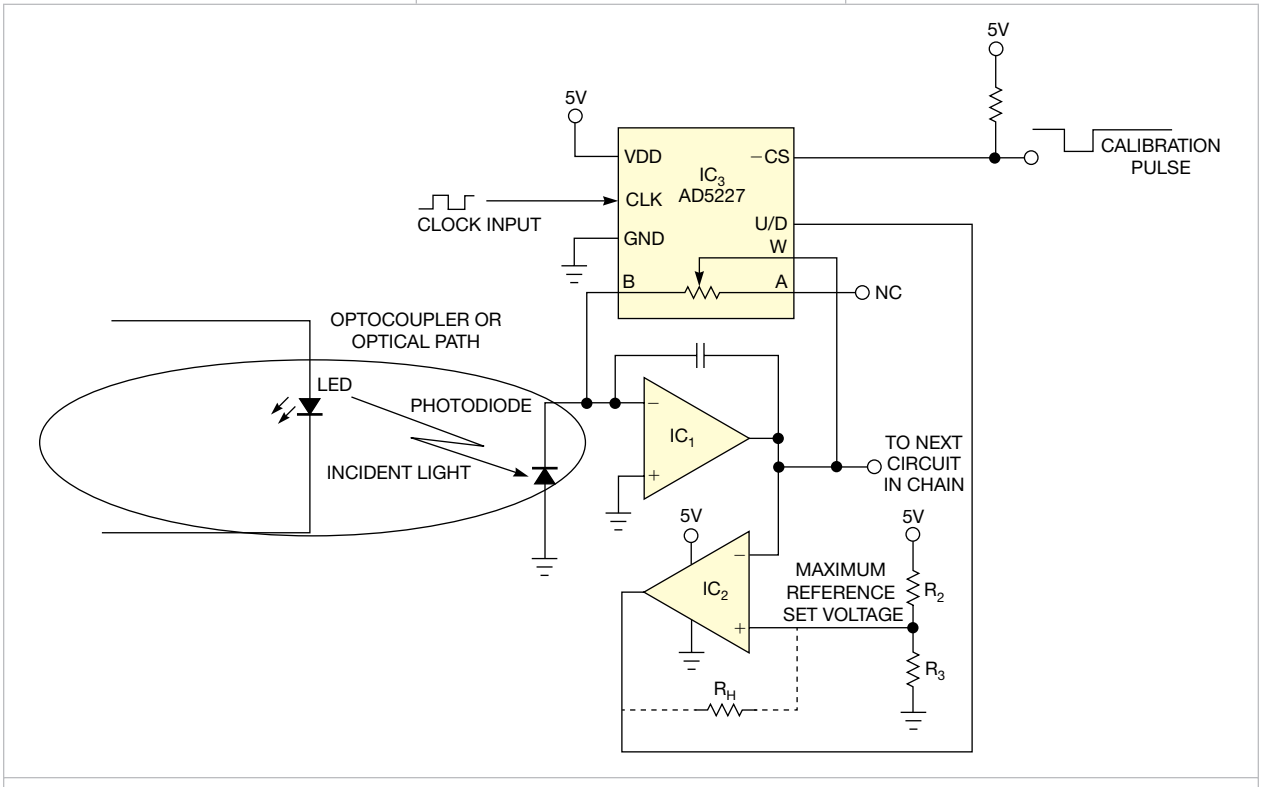

Figure 1 This circuit lets you calibrate an optocoupler's output using an up/down digital potentiometer.

voltage, IC_2's output goes high. This action increases the resistance from Pin W to Pin B, increasing the amplifier's gain. If the output of the amplifier is higher than the reference, IC_2's output goes low, causing the AD5227 to decrement the resistance, which reduces the gain.

For IC_2, use a comparator with built-in hysteresis or use external hysteresis, which resistor R_H provides. You can use this method for other applications besides optocouplers; for example, you can also apply it to lasers. Photoamplifier designs can be tricky, so make sure to carefully craft your amplifier's compensation, layout, and power-supply decoupling. EDN

Drive 16 LEDs with one I/O line

Zoran Mijanovic and Nedjeljko Lekic,
University of Montenegro, Podgorica, Montenegro

Over the last few years, several Design Ideas have described how to use just a few microcontroller I/O pins to drive many LEDs (**references 1** through **7**). The circuit in **Figure 1** can drive 16 LEDs with just one pin and two shift registers. You can use the circuit to drive long-dot-bar or two seven-segment-digit displays. Adding multiplexing to the same circuit enables it to drive eight seven-segment LED digits.

The microcontroller drives the shift registers' clock inputs. That signal also passes through an RC filter and drives data inputs A and B. A 100-kΩ resistor, R, and the A and B input pins' capacitances form the RC filter (**Figure 2**), producing time delay of approximately R×C×ln2=100 kΩ×(5 pF+5 pF) ×0.7=0.7 µsec.

To write a logic zero to the shift register, the microcontroller holds a low level for approximately 2 µsec, which is longer than the time delay. It then sets the signal to a logic one, or high, level. To write a logic one, the microcontroller holds the high level for longer than the time delay. The microcontroller then makes negative pulses of approximately 0.25 µsec, or two CPU cycles, which is shorter than the time delay and which doesn't change the logic level at the data inputs.

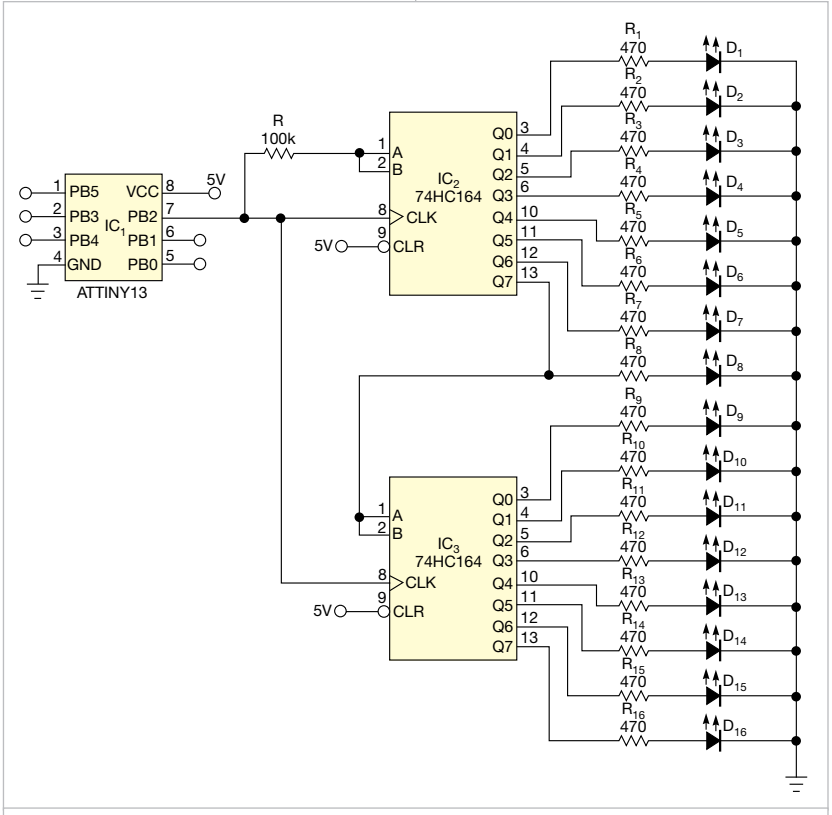

Figure 1 A 16-LED dot-bar/bar-graph display uses two 8-bit serial-input/parallel-output shift registers.

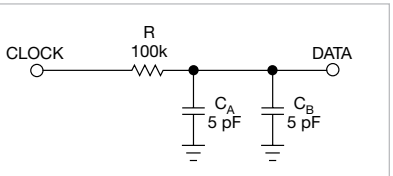

Figure 2 An RC filter provides a 0.7-µsec delay.

Figure 3 shows the clock signal in Channel 1 (yellow) and the data signal in Channel 2 (blue). The oscilloscope is a Tektronix (www.tektronix.com) DPO4034 with TPP0850 high-voltage probes. These probes have 40-MΩ input resistance and only 1.5-pF input capacitance, minimizing distortion.

A rising edge on the clock signal clocks the shift registers. This edge corresponds to the data signal's local minimum. **Figure 3** also shows that the minimum data-signal voltages for logic zero and logic one are 1.3 and 3.1V, respectively. The shift register's logical threshold is 2.5V. These voltages guarantee sufficient voltage margins. If your design requires higher margins, vary the signal timing and use a higher resistance for R in **Figure 1**. This circuit stores 16 bits in shift registers in approximately 35 µsec.

You can view a short video of the circuit in operation and download a code listing, in C, at the online version of this Design Idea at www.edn.com/110609dia. The software turns on

the LEDs one by one every 500 msec until all LEDs are on. It then turns off all the LEDs and repeats the cycle. EDN

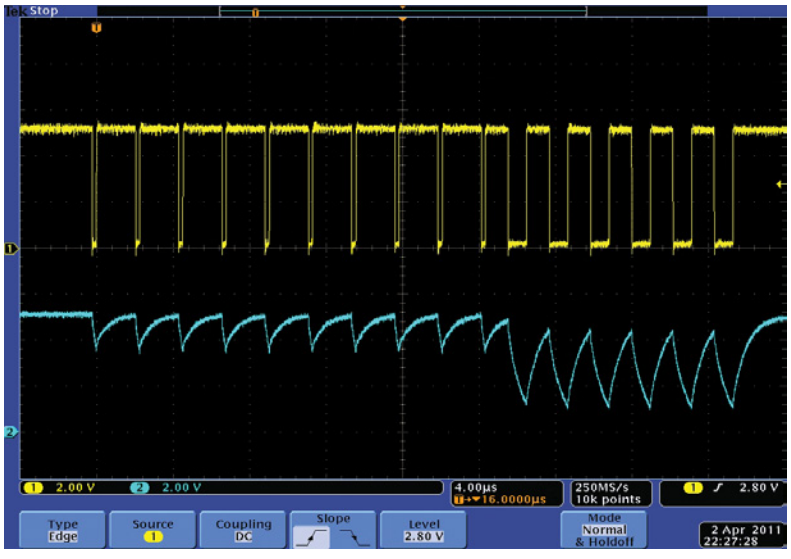

Figure 3 The waveform shows the circuit writing the pattern 1111111111000000 for the display. The upper, yellow trace is the clock signal, and the lower, blue trace is the data signal.

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Circuit measures battery capacity

Vladimir Oleynik, Moscow, Russia

Batteries and energy cells lose their capacity as they age. If a cell or battery's capacity is too low, your equipment may also soon stop working. You can use the circuit in **Figure 1** to measure a battery's discharge time. The circuit uses an electromechanical clock and a DVM (digital voltmeter). The cell should be fully charged before testing. The circuit discharges the cell at a fixed current and measures the time it takes to discharge the cell from 100 to 0%.

For example, if a manufacturer rates a cell's capacity and you discharge the cell at a constant current equal to 0.1 times the capacity, the cell should take about 10 hours to discharge from full to empty. Manufacturers of NiCd (nickel-cadmium) or NiMH (nickel-metal-hydride) cells rate the end of the discharge voltage at 1V. At that point, the cell is using 0% of its capacity, is flat, and requires charging for further operation. If this procedure takes less than 10 hours, the cell's capacity is less than what the cell manufacturer rates.

Before testing the cell, charge it to full capacity using your charger. Apply 12V dc to the circuit and use potentiometer P_2 to set a voltage of 1V at Pin 6 of IC_{1B}. Set the clock to 12:00. An AA-size, 1.5V cell powers the clock through relay switch S_3.

When you press the momentary pushbutton switch, S_1, the tested cell starts to discharge through transistor Q_1 and resistor R_1. Set the discharge current using potentiometer P_1. Op amp IC_{1A} keeps the voltage across resistor R_1 constant, thus providing stable cell-discharge current. Set the DVM to measure the dc voltage and measure the voltage across R_1. The display shows discharge current in amperes. For example, 0.25V corresponds to 0.25A. Because the initial cell voltage is higher than 1V, Pin 7 of op amp IC_{1B} is high, transistor Q_2 is on, and the DPST (double-pole/single-throw) relay coil is active. Relay-contact switch S_2 closes and bypasses the start pushbutton switch, S_1, which keeps the discharge process active. Closed relay-contact switch S_3 lets the clock keep time.

When the cell's voltage is equal to the end-of-discharge value, 1V, IC_{1B}'s output goes low and deactivates the relay coil, halting the discharge process. The clock also stops. To get the cell's capacity, multiply the set discharge-current value by the elapsed time. If the discharge-current value is small and the time necessary for the discharge of a cell is longer than 12 hours, you must check this value every 12 hours after you start the test and keep in mind laps of one to 12 hours.

This circuit also lets you estimate the self-discharge rate of the cell or battery you use. Charge your cell to 100% of its capacity and measure cell capacity

according to this procedure. Charge your cell again, store it for a month, and then measure the cell capacity again. The difference between the two values is the monthly self-discharge rate.

If you arrange the cells in a stack, you should provide a reference voltage that's higher than the battery's end-of-discharge voltage. If the battery voltage is higher than 12V, use a higher-voltage value to power the circuit. Furthermore, the reference voltage value should be higher than the battery's end-of-discharge value. Specifications of the discharge path comprising transistor Q_1 and resistor R_1 should fit higher discharge-current requirements.

The circuit works with cells or batteries of any chemistry, including NiCd, NiMH, lead acid, and lithium-ion. You can also use this circuit to measure the real capacity of nonrechargeable cells, such as AA alkaline cells. In that case, the discharged cell's voltage should be equal to the lowest power-supply voltage of your device. A cell that has passed the test is not suitable for further use, but you can use its capacity information to estimate the capacity of the batteries of the same type and manufacturer. EDN

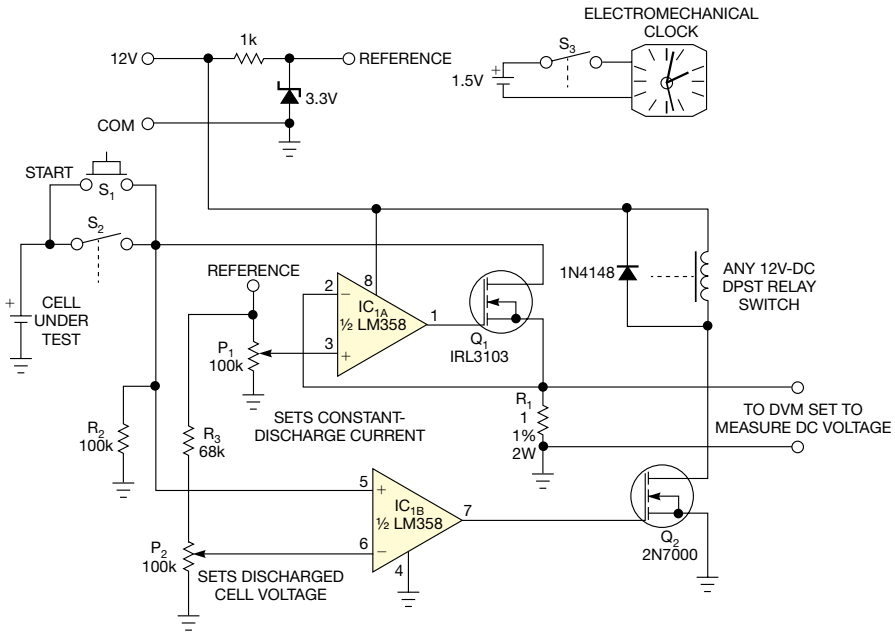

Figure 1 An electromechanical clock indicates a battery's discharge time.

Programmable driver targets piezoelectric actuators

P Saxena, VK Dubey, IJ Singh, and HS Vora, Raja Ramanna Centre for Advanced Technology, Indore, India

Motors using piezoelectric screws and linear/stack piezoelectric actuators make good choices for precise positioning (**Reference 1**). These motors typically use feedback control for applications such as optical mounts in wavelength scanning and in cavity-length stabilization. The motors are smaller than stepper motors, are lightweight and efficient, and provide fine resolution. Unfortunately, they need complex driver circuits with programmable waveshapes.

Commercially available OEM driver circuits may suffer from EMI (electromagnetic-interference)-immunity problems or can cost approximately $500. The circuit in

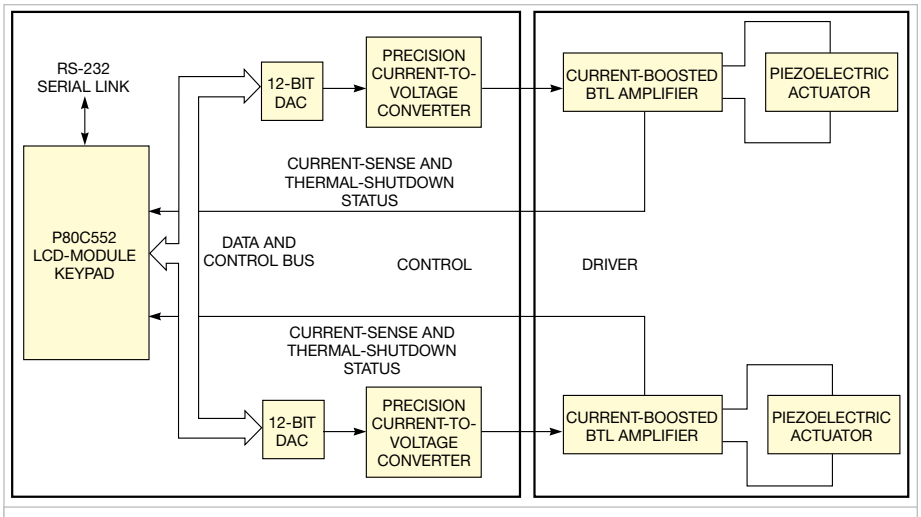

Figure 1 The controller comprises a microcontroller and a BTL-driver unit.

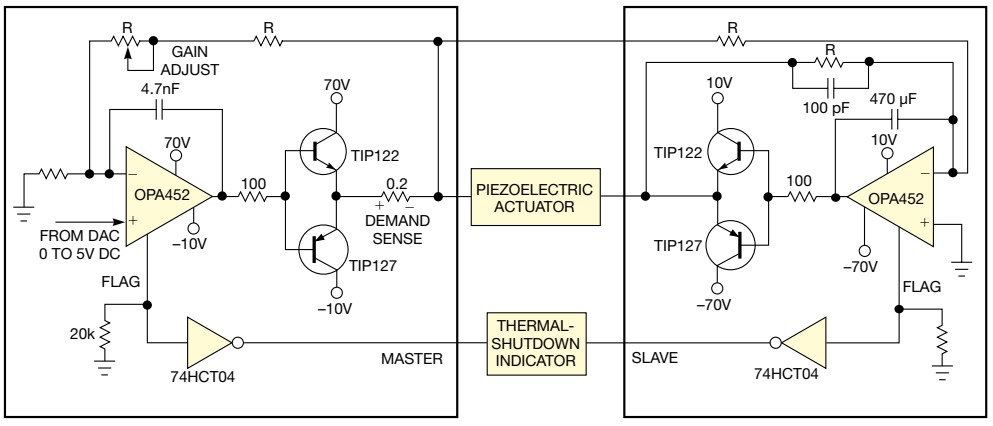

Figure 2 The circuit comprises a pair of low-cost OPA452 power op amps, which act as the BTL and drive the screw-type piezoelectric actuator.

this Design Idea presents a low-cost, microcontroller-based, multiaxis programmable driver for piezoelectric actuators.

Piezoelectric actuators often receive their power from unipolar drivers, which have slow slew rates. In this design, a microcontroller powers a universal BTL (bridge-tied-load) power amplifier. A BTL configuration doubles the slew rate, which is important in piezoelectric-drive applications. The microcontroller generates the pulse shape necessary for the forward and backward movements of actuators at a selectable speed of 0.1 Hz to 1.5 kHz. For interfacing two motors to run simultaneously, you can program synchronized speeds in an integer ratio of 1-to-N.

The circuit in **Figure 1** comprises a microcontroller and a BTL-configured driver unit. The P80C552 microcontroller uses two numbers of the 12-bit DACs, which have a conversion time of 2 µsec. These DACs directly connect to ports P3 and P4 of the microcontroller for fast response. Using this configuration, you can generate programmable waveshapes. Screw-based piezoelectric actuators need a waveshape with a rise time of approximately 110 µsec and a fall time of approximately 12 µsec to move clockwise and a mirror of it for counterclockwise motion. Software in 8051 assembly language can generate the waveforms for these motions. Using slow ramps, the system can control a linear piezoelectric actuator.

You can use the front-panel LCD and keypad to select the operations for setting the speeds, the motors, and the direction, or you can remotely set them using an RS-232 interface. You must make sure that on/off transients don't cause motor motion.

The heart of the design is a precision power driver. You can model the device using one capacitor with an impedance of $1/\omega C$. Current rises with frequency when a periodic voltage source has a frequency lower than the actuator's resonant frequency. The BTL is an output configuration for power amplifiers in which the load—the actuator—connects between two amplifiers, bridging the output terminals. This action makes the voltage swing at the load twice that of single-ended amplifiers with the outputs driven in opposite phases.

Figure 2 shows a pair of low-cost OPA452 power op amps, which act as the BTL and drive the screw-type piezoelectric actuator, which receives its asymmetric power supplies at ±70 and ±10V. This configuration delivers an output swing of 140V with a slew rate that is twice that of a unipolar device. Internal diodes comprising Darlington transistors offer flyback protection. Connecting the ultrafast diodes from the output to their corresponding power-supply rails can also protect each amplifier. To enhance the output current at as much as 1A, use external transistors in complementary symmetry mode.

WHEN OPERATING IN STATIC MODE, THE CIRCUIT IN ITS DRIVING VOLTAGE HAS A RIPPLE OF LESS THAN 20 mV. IT ACHIEVES FULL-SCALE OUTPUT-VOLTAGE POSITIONAL ACCURACY.

The circuit in **Figure 2** is valid for both static and ac operation. Static operation requires low current, and, for ac operation, the current is proportional to the rate of change of the driving voltage. In this case, the driver can supply a peak current of as much as 1A. When operating in static mode, the circuit in its driving voltage has a ripple of less than 20 mV. It achieves good full-scale output-voltage positional accuracy. A 100Ω resistance limits the current through the OPA452.

The system's full-power bandwidth is 3.5 kHz, and it provides thermal-shutdown and current-limiting features.

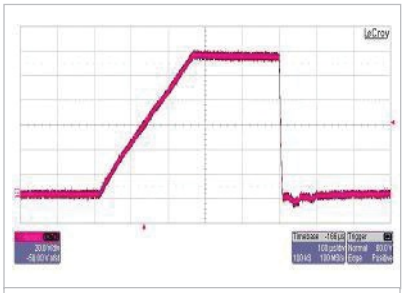

Figure 3 An oscilloscope shows the driver circuit's slow rise time and fast fall time.

Figure 3 shows the driver output of the system as tested with a piezoelectric screw. This pulse shape with slow rise time and fast fall time moves the piezoelectric screw clockwise. It has a differential output of 122V with a proportional gain of 24. Testing the driver with picomotors and linear actuators shows a step size of 30 nm/pulse and linear movement of 50 nm/V, respectively.

The drive can synchronize the etalon, and the tuning mirror handles hop-free tuning of a narrow-bandwidth dye laser. In a single-axial-mode dye-laser setup, the circuit can obtain approximately 25-GHz hop-free mode tuning by synchronizing the movement of the tuning mirror angle and etalon tilt. EDN

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Circuit boosts voltage to piezoelectric transducers

Kurt Nell, Sankt Pölten, Austria

Piezoelectric transducers are common in ultrasonic and acoustic-alarm-signaling applications. To get enough acoustic power from a piezoelectric transducer, you must power the device with a frequency at or near its resonant frequency. Furthermore, the driving voltage should be as high as the transducer allows.

A transformer circuit drives the transformer and the transducer at resonant frequency. You must usually build and optimize these transformers for the transducer you are using—a time-consuming job. You can, however, drive the piezoelectric transducer without the transformer using the circuit in **Figure 1**.

The circuit includes an oscillator using Schmitt trigger IC_{1A}. The frequency depends on resistor R_1 and capacitor C_1. You must select both components to fit the oscillator frequency with the resonant frequency of the piezoelectric transducer. You can replace R_1 with a variable resistor and change the value to maximize the voltage on the transducer.

The driver includes the five additional inverters of IC_1, IC_{1B} through IC_{1F}. A voltage tripler comprises diodes D_1 and D_2 and the surrounding components. The amplifier comprises Q_2, and the piezoelectric driver comprises Q_1 and Q_2.

Diodes D_1 and D_2 come in one BAS40-04 package. Alternatively, you can use double transistors for Q_1, Q_2, and Q_3. You can replace the oscillator with a microcontroller if you have one available. The circuit works with supply voltages of less than 10V. You can use it in 3.3V systems, but you should then use a 74HC14 inverter for the oscillator and the driver. You can also use additional voltage-doubler stages to get even more driving voltage for the transducer. EDN

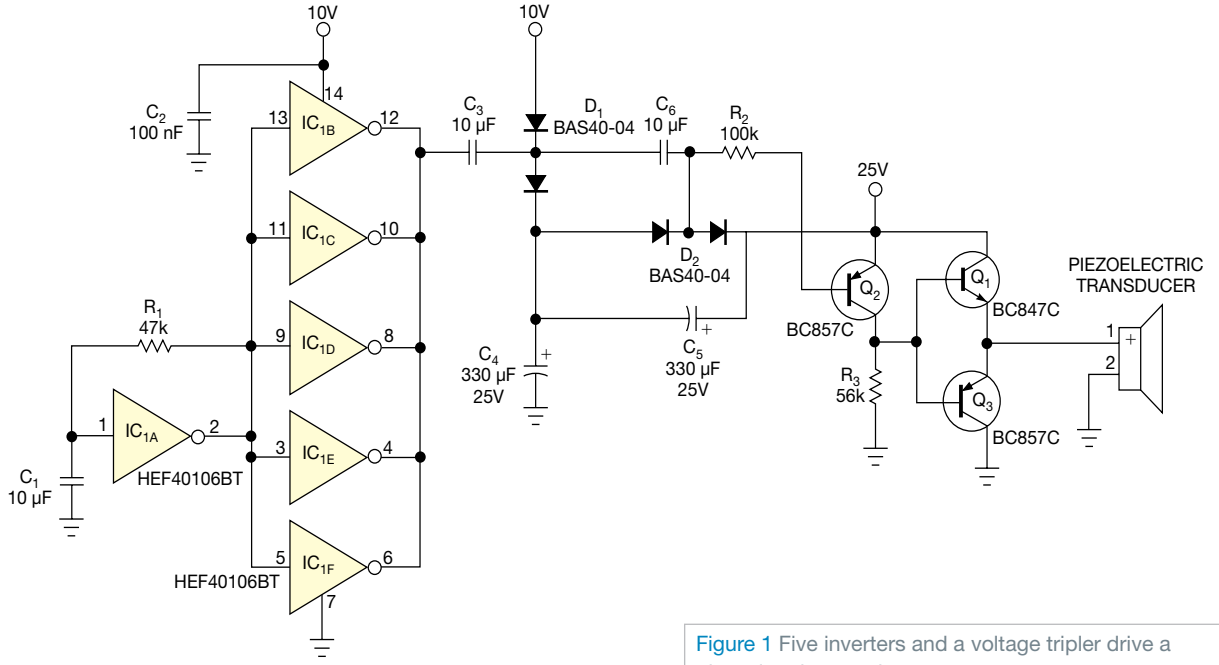

Figure 1 Five inverters and a voltage tripler drive a piezoelectric transducer.

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READERS SOLVE DESIGN PROBLEMS

Protect power-LED strings from overcurrent

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

A common method for driving multiple power LEDs is through two parallel strings. This inexpensive and less critical driver circuit can provide a lower voltage. However, the driver circuit must deliver twice the current of other methods and needs a circuit that halves the current in the two strings, regardless of the LEDs' forward voltages. The LEDs' forward-voltage tolerance is as high as 20%, and the voltages change with LED temperature and aging.

A current mirror performs this task well. If an LED breaks, it can cause destructive overcurrent. The current mirror, however, can safely partially protect two parallel, connected strings of any number of 350-mA power LEDs from these overcurrents (**Figure 1**).

The circuit can balance the currents between strings with a matching error of approximately 2% because of the equal voltages of 0.5V developed on 1.5Ω emitter resistors R_1 and R_2 with 1% tolerance. The voltage drop across resistor R_3 compensates for the mismatching of LED voltage drops and holds both Q_1 and Q_2 in the linear region. The voltage drop depends on how many LEDs make up the two strings.

If an LED of String 2 fails, however, no base current flows to transistors Q_1 and Q_2, and they turn off. All LEDs in String 1 have automatic overcurrent protection. The circuit doesn't perform the same function if an LED in String

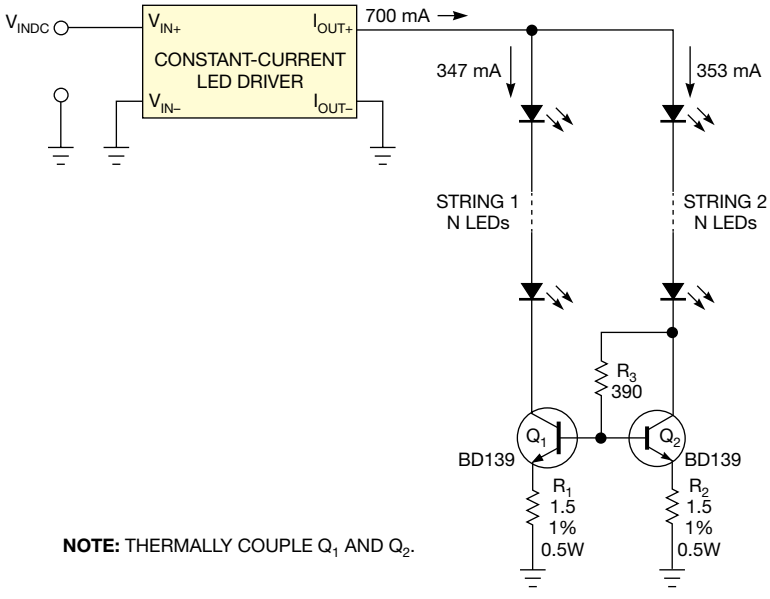

Figure 1 Using a current mirror, you can safely protect two parallel, connected strings of any number of 350-mA power LEDs from destructive overcurrents.

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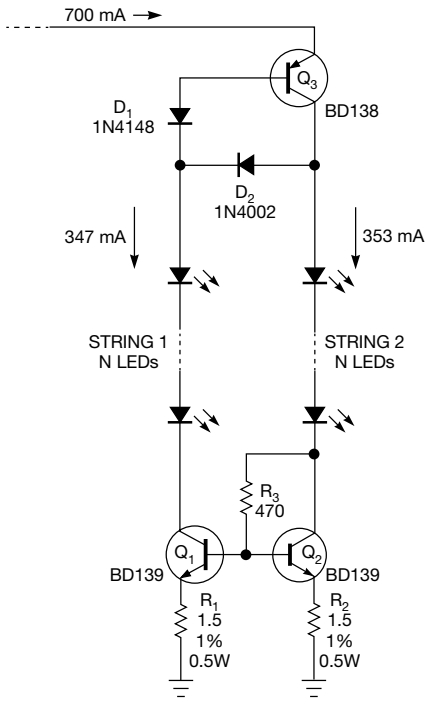

Figure 2 An LED in String 1 can fail because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components.

1 fails because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components (**Figure 2**).

In normal operation, transistor Q_3 operates in its linear region with an emitter-collector voltage of 0.7V because both diodes D_1 and D_2 are forward-biased. The power dissipation of Q_3 is only about 0.5W, and it thus needs no heat sink. The 700-mA driver current coming from the collector of Q_3 divides equally between the strings through steering diode D_2, as the current mirror dictates. If an LED in String 1 fails, diode D_2 blocks the base current of Q_3, turning it off. The driver current can no longer flow through String 2, safeguarding the LEDs.

You must compensate for diode D_2's 0.7V voltage drop, which slightly increases the value of resistor R_3. You can adapt the current mirror for driving any type of LED without exceeding the absolute maximum rating of the transistors' collector current, which is 1.5A. You can test the current mirror with any 700-mA constant-current LED driver, or even a voltage regulator configured as a current source, such as National Semiconductor's (www.national.com) LM317 regulator. The circuit underwent testing, with the LM317 acting as a 700-mA current source with five LEDs per string. EDN

Simple flasher operates off ac mains

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

Looking for a mains switch in the dark is easier if the switch contains a built-in neon or filament miniature lamp. Adding a small indicator to any mains switch is helpful. It is even better if the indicator flashes. This circuit makes a simple flasher using only four discrete components (**Figure 1**).

The neon lamp flashes at a frequency of 1 to 5 Hz, according to experimental values for resistance and capacitance. When the switch terminals are open, diode D_1 acts as a half-wave rectifier. Capacitor C_1 charges through resistor R_1 until the voltage on the capacitor exceeds the breakdown voltage of a miniature neon lamp. C_1 then discharges rapidly through the lamp, which flashes. You can access the switch terminals by prying off the front panel with a small screwdriver. This circuit can be installed inside the switch block. You assemble it on a 5×10-mm PCB (printed-circuit board).

This flasher circuit works properly only with 220V tungsten lamps. To use it with 220V fluorescent lamps, you must make a small modification (**Figure 2**). Disconnect resistor R_1 from the flasher circuit and place it in parallel with the starter of the fluorescent lamp, which is connected in series with the mains switch. EDN

THIS CIRCUIT MAKES A SIMPLE FLASHER USING ONLY FOUR DISCRETE COMPONENTS.

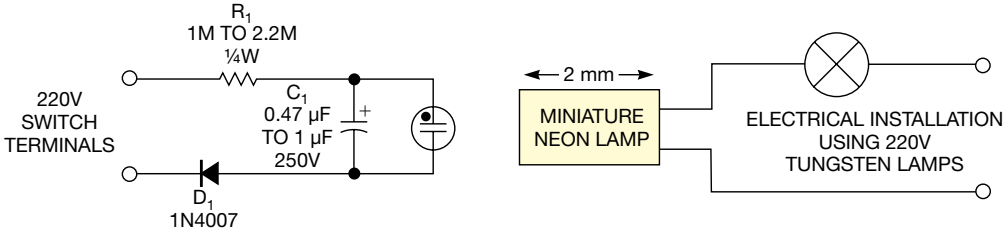

Figure 1 You can add this simple flasher inside a mains switch.

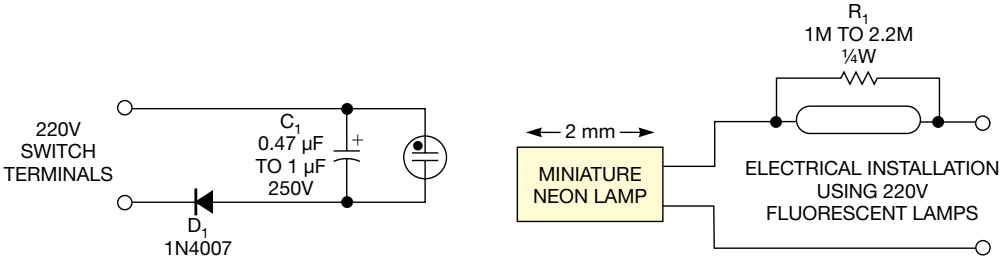

Figure 2 Use this modified circuit to operate with fluorescent lamps.

Use resistor noise to characterize a low-noise amplifier

Joe Geller, Whitesboro, NY

If you know or can estimate a low-noise amplifier's gain or noise bandwidth, you can measure the other spec using only a handful of resistors and an ac voltmeter (**Reference 1**). The method in this Design Idea uses the Johnson Equation, which describes the amount of noise a resistor generates (**Reference 2**). To find the missing parameter, measure an amplifier's output-noise voltage, first for a shorted input and then using a few resistors of different values. You can download an Excel spreadsheet that can calculate gain or noise bandwidth from the online version of this Design Idea at www.edn.com/110623dia.

To begin the measurement, place a short circuit across the low-noise amp's input terminals and measure the noise voltage with the voltmeter. Next, insert the resistors, one at a time, across the amplifier's inputs and measure the noise voltage at the output of the amplifier. Enter the measured output-noise voltages, the measured values of each resistor's resistance, the ambient temperature, and either the known or the estimated gain of the low-noise amp or the known or estimated effective noise bandwidth into the spreadsheet.

Using each of the measured resistance values, the spreadsheet plots a theoretical "blue" curve representing the Johnson noise in normalized units of nV/√Hz (**Figure 1**). You can compensate

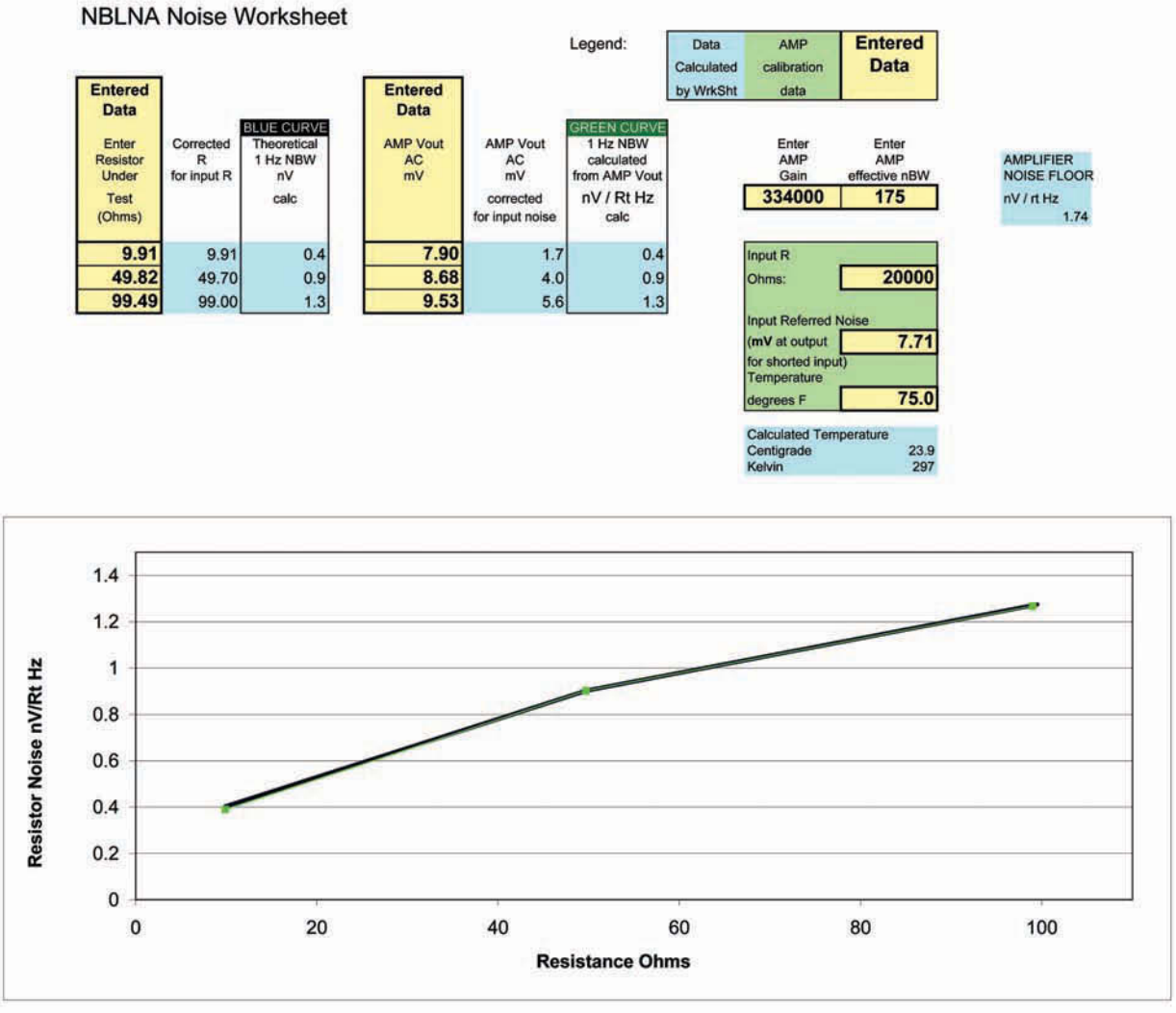

Figure 1 This downloadable spreadsheet lets you characterize an amplifier's gain and noise.

the blue curve for any low-noise-amp input resistance. The graph also shows a "green" curve that represents the amplifier's calculated "excess" output noise—the measured output minus the amplifier's uncorrelated input-referred noise. The input-referred noise is an uncorrelated noise signal that adds to any excess input noise as the square root of the sum of the squares of the noise voltages. You can find the amplifier's input-referred noise using its effective-noise-bandwidth and gain values and measuring the output-noise voltage by short-circuiting the amplifier's input terminals.

You can use a multimeter, such as Agilent's (www.agilent.com) 34410A, with a second-display math-average feature to fill in the measured output-noise values (**Reference 3**). After you connect each resistor to the amplifier's input terminals when the amplifier is on, reset the math average; wait until the new value settles down, which typically takes 10 seconds to approximately one minute; and record the average value for that resistor on the noise worksheet. Use the ohmmeter function to measure the actual resistance value and enter that value into the spreadsheet.

Enter the input parameters and measured output-noise values into the spreadsheet. Take a guess at the unknown parameter's initial value and then vary it until the green curve almost exactly overlaps the theoretical blue curve. When the curves overlap, you've found the missing parameter. You can then try what-if scenarios by varying both parameters. EDN

A MULTIMETER HAS A SECOND-DISPLAY MATH-AVERAGE FEATURE THAT CAN BE USED TO FILL IN THE MEASURED OUTPUT-NOISE VALUES. USE THE OHMMETER FUNCTION TO MEASURE THE ACTUAL RESISTANCE VALUE.

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2 Johnson, JB, "Thermal Agitation of Electricity in Conductors," *Physical Review*, Volume 32, July 1928, pg 97.

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Build a UWB pulse generator on an FPGA

Punithavathi Duraiswamy, Xiao Li, Johan Bauwelinck, and Jan Vandewege,
Ghent University, IMEC/Department of Information Technology, Ghent, Belgium

You can implement a digital UWB (ultrawideband) pulse generator in most FPGAs. The design lets you create a pulsed signal with a frequency that's twice the FPGA's clock frequency (**Figure 1**). A previous design relies on asynchronous delays to make pulses of the desired frequency. That design, however, requires an FPGA that supports tristate pullups, such as the Xilinx (www.xilinx.com) Virtex 2 (**Reference 1**). That approach also requires manual placement and routing. Today's FPGAs don't support tristate pullups. In addition, asynchronous delays vary with temperature. This Design Idea uses a synchronous-delay approach employing a combination of multiple clock phases. You can implement this design in all types of FPGAs.

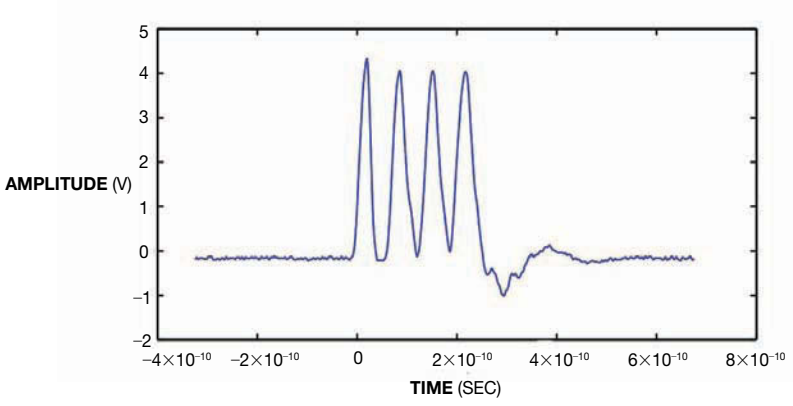

Figure 1 A pulse's frequency reaches twice the FPGA's clock frequency.

The maximum clock frequency of the DCM (digital clock manager) and the flip-flops are the main limiting factors in this design. For example, the DCM of a Xilinx Virtex 4 can't exceed 400 MHz. An FPGA can generate signals of frequencies that are half the clock frequency because it takes two clock pulses to toggle the signal from zero to one and back. Thus, you can't directly generate frequencies greater than half the clock frequency. This design lets you generate pulsed signals higher than half the clock frequency and reaches twice the clock frequency by using multiple clock phases from the DCM and synchronous delays smaller than one clock period.

Figure 2 shows the proposed pulse generator. It consists of three functional blocks, an OOK (on/off-key) modulator, a synchronous-delay generator, and an edge combiner comprising an exclusive OR gate. The OOK modulator comprises an inverter that the pulse-repetition-frequency signal triggers at every start of a new pulse. When a trigger occurs, the OOK circuit inverts a preinitialized signal to a time equal to a count value derived for a pulse width and remains zero until the next trigger. The OOK block generates a frequency that is one-half the clock frequency. This OOK output passes through the synchronous-delay generator, which generates three delayed versions of the OOK output.

These delays are smaller than one clock period. The clock phases in turn clock flip-flops FF_1, FF_2, and FF_3, which lag by 90, 180, and 270°, respectively. These delayed pulses then combine with the output of the OOK modulator using combinatorial logic to generate the desired frequency for the UWB pulses. The edge combiner performs an XOR (exclusive-OR) operation, which generates signal frequencies that depend on the edges you want to combine. Combining the output of the OOK edge with the output of FF_1 generates a signal frequency equal to the clock frequency. Combining the edges of all outputs generates a signal frequency equal to two times the clock frequency. The DCM synchronizes these

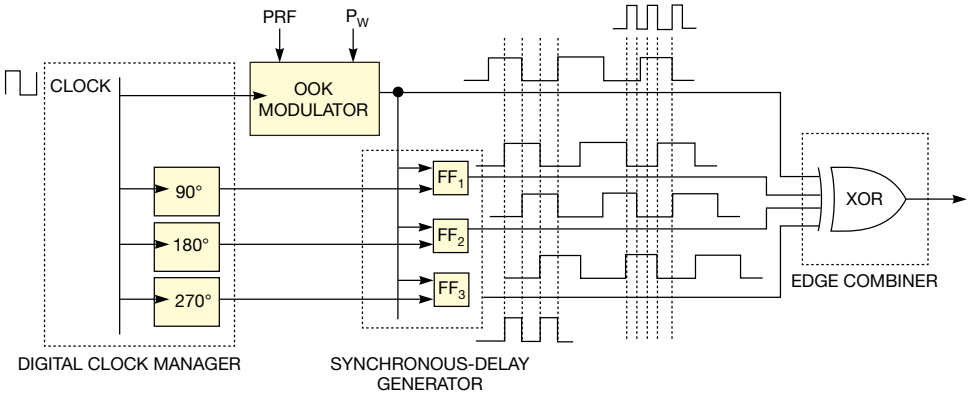

Figure 2 The design uses an OOK modulator, a clock manager with three phase shifters, three flip-flops, and an exclusive OR gate.

delays, producing an accurate signal frequency. This design is less complex than the asynchronous-delay approach in **Reference 1**.EDN

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1 Park, Youngmin, and David D Wentzloff, "All-digital synthesizable UWB transmitter architectures," *Proceedings of the 2008 IEEE International Conference on Ultra-Wideband*, Volume 2, 2008, http://bit.ly/j3wVuG.

Generate swept sine/cosine waveforms with two filters

John R Ambrose, Mixed Signal Integration, San Jose, CA

Demodulators, directional circuits, and other electronics applications often need two sine waves with a 90° difference in phase—a sine wave and its cosine wave. Engineers typically use analog filters to create the phase shift. This approach, however, offers a limited frequency range. Using the circuit in **Figure 1**, you can make a swept sine/cosine pair at frequencies of less than 1 Hz to 25 kHz.

The Mixed Signal Integration (www.mix-sig.com) MSFS5 selectable lowpass/bandpass switched-capacitor filter removes the harmonics from a square wave you apply to its inputs. The clock for the MSFS5 is 100 times the input square wave. The 74HC390 and 74HC74 form a divide-by-25 and a divide-by-two circuit. The Q outputs from the 74HC74 connect to the two divide-by-two circuits in the 74HC390A, which produces square waves that are 1/100 of the filter clock's frequency and are 90° out of phase from each other. A square wave at CMOS levels would saturate the filter, so the circuit uses resistor dividers R_1 through R_4 to reduce the signal's amplitude.

Figure 2 shows the output of the two filters at 20 kHz with a system clock of 2 MHz. Note that the phase reading on the scope is at –89.85°. When swept in frequency, the phase varies from –89 to –91°. **Figure 3** shows a 20-kHz Lissajous pattern.

Measuring the circuit's distortion using a spectrum analyzer and an Audio Precision (www.ap.com) audio analyzer shows a THD (total harmonic distortion) of –49 dB. Testing shows that the circuit has no discontinuity at the filter outputs with either FSK (frequency-shift keying) or FM (frequency modulation).EDN

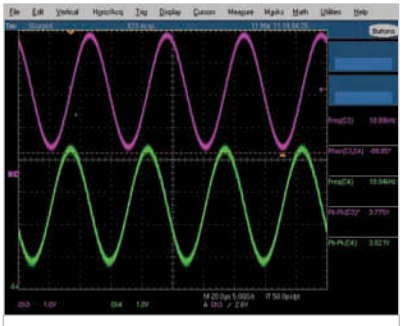

Figure 2 The phase reading on the scope is –89.85°.

Figure 3 When swept in frequency, the phase varies from –89 to –91°.

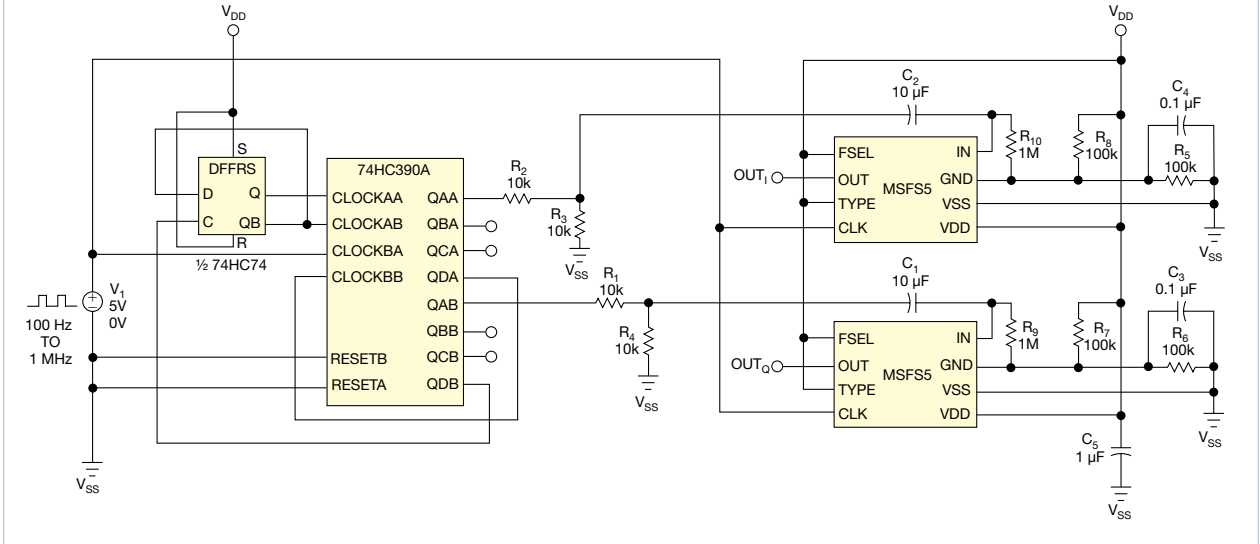

Figure 1 This circuit lets you make a swept sine/cosine pair at frequencies of less than 1 Hz to 25 kHz.

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Compensate for four-wire sensor errors

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Resistive pressure sensors that use two resistive elements and four wires are useful in pressure-monitoring applications. When the pressure rises, one resistance rises and the other falls. Accurate measurements with resistive sensors require compensation for losses due to wire resistance, especially when wire lengths are tens of meters. The compensation method in this Design Idea relies on the equal resistance of wires: $R_{L1}=R_{L2}=R_{L3}=R_{L4}=R_L$ (**Figure 1**).

A microcontroller or computer can calculate the resistance of the sensors using a differential voltage across sensor elements R_{S1} and R_{S2}. Resistances R_A, R_{REF}, and R_B and the sensor resistance limit the current through R_{S1} and R_{S2}. To measure the sensor values, the circuit uses an Analog Devices (www.analog.com) AD7705 ADC, which has three pseudodifferential inputs that provide 16-bit resolution. In this application, the AD7705 operates in buffered mode—that is, the input bias current is less than 1 nA. In buffered mode, the analog inputs can handle large source impedances, but the absolute input voltage must be from ground plus 50 mV to the drain-to-drain voltage minus 1.5V. Resistance R_B provides an input common voltage.

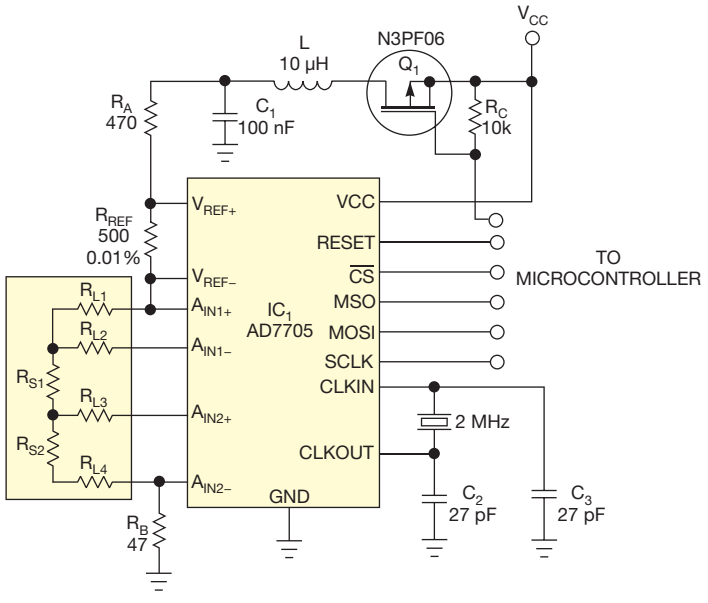

Figure 1 A measurement circuit measures the values at three points, and a microcontroller can calculate the sensor values.

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The measurements depend on the value of reference resistor R_{REF}. For best accuracy, R_{REF} must have a tolerance of 0.01% and must have a low temperature coefficient. To avoid sensor self-heating, you should pulse the excitation current; software through Q_1 controls the pulse width.

The AD7705 performs the data acquisition through three channels. The sensors connect directly to the AD7705's input channels, which make three successive acquisitions. Because the excitation current is the same in all sensor elements, the software computes each input voltage for the sensor elements in the following sequence:

1. A_{IN1+}, A_{IN1-} compute R_L;
2. A_{IN2+}, A_{IN2-} compute $R_{S2}+R_L$;
3. A_{IN1-}, A_{IN2-} compute $R_{S1}+R_{S2}+R_L$.

You can compute the resistances R_{S1} and R_{S2} by subtraction. The AD7705 has a PGA (programmable-gain amplifier) that amplifies low input signals. The part contains self-calibration and system-calibration options that eliminate gain and offset errors in the part or in the system.

The pressure measurement also depends on both the resistance ratio and the temperature through the **equation** $P=F(R_{S1}/R_{S2},T)$. The parameter T is a compensation factor for the resistive sensors' temperature dependence, $T=F(R_{S1}+R_{S2})$. EDN

LED-current limiter accepts ac or dc

Roger Griswold, Micrel, San Jose, CA

LED drivers have lots of features and require plenty of external components. When your application requires no PWM (pulse-width-modulated) dimming or controlled frequency operation, your primary concern may be that too much current could damage or destroy your LEDs. In this case, you can make a simple LED-current limiter from a common low-dropout linear regulator. The circuit in **Figure 1** is an LED light bulb for a landscape-lighting system. Landscape lighting typically operates from 12V ac, and peak voltage is approximately 17V. Because the regulator is in series with the LED string, the LED-string current equals the regulator's output current.

The circuit uses reasonably priced, 150-mA, warm-white LEDs; low-cost rectifier diodes; and Micrel's (www.micrel.com) 2.5V MIC5209-2.5YS regulator (**Figure 1**). The regulator must source at least the required LED current and handle the peak input voltage minus the drop across two of the four rectifier diodes and the drop across the LEDs. Selecting a regulator with the lowest possible output and dropout voltages lets LED current flow for a larger portion of each ac cycle, and it reduces the power requirement of current-setting resistor R_1. As output and dropout voltages decrease, cost increases. The regulator sees the peak voltage at approximately 5.1V and dissipates approximately 0.2W.

The MIC5209-2.5YS' output voltage regulates to 2.5V between its output and ground. R_1 sets the LED-string current using $R_1=(2.5/I_{LED})$, where I_{LED} is the LED-string current. With a value of 16.9Ω for R_1, the string current is 148 mA. The circuit has slightly more than 2.5W peak dissipation. With an ac input, the current flows only about half the time, so the average power dissipation is approximately 1.26W.

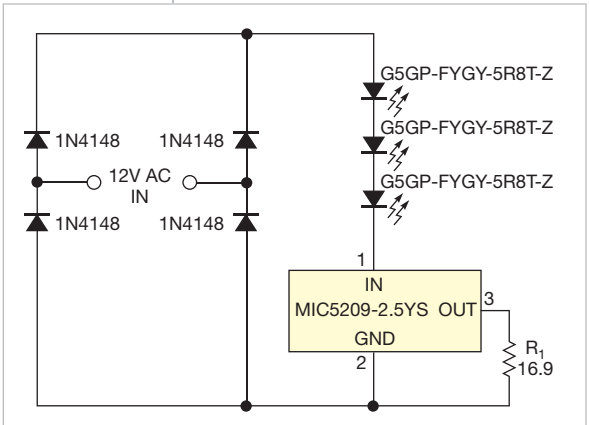

Figure 1 A low-cost regulator is the heart of an LED-current limiter.

You can easily modify the circuit to accept almost any input voltage. Simply change the number of LEDs and make sure that the rectifier diodes can handle the reverse voltage. Add or subtract one LED for each 3.33V increase or decrease in peak input voltage. Don't use LEDs for the rectifier diodes to get more light output because LEDs don't have sufficient reverse-breakdown voltage and will fail. The input bridge accepts either ac or dc and negates the need to worry about the polarity of a dc input. EDN

Voltage inverter employs PWM

Jeff Wilson, STMicroelectronics, Schaumburg, IL

This Design Idea describes a circuit employing a small microcontroller-based sensor module with only three connections: 5V dc, an RS-232 transmit-data output, and ground. A dedicated single-voltage level shifter or a dc/dc converter would be too costly, but the design still needs to supply ±3V at 1 mA to drive the transmit-data pin. Because a spare PWM (pulse-width-modulator) output on the 5V microcontroller could drive ±5 mA at nearly 5V, a PWM-based voltage inverter using a BAT54S dual-series Schottky diode, two capacitors, and a limiting resistor would produce the negative voltage (**Figure 1**).

The microcontroller's PWM output drives the inverter with a 1-kHz, 50%-duty-cycle, 0 to 5V waveform. When the PWM output is 5V, it charges C_1. The lower diode in D_1 biases in a forward mode to connect the terminal to ground. When the PWM output is low, it transfers the charge in C_1 to C_2 by forward-biasing the upper diode in D_1. Meanwhile, it inverts the charge by taking the positively charged terminal of C_1 nearly to ground potential. When the PWM output switches high again, the cycle repeats.

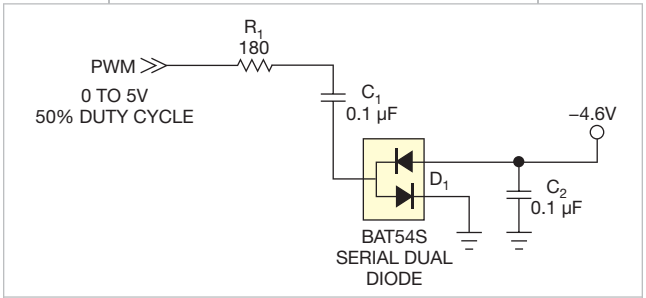

Figure 1 The diodes and capacitors produce a negative voltage.

Due to D_1's minimum voltage drop of 0.2V, it is impossible to get to –5V from 5V, so the voltage output will be approximately –4.6V, with 0.2V loss in each phase. The design requires a limiting resistor,

R_1, only when the driving microcontroller is sensitive to the current transients when switching or if the switching transients disturb the analog inputs on the microcontroller.

The PWM's timebase is 1 kHz, so component values must accommodate that frequency. If you need other frequencies, you must calculate new component values using the following **equation**: C=1/(10×F×R), where C is the value of C_1 and C_2, F is the PWM switching frequency in hertz, and R is the total resistance of the PWM's output-driving circuit.

When calculating the total resistance of the PWM output, you must take into account the drive rating of the digital output. A simple substitution for the value of R is V/A, where V is the drive voltage of the PWM's output and A is the current drive of the output in amps. For example, the original values for this design are R=V/A=5V/0.005A=1000Ω, and C=1/(10×F×R)=1/(10×1000 Hz×1000Ω)=1×10^{-7}, or 0.1 µF.

You can also use this circuit as a negative-voltage supply for ADC/DAC and op-amp dual supplies. For analog usage, you probably need to use additional filtering or micropower voltage regulators on the output to filter out the switching transients. EDN

Form positive pulses from negative pulses

Vladimir Rentyuk, Zaporozhye, Ukraine

The circuit in this Design Idea converts negative pulses to positive pulses. Although that task may seem simple, the negative pulses have amplitudes of –5 to –2V. The positive pulses also need different pulse widths, depending on the application, and the negative pulses are trapezoidal. The pulses must travel over a long-distance transmission line to a control device. Several circuits solve the problem, depending on the amplitude and shape of the pulses.

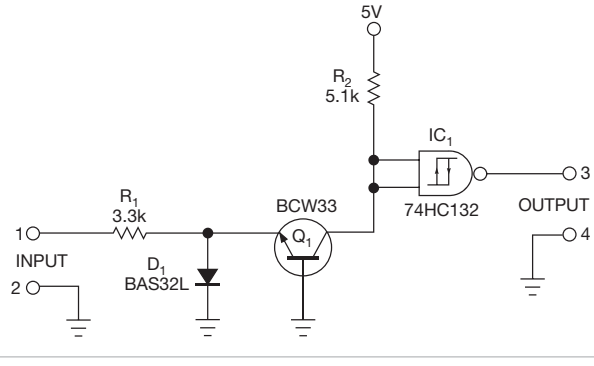

Figure 1 This circuit uses a single power supply and has good noise immunity but doesn't reliably convert pulses of trapezoidal shape.

Figure 1 shows a circuit that needs just one 5V power supply. Its high trigger threshold maximizes noise immunity. This circuit requires a high input current that's comparable to a collector current. It also needs a CMOS or TTL (transistor-transistor-logic) inverter to trigger on a threshold voltage. If the input pulse is a trapezoid, the output pulse width doesn't correspond to the input pulse widths. You can calculate a threshold, V_{T-}, as V_{T-}=–[(V_+–V_{IH})×R_1/R_2+0.62], where V_{T-} is the lower voltage threshold, V_+ is the power-supply voltage, and V_{IH} is the high-level input voltage of the 74HC132. **Figure 2** shows the input and output waveshapes.

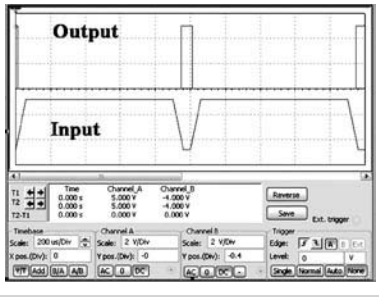

Figure 2 Output pulses are approximately the width of the most negative part of the input.

Figure 3 shows a pulse shaper that can convert 3-µsec negative-polarity pulses to positive pulses. The output pulse's width is sufficiently close to the pulse width of the input pulse. This circuit requires neither high input current nor an inverter. It has a lower voltage threshold than the circuit in **Figure 1**: V_{T-}≥–0.3V, but the circuit in **Figure 3** needs two supply voltages: ±5V. **Figure 4** shows the waveforms for the circuit in **Figure 3**.

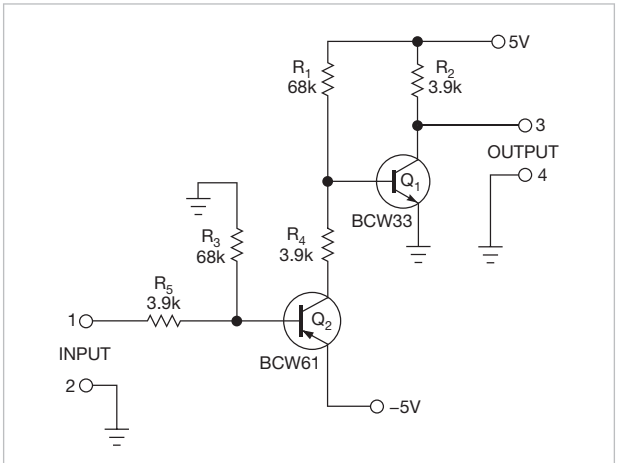

Figure 3 You can use this circuit to convert pulse polarity, but it needs two power supplies.

The circuit in **Figure 5** goes a step further. It uses an inexpensive LM211 or LM311 IC comparator and produces positive output pulses that fully correspond to the pulse width of the input pulse on its adjusted level (**Reference**

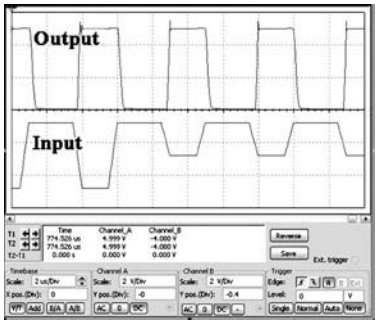

Figure 4 Pulse widths are a minimum of 3 µsec.

1). Resistors R_3 and R_4 set the comparator's threshold voltage, but it depends on the value of the negative supply's voltage. You can calculate the threshold voltage using the **equation** $V_{T-}=[V_-/(R_2+R_4)]\times R_4$, where V_- is the negative power-supply voltage. **Figure 6** shows the circuit's waveforms.

You can use the less expensive LM211 comparator if the pulse width is 2 µsec or longer. Otherwise, use a high-speed comparator. Doing so eliminates the need for the additional output resistor, R_1. The LM211 requires this resistor because of the IC's open-collector circuit. This circuit needs two supply voltages.

The circuit in **Figure 7** can convert negative-polarity pulses to positive pulses where the output does not depend on the amplitude of input pulses. This version uses a single supply and a 555 timer (**Reference 2**). It produces output pulses of positive polarity with a desired pulse width. Resistors R_1 and R_3 establish a threshold of actuation. You can calculate this threshold using $V_{T-}=V_+/3\times(1-2R_3/R_1)$, where V_+ is the 555's power-supply voltage. Resistor R_2 and capacitor C_1 set the pulse width. The **equation** $t=1.1R_2C_2$ calculates the duration of the output high state. For proper operation of the circuit, the actuation pulse must be shorter than the desired pulse width, and the pulse period must be greater than t. Resistor R_3 must have a value of at least 1.5 kΩ. Resistor R_4 is optional.

In contrast to the circuits in **figures 1**, **3**, and **5**, the circuit in **Figure 7** operates on low-resistance loads, with output source or sink current as high as 200 mA, or a high-capacity load. The circuit requires no additional inverter or driver. Resistor R_5 protects the IC from short circuits at its output. **Figure 8** shows the circuit's waveforms. EDN

REFERENCES

1 "LM111/LM211/LM311 Voltage Comparator," National Semiconductor, January 2001, http://bit.ly/lMkjPC.
2 "LM555 Timer," National Semiconductor, July 2006, http://bit.ly/igQqgz.

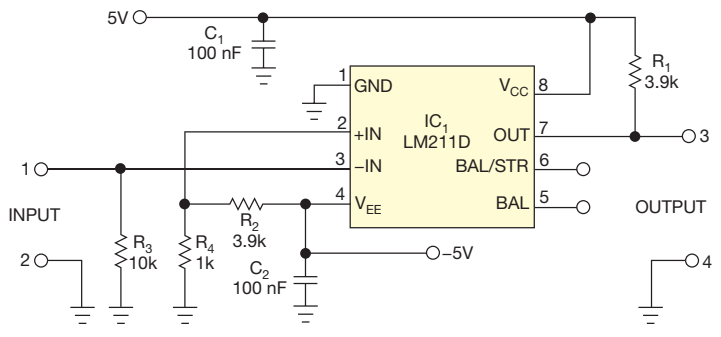

Figure 5 A comparator in this circuit produces accurate pulse widths.

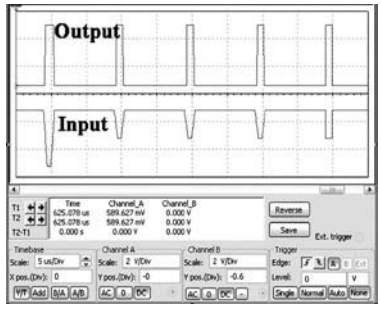

Figure 6 Positive output pulses are nearly the same width as negative input pulses.

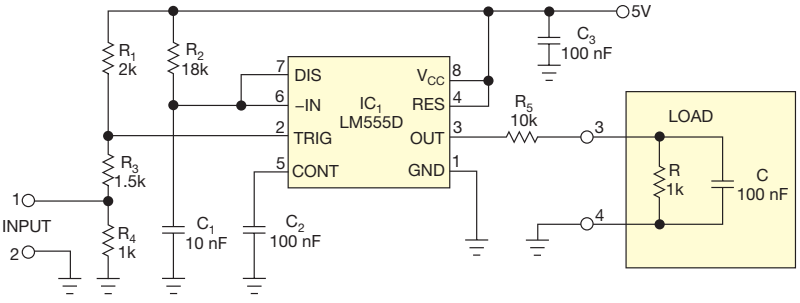

Figure 7 This pulse converter uses a 555 timer.

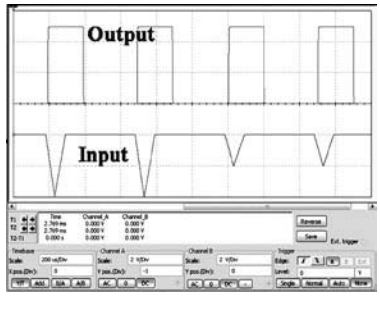

Figure 8 The 555 timer in Figure 7 produces positive pulses of the desired width.

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Positive edges trigger parabolic timebase generator

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Nonlinear systems often need to become linear to be useful, and the circuit in **Figure 1** provides a nonlinear sawtooth pulse for a PWM (pulse-width modulator) that can compensate for nonlinearities in sensors, controllers, or systems. The circuit outputs a linear sawtooth pulse, a quadratic parabolic pulse, and a cubic parabolic pulse of equal and constant width following an external trigger pulse. All pulses have equal peak amplitudes.

The circuit incorporates a cascade of three synchronously switched integrators. IC_3's S_2D_2 switch switches the input of integrator IC_{2D}, the first in the chain, to the source of reference voltage V_{REF}. You need two integrators employing IC_{2D}

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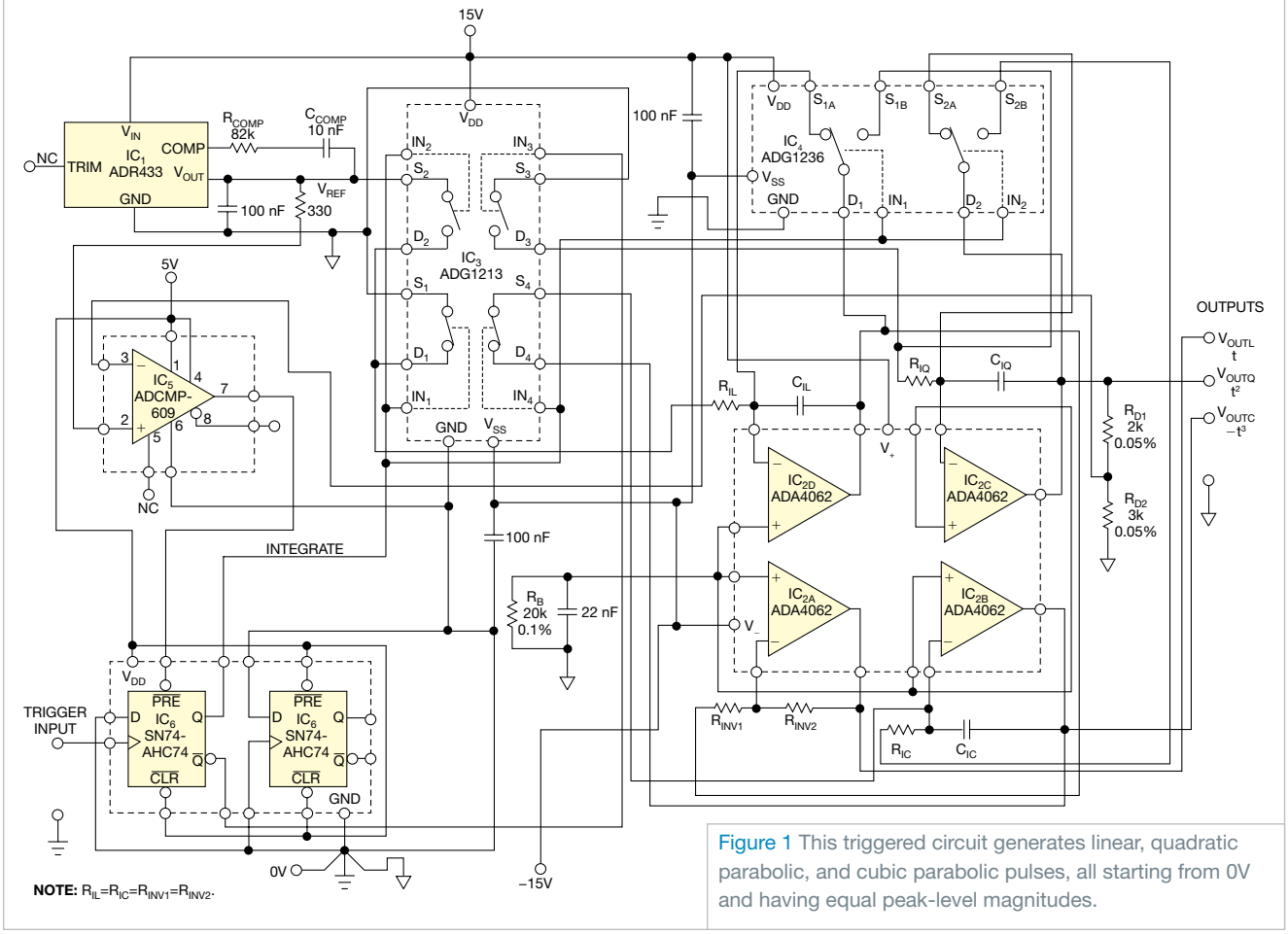

NOTE: $R_{IL}=R_{IC}=R_{INV1}=R_{INV2}$.

Figure 1 This triggered circuit generates linear, quadratic parabolic, and cubic parabolic pulses, all starting from 0V and having equal peak-level magnitudes.

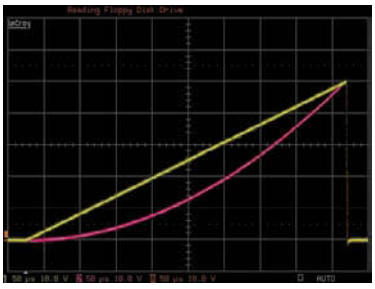

Figure 2 At the midwidth of the pulse, the quadratic parabolic pulse's voltage level (pink trace) is exactly one-fourth of its peak level.

and IC_{2C} to generate a quadratic parabolic pulse. The third integrator, using IC_{2B}, lets you simultaneously generate a cubic parabolic pulse. Each integrator has a series input switch and a reset switch that connects in parallel with a respective integrating capacitor.

The $S_{1A}D_1$ switch in IC_4 is a reset switch for integrator IC_{2D}. The complementary $S_{1B}D_1$ switch serves as a series input switch for integrator IC_{2C}. Similarly, the $S_{2A}D_2$ switch is a reset switch for integrator IC_{2C}. The $S_{2B}D_2$ switch is a series input switch for integrator IC_{2C}. The positions of all switches are at logic high at all control inputs: IN_1 to IN_4 of IC_3 and IN_1 and IN_2 of IC_4.

Integrators IC_{2D} and IC_{2C} also have input-grounding switches in IC_3, S_1D_1, and S_3D_3, respectively. The grounding switches ensure that error due to leakage currents of the series switches is approximately 50% less than that of a design not using the grounding switches.

The Integrate logic signal controls all series switches. When the signal is high, it turns on all the reset and grounding switches. Thus, integrators IC_{2B}, IC_{2C}, and IC_{2D} are either integrating their respective analog input signals or resetting to a 0V output. The input of integrator IC_{2D} switches to the output of precision voltage-reference cell IC_{2A}. Thus, signal V_{OUTL} becomes a negative sawtooth pulse. The pulse varies within its duration, T_1, as:

$$V_{OUTL}(t) = -V_{OUTLPEAK} \times \frac{t}{T_1}.$$

Inverter IC_{2A} inverts this pulse. IC_{2A} has a voltage gain of negative one because positive pulses are more common. Integrator IC_{2B} integrates sawtooth pulse V_{OUTL}; IC_{2B} therefore outputs a quadratic parabolic pulse:

$$V_{OUTQ}(t) = V_{OUTQPEAK} \times \left(\frac{t}{T_1}\right)^2.$$

The **equation** describes a pulse that integrator IC_{2B} simultaneously integrates, producing a cubic parabolic pulse:

$$V_{OUTC}(t) = -V_{OUTCPEAK} \times \left(\frac{t}{T_1}\right)^3.$$

$V_{OUTLPEAK}$, $V_{OUTQPEAK}$, and $V_{OUTCPEAK}$ are negative or positive voltage peaks at the outputs of their respective integrators. T_1 is the width of the Integrate pulse. Theoretically, to achieve $V_{REF}=V_{OUTLPEAK}=V_{OUTQPEAK}=V_{OUTCPEAK}$, you must stagger the integrating time constants of the respective integrators as 1-to-1/2-to-1/3, respectively. In this case, however, V_{REF}=3V, whereas $V_{OUTLPEAK}=V_{OUTQPEAK}=V_{OUTCPEAK}$=5V.

You must multiply the 1 in the staggering ratio by 3/5. Considering the time constant of integrator IC_{2C}, you get a stagger ratio of 6/5-to-1-to-2/3. For the equal values of integrating resistors $R_{IL}=R_{IQ}=R_{IC}$, this staggering holds true for the values of respective integrating capacitors. The circuit uses a high-quality, SMD (surface-mount-device) ceramic capacitor, C_{IQ}, with a value of 2.3692 nF. To achieve the necessary precision staggering, C_{IL} comprises 2.4016-nF, 343-pF, and 79-pF capacitors in parallel. C_{IC} is a parallel combination of 1067 pF and 499 pF.

A rising edge at the trigger input forces the Integrate signal low, which turns off the reset and grounding switches and turns on the series switches. The integration lasts until $V_{OUTQPEAK}$=5V, forcing the output of IC_5 low, which in turn sets Integrate high. Thus, the series switches are off, and the reset and grounding switches are on. The circuit remains in this steady state until the next rising edge at the trigger input. The Analog Devices (www.analog.com) ADG1213 and ADG1236 switches work well in this design because of their charge injection of 1 pC or less. **Figure 2** shows the circuit's high precision, depicting linear and quadratic-parabolic-pulse shapes. EDN

Measure small currents without adding resistive insertion loss

Maciej Kokot, Gdansk University of Technology, Gdansk, Poland

In most cases, you measure current by converting it into a proportional voltage and then measuring the voltage. **Figure 1** shows two typical methods of making the conversion. In one method, you insert a probing resistor, R_P, in series with the current path and use differential amplifier IC_1 to measure the resulting voltage drop (**Figure 1a**). A second method is a widely known operational amplifier current-to-voltage converter in which inverted IC_1's output sinks the incoming current through the feedback resistor (**Figure 1b**).

In the first method, the same current that flows into one node flows from the second node, but a significant voltage drop occurs across probing resistor R_P. In the second method, the voltage drop is on the order of tens of microvolts to millivolts, depending on IC_1's quality, but the measured current flows only into the sensing node with no return to the circuit. You can measure only currents flowing to ground.

The circuit in **Figure 2** operates in a somewhat similar manner to the one in **Figure 1b** in that an op amp's output sinks the incoming measured current. However, the other op amp's output sources an equal outgoing current back to the circuit under test.

In **Figure 2**, input current I flows through R_1 into the output of IC_2, which reduces its voltage by the amount of IR_1 relative to the input node. That voltage equals the voltage mean of the op amp's outputs, which R_3 and R_4 set at the op amp's inverting inputs. Consequently,

the output of IC_1 must rise to a voltage of IR_2 relative to the inverting inputs and the equal-voltage noninverting input node of IC_2. IC_1 sources this current, which returns through R_2 to the circuit under test. R_1=R_2, so the output current is the same as the input current. Because the op amp's outputs maintain their inputs at equal voltages, the circuit under test has virtually no resistance.

The circuit in **Figure 2** has the advantages but not the drawbacks of those in **Figure 1**. The current that flows into the first node flows from the other node, and the voltage drop is almost zero; the maximum is twice the input offset voltages. You can use this circuit in a circuit under test without changing the voltage and current flows. EDN

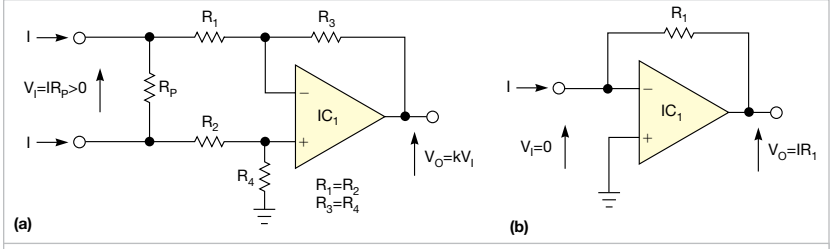

Figure 1 In one method of converting current to a proportional voltage, you insert a probing resistor, R_P, in series with the current path and use differential amplifier IC_1 to measure the resulting voltage drop (a). In another method, inverted IC_1's output sinks the incoming current through the feedback resistor (b).

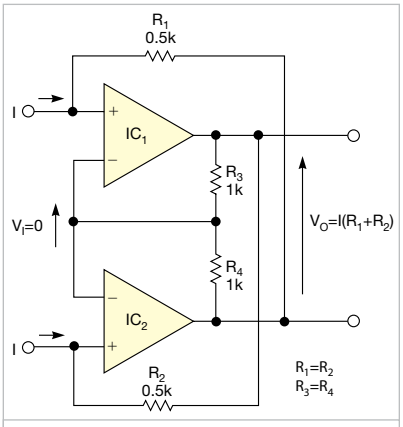

Figure 2 This current-to-voltage conversion method forms a zero-voltage converter.

Power resistor varies in value

Bogdan Raducanu, Bucharest, Romania

Testing power supplies or discharging batteries usually requires a constant-current load. Sometimes, however, you must study the behavior when the load is a resistor. Using a high-power potentiometer is an expensive approach that might not be worth the cost. The circuit in **Figure 1**, which performs like a high-power resistor that connects between P_1 and P_2, provides an alternative approach.

To understand how the circuit works, assume that the op amp is ideal and that the total resistance of R_2 and R_3 exceeds that of a high-power resistor (not shown). R_2 and R_3 form a divider that produces an output voltage, according to the following **equation**:

$$V_{REF}=V_{IN}\frac{R_2}{R_2+R_3}.$$

The operational amplifier maintains a voltage, such that R_1's voltage equals the reference voltage, that causes the current through R_1 to be:

$$I_{R_1}=\frac{V_{R_1}}{R_1}=\frac{V_{REF}}{R_1},$$

Substituting the first **equation** in the second **equation** yields:

$$I_{R_1}=\frac{V_{IN}\frac{R_2}{R_2+R_3}}{R_1}=V_{IN}\frac{R_2}{R_1(R_2+R_3)}.$$

If you neglect the current through R_2 and R_3, then R_1's current equals the input current, as the following **equation** describes:

$$I_{IN}=V_{IN}\frac{R_2}{R_1(R_2+R_3)}.$$

This **equation** shows a linear relationship between the input current and the input voltage. Thus, the circuit between P_1 and P_2 acts as a resistor. The **equation** then becomes:

$$R=\frac{V_{IN}}{I_{IN}}=R_1\frac{R_2+R_3}{R_2}=R_1k.$$

where $k=(R_2+R_3)/R_2$ is a factor greater than 1, which multiplies R_1. Making either R_2 or R_3 variable lets the circuit function as a variable resistor. The cost of a suitable transistor and R_1, along with the rest of the components, is smaller than that of a variable potentiometer that can dissipate the same amount of power.

The circuit has some limitations, however. First, it can accept input voltages

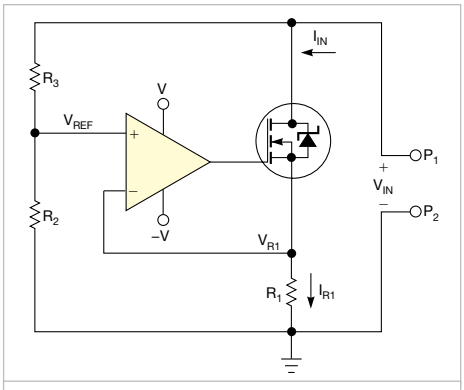

Figure 1 The resistance of the MOSFET, functioning as a variable resistor, changes.

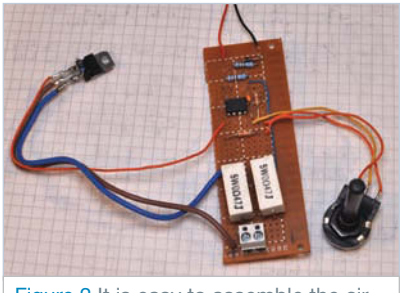

Figure 2 It is easy to assemble the circuit on a prototype board.

of only one polarity, which might limit its use in some applications. Second, the minimum resistor value is the value of R_1 plus the transistor's minimum on-resistance. Other factors such as op-amp offset, the values of R_2 and R_3, and input voltage influence the circuit's linearity, but the circuit still achieves high performance with low-cost components. Depending on the op amp's input range, the circuit requires an external dual power supply. **Figure 2** shows a prototype of the tested and built circuit using a potentiometer for changing the equivalent resistance and no heat sink on the power transistor. EDN

Minimize noise in power-supply measurements

John Lo Giudice, STMicroelectronics, Schaumburg, IL

You must minimize noise when measuring ripple in power rails because the ripple's amplitude can be low. Oscilloscope probes are essential measurement tools, but they can introduce noise and errors. Ground leads, such as those that attach to standard oscilloscope probes, can add noise that's not present in your circuit to an oscilloscope's trace. The wire loop acts as an antenna that picks up stray magnetic fields. The larger the loop area, the more noise it picks up. To prove this theory, connect the oscilloscope ground lead to the probe tip and move it around. The oscilloscope will show the noise increasing and decreasing with the ground-lead movement. You can use an oscilloscope probe with its ground lead and sockets to build a simple interconnect board (**Figure 1**).

Start by removing the probe's cover, which reveals the probe tip. There is a short distance between the tip and the ground ring. You need one of two sockets: a right-angle, or horizontal, socket or a vertical socket, similar to those in **Figure 1**. Solder the center leg of the socket to the output of the power supply and solder the other leg to the power-supply return. Connect a 0.1-µF surface-mount, stacked ceramic capacitor between the two sockets. This step limits the probe bandwidth to approximately 5 MHz, which further reduces high-frequency noise and lets the lower-frequency ripple pass through. **Figure 2** shows the completed interconnect board, and **Figure 3** shows a schematic of the board. Insert the probe tip into the socket to measure ripple. You will get a ripple measurement without spikes or other noise.

You should use a multilayer stacked ceramic capacitor because it's better at decoupling high-frequency noise. Electrolytic, paper, and plastic-film capacitors comprise two sheets of metal foil. A sheet of dielectric separates the metal-foil sheets, and these three components form a roll. Such a structure has self-inductance; thus, the capacitor acts more like an inductor than a capacitor at frequencies higher than a few megahertz. **Figure 4** shows the impedance to the power supply for various stacked-ceramic-capacitor values. EDN

Figure 1 A standard oscilloscope probe has a ground lead that can pick up noise.

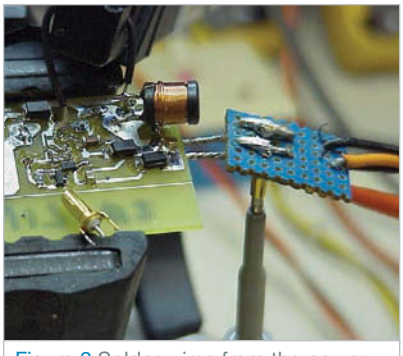

Figure 2 Solder wires from the power supply under test to an interconnect board reduce ground-lead length.

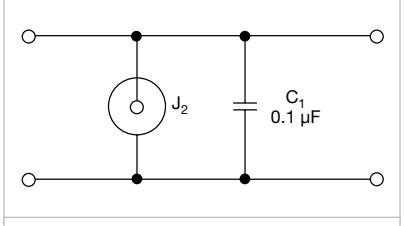

Figure 3 A ceramic capacitor further reduces high-frequency noise.

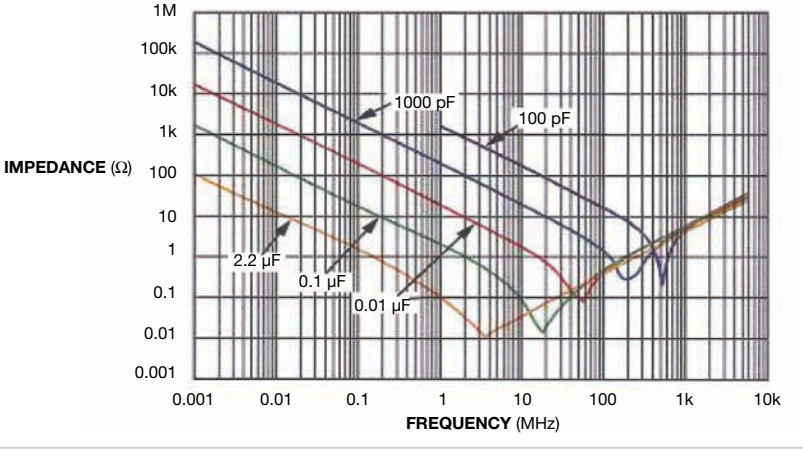

Figure 4 Probe impedance varies with capacitor value.

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AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Driver circuit lights architectural and interior LEDs

Steve Sheard, On Semiconductor, Tempe, AZ

LEDs are more efficient than incandescent lights and can last 100 times longer, but they require specialized electronic-drive circuits to avoid overstress conditions. The main operating parameter is relatively simple: Keep the current through the LEDs constant and under the specified maximum.

Traditional power supplies have accurate voltage outputs with variations in current. A resistor in series with an LED string controls the current. Such a design assumes a known voltage across the LEDs that does not vary with changes in LED temperature. Unfortunately, LEDs' forward voltage does change with temperature. LED manufacturers generally bin their devices by forward voltage, allowing a lighting manufacturer to build a lighting fixture to match this forward voltage at a fixed temperature. A circuit using unbinned LEDs saves the LED manufacturer time and results in less expensive LEDs. LEDs also have a negative forward-voltage-to-temperature coefficient that can cause the drive circuit to go into thermal runaway, requiring the designer to build safeguards into the design.

The ideal approach for driving LEDs is one in which the circuit monitors the current and keeps it constant. LEDs' forward voltage does not affect this type of circuit, eliminating the need for binning and the effect of the LEDs' negative forward-voltage-to-temperature coefficient. These circuits can be complex switching regulators or simple linear regulators with feedback loops. Complex switching regulators are ideal for high-light-output applications, such as streetlights.

Simple, economical, and robust hybrid circuits find use in architectural- and interior-lighting fixtures. These circuits' design may be less efficient than that of a complex switching regulator, but their low cost and simplicity make them attractive. These circuits operate over the full universal voltage specification of 85 to 265V ac at 50 or 60 Hz.

The circuit in **Figure 1** comprises a bridge, a chopper, and a current regulator. The full-wave bridge comprising diodes D_1, D_2, D_3, and D_4, feeds into the chopper circuit. MOSFET Q_2 immediately turns on, and capacitor C_1 begins to charge.

Resistors R_1 and R_2 form a voltage divider. When the voltage on the cathode of D_5 reaches 43.5V, the zener diode conducts and turns on Q_1, which pulls the gate of Q_2 low, causing it to turn off. Diode D_6 protects Q_2's gate.

The voltage across C_1 stays at 80 to 90V. The charge on C_1 feeds the CCR (constant-current regulator) and the LED string. This circuit example has 22 LEDs. The CCR maintains the current at 20 mA through the LED string. The circuit includes resistor R_4, in series with the LEDs, for measuring the current through the LED string.

Figure 2 shows the voltages at different parts of the cycle with an input voltage of 150V ac. Trace 1 is the output of the bridge-rectifier circuit. Trace 2 is the voltage across C_1, the output of the chopper circuit. Trace 3 is the voltage across the current-sense resistor. The traces clearly show that, when the voltage from

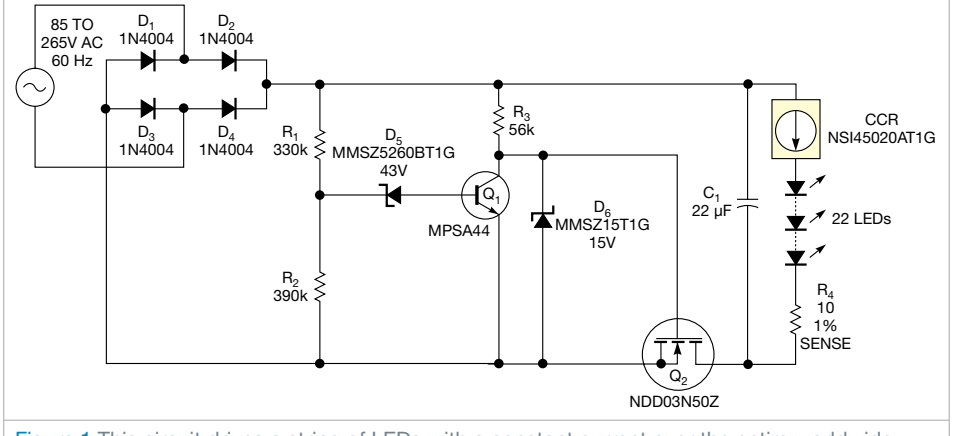

Figure 1 This circuit drives a string of LEDs with a constant current over the entire worldwide range of ac-mains voltages.

DIs Inside

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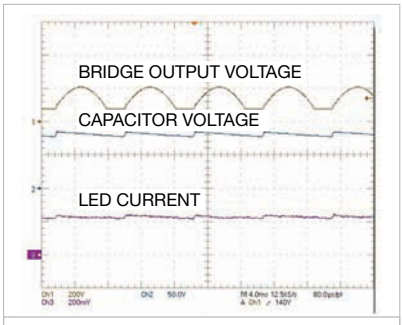

Figure 2 When the voltage from the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit.

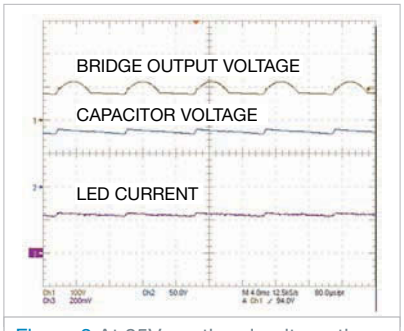

Figure 3 At 85V ac, the circuit continues to operate by keeping Q_1 on for a longer period.

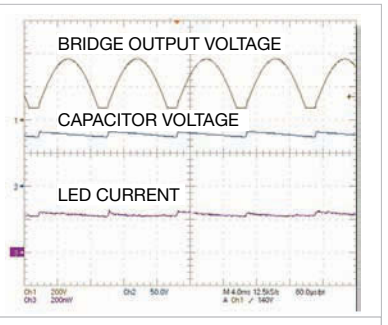

Figure 4 At 265V ac, the circuit has enough energy to keep C_1 charged during off cycles.

the bridge increases to more than 80V, the chopper circuit switches and limits the voltage applied to the regulator circuit. **Figure 3** shows the voltages with an input voltage of 85V ac.

The oscilloscope traces show that there is still sufficient design head room, with Q_1 staying on for a longer period, during which C_1 fully charges. The input voltage drops to 54V ac before the current through the LEDs begins to drop.

Figure 4 shows the circuit operation at an input voltage of 265V ac. Trace 1 shows that, because of its high input voltage, Q_1 is on for a short time. Trace 2, however, shows that sufficient energy still remains to charge Q_1 and maintain the current through the LEDs during the off cycle.

You can scale this circuit to operate with different LED arrays. CCRs are available with current ratings as high as 160 mA. For higher currents, you can place the CCRs in parallel. The values of C_1, R_1, and R_2 match the type and number of LEDs. EDN

Use op amps to make automatic-ORing power selector

Bob Zwicker, Analog Devices, Fort Collins, CO

Many systems must select among two or more low-voltage dc-input sources, such as an ac adapter, a USB (Universal Serial Bus) port, or an onboard battery, for example. You can implement this selection using manual switches, but automatic switching is preferable. You usually want to use the highest-available input voltage to power your system. You can accomplish this task using a Schottky-diode ORing scheme (**Figure 1**). Unfortunately, the forward-voltage drop of a Schottky diode ranges from 300 to 600 mV. This voltage wastes power, creates heat, and decreases the voltage available to your system.

Efficient voltage ORing requires only a P- or an N-channel MOSFET, a suitable op amp, and a few passives. This Design Idea describes the application of voltage ORing to positive dc-power rails. The P-channel-MOSFET design is suitable for low-power, single-supply systems operating at 3.3V or higher, and the N-channel MOSFET fits situations in which the bus voltage is lower or the current is higher and a suitable op-amp bias voltage is available.

Positive current flows from the MOSFET drain in an N-channel-FET design. In a P-channel design, the current flows from the MOSFET source. The MOSFET's drain-body diode would defeat rectifier operation if the usual current flow (for switching or amplification) were used.

Your first design task is to choose a suitable MOSFET. The MOSFET's worst-case on-resistance must be low enough so that the I×R (current-times-resistance) drop with full-load current is low enough to accomplish the design objectives. A 0.01Ω MOSFET has a 50-mV forward-voltage drop when 5A flows through it. Be sure to consider power dissipation due to $R \times I^2$ and the resulting temperature rise.

Your second design task is to choose an op amp. The op amp must be able to operate with the voltages involved and to adequately drive the MOSFET's gate voltage. The P-channel design requires a rail-to-rail I/O type. A single-supply op amp is adequate for the N-channel design. Another important consider-

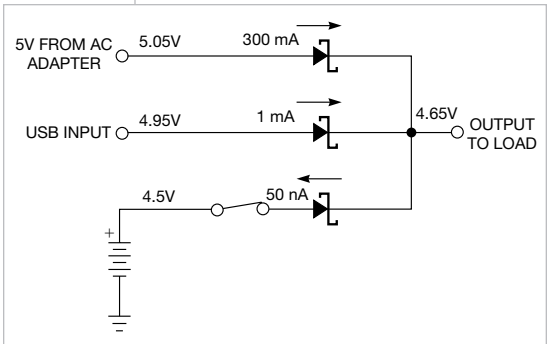

Figure 1 Schottky-diode ORing can power a load from the highest input-voltage source.

ation is the op amp's input offset voltage, V_{OS}. The total $\pm V_{OS}$ window must be less than the maximum desired voltage drop across the MOSFET. For example, if you permit a 10-mV forward-voltage drop at full load, then the op amp should specify an offset voltage of ±5 mV or better.

R_1/R_2, R_{11}/R_{12}, and R_{21}/R_{22} form the input-voltage divider, which biases the op-amp input at a level slightly below that of the input voltage that it is controlling (**figures 2** and **3**). This offset must exceed the op amp's maximum offset voltage to ensure that all op-amp parts in production always turn off the MOSFET when you apply reverse voltage. In the example of the P-channel 5V design, R_1 and R_2 bias the inverting op-amp input at 99.9% of the input voltage, or 4.995V dc. In steady-state operation, the op amp servos with the conducting MOSFET to keep the other op amp's input at the same voltage, within the tolerance of the op amp's offset voltage. With a perfect 0V-offset op amp, light-load currents cause the MOSFET to only partially enhance, so the circuit delivers a 5-mV MOSFET forward-rectifier drop. This mild effect is the only disadvantage of R_1 and R_2's input offset biasing. If the MOSFET resistance is too high to allow it to maintain 5 mV at full load, then the op amp fully enhances the MOSFET as its output swings to the rail, and the ORing circuit delivers the MOSFET's fully enhanced on-resistance.

You can consider the MOSFET's variable on-resistance as the element with which the op amp senses current. When you apply reverse voltage, the MOSFET de-enhances, the I×R voltage drop increases, and the op amp's output ends up at the appropriate supply rail, driving off the MOSFET as hard as it can.

With light-load conditions and a given offset voltage, the op amp tries to servo the voltage on its power-output-sensing input to the voltage on its power-input-sensing input plus the offset voltage. With R_2 open-circuited, the op amp has no intentional external offset. If the op amp's offset voltage were in the unfavorable direction, a sizable reverse-cutoff current would occur if the input-power bus were to fall to a lower potential than the output-voltage bus.

Figure 4 shows current-voltage test data for the operating region. The complete design, including intentional offset, produces the green curve. The

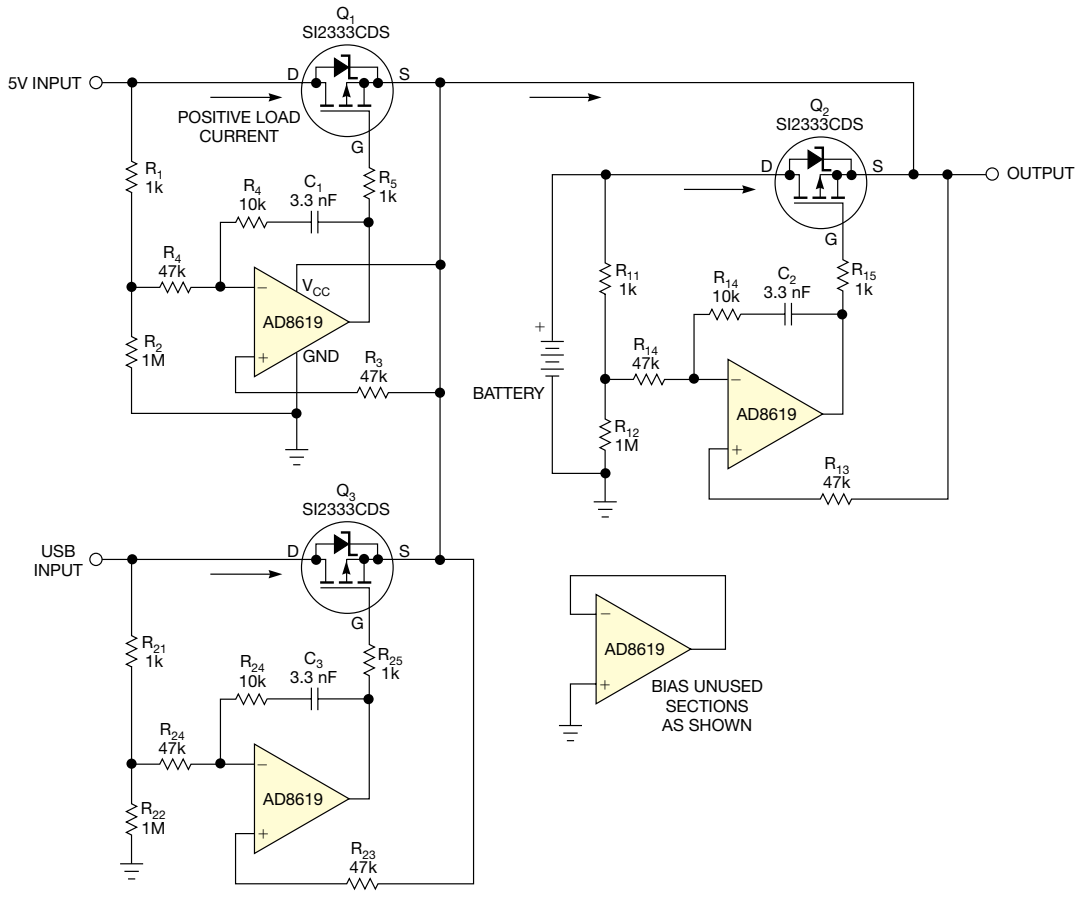

Figure 2 MOSFET power ORing using P-channel MOSFETs is the more common choice for single-rail systems when the rail voltage is sufficient to operate the op amp and drive the MOSFET gate.

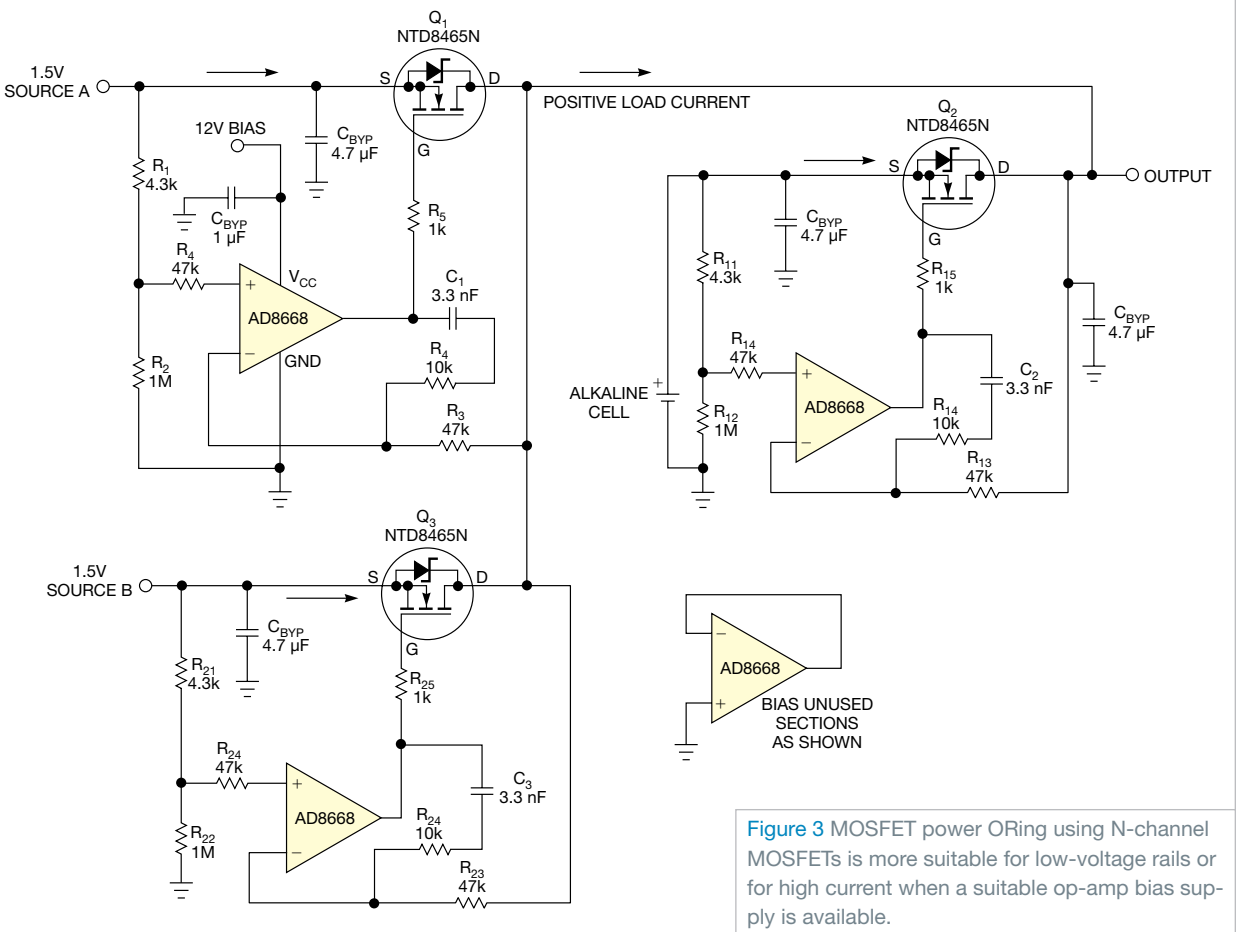

Figure 3 MOSFET power ORing using N-channel MOSFETs is more suitable for low-voltage rails or for high current when a suitable op-amp bias supply is available.

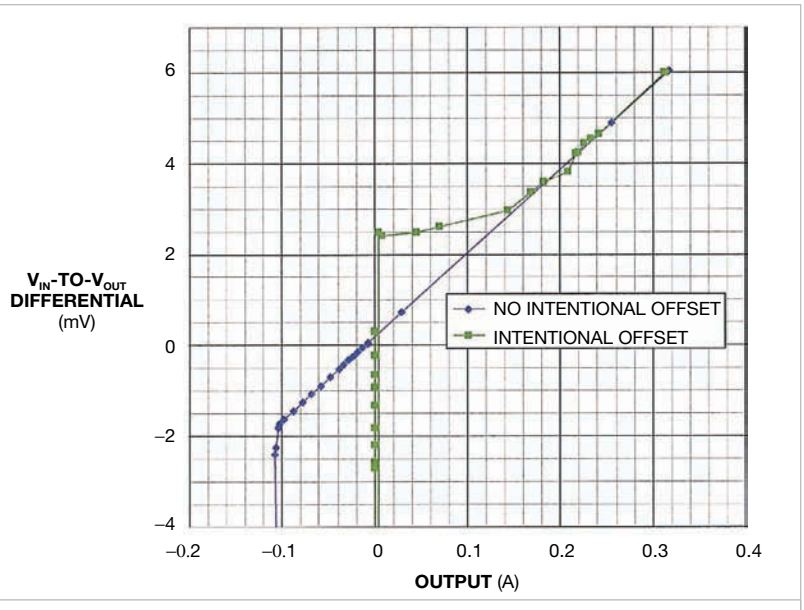

Figure 4 The green curve shows results with the correct external offset applied. The blue curve shows results when the op amp's internal offset is in the unfavorable direction and no external offset is applied.

equivalent of an unfavorable internal offset and no intentional external offset produces the blue curve. Although the green curve sacrifices some forward-voltage drop at light-load conditions, its forward voltage is always less than the full-load maximum. The intentional offset avoids any significant reverse current in the MOSFET. This design can switch at the 0A current transition, at which the leakage-current MOSFET's drain-body diode is likely to dominate.

On the other hand, the blue curve, without intentional offset, permits significant reverse current under some circumstances. This example shows approximately 100-mA reverse current with 2-mV reverse voltage across the MOSFET before the circuit switches off the MOSFET. Both the P- and the N-channel designs have undergone testing, and the P-channel design is in production. EDN

Charging time indicates capacitor value

Vlad Bande and Ioan Ciascai, Technical University of Cluj-Napoca, Cluj-Napoca, Romania

A recent research project using a capacitive sensor to measure water levels comprises two PCB (printed-circuit-board) plates placed one in front of the other at a controlled distance. Every plate divides into eight equal copper zones, resulting in eight equivalent parallel-plate capacitors (**Figure 1**). Every capacitor has a plate area of 25 cm^2. To measure the water's total height, the project uses a special hydro-insulated layer to avoid short circuits. Knowing the layer thickness and the electrical permittivity of the hydro-insulated substance allows you to express the distance between every two plates and the dielectric's electrical permittivity.

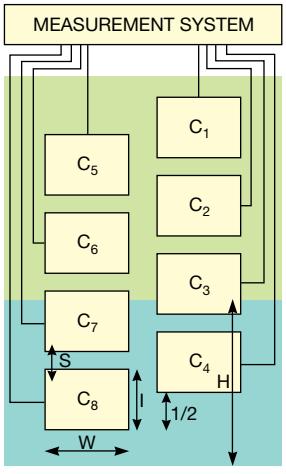

Figure 1 Plates and a PCB's dielectric form a capacitor bank for measuring water level.

The capacitance of every two overlapped copper zones can vary only when the electrical permittivity changes because all other parameters—the plate's area and the distance between the plates—are constant, as the following **equation** shows: $C_X=(\varepsilon_0\varepsilon_R A)/D$, where $\varepsilon_0=(8.854\times10^{-12})$F/m, the void electrical permittivity, ε_R is the dielectric's relative electrical permittivity, D is the total dielectric thickness, C_X is the capacitance of the measured capacitor, and A is every plate's surface. The relative electrical permittivity strictly depends on which and how many materials are between the capacitor plates. This application uses four kinds of ε_R: air, air-hydro-insulated varnish, water-hydro-insulated varnish, and air-water-hydro-insulated varnish. At this point, you must consider the capacity of the capacitors at the surface-separation line between air and water.

To measure capacitance and thus measure the water level, a measurement system employs a 20-MHz ATTiny 2313 microcontroller and a fast LT1016 analog comparator (**Figure 2**). The measurement algorithm uses the microcontroller's OC1A and OC1B output-comparator signals. The ATTiny 2313 sets both pins at once but to opposite values. When OC1A is 5V, you can simultaneously set OC1B using assembly-language code. The same situation occurs when OC1B is 5V; OC1A is then 0V. In the first case, the quantity of the charge rises on the first plate and lowers on the other plate. Reversing the polarity causes the second plate to acquire more charge, and its potential rises. When both plates have the same potential, the LT1016 comparator enables the ICP pin on the microcontroller, saving the number in the internal timer counter and sending it through the serial port for further processing. When the voltages on both plates are equal, the voltage on the capacitor is halfway from the input signal's amplitude, $V_{CC}/2$.

The pulse width of both OC1A and OC1B must be larger than the maximum capacitor's charging time, which you obtain when you measure the water's dielectric capacitor, according to the following **equation**: $PW\geq10\times R_e\times C_{MAX}$. **Figure 3** shows the waveforms.

The charging **equation** in the transient region is:

$$\frac{V_{CC}}{2}=V_{CC}+[0-V_{CC}]e^{-\frac{t}{2RC}}\Rightarrow\frac{1}{2}=e^{-\frac{N_1 t_{CLK}}{2RC}}.$$

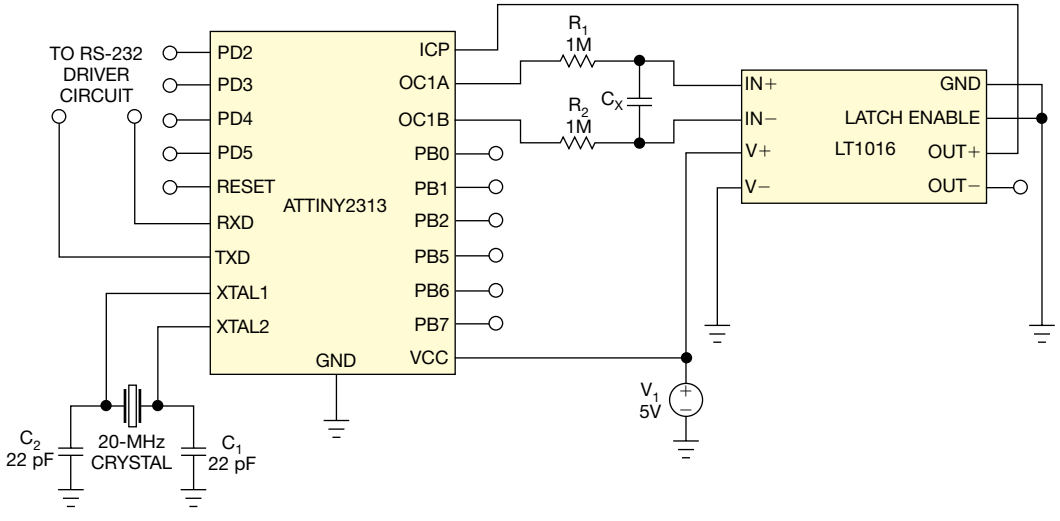

Figure 2 The measurement circuit comprises an ATTiny 2313 microcontroller and a comparator.

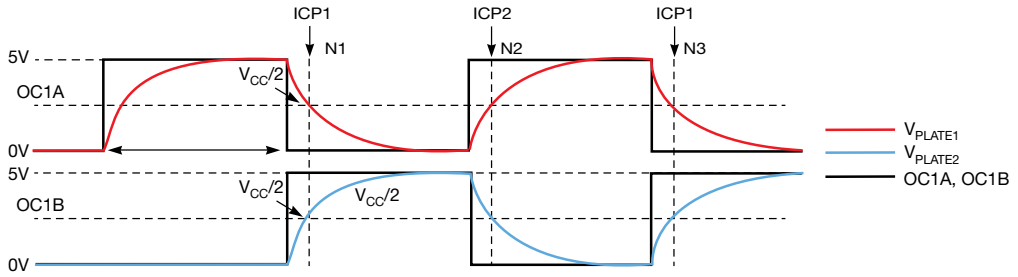

Figure 3 The capacitor plates have equal voltages at $V_{CC}/2$.

You can then extract the capacitance using the following **equation**:

$$C_x=\frac{N_1 t_{CLK}}{2R\ln 2},$$

or

$$C_x=0.036067376\times N_1 \text{ pF}.$$

You can extract the level on both the left and the right side of the capacitive sensor in **Figure 1**, resulting in two **equations** but the same result. The algorithm consists of first measuring all the capacitors—completely immersed, partially immersed, and nonimmersed—and then expressing the surface of both C_7's and C_3's capacitor plates at the surface-separation line, using the unknown H variable. You then extract the unknown value of the level, obtaining both capacitive-dependent **equations**:

$$H=f\left(\frac{C_{PARTIALLYIMMERSED}}{C_{NONIMMERSED}}, L, \varepsilon_{AIR}, \varepsilon_{LAYER}, \varepsilon_{WATER}, D_{AIR}, D_{LAYER}\right).$$

From the capacitive-measurement-procedure point of view, the designed system represents a floating measurement method that implies two similar parallel-plate armatures. This method halves the parasitic capacitances that occur during measurement referred to system ground. EDN

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READERS SOLVE DESIGN PROBLEMS

Circuit provides universal ac-input-voltage adapter

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C Castro-Miguens, University of Vigo, Vigo, Spain

The input-rectifier stage of an offline power supply converts an ac-line voltage to a dc voltage, which powers a dc/dc converter. If you configure the rectifier section as a full-wave bridge for a universal mains input of 92 to 276V rms and 47 to 63 Hz, you must design the dc/dc converter to operate over a wide range of input voltages. This approach increases the cost of components and reduces the efficiency of the dc/dc converter.

For 115V-rms operation, if you configure the rectifier stage as a simple bridge, the output-voltage ripple ranges from 113 to 192V, given a ±20% tolerance on the ac input voltage (**Table 1**). Note that the voltage ripple corresponds to an effective output capacitance of 115 µF, the series equivalent of two 330-µF capacitors, and to a load of 250W. However, if you configure the rectifier stage as a voltage doubler for 115V-rms operation, the output voltage ranges from 200 to 372V—much closer to the 215 to 387V voltage ripple for 230V-rms operation.

This Design Idea proposes a rectifier stage that automatically configures itself as a voltage doubler for 115V-rms±20% line operation. **Figures 1** and **2** show the proposed rectifier stage. The STMicroelectronics (www.st.com) snubberless BTB16-600BW TRIAC (triode alternating current) is suitable for a 250W load (**Figure 1**).

For 115V-rms±20% line operation, the Reference terminal of the TL431 programmable shunt regulator has a voltage lower than its 2.5V internal reference (**Figure 2**). In this situation, the MOSFET is on, and the IL4216 optocoupler continuously fires the TRIAC.

For 230V-rms±20% line operation, the Reference terminal has a voltage higher than 2.5V, and the MOSFET and the TRIAC are off. C_1 is necessary to prevent the rectifier from starting in doubler mode when you turn on the supply with a low rectified line voltage.

This approach prevents the rectifier stage from changing from doubler mode to bridge mode during start-up, which would create a voltage drop in the bulk output capacitors that would differ from the voltage in steady-state operation. This difference would cause one of the capacitors to have an abnormally

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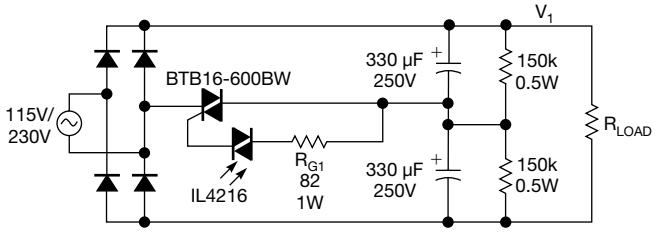

Figure 1 This ac-rectification circuit uses a TRIAC and an optocoupler to automatically switch between doubler and bridge configurations.

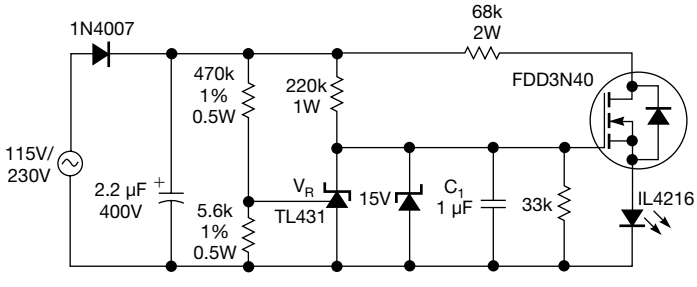

Figure 2 This control circuit uses a programmable shunt-regulator IC to sense the ac-input-voltage range.

high voltage and the other to have an abnormally low voltage.

A practical value of C_1 is 1 µF, which introduces an approximately 8-msec time delay for starting in doubler mode. You can use a 15V zener diode to clamp the gate voltage of the MOSFET. EDN

TABLE 1 200W INPUT-RECTIFIER/FILTER SECTION

	115V-rms±20% 60-Hz bridge	115V-rms±20% 60-Hz doubler	230V-rms±20% 50-Hz bridge
RMS ac-line voltage	92 to 138	92 to 138	184 to 276
Peak ac-line voltage	130 to 195	130 to 195	260 to 390
V_{1MIN}–V_{1MAX}	113 to 192	200 to 372	215 to 387

Logic probe uses two comparators

Vladimir Rentyuk, Zaporozhye, Ukraine

Measurement instruments must not affect the circuits they're measuring. A logic probe, for example, must correctly detect logic levels, and it must place no undue loads on the test circuit. The logic probe must set thresholds on automatically checking logic levels, depending on the supply voltages of the ICs it is checking. It should also not cause the checking circuit to function incorrectly.

The logic probe in a previous Design Idea suffers from loading problems (**Reference 1**). Its thresholds do not adequately depend on the supply voltages of the ICs it is checking. After some analysis, you'll find that the circuit can have an input-current range of 50 to 80 µA. Unfortunately, CMOS ICs such as NXP's (www.nxp.com) HCMOS 74HC/HCT/HCU (**Reference 2**) and Signetics' (www.signetics.com) LOCMOS HE4000 families have input current as low as ±1 µA. The HE4000 family of logic ICs has input currents of ±0.1 to ±0.3 µA. Connecting the referenced logic probe to input pins of these ICs loads the circuit under test and distorts the waveforms to the point at which you may not be able to see some problems, such as glitches, on an oscilloscope. Logic probes also have negligible input capacitance. Too much capacitance attenuates at high frequencies.

The circuit in **Figure 1** is an alternative logic probe for ICs of the 74HCxx family, for example. It comprises comparators IC_{1A} and IC_{1B}. Not every comparator will work properly in this circuit. The comparator must, for example, operate with minimal supply voltages, and it must have low input leakage current. The Analog Devices (www.analog.com) AD823AR or an equivalent comparator is a good choice.

Comparators IC_{1A} and IC_{1B} check logic-high and -low levels, respectively. The resistor-divider network comprising the 1%-tolerant, surface-mount, size-0805 R_4, R_5, and R_6 resistors sets the voltage levels, which vary in relation to the power-supply voltage. Connect the probe circuit to the same power supply that you use to power the circuit under test, allowing the comparator voltages to track the circuit's power supply. Green LED_1 and red LED_2 indicate logic-high and -low levels, respectively. If the input voltage is between those levels, neither LED will illuminate. **Table 1** highlights the logic-level voltages for the 74HCxx family of ICs, and **Table 2** shows the voltage levels for the 4000 series ICs.

The input current of the AD823AR is less than ±3 µA at a drain-to-drain voltage of 5V, ±6 µA at a drain-to-drain voltage of 10V, and ±9 µA at a drain-to-drain voltage of 15V. You can reduce this current by increasing the value of

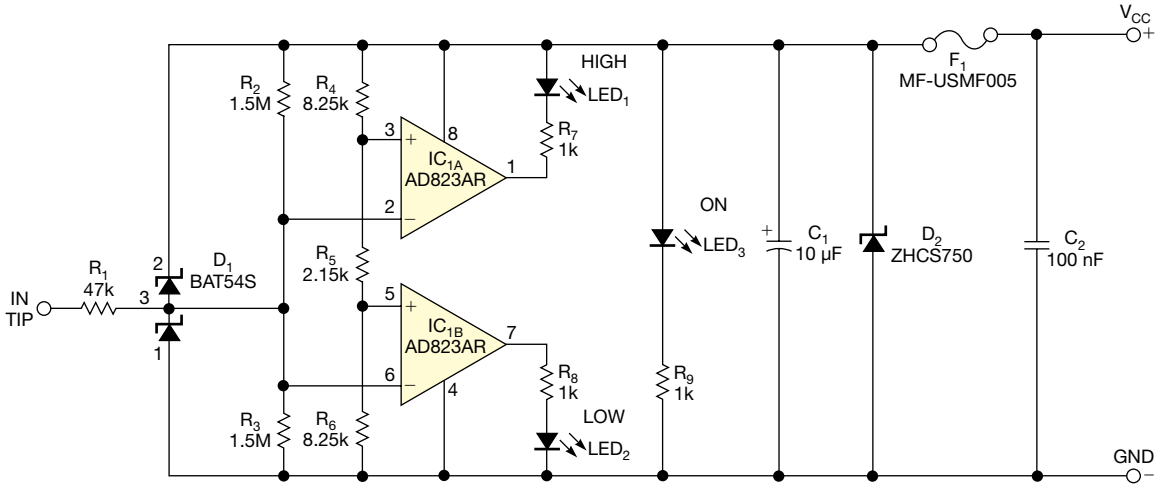

Figure 1 Two comparators and a resistor network track power-supply voltages and set logic-voltage levels.

TABLE 1 LOGIC-LEVEL VOLTAGES FOR 74HCXX FAMILY

Parameter	Symbol	Value (V)	Threshold (V)	Value (V)	Threshold (V)
DC-supply voltage	V_{CC}	4.5		6	
Low-level input voltage	V_{IL}	2.1	1.99	2.8	2.65
High-level input voltage	V_{IH}	2.4	2.51	3.2	3.35

Note: Thresholds were chosen on the basis of typical logical levels for ICs in the 74HCxx family.

TABLE 2 LOGIC-LEVEL VOLTAGES FOR 4000 FAMILY

Parameter	Symbol	Value (V)	Threshold (V)	Value (V)	Threshold (V)	Value (V)	Threshold (V)
DC-supply voltage	V_{CC}	5		10		15	
Low-level input voltage	V_{ILMAX}	1	0.93	2	1.86	2.5	2.51
High-level input voltage	V_{IHMIN}	4	4.3	8	8.61	12.5 8.25	11.62

Note: R_4, R_5, and R_6 are 6.2, 30, and 8.25 kΩ, respectively.

resistors R_2 and R_3, which are 1.5 MΩ in **Figure 1**.

The network comprising R_1 and D_1, two BAT54S Schottky diodes, protects the logic-probe circuit from overvoltage at its input, from ESD (electrostatic discharge), and from signals of negative polarity. Yellow LED_3 indicates when the logic-probe circuit and the circuit under test start up. The yellow LED is useful if you connect the probe to the circuit under test with crocodile clips. This approach ensures that both the probe and the test circuit are always on. D_2 and resettable fuse F_1, an MF-USMF005, which has a hold current of 0.05A and which comes in a surface-mount package, protect the probe circuit from improperly powering up. Tantalum capacitor C_1, in size A or B, and ceramic capacitor C_2, in size 0805, prevent the test circuit from influencing power for the logic probe. R_1 minimizes the influence of input capacitance on this logic probe.

The logic-level thresholds automatically depend on the supply voltages (**tables 1** and **2**). You can use this logic probe with other ICs, such as the 74HCU, 74HCT, or 4000 series. You can freely select the value of R_6. You can also calculate the value of R_5 and R_4 using $R_5=V_H/(V_L/R_6)-R_6$ and $R_4=V_{DD}//(V_L/R_6)-R_6-R_5$, where V_{DD} is the supply voltage of the device, V_H is the threshold for checking the high logic level for the chosen supply voltage, and V_L is the threshold for checking the low logic level for the chosen supply voltage. EDN

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1 Baddi, Raju R, "Logic probe uses six transistors," *EDN*, Dec 15, 2010, pg 46, http://bit.ly/n24oau.

2 "HCMOS family characteristics," NXP Semiconductor, March 1988, http://bit.ly/npckkN.

DAC fine-tunes reference output

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Data converters must have a stable reference voltage to accurately measure or generate analog signals. Such references offer many guaranteed levels of precision and stability. Their variety of output-voltage levels is much smaller, which manufacturers specify as standard values, such as 2.048, 2.500, or 4.096V. You sometimes need to dynamically calibrate the reference, fine-tune its output value, or generate a slightly different value. For instance, when you measure a voltage with a resistive divider, you could adjust the reference voltage to compensate for an error in the divider.

You can adjust any three-terminal voltage reference using a resistor, a current sink/source, and a buffer amplifier (**Figure 1**). Sinking or sourcing current causes the resulting voltage drop across R_1 to subtract from or add

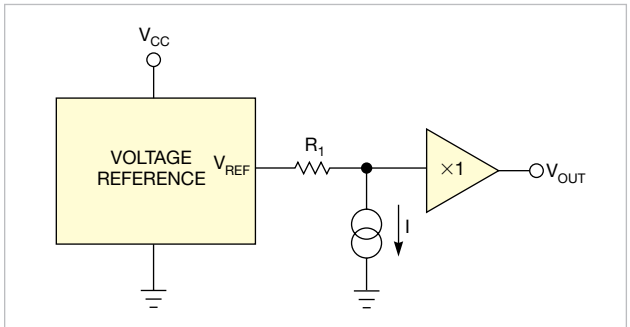

Figure 1 Adding a resistor, a current source, and a buffer to a voltage reference lets you adjust its output.

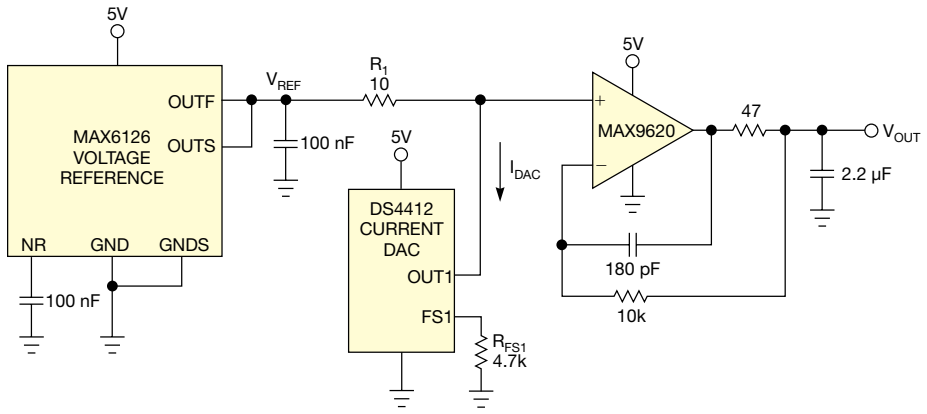

Figure 2 You can implement the idea of Figure 1 with three ICs.

to the nominal reference output, V_{REF}:

$$V_{OUT}=V_{REF}-I\times R_1.$$

The buffer amplifier isolates V_{OUT} from the load, so the only current flowing through R_1 is that from the current source. You can implement this idea with a highly stable voltage reference, a current DAC, and a low-offset op amp (**Figure 2**). If you choose a value of 4.7 kΩ for R_{FS1}, the full-scale DAC current is 0.981 mA, as the data sheet states. With a value of 10Ω for R_1, this current value yields a tuning range of ±0.981 mA×10Ω=±9.81 mV, divided into 31 steps of 0.654 mV each.

Depending on the performance grade of the reference and its package, the initial output accuracy can be as high as ±0.02%. The DAC's output-current accuracy is only ±6%, but the tuning range is small, so the large tolerance has only a small effect on the output error. Combining these values with a 1% resistor tolerance for R_1 and the maximum offset value for the op amp yields the following **equation** for the maximum initial output-voltage error:

$$0.0002\times V_{REF}+\sqrt{0.06^2+0.01^2}\times|I_{DAC}|\times R_1+V_{OFFSET}.$$

If you use a 2.048V reference, the following **equation** calculates the error:

$$0.4096\ \text{mV}+0.5969\ \text{mV}\times\frac{|\text{DAC}|}{15}+10\ \mu\text{V},$$

where DAC represents the DAC's decimal equivalent-output value (−15≤DAC≤15). Thus, the DAC introduces a maximum error of 0.5969 mV, yielding a total of roughly 1 mV when you combine it with the initial accuracy of the voltage reference itself.

Because the DAC has an operating-temperature range of −40 to +85°C, you use the voltage reference's drift specification in that same range, ±3 ppm/°C. IC makers often use the box method to specify temperature drift (**Reference 1**). You can then calculate this maximum reference-voltage drift over the temperature range of −40 to +85°C:

$$125°\text{C}\times\pm3\ \text{PPM/°C}\times2.048\text{V}=\pm0.768\ \text{mV}.$$

The drifts in the DAC, R_{FS1}, and of R_1 cause the drift in the second term ($I_{DAC}\times R_1$). The IC vendor specifies drift in the DAC as a typical value of ±75 ppm/°C. You assume ±25 ppm/°C for the resistors. These values yield a typical drift:

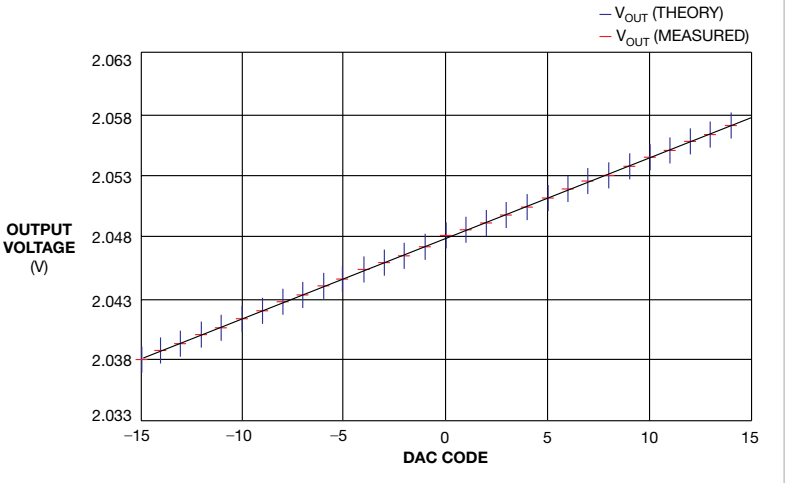

Figure 3 You can examine the theoretical (blue line) and measured (red bars) output voltage as a function of DAC code. The nominal reference output is 2.048V. Error bars show that the accuracy drops slightly toward the absolute higher values of DAC code. The graphic omits error bars for the voltage meter.

$$\sqrt{(125°C\times\pm75\ PPM/°C)^2+(125°C\times\pm25\ PPM/°C)^2+(125°C\times\pm25\ PPM/°C)^2}\times I_{DAC}\times R_1=\pm0.102\ mV\times\frac{DAC}{15}.$$

The DAC and the resistors typically introduce only roughly ±0.1 mV of drift, which is substantially lower than the maximum drift of the voltage reference. The IC vendor specifies the op amp's maximum input offset over temperature as 25 µV—also much lower than the maximum drift of the voltage reference. You can examine the DAC's output voltage as a function of its input code, using error bars to indicate the initial accuracy and temperature drift (**Figure 3**). The error increases slightly for the higher DAC values, mostly due to temperature drift. The measured values are at room temperature and are close to the theoretical values. EDN

REFERENCE

1 Fry, David, "Calculating the Error Budget in Precision Digital-to-Analog Converter (DAC) Applications," Application Note 4300, Maxim Integrated Products, Sept 25, 2008, http://bit.ly/rtE0TR.

LEDs indicate sound level

Stephen Kamichik, Ile Bizard, PQ, Canada

This Design Idea describes a battery-operated, portable sound-level meter (**Figure 1**). Its portability makes it useful for detecting the source of noise in automotive engines and power trains, factory machinery, and residential HVAC (heating/ventilation/air-conditioning) systems.

Resistor R_1 biases the condenser microphone. C_1 couples R_1 to transistor Q_1. Q_1 and R_2 through R_5 form a self-biasing common-emitter amplifier. Resistor R_5 provides negative feedback. Shunt capacitor C_2, in parallel with R_5, increases the amplifier's voltage gain. The input resistance of the amplifier is equal to $(R_2R_3)/(R_2+R_3)$.

In this circuit, the input resistance is 10.8 kΩ. Capacitor C_3 limits the high-frequency response of the amplifier. Capacitor C_5 is a filter capacitor. Capacitor C_4 couples the output of the amplifier to the load, P_1.

IC_1, a 5V positive-voltage regulator, regulates the 9V battery supply to 5V for IC_2, an LM3915 dot/bar-display driver. IC_2 senses analog voltage levels and drives LED_1 through LED_{10}.

In the sound-level-meter circuit, IC_2 provides a logarithmic 30-dB display. IC_2 also contains an adjustable voltage reference and an accurate 10-step voltage divider.

The high-impedance input buffer accepts signals from ground to within 1.5V of the positive supply. You set the sound-level meter to bar mode by connecting Pin 9 to Pin 3. Pin 3 is the V+ pin of IC_2 and connects to IC_1's Pin 3, which is the device's output voltage. Potentiometer P_1 functions as a sensitivity control. Resistor R_6 sets the voltage reference for IC_2. EDN

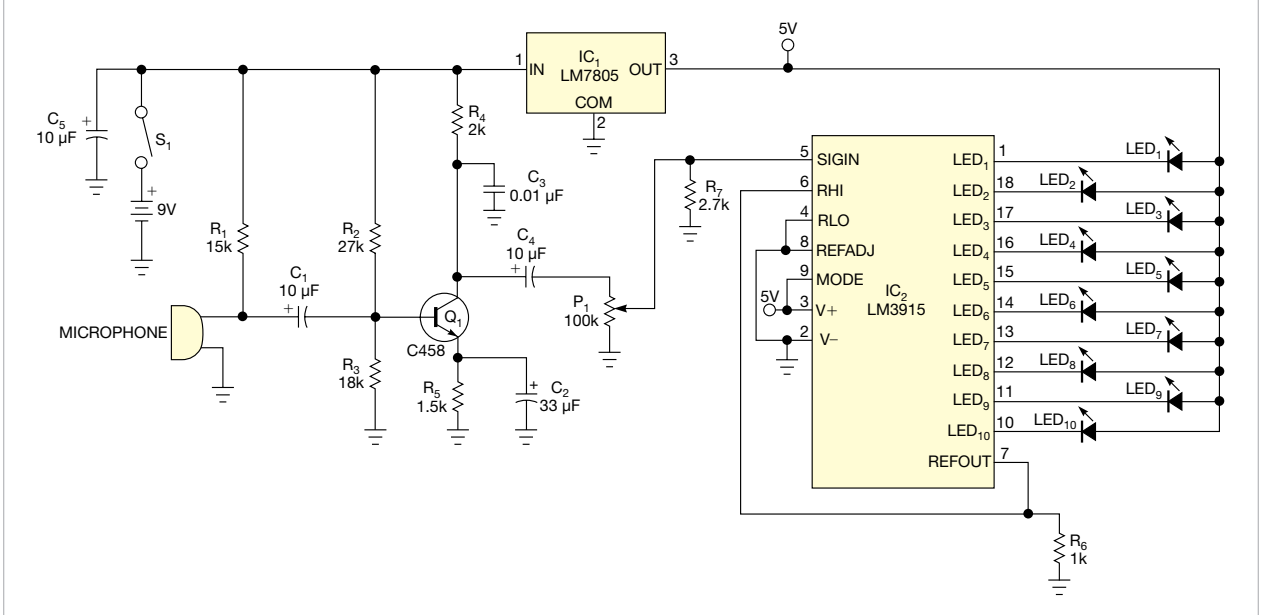

Figure 1 This sound-level meter uses an LM3915 LED driver.

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READERS SOLVE DESIGN PROBLEMS

Polynomial rotation accelerates CRC calculations

Josef Valasek, AWOS, Pardubice, Czech Republic

Engineers commonly use two methods of CRC (cyclic-redundancy-check) calculations. One method uses shift registers, and the other uses precalculated CRC values. The first method shifts the data bit by bit, and, depending on the bit value, a polynomial divides the bits. **References 1** and **2** explain this method in detail. You can find assembly-language procedure codes for 8- and 16-bit calculations in **references 1**, **3**, and **4**.

THIS IDEA INTRODUCES A METHOD OF CRC CALCULATION THAT ROTATES A POLYNOMIAL INSTEAD OF SHIFTING DATA.

References 1, **3**, and **4** describe procedures that use just a few bytes of program memory, but they work slowly. When you study procedure codes, you'll find that shifts and cycles use more than 70% of execution time, whereas the CRC calculation uses less than 30%. **Listings 1** and **4**, which are available at www.edn.com/110908dia, show simpler and faster procedure codes for 8- and 16-bit CRC calculations, respectively, for 8051 microcontrollers.

The second method for CRC calculations uses the table of precalculated CRC values. **References 1**, **3**, and **4** contain links to 8- and 16-bit assembly-language procedure codes, respectively. The procedures work quickly, but they consume many bytes of program memory, which can cause a problem if you use a microcontroller with little program memory.

This Design Idea introduces a method of CRC calculation that rotates a polynomial instead of shifting data. You know the polynomial's value before you write the procedure's code. Therefore, you can prepare polynomial values and write them into the procedure code as constants. Online **figures**, also available at www.edn.com/110908dia, show the principle of the method.

The method exclusive-ORs the data with the old CRC value and places the result to bits 7 to 0 of a 16-bit register. Each calculation has eight steps. In each step, a polynomial value shifts one bit to the left, and the code tests one bit of the register. The results of the tested bit determine whether the code performs or skips the polynomial division. The resulting CRC value is subsequently written to bits 15 to 8 of the register. When all steps are complete, bits 15 to 8 of the register comprise a new CRC value. The lowest significant bits of the register remain unused after testing. You can use these dormant bits in the register to store result bits by modifying the method using polynomial rotation instead of a polynomial shift. **Listings 2** and **5** show this procedure for 8- and

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TABLE 1 COMPARISON OF 8-BIT CRC-CALCULATION PROCEDURES

Method	Procedure code	Code length (bytes)	Minimum/maximum execution times (µsec)
Shift-register simulation	Reference 3, calculation method	26	119/127
	Reference 1, Example 1	28	120/128
	Listing 1	15	45/53
Polynomial rotate	Listing 2	45	20/28
Look-up table	Listing 3	265	8/8

TABLE 2 COMPARISON OF 16-BIT CRC-CALCULATION PROCEDURES

Method	Procedure code	Code length (bytes)	Minimum/maximum execution times (µsec)
Shift-register simulation	Reference 4, calculation method	26	92/124
	Reference 1, Example 4	37	156/180
	Listing 4	23	77/101
Polynomial rotate	Listing 5	57	22/36
Look-up table	Reference 4, table method	550	40/40
	Reference 1, Example 5	533	16/16
	Listing 6	530	14/14

16-bit CRC calculations, respectively. These routines perform only bit-testing and polynomial-dividing instructions.

Tables 1 and **2** highlight calculation procedures for 8- and 16-bit calculations, respectively, using this method. The **tables** describe execution times for a standard 12-clock 8051 core with a 12-MHz crystal. The code lengths and execution times of procedure codes come from **Reference 1**; **references 3** and **4** calculate without saving or restoring the procedure's working registers.

You should properly set the initial CRC value before starting CRC calculation. Some communication protocols, such as the one in **Reference 2**, use an initial CRC value other than 00 Hex. **Listings 7** through **10** show the procedure codes for 8- and 16-bit CRC calculation with PIC (www.microchip.com) microcontrollers. EDN

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2 *MODBUS over Serial Line Specification and Implementation Guide*, Version 1.02, Modbus Organization, December 2006, pg 39, www.modbus.org/specs.php.

3 Wren, John C, "A CCITT-8 CRC calculator," www.8052.com/codelib.htm.

4 Wren, John C, "A CCITT-16 CRC calculator," www.8052.com/codelib.htm.

Simple circuit measures optocoupler's response time

Peter Demchenko, Vilnius, Lithuania

You can use the circuit in this Design Idea to measure the attack and release times of photoresistor-type optocouplers (**Figure 1**). Such devices often find use in audio compressors or volume-control circuits. The design uses an oscillating Schmitt trigger with the optocoupler DUT (device under test) in the feedback loop. The photoresistor and resistor R_1 form a voltage divider that controls the input of the Schmitt trigger. The optocoupler's LED connects to the trigger output. You can measure the duration of the output pulses with an oscilloscope or a digital meter. The duration of the negative output pulses is equal to the switching on-time, or attack time. The duration of the positive pulses is equal to the switching off-time, or release time. The attack and release times depend on the value of R_1; you can

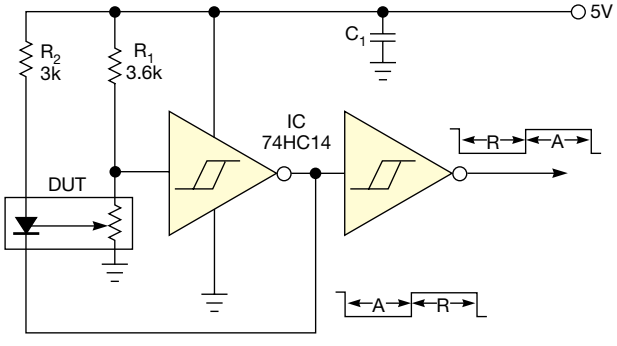

Figure 1 You can determine an optocoupler's rise and fall times by incorporating a photoresistor in the feedback loop of an oscillator circuit.

observe both by varying the value of R_1. With the component values in **Figure 1**, the durations of the output pulses are a 0.15-msec attack time and a 2.7-msec release time.

During oscillation, the resistance of the photoresistor sweeps in from R_{P1} to R_{P2}. The circuit sweeps these photoresistor values according to R_1, the power-supply voltage, and the Schmitt-trigger thresholds, as the following **equations** show: $R_{P1}=R_1\times V_{T2}/(V_{CC}-V_{T2})$, and $R_{P2}=R_1\times V_{T1}/(V_{CC}-V_{T1})$, where V_{T1} is the positive-going threshold voltage and V_{T2} is the negative-going threshold voltage of the Schmitt trigger.

In the case of the 74HC14 logic family, you can determine the thresholds from the data sheet and your power-supply voltage, according to the following **equations**, which yield typical values: $V_{T1}=0.53\times V_{CC}$, and $V_{T2}=0.31\times V_{CC}$. Using 5V as a power-supply voltage and solving the following **equations**, you can determine the photoresistor range: $R_{P1}=0.45\times V_{R1}$, and $R_{P2}=1.13\times V_{R1}$.

This approach lets you pick a value for R_1 so that the photoresistor range is suitable for your device. You can also vary the value of resistor R_2 to observe the LED-current-to-attack-time characteristic of the DUT but not affect the release time. Note that R_2 limits the current through the LED; if its value is too large, oscillation will not occur.

Using this circuit allows you to match custom optocouplers comprising green, superbright LEDs and an MPY7P photoresistor. A recent Design Idea, although thorough, lacked data on response time (**Reference 1**). EDN

REFERENCE

1 Foit, Julius, and Jan Novák, "Photoresistor provides negative feedback to an op amp, producing a linear response," *EDN*, May 27, 2010, pg 49, http://bit.ly/oPQMfo.

Circuit provides visual verification of IR pulses

Michael J Gambuzza, General Electric Measurement and Control Solutions, Billerica, MA

You can test an IR (infrared) link with a circuit that converts an IR-generated photocurrent to an amplified current that drives a standard LED. This approach provides a visual feedback to indicate that the transmitter is working. The circuit can be enclosed in a small plastic or metal box and requires just a 9V transistor battery for operation. Diode D_1 is a basic Everlight (www.everlight.com) PD333-3C/H0/L2 or equivalent IR photodiode in a T1¾ package.

You can configure amplifier IC_{1A} as a photovoltaic amplifier. When the IR-light energy impinges on photodiode D_1, it generates a small photocurrent that tries to pull the inverting input negative. Meanwhile, the output of IC_{1A} goes positive, maintaining the virtual-ground node on Pin 2 of the amplifier at 0V. The transfer function for the circuit is $V_{OUT}=I\times R_1$. If you set the gain high, IC_{1A} goes to the power-supply rail when the circuit detects light. Analog Devices' (www.analog.com) AD823AR JFET-input amplifier directly drives the LED through a 750Ω current-limiting resistor. C_1 compensates the amplifier, preventing it from oscillating due to capacitive load from D_1 and the input parasitic capacitance.

If the output of IC_1 oscillates, you may need to increase the value of C_1. You can determine the value of C_1 by using the following **equation** for a 45° phase margin: $C_1=\sqrt{(C_D/2\pi R_1 F_C)}$, where F_C is the unity-gain-crossover frequency of IC_{1A}—typically, 16 MHz for the AD823—and C_D is D_1's 0V junction capacitance, including any parasitic capacitance on that node. Adjust R_1 for optimum gain. For testing, the remote-control transmitter window should be as close as possible to photodiode D_1 for maximum signal transfer. EDN

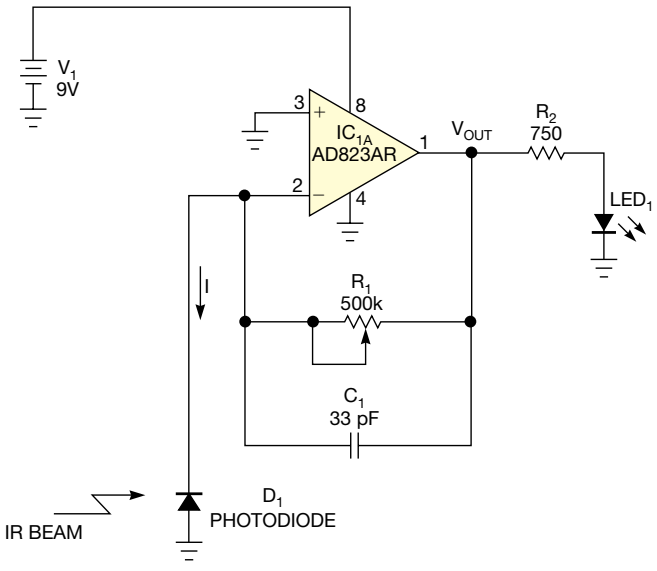

Figure 1 This circuit detects the transmitter in an IR communication link and provides a visual output from the LED.

An LED's intrinsic capacitance works in a 650-mV LRC circuit

Sajjad Haidar, University of British Columbia, Vancouver, BC, Canada

You can use the inherent capacitance of an LED to make a series resonant boost circuit that can create a voltage large enough to light the LED. Depending on the color of the LED, you need a voltage higher than 1.6V to turn it on. The threshold, or knee, voltage rises higher as the LED wavelength becomes shorter. All PN-junction diodes, including LEDs, have capacitance due to depletion and diffusion profiles.

You can light an LED using its capacitance in a series LRC (inductance/resistance/capacitance) resonant circuit. In such a circuit, the Q factor determines the multiple of the generator voltage that appears across LC. If you fashion a circuit with a high enough Q factor, you boost the generator voltage enough to light the LED. The Q factor of the resonant circuit is a function of the resistance, inductance, and capacitance, as the following **equation** shows: $Q=(1/R)\sqrt{(L/C)}$.

You can verify this calculation with a simple circuit using a blue LED in series with an inductor (**Figure 1**). The knee voltage of the LED is 2.45V, and the signal generator has an internal resistance of 50Ω. An inductance of 100 µH and the 50-pF capacitance of a typical LED yield a Q of 28. The amplitude of the sinusoidal signal generator is set at 650 mV p-p. You can then vary the generator's output frequency until you see the circuit's resonant point. As the circuit approaches the

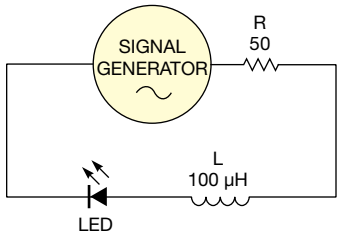

Figure 1 In this LRC circuit, the resistance is the source resistance of the sine-wave generator. The LED provides the capacitance.

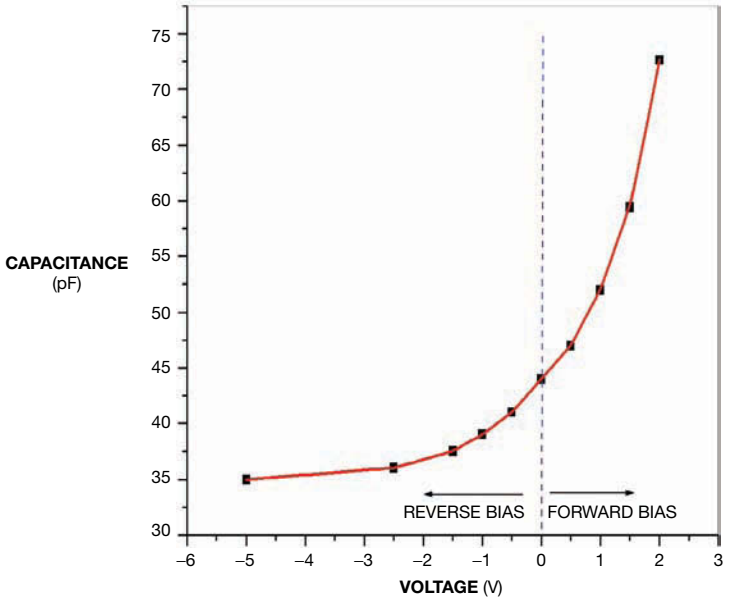

Figure 2 The junction capacitance of an LED increases as you go from a reverse bias of –5V to a forward bias of 2V.

resonant frequency, the voltage across the LED starts to increase. The resonant point manifests itself as a small jump in voltage, rather than a smooth progression, due to a positive feedback at resonance. The positive feedback happens because the capacitance of any PN-junction device is not linear (**Figure 2**). As the circuit approaches the resonant frequency, the LED voltage increases, which also increases the LED capacitance, resulting in lower resonant frequency.

For a blue LED, the voltage waveform as the circuit approaches resonance is 1.55 MHz. The circuit settles at 1.69 MHz (**Figure 3**). The forward-biased LED is thus emitting light, clipping the positive parts of the boosted waveform. Using the same 650-mV-p-p generator amplitude on other colors of LEDs produces different resonant frequencies. You can see a similar effect with a square-wave generator because it also contains the fundamental components of the resonant frequency. EDN

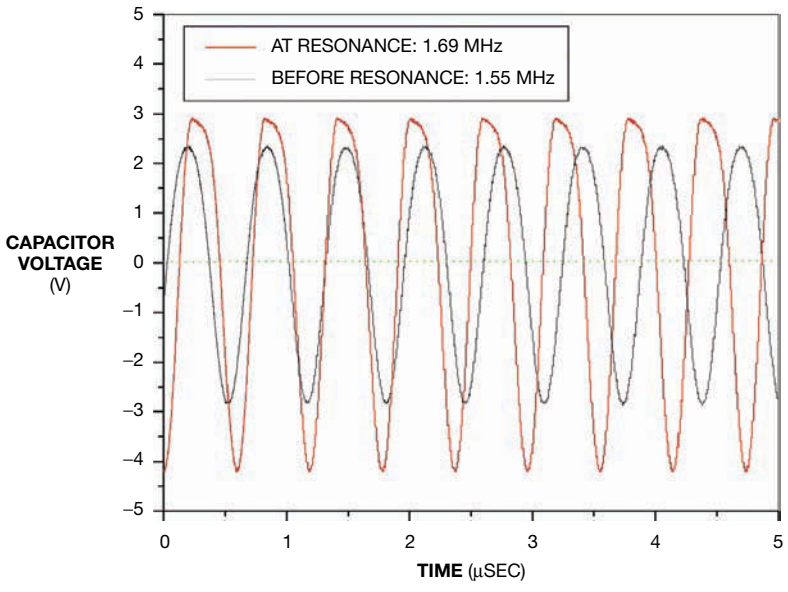

Figure 3 The effect of the LED capacitance increasing with applied voltage means the circuit will jump to a frequency as you approach the resonant point.

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Eight LEDs make a 100-division voltmeter

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The circuit in this Design Idea makes a voltmeter that reads to 0.99V. The idea uses a counter IC to drive two sets of four LEDs (**Figure 1**). Each of these two sets represents a BCD (binary-coded-decimal) value. With all of the LEDs off, the voltmeter reads 0V. With all of the LEDs on, the reading is 0.99V. Op amp IC_{1A} generates a predictable voltage ramp.

You use op amp IC_{1B} as a comparator to compare the ramp to an input signal. The higher the input voltage, the longer the output pulse from IC_{1B} is. You use this pulse to gate free-running oscillator IC_{2B}. A potentiometer on this multivibrator circuit allows you to adjust the full-range count. The voltmeter has a maximum input of 1V and uses three dual-part packages. You make output counter IC_3 work as a two-digit counter by strapping the enable pin of the IC_{3B} part to the MSB (most-significant-bit) output of the IC_{3A} part.

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A dual op amp is used to create the comparator function and the ramp generator. The design also uses a dual 555-type timer chip. You use IC_{2A} to

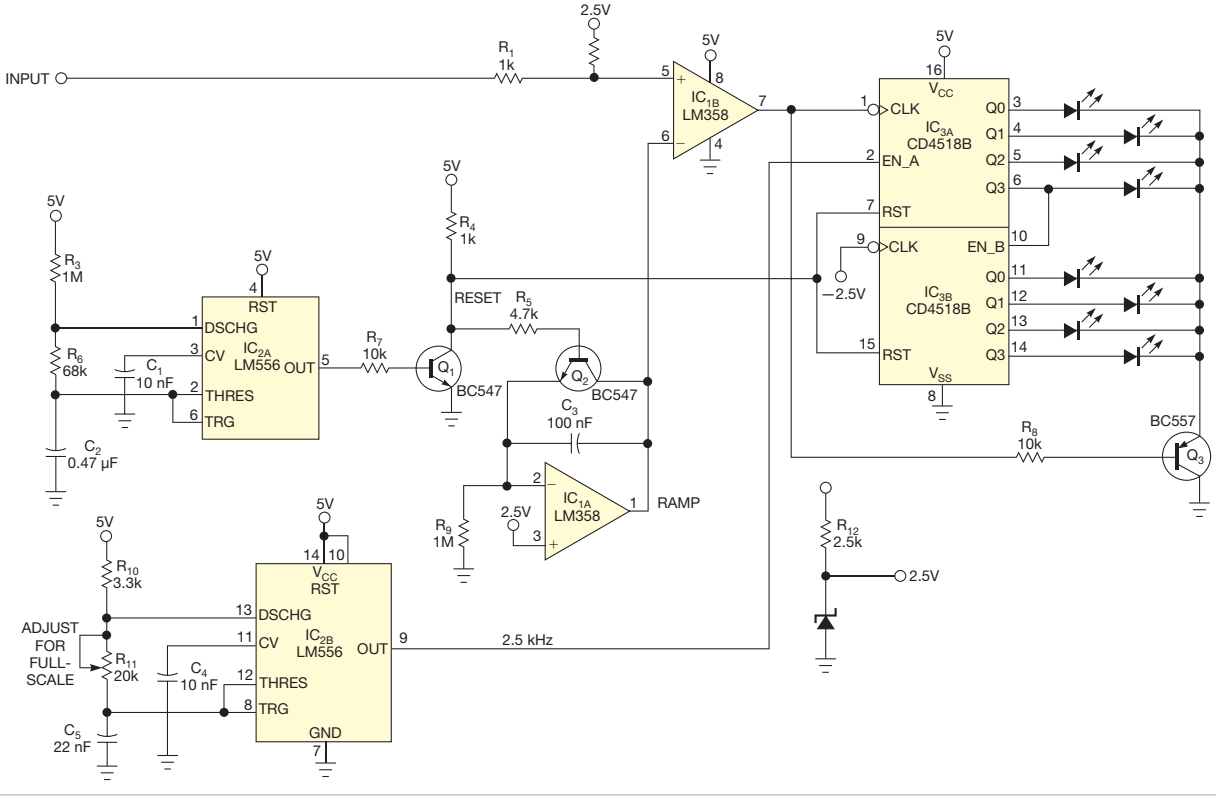

Figure 1 This 100-division voltmeter uses three simple chips.

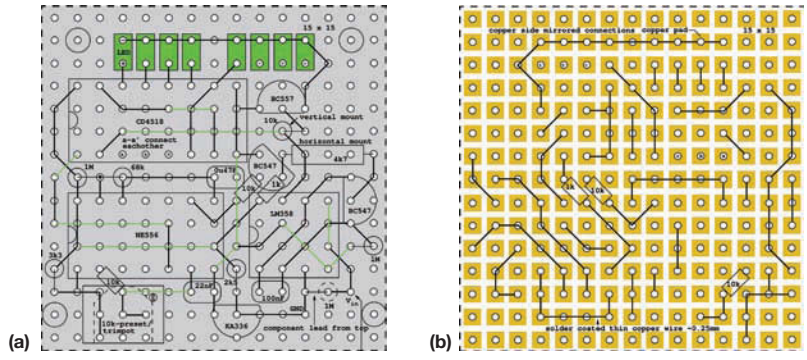

Figure 2 A top view of a 15×15-hole prototype board shows component placement and connections on the top (green) and bottom (black) for the voltmeter circuit (a). A bottom view of the board shows the connection on the bottom, along with three resistors (b). For a full-size view of this figure, go to www.edn.com/110922dia.

create the ramp and to reset it and the output counter, and you use IC_{2B} as a free-running oscillator that drives the counter chip. To blank the output LEDs when the chip is counting, Q_3 disables drive current to the LEDs when IC_3 is incrementing. You use IC_4 to derive a reference of 2.5V.

Tests of the design use TL084 op amps, but you can also use an LM358. A top view of the 15×15-hole prototype board shows component placement (**Figure 2a**). **Figure 2b** shows a bottom view of the board, with the connection and three resistors. You might use flat-green LEDs with the sides painted black or covered with black-plastic sleeves for good visibility. EDN

Simple circuit controls the rate of voltage change across a capacitor or another load

Fabien Dubois, Ampere Lab, Lyon, France

The circuit in this Design Idea lets you set a well-controlled voltage rate of change, often expressed as the differential dV/dt (instantaneous rate of voltage change over time in volts per second). You can vary the sensitivity with a potentiometer. Set the dV/dt from 1V/200 nsec to 1V/3 msec. The input voltage can range from a few volts to 30V. Higher-voltage transistors can be used to increase the upper voltage limit. The circuit precharges a capacitor with a slow and controllable dV/dt to avoid a large inrush current during power-up. You can also use the circuit to create a high dV/dt for susceptibility testing on other circuits.

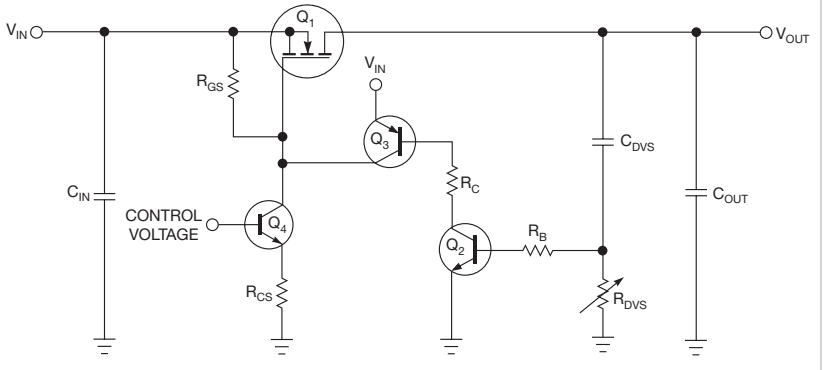

Figure 1 This circuit creates a fixed dV/dt based on the control voltage and the setting of R_{DVS}.

The circuit uses a P-channel MOSFET, Q_1, to control the rate of change of the output voltage (**Figure 1**). You drive the MOSFET with a constant-current source comprising Q_4 and R_{CS}, which feeds gate-to-source resistor R_{GS}. Applying a positive control voltage to the base of Q_4 draws a current that creates a voltage across R_{GS}. This voltage occurs across the gate and source of Q_1, turning it on. The circuit uses capacitor C_{DVS} as a sensing device of the rate of change of the output voltage. Voltage variations across C_{DVS} generate a current that creates a current proportional to the dV/dt, as the following **equation** shows:

$$I_{CS}=C_{DVS}\times\frac{dV_{OUT}(t)}{dt}.$$

Resistor R_{DVS} converts this current into a voltage signal. When that voltage reaches approximately 0.67V, it turns on Q_2, which turns on Q_3. The current that Q_3 supplies from the input tends to lower the Q_1 gate-to-source voltage and reduces its drive. You use R_B to limit the base current of Q_2. This servo action puts the gate-to-source voltage of the MOSFET in the Miller plateau, a constant-current region of the FET's characteristic curve. The FET has an internal Miller capacitance, C_{GD}, between the gate and the drain pins.

TABLE 1 CIRCUIT PART NUMBERS

Component	Description	Manufacturer	Part no.
C_{IN}	10-µF, 50V tantalum capacitor	AVX	TPSE106K050R0500
C_{OUT}	1-µF, 50V ceramic capacitor	AVX	12065C105KAT2A
C_{DVS}	10-nF, 50V ceramic capacitor	AVX	08055C103KAT2A
Q_2 and Q_4	40V, 0.6A NPN transistor	On Semiconductor	MMBT2222ALT1G
Q_3	60V, 1.2A PNP transistor	On Semiconductor	MMBT2907ALT1G
Q_1	100V, 4A power MOSFET	Vishay	IRF9510SPBF
R_B	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_C	1-kΩ, 0603, 1% resistor	Vishay	CRCW12061K00FKEA
R_{CS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA
R_{DVS}	10-kΩ trimming potentiometer	Bourns	3362W-1-503LF
R_{GS}	10-kΩ, 0603, 1% resistor	Vishay	CRCW120610K0FKEA

The circuit's constant-current source controls the charge current of this Miller capacitance. As transistor Q_3 injects current to the gate, Miller current I_{GD} decreases and the slope of the output voltage decreases accordingly, as the following **equation** shows:

$$\frac{dV_{dS}(t)}{dt} = \frac{I_{GD}}{C_{GD}}.$$

The feedback loop keeps the dV/dt ratio constant. The rate of change of the output voltage is a function of the base-emitter voltage of Q_2, R_{DVS}, and C_{DVS}, as the following **equation** shows:

$$\frac{dV_{OUT}(t)}{dt} \simeq \frac{V_{BEQ1}}{R_{VDS} \times C_{DVS}}.$$

You can build the circuit with the part numbers in **Table 1**. EDN

LED bar-graph display represents two digits

Ajoy Raman, Bangalore, India

This circuit uses two National Semiconductor (www.national.com) LM3914 dot/bar-display-driver ICs to implement a two-digit, 0 to 5V LED voltmeter that mimics a subranging flash ADC. An LED bar graph comprising five LEDs, each representing 1V of input signal, represents the MSD (most-significant digit). Nine LEDs in dot mode, in which only one LED lights, represent the LSD (least-significant digit). The circuit senses the operation of the MSD LEDs and uses them to change the input reference ladder of the chip that drives the LSD. The input signal ranges from 0 to 5V, and accuracy is better than ±50 mV. The circuit operates over a supply voltage range of 5 to 8V.

R_1 and R_2 divide the input voltage in half, such that a 5V maximum input is 2.5V at the LM3914s, IC_1 and IC_2 (**Figure 1**). You strap the mode pin of IC_1 high, so it operates as a bar graph, and use V_{R1} to adjust the REFOUT pin of IC_1 to 2.5V. Thus, each of the IC_1 output pins lights successively in 0.5V increments. Because this IC makes the MSD, you wire in only five LEDs on every other output, starting at output D_2, meaning that the five LEDs will light at 1V intervals from 1 to 5V. The LM3914's data sheet explains how you can use R_3 to set a constant-current output on the LED pins (**Reference 1**). The current in each LED is approximately 10 times the current that you draw from the REFOUT output pin. The part maintains 1.25V between the REFADJ and REFOUT pins. The $V_{R2}/R_{10}/R_{13}$ voltage divider causes a load, which, along with the 1.5-kΩ value of R_3, sets a fixed output current in LEDs D_1 through D_5. You should select these LEDs from the same batch so that their forward voltage drops match.

You then wire a resistor and a transistor around each of the four LEDs. The voltage across the LED also presses across the resistors, so these LEDs form four constant-current sources that operate in conjunction with the LEDs. Adjust V_{R3} such that each LED when on

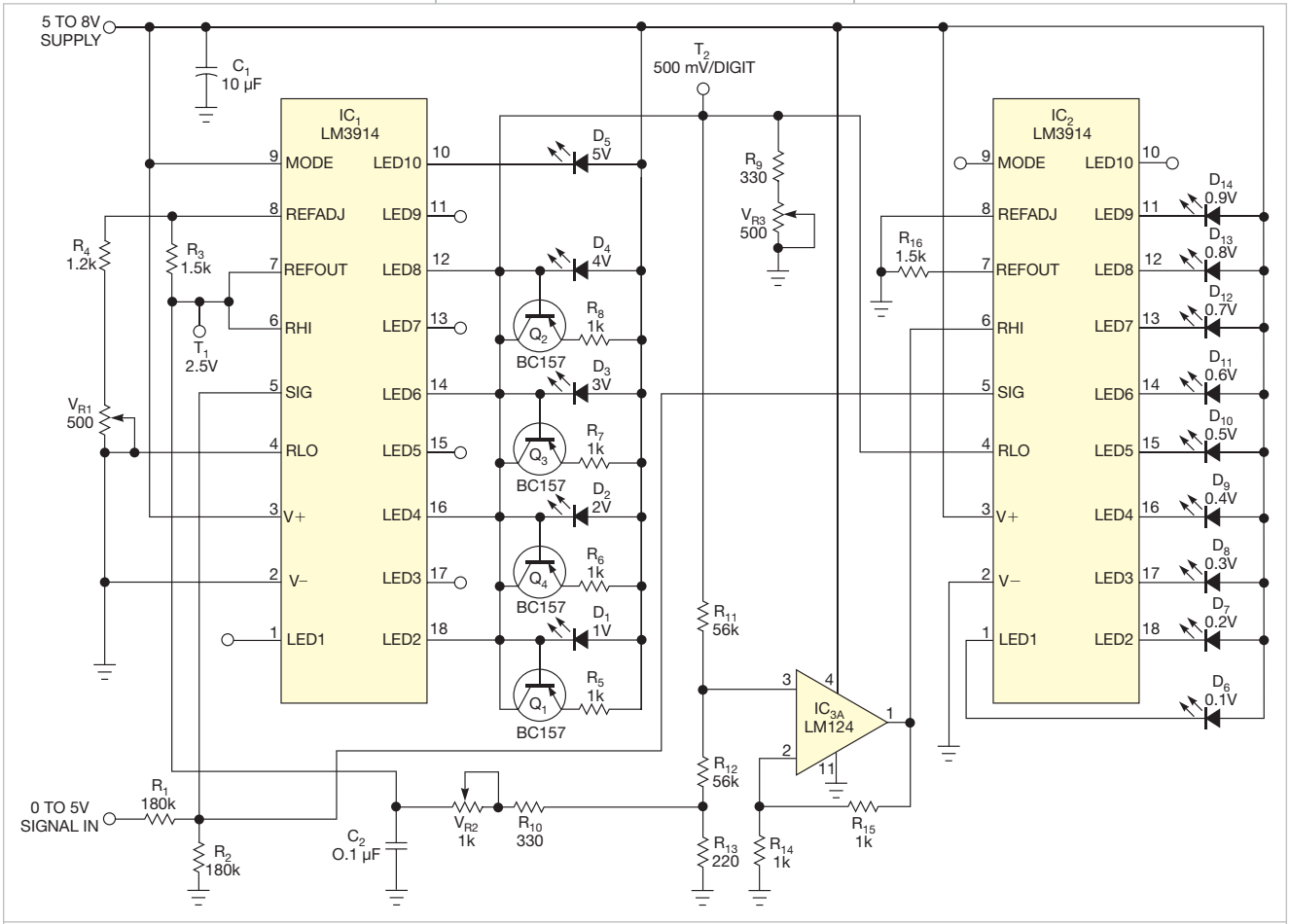

Figure 1 This voltmeter displays 1 to 5V as a bar graph from IC_1. A dot display from IC_2 represents the least-significant digit, with the LEDs representing 0.1 to 0.9V.

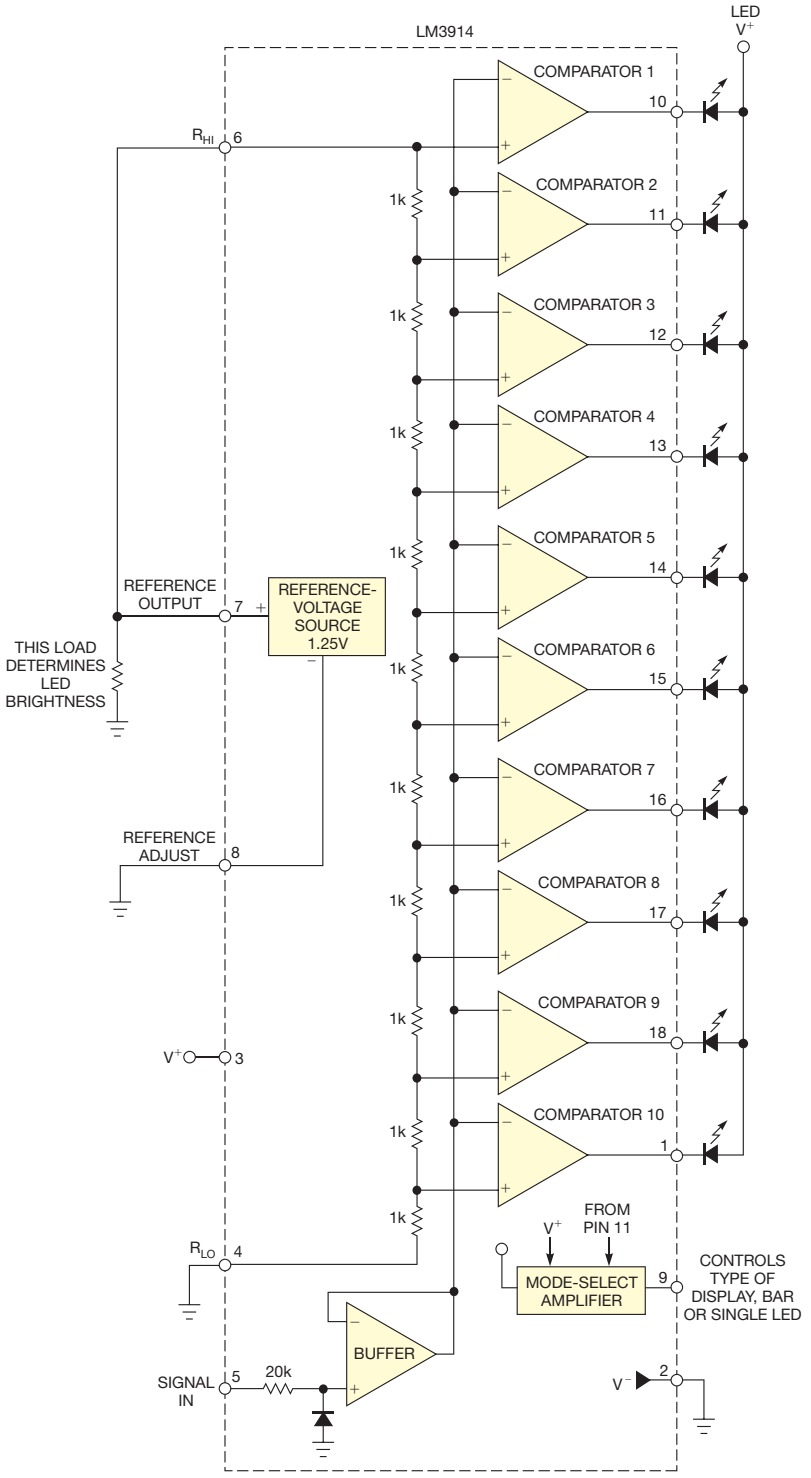

Figure 2 The LM3914 IC has an internal reference and a resistor ladder you can configure to make bar or dot LED displays (courtesy National Semiconductor).

adds 500 mV to their summed output. You send this signal to R_{LO}, the bottom of the internal resistor string in the second LM3914 (**Figure 2**). You then send the 50%-divided input signal to the SIG Pin of IC_2. Use an op amp, IC_3, to add a fixed 500-mV offset plus the summed-current signal from the outputs of IC_1. R_1 and R_2 reduce the input signal to the circuit by 50%, so a 500-mV excursion at IC_2's SIG Pin input represents 1V of the input excursion.

LEAVE THE MODE PIN ON IC_2 FLOATING SO THAT THE PART OPERATES IN DOT MODE, NOT BAR MODE.

As the input to the circuit goes from 0 to 1V, the SIG inputs to both bar-graph ICs go from 0 to 0.5V. No LEDs light on IC_1, meaning that IC_2 has R_{LO} at 0V and R_{HI} at the 500-mV offset you adjusted with V_{R2}. The LED outputs of IC_2 now light in sequence as the input to the chip goes from 0 to 0.45V, corresponding to a 0 to 0.9V input at the Signal-in Port. When the input signal is high enough to light LED D_1, the value at IC_2's R_{LO} jumps to 500 mV, and the input at R_{HI} jumps to just 500 mV higher than R_{LO}, or 1V. Because IC_2's internal resistor ladder is now biased between 0.5 and 1V, IC_2 indicates 0.1V steps between 1 and 2V at the Signal-in Port. Leave the Mode Pin on IC_2 floating so that the part operates in dot mode instead of bar-graph mode.

At a 4.9V input to the Signal-in Port, LEDs D_1 through D_4 illuminate, resulting in 2V at the R_{LO} input of IC_2. The op amp adds 500 mV to that value and presents it to the R_{HI} input of IC_2 for a total of 2.5V. The input to IC_2 is 2.45V, so the D_9 output of IC_2 lights D_{14}, correctly indicating the LSB (least-significant bit) of the measurement as nine-tenths. EDN

REFERENCE

1 "LM3914 Dot/Bar Display Driver," National Semiconductor, February 2003, http://bit.ly/naDCRG.

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READERS SOLVE DESIGN PROBLEMS

DYNISTOR = DIAC

Circuit controls inrush current in ac-operated power supplies

Peter Demchenko, Vilnius, Lithuania

Large power supplies that operate from ac wall voltage have large input-filter capacitors. You must limit the inrush current to those capacitors. Otherwise, the supply may trip the ac circuit breaker, or you may damage the rectifier, filer chokes, or PCB (printed-circuit-board) traces. The circuit in this Design Idea inserts a current-limiting resistor in the capacitor's charging path. It senses when the capacitor has charged to a minimum threshold voltage. It then uses a TRIAC (triode alternating current) to short the resistor. Monitoring the capacitor voltage is preferable to monitoring the input current, thus avoiding large load currents during operation that can cause inrush limiting.

This circuit uses a dynistor to detect the minimum threshold voltage across the filter capacitor. Once called a Shockley diode, a dynistor is an asymmetric thyristor with an alternating P+ and N– structure in its anode. In this break-over diode, avalanche current triggers a gateless thyristor. The unidirectional dynistor differs from the bidirectional STMicroelectronics (www.st.com) Trisil, the Bourns (www.bourns.com) TISP (thyristor-surge-protector), and the Littelfuse (www.littelfuse.com) SIDACtor (silicon-diode-alternating-current) devices. Dynistors are somewhat rare, but you can still obtain a DB3 type with a 32V break-over voltage. These devices sense capacitor voltages greater than 38V. You can use PNP/NPN transistor pairs or a low-power thyristor with a zener diode to emulate a dynistor of any voltage.

A dynistor makes a 700-Hz oscillator when the capacitor reaches the threshold voltage. You can easily transmit this ac signal across an isolation boundary comprising a transformer or capacitors. If you are unsure of the isolation rating of your signal transformer, you can capacitively couple the transformer (**Figure 1**). If you use optional capacitors C_2 and C_3, their rating voltage should exceed 800V. Power resistor R_3 limits inrush current and should have a power rating greater than 2 to 10W. Resistors with integrated thermofuses are preferable. Use the ZCD (zero-crossing detector) to synchronize R_3's shorting event with the transition of the ac voltage through 0V. Parts such as Fairchild's (www.fairchildsemi.com) MOC3062M zero-crossing phototriac-driver optocoupler serve this function.

Dynistor D_1, capacitor C_1, resistor R_1, and transformer T_2 comprise an oscillator. It begins working when the value of E exceeds the value of the dynistor's break-over voltage. The oscillator provides current pulses greater than 20 mA, enough to trigger many types of TRIACs and consuming less than 1.5 mA dc. Because the frequency of pulses is approximately 700 Hz, transformer T_2 is small. Resistor R_2 limits the discharge current through dynistor D_1. If the transformer has adequate dc resistance, you can omit R_2. Choose a TRIAC with a gate-trigger current lower than 20 mA. You may not need the

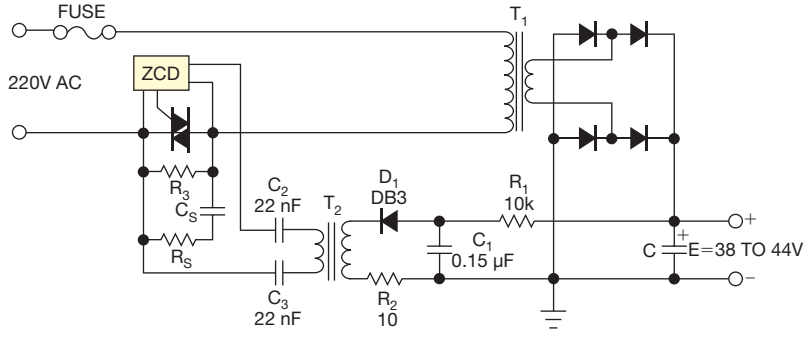

Figure 1 This circuit uses a dynistor to create a 700-Hz oscillator when the voltage on the filter capacitor reaches 32V.

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snubber network comprising R_S and C_S if the leakage inductance of T_1 and the inductance of the ac lines are low.

You can adapt the circuit for capacitor voltages greater than 45V (**Figure 2**). Feed the dynistor oscillator through a voltage divider comprising R_4 and R_5. This divider consumes 10 to 20 mA but keeps the oscillator's frequency close to 700 Hz. To avoid dc-current draw, you can use or simulate a higher-voltage dynistor. This circuit dispenses with the isolation transformer and uses capacitors C_2 and C_3. Replacing R_1 in **Figure 1** with R_{11} and R_{12} helps reduce current injection into earth ground and audio interference due to 700-Hz oscillations. EDN

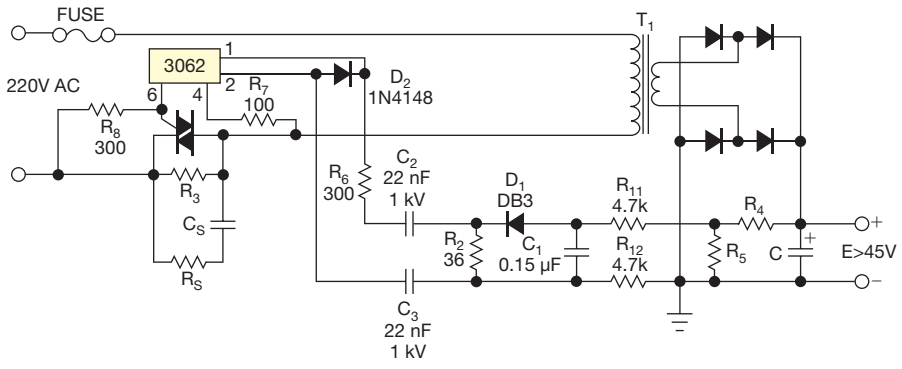

Figure 2 By using the R_4/R_5 voltage divider, you can use the same dynistor to sense capacitor voltages greater than 45V.

Save 3 dB of output power using feedback to set the output impedance

Vic Jordan, Carson City, NV

It's common practice to series-terminate an op amp to match the impedance of the load. This practice causes a 3-dB loss of output power in the termination resistance, however (**Figure 1**). Newer op amps operating on 3 and 5V have limited output swings, meaning that you should avoid using series-build-out resistors. Instead, you can use a series-feedback circuit to set the output impedance. John Wittman, then a senior staff engineer at GTE Lenkurt Electric Co, introduced this technique more than 40 years ago.

With this technique, you add 6 dB of the reciprocal feedback to set the output impedance, obtaining a return loss of more than 30 dB. You add a series-current-sensing resistor, another op amp, and a limiting resistor (**Figure 2**). This example shows a high-side sensor and an unbalanced load. The forward amplifier is designed to have twice the needed gain when unloaded. In this example, the open-circuit gain is 2.7, and the input impedance is 1Ω. The input current is 1A, with an input signal of 1V.

To match the amplifier's 1Ω load, the series-feedback circuitry must divert one-half of the input current from the negative input node of the op amp. The original 1A input current that flows through R_F then decreases to 0.5A, meaning that the output voltage is half of the open-circuit voltage. The output impedance is now 1Ω, and the series feedback is 6 dB, allowing you to match the output impedance to the load and still get almost the full voltage swing from the amplifier. You no longer waste half the output power in a series termination. This example uses a current-sense resistance value that is 3% of the output load, so power loss will be 3%. With careful design, you can lower the loss to less than 1%.

In telecommunications lines, for longitudinal balance, the impedance of both conductors to ground should be the same. Longitudinal balance protects against crosstalk and 60-Hz-induced noise. It is also important at the higher frequencies that DSL (digital-subscriber-line) service uses. Telecom companies commonly use transformers to provide longitudinal balance of 80 to 120 dB. The transformers also isolate transients, such as those due to lightning. You can apply this technique using transformer coupling and low-side current sensing

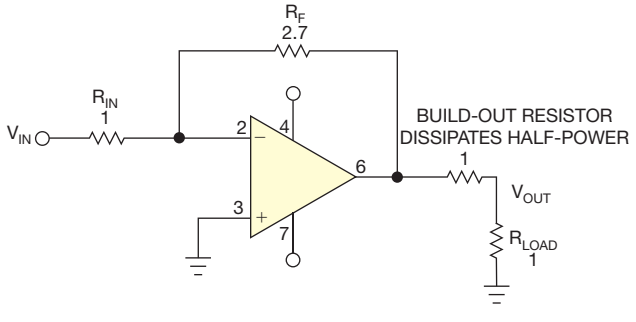

Figure 1 Using a series-termination resistor equal to the load wastes 3 dB of power and reduces the output swing by one-half.

(**Figure 3**). The design process is still the same, except that just two resistors can provide 6 dB of feedback.

You can formalize the analysis of the circuits using state **equations**. For the circuit of **Figure 2**, because the negative input of an op amp is at virtual ground, you can relate input voltage and current by inspection: $I_{IN}=(V_{IN}-V-)/1\Omega=V_{IN}/1\Omega$. You can derive a second **equation** employing the fact that the negative input of an op amp has high impedance, so the currents at that node must add to 0A.

Sum the currents at V–, except you reference the node currents back to the sense resistor, including the 0.3Ω resistor and the 0.03Ω sense resistor: $0=V_{IN}/1\Omega+V_{OUT}/2.7\Omega+0.37V_{OUT}/R_{LOAD}$. You can express the circuit function in vector and matrix terms: (I)=(**ADMITTANCE**)×(**V**). You can also expand for the appropriate states of current:

$$(I)=\begin{pmatrix}I_1\\I_2\end{pmatrix},\ \begin{matrix}I_1=I_{IN}\\I_2=0\end{matrix}$$

and then expand for the vector expression of voltage:

$$(V)=\begin{pmatrix}V_1\\V_2\end{pmatrix},\ \begin{matrix}V_1=V_{IN}\\V_2=V_{OUT}\end{matrix}$$

Plug these values into the (I)=(**ADMITTANCE**)×(**V**) **equation** and solve for (**V**):

$$(\mathbf{ADMITTANCE})=\begin{pmatrix}1 & 0\\ 1 & \frac{0.37}{R_{LOAD}}+\frac{1}{2.7}\end{pmatrix}.$$

For the circuit of **Figure 2**, the forcing function is I_1; the input current is 1A. Invert the admittance matrix and then multiply the current vector to find the voltage vector. You can use a Hewlett-Packard (www.hp.com) HP-48 calculator to do the hard work. It yields the result that V_{IN} is 1V and calculates V_{OUT} at –1.35V, one-half the unloaded gain of 2.7. You then repeat the analysis for a load resistance of 1000Ω:

$$(\mathbf{ADMITTANCE})=\begin{pmatrix}1 & 0\\ 1 & \frac{0.37}{1000}+\frac{1}{2.7}\end{pmatrix}.$$

Inverting the (**Y**) matrix and multiplying it with the I matrix, with I_1 of 1A, yields an open-load voltage vector, with V_{IN} equal to 1V and V_{OUT} equal to –2.7V, confirming that the design is correct.

Be careful writing your own equations; two dependent equations can easily lead to an incorrect answer. An HP-48 calculator solves them using the "least-squares" method, but it does not check for a determinant condition of zero to warn you of nonindependent equations. You can use the HP-48 to sum two real matrices to form a complex one. This approach comes in handy when you include reactive elements in the circuit models. If you prefer using a computer rather than a paper napkin, you can also use Spice to analyze this circuit.

Three **equations** are used to analyze the circuit of **Figure 3**. You can express the input current as a function of the input resistance: $I_{IN}=(V_{IN}-V-)/R_{IN}=V_{IN}/R_{IN}$. As in the previous example, you sum the currents at the amplifier's negative pin to zero, $0=V_{IN}/R_{IN}+V_{OUT}/28k\Omega+(V_4-V-)/900\Omega$, and then sum the currents at the V_4 node: $0=(V_4-V-)/900\Omega+(V_4-V_{OUT})/R_{LOAD}+V_4/20\Omega$.

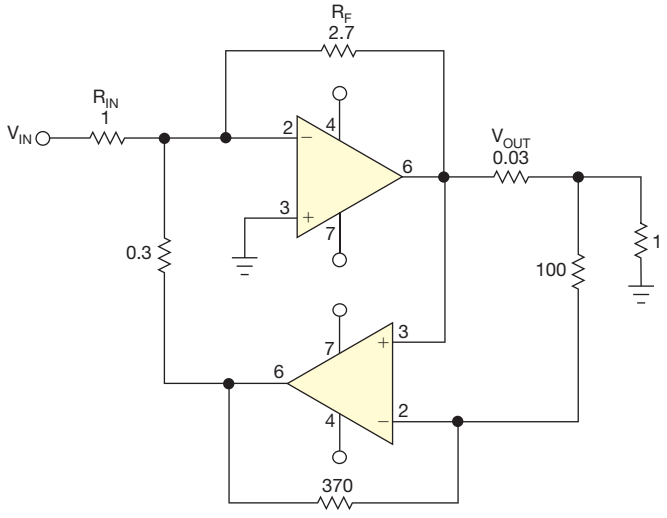

Figure 2 This scheme uses a high-side-current-sense resistor and a second amplifier to set the output impedance to match the load, and it allows almost full output swing.

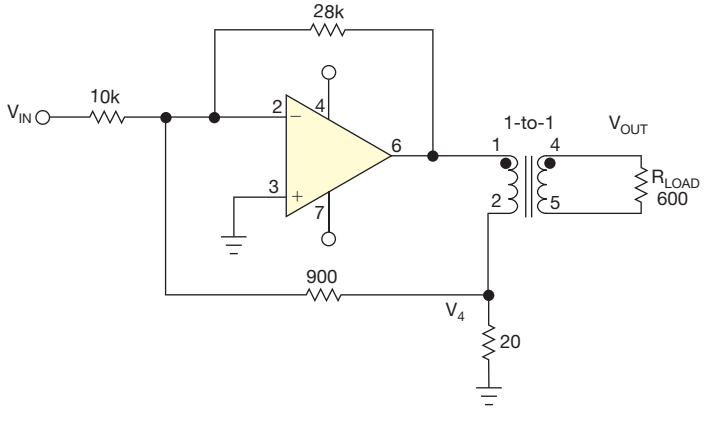

Figure 3 You can also use low-side sensing of output current to match the output impedance when you have a transformer-coupled output.

You express the currents as a vector:

$$(I)=\begin{pmatrix} I_{IN} \\ 0 \\ 0 \end{pmatrix}, \text{ where } (V)=\begin{pmatrix} V_{IN} \\ V_O \\ V_4 \end{pmatrix}.$$

The admittance matrix becomes:

$$(\text{ADMITTANCE})=\begin{pmatrix} \frac{1}{R_{IN}} & 0 & 0 \\ \frac{1}{R_{IN}} & \frac{1}{R_F} & \frac{1}{900\Omega} \\ 0 & \frac{-1}{R_{LOAD}} & \frac{1}{20\Omega}+\frac{1}{900\Omega} \end{pmatrix}.$$

This **equation** determines (**Y**), the admittance matrix.

In this case, the input current should be 100 µA, and the load resistance should be 600Ω. Use an HP-48 calculator to invert the admittance matrix and multiply it by the current matrix. The resulting voltage matrix yields an input voltage of 1V, an output voltage of –1.4V, and a V_4 of –0.05V. Next, set the load to 10,000Ω. Assume that the magnetizing inductance of the transformer is infinite. You then repeat the exercise to check that the output voltage is |2.8V|.

You can match the maximum available signal power from the op amp to the load by changing the transformer turns ratio. Calculate the optimum op-amp signal output impedance to be the peak output swing voltage divided by the maximum peak capability of the op amp. EDN

Optically isolated overcurrent detector works from ac mains

José M Espí, Jaime Castelló, Rafael García-Gil, and Marcos Arasa, University of Valencia, Valencia, Spain

The circuit in this Design Idea detects short-circuit faults or excess-current conditions in line-operated equipment, such as a UPS (uninterruptible power supply), across an isolation boundary. If the load current rises higher than a predetermined level, the circuit generates a 5V pulse to immediately shut down the power inverter. This compact circuit provides a reliable means for protecting power semiconductors and batteries against overcurrent conditions. It features an isolated output and a fast response. The ac mains self-power the sensing network. The circuit requires a 5V power supply to the output-enable circuit on the other side of the isolation boundary. The circuit detects bipolar over-

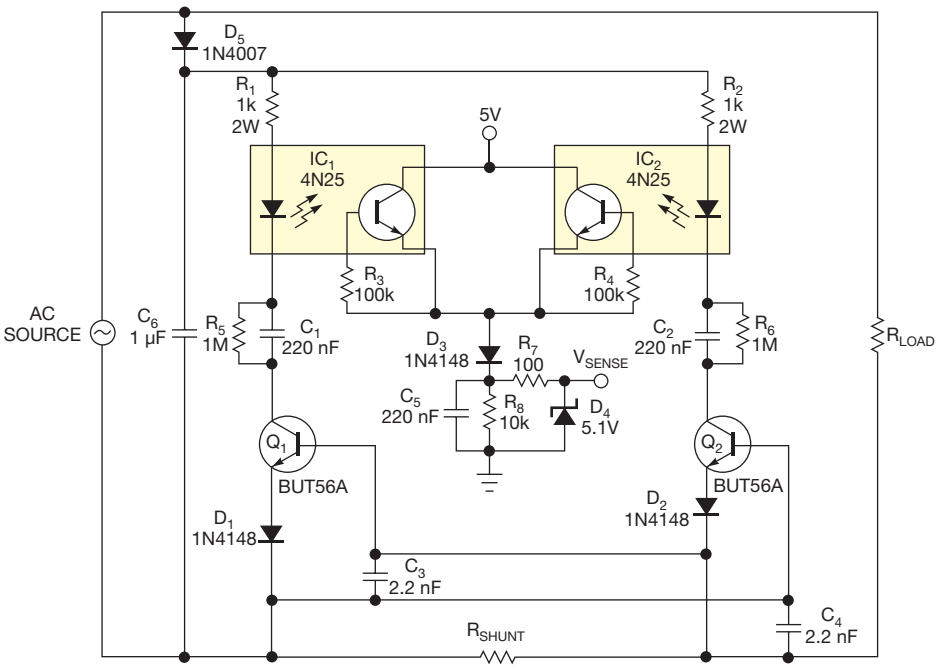

Figure 1 This isolated circuit detects bipolar overloads in a UPS or another ac load.

currents through the load, using shunt resistor R_{SHUNT}'s resistance.

During the positive cycle of the ac source, components R_1, IC_1, R_5, C_1, Q_1, D_1, and C_3 work to detect an overcurrent (**Figure 1**). If the load produces an overcurrent, the voltage drop at the shunt resistor generates a positive voltage on the base of Q_1 that turns it on. Consequently, capacitor C_1, which R_5 initially discharges, receives charge from current across R_1 and IC_1's photodiode. IC_1's photoresistor saturates, charging capacitor C_5 and providing a 5V output at V_{SENSE}, indicating the overcurrent detection. D_1 increases Q_1's base-voltage turn-on threshold to approximately 1.4V. Capacitor C_3 filters any noise or peak voltage that may accidentally turn on the transistor, thus enhancing the system's detection reliability.

A circuit, comprising R_2, IC_2, R_6, C_2, Q_2, D_2, and C_4, for fault detection during the negative cycle of the ac source works similarly. In this case, the direction of current flow through the shunt resistor generates a positive voltage on the base of Q_2. D_5 and C_6 rectify the ac source, providing the isolated supply voltage to polarize the photodiodes. The inverter logic's power supply supplies the 5V source. When the load currents are within limits, the output at V_{SENSE} extinguishes due to the discharge of C_5 through R_8. EDN

Simple circuit helps to protect a vehicle-reverse camera

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

The circuit in this Design Idea uses a simple comparator circuit to make a power-on time delay for an automotive rearview camera. Auto manufacturers typically power reverse-view cameras from the reverse-light circuit. In automatic-transmission vehicles, a short power pulse is applied to the camera when you shift through reverse as you go from park to drive, or vice versa. This sudden voltage pulse is bad for the sensitive circuits in the camera and may reduce its lifetime. This Design Idea suggests a simple and cheap method for avoiding this situation.

The input to this circuit connects to the positive and negative terminals of the reverse light (**Figure 1**). The circuit powers the camera using a MOSFET. R_1 and C_1 form a time-delay element (**Reference 1**). When the reverse light turns on, it slowly charges the capacitor through resistor R_1. R_3 and R_4 form a voltage divider, which you use to set 6V on the inverting pin of the comparator. At the instant of power application to the circuit, the comparator output is

low, and the MOSFET is off. Once the voltage of C_1 rises above 6V, the comparator's output becomes high, and the MOSFET turns on. The values of R_1 and C_1 set the time delay to 2.2 sec. You can calculate this time based on the exponential charging of a capacitor using the following **equations**:

$$V_C(t)=V_{IN}\times\left[1-e^{-(t/R_1C_1)}\right],$$

$$6=12\times\left[1-e^{-(t/33\ k\Omega\times100\ \mu F)}\right],$$

and

$$t=2.287\ SEC.$$

You can set a different time delay by changing the value of R_1 or C_1. When you shift the gear lever from the reverse position to any other position, capacitor C_1 discharges within 60 msec through D_1, R_3, and R_4. As you pass through reverse, shifting between park and drive, the camera does not turn on due to the 2-sec delay. EDN

AS YOU PASS THROUGH REVERSE, SHIFTING BETWEEN PARK AND DRIVE, THE CAMERA DOES NOT TURN ON.

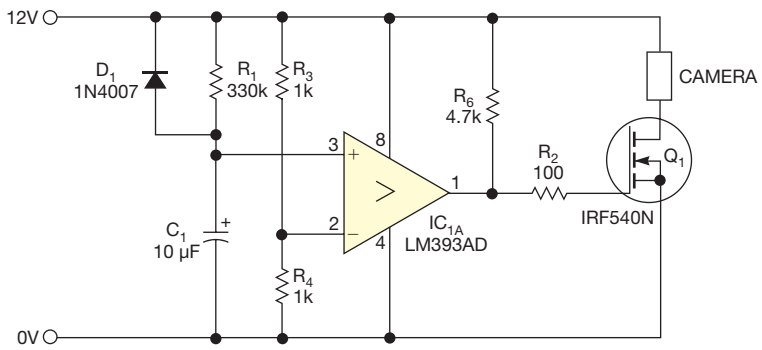

Figure 1 This circuit creates a 2-sec turn-on delay for a car's reverse camera.

REFERENCE

1 "Charging and discharging a capacitor," Kotisivukone, Oct 31, 2007, http://bit.ly/qsmTb6.

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Use a self-powered op amp to create a low-leakage rectifier

Martin Tomasz, Sageloop Designs, San Francisco, CA

You can combine a carefully chosen op amp, a low-threshold P-channel MOSFET, and two feedback resistors to make a rectifier circuit with less forward drop than a diode (**Figure 1**). The rectified output voltage powers the active circuitry, so no additional power supply is necessary. The circuit's quiescent current is lower than most Schottky diodes' reverse-leakage current. This circuit provides active rectification at voltage drops as low as 0.8V. At lower voltages, the MOSFET's body diode takes over as an ordinary diode.

The op-amp circuit turns on the MOSFET as a forward voltage develops between the input and the output voltages, according to the following **equation**:

$$V_{GATE}=V_{OUT}-(R_2/R_1)(V_{IN}-V_{OUT}),$$

where V_{GATE} is the MOSFET's gate drive, V_{IN} is the input voltage, and V_{OUT} is the output voltage. You can relate the input and the output voltages to the MOSFET's drain-to-source and gate-to-source voltages, according to the following **equations**:

$$V_{DS}=V_{IN}-V_{OUT} \text{ and } V_{GS}=V_{GATE}-V_{OUT},$$

where V_{DS} is the drain-to-source voltage and V_{GS} is the gate-to-source voltage. Combine these **equations** to relate the MOSFET's gate drive to a function of the drain-to-source voltage:

$$V_{GS}=-(R_2/R_1)V_{DS}.$$

If you make R_2 12 times larger in value than R_1, a 40-mV voltage drop across the MOSFET's drain-to-source voltage is sufficient to turn on the MOSFET at low drain currents (**Figure 2**). You could choose a higher ratio to further reduce the voltage drop within the limits of the op amp's worst-case input-offset voltage of 6 mV. The op amp is powered from output-reservoir capacitor C_1. The amplifier has rail-to-rail inputs and outputs and no phase inversion when operating near the rails. The amplifier operates at power-supply voltages as low as 0.8V. You directly connect the op amp's noninverting input to the V_{DD} rail and the amp's output to the gate of the MOSFET. The circuit consumes slightly more than 1 µA when actively rectifying a 100-Hz sine wave, less current leakage than that

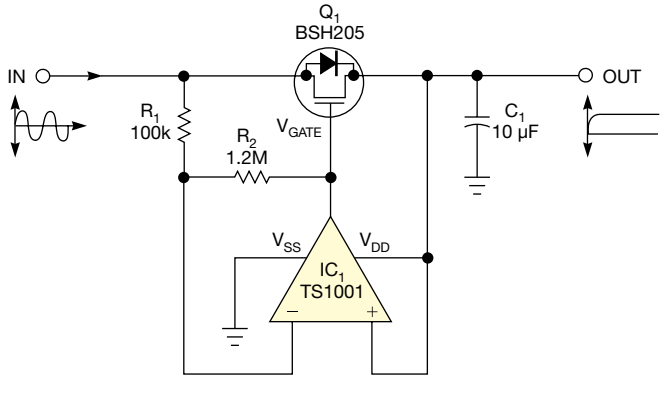

Figure 1 This circuit emulates a rectifier, but it has forward-voltage drop of 40 mV or less. The circuit has less reverse leakage than a Schottky diode.

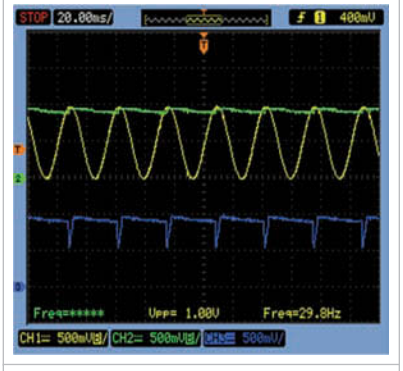

Figure 2 The output of the circuit (green) with a sine-wave input (yellow) shows that the FET's gate voltage (blue) drops out only when the input-to-output differential is less than 40 mV.

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of most Schottky diodes. The BSH205 supports milliamp-level currents at a gate-to-source voltage of 0.8V.

The op amp's bandwidth limits the circuit to lower-frequency signals. At bandwidths higher than 500 Hz, the amplifier's gain begins to decline. As the signal frequency increases, the MOSFET remains off, and the body diode of the MOSFET takes over the rectification function. An input with a fast fall time could potentially drag the output with reverse current through the MOSFET. However, for small currents, the MOSFET operates in its subthreshold range. The amplifier quickly turns off due to the exponential relationship of the gate-to-source voltage to the drain-to-source current in the subthreshold range. The limiting factor is the amplifier's slew rate of 1.5V/msec. As long as you don't load the circuit so heavily that you drive the MOSFET into its linear range, reverse currents won't exceed forward currents.

You can use the circuit in a micropower solar-harvesting application (**Figure 3**). Depending on the light, the BPW34 cells generate 10 to 30 µA at 0.8 to 1.5V. The active-diode circuit rectifies the peak harvested voltage in conditions of rapidly changing light and minimizes reverse leakage to the cells. EDN

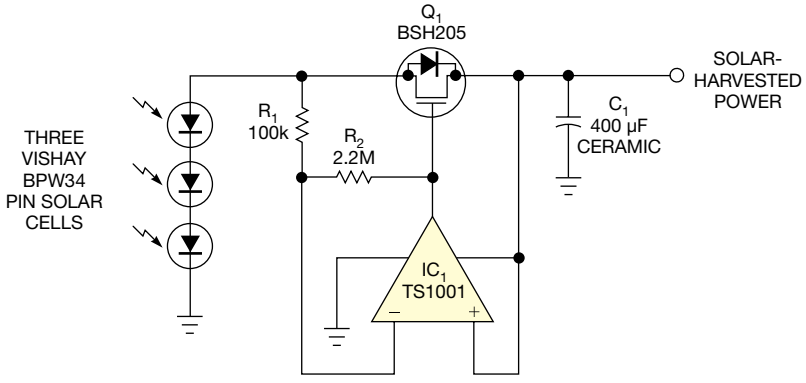

Figure 3 You can use the active-rectifier circuit to charge a capacitor from solar cells. The rectifier has low voltage drop and protects the cells from reverse current when there is no light.

Simple reverse-polarity-protection circuit has no voltage drop

Aruna Prabath Rubasinghe, University of Moratuwa, Moratuwa, Sri Lanka

Common methods of reverse-voltage protection employ diodes to prevent damage to a circuit. In one approach, a series diode allows current to flow only if the correct polarity is applied (**Figure 1**). You can also use a diode bridge to rectify the input so that your circuit always receives the correct polarity (**Figure 2**). The drawback of these approaches is that they waste power in the voltage drop across the diodes. With an input current of 1A, the circuit in **Figure 1** wastes 0.7W, and the circuit in **Figure 2** wastes 1.4W. This Design Idea suggests a simple method that has no voltage drop or wasted power (**Figure 3**).

Select a relay to operate with the reverse-polarity voltage. For example, use a 12V relay for a 12V supply system. When you apply correct polarity to the circuit, D_1 becomes reverse-biased, and the S_1 relay remains off. Then connect the input- and output-power lines to the normally connected pins of the relay, so current flows to the end circuit. Diode D_1 blocks power to the relay, and the protection circuit dissipates no power.

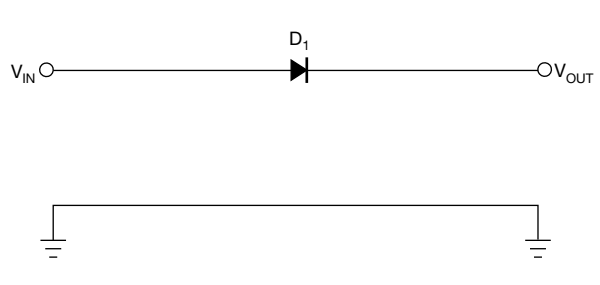

Figure 1 A series diode protects systems from reverse polarity but wastes power in diode losses.

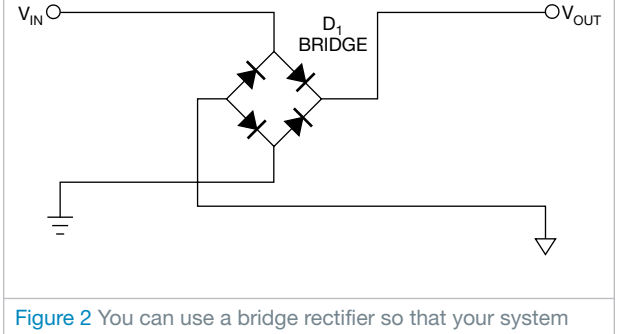

Figure 2 You can use a bridge rectifier so that your system works no matter what the input polarity is. This circuit wastes twice the power, in diode losses, of the circuit in Figure 1.

When you apply incorrect reversed polarity, diode D_1 becomes forward-biased, turning on the relay (**Figure 4**). Turning on the relay cuts the power supply to the end circuit, and red LED D_3 turns on, indicating a reverse voltage. The circuit consumes power only if reverse polarity is applied. Unlike FETs or semiconductor switches, relay contact switches have low on-resistance, meaning that they cause no voltage drop between the input supply and the circuit requiring protection. Thus, the design is suitable for systems with tight voltage margins. EDN

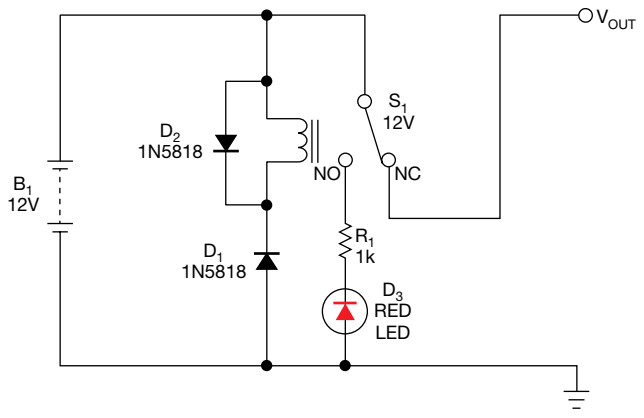

Figure 3 You can wire a relay switch to pass power to your system with no power loss. D_2 clamps inductive kicks from the relay coil.

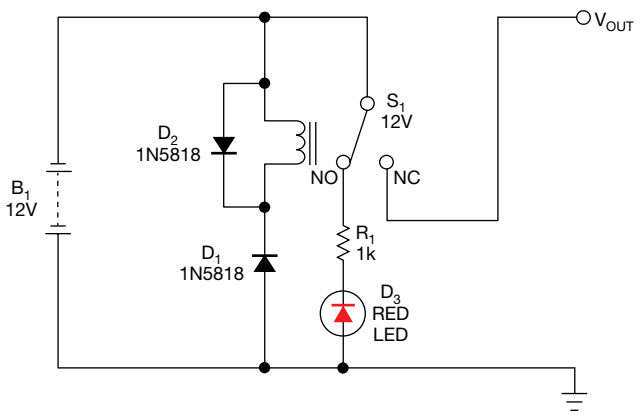

Figure 4 With reversed input voltage, the relay switch engages, interrupting power to the system, and the LED lights.

Series-LC-tank VCO breaks tuning-range records

Louis Vlemincq, Belgacom, Evere, Belgium

This Design Idea applies a novel topology to an oscillator. It uses a series-connected LC (inductive-capacitive) tank circuit to give the circuit a higher tuning range than circuits that use a parallel-LC connection. The architecture of the oscillator permits wide frequency swings, well beyond the capabilities of the best hyperabrupt varactor. Engineers deem a VCO (voltage-controlled oscillator) capable of covering one octave as state of the art. This topology allows a 4-to-1 ratio in output frequency. The LC tank alone sets this frequency so that the parasitic capacitances of other components do not limit the output frequency. Unlike standard oscillators, this circuit works well at its frequency extremes.

At first glance, the central structure of the oscillator resembles two transistors that form a latching SCR (silicon-controlled-rectifier) structure (**Figure 1**). The structure is similar to that of a thyristor, but you add degeneration resistors that keep the circuit in a linear mode of operation. The resistors make the gain of this "SCR" smaller than one, and it is dc-stable. The series-tuned tank circuit increases the gain beyond one at the resonant frequency, causing the circuit to oscillate. No auxiliary components are necessary for oscillation, and the node between the inductor and the capacitor is free of other connections, meaning that only the varactor you use as the capacitor determines the tuning range. The frequency varies as the square root of the tuning elements. To change the frequency by a factor of two, you need a fourfold variation of the tuning capacitance.

Unlike a parallel-LC tank, the resonant current passes through the active element and is, therefore, limited. This limit in turn means that the ac voltage appearing across the tuning components is small—typically, less than 100 mV. The small signal reduces the effects of circuit nonlinearity and the impact of the self-biasing effects of the signal on the varactor. You can use control voltages as small as 0.3V across the varactor. If you use a 1-µH inductor, the circuit still oscillates with capacitor values of 4.7 pF to 4.7 µF—a ratio of 106-to-1.

For the detailed design, move the LC tank to the emitter of PNP transistor Q_2 (**Figure 2**). The lower speed of the PNP creates greater phase difference and encourages oscillation. Connect L_2 and C_2 at a common power point on the power rail, emphasizing

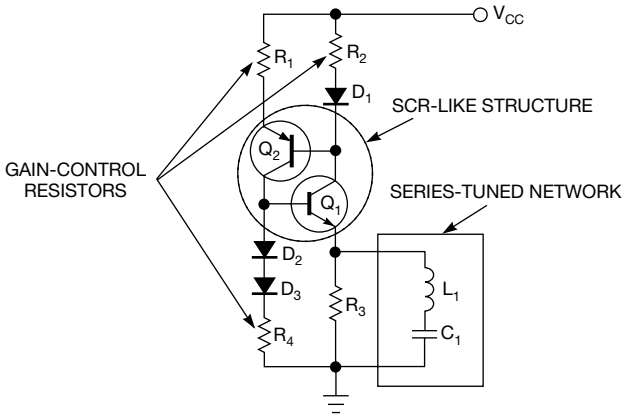

Figure 1 The heart of the oscillator are two transistors and a series-LC tank. The gain-control resistors add degeneration so that the transistors operate in their linear range instead of latching, as an SCR would.

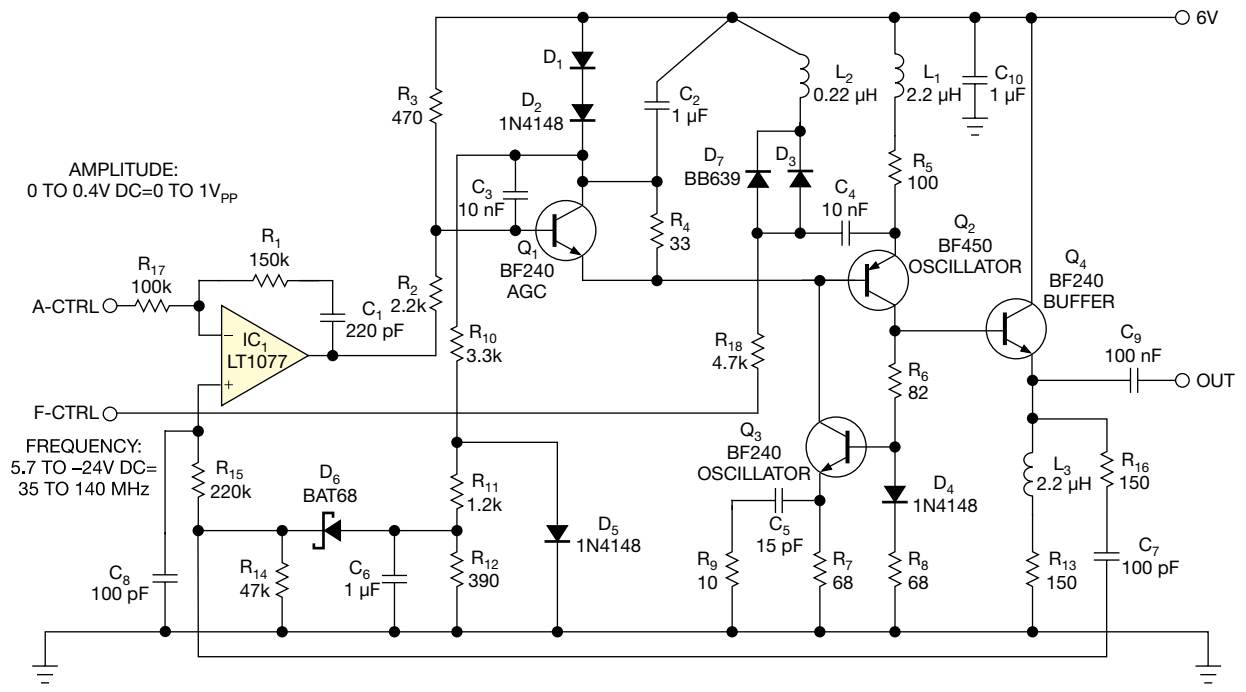

Figure 2 For the detailed design, move the LC tank to the PNP transistor. Varactors D_7 and D_3 form the capacitance, and L_2 is the inductance.

the criticality of the layout in this part of the circuit. The oscillator "senses" the tuned circuit through C_2 and C_4, and anything inside that loop adds uncontrolled parasitics to L_2. These parasitics would compromise the AGC (automatic-gain-control) action and degrade the performance and accuracy of the oscillator.

Q_1 and associated components implement the AGC. A parallel-LC oscillator tolerates clipping of the signal, but this series-LC circuit degenerates into a multivibrator if you allow the signal to grow so large that it clips. The AGC servo action has the added advantage of producing uniform output amplitude. Use D_5 to create a 0.6V dc bias. R_{11} and R_{12} form a voltage ladder that creates a dc-bias voltage close to the forward-voltage drop of Schottky diode D_6. This bias allows D_6 to work as a more perfect rectifier of the small output signal. C_8 integrates the rectified signal into a dc voltage proportional to the amplitude of the circuit's output. Apply this dc signal to IC_1, the AGC amplifier, through a filter comprising R_{15} and C_8. The op amp servo-controls the filtered dc signal against the A-CTRL input-amplitude signal you send to the circuit. This signal allows you to set output amplitude at 0 to 1V.

In this example, the output amplitude is 0.9V. The frequency range extends from 35 to 140 MHz, a 1-to-4 ratio—twice that of conventional high-performance VCOs—and requires a fourfold increase in the capacitance ratio. The overall capacitance ratio is 1-to-16, exactly that of the varactor itself. At the lowest (**Figure 3**) and highest (**Figure 4**) frequencies of the output range, the quality of the sine wave remains excellent, thanks to AGC action. EDN

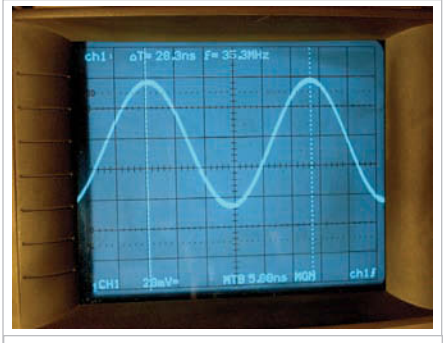

Figure 3 At 35 MHz and 0.9V output, the oscillator creates a high-quality sine wave.

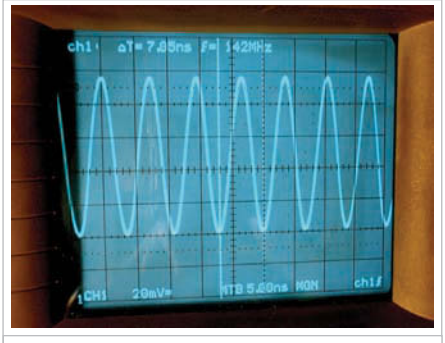

Figure 4 At 142 MHz and 0.9V, the output is still pure and stable, thanks to the AGC circuit.

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Circuit detects rapidly falling signals and rejects noise

Vladimir Rentyuk, Zaporozhye, Ukraine

Detecting a rapidly falling signal over some threshold is important for ultrasonic or location equipment as well as for seismology systems. You can combine a rail-to-rail operational amplifier with a Schmitt-trigger logic gate to perform this function (**Figure 1**). This example works well in an ultrasound machine. It controls a sample-and-hold amplifier that sets the gain of an AGC (automatic-gain-control) system.

The circuit works only with positive signals, so the signal must pass through a full-wave rectifier before it is applied to the circuit input. You configure the main part of the circuit, op amp IC_1, as a comparator with hysteresis. It produces a high-level output when an input signal is higher than the specified threshold. The output goes to a low level when the input signal begins to fall but only when the input falls faster than an established rate of change or if the level of the input signal will be lower than the established threshold of sensitivity. This circuit detects the moment when a signal is above the established threshold and the falling signal—or a mix of the signal and noise—has higher-than-specified speed.

R_1 and C_1 form an input lowpass filter to smooth the input signal. You set the values of R_1 and C_1 to create a filter roll-off for the input signal you are processing. Resistors R_3 and R_4 establish a small hysteresis, which is necessary so that slow signals with noise don't cause the output to change state. You set the threshold level with voltage divider R_6 and R_7. D_1, R_5, and C_2 form a peak detector. R_5 establishes a time constant of the discharge of C_2 and provides sensitivity to a falling signal's rate. You establish the circuit's sensitivity to a falling signal's rate of change using the time constant, which the values of C_2 and R_5 set. Hysteresis resistor R_4 is more than a decade larger than R_5, so the effect of resistors R_3 and R_4 is negligible.

A rising input signal greater than the threshold charges C_2 to approximately the level of the input signal. The output amplifier is at a high level because the

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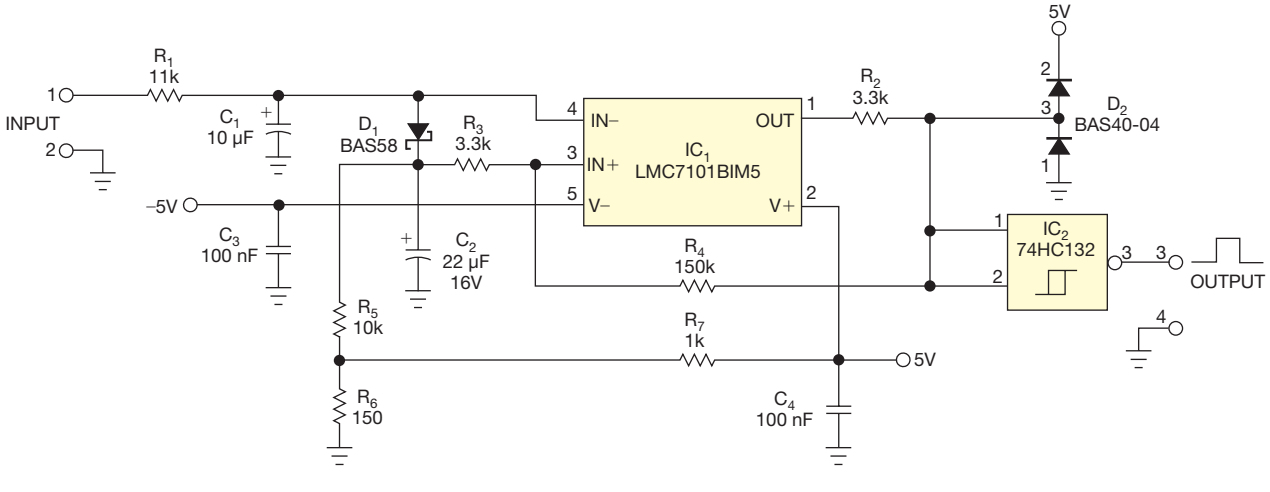

Figure 1 This circuit detects signal excursions higher than a set threshold and rejects noise and recognizes fast falling signals.

voltage on C_2 is always lower than the value of the rising input signal due to D_1's voltage drop. When the input drops faster than C_2 can discharge through R_5, the output level of the device changes to a low level because the voltage on C_2 is higher than the value of the falling input signal. If the input signal falls more slowly than the discharge of C_2 through resistor R_5, the output remains high. Schottky diode D_1 prevents the discharge of C_2 through the input. R_2 and D_2 clamp the amplifier's output to positive values. Feed the clamped signal to Schmitt-trigger logic gate IC_2 to give a logic-level output with fast transitions (**Figure 2**). EDN

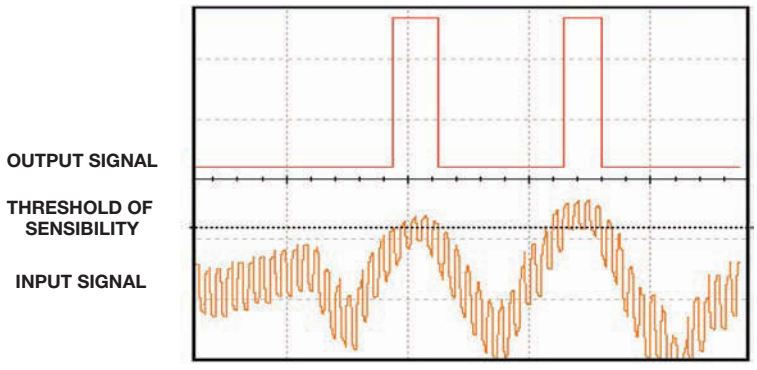

Figure 2 The circuit recognizes a pulse when it falls; noise is exaggerated for clarity.

Hack into a stopwatch to make a phototimer

Ralf Kelz, Seefeld, Germany

The exposure tester in this Design Idea measures the on time of a light source, whether an LED, an incandescent lamp, a halogen lamp, or another source. It can be made with an ordinary stopwatch and a few simple components (**figures 1** and **2**). An electronic stopwatch needs two pulses to operate; one starts the internal counter, and another one stops it. A light source provides only one pulse, corresponding to the time the light is illuminated. This circuit generates a short trigger pulse whenever the luminous intensity changes.

When the photodiode is not illuminated, capacitor C_1 charges to 1.5V (**Figure 3**). The charge initially comes through the base-emitter junction of Q_1 with a time constant that $R_1 \times C_1$ sets. Once C_1 charges to 1.5V minus the base-to-emitter voltage, R_3 tops off the charge on C_1 until it reaches 1.5V. Because R_3 and R_1 are in series during this time, this topping off occurs with a slower time constant that $(R_1+R_3)\times C_1$ sets.

When the photodiode is illuminated, photocurrent flows through R_1, raising its voltage to more than 0V, which drives the right side of C_1 above the 1.5V rail. The base of Q_1 is reverse-biased and has no effect. However, Q_2's emitter is now forward-biased because R_4 holds the base near 1.5V. As Q_2 turns on, the charge in C_1 dissipates across R_2, raising its voltage and creating a positive pulse. You convey this pulse to the stopwatch through R_5, which is necessary in the case of extreme illumination of the photo-

Figure 1 You build the circuit on a small prototype board that connects to the CG-501 stopwatch.

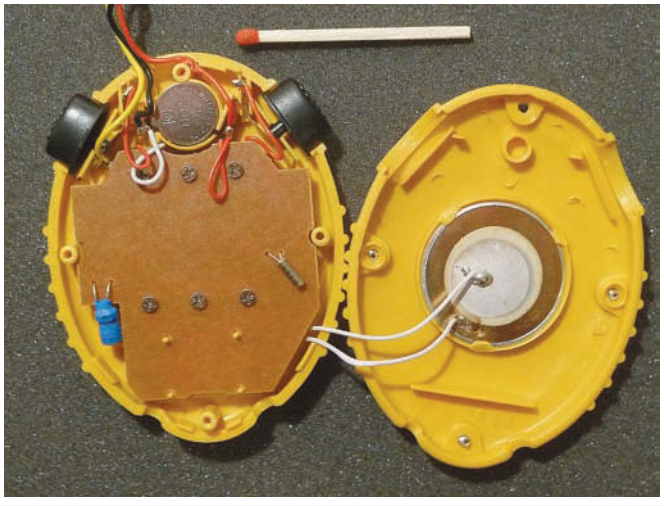

Figure 2 You can solder in pigtails to bring power, ground, and the trigger circuit to the prototype.

diode. It limits the current into the stopwatch circuitry so that a large pulse cannot latch or overpower the internal stopwatch circuitry. The photocurrent creates a difference between 1.5V and the voltage of R_1; this difference causes C_1, under illumination, to enter a final voltage.

When the photodiode is not illuminated, no photocurrent goes through R_1, so C_1 can charge back up as its left side goes to ground and its right side goes first to a base-emitter drop below 1.5V and subsequently all the way to 1.5V. Because the initial charge conducts through the base-emitter junction of Q_1, that transistor again turns on, delivering a pulse across R_2 and halting the stopwatch.

Your selection of the value of C_1 depends on the exposure time to be measured and on the photodiode used. The response rate of this circuit is approximately 500 msec. This example uses an Everlight PD333-3C/HO/L2 photodiode with a large spectral bandwidth, but any other photodiode or even a photoresistor will also work. EDN

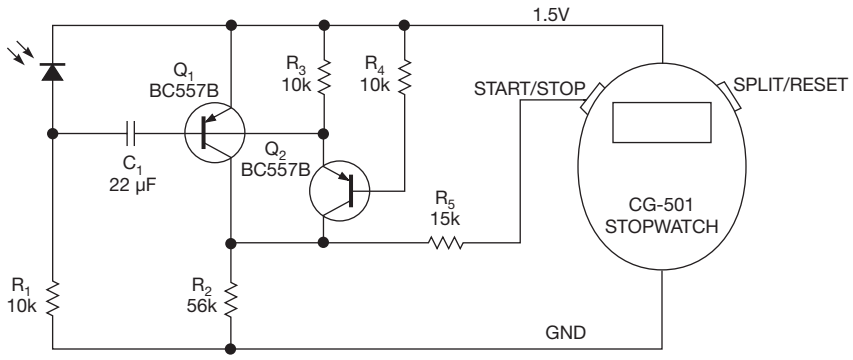

Figure 3 This simple circuit times a light source. When you illuminate the photodiode, Q_2 creates a pulse. When you remove the illumination, Q_1 creates a pulse.

Comparator directly controls power-MOSFET gate

Peter Demchenko, Vilnius, Lithuania

It is common practice to power a MOSFET with a comparator and with an unregulated voltage and to power the comparator driving it from a regulated one (**Figure 1**). Many loads are insensitive to driving voltage, so it would be a waste of money and power to use a regulated supply to drive the FET. It is also common practice to add resistors R_1 and R_2 to the comparator to put hysteresis in the operation, making the circuit less susceptible to noise, especially with slowly changing signals.

This circuit's comparator changes with changes in the unregulated power supply. You can correct this problem by adding diode D_2 and resistor R_5 to the circuit (**Figure 2**). This approach isolates the hysteresis circuit from the unregulated output and instead drives it from the same regulated supply that drives the comparator. When the comparator is on, it drives the FET just as the original circuit does, pulling the P-channel FET gate toward ground. In both cases, you connect zener diode D_1 to the FET gate to avoid exceeding the gate-to-source voltage. The improvements in the circuit in **Figure 2** become

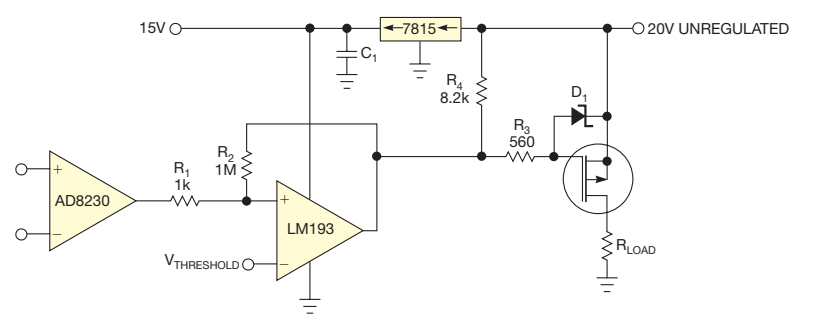

Figure 1 Hysteresis components R_1 and R_2 tie to the unregulated supply, causing the comparator's switching point to vary with the power supply.

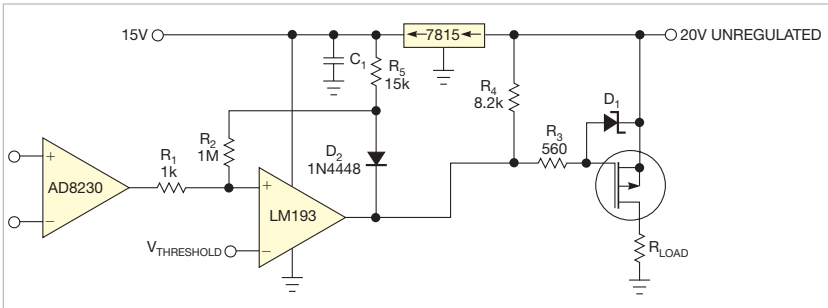

Figure 2 Resistor R_5 and an ORing diode isolate the hysteresis circuit from the power supply and keep the switching point constant no matter how the power supply changes.

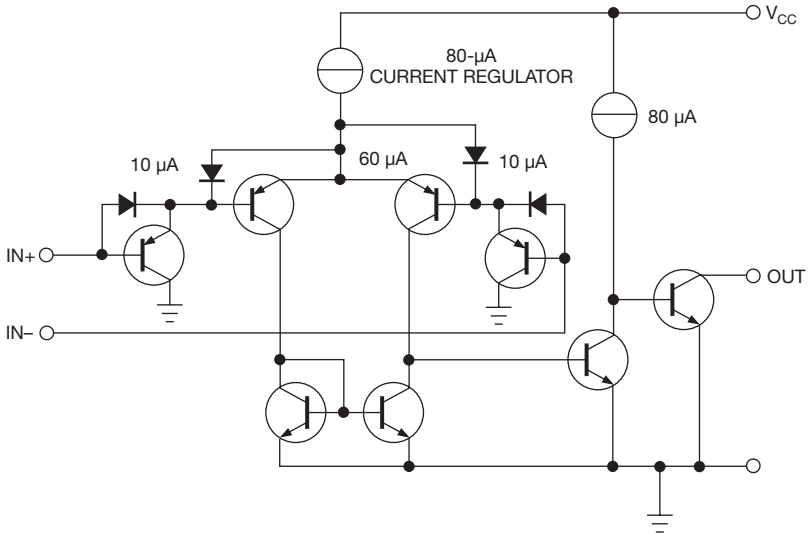

Figure 3 The internal design of the LM193 comparator requires that you keep the input pins 2V below the positive rail (courtesy Texas Instruments).

apparent when the comparator turns off. In either case, R_4 pulls the comparator's open-collector output up to the positive power supply. In **Figure 2**, however, the diode isolates the hysteresis circuit from the power supply so that R_4 pulls up R_5 to the regulated 15V, no matter how the power supply changes.

With a legacy comparator such as Texas Instruments' LM193, the common mode of the inputs must stay well below the power-supply rail (**Figure 3**). The circuit requires 1.5V head room at 25°C and 2V head room over temperature. Thus, for the circuits in **figures 1** and **2**, you cannot set the threshold voltage higher than 13V. If your circuit requires a threshold voltage closer to the power rail, consider using newer parts with rail-to-rail inputs. You must use an open-collector or open-drain comparator for this hysteresis-isolation circuit to work. It would be incompatible with a totem-pole-output IC. EDN

Originally published in the September 4, 1986, issue of *EDN*

AGC circuit uses an analog multiplier

Steve Lubs, Department of Defense, Washington, DC

In the AGC circuit of **Fig 1**, a 4-quadrant analog multiplier (IC_1), an amplifier stage (IC_2), an active, full-wave rectifier (D_1, D_2, R_4-R_7, and IC_3), and an integrator (IC_4) accomplish automatic gain control of V_{IN}'s amplitude variations in the audio-frequency range.

The multiplier's output is $-V_{IN}V_Y/10$, where V_Y is a negative voltage generated by the integrator IC_4. Together, the integrator and the rectifier extract the dc component (V_Y) of V_{OUT} for use as a feedback signal to the multiplier. The integrator sums signal current from the rectifier and control current from potentiometer R_9, which lets you adjust V_{OUT}'s signal level.

Circuit analysis yields the frequency-response **equation**

$$V_{OUT}=\frac{K_1AV_C}{10RC_3}\left(\frac{1}{s+\frac{10A}{RC_3}}\right),$$

or, in the time domain,

$$V_{OUT}=\left(\frac{K_1AV_C}{10RC_3}\right)\exp\left(-\frac{10At}{RC_3}\right).$$

In both **equations**, K_1 is the gain of amplifier IC_2, A is the peak amplitude of V_{IN}, and R is the resistance between the integrator input and the rectifier output. (For this circuit, R equals R_6 in parallel with R_7.)

This AGC circuit is suitable for controlling the long-term variations of amplitude within a limited range. It doesn't respond uniformly over a wide dynamic range, however, because the time response is inversely proportional to input-signal amplitude. EDN

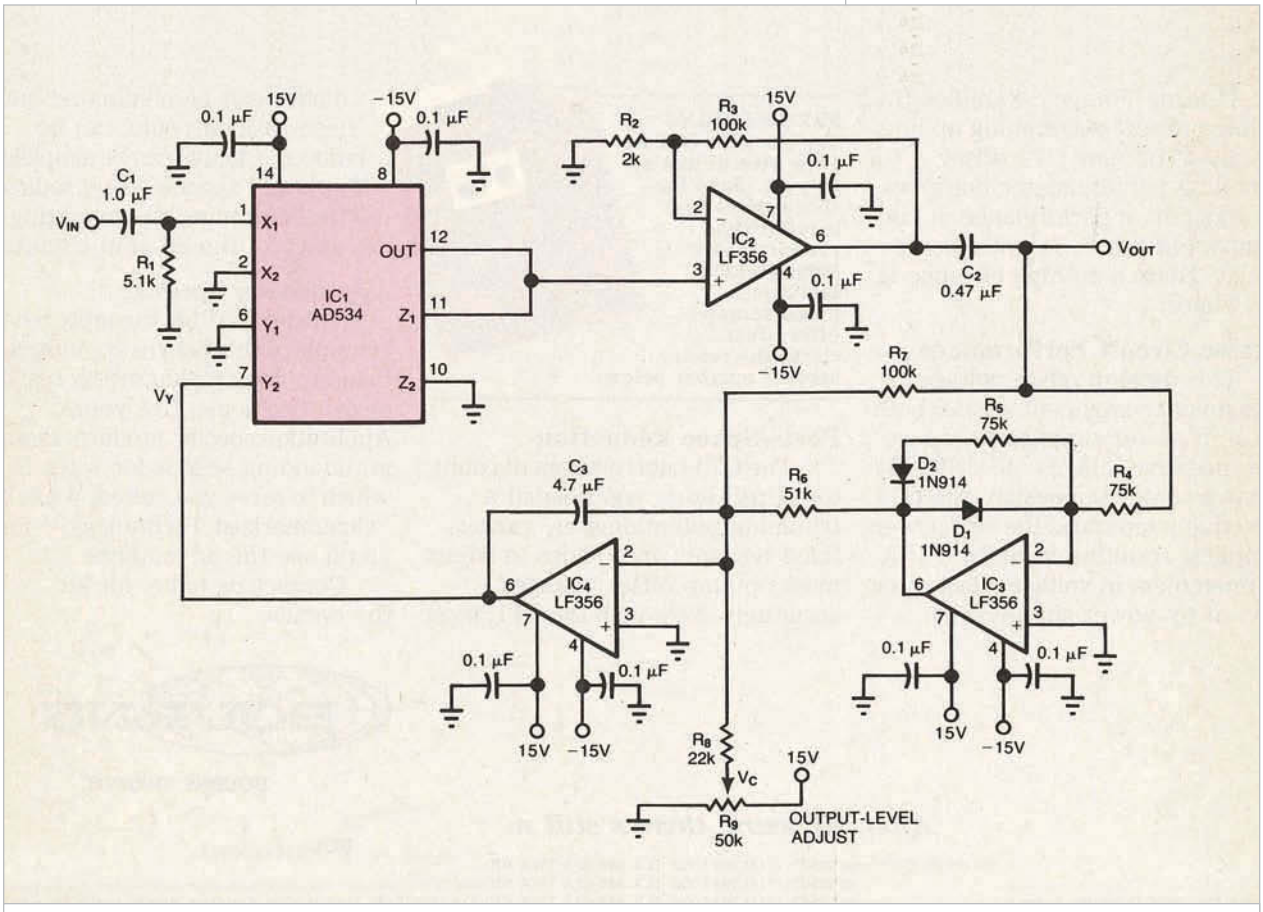

Figure 1 Analog multiplier IC_1 combines V_{IN} with a feedback signal V_Y to achieve automatic gain control.

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designideas

READERS SOLVE DESIGN PROBLEMS

Add extra output to a boost converter

Vladimir Oleynik, Moscow, Russia

Designers use step-up-converter ICs in battery-powered portable equipment. These chips usually provide one output with a fixed or an adjustable voltage. Some chips contain an LBI/LBO (low-battery-in/low-battery-out) function. The chip manufacturer intends for these pins to be used for monitoring a low-battery condition and to warn gadget owners when a battery goes flat. You can instead use this function to provide an extra voltage output.

The Maxim MAX756 boost converter provides a fixed output of 3.3 or 5V at 300 and 200 mA, respectively (**Figure 1**). The input voltage can range from 0.7 to 5.5V. For low-battery detection, the part has on-chip circuitry comprising a comparator, a reference, and an open-drain MOSFET. When the voltage at the LBI input is lower than its threshold level of 1.25V, the MOSFET at the LBO output sinks current to ground.

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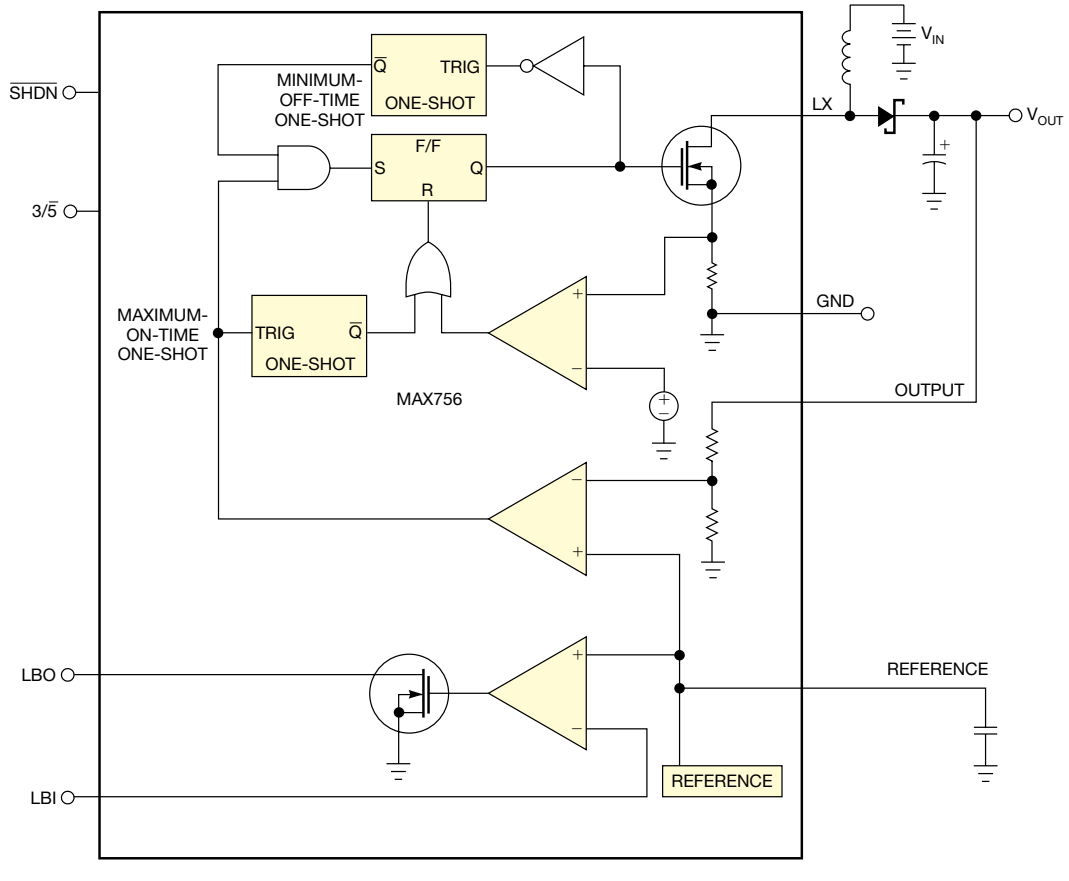

Figure 1 You can use the battery-monitoring circuit in this fixed-output boost converter to make a secondary output voltage (courtesy Maxim).

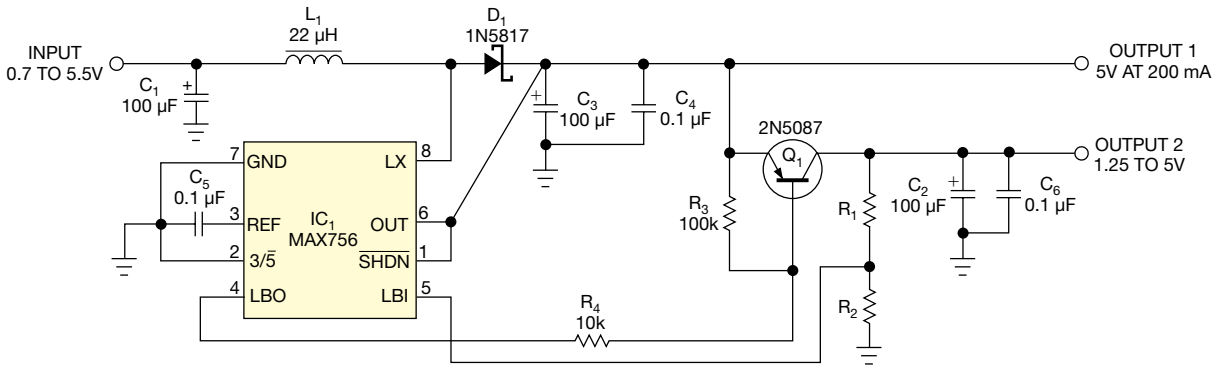

Figure 2 You can use the LBI and LBO pins of this boost-converter IC to operate a low-dropout secondary output.

You can use these components to make a second output with a regulated voltage (**Figure 2**). R_1 and R_2 determine the secondary output voltage according to the following **equation**: Output 2 $=V_{REF}(R_1+R_2)/R_2$, where V_{REF} is the reference voltage, which is 1.25V for this chip.

You can set Output 2 from 1.25 to 5V as long as it is less than Output 1. Because Output 2 is derived from Output 1, the total output current for both outputs should not exceed 200 and 300 mA for Output 1 and Output 2 voltages of 5 and 3.3V, respectively.

You can also use the LBI/LBO function to make a second boost converter (**Figure 3**). The CD4093 quad Schmitt-triggered NAND gates, inductor L_2, R_2 through R_4, Q_1, D_1, C_1, and C_2 compose this boost converter. Add C_1 and R_2 to IC_{1B} to make a free-running oscillator that IC_{1A} gates on. For the values of R_2 and C_1 in the **figure**, the oscillator frequency is approximately 17 kHz. R_1 pulls up the open-drain LBO output.

When the voltage at the LBI pin is lower than 1.25V, the LBO pin is low, thus allowing operation of the IC_{1B} oscillator. IC_{1C} and IC_{1D} drive

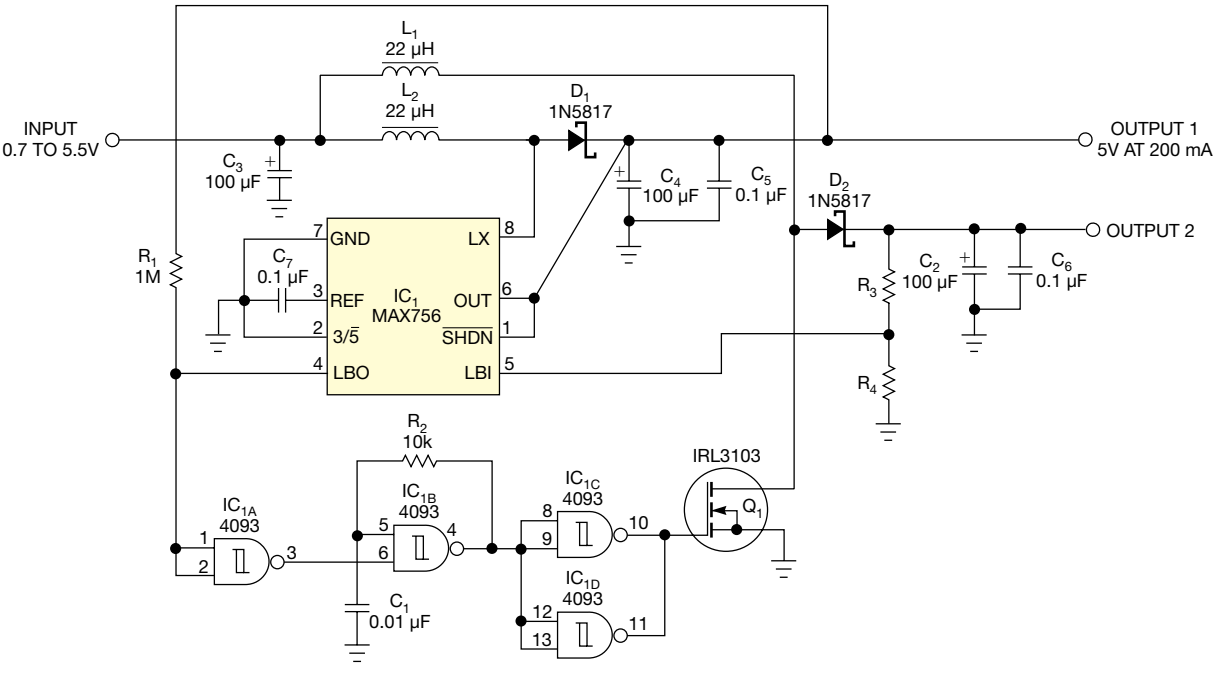

Figure 3 If you need a boosted secondary output, you can use the LBI and LBO pins to make another switching boost converter.

power MOSFET transistor Q_1. When Q_1 is on, it pulls current from inductor L_1. When Q_1 is off, this energy charges capacitor C_2 through flyback diode D_1. You apply feedback with resistor divider R_3 and R_4 to determine the Output 2 voltage, according to the following **equation**: Output 2=1.25V×(R_3+R_4)/R_4. IC_1 gets power from Output 1.

The voltage at Output 2 is a function of the output current and the input voltage (**Figure 4**). If you have adequate input voltage, the output graph shows a flat section where the IC's regulation is effective (**figures 5** and **6**).EDN

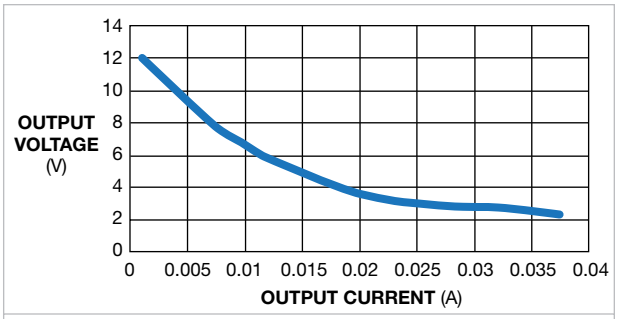

Figure 4 With only 1V input, the circuit cannot hold regulation, and the output voltage drops directly with output current.

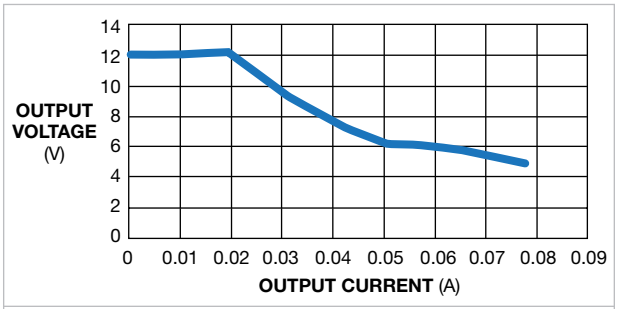

Figure 5 With a 2V input, the circuit maintains regulation to an output current as high as 20 mA.

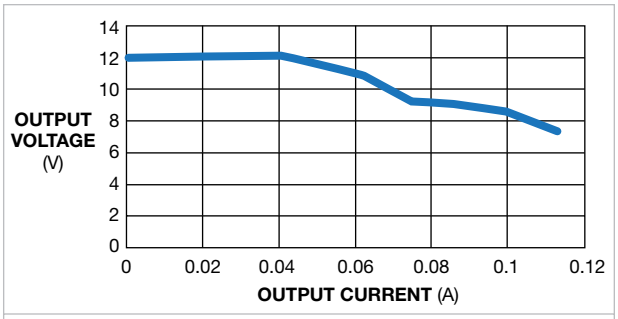

Figure 6 With a 3V input, the circuit holds regulation to an output current as high as 40 mA.

Fabricate a high-resolution sensor-to-USB interface

Zoltan Gingl, University of Szeged, Szeged, Hungary

The circuit in this Design Idea combines a mixed-signal microcontroller, a USB UART (universal asynchronous receiver/transmitter), and a novel adaptable analog sensor-input circuit. It allows you to connect many types of sensors to the design's two analog-input channels, control the device, and read measurement data on a USB host. The USB connection powers the circuit. You can control the device from your computer with simple commands; even terminal software can make the measurements. The 8051 core allows for easy programming with freely available tools, such as IDEs (integrated development environments), debuggers, and C compilers.

The design is based on a $8 microcontroller that features an 8051 architecture, as well as a PGA (programmable-gain amplifier) and a 24-bit sigma-delta ADC (**figures 1, 2**, and **3**). Microcontroller IC_1 has an input multiplexer allowing differential or single-ended mode. It also has two DAC outputs and can provide five unassigned digital-I/O pins (**Figure 1**). One output pin drives D_1 under program control. The remaining digital pins are used to configure the two analog-input ports. You also send the microcontroller's reference output to one of the analog-input ports. Four remaining digital pins interface with the USB's UART chip (**Reference 1**).

A 3.3V linear regulator, IC_2, powers the microcontroller (**Figure 2**). You power USB chip IC_1 directly from the USB port through a ferrite bead and a filter network. This popular and reliable USB UART chip lets you communicate with a computer using any operating system. Op amp IC_4 buffers the microcontroller's reference output (**Figure 3**).

Two configurable analog ports allow you to connect many sensor types using two three-input connectors, each of which has a ground pin (**Figure 4**). One ground pin provides 3.3V power, and the other outputs the buffered reference voltage—nominally, 2.5V. Wire

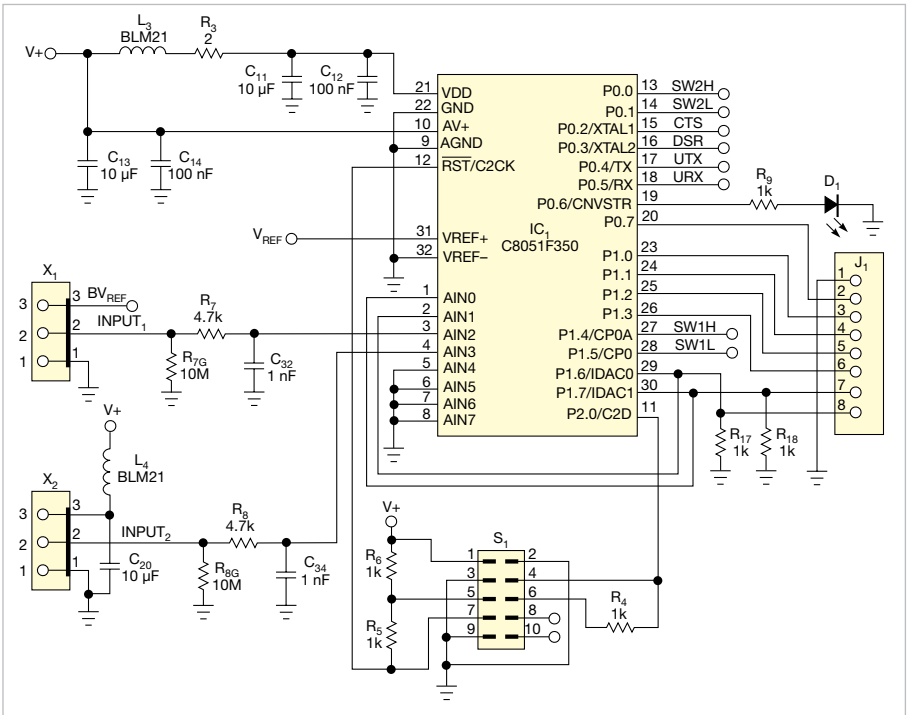

Figure 1 Microcontroller IC_1 has an input multiplexer allowing differential or single-ended mode and two DAC outputs, and it can provide five unassigned digital-I/O pins.

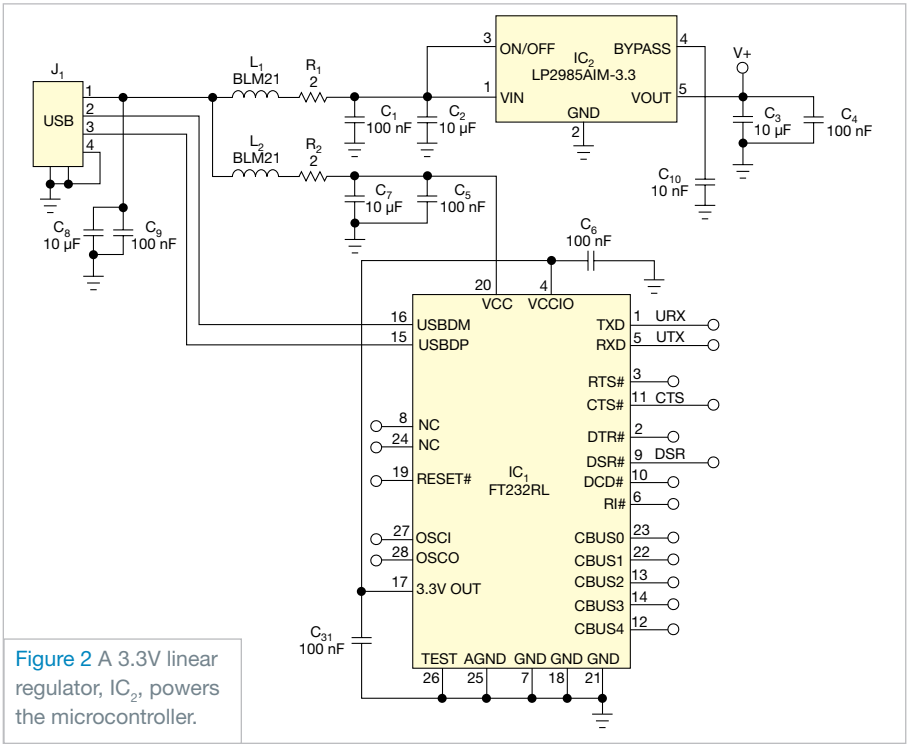

Figure 2 A 3.3V linear regulator, IC_2, powers the microcontroller.

the central pins of the two connectors to the microcontroller's analog-input multiplexer. In this way, you can either measure two single-ended voltages or use these two connectors as differential inputs. Both inputs have individually switched pullup and pulldown resistors, R_{10}, R_{11}, R_{14}, and R_{15}.

CURRENT-OUTPUT SENSORS CAN BE CONNECTED AS YOU WOULD CONNECT PHOTODIODES—BETWEEN THE GROUND AND THE INPUT PINS.

The analog-input architecture allows you to directly connect many kinds of sensors. For example, you can connect a thermistor or a photoresistor between the ground and the input pins and switch on the pullup resistor to form a voltage divider; the on-chip ADC can directly digitize this voltage divider's output (**Figure 5**). This approach also features ratiometric operation, meaning that the ADC uses the same reference as the driving voltage of the voltage divider. Current-output sensors can also be connected as you would connect photodiodes—directly between the ground and the input pins. Switch the pulldown resistor so that the photocurrent develops a voltage.

The high-resolution ADC and PGA allow direct connection of thermocouples (**Figure 6**). You achieve the required bias point by switching on both the pullup and the pulldown resistors on one channel. You can use directly connected bridge-type sensors, such as load cells and pressure sensors, by switching off all of the internal resistors. In these cases, you should operate the ADC in differential mode. Leaving all of the switches open also suits use in potentiometer inputs or IC sensors, such as the SS49E Hall-effect magnetic-field sensor.

When using directly connected sensors, you should consider source impedance, signal range, filtering, and noise

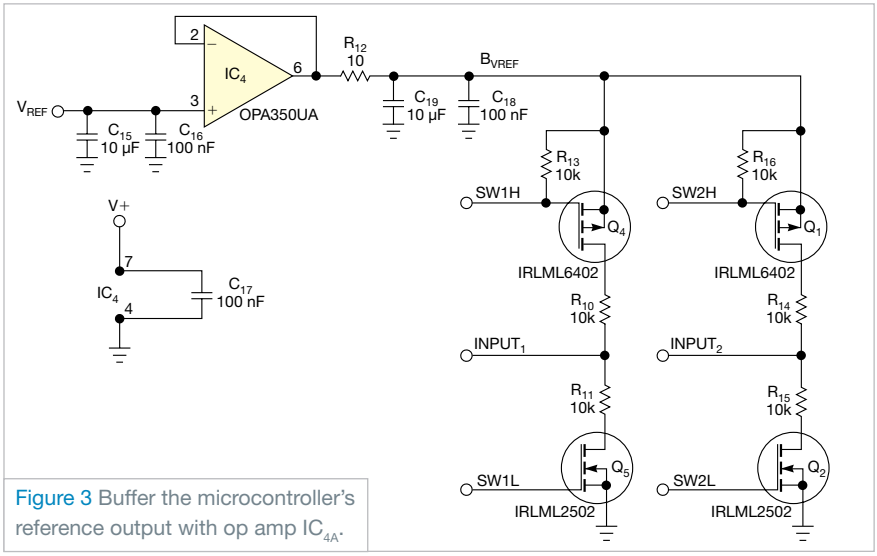

Figure 3 Buffer the microcontroller's reference output with op amp IC_{4A}.

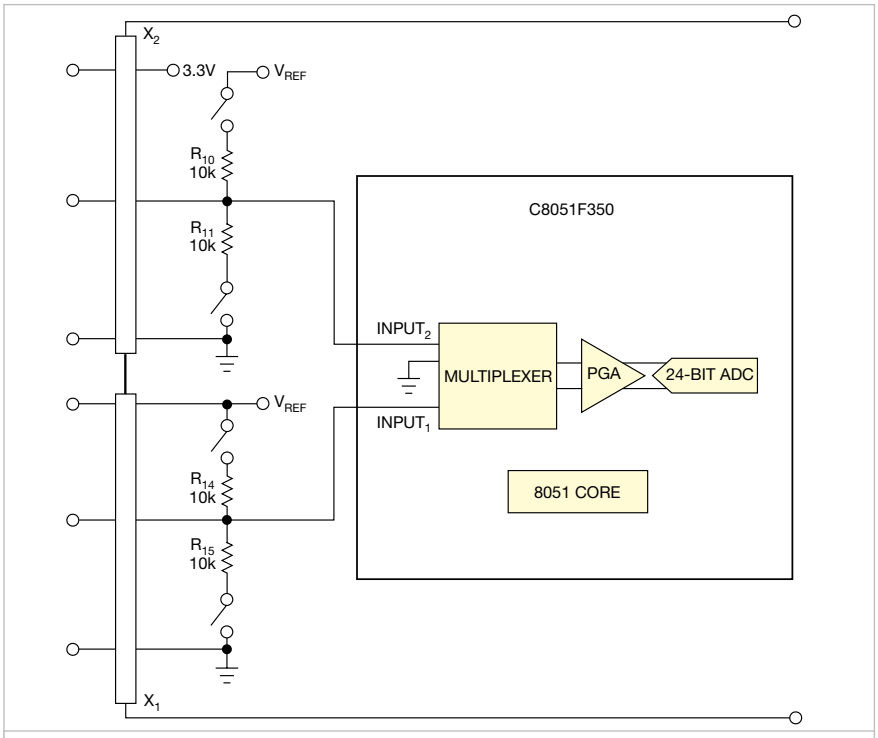

Figure 4 You create two configurable analog ports that allow you to connect many sensor types using two three-input connectors, each of which has a ground pin.

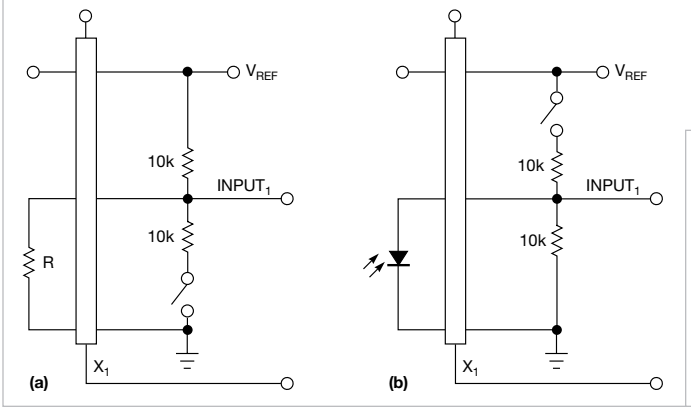

Figure 5 You could configure analog-input port X_1 for a resistive sensor (a) and for a current-output sensor (b), such as a thermistor or a photodiode.

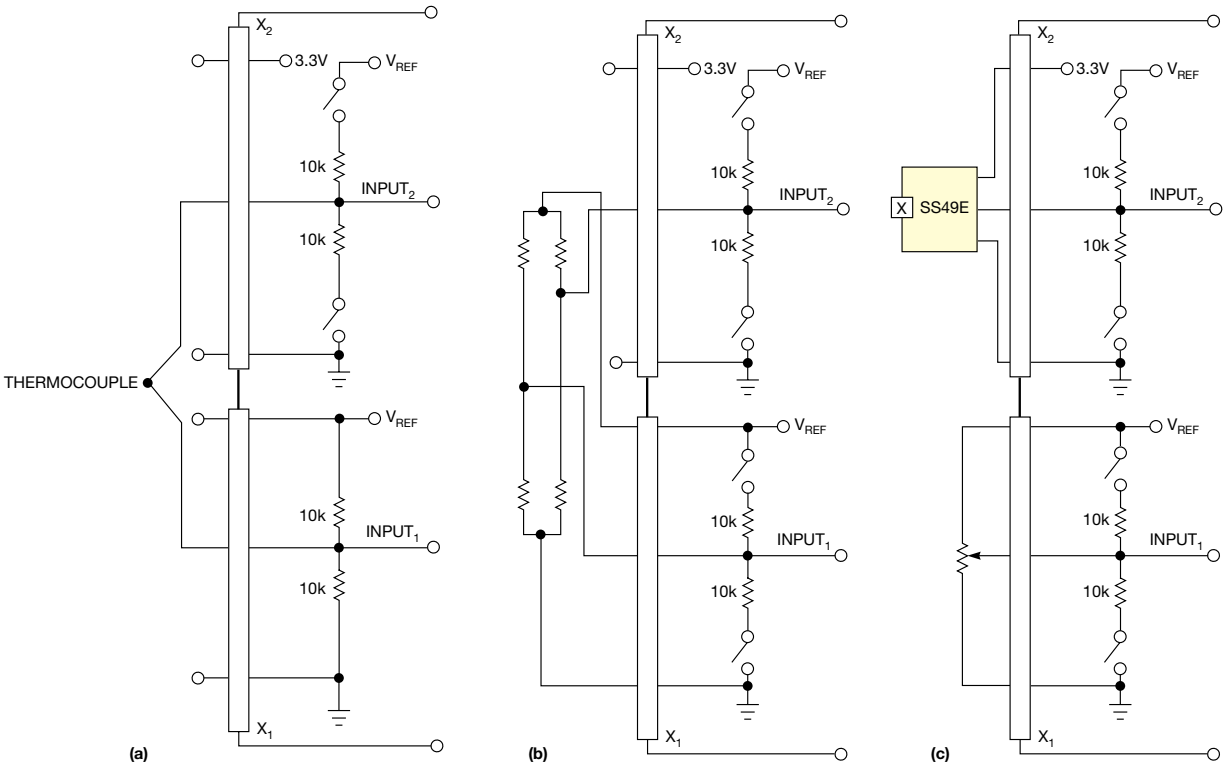

Figure 6 You can directly connect small-output voltage sensors (a), resistor bridges (b), or IC sensors and potentiometric sensors (c).

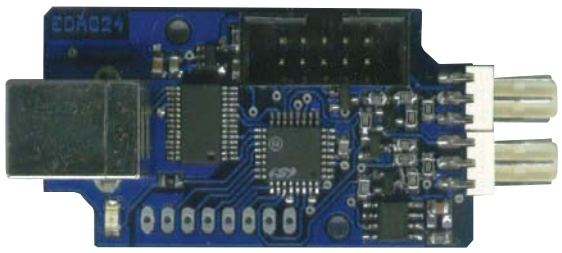

Figure 7 The design fits into a 2.36×1.38-in. enclosure.

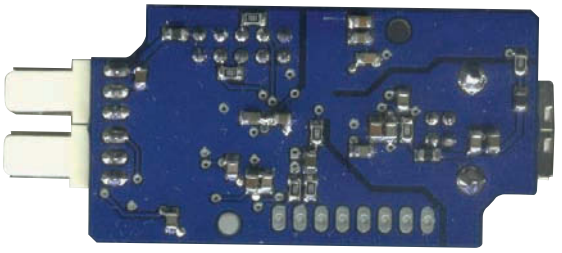

Figure 8 The underside of the PCB holds several passive components.

pickup (**references 2** and **3**). You might need to add external buffer amplifiers or a more precise voltage reference. The availability of a reference voltage and 3.3V power on the analog ports makes this setup possible. You can also use the DAC outputs in connector J_1 to trim a value or to provide an arbitrary voltage to the sensors. Note that J_1 also has five digital-I/O pins (**Figure 1**).

The design fits into a 2.36×1.38-in. enclosure (**Figure 7**). The underside of the PCB holds several passive components (**Figure 8**). **Reference 4** provides details and enables you to download the entire design, as well as CAD/CAM files, bills of materials, and software. EDN

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Originally published in the January 23, 1986, issue of *EDN*

Converters yield droop-free S/H circuit

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In low-frequency applications, many monolithic sample/hold circuits suffer a droop rate that can cause an unacceptably large output error. The S/H circuit in **Fig 1** eliminates droop error by operating two 8-bit multifunction converters back to back. The circuit requires a 5V supply and accepts analog inputs between 0 and 2.5V (although you can scale and offset any input signal to fall within this range).

The analog input is applied to the inverting input of an LM324 op amp (IC_1), which is wired as a comparator. The op amp and the IC_2 multifunction converter form a ramp-and-compare A/D converter. (Because the Ferranti ZN435 multifunction converter includes a voltage-output D/A converter, an 8-bit up/down counter, a 2.5V bandgap reference, and a clock generator, you can configure the device either as an A/D or as a D/A converter.) The converter's internal counter counts from 0, producing a positive-going ramp at the analog output.

When the ramp voltage exceeds the analog input, the comparator output goes high and sets IC_5's Q_1 output high, thus inhibiting IC_2's clock and stopping the counter. IC_2's digital outputs are connected to the digital inputs of IC_3, which is wired as a D/A converter. The D/A converter provides the S/H circuit's analog output.

The output will remain in a hold state until you reset the monostable multivibrator (IC_4), whose outputs apply simultaneous reset pulses to IC_2 and IC_5. The circuit then resamples and holds a new value of analog input. The S/H circuit provides 8-bit hold accuracy for analog input frequencies as high as 1 kHz; you can use a faster op amp for IC_1 for higher-frequency operation. EDN

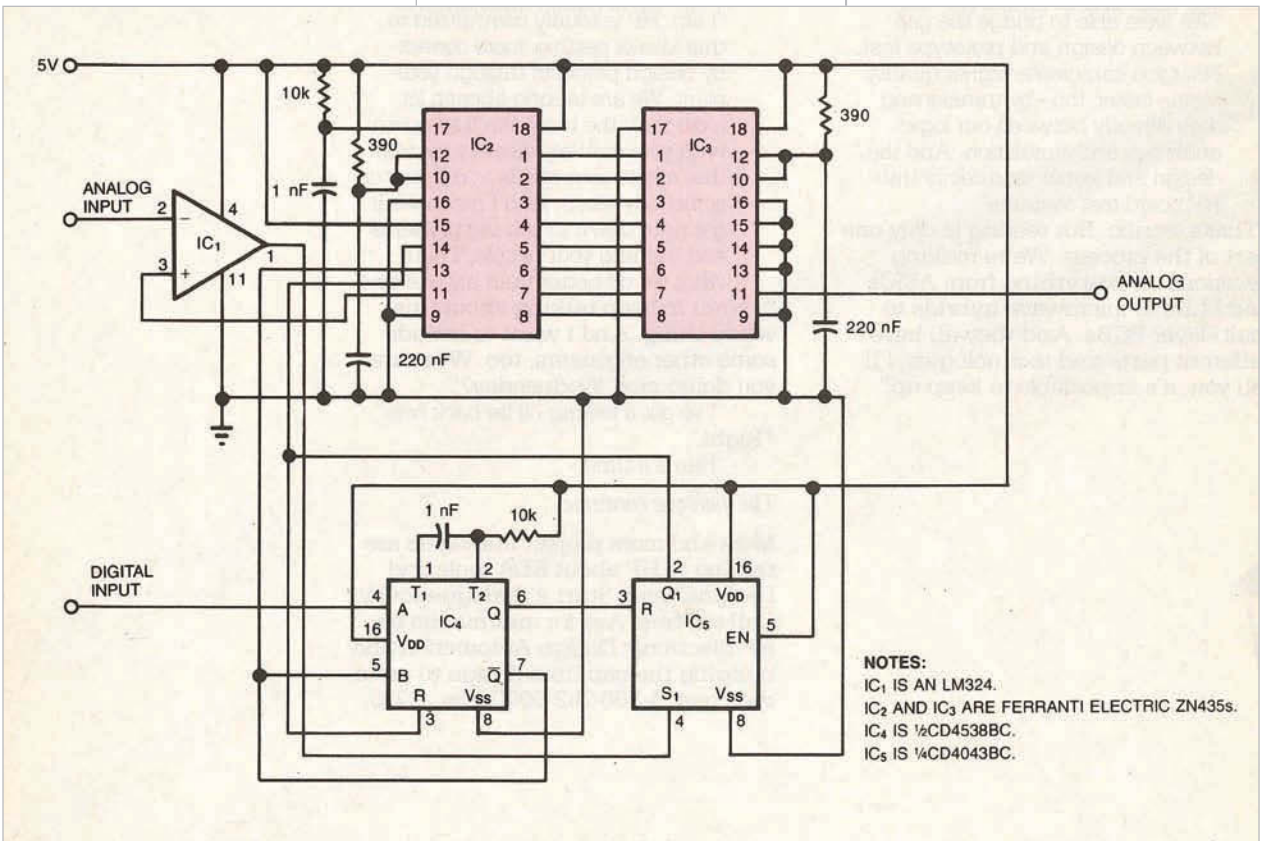

Figure 1 This S/H circuit provides unlimited hold time without droop by digitizing the analog input (IC_2) and converting back to analog using a D/A converter (IC_3).

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

Inexpensive VFC features good linearity and dynamic range

Jordan Dimitrov, Toronto, ON, Canada

VFCs (voltage-to-frequency converters) were favorite circuits of the late analog gurus Bob Pease and Jim Williams (**references 1** to **5**). In tribute to them, this Design Idea reveals a circuit that provides good performance at a low price. You can obtain all of the parts for a few dollars from a local electronics shop.

The circuit has high input impedance, works with a single power supply, and connects directly to microcontrollers. The linearity error is less than 0.1% for frequencies as high as 700 kHz, and the dynamic range is 60 dB. The circuit exploits the integrator, comparator, and one-shot architecture (**Figure 1**). The output frequency is proportional to the input voltage: $f=(1/V_{CC}t_{OS})V_{IN}$, where V_{CC} is the power supply, 5V, and t_{OS} is the duration of the pulse that the one-shot generates, according to the **equation** $t_{OS}=0.7\times R_{OS}\times C_{OS}$. You must filter and regulate the power supply, V_{CC}. If the magnitude of the power supply changes, the slope of the calibration curve also changes. The components you use for the integrator, C_{INT} and R_{INT}, do not participate in the **equation** so they need not be either accurate or stable. However, capacitors C_{INT} and C_{OS} must have low dielectric absorption.

You build a start-up circuit with switch S_1 and the timing network comprising R_1, C_1, and R_2. This step ensures that the circuit will oscillate with any value of input voltage. After you turn on the power supply, the switch stays closed for approximately 1 sec, keeping C_{INT} completely discharged. When the switch opens, C_{INT} starts charging by a fixed current, which the magnitude of the input voltage defines. The result is a rising ramp at the integrator's output. When the ramp reaches 2.5V, IC_2 generates a pulse because 2.5V is the threshold level of the Schmitt trigger at the 1B input of IC_2. Because the pulse magnitude is larger than the input voltage, the current through C_{INT} reverses, and C_{INT} partially discharges (**Figure 2**).

When the pulse is over, the integrator starts another rising ramp, and the cycle repeats. Because of the built-in Schmitt trigger, the circuit requires no separate comparator IC. Most applica-

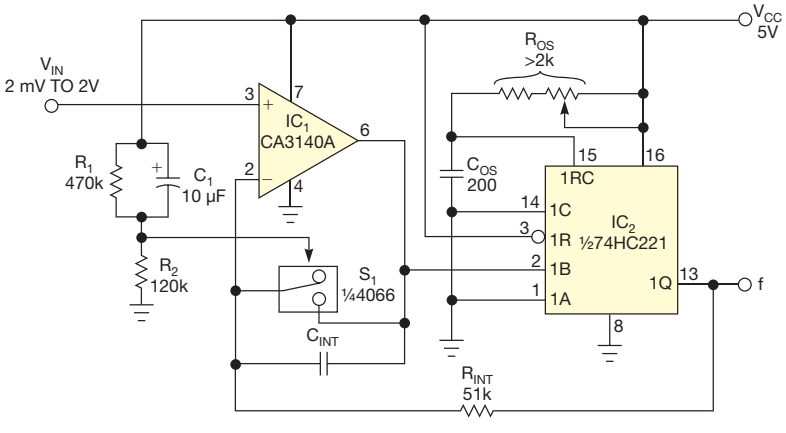

Figure 1 Three inexpensive ICs and a few passive components make a VFC with good linearity, speed, and dynamic range.

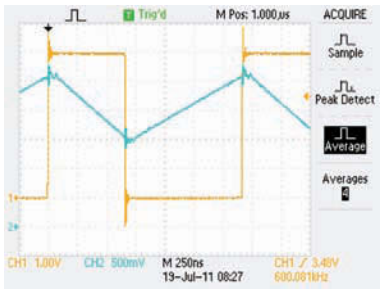

Figure 2 Because the pulse magnitude is larger than the input voltage, the current through C_{INT} reverses, and C_{INT} partially discharges.

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tions can go without any adjustment. You adjust the full-scale frequency using only the trimming potentiometer, which is part of R_{OS} in **Figure 1**.

You can select different frequency spans (**Table 1**), each requiring its own values for C_{INT} and R_{OS}. The spans have different linearity. The **table** shows the linearity error as a percentage of the full-scale frequency for 11 equally spaced values of the input value in a range from 2 mV to 2V. EDN

TABLE 1 PERFORMANCE AT DIFFERENT FREQUENCY SPANS

Maximum frequency (kHz)	Duration of t_{os} (µsec)	R_{OS} value (kΩ)	C_{INT} value (pF)	Linearity (% of full-scale)
50	8	57.2	400	±0.044
100	4	28.6	200	±0.056
200	2	14.2	100	±0.021
400	1	7.15	50	±0.031
600	0.67	4.77	33	±0.066
800	0.5	3.58	25	±0.11
1000	0.4	2.86	20	±0.42

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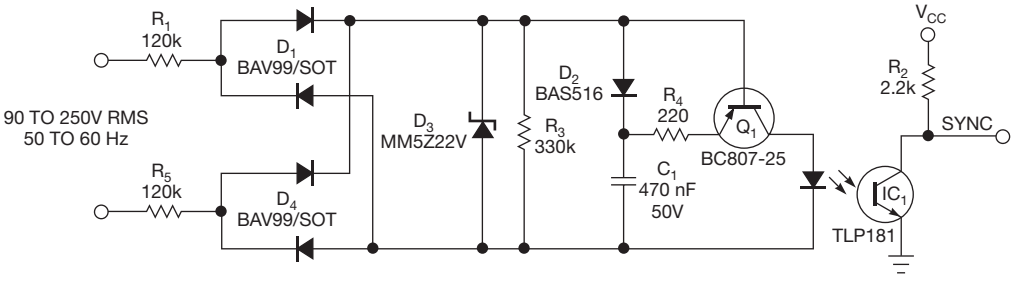
Mains-driven zero-crossing detector uses only a few high-voltage parts

Luca Matteini, Agliana, Italy

The circuit in this Design Idea generates a zero-crossing pulse off the ac mains and provides galvanic isolation. The falling edge of the output pulse happens at approximately 200 µsec before the zero crossing. You can use the circuit to safely stop the triggering of a thyristor gate, giving it time to properly turn off. The circuit generates short pulses only when the mains voltage is approximately 0V, thereby dissipating only 200 mW at 230V and a 50-Hz input.

The circuit charges capacitor C_1 up to the limit that 22V zener diode D_3 creates (**Figure 1** and **Reference 1**). You limit the input current with resistors R_1 and R_5. As the input-rectified voltage drops below the C_1 voltage, Q_1 starts conducting and generates a pulse a few hundreds of microseconds long. The coupling of IC_1 makes the response of Q_1 squarer. The rms operating voltage dictates the only requirement for R_1 and R_5. SMD, 1206-size resistors typically withstand 200V-rms operation. This design splits the input voltage between R_1 and R_5, for a total rating of 400V rms. D_3 limits the voltage across the bridge to 22V so that all of the sub-



NOTES:
YOU CAN LOWER D_3 TO AN 18 TO 20V PART, PERMITTING A LOWER VOLTAGE RATING, SUCH AS 25V, FOR C_1.
R_1 AND R_5 MUST BE 1206-SIZE PARTS TO WITHSTAND THE RMS VOLTAGE ACROSS THEM; 1206-SIZE PARTS ARE USUALLY RATED FOR 200V.

Figure 1 This zero-crossing detector uses low-voltage parts and consumes little power.

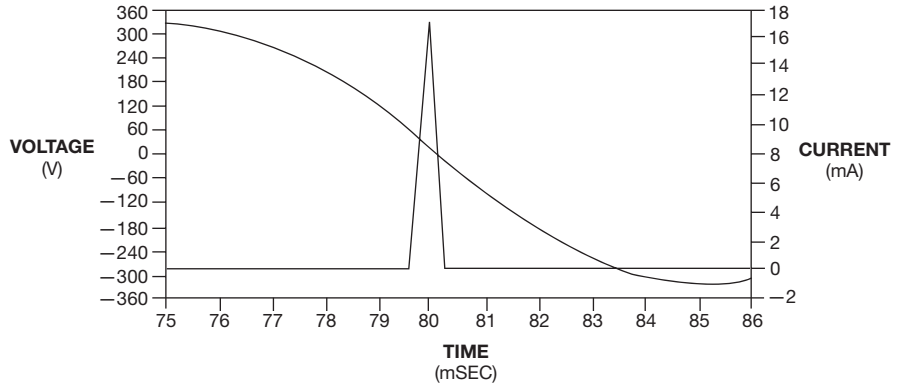


Figure 2 In this LTspice simulation, as the input voltage drops through 0V, the LED current makes a pulse whose edges lead and lag the crossing point. The peak optocoupler-LED current is 17 mA.

WITH A 230V INPUT AT 50V, THE LTSPICE SIMULATION SHOWS A 17-mA PEAK IN THE OPTOCOUPLER LED.

sequent components can have lower voltage ratings. A 22V zener diode can clamp as high as 30V, so this design uses a 50V, 470-nF ceramic capacitor. Ceramic capacitors have better reliability than electrolytic or tantalum capacitors, especially at higher temperatures. If you prefer a cheaper and smaller 25V part, you can change the zener diode's voltage to 18V and still have a good margin for safety. Use R_4 to limit the peak current in the LED. The primary limit on the LED current is the slope of the rectified ac input. The gradual slope doesn't let Q_1 generate current spikes when it discharges C_1's stored energy.

You can simulate the operation of the circuit in LTspice Version IV (**Figure 2** and **Reference 2**). With a 230V input at 50 Hz, the simulation shows a 17-mA peak in the optocoupler LED. The simulation gives good results with inputs of 90 to 250V, both at 50 and 60 Hz. At 110V and a 60-Hz input, the LED current peak is 8.5 mA, so IC_1 still works. If you need higher LED-drive currents, you can reduce the value of R_3 or increase the value of C_1.

Testing a physical circuit shows good correlation with the simulation (**Figure 3**). Driving the isolated output from a 5V logic supply yields a good pulse waveform (**Trace 1**). The mains input is fed to the scope with a 15V isolation transformer for safety (**Trace 2**). You can use the persistence feature of the oscilloscope to show the zero-crossing point when zooming in to the transition (**Figure 4**). This approach allows you to accurately measure the pulse timing relative to the input zero crossing. EDN

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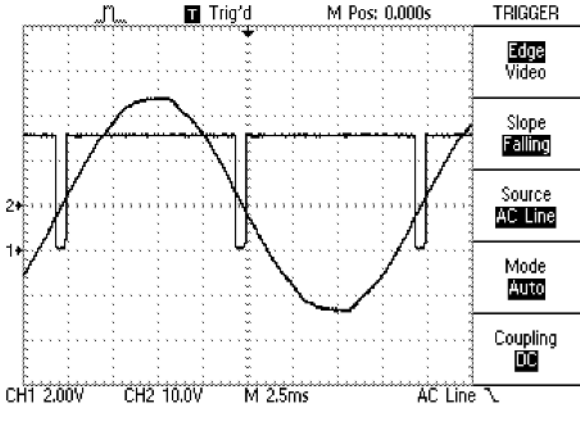

Figure 3 Results for a prototype circuit correlate well with the simulation.

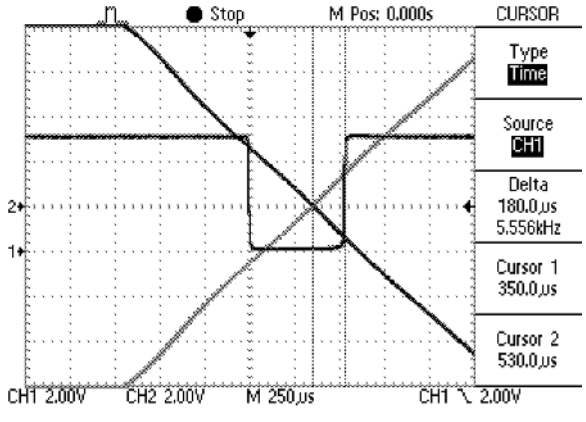

Figure 4 You can use the oscilloscope's persistence function to relate the exact zero-crossing point to the output-pulse timing.

Build an op amp with three discrete transistors

Lyle Russell Williams, St Charles, MO

You can use three discrete transistors to build an operational amplifier with an open-loop gain greater than 1 million (**Figure 1**). You bias the output at approximately one-half the supply voltage using the combined voltage drops across zener diode D_1, the emitter-base voltage of input transistor Q_1, and the 1V drop across 1-MΩ feedback resistor R_2.

Resistor R_3 and capacitor C_1 form a compensation network that prevents the circuit from oscillating. The values in the **figure** still provide a good square-wave response. The ratio of R_2 to R_1 determines the inverting gain, which is –10 in this example.

You can configure this op amp as an active filter or as an oscillator. It drives a load of 1 kΩ. The square-wave response is good at 10 kHz, and the output reduces by 3 dB at 50 kHz. Set the 50-Hz low-frequency response with the values of the input and the output capacitors. You can raise the high-frequency response by using faster transistors and doing careful layout. EDN

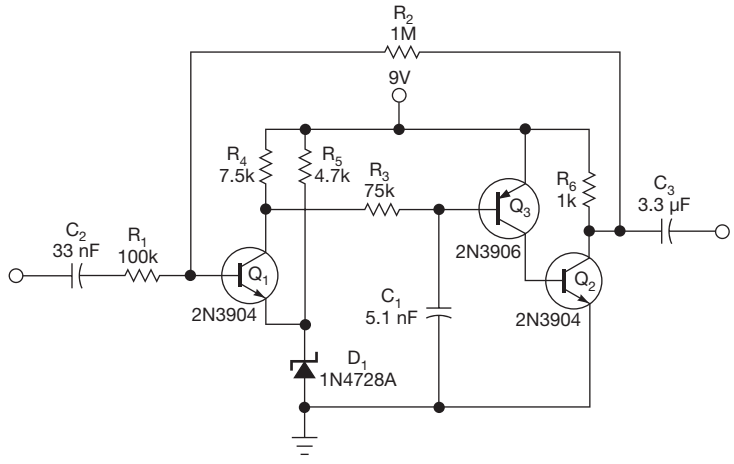

Figure 1 This ac-coupled inverting op amp has an open-loop gain of 1 million. R_1 and R_2 set a closed-loop gain of –10.

A diode ladder multiplies voltage under software control

William Grill, Riverhead Systems, Greeley, CO

The circuit in this Design Idea uses a Microchip 12F10 controller to drive a voltage multiplier ladder and a single pin to output status and to input a trigger signal you supply (**Figure 1**). When you trigger the signal, the software turns on a MOSFET to connect the multiplier output to a load. The microcontroller has an internal comparator with a 0.6V trip point. The circuit attenuates and feeds back the output voltage to this comparator.

Listing 1, which is available at www.edn.com/111201dia, shows the controller-based software, which stops the oscillator, driving the voltage multiplier when the internal comparator indicates that the output voltage has reached an upper limit. This circuit works in a wireless-monitor design, increasing the voltage, power, and range of a small periodic transmitter. It can provide 12 to 15V and 9 to 11 mA.

Processing begins when power is applied. The controller qualifies its Port 3 input on Pin 4. When at a logic high, logic is true, and the software code generates complementary PWM outputs on ports 4 and 5, which are pins 3 and 4, respectively.

These oscillations charge the ladder network. The controller outputs a low on the Port 2/Pin 5 status line, indicating that charging is under way. You choose the ratio of R_1 and R_2 so that the center node of the ladder is at 0.6V when the output voltage reaches the desired value. When the output reaches the final value, the controller puts the status pin in tristate mode, and the 20-kΩ resistor pulls the pin up to the power-rail voltage. Port 2 on Pin 5 then becomes an input.

When you pull this pin low, the microcontroller asserts Port 1 and Pin 6 high, turning on the P-channel MOSFET through Q_2, and applies the output voltage on C_4 to the load. Meanwhile, Port 1 and Pin 6 go high, shifting the lower pin of output capacitor C_4 from ground to the power rail and adding a few volts to the output of the voltage ladder.

The program drives the complementary outputs at pins 2 and 3 with a 700-µsec PWM period with a 50% duty cycle. You can change the software code to vary these parameters. The controller has an internal 4-MHz oscillator and supports a user-settable reference block. The code continues to monitor the enable pin, C_4's voltage feedback, and the pump operation during the discharge to the load. You must set certain bits in the processor configuration for this code to work (**Figure 2**). EDN

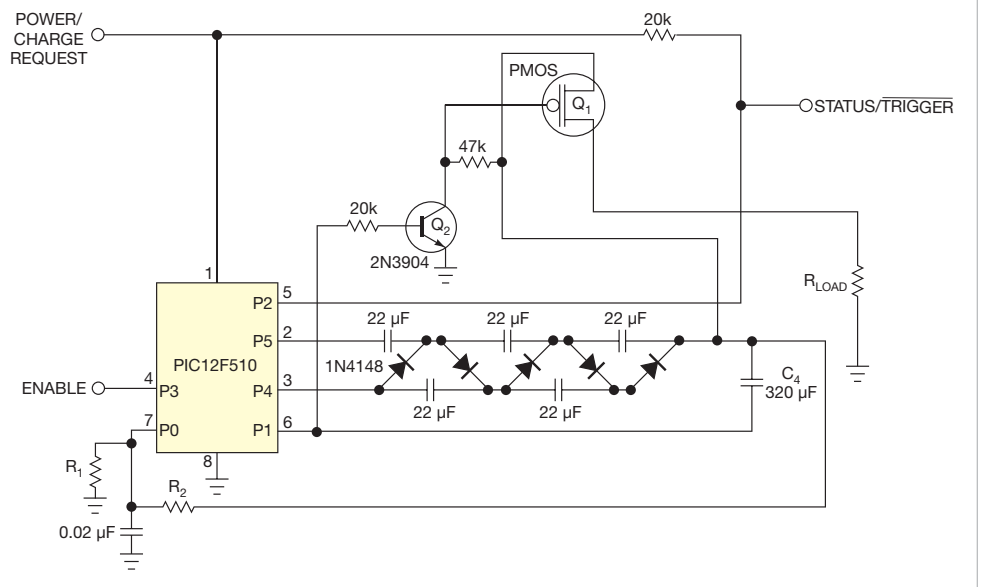

Figure 1 This circuit boosts 3V to a regulated 12V and connects the multiplied voltage to a load under software control.

Configuration Bits

Setting
INTOSC with 1.125 ms DRT
WDT disabled
Code protection off
GP3/MCLR pin functions as GP3, MCLR internally tied to VDD
4 MHz INTOSC Speed

Figure 2 Set these configuration bits for proper operation of the software code in the microcontroller.

Originally published in the February 7, 1985, issue of *EDN*

Charger extends lead-acid-battery life

Fran Hoffart, National Semiconductor Corp, Santa Clara, CA

A circuit that properly charges sealed lead-acid batteries ensures long, trouble-free service. **Fig 1** is one such circuit; it provides the correct temperature-compensated charge voltage for batteries having from one to as many as 12 cells, regardless of the number of cells being charged.

The **Fig 1** circuit furnishes an initial charging voltage of 2.5V per cell at 25°C to rapidly charge a battery. The charging current decreases as the battery charges, and when the current drops to 180 mA, the charging circuit reduces the output voltage to 2.35V per cell, floating the battery in a fully charged state. This lower voltage prevents the battery from overcharging, which would shorten its life.

The LM301A compares the voltage drop across R_1 with an 18-mV reference set by R_2. The comparator's output controls the voltage regulator, forcing it to produce the lower float voltage when the battery-charging current passing through R_1 goes below 180 mA. The 150-mV difference between the charge and float voltages is set by the ratio of R_3 to R_4. The LEDs show the state of the circuit.

Temperature compensation helps prevent overcharging, particularly when a battery undergoes wide temperature changes while being charged. The LM334 temperature sensor should be placed near or on the battery to decrease the charging voltage by 4 mV/°C for each cell. Because batteries need more temperature compensation at lower temperatures, change R_5 to 30Ω for a TC of −5 mV/°C per cell if your application will see temperatures below −20°C.

When the circuit charges more than six cells, the additional voltage across the LM334 increases self-heating, so use a small heat sink and increase the resistance of R_6. Likewise, use higher resistances in series with the LEDs to avoid overloading the LM301A.

The charger's input voltage must be filtered dc that is at least 3V higher than the maximum required output voltage: approximately 2.5V per cell. Choose a regulator for the maximum current needed: LM371 for 2A, LM350 for 4A, or LM338 for 8A. At 25°C and with no output load, adjust R_7 for a V_{OUT} of 7.05V, and adjust R_8 for a V_{OUT} of 14.1V. EDN

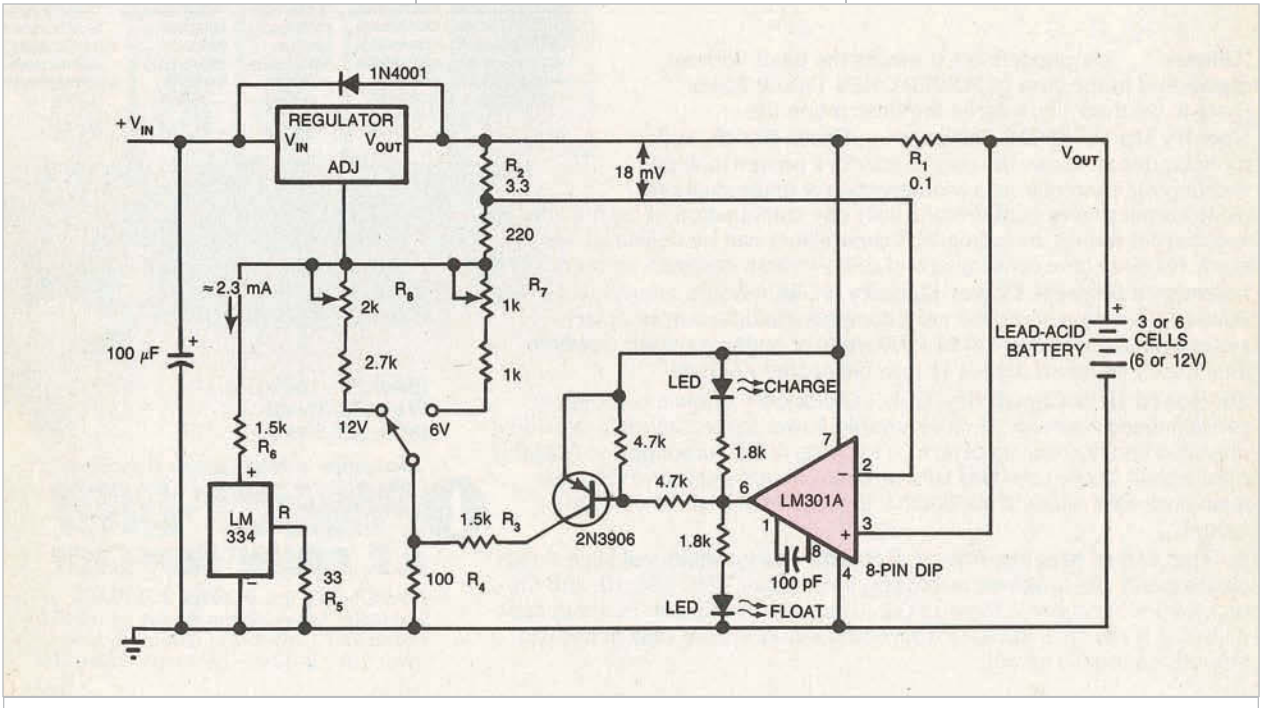

Figure 1 This circuit charges lead-acid batteries by applying 2.5V per cell (at 25°C) and floats them at 2.35V when they are fully charged. Use an LM371 regulator for a 2A rating, an LM350 for 4A, or an LM338 for 8A.

EDITED BY PAUL RAKO
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Circuit provides more accurate multiplication

Yakov Velikson, Lexington, MA

Common analog multiplying devices employ methods using transistor parameters. Precise versions of these devices use the logarithm method of multiplication. This method involves the addition of logarithms and an exponential conversion (**Reference 1**). Using these methods, you can achieve a minimal error of ±0.1%. This Design Idea reduces the error, employs readily available standard components, and maintains the correct voltage scale.

The structure squares the sum and the difference of both components of the desired multiplication. The difference of these squared values yields the result of the multiplication. You can scale the desired multiplication of a and b using the identity of $4ab=(a+b)^2-(a-b)^2$. In a conceptual diagram, blocks 1 and 2 represent the input part of the device (**Figure 1**). They comprise identical precise rectifiers. You implement these rectifiers with amplifiers A_1, A_2, A_3, and A_4 (**Figure 2**). They provide the addition and the subtraction of input voltages V_A and V_B. The rectifiers create the output voltages $k(V_A+V_B)$, $k(V_A-V_B)$, which have only positive polarity. You connect these outputs to a two-channel ADC, Block 3, and then to two identical DACs: DAC_1 (Block 4) and DAC_2 (Block 5).

The ADC converts $k(V_A+V_B)$ and $k(V_A-V_B)$ to proportional codes N_1 and N_2. The ADC must handle the conversion over the full range of the absolute sum $|k(V_A+V_B)|$. The reference voltage of the ADC should be equal to the maximum expected value of $|k(V_A+V_B)|$. Codes N_1 and N_2 translate to Register 1 of DAC_1 and Register 2 of DAC_2, respectively (**Reference 2**). These codes establish the values on the R–2R dividers of each DAC. The output voltages of blocks 4 and 5, comprising $N_1|k(V_A+V_B)|$ and $N_2|k(V_A-V_B)|$, pass through operational amplifier A_7 in Block 6. You configure the op amp with a differential input, which takes the difference between the inputs and creates the multiplication result on the output. For example, if both voltages V_A and V_B have a range of ±10V and the input range of the ADC is 0 to 10V, then coefficient $k=R_2/R_1=0.5$. The full sum of each part should be ±10V. **Table 1** provides the results for all four quadrants of these conditions.

The systematic error of the multiplication is the sum of the discrete errors

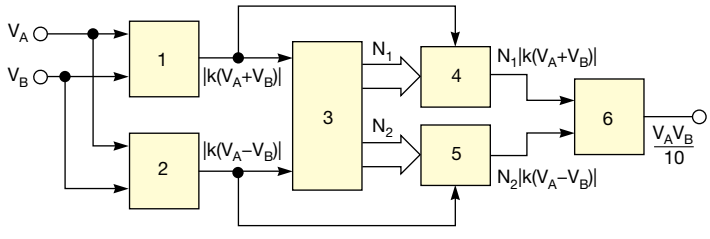

Figure 1 Perform a multiplication of two values, V_A and V_B, by using ADCs, DACs, and amplifiers to do the mathematics of an equivalent expression.

DIs Inside

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TABLE 1 RESULTS OF FOUR QUADRANTS

V_A (V)	V_B (V)	$k(V_A+V_B)$ (V)	$k(V_A-V_B)$ (V)	N_1	N_2	V_5 (V)	V_6 (V)	V_5-V_6 (V)
5	3	4	1	0.4	0.1	–1.6	–0.1	1.5
5	–3	1	4	0.1	0.4	–0.1	–1.6	–1.5
–5	3	1	4	0.1	0.4	–0.1	–1.6	–1.5
–5	–3	4	1	0.4	0.1	–1.6	–0.1	1.5

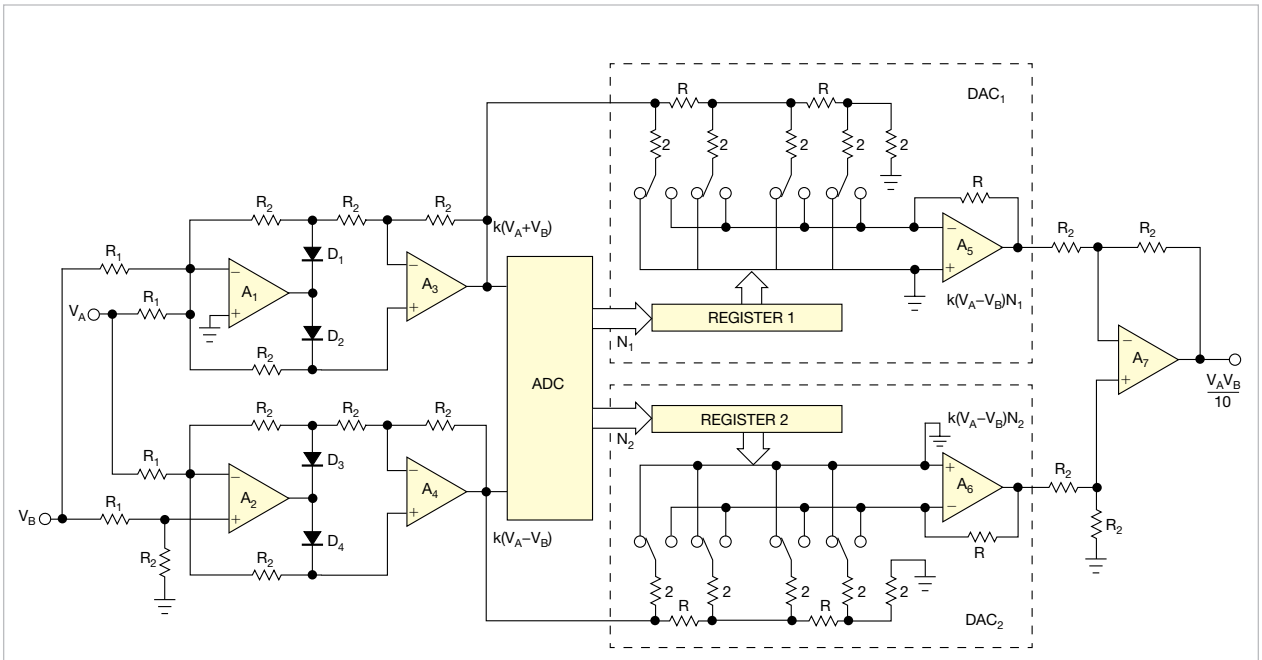

Figure 2 The detailed schematic of the multiplier follows the block diagram of Figure 1.

of the ADC and both DACs. This error depends on the resolutions of these devices. Choosing an ADC and DACs with greater resolutions will further reduce the overall error. EDN

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A few added components make a self-contained controller for 100A load

Steve Hageman, AnalogHome.com, Windsor, CA

The late Jim Williams' last project was a 100A active load (**Reference 1**). That design needed a separate signal generator and other components. This Design Idea makes the load self-contained. It adds potentiometers to control the stepped load levels, a chopper oscillator to switch between the set load levels, and a dual-readout DPM (digital-panel meter) to allow for direct voltage and current readout. In tribute to Williams, it uses three Linear Technology chips.

The heart of the load controller is two potentiometers, Set A and Set B (**Figure 1**). These devices allow you to set A and B load levels anywhere in the 0 to 100A-load-range capability of Williams' design. For instance, assume that Set A is at –0.5V and Set B is at –0.75V. Switching the load between these two levels changes it from 50 to 75A. Timer chip IC_1 controls the stepping rate and duty cycle between the Set A and the Set B levels. This timer IC allows you to control frequency over a decade range. It also allows you to set the duty cycle between 0 and 100%.

The full 0 to 100% duty-cycle control comes in handy when you set up the load. At 100% duty cycle, the voltage between the potentiometers does not switch, and the Set A control is active alone. This situation allows you to adjust Set A and watch the actual dc level on the dual-readout panel meter. Likewise, setting the duty-cycle control to 0% switches to the Set B potentiometer and allows you to adjust its static or dc level.

THE FULL 0 TO 100% DUTY-CYCLE CONTROL COMES IN HANDY WHEN YOU SET UP THE LOAD.

Setting any duty cycle other than 0 or 100% causes the Set A and Set B levels to alternate. You control the chopping frequency by adjusting the fre-

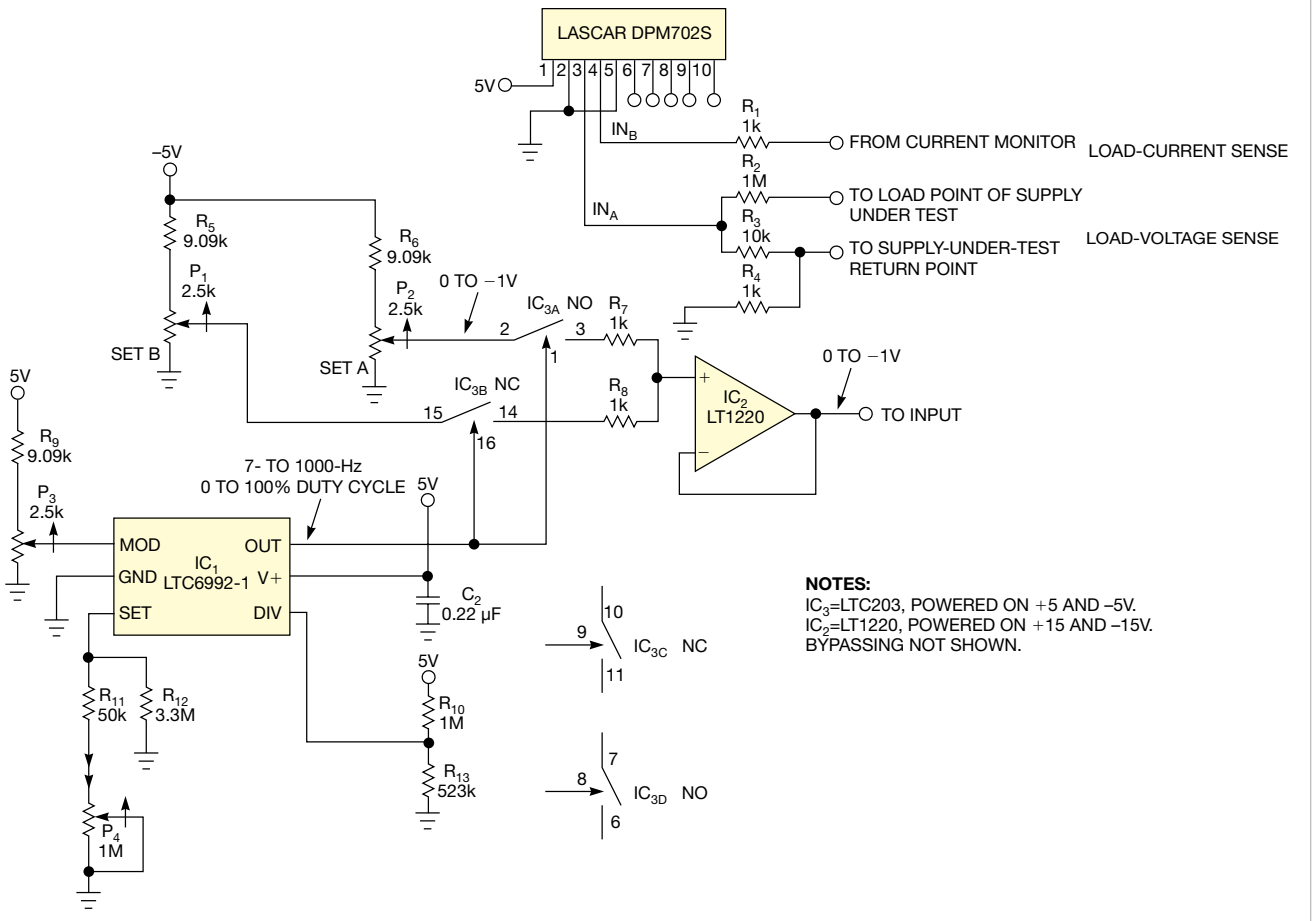

Figure 1 Adding this circuit to a 100A active load makes a stand-alone piece of test equipment.

quency potentiometer, P_4. A frequency of 60 to 1000 Hz best suits use in large power supplies. You can adjust the values of the resistors to get chopping frequencies of 4 Hz to 1 MHz.

Take care with the physical mounting of potentiometer P_4. Any stray capacitance on the Set pin of IC_1 is detrimental to its proper operation. Resistors R_{11} and R_{12} should be placed next to IC_1. You can wire potentiometer P_3 a few inches away for panel mounting.

Connect the labeled points in **Figure 1** directly to the labeled points in Williams' original schematic. You should change the 51Ω resistor at the earlier circuit's Input pin to something on the order of 1 kΩ. IC_2 should be close to the previous design's A_1 amplifier. You can slightly optimize the pulse's shape if necessary by adjusting the 300-pF capacitor at the input to A_1 on the original design.

The dual-readout DPM from Lascar Electronics is handy in active-load applications (**Reference 2**). The dual 3½-digit voltmeter has a ±1.999V input and has built-in annunciations for amperes and volts. Set the decimal place to the proper location by soldering jumper pads on the back of the unit.

This design connects the voltmeter across the load terminals but doesn't compensate for voltage drop on the leads connecting the load to the power supply. At the 100A level, the voltmeter doesn't provide the kind of accuracy that load-regulation testing requires. The voltage indication at the load is useful, however. It provides adequate indication that the power supply under test is still regulating and that the test leads connect properly to the load. If you need a more accurate reading, it is a simple matter to connect a 6½-digit bench DMM (digital multimeter) directly to the power supply under test. EDN

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Simple night-light uses a photoresistor to detect dusk

Chau Tran, Analog Devices, Malden, MA

Streetlights, emergency lights, and security lights must automatically turn on when it gets dark. You base the control circuit on the resistance of a photoresistor or another LDR (light-dependent resistor) that varies with light intensity. An LDR's resistance of several megohms in darkness decreases to a few hundred ohms in bright light (**Figure 1**). This feature allows a circuit to distinguish between one light bulb and two, direct sunlight or total darkness, or anything in between.

You can use an LDR in a circuit that detects darkness and turns on an LED (**Figure 2**). The circuit uses a high-voltage threshold-detector IC that features a current output and operates as a comparator. The LDR and potentiometer R_3 form one side of a Wheatstone bridge. Fixed resistors R_1 and R_2 form the other side. You can operate the circuit from a 5 to 65V battery because the bridge excitation comes from an on-chip 2.4V series regulator that is referenced to the supply voltage. The chip keeps the 2.4V regulation voltage below the supply voltage. Resistors R_1 and R_2 form a fixed reference voltage at the noninverting input of internal comparator A_1. The LDR and R_3 form a variable voltage at the inverting input. When the light level falls, the voltage on the inverting input falls below the reference voltage until the comparator trips, activating the relay and the LED. The total voltage across the resistors is always 2.4V. Choose the values for these resistors based on your desired threshold voltage using the **equation** $V_{TH}=-2.4\times(R_1/(R_1+R_2))=-2.4\times(LDR/(R_3+LDR))$, where V_{TH} is the threshold voltage.

YOU CAN ADJUST THE POTENTIOMETER TO PRESET THE SWITCH TO ANY LIGHT LEVEL, MAKING IT AN IDEAL LIGHT SENSOR.

You can reverse the position of the LDR and potentiometer R_3 to switch on the relay when the light exceeds a preset level. You can adjust the potentiometer to preset the switch to any light level, making it an ideal light sensor. The IC's output current is less than 100 nA when the negative pin's value is greater than that of the positive pin. The output current goes to 1 mA when the positive pin's value is greater than that of the negative pin. This current drives a ground-referenced resistor to develop a logic-level signal at D_{OUT}. The logic signal is buffered with the NPN transistor that then drives relay switch S_1. You should use a latching relay, which uses permanent magnets to hold the armature in place after the drive current is removed.

When you turn on the LED, the resistance of the LDR may decrease dramatically, and the comparator will switch off, cutting back the output current to nanoamps while the latching relay keeps the light on. EDN

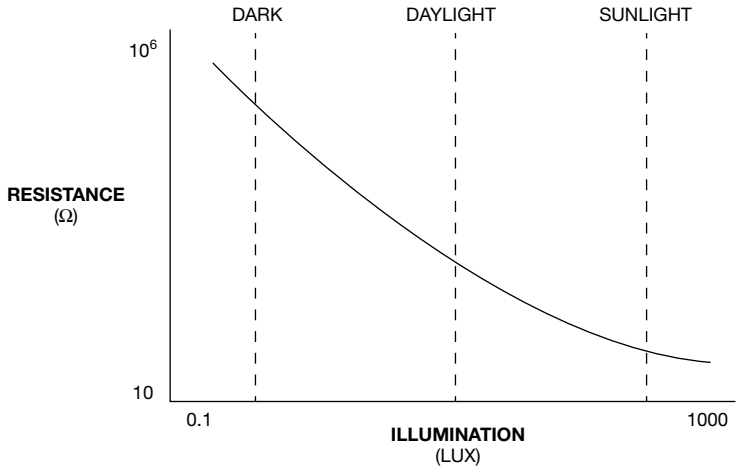

Figure 1 The resistance of a photoresistor falls dramatically as you illuminate it.

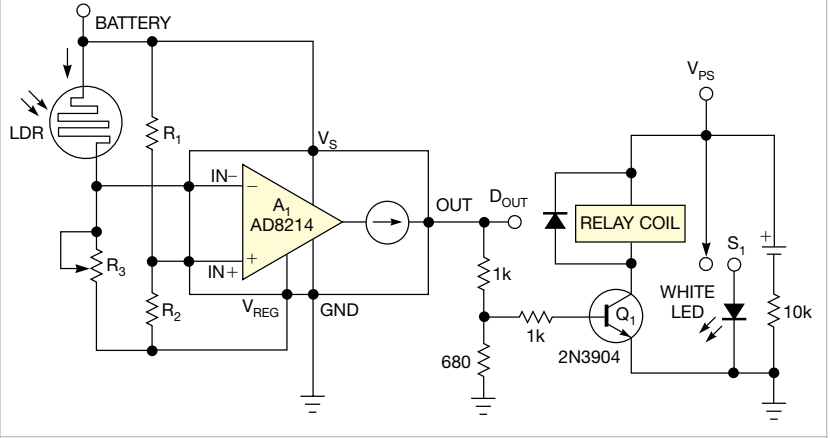

Figure 2 This night-light circuit turns on as the illumination on the photoresistor dims.

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Originally published in the December 23, 1999, issue of *EDN*

Simple tester checks Christmas-tree lights

William Dias, Brown & Sharpe, North Kingstown, RI

Why is it that you always test 48 bulbs before you find the bad one in a 50-light string? The simple circuit in **Figure 1** allows you to divide and conquer, greatly reducing the time it takes to find the bad bulb. The circuit uses a pair of NE2 neon bulbs with current-limiting resistors. You can use a pair of Radio Shack 272-1100 bulb-resistor sets. It's convenient to house the tester in a clear piece of plastic tubing, with the probe tip emerging from one end and a light-duty power cord emerging from the other end. You place the bulbs in the tube such that one is close to the probe tip and the other is near the power cord, so it's easy to remember which bulb lit last. The probe tip connects to the common point between the neon bulbs. It consists of thin spring wire with all but the last ¼ in. insulated. You use the bare tip to make contact with the crimp connectors in the base of the bulbs.

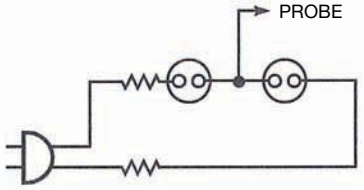

Figure 1 A simple probe set cuts the time you spend troubleshooting a series-string light set.

Series-string Christmas-tree lights come in two types. The first type is the continuous-series string (**Figure 2a**). In this configuration, one wire from the plug goes from bulb to bulb until it reaches the last bulb. A return wire bypasses all the bulbs and returns to the plug. The second type is the alternating-series string (**Figure 2b**). In this connection, one wire from the plug goes to the first bulb, and the other wire from the plug goes to the second bulb. The connections then alternate through the string. To troubleshoot a defective continuous-series string:

- Plug in both the tester and the bulb set.
- Insert the tip of the tester's probe into the wire hole in the base of the first bulb. One of the neon bulbs should light; remember which one.
- Move halfway down the set and insert the probe again. If the same neon bulb lights, then the problem is in the second half of the set. If the other neon bulb lights, then the problem is in the first half of the set. Either way, you are testing 25 of the 50 bulbs without breaking into a sweat.
- If the original neon bulb lights, move halfway down the remaining part of the set and try again. If the other neon bulb lights, you must move back halfway to the last bulb you tested and try again. This process should allow you to find a bad bulb in a set of 50 in only seven steps. You know you have the bad bulb when inserting the probe tip into one side of the bulb lights one neon bulb and placing the tip in the other side lights the other neon bulb.

To troubleshoot a defective set with many bad bulbs, use the same process as above. At some point, you will reach the dead spot between two or more bad bulbs. When you reach this point, neither neon lamp will light. Back up, just as if the other neon bulb had lit. You know you have a bad bulb if the probe lights when you plug it into one side and nothing lights when you plug it into the other side. Replace this bulb and start over.

To troubleshoot an alternating-series string, you must work in pairs. Test the first bulb, and one neon bulb lights. Test the second bulb, and the other neon bulb lights. Now move down the set an even number of lights and test the next pair of lights. When you pass the bad bulb, the same neon lamp lights for both series-string bulbs. EDN

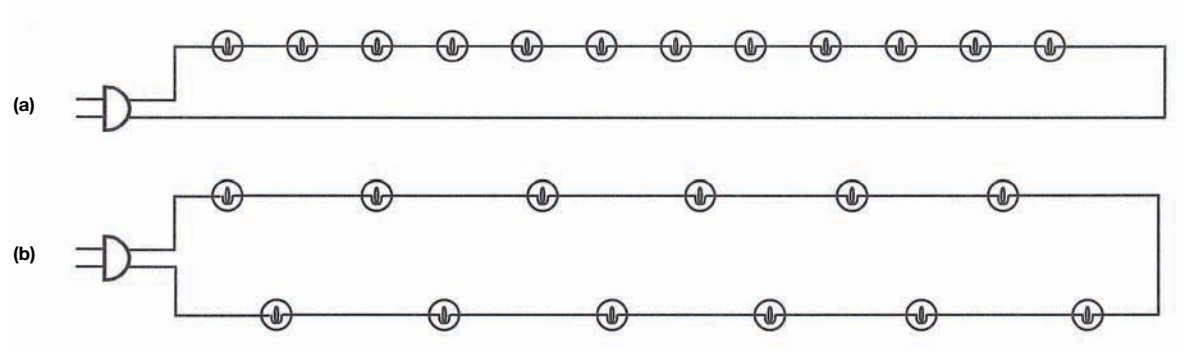

Figure 2 Series-string light sets come in two flavors: a continuous-series string (a) and an alternating-series string (b).