Design Ideas from EDN

January 1999 pag.6 μ C reprograms audio DAC via serial interface Calibrated trim tool tweaks multiturn pots Off-the-shelf watchdog serves in a pinch Novel circuit controls ac power Two AA cells power step-down regulator Temperature controller keeps IR detector at 8°K Flyback circuit provides isolated power conversion RISC μ P implements fast FIR filter Simple algorithm transforms filter coefficients Door/window sensor resists tampering Use a trick to count scope events A primer on binary-arithmetic rounding Light powers isolation amplifier Low-cost feedback circuit boosts efficiency

February 1999 ADC circuit optimizes key encoding RS-232C circuit has galvanic isolation Digital pot adjusts LCD's contrast Add speech encoding/decoding to your design Cheap PWM IC makes synchronous gate driver Circuit detects total on-time Simple circuit provides efficient PWM Visual Basic models MDAC offset Charge-pump circuit divides by two Pass transistor lowers dropout voltage PIC μC implements CRC-16 algorithm Monostable makes low-cost F/V converter

March 1999

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April 1999

Shift register makes a fast counter RS-232C monitor operates without a power supply Simple circuits control RC servos One amplifier makes one-shot High-power latch provides 48V, 10A Tiny IC debounces pushbutton switch Back-to-back FETs thwart reverse current

May 1999

Switching regulator drives robot motor Simple fix adds door-chime repeater Clock multiplier circumvents PLL Synthesize optimal digital-frequency dividers Voltage regulator controls scanner-lamp brightness Simple changes improve Schmitt trigger Access odd memory locations without hardware Charge indicator gauges lead-acid batteries Use derivatives to catch RF calibration errors µC-based circuit performs frequency multiplication Kick start a crystal oscillator in Spice

June 1999

Missing-codes tester checks 16-bit ADC in 7 sec Switch-mode supply draws 43-mW standby power Circuit rejects ambient light V/I converter accommodates grounded load Digitally controlled potentiometer sets cutoff frequency Precision reference bans precision resistors Easy method calculates comparator trip points Controller supports differential monitor display Ultrasonic range finder uses few components Simple technique improves transient dynamics Multiplying DAC makes programmable resistor Equip switchers with overcurrent protection

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Comparator has programmable limits DAA circuit emulates central-office operation Speedy logic translator uses little power Parallel port replaces embedded μ C Transimpedance amp covers dc to gigahertz range Simple scheme detects shorts High-isolation converters use off-the-shelf magnetics Autoranging circuit simplifies hardware and software Simple technique speeds Microstrip breadboarding Comparator has independent trip voltages Modem-access adapter reduces interference Synchronous oscillator converts audio, video to FM

August 1999

Scheme extends DDS phase-shift resolution Single μ C pin makes half-duplex RS-232C Binary counter uses LSB feedforward Simple logic reduces EMI Emergency strobe flasher generates 250V 3.3V lithium-cell supply requires one inductor Circuit monitors quad supply for PCI systems Circuit controls multiple thermoelectric coolers Current-input ADC measures voltages You've got mail Circuit provides brownout control of 80C31 Circuit emulates mechanical metronome PC controls light dimmer

September 1999

DDS device provides amplitude modulation Charge pump converts V IN to \pm V OUT Electronic SPDT controls two PCs GMR sensors manage batteries Driver thermally compensates LED Program turns PC sound card into a function generator Li-ion battery charger adapts to different chemistries Current-sense amplifier precisely measures low side Connect a modem to a Basic Stamp Bias supply provides short-circuit protection Analog multiplier works over large frequency range 5V logic pulser is battery-powered Square-root function improves thermostat μ C detects transmission rate of RS-232 interface Current sensor measures 0 to 500A Safely swap SCSI disk drives SSB modulator covers HF band Switched-capacitor IC forms notch filter

October 1999 PC and DACs generate two simple analog outputs Dual 8-bit ADCs provide pseudo high resolution Disturbance simulator checks lines Circuit latches solenoids at a distance Dual supply suits portable systems Zener diode and MMICs produce true broadband noise Comparator exhibits temporary hysteresis Fast algorithm computes histograms Loop powers current transmitter Spice creates time-variant resistor VCO supply touts low noise μ C forms FM oscillator Circuit converts pulse width to voltage Restore dc to NRZ sigmals

November 1999 Controller IC halves switcher's standby power Load detector controls power sources Two-wire interface has galvanic isolation Measure power-on current transients on ac line Generator has independent pulse width, frequency Customized potentiometers aid amplifier design Ring your bell; light your light Voltage regulator goes digital Supply converts 5V to-48V C routine speeds decimal-to-binary conversion Resistor implements half-duplex RS-232 with echo Circuit monitors ac-power loss RF transmitter uses AMI encoding High-voltage regulator is 100%-surface-mountable

December 1999 Scheme cancels amplifier error Serial port provides interrupts for 8031µC ADC-to-PC interface transfers data in nibbles Matched offsets put signals into ADC's range Amplifier compensates piezoelectric-rate gyros Digital camera subs as a scope camera MOSFET pair makes simple SPDT switch Motor controller operates without tachometer feedback Cascade ABCD two-port networks Simple tester checks Christmas-tree lights Power meter uses low-cost multiplier Add music to your next project PWM circuit uses fuse to sense current Bias supply accepts high inputs Method provides simple error-rate generator Edited by Bill Travis and Anne Watson Swager

μC reprograms audio DAC via serial interface

³ⁿideas

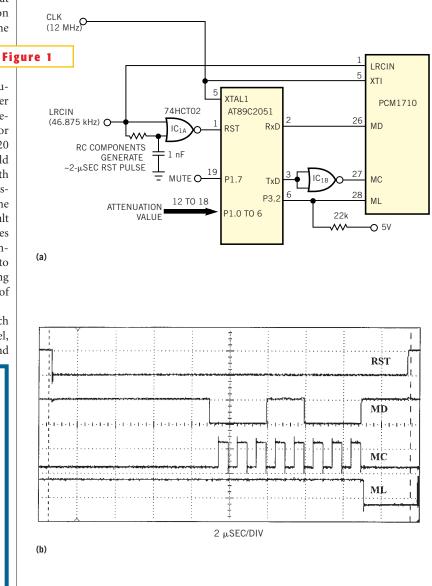
Lukasz Sliwczynski, University of Mining and Metallurgy, Institute of Electronics, Cracow, Poland

OU CAN USE A SIMPLE μ C to continuously program an audio DAC so that it operates in a 20-bit resolution mode (**Figure 1**). After power-on, the

PCM1710 $\Delta\Sigma$ DAC (Burr-Brown Corp, www.burr-brown.com) operates in its default 16-bit resolution mode. Switching to its 20-bit resolution mode requires supplying the converter with a control word using its three-wire serial digital interface (SDI). A risk exists for using this converter at a resolution of 20 bits in a transmission system that should work 24 hours a day, seven days a week with no, or only occasional, supervision. A disturbance can cause reprogramming of the converter and cause it to revert to its default settings. The circuit in Figure 1 eliminates this possibility by repeatedly reprogramming the DAC. The circuit uses the SDI to continuously supply three programming words, which define the converter's state of operation, to the DAC.

The reprogramming circuitry, which uses a popular AT89C2051 µC (Atmel, www.atmel.com), has few components and

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A simple μ C-based circuit (a) continuously reprograms the PCM1710 audio DAC for a resolution of 20 bits. The μ C sends 1 byte of code after each RST pulse (b).

www.ednmag.com



is power-efficient (**Figure 1a**). Because any μ C system is also vulnerable to external disturbances, it's best to reset the μ C repetitively. The circuit uses the LRCIN signal to reset the μ C and invoke the programming procedure. The LRCIN signal also switches digital-audio words between the left and right channels of the converter. Thus, the μ C takes less time to execute the program than the period of the LRCIN signal. The sampling rate is 46.875 kHz, so the period of the LRCIN signal is approximately 21 μ sec. The circuit must devote some of this time to properly resetting the μ C.

The SDI of the PCM1710 comprises data (MD), clock (MC), and latch (ML) lines. To drive this SDI, the serial port of the μ C operates in the default mode, Mode 0. Although this mode of operation is rare in many applications, it is convenient in this case because, apart from sending serial data via its RxD pin (P3.0), the serial clock is available on the TxD pin (P3.1). Thus, the RxD line directly serves as the MD signal, and the inverted TxD line serves as the MC signal. The program generates the third SDI line (ML). Sending 3 bytes of data to the DAC requires at least 36 µsec, assuming a 12-MHz clock from the DAC clock and omitting the time that the internal reset procedure of the μ C consumes. Thus, you can transmit 1 byte for one program execution, which occupies about 17 µsec. Assuming that 2 µsec is enough time for the μ C to properly reset, the entire program should easily fit into the allowable 21µsec frame. The low time of RST is approximately 19 µsec (Figure 1b).

This interface circuit relies on the fact that after you apply the RST signal to the μ C, some internal registers do not change their values, and others reset to 00H. Listing 1 is the corresponding assembler code. (You can download this listing from *EDN*'s

LISTING 1–PCM1710 DAC ASSEMBLER CODE ; ATTENUATION SET ON PORT P1.0 (MSB) - P1.6 (LSB) .EQU PCON, 087H .EQU FLAG.7, 07H .EOU FLAG.6, 06H .EQU FLAG.5, 05H .ORG 00H JBC FLAG.7.B 03 JBC FLAG.6, B_02 ;2 -> TOTAL MACHINE CYCLES: 4 B_01: MOV SBUF, RO ;2 SEND ATTENUATION BYTE MOV R0,#25H ;1 SAVE MODE 2 BYTE BEFORE RESET SETB FLAG.6 MOV A,#02H :1 SET UP FOR THE NEXT RESET ;1 NOP NOP NOP NOP NOP CLR P3.2 ;1 GENERATE ML SIGNAL ORL PCON, A ;1 GO TO POWER DOWN -> TOTAL MACHINE CYCLES: 12 B 02: MOV SBUF, R0 SEND BYTE MODE 2 MOV A, P1 ANL A, #080H ;1 READ MUTE SIGNAL FROM P1.7 ORL A.#060H ;1 ;2 CALCULATE ADDRESS OF MODE 1 BYTE ;1 SAVE MODE 1 BYTE BEFORE RESET MOVC A, @A+DPTR MOV RO,A SETB FLAG.7 MOV A,#02H ;1 SET UP FOR THE NEXT RESET ;1 CLP P3 2 -1 GENERATE MJ. SIGNAL ORL PCON, A ;1 GO TO POWER DOWN B 03: MOV SBUF, RO ;2 SEND BYTE MODE 1 :1 READ ATTENUATION FROM PORT P1.0 - P1.6 MOV A, Pl RL A ANL A,#0FEH MOV R0,A SETB FLAG.5 1 SAVE ATTENUATION VALUE BEFORE RESET 1 SET UP FOR THE NEXT RESET MOV A,#02H NOP - 1 CLR P3.2 ;1 GENERATE ML SIGNAL ORL PCON, A ;1 GO TO POWER DOWN ;MODE 1 BYTE FOR MUTE-OFF -> P1.7 = L ORG 060H .DB 001H ;MODE 1 BYTE FOR MUTE-OFF -> P1.7 = H .ORG 0E0H .DB 041H

web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2312.) After each RST pulse, the μ C sends 1 byte of code; the μ C sends the same byte every third RST pulse. The circuit uses register R_o to temporarily save the value of the next word to send because the μ C reset does not affect this register. The circuit also uses one bit-addressable memory location, designated FLAG (20H), to switch between bytes to send. Port P1 supplies the program with the attenuation value on pins P1.0 to P1.6 (from MSB to LSB) and supplies the MUTE signal on pin P1.7. The circuit stores the proper value of the Mode 1 control word in the program-memory area of the μ C at locations 60H (MUTE deasserted) and E0H (MUTE asserted). (DI #2312)

To Vote For This Design, Circle No. 427

Calibrated trim tool tweaks multiturn pots

Sanjay Chendvankar, Tata Institute, Mumbai, India

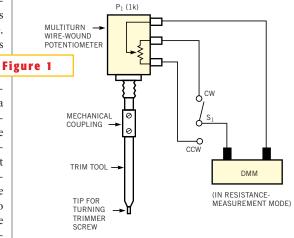
ANY ANALOG CIRCUITS contain multiturn trimming potentiometers whose settings you may need to change during maintenance or calibration. Also, some instruments have panelmounted potentiometers that may need periodic adjustments. After disturbing a setting by more than one or two turns, it becomes difficult or impossible to restore the original setting. The usual method is to measure the resistance between the wiper and one of the ends of the potentiometer before disturbing the setting and then to readjust to the same setting if and when necessary. However, this method is incon-



venient and sometimes impossible, such as when the trimmer is mounted on a panel, for example. The simple tool in **Figure 1** comes in handy in such situations.

You construct the tool by mechanically coupling the trimming tool's shaft to the shaft of a high-quality, multiturn, wirewound potentiometer (P_1). The wiper and one of the end terminals of this potentiometer connect to a DMM operating in resistancemeasurement mode. The toggle switch, S_1 , selects one of the two available end terminals. Before disturbing the setting of a multiturn potentiometer in a circuit, you rotate the trim tool to the endpoint of P_1 's rotation span in

the opposite direction to that in which you intend to adjust the trimming potentiometer. Set the selector switch such that the DMM reads zero (or near-zero) resistance. Then, you rotate the trim tool by



This "tool with a memory" allows you to accurately restore the original setting of a multiturn potentiometer.

firmly holding P_1 with one hand and turn the trimming potentiometer to the desired setting. The corresponding P_1 resistance value on the DMM, along with S_1 's position, tells you whether the tool rotates clockwise or counterclockwise. You record these data for future reference.

If you wish to restore the potentiometer's original position, you adjust P, to the recorded value with the same position of S₁ by turning the trim tool in the opposite direction until the DMM reads zero resistance. This position is the original setting of the potentiometer. The resistance value of P, is not critical. However, it's better to select low values to obtain higher resolution on the DMM. Also, a single range of the DMM should cover the value. This prototype uses 1 k Ω . You can improve the tool by replacing P₁ with a miniature bidirectional optical shaft en-

coder and connecting its output to an up/down counter. (DI #2308)

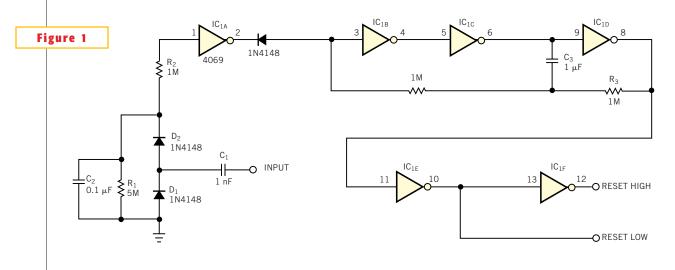
To Vote For This Design, Circle No. 428

Off-the-shelf watchdog serves in a pinch

Giovanni Romeo, Istituto Nazionale di Geofisica, Roma, Italy

HE PERFORMANCE OF THE WATCHDOG CIRCUIT in **Figure 1** may not match that of a dedicated watchdog circuit, but this circuit is helpful when the only watchdog in the lab doesn't meet your design's temperature requirement and when you are in a hurry to finish a prototype.

The circuit operates on a simple principle. When digital activity occurs on the in-



A charge pump comprising D_{1} , D_{2} , C_{1} , and C_{2} inhibits a three-gate oscillator when input activity exists. After 40 msec without input activity, the oscillator starts running and produces a reset signal.

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put, a charge pump comprising C_1 , D_1 , D_2 , and C_2 keeps C_2 charged. R_1 is the discharge resistor for C_2 . IC_{1A} detects the charge level through R_2 . A charged condition inhibits the three-gate oscillator comprising IC_{1B} , IC_{1C} , and IC_{1D} , and the active-high resethigh output stays low.

When the voltage at the input of IC_{1A} drops below the CMOS threshold, the oscillator starts working and produces a

square wave. The high time of the resethigh output resets the μ P under control, which must start the activity (and activate the watchdog input) before the end of the low time. R₃ and C₃ essentially control the high and low times, which have almost the same value.

Although this design monitors an RS-232C line, you can use the circuit to monitor a digital level. When monitoring an RS- 232C line with the values in **Figure 1**, the watchdog starts resetting 40 msec after detecting no activity and requires less than 20 msec to inhibit the oscillator after input activity resumes. (DI #2311)

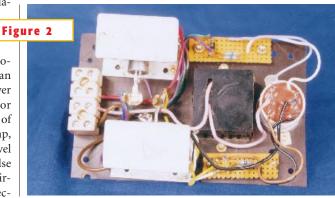
To Vote For This Design, Circle No. 429

Novel circuit controls ac power

Narendra Paranjape, Tata Chemicals Ltd, Mithapur, India

The SIMPLE AND INEXPENSIVE powercontrol circuit in **Figure 1** uses a readily available fan regulator with built-in phase control. Such fan regula-

tors are limited to approximately 100W. The circuit in **Figure 1** adds two SCRs and a few components to turn the humble fan regulator into a mighty power controller. The fan regulator operates with a nominal load of 10 to 25W through a lamp, which also gives a power-level indication. The 1:1:1 pulse transformer completes the circuit. The transformer's secondary windings fire the back-to-back SCRs, which then control a load of 1000 to 3000W. You can house the circuit in any in-

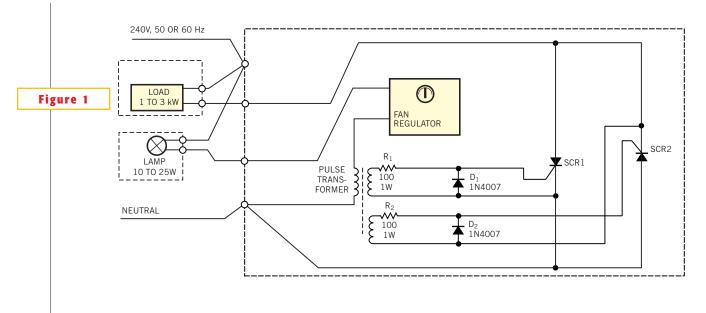


sulated box. You should mount the SCRs on heat sinks. R_1 , D_1 and R_2 , D_2 limit the gate current and prevent the application of

reverse voltage between gate and cathode. **Figure 2** shows construction details of the prototype. (DI #2310)

To Vote For This Design, Circle No. 430

An easy-to-build power controller works with an inexpensive fan regulator to control 1000 to 3000W.



A couple of thyristors, a pulse transformer, and two diodes transform a humble 100W fan regulator into a high-power ac controller.

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design**ideas**

Two AA cells power step-down regulator

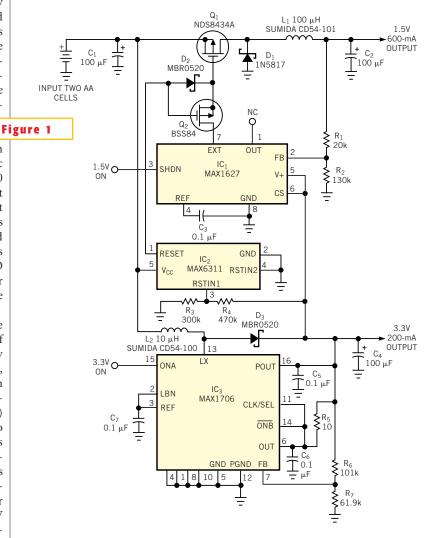
Len Sherman, Maxim Integrated Products, Sunnyvale, CA

D C/DC CONVERSION IS particularly challenging when both the input and output voltages are low. Step-up ICs that operate with inputs lower than 1V are available, but step-down ICs that accept input voltages near 2V are not. Thus, providing efficient power for the low-voltage CPU in a handheld product can be a prob-

lem if the power source is a two-cell AA battery. The battery's output can drop to 1.8V as the battery discharges. In **Figure 1**, the upper switch-mode dc/dc converter (IC_1) generates more than 600 mA at 1.5V, from a two-AA-cell input that varies from 3.4 to 1.8V. The 3.3V rail that powers this step-down controller comes from a high-current, synchronous-rectified boost controller (IC_3), which also provides power for external logic and the CPU's I/O blocks. IC_1 receives 3.3V bias, but power for the 1.5V output comes directly from the battery.

 Q_2, D_2 , and a SOT-23 reset IC (IC₂) force the switching power MOSFET (Q₁) off when the 3.3V rail is too low to properly operate IC₁. Without those components, the conditions at power-up (during which battery voltage is present but 3.3V are momentarily absent, pulling Q₁'s gate low) may cause the 1.5V output to overshoot to the battery voltage. The 1.5V output's buck-conversion efficiency (approximately 85%) is reasonably good for the circuit's extra-small components: a three-pin SOT-23 power MOSFET and 5-mm-diameter surface-mount inductors. For the 3.3V output, IC,'s on-chip synchronous rectification yields a boost efficiency higher than 90%. (DI #2302)

To Vote For This Design, Circle No. 431



Powered by the 3.3V boost controller IC_3 , this step-down controller (IC_1) generates 1.5V from inputs as low as 1.8V.

Temperature controller keeps IR detector at 8°K

Jerry Penegor, Space Sciences Laboratory, University of California—Berkeley

S ENSITIVE INFRARED array detectors must operate at a low temperature to avoid thermally generated dark current throughout the photoconductive elements. This requirement is

particularly true for SiAs array detectors, which need cooling to near liquid-helium temperatures. Furthermore, the sensitivity of these detectors can be temperature-dependent. The optimal operating temperature for a long-wavelength IR camera is about 8°K. This temperature must remain constant despite changes in the radiation level falling on the array, in the liquid helium level as it boils away, and



in the orientation of the Dewar flask.

To measure and control these low temperatures, the circuit in **Figure 1** uses a four-wire silicon diode. One pair of #38 AWG wire forward-biases the diode with a fixed 10 μ A of drive current. The second pair of wires provides for Kelvin-connection measurement of the forward-voltage drop, V_P, which is a very nonlinear function of temperature. Around 8°K, the V_P is 1.5V and changes about -35 mV/°K. To accurately measure the array temperature requires mounting the diode as close as possible to the SiAs array in its ceramic chip carrier.

The back of this carrier is spring-loaded against an oxygen-free, high-conductivity copper plug onto which a 500 Ω wirewound resistor attaches. A heavy copper braid also connects the plug to the liquidhelium reservoir. Good thermal contact between the power resistor and the chip carrier ensures that a simple circuit can control the temperature. The simple proportional-integral servo circuit in **Figure** 1 can control array temperature to $\pm 5 \text{ m}^\circ\text{K}$ over an 8 to 12°K range. Slewing the array to a new setpoint temperature takes approximately 30 sec.

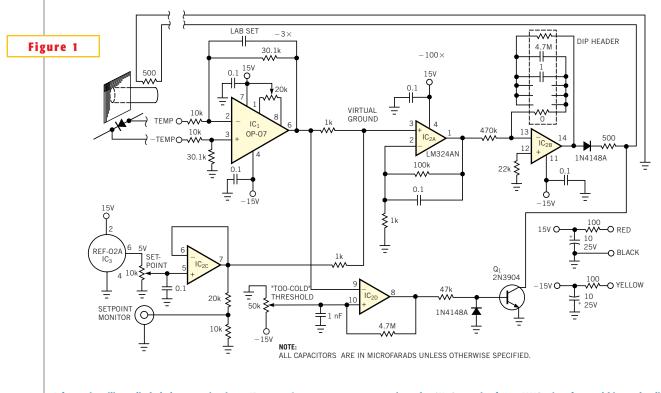
Special low-thermal-conductivity steel coax cable goes through hermetic connectors in the vacuum Dewar flask wall. This cable makes all electrical connections to the cooled camera. The schematic shows no low-leakage unity-gain buffers that isolate the voltages at the sensor diode's anode and cathode (+ and -T) from all the meters and circuitry that operate at room temperature.

Op amp IC₁ is a differential receiver for the + and -T voltages and has a gain of -3. Because -3 times the coldest expected V_F is about -4.8V, a stable 5V reference, IC₃, supplies the voltage at the potentiometer for the temperature setpoint over the necessary range. The setpoint-monitor output has an attenuation of 3, so you can see the setpoint voltage directly on any meter.

When the sensor and setpoint voltages are in balance, the noninverting input to IC_{2A} is 0V. IC_{2A} amplifies any imbalance. IC_{2B} sets the frequency response of the servo with a zero at a corresponding time constant of 10 sec. That is, IC_{2B} 's gain term of 10 is constant for any ac disturbances but is high for dc error. Mounting the resistors and capacitors that set the servo time constant on a seven-position header allows you to easily add component values when the controller is mounted on the Dewar flask. The output diode ensures that positiveonly current goes to the power resistor on the heat sink; power off is 0V, and no negative currents can flow. (Negative current does not cool the power resistor.) The optional 500 Ω series resistor in series with the output diode provides additional current limiting for IC₂₈.

One condition to guard against is a broken or disconnected sense diode that sends the temperature controller into full-power application. IC_{2D} senses temperatures that are too cold—excessive negative voltage from IC—to be valid. The 50-k Ω potentiometer sets the "too-cold" threshold at approximately –5V. If the circuit detects a too-cold condition, IC_{2D} turns on Q_1 , which shorts the output and sinks the output current within Q_1 . (DI #2296)

> To Vote For This Design, Circle No. 432



A four-wire silicon diode helps to maintain an IR camera's temperature at approximately 8°K. One pair of #38 AWG wires forward-biases the diode with a fixed 10 mA of drive current. A second pair of wires provides for a Kelvin-connection measurement of the diode's forward voltage drop, which is a nonlinear function of temperature.

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design**ideas**

Flyback circuit provides isolated power conversion

Philip Cooke, Unitrode Corp, Merrimack, NH

COMMON REQUIREMENT in telecommunications systems is to convert an unregulated 48V line to an isolated, accurate dc supply voltage. The circuit in Figure 1 provides a 5V, 15W output. The circuit uses a UCC3809 primary-side controller, which can also control other single-ended converters. The topology uses peak-current-mode control with a fixedfrequency oscillator. The design is cost-efficient, because it assumes that compensation of the voltage loop occurs on the secondary side, where you would place the error amplifier and reference anyway. By eliminating a primary-side amplifier, you reduce system cost and complexity.

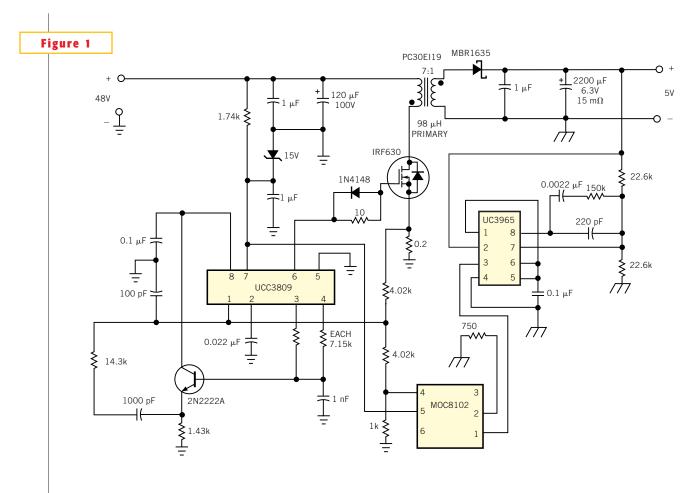
The feedback signal from the secondary comes from the UC3965 precision refer-

ence. In addition to a low-offset error amplifier, this IC also contains an optocoupler driver for simplicity in designing isolated converters. An undervoltage-lockout circuit provides a controlled start-up transient. The design in Figure 1 uses discontinuous-conduction mode (in which the flyback transformer undergoes complete demagnetization in every cycle), with maximum duty cycle set to 50%. Continuous-mode flyback circuits (in which the flyback transformer operates in continuous inductor-current mode) have a righthalf-plane zero that limits the control bandwidth, as opposed to discontinuousmode flybacks that do not restrict bandwidth.

Both ICs operate in either mode; the

choice of mode depends on the powersupply requirements. You can easily buffer the primary-side oscillator with an emitter follower to provide slope compensation for designs requiring duty cycles beyond 50%. Note, however, that you have the option of programming a duty-cycle clamp to 50% or less, which can save cost by eliminating several slope-compensation components. The maximum-dutycycle clamp in the UCC3809 is completely programmable by selecting the two resistors connected to pins 3 and 4. (DI #2288)

> To Vote For This Design, Circle No. 433



A discontinuous-mode flyback regulator provides an isolated, regulated supply, and saves cost by cutting compensation components.

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Edited by Bill Travis and Anne Watson Swager

RISC μ P implements fast FIR filter

Sorin Zarnescu, NEC Electronics, Santa Clara, CA

HEN IT COMES TO implementing a fast FIR filter, current RISC μPs can compete with DSP μPs. The FIR algorithm continuously implements the following equation:

N=n-1

Out=Sum[in(t[-]n)coeff(n)] N=0,

where N is the number of taps, or the number of multiply-accumulate (MAC) instructions of the filter.

Using a delay line to implement this equation is common and involves the ability to manage a circular buffer. Specialized DSP μ Ps have can manage this task in hardware, and general-purpose μ Ps have to implement the buffer management in software. As you might expect, the software implementation is significantly slower than the hardware one. However, modern RISC μ Ps operating at high speeds and with features lacking in

previous generations of generalpurpose μ Ps can compete in price and performance at executing these types of algorithms.

For example, consider the following algorithm, which you can implement using the V832 RISC processor (NEC Electronics, www.el.nec.com), which runs at 144 MHz. This µP features large internal

RISC µP imple	ements fast FIR filter
1 5	hm transforms filter 120
Door/window : tampering	sensor resists 120
Use a trick to c	count scope events
,	inary-arithmetic 124
Light powers is	solation amplifier128
2011 0000100000	back circuit boosts

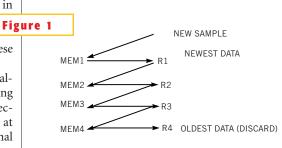
LISTING 1-RISC-µP FAST-FIR ROUTINE

Ideas

.data .align 4 .global M1,M2,M3,M4,New

.set	0x00; coef 1	
.set	0x10; coef 2	
.set	0x20; coef 3	
.set	0x30; coef 4	
.hword	0x0010	; first sample
.hword	0x0020	; second sample
.hword	0x0030	; third sample
.hword	0x0040	; fourth sample
.hword	0x0050	;new sample - written by the interrupt routine
	.set .set .hword .hword .hword .hword	.set 0x10; coef 2 .set 0x20; coef 3 .set 0x30; coef 4 .hword 0x0010 .hword 0x0020 .hword 0x0030 .hword 0x0040

ld.h	M1[r0],r1; load first sample into register 1
ld.h	M2,[r0]r2; load second sample into register 2
muli	c1,r1,r1 ;(coef 1 x sample 1) → accumulator
st.h	r1,M1[r0]; store first sample into the second memory location
ld.h	M3[r0],r3; load third sample into register 3
maci	c2,r2,r1 ; (coef 2 x sample 2) + accumulator → accumulator
st.h	r2,M3[r0]; store second sample into third memory location
ld.h	M4[r0],r4 ; load 1st sample
maci	c3,r3,r1 ; (coef 3 x sample 3) + accumulator → accumulator
st.h	r3,M4[r0]; store third sample into last memory location
maci	c4,r4,r1; (coef 4 x sample 4) + accumulator -> accumulator



The trick to the RISC- μ P FIR algorithm is to store the data back into a memory location that's shifted by one position.

memories, the ability to execute instructions from internal memory in one clock cycle, and the ability to execute one MAC instruction in one clock cycle. The algorithm is not new, but it takes advantage of these features.

The algorithm runs linearly with no loops and implements the circular buffer with the addition of load/store instructions. Because the V832 is a RISC processor, arithmetic operations can take place only between registers. When a new sample is available, data loads from memory into the registers; the algorithm operates on the data and then stores it back in memory. The trick is to store the data back into the memory but shifted by one position. For the simple case of a four-tap filter, the algorithm looks like **Figure 1**.

For each tap, the processor needs to execute only ld.h (load the sample into the register), maci (multiply-accumulate immediate, in which the immediate value is the coefficient), and st.h (store the register back into the memory according to **Figure 1**).

Listing I comprises sample code for a four-tap FIR filter. (You can download this listing from *EDN*'s web site, www.ednmag.com. At the registereduser area, go into the Software Center to download the file from DI-SIG, #2313.) The instruction arrangement minimizes the dependencies inherent in a pipeline-based µP. The next time the program

executes, all of the samples are in the right position, assuming that the ADC interrupt routine writes the new sample into M1 before calling the filter routine. Regardless of the number of taps, the program takes three clock cycles per tap, which in the case of the V832 translates into 21 nsec/tap and occupies 3N memory locations. (DI #2313).

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Simple algorithm transforms filter coefficients

Frank Vitaljic, Bellingham, WA

T O SYNTHESIZE INFINITE-impulse-response (IIR)-filter functions, expressed as H(z), you commonly use analog prototype-filter functions, expressed as H(s), using the bilinear-z transform. This operation entails some algebraic complexity in calculating the filter coefficients. The simple algorithm shown here transforms the prototype-filter coefficients (W_0 , W_1 , W_2) to the IIR digital-filter coefficients (U_0 , U_1 , U_2). These coefficients transform from the s (analog) domain to the z (digital) domain as:

$$W_0 + W_1 s + W_2 s^2 \rightarrow U_0 + U_1 z^{-1} + U_2 z^{-2}$$

The filter conventions are:

$$H(s) = \frac{A_0 + A_1 s + A_2 s^2}{B_0 + B_1 s + B_2 s^2}, \text{ and}$$
$$H(z) = \frac{C_0 + C_1 z^{-1} + C_2 z^{-2}}{D_0 + D_1 z^{-1} + D_2 z^{-2}},$$

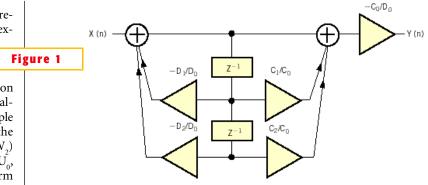
where the numerator and denominator polynomials undergo independent transformation. The matrix equations are

$$[U_0U_1U_2]^{T} = M[W_0W_1W_2]^{T}$$
, and

$$[W_0 W_1 W_2]^{T} = M^{-T} [U_0 U_1 U_2]^{T},$$

where

$$\mathbf{M} = \begin{bmatrix} 1/4 & 1/2 & 1\\ 1/2 & 0 & -2\\ 1/4 & -1/2 & 1 \end{bmatrix} \quad \mathbf{M}^{-1} = \begin{bmatrix} 1 & 1 & 1\\ 1 & 0 & -1\\ 1/4 & -1/4 & 1/4 \end{bmatrix},$$



You combine biquad sections in cascade to form high-order IIR digital filters.

and, for first-order filters,

 $M = \begin{bmatrix} \frac{1}{2} & 1\\ \frac{1}{2} & -1 \end{bmatrix} \qquad M^{-1} = \begin{bmatrix} 1 & 1\\ \frac{1}{2} & -\frac{1}{2} \end{bmatrix}.$

These equations assume that the prototype filter is normalized with respect to the sampling frequency, f_s . For example, design a second-order Butterworth unity-gain, lowpass IIR filter with cutoff frequency, f_{C} =100 Hz, and sampling rate, f_s =1000 Hz. First, you use C_w to frequency-scale the Butterworth prototype (in normalized form, C_w =1). The expression for C_w is

$$C_{\rm W} = 2\tan\left(\pi \frac{f_{\rm C}}{f_{\rm S}}\right)\pi \frac{f_{\rm C}}{f_{\rm S}} =$$

$$2\tan(0.1\pi) = 0.649839$$
rad/sec.

The prototype filter is thus

$$H(s) = \frac{0.4223}{0.4223 + 0.919s + s^2}$$

Now, calculate the IIR coefficients using the transform in **equations 1** and **2**:

$\begin{bmatrix} C_0 \\ C_1 \\ C_2 \end{bmatrix} =$	0.25	0.5	1	0.4223]	0.1056	
C ₁ =	0.5	0	-2	0	=	0.2112	;
C_2	0.25	-0.5	1	0		0.1056	
$\begin{bmatrix} D_0 \end{bmatrix}$	0.25	0.5	1	0.4223	ſ	1.5651]
D ₁ =	0.5	0	-2	0.9190	=	-1.7889	ŀ
$\begin{bmatrix} D_0 \\ D_1 \\ D_2 \end{bmatrix} =$	0.25	-0.5	1	1.0000		0.6461	

Figure 1 gives the filter's flow diagram. (DI #2287).

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Door/window sensor resists tampering

(1)

(2)

Paul Nocella, Q Research, Brookline, NH

THE SIMPLE, INEXPENSIVE circuit in **Figure 1** detects a failure (or deliberate tampering) on lines connected to normally closed switch sensors. For example, common door interlocks and door/window sensors consist of normal-

ly open or normally closed magnetic reed switches. Depending on the monitoring configuration, an open or short on a line may go undetected, thus preventing alarm activation. Embedding a resistor in a normally closed sensor and using bipolar dc power supplies produces the balanced configuration in **Figure 1**. A short or open on a line (or sensor activation) produces a net positive or negative voltage at the input of the Q_1 - Q_2 pair.

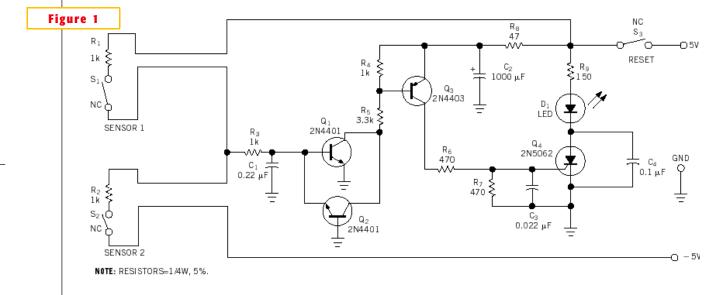
A positive-voltage imbalance turns Q₁

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on; a negative-voltage imbalance turns Q_2 on. The back-to-back clamping action of the base-emitter junctions of Q_1 and Q_2 protects the transistors from excessive reverse VBE voltages. The clamping prevents intrinsic base-emitter zener breakdown. R_3 limits the input current to Q_1 and Q_2 in the event of a line short. The collectors of Q_1 and Q_2 form a wired-OR configuration that turns Q_3 on by pulling its base toward ground. Q_3 provides gate current to trigger the alarm, SCR Q_4 , which can handle several hundred milliamperes. Q_4 can drive a variety of alarm indicators, including LEDs, piezoelectric buzzers, or relays that control high-power alarms.

It's easy to add monitoring locations, simply by adding sensors in pairs and replicating the Q_1 - Q_2 circuit configuration, including the wired-OR connection to R_5 . With power-supply voltages of ±5V, worst-case resistor tolerances of ±5% and a 2.5% supply imbalance do not cause Q_1 or Q_2 to turn on. The ±5V supplies should rise approximately simultaneously; otherwise, a net voltage imbalance would appear at the input of Q_1 and Q_2 , resulting in alarm activation. Momentarily opening S_3 resets Q_4 by interrupting its anode current. C_2 provides a small time delay to allow the voltage at the input of Q_1 and Q_2 to stabilize before enabling Q_3 . C_1 , C_3 , and C_4 prevent stray ac pickup or transients from triggering Q_4 . (DI #2286).

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Normally closed sensor pairs form the detectors in a tamper-resistant and foolproof window/door security system.

Use a trick to count scope events

Allen Montijo, Hewlett-Packard, Colorado Springs, CO

O NE ADVANTAGE DIGITAL storage oscilloscopes (DSOs) have over analog scopes is trace persistence. You can easily see infrequent waveform features using a scope in infinite-persistence mode. However, the frequency of these features relative to that of a "normal" signal can sometimes be less than obvious. You may wonder, does that glitch appear 10% or only 1% of the time? And how often does that short clock cycle occur? When you take trace noise into account, even a color-graded display does not directly or accurately give the information. A histogram is the

most accurate way to give the information, but it requires time and expertise. The following hint provides a quick way to determine, using a DSO, how often each of two waveforms occurs.

First, use a standard nonaveraging mode to find the voltages of the two states at a fixed point in time $(V_1 \text{ and } V_2)$. Now, turn averaging on using a large number of averages. After the trace settles, measure the average level (V_A) . The percentage of time the signal at V_2 is:

$$\frac{\frac{V_{A} - V_{1}}{V_{2} - V_{1}} \times 100\%}{15}.$$

The accuracy of your answer depends on the accuracy of your V_1 , V_2 , and V_A measurements. To increase the accuracy of V_A , simply increase the number of averages on the scope. If you can use your DSO's advanced triggering capabilities to trigger on only one waveform, then you can use the DSO's averaging mode to make more accurate measurements of V_1 , V_2 , or both. (DI #2298).

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A primer on binary-arithmetic rounding

Tom Balph, Motorola SPS, Tempe, AZ

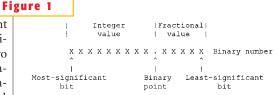
A S DIGITAL COMMUNICATIONS and data compression/decompression proliferate, signal-processing functions grow in importance. Whether you're dealing with hard-wired logic or programmable engines, an understanding of binary-arithmetic rounding is important in getting correct and consistent results. Before we discuss rounding, consider a binary number (**Figure 1**).

At first glance, rounding seems a simple matter. However, several variations on rounding exist. Depending on the application, you may use one of the following techniques:

- Truncation (round to minus infinity)—This form of rounding ignores any information in the fractional value to the right of the binary point. You discard these bits, leaving the integer value to the left of the binary point unaffected. Truncation is also called round to minus infinity because it has the effect of rounding to the more negative number. Truncation is in wide use because it is simple to implement: Just ignore the unused bits.
- Round to plus infinity—This variation is essentially the inverse of truncation. If the fractional value to the right of the binary point is not exactly zero, then you round up (make more positive) the integer value. The implementation is more complex than truncation, because you must test all the fractional bits for the existence of a one and then increment the integer value if you find a one.
- Round to zero—Round to zero applies to 2's complement numbers. (For the case of positive numbers only, round to zero reduces to truncation.) For negative numbers, this rounding technique depends on the fractional value—the existence of any nonzero LSBs causes a round up to a less negative number. The positive-number case is simply truncation. The implementation must consider both the fractional-number value and the sign bit.

You increment the integer value only when the sign bit equals one (negative number) and the fractional value is not zero.

- Up-magnitude (round to infinity)-Up-magnitude is the inverse of round to zero and applies to 2's complement numbers. If the number is positive, round up for any fractional number not equal to zero. If the number is negative, round down (truncate) for any fractional number not equal to zero. This algorithm is perhaps most useful for maintaining the largest possible magnitude for digital-to-analog conversion. The technique finds use in recent standards, such as ISO/IEC 11172-3 MPEG audio. Implementation again considers the sign and fractional values: Increment the integer only when the sign bit equals zero (positive number) and the fractional value is not zero.
- Simple round (2's complement round)—Simple round applies to both magnitude-only and 2's-complement numbers. You round up the integer value for all fractional values greater than or equal to half the fullscale value of the fractional number. Half the full-scale value is a one and all zeros at the right of the binary point. For fractional values lower than half full-scale, the integer number remains unchanged (truncation). Implementation is relatively simple in that you can add a one to



A binary number can consist of any number of bits with the binary point at any bit position. All bits to the left of the binary point are the integer, or most-significant, bits of the number. All bits to the right of the point are the fractional, or least-significant, bits of the number. For 2's complement numbers, the most-significant bit has a negative binary weight and is the sign bit. If no sign bit exists, the number is magnitude only and unsigned.

the number at the bit position directly to the right of the binary point. This action increments the integer for any fractional value equal to or greater than half the fractional full-scale value.

Convergent round—Convergent round is similar to simple round. The difference has to do with the half-full-scale value of the fractional number. A fractional number greater than half full-scale always causes rounding up of the integer number, a fractional number less than half full-scale causes the integer to remain unchanged, and a fractional number equal to half fullscale causes the integer to round up to the nearest even value. Convergent round is most useful for iterative processes in which cumulative addition causes errors to occur more readily. Implementation requires testing the fractional value, as well as the LSB of the integer number. The integer number increments if the fractional value is greater than half full-scale or if the fractional value equals half full-scale and the integer LSB is one (producing an odd number).

Listing 1 illustrates the rounding methods using Verilog HDL. A 12-bit number, "x," with the binary point located to the left of Bit 3 serves as the input (yielding an 8-bit integer and a 4bit fraction). Each of the rounded results are 8-bit integer numbers. Part A

> of Listing 1 is the module listing, which defines and exercises the rounding outputs and displays the results. Part B gives the displayed simulation results, which you can use to observe the rounding differences. Be aware that, although this HDL routine is fully synthesizable, the resulting logic may not deliver the best performance or be the minimum configuration. You can download Listing 1 from EDN's Web site, www.ednmag.com. At the registered-user area, go into the Software Center to down-

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load the file from DI-SIG, #2285.

When you implement rounding, performance can suffer if an additional add occurs, because of the rounding algorithm. At times, however, the logic producing the original number can hide the additional add. As an example, if you use simple round (2's complement round) with a multiplier to round the results, a constant one can appear in the partial-product array (at the proper location), and summing the one along with all the partial products produces no loss in performance. Here, the increment of the integer product is buried in the multiplier-adder array. (DI #2285).

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LISTING 1–ROUNDING EXAMPLES USING VERILOG HDL

A) Module listing	x = 12'h008; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
# File : round.v	converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
module test;	x = 12'h018; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
reg [11:0] x;	converg = %h°,
# Simple truncation	x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
wire [7:0] trunc = x[11:4];	x = 12'h808; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
// Round-to-plus-infinity // Increment the integer when the fraction is not equal to zero.	converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
wire [7:0] plus_inf = (x[3:0] == 4'h0)? x[11:4] : x[11:4] + 8'h01;	x = 12'h818; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
# Round-to-zero $#$ lncrement the integer when a negative number and the fraction is not equal to zero.	converg = %h*, x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
wire [7:0] zero = (x[11] & (x[3:0] != 4'h0))? x[11:4] + 8'h01 : x[11:4];	x = 12'h019; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
# Up-magnitude round $#$ Increment the integer when a positive number and the fraction is not equal to zero.	converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
wire [7:0] up_mag = (~x[11] & (x[3:0] != 4'h0))? x[11:4] + 8'h01 : x[11:4];	x = 12'h819; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
// 2's Complement round // Add fractional number 4'h8 to original number before using integer	converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
wire [11:0] temp = x[11:0] + 12'h008; wire [7:0] twos_comp = temp[11:4];	x = 12'h028; #10; 5display!"x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h converg = %h",
// Convergent round // Increment the integer when; a) fraction is greater than 4°h8,	x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
// or b) fraction = 4'h8 & integer is odd (lsb = 1). reg [7:0] converg:	x = 12h828; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h converg = %h",
	x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
always @(x)	x = 12'h029:
if (x[3:0] > 4'h8) converg = x[11:4] + 8'h01;	#10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h
else if ((x[3:0] == 4'h8) & (x[4])) converg = x[11:4] + 8'h01; else converg = x[11:4];	converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
// display input and outputs	x = 12'h829;
initial	#10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h converg = %h",
begin	x,trunc,plus_inf,zero,up_mag,twos_comp,converg);
x = 12'h000; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h	\$finish; endmodule // test module
converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);	
x = 12'h001; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h convera = %h".	B) Simulation results:
converg = ~n"; x,trunc,plus_inf,zero,up_mag,twos_comp,converg);	Compiling source file "round.v"
x = 12'h800; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h	Highest level modules: test
converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);	x = 000 trunc = 00 plus_inf = 00 zero = 00 up_mag = 00 twos_comp = 00 converg = 00 x = 001 trunc = 00 plus_inf = 01 zero = 00 up_mag = 01 twos_comp = 00 converg = 00
x = 12'h801;	x = 800 trunc = 80 plus_inf = 80 zero = 80 up_mag = 80 twos_comp = 80 converg = 80 x = 801 trunc = 80 plus_inf = 81 zero = 81 up_mag = 80 twos_comp = 80 converg = 80
#10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h converg = %h",	x = 011 trunc = 01 plus_inf = 02 zero = 01 up_mag = 02 twos_comp = 01 converg = 01 x = 811 trunc = 81 plus_inf = 82 zero = 82 up_mag = 81 twos_comp = 81 converg = 81
x,trunc,plus_inf,zero,up_mag,twos_comp,converg); x = 12'h011;	x = 008 trunc = 00 plus_inf = 01 zero = 00 up_mag = 01 twos_comp = 01 converg = 00 x = 018 trunc = 01 plus_inf = 02 zero = 01 up_mag = 02 twos_comp = 02 converg = 02
#10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h	x = 808 trunc = 80 plus_inf = 81 zero = 81 up_mag = 80 twos_comp = 81 converg = 80 x = 818 trunc = 81 plus_inf = 82 zero = 82 up_mag = 81 twos_comp = 82 converg = 82
converg = %h", x,trunc,plus_inf,zero,up_mag,twos_comp,converg);	x = 019 trunc = 01 plus_inf = 02 zero = 01 up_mag = 02 twos_comp = 02 converg = 02 x = 819 trunc = 81 plus_inf = 82 zero = 82 up_mag = 81 twos_comp = 82 converg = 82
x = 12'h811; #10; \$display("x = %h trunc = %h plus_inf = %h zero = %h up_mag = %h twos_comp = %h	x = 028 trunc = 02 plus_inf = 03 zero = 02 up_mag = 03 twos_comp = 03 converg = 02 x = 828 trunc = 82 plus_inf = 83 zero = 83 up_mag = 82 twos_comp = 83 converg = 82
<pre>#ru; susplay(x = "on trunc = "on plus_int = "on zero = "on up_mag = "on twos_comp = "on converg = %h", </pre>	x = 029 trunc = 02 plus_inf = 03 zero = 02 up_mag = 03 twos_comp = 03 converg = 03 x = 829 trunc = 82 plus_inf = 83 zero = 83 up_mag = 82 twos_comp = 83 converg = 83
	L114 "round.v": \$finish at simulation time 160 161 simulation events



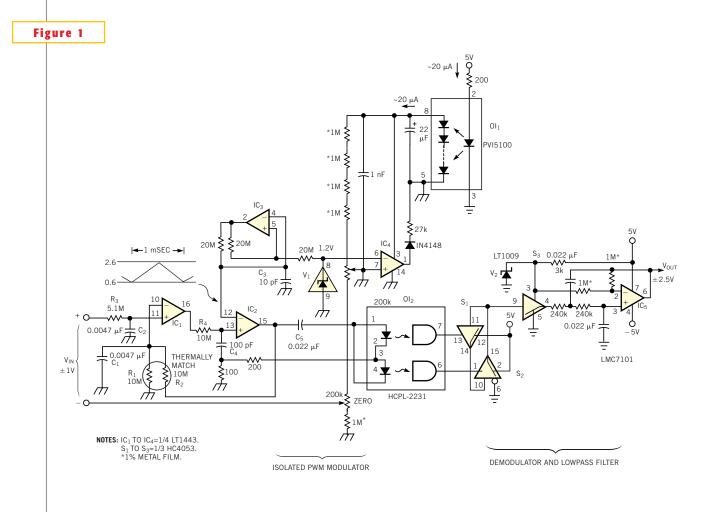
Light powers isolation amplifier

Stephen Woodward, University of North Carolina, Chapel Hill, NC

S ELF-POWERED isolation amplifiers, which need no external isolated power supply, provide versatile and convenient interfaces in many applications that require galvanic isolation of the signal source. Examples of such applications include circuits that serve in industrial or medical environments, in which isolation is necessary for noise reduction or safety. You can use a variety of isolated signal-coupling techniques for the signal paths of these amplifiers. Transformers, differential-capacitor, and optoisolator schemes are all popular choices. For the internal isolated power supply,

transformer coupling is virtually universal, despite the problems inherent in inductively coupled circuits. These problems include relatively high interwinding stray capacitance and a tendency to couple switching noise into the signal. In contrast, the self-powered amplifier in **Figure 1** is different in that it incorporates optoisolators to effect communication of both signal and power around the isolation barrier.

As in many isolation-amplifier designs, the signal processing in **Figure 1**'s circuit uses PWM. The isolated-modulator front-end circuitry derives from an earlier ADC design and works as follows. IC_1 compares the ±1V filtered input signal with the voltage on C_1 . The R_4C_4 time constant smoothes IC_1 's output, and IC_2 compares the output with IC_3 's approximately 1-kHz triangle waveform. R_1 , R_2 , and C_1 scale and average the resulting variable-duty-factor square wave and feed the signal back to IC_1 . This feedback loop continuously adjusts IC_2 's duty factor to maintain equal voltages on C_1 and C_2 . In doing so, the feedback forces IC_2 's output square wave to track the unique $T_+/(T_++T_-)$ duty factor that maintains balance at IC_1 's inputs.



A virtual perpetual-motion machine (when there's light), this self-powered amplifier provides complete galvanic isolation for both power and signal.

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 C_5 differentiates the IC₂ square wave to provide bipolar drive pulses to the antiparallel LEDs in the high-speed, lowcurrent optoisolator OI₂. In turn, OI₂ produces ground-referred pulses. The rather unusual RS flip-flop formed by cross-connected switches S₁ and S₂ converts these pulses back to a logic-level square wave having the same duty factor as IC₂'s output. Demodulation and filtering of the square wave to accurately reproduce the original analog signal occurs through the action of the single-pole, double-throw switch, S₃, which chops the 2.500V V, reference voltage according to the $T_{+}/(T_{+}+T_{-})$ square-wave duty factor. The lowpass, gain-of-two filter, $IC_{5^{2}}$ then extracts the dc component of S_{3} 's 0 to 2.5V waveform and scales and offsets it to produce a low-ripple, $\pm 2.5V$ signal, according to the formula

 $V_{\rm O} = 2.5 \times T_+ \; / (T_+ + T_-) = 2.5 \times V_{\rm IN} \, . \label{eq:VO}$

Power for the isolated-modulator side of the amplifier comes from OI_1 , an International Rectifier (El Segundo, CA) PVI5100 photovoltaic opto IC. Marketed as an isolated MOSFET-gate driver, the PVI5100 can source approximately 20 μ A of current at 4V (80 μ W), just enough to keep the anorexic LT1443 alive and functional. IC₄ shunt-regulates OI₁'s output to provide a stable 4V ratioed against the MAX924's 1.2V \pm 1% internal reference. Overall frequency response is dc to 10 kHz; input impedance is approximately 1 T Ω with less than 1-pA bias. The circuit can thus provide good overall accuracy with high-impedance input sources. You can trim gain and offset errors to zero; the excellent drift specs of the LT1443 maintain the trim over temperature. (DI #2304).

> To Vote For This Design, Circle No. 390

Low-cost feedback circuit boosts efficiency

John Guy, Maxim Integrated Products, Sunnyvale, CA

T O IMPLEMENT A STEP-UP converter with a current output, designers often simply connect the load in place of the top resistor in a resistive-divider feedback network. The bottom resistor then serves as a current-sense resistor. Though simple, this approach is ineffi-

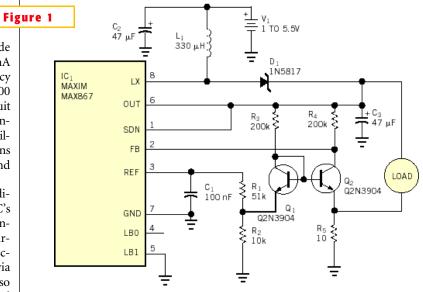
cient. Low efficiency results from the relatively high sense voltages—usually, 1.25V but as high as 2.5V for some ICs. A switch-mode dc/dc converter configured as a 20-mA current source minimizes the efficiency loss by lowering the sense voltage to 200 mV (**Figure 1**). Advantages of this circuit include the factor-of-six gain in efficiency; minimal board area; and readily available, low-cost components. Applications include battery charging, LED drive, and general-purpose current sources.

Resistors R_1 and R_2 form a voltage divider that derives 200 mV from the IC's reference output. This sense voltage connects to one emitter of the current mirror comprising Q_1 and Q_2 . Both collectors connect to the output voltage via 200-k Ω resistors. The collector of Q_2 also connects to the IC's feedback pin, and Q_2 's emitter connects to the low-side current-sense resistor, R_5 . The feedback network appears to the IC's control loop as

a common-base amplifier. Selecting a 2N3904 for Q_2 yields sufficient emitterto-collector gain for the purpose: approximately 80V/V. Moreover, the network's large bandwidth (characteristic of

common-base configurations) prevents instability in the IC's control loop. (DI #2307).

To Vote For This Design, Circle No. 391





Edited by Bill Travis and Anne Watson Swager

ADC circuit optimizes key encoding

Vitor Amorim, Siemens, and J Simões, University of Coimbra, Coimbra, Portugal

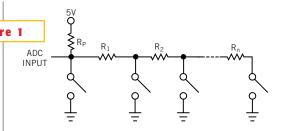
OU CAN IMPLEMENT a simple and

Figure 1 low-cost keyboard encoder by using a key-controlled resistive divider connected to an ADC (**Figure 1**). This type of circuit is especially suitable for embedded systems that use a μ C with an integrated ADC section. To obtain the best noise margin between keys, select resistors to yield an equal division of the voltage levels. To meet this criterion using the circuit in **Figure 1**, you must use a set of resistors

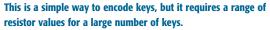
with all-different, specific values. For example, a 10-key **Figure 2** keyboard uses a 10-k Ω pullup resistor, R_p, and values of 1.1, 1.3, 1.8, 2.4, 3.3, 5.1, 8.2, 16, and 51 k Ω for R₁ through R₉. Using commonly available resistor values and tolerances and taking account of the key resistivity and ADC linearity errors, you're limited in the number of keys you can encode with a safe noise margin. Using an 8-bit ADC, the cited 10-key example is close to that limit.

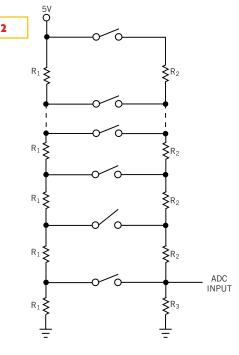
The circuit in **Figure 2**, despite its many resistors, overcomes the problem of the many restore values. The circuit is symmetric and uses the same two resis-

ADC circuit optimizes key encoding	101
RS-232C circuit has galvanic isolation	102
Digital pot adjusts LCD's contrast	104
Add speech encoding/decoding to your design	106
Cheap PWM IC makes synchronous gate driver	110
Circuit detects total on-time	112



deas





This key-encoding circuit simplifies resistor inventories, and provides a comfortable noise margin to boot.

tor values for all keys. It is also easy to expand the circuit for more keys. As in **Figure 1**'s circuit, if you simultaneously press more than one key, the circuit detects only the key whose connection is closest to the ADC. The chain of R₁ resistors de-

fines the voltage level associated with each key. Their nominal value is a trade-off between the power dissipation and the values of R_2 and R_3 , which depend on R_1 ; the total number of keys; and the desired noise margin. R_2 minimizes the voltage deviations at the nodes of the R_1 chain whenever you simultane-

ously press two or more keys. Therefore, you should calculate its value, much higher than that of R_1 , by taking into account R_1 and the desired width of the voltage window associated with each key. Similarly, R_3 's value should be much higher than that of R_2 to ensure that the voltage level associated with each key almost completely transfers to the ADC's input.

The circuit was tested by encoding 15 keys with one 8-bit analog input of the Microchip PIC16C71 μ C. The resistor values are 47 Ω , 3.9 k Ω , and 4.7 M Ω for R₁, R₂, and R₃, respectively. Only R₁ needs a tight tolerance; the others are less demanding. The window of key acceptance is set to a 7-LSB interval centered on the theoretical key level. This interval is large enough to accommodate the worst case (simultaneously pressing the two

more-distant keys from the analog input) with a safety noise margin between valid keys of 10 LSBs. (DI #2319).

To Vote For This Design, Circle No. 332



RS-232C circuit has galvanic isolation

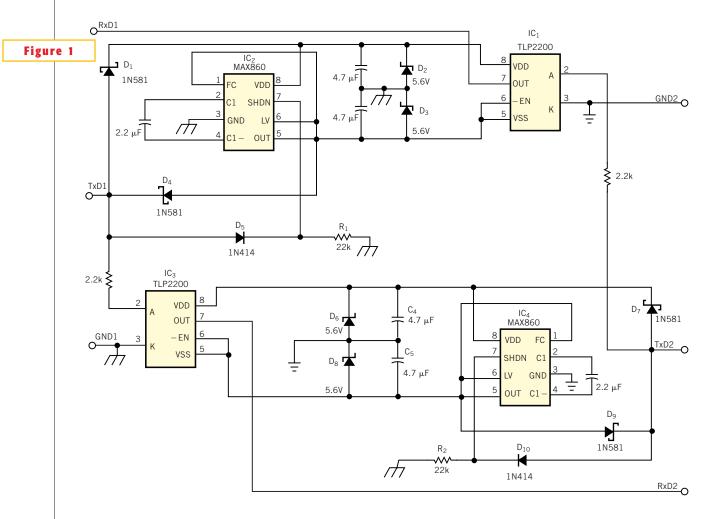
Ioan Ciascai, REI Data, Napoca, Romania

Y OU CAN OBTAIN LONGER TRANSMIS-SION distances with the RS-232C interface if you use galvanic isolation between the two linked terminals. Galvanic isolation also eliminates problems arising from disparate potentials between terminals. Using two MAX860/861 ICs and two TPL2200 optoisolators, you can obtain galvanic isolation for three-wire transmission without external supplies (**Figure 1**). The MAX860/861 circuits, which generate two voltages of different polarity, regardless of the polarity of TxD, which provides the supply voltage, are the basis of the design. For the positive TxD polarity, the MAX860/861 ICs function as voltage inverters, whereas for negative-polarity TxD, the ICs function as voltage doublers. Diodes D_1 and D_7 provide the positive supply voltages; D_4 and D_9 provide the negative supply voltages, depending on the polarity of TxD. The diode-resistor pairs D_5 , R_1 and D_{10} , R_2 determine the operating mode (doubler or inverter) of the MAX860/861 ICs, depending on the polarity of TxD. Zener diodes D_2 , D_3 , D_6 , and D_8 protect the MAX860/861 ICs from supply overvoltages.

The digital-output TLP2200 optoiso-

lators provide galvanic isolation and generate the RxD received signals with RS-232C logic levels. The circuit provides galvanically isolated communication in full-duplex mode at any standard transmission speed. The use of galvanic isolation allows transmission over nearly twice the distance for nonisolated systems. If you use a four-wire cable and split the separation circuits at the cable ends, you can further increase the transmission distance. (DI #2315).

> To Vote For This Design, Circle No. 333



RS-232C-interface ICs and optoisolators provide a supplyless RS-232C transmission link with galvanic isolation for increased distance.

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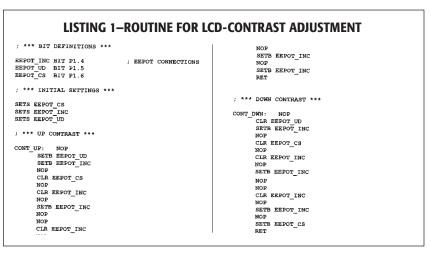
design**ideas**

Digital pot adjusts LCD's contrast

Jef Collin, CSE Systems, Turnhout, Belgium

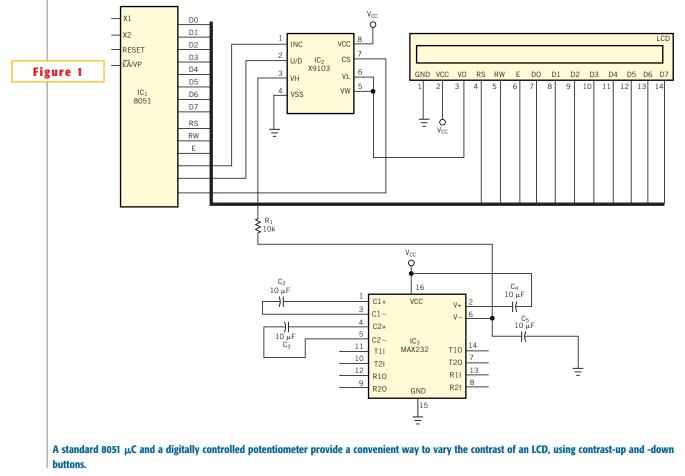
OU CAN USE A DIGITALLY controlled potentiometer for many purposes. In this example, you can use the device to regulate the contrast of a standard (such as two lines by 40 characters) LCD. You can use the circuit in Figure 1 in a portable test system, in which you need to change the contrast of the LCD as a function of the viewing angle. You choose the contrast setup from a menu and then use up or down buttons with $\mu C IC_1$ to adjust the contrast. The µC stores the contrast value in the digital potentiometer, IC₂. This design uses a Xicor 10-k Ω unit (dubbed "EEPOT"), but you could use other devices in the design.

The EEPOT connects to the LCD's VO line. You could connect the other side of the potentiometer to ground, but, for better contrast, you can apply a negative voltage to this terminal. This circuit has a



serial interface, so it uses the negativevoltage generator in the MAX232 RS-232C/TTL converter. **Listing 1** is the subroutine for the 8051 μ C. The program calls the routines for contrast-up or -down. (DI #2314).

To Vote For This Design, Circle No. 334





Add speech encoding/decoding to your design

/* Table of index changes */

int step;

1

step >>= 1;

{

}

}

if(diff >= step)

Rodger Richey, Microchip Technology Inc, Chandler, AZ

DDING SPEECH capabilities to a design can sometimes lead to complex algorithms and expensive DSPs or specialized audio chips. However, with the completion of a simplified adaptive differential pulse-codemodulation (ADPCM) algorithm, you can now implement these audio capabilities in low-cost 8-bit µCs, which typically have lower power consumption and cost than their DSP or audio-chip counterparts. A two-chip design is feasible by offloading the encoding and decoding tasks onto the μ C as if it were a peripheral.

Since 1991, the Interactive Multimedia Association (IMA) Digital Audio Technical Working Group (DATWG) has been working to define a cross-platform digital-audio exchange format. An inherent problem exists with the exchange of audio data between PC, Mac, and workstation computers. Each computer has its own data types and sampling rates. In May 1992, IMA DATWG published the first revision of the Cross-Platform Digital Audio Interchange recommendation that specifies three uncompressed and one compressed data type at various sample rates. The compressed data type is the Intel (www. intel.com) 4-bit DVI ADPCM algorithm. This algorithm compresses a 16-bit signed audio sample into 4 bits and takes advantage of the high correla-

tion between consecutive samples, which enables the prediction of future samples. Instead of encoding the sample itself, ADPCM encodes the difference between a predicted sample and the actual sample. This method provides more efficient

/* Quantizer step size lookup table * const long StepSizeTable(89] = {7,8,9,10,11,12,13,14,16,17,19,21,23,25,28,31,34,37,41, 45,50,55,60,66,73,80,88,97,107,118,130,143,157,173,190, 209,230,253,279,307,337,371,408,449,494,544,598,658,724 796,876,963,1060,1166,1282,1411,1552,1707,1878,2066,2272, 2499, 2749, 3024, 3327, 3660, 4026, 4428, 4871, 5358, 5894, 6484, 7132, 7845, 8630, 9493, 10442, 11487, 12635, 13899, 15289, 16818, 18500,20350,22385,24623,27086,29794,32767}; signed int diff; // Diff. between sample and predicted sample // Quantizer step size // ADPCM predictor output, Predicted diff. signed int predsample, diffq; char index; // Index into step size table char ADPCMEncoder(signed int sample) char code: // ADPCM output value predsample = state.prevsample; // Restore previous values of predicted index = state.previndex; step = StepSizeTable[index]; // sample and quantizer step size index diff = sample - predsample; // Compute diff. between actual sample $if(diff \ge 0)$ // and the predicted sample code = 0;else code = 8; diff = -diff; diffq = step >> 3; // Ouantize the diff. into 4-bit ADPCM code if(diff >= step) // using the quantizer step size code |= 4; diff -= step; // Inverse quantize the ADPCM code into a // predicted diff. using the quantizer step diffq += step; // size step >>= 1; if(diff >= step) code |= 2; diff -= step; diffq += step;

LISTING 1-ADPCM ENCODER

const char IndexTable[16] = {-1,-1,-1,-1,2,4,6,8,-1,-1,-1,-1,2,4,6,8};

code |= 1; diffq += step; if(code & 8) // Compute new predicted sample by adding predsample -= diffq; // the old predicted sample to new diff. else predsample += diffq; // Check if overflow of the new pred. sample index += IndexTable[code]; // Find new quantizer stepsize if(index < 0) $\,$ // Check if overflow of new quantizer step index = 0;if(index > 88) index = 88; state.prevsample = predsample; // Save values for next iteration state.previndex = index; return (code & 0x0f); // Return the ADPCM code

compression with fewer bits per sample and yet preserves the overall quality of the audio signal. Both the encoder routine (Listing 1) and the decoder routine (Listing 2) are written in C to ease readability.

The hardware implementation depends on the type of interface. With a parallel interface, you can use the PIC16C556A (Microchip Technology, www.microchip.com) (Figure 1a). A standard parallel interface uses the chip-



select (CS), output-enable (OE), and write-enable (WR) pins on Port A. The 8-bit data interface connects to the 8-bit Port B on the μ C. You can use two additional I/O lines for status information, such as encode/decode select, to the μ C or an interrupt line to the main controller to indicate when data is ready. CS, which connects to the RA₄ pin, can interrupt the PIC16C556A on the start of a transmission.

The second hardware implementation uses a serial interface and an eight-pin μ C (**Figure 1b**). The PIC12C672 uses four of the pins for power, ground, and oscillator input and output. Three of the remaining I/O pins are for clock (SCK), data in/out (D_{IN}/D_{OUT}), and CS. You can use the other I/O pin to indicate the desired encode/decode operation or as an interrupt to the main controller. CS connects to the external interrupt pin, GP₂, to detect the start of a transmission.

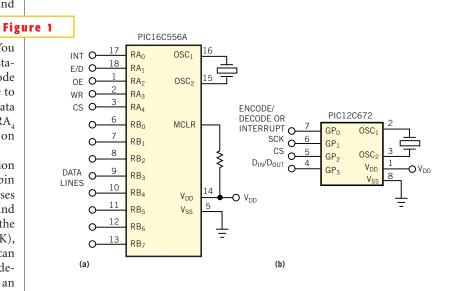
Both µCs have a flexible oscillator structure for use with a crystal, a resonator, or an external clock signal. Both parts of the figure show the μC using an external crystal as the clock source. Because these devices are fully static, the main controller can provide the clock source to the µC. By turning the clock source on and off as necessary, the main controller can further decrease overall power consumption. This method also allows control of the speed at which the algorithm runs, which is proportional to the sample rate of the system.

To fully implement the μ C as an ADPCM-encoder/decoder peripheral requires firmware to implement the serial or parallel interface, such as **listings 1** and **2**, and a main routine to tie everything together. The main controller is responsible for sampling the incoming audio waveform, storing and retrieving the AD-PCM codes from nonvolatile memory, and then playing the resulting samples. The main con-

troller feeds samples or ADPCM codes to the μ C and then reads the resulting AD-PCM codes or samples from the μ C.

The listings are available for down-

ł



Using the simplified ADPCM algorithm, you can now implement audio capabilities in μ Cs by offloading the encoding and decoding tasks onto the parallel (a) or serial (b) mC as if it were a peripheral.

LISTING 2–ADPCM DECODER

// This routine also uses the IndexTable and StepSizeTable from Listing 1 signed int ADPCMDecoder(char code) $\,$

<pre>predsample = state.prevsample; index = state.previndex;</pre>	// Restore previous values
<pre>step = StepSizeTable[index];</pre>	// Find quantizer step size
<pre>diffq = step >> 3; if(code & 4)</pre>	<pre>// Inverse quantize ADPCM code into a // diff. using the quantizer step</pre>
<pre>if(code & 8)</pre>	// Add the difference to predicted sample
if(predsample > 32767) predsample = 32767; else if(predsample < -32768) predsample = -32768;	// Check if overflow of new predicted samp.
index += IndexTable[code];	// Find new quantizer step size
<pre>if(index < 0)</pre>	// Check if overflow of new quantizer step
<pre>state.prevsample = predsample; state.previndex = index;</pre>	<pre>// Save values for next iteration</pre>
Seaterprevinder inder,	

loading from at *EDN*'s Web site, www. ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2292. (DI #2292)

To Vote For This Design, Circle No. 335

24

^{design}ideas Cheap PWM IC makes synchronous gate driver

Dimitry Goder, Switch Power Inc, Campbell, CA

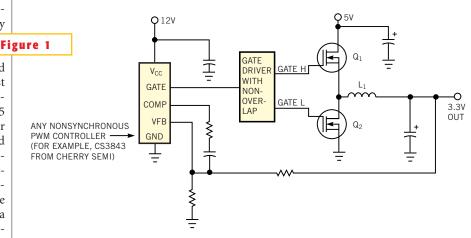
and peripherals usually requires several power-supply voltages. Designers typically use local switching regulators to produce the desired voltage rails. One of the most common topologies, the synchronous buck regulator, converts a 5 or 12V bus to some other, lower voltage. This approach has gained vast acceptance, thanks to its relative simplicity and high conversion efficiency. Specialized synchronous buck controllers are available, but you generally pay a premium for these ICs. Meanwhile, many inexpensive, generalpurpose PWM controllers are available, but they require you to implement synchronous rectifica-

system with a µP, memory,

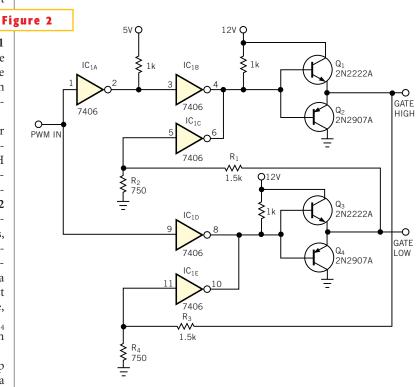
tion with discrete circuitry. The implementation is a difficult task, because it involves building two out-ofphase, mutually exclusive gate drivers. The block diagram in **Figure 1** shows how to use any general-purpose PWM controller (for example, the CS3843 from Cherry Semiconductor in East Greenwich, RI) to configure a synchronous buck regulator.

The most critical aspect of the driver design is nonoverlap timing, which prevents simultaneous high states at gates H and L, thus eliminating the simultaneous turn-on of Q_1 and Q_2 , with resulting shoot-through currents. Figure 2 shows details of the driver block. The input signal passes through two inverters, IC_{1A} and IC_{1B} , to generate the Gate H signal in phase with the input. The complementary follower, Q1 and Q2, forms a current amplifier to provide sufficient drive for the top MOSFET. Meanwhile, IC_{1D} inverts the input, and Q_3 and Q_4 amplify the signal to drive the bottom MOSFET.

 IC_{1C} and IC_{1E} provide the nonoverlap function. Each of the inverters ensures a low state at the corresponding gatedrive output until the other driver's output falls below a certain threshold. This



All it takes to drive high- and low-side MOSFETs from a PWM controller is a simple driver with 180° out-ofphase outputs, but you must beware of simultaneous MOSFET conduction.

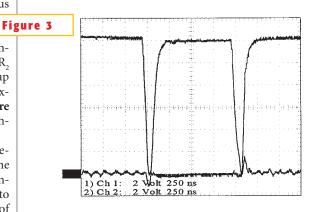


A sprinkling of TTL gates and four bipolar transistors provide efficient, nonoverlap drive to the two MOSFETs in a synchronous rectifier.



function prevents simultaneous high states, regardless of the circuit delays and the type of MOSFETs you use. The TTL switching threshold and the values of R_1, R_2 and R_3, R_4 determine the nonoverlap threshold. The threshold is approximately 3V for the circuit in **Figure** 2, but you can easily adjust it for other values.

Creating a high-side driver requires a bias voltage higher than the input voltage. A 12V line is commonly available, so you can use it to power the driver. The outputs of IC_{1B} and IC_{1D} must swing between ground and 12V; you thus need a 7406 open-collector inverter with a



At least 60 nsec separates the turn-on drive from the upper and lower drivers, thus preventing simultaneous MOSFET conduction.

high-voltage capability. If 12V is unavailable, you can use charge-pump circuitry to double the input voltage. The driver shows excellent performance, with 60-nsec nonoverlap time, superior to that of many available ICs. Figure 3 shows the two gate drivers' outputs, with each driver switching an IRL3103 n-channel MOSFET, a good choice for a 10A converter. The total cost of the driver does not exceed 30 cents. (DI #2306).

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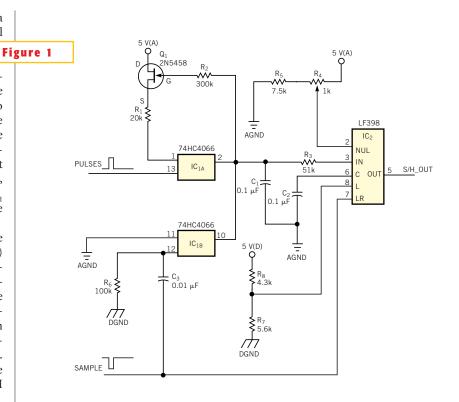
Circuit detects total on-time

Richard Nachazel, Vista Electronics Co, Ramona, CA

T HE CIRCUIT IN **Figure 1** provides a voltage that is directly proportional to the sum of the total ontimes for a number of positive pulses that occur during the interval between sample signals. When a positive pulse arrives at the control input to switch IC_{1A} , a constant-current source charges capacitor C_1 through IC_{1A} for the duration of that pulse and for each subsequent pulse. The constant-current source comprises Q_1 ; R_1 ; C_1 ; and R_2 , which drives Q_1 's gate at C_1 's potential. C_1 and C_2 should be noninductive and have low dielectric absorption.

When you apply a low signal to the Sample line, the sample/hold circuit (IC₂) latches the analog voltage on C_1 . You adjust R_4 for 0V at the output with no pulses at the input. The trailing edge of the Sample signal switches IC_{1B} on, discharging C_1 to an initial 0V potential. You can connect unused analog switches in parallel with IC_{1B} to speed the discharge. Higher supply voltages also improve the circuit's speed and performance. (DI #2300).

To Vote For This Design, Circle No. 337



Two ICs, a FET, and a handful of components form a pulse-width-to-voltage converter.

Edited by Bill Travis and Anne Watson Swager

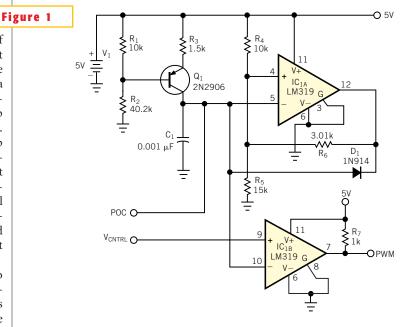
Simple circuit provides efficient PWM

Kenneth Levine, Eldec, Lynwood, WA

ou often need to control the duty cycle of a square wave. The circuit in Figure 1 works from a single 5V supply at a frequency of 100 kHz. With minor component changes, you can configure it for a range of frequencies. The circuit consists of a ramp (sawtooth) oscillator and a comparator. The circuit compares the ramp to an externally applied voltage, V_{CNTRL}. When V_{CNTRL} is greater than the ramp voltage, the PWM output is 5V. The sawtooth oscillator consists of a current source $(R_1, R_2, R_3, and Q_1)$, a timing capacitor (C_1) , and the oscillator-control circuitry $(R_4, R_5, R_6, and IC_{1A})$. The oscillator-control circuitry sets the upper and lower voltages of the timing capacitor at 3 and 1V.

 R_1 and R_2 set the voltage at Q_1 's base to 1V. R_3 and the V_{BE} drop (0.7V) are in parallel with R_1 , so the voltage across R_3 is 0.3V for a current of 200 mA. Because the emitter current greatly exceeds the base current, the collector current is nearly 200 mA. A capacitor receiving its charge from a current source charges linearly. The current in C_1 is 200 mA, and the change in voltage is 2V (1 to 3V). From I=CdV/dt, dt=10 msec, and the frequency is 100 kHz. The oscillator-control circuitry uses a comparator with hysteresis to compare the capacitor (ramp) voltage

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Monostable makes low-cost F/V converter 148



ideas

A dual comparator and a handful of components configure an inexpensive PWM generator.

with the charge limits. An externally applied power-on-clear (POC) signal ensures reliable start-up. POC must connect to an open-collector device that pulls to ground at power-on and produces no voltages when inactive.

After removal of POC, IC_{1A} 's Pin 5 is at ground, IC_{1A} 's Pin 12 is at open-collector status, and IC_{1A} 's Pin 4 is at 3V (the voltage across R_5). C_1 now starts charging. When the voltage on C_1 exceeds 3V, IC_{1A} 's Pin 12 switches to nearly ground, IC_{1A} 's Pin 4 drops to 1V (the voltage across the parallel combination of R_5 and R_6), and the charge on C_1 rapidly bleeds off through D_1 . The discharge time is short enough to have a negligible effect on the oscillation frequency. When the voltage on C_1 drops below 1V, IC_{1A} 's Pin 12 switches to open-collector status, D_1 stops conducting, and C_1 begins to charge again. The entire cycle repeats, creating sawtooth oscillation.

The circuit creates PWM by comparing the voltage on C_1 with V_{CNTRL} . As long as V_{CNTRL} is greater than the voltage on C_1 , the PWM output stays at 5V. You should limit V_{CNTRL} to a bit more than 1V and a bit less than 3V to prevent comparator oscillation. If the source of V_{CNTRL} can tolerate it, you can add hysteresis. The relationship of PWM to V_{CNTRL} is linear: PWM width=50(V_{CNTRL} 21)%, valid for $1V < V_{CNTRL} < 3V$. To increase the operating frequency, you can replace the LM319 with a faster comparator. (DI #2309).

To Vote For This Design, Circle No. 385



Visual Basic models MDAC offset

Olga Belousava, Los Alamos, NM, and Alex Belousov, New York, NY

T'S HARD TO IMAGINE THAT, for such an old-hat item as a standard R-2R multiplying DAC (MDAC), there still exists some "dark area" in modeling and calculating its dc offset, V_{OFF}, and related output resistance, R_o. You can obtain some information from references 1 and 2 and other references regarding the code dependency of Ro and Vo, but the simplified formulas given therein are insufficient for thorough engineering analysis/design and computer modeling/ simulation. Moreover, these formulas apply mainly to the case in which the Ref erence pin (Figure 1) is open, whereas most MDAC applications connect the Reference pin to a low-impedance source. Also, the source resistance, R_{IN} , has an impact on V_{OFF} and R_o. This Design Idea introduces an equivalent circuit for the MDAC and discusses mathematical models. A software program, "DAC Designer AO," simplifies the offset calculations. You can download the Visual Basic files from EDN's Web site, www. ednmag.com. At the registered-user area, go into the Software Center to download

TABLE	1-MAXIMU	M OFFSET	WITH REF PIN GRO	UNDED
Ν			Binary	
(bits)	Decimal	Hex	(maximum)	V _{OFF}
8	235	00EB	11101011	2.652*V _{os}
9	469	01D5	111010101	2.763*V _{os}
10	939	03AB	1110101011	2.875*V _{os}
11	1877	0755	11101010101	2.986*V _{os}
12	3755	OEAB	111010101011	3.097*V _{os}

the files from DI-SIG, #2305.

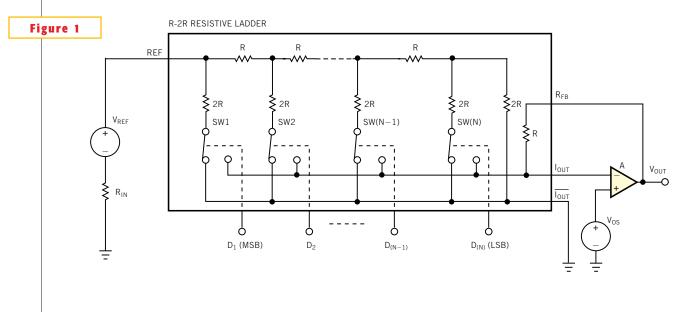
The models are based on the idealized R-2R resistive ladder in **Figure 1** with zero on-resistance and infinite off-resistance in the switches and without current leakage or parasitic voltages. **Figure 2** gives an equivalent reciprocal- π network for the ladder, in which G₁₁ is the input conductance with the output terminals shorted, G₁₂ is the transfer conductance, and G₂₂ is the output conductance with the input terminals shorted. The applicable math formulas are as follows:

$$G_{11} = 1/R,$$

 $G_{12} = \sum_{i=1}^{N} (D_i - 2^{-i})/R,$

$$G_{22} = (\sum_{i=1}^{N} (D_i(1+2 \cdot 4^{-i}) - \frac{N^{-1}}{(D_i(1-4^{-i}) \cdot \sum_{j=i+1}^{N} (D_j \cdot 2^{-j})))/3R}$$

It's obvious that G_{11} has a constant value, the reciprocal of the base resistance, R. G_{12} is a linear function of the input code and base resistance R. The expression for G_{22} , however, reveals complex, nonlinear behavior as a function of the digital input code. A Thevenin transform in **Figure 2**'s circuit produces the simplified equivalent circuit in **Figure 3**. The output resistance, R_0 , in the most common case, when the MDAC connects to



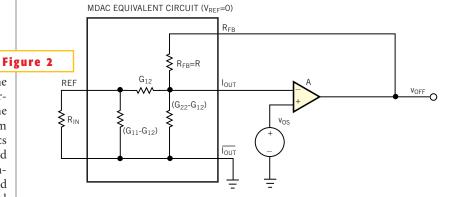
The output impedance of a multiplying R-2R DAC is a complex, nonlinear function (third equation in the text) of the digital input code.



a low-resistance source, is the reciprocal of G_{22} . The offset voltage is thus

 $V_{OFF} = V_{OS} \bullet (1 + R \bullet G_{22}).$

Table 1 gives the maximum theoretical values for V_{OFF} in 8- to 12-bit MDACs. You can easily obtain the exact values for V_{OFF} and R_O for any arbitrarily chosen input code by using the cited software program. The program also allows you to compute the statistics (maximum V_{OFF} , its mean, and standard deviation) for any predefined range of input codes. You can use the suggested equivalent circuit and mathematical models with any computer simulation packages in dc-analysis mode. (DI #2305).

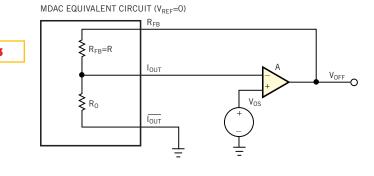


The input conductance, transconductance, and output conductance of the MDAC in Figure 1 provide a convenient simplification of the circuit.

References

1. Sheingold, Daniel H, Editor, Analog-Digital Conversion Databook, Prentice-Hall, 1986. 2. Data Converter Reference Manual, Volume 1, pg 2-540 to 2-541, Analog Devices, 1992.

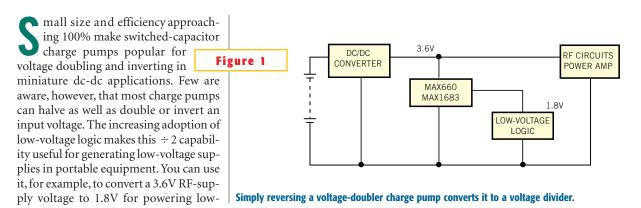
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A Thevenin transformation of the equivalent circuit in Figure 2 produces a greatly simplified circuit.

Charge-pump circuit divides by two

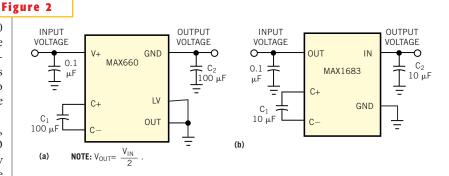
Budge Ing, Maxim Integrated Products, Sunnyvale, CA



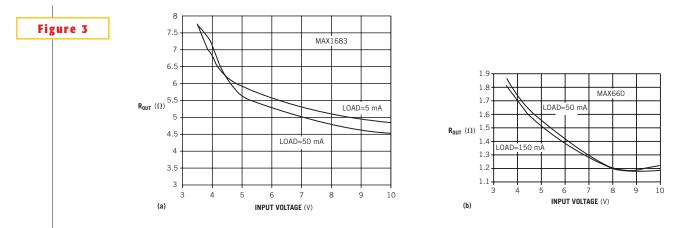


voltage logic (**Figure 1**). Simply reversing the input and output of a voltage doubler makes it a voltage divider. Implementing this scheme with MAX660 or MAX1683 voltage-doubler charge pumps requires only three external capacitors (**Figure 2**). Both configurations in **Figure 2** accept input voltages of 3.6 to 10V, but they present trade-offs in size and output-current capability.

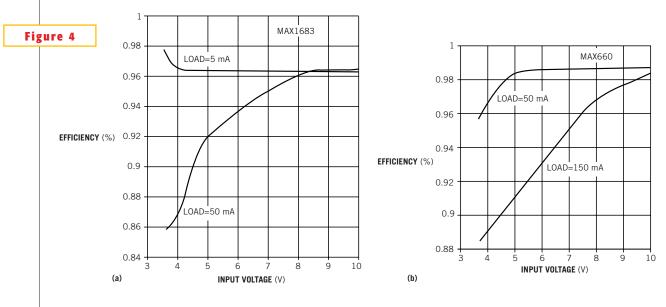
For 3.6V inputs, the robust MAX660, which comes in an eight-pin DIP or SO package, delivers 150 mA with efficiency greater than 88% and an output-voltage drop of less than 300 mV. If you require a smaller package, the MAX1683 (avail-



A MAX660 voltage doubler makes an efficient 150-mA voltage divider (a); the smaller MAX1683 does the same for applications requiring only 50 mA (b).



Over the usable 3.6 to 10V input-voltage range, the small MAX1683 (a) exhibits higher output resistance than the more robust MAX660 (b).



Both the MAX1683 (a) and the MAX660 (b) offer better than 90% efficiency over a large portion of their usable operating range.

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able in a five-pin SOT-23) offers 50-mA capability with a 3.6V input and as much as 100 mA with inputs higher than 8V. Its efficiency is 97% at 5 mA and 86% at 50 mA. Each device has an internal clock. The MAX660 runs at a nominal 10 kHz (with the FC pin open), and the MAX1683 runs at a nominal 35 kHz. Each divider's output resistance depends on the internal clock frequency, the flying capacitor (C_1), the resistance of the

$$R_{OUT} = \frac{1}{f_{OSC}C_1} + 4(R_4 + R_2 - R_1 - R_3) + 2R_{ESR}$$

internal switches, and the resistance of the output capacitor C_2 . You can calculate the output resistance by:

where f_{OSC} is the oscillator frequency, R_1 to R_4 are the $R_{DS(ON)}$ values for the four internal switches, and R_{ESR} is the equivalent series resistance for the output capacitor, C_2 . The graphs in **Figure 3** illustrate the

performance of the charge pumps operating in voltage-divider mode. **Figure 3a** shows the output resistance versus input voltage for the MAX1683. **Figure 3b** shows the same parameters for the MAX660. **Figure 4** shows efficiency versus input voltage for the MAX1683 (**Figure 4a**) and the MAX660 (**Figure 4b**). (DI #2301).

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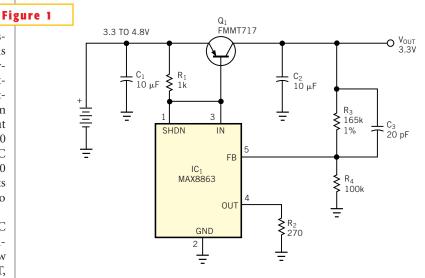
Pass transistor lowers dropout voltage

Matt Schindler, Maxim Integrated Products, Sunnyvale, CA

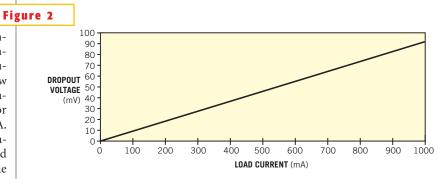
ITH LINEAR REGULATORS, YOU measure dropout voltage, V_{IN}-V_{OUT}, at the minimum input voltage for which the IC sustains regulation. Low dropout means longer battery life, because the load circuit continues to operate while the battery discharges to a lower terminal voltage. The external transistor helps to form a linear-regulator circuit whose dropout voltage at 100-mA load current is only 10 mV (Figure 1). (The linear-regulator IC by itself specs a 100-mV dropout at 100 mA.) The external transistor also boosts the maximum available load current to 1A.

Unorthodox connections enable the IC to drive Q_1 . Connecting Pin 3 to the transistor's base allows base current to flow through the internal switching MOSFET, out of Pin 4, and through R_2 to ground. The MOSFET then regulates V_{OUT} by controlling Q_1 's base current. Because C_2 sets a dominant pole that stabilizes the

loop, you should choose a ceramic type or other low-ESR capacitor. C_2 improves the phase margin by forming a pole-zero combination that increases the phase at crossover. Q_1 saturates when the battery voltage drops low enough for V_{OUT} to drop out of regulation, and R_2 limits the base current for that condition to approximately 10 mA. Q_1 's collector-emitter voltage at saturation, 10 mV with 1-mA base current and 100-mA collector current, sets the dropout voltage for these conditions.







Dropout voltage for the circuit in Figure 1 varies from 10 mV at 100 mA to 90 mV at 1A.



The measured dropout voltage varies with load current (**Figure 2**). The circuit delivers as much as 1A at 3.3V. You can adjust the output from 5.5V down to 1.25V using the formula V_{OUT} =

1.25[1+(R_3/R_4)], with appropriate changes to the value of R_2 , using the formula R_2 =($V_{IN(MIN)}$ -0.7V)/10 mA. Small components allow the entire circuit to occupy less than 0.24 in.² of board area.

(IC₁ comes in an SOT-23 package.) (DI #2323).

To Vote For This Design, Circle No. 388

PIC μC implements CRC-16 algorithm

Lon Glastner, Solutions Cubed, Chilo, CA

ETECTING ERRORS IN SERIAL DATA can be paramount in completing an embedded-control design. Determining which algorithm to use for detecting serial-communications errors depends on several factors. Ideally, the method should require minimal hardware and little computational power from your processor and still provide high-level protection against undetected data errors. The cyclic redundancy check (CRC) combines all these factors under one umbrella. A multitude of CRC flavors exists, including the Dow CRC (8 bits), CRC-16, and CRC-CCITT (both 16 bits). The CRC-16 uses a 16-bit shift register and can detect the following error types:

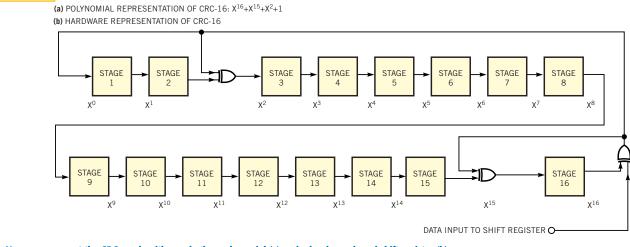
- any cluster of errors within a 16-bit section of data,
- any odd number of errors within the data field,
- all double-bit errors in the data field, and
- most large clusters of errors.

T/	\BL	E 1-XOR TRUTH TABLE
X	Y	XOR
0	0	0
0	1	1
1	0	1
1	1	0

You can characterize the CRC-16 as both a polynomial expression and as a hardware-based shift register (Figure 1). You can implement a CRC-16 in a midrange PIC µC with minimal coding and without additional hardware. Selecting a µC with an on-chip USART, such as the PIC16C63, eases serial communications. This implementation does not focus on the mathematical proof of a CRC-16's error-correcting effectiveness. The CRC algorithm is so effective it's an industry-accepted method for detecting data errors. The heart of a CRC-16 algorithm is a shift register. You generate the shift register by shifting each data bit through the algorithm. In this implementation, the data shifts the most significant bit first, one data byte at a time.

Two temporary registers buffer the data to prevent the shifting from corrupting the data. The shift register comprises two separate 8-bit registers, CRC16_HI and CRC16_LO. The most significant bit of CRC16 HI is the location of Stage 16 (Figure 1). From the figure and Table 1, you can see that the result of XORing the input data bit and the contents of Stage 16 of the shift register determines the effect that new data has on the shift register. If the result is a one, then you must complement the contents of stages 2 and 15 before rotating the new data into the shift register. If the result is a zero, then the new data can rotate immediately into the shift register. Some housekeeping tips can be helpful here. The data transmitter should generate its CRC-16 in the same manner as the data receiver. Also, it's advisable to clean the CRC-16 shift register before rotating the first data bit of the data string into it.

Figure 1



You can represent the CRC-16 algorithm as both a polynomial (a) and a hardware-based shift register (b).

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How does the CRC-16 identify data errors? The simplest method is to attach the shift register to the end of the data string. In this implementation, the CRC16_HI register should follow the last byte of data sent. The CRC16_LO register follows the CRC16_HI register. If the receiving system computes a CRC-16 value from all the data bytes and the attached shift register (CRC16_HI and CRC16_LO), then the resulting CRC-16 code is 0000h. Any nonzero result indicates an error in the data. In some systems, an error may occur that results in all zeros being sent as the data and attached CRC-16. This type of error poses as error-free data. In these systems, you can overcome the false indication by complementing the CRC-16 before attaching it to the data string. The CRC-16 shift register generated by attaching the complement is always 800Dh.

The code fragment in **Listing 1** generates a CRC-16 shift register on a byte-bybyte basis. You could embed this code within serial-receive and serial-send routines to provide a powerful error-detection tool. You can easily generate the

movf CRC16_HI,W ;Move upper shift register to working reg. xorwf DATA_TEMP1 ;XOR shift register with data register btfss DATA_TEMP1,7 ;MSB is XOR of stage16 and input data bi goto No_Xorwf ;1f bit is clear then no complement of stage moviw 00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rf DATA_TEMP0 rlf DATA_TEMP1 ;Rotate next data bit into position rlf CRC16_LO ;Shift CRC16_LO rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits			CRC-16 shift register from the data byte stored
MAKE_CRC16 movf DATA_REG,W movfw Y0001000°b ;Store data in temporary register movfw Y0001000°b ;Store data bits movfw YUMBER_BITS ;Load counter register movf DATA_TEMP0,W ;Move buffered data to 2 nd buffer movf DATA_TEMP1 ;This register is corrupted with every pass movf CRC16_H1,W ;Move upper shift register to working reg. xorwf DATA_TEMP1 ;XOR shift register with data register btfss DATA_TEMP1 ;XOR shift register to complement of stage movlw '00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage15 of shift register xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate next data bit into CRC16_LO pistift CRC16 register			
MAKE_CRC16 movf DATA_TEMP0 movwf DATA_TEMP0 movwf DATA_TEMP0 movwf DATA_TEMP0 movwf NUMBER_BITS movwf NUMBER_BITS movwf DATA_TEMP0,W movwf DATA_TEMP1 movwf DATA_TEMP1 movf DATA_TEMP1 movf DATA_TEMP1 movf DATA_TEMP1 movf DATA_TEMP1 movf DATA_TEMP1 movf OATA_TEMP1 movf OATA_TEMP1 movf OATA_TEMP1 movf OATA_TEMP1 movf OATA_TEMP1 movf OATA_TEMP1 goto No_Xorwf movlw '00000010'b prepare to complement stage2 xorwf CRC16_LO movlw '01000000'b prepare to complement stage15 xorwf CRC16_HI complement stage15 of shift register No_Xorwf "ff rlf DATA_TEMP1 rlf			
movf DATA_REG,W movvf DATA_TEMP0 ;Store data in temporary register movvf DATA_TEMP0 ;Store data in temporary register movvf NUMBER_BITS ;Load counter register More_Rotates	,		
movwf DATA_TEMP0 ;Store data in temporary register movlw '00001000'b ;Set counter for 8 data bits movwf NUMBER_BITS ;Load counter register More_Rotates : : movf DATA_TEMP0,W :Move buffered data to 2 nd buffer movf DATA_TEMP1 :This register is corrupted with every pass movf CRC16_H1,W :Move upper shift register to working reg. xorwf DATA_TEMP1 :XOR shift register with data register btfss DATA_TEMP1 :XOR of stage16 and input data bit goto No_xorwf :If bit is clear then no complement of stage movlw '00000010'b :Prepare to complement stage2 xorwf CRC16_LO :Complement stage15 of shift register No_Xorwf :If DATA_TEMP0 :Rotate next data bit into position rlf DATA_TEMP1 :Rotate XOR of input into CRC16_LO rlf DATA_TEMP1 :Rotate XOR of input into			
movlw '00001000'b ;Set counter for 8 data bits movvf NUMBER_BITS ;Load counter register More_Rotates			:Store data in temporary register
More_Rotates :Move buffered data to 2 nd buffer movf DATA_TEMP0,W :Move buffered data to 2 nd buffer movf DATA_TEMP1 :This register is corrupted with every pass movf CRC16_H1,W :Move upper shift register to working reg. xorwf DATA_TEMP1 :XOR shift register with data register btfss DATA_TEMP1,7 :MSB is XOR of stage16 and input data bi goto No_Xorwf :If bit is clear then no complement of stage movlw '00000010'b :Prepare to complement stage2 xorwf CRC16_LO :Complement stage15 xorwf CRC16_HI :Complement stage15 xorwf CRC16_HI :Complement stage15 vorwf DATA_TEMP0 :Rotate next data bit into position rlf DATA_TEMP1 :Rotate XOR of input into CRC16_LO rlf CRC16_LO :Shift CRC16 register rlf CRC16_LO :Shift CRC16 register rlf CRC16_LO :Shift CRC16 register cdecfsz NUMBER_BITS :Count out 8 data bits			
movf DATA_TEMP0,W ;Move buffered data to 2 nd buffer movvf DATA_TEMP1 ;This register is corrupted with every pass movvf CRC16 HI,W ;Move upper shift register to working reg. xorwf DATA_TEMP1 ;XOR shift register with data register btfss DATA_TEMP1,7 ;MD8 is XOR of stage16 and input data bit goto No_Xorwf ;If bit is clear then no complement of stage movlw '00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage2 of shift register worwf CRC16_HI ;Complement stage15 of shift register xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Shift CRC16 register rlf CRC16_LO ;Shift CRC16 register rlf CRC16_LH ;Shift CRC16 register	movwf	NUMBER BITS	:Load counter register
movf DATA_TEMP0,W ;Move buffered data to 2 nd buffer movvf DATA_TEMP1 ;This register is corrupted with every pass movvf CRC16 HI,W ;Move upper shift register to working reg. xorwf DATA_TEMP1 ;XOR shift register with data register btfss DATA_TEMP1,7 ;MD8 is XOR of stage16 and input data bit goto No_Xorwf ;If bit is clear then no complement of stage movlw '00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage2 of shift register worwf CRC16_HI ;Complement stage15 of shift register xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CATA_TEMP1 ;Shift CRC16 register rlf CRC16_LO ;Shift CRC16 register rlf CRC16_LH ;Shift CRC16 register	More Rotates	-	
movf CRC16_HI,W ;Move upper shift register to working reg. xorwf DATA_TEMP1 ;XOR shift register with data register btfss DATA_TEMP1,7 ;MSB is XOR of stage16 and input data bi goto No_Xorwf ;If bit is clear then no complement of stage movlw 00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rlf DATA_TEMP0 rlf DATA_TEMP1 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_HI ;Shift CRC16 register rlf CRC16_LO ;Shift CRC16 register rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits		DATA TEMP0,W	;Move buffered data to 2 nd buffer
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bifss DATA_TEMP1,7 MSB is XOR of stage16 and input data bi goto No_Xorwf ;If bit is clear then no complement of stage movlw '00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage16 and input data bi movlw '0100000'b ;Prepare to complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	movf	CRC16 HI,W	;Move upper shift register to working reg.
goto No_Xorwf ;If bit is clear then no complement of stage movlw '00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage2 of shift register movlw '01000000'b ;Prepare to complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf	xorwf	DATA_TEMP1	;XOR shift register with data register
movlw 00000010'b ;Prepare to complement stage2 xorwf CRC16_LO ;Complement stage2 of shift register movlw 0100000'b ;Prepare to complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rff DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_HI ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	btfss	DATA TEMP1,7	;MSB is XOR of stage16 and input data bit
xorwf CRC16_LO ;Complement stage2 of shift register movlw 01000000b ;Prepare to complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	goto	No Xorwf	;If bit is clear then no complement of stage2,15
movlw '01000000'b ;Prepare to complement stage15 xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	movlw	'00000010'Ь	;Prepare to complement stage2
xorwf CRC16_HI ;Complement stage15 of shift register No_Xorwf	xorwf	CRC16_LO	;Complement stage2 of shift register
No_Xorwf Rotate next data bit into position rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	moviw	'01000000'ь	;Prepare to complement stage15
rlf DATA_TEMP0 ;Rotate next data bit into position rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	xorwf	CRC16_HI	;Complement stage15 of shift register
rlf DATA_TEMP1 ;Rotate XOR of input into CRC16_LO rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	No_Xorwf		
rlf CRC16_LO ;Shift CRC16 register rlf CRC16_HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	rlf	DATA_TEMP0	;Rotate next data bit into position
rlf CRC16 HI ;Shift CRC16 register decfsz NUMBER_BITS ;Count out 8 data bits	rlf	DATA_TEMP1	;Rotate XOR of input into CRC16_LO
decfsz NUMBER_BITS ;Count out 8 data bits	rlf	CRC16_LO	;Shift CRC16 register
, · · · · · · · · · · · · · · · ·	rlf		
soto More Rotates :Not finished with this data byte	decfsz		
Pero viere-received in the manual of the	goto	More_Rotates	;Not finished with this data byte

LISTING 1–PIC CODING FOR CRC-16 SHIFT REGISTER

CRC-16 on the fly, thus minimizing the use of processor resources. You can download the listing from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to

download the files from DI-SIG, #2321. (DI #2321).

To Vote For This Design, Circle No. 389

Monostable makes low-cost F/V converter

Mark Brinegar, Dart Controls Inc, Zionsville, IN

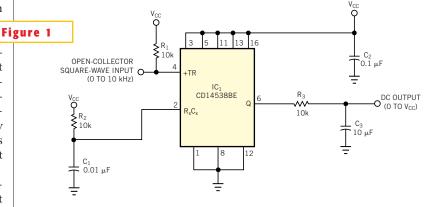
THE CIRCUIT IN **Figure 1** is a low-cost frequency-to-voltage (F/V) converter. Using a monostable (one-shot) multivibrator, the circuit accepts an open-collector square wave that varies in frequency from 0 to 10 kHz. The oneshot produces a pulse of a fixed width

each time the input signal triggers it. The result is a variable-frequency, variable-duty-cycle signal at the output of the one-shot. The time constant determined by R_2C_1 , 100 µsec, determines the width of the pulses the oneshot produces. This time matches the period of the maximum input frequency (10 kHz). The duty cycle of the one-shot's output is thus 100% when the input is at its maximum frequency.

The variable-frequency, variable-dutycycle output of the one-shot is the input for the lowpass filter comprising R_3 and C_3 . The net result is, as the input frequency varies from 0 to 10 kHz, the dc output signal varies from 0V to $V_{\rm CC}$. You can alter the circuit to accommodate different input frequencies by simply adjusting the $R_{\rm s}C_{\rm 1}$ time constant to match

the period of the desired maximum input frequency. (DI #2322).

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A single CMOS one-shot multivibrator provides a simple and inexpensive frequency-to-voltage conversion function.

Edited by Bill Travis and Anne Watson Swager

Simple circuit prevents processor latch-up

Michal Kobylecki and Wojda Wlodzimierz, MK Design, Warsaw, Poland

HE CIRCUIT IN Figure 1 uses a Dallas Semiconductor DS1820 one-wire digital thermometer in a multipoint temperature-measurement system. The DS1820 sensor allows distributed temperature measurement and uses only one wire for both data communication and the power supply. You can easily connect the one-wire interface to a µC (in this example, a PIC16C63). The application accommodates as many as 16 DS1820 sensors in a 100m-long network, dubbed MicroLAN by Dallas. Unfortunately, with such long wires near high-current power cables, inductively coupled high-voltage peaks can cause µC latch-up, because the transient-voltage suppressor, D₁, can-

not limit the line voltage below 9.8V. The interface circuit in **Figure 1** prevents such faults.

The sensor needs only one data line, but the interface circuit in **Figure 1** needs two CPU-control signals. The first is the inverted-output data line, connected to transistor Q_1 through resistor R_3 . If this line is at logic 1, the sensor's data line connects to ground. Otherwise, resistor R_4 pulls the sensor's data line to 5V. If the

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Photodetector sorts objects	114
Single-button lock provides high security	116

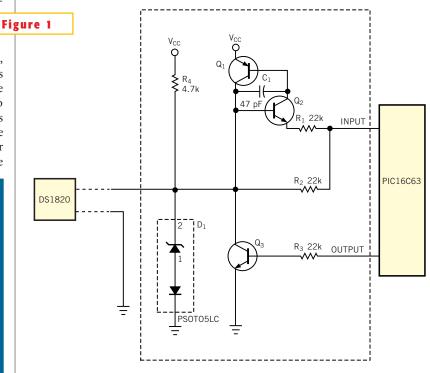
sensor transmits data, the μ C captures the data via R₂. If an overvoltage peak occurs, R₂ prevents μ C latch-up by limiting the current to the μ C pin. During the temperature conversion, the DS1820 needs an effective pullup circuit to provide an accurate conversion. Transistors Q₁, Q₂, and R₁ provide an effective pullup function, which the μ C activates by grounding the input signal to Q₃.

lideas

The pullup function also improves the rising edge of the transmitted data. If the sensor connects to the μ C through a long wire, the capacitance of the line degrades the rising edge of the data signals, because

of the line-capacitance- R_4 time constant. The short pulse from the pullup circuit improves the signal's rising edge. It's obvious that, when the pullup circuit turns on, Q_3 must be off. However, the circuit protects itself against unintended signal corruption. If Q_3 is open, the power voltage does not connect to the sensor's data line. If you replace R_4 with a 1-mA current source, you can obtain effective data transmission with lengths as great as 500m (empirically verified). (DI #2317).

To Vote For This Design, Circle No. 395



A simple three-transistor circuit provide both latch-up protection and signal conditioning in this one-wire sensor/µC interface.

34

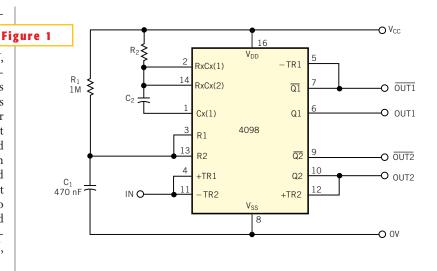


Dual one-shot makes rising- and falling-edge detector

Santo Camonita, Catania, Italy

HE DESIGN IN Figure 1 is an upgraded version of the circuit in a previous Design Idea ("Edge detector runs off single supply," EDN, Dec 4, 1997, pg 140). It has fewer components, draws less current, and has higher input impedance. The circuit uses a 4098 dual monostable multivibrator with both sections connected. The circuit generates a pulse on both the rising and the falling edges of a signal. The duration of the output pulse is T=0.5R₂C₂. R₁ and C₁ provide power-on reset. The circuit has another advantage: It provides two independent true outputs (Q1, Pin 6 and Q2, Pin 10) and two independent complementary outputs ($\overline{Q1}$, Pin 7 and $\overline{Q2}$, Pin 9). (DI #2316).

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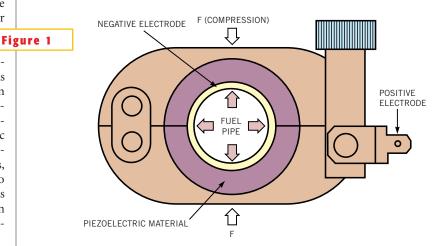
A dual monostable multivibrator provides a convenient means of detecting a signal's rising and falling edges.

Simple circuit measures diesel's rotations per minute

David Magliocco, CDPI, Scientrier, France

OU MAY FIND IT USEFUL to measure a diesel engine's rotations per minute to accurately adjust the idling or to compare the motor's speed under hot and cold conditions, for example. Not all cars or trucks come with a tachometer. The scheme in figures 1 and 2 allows you to measure rotations per minute with a DMM or an oscilloscope. In Figure 1, a piezoelectric sensor and an alligator clip, fastened directly to one of the four metal fuel pipes, detect the fuel-injection pulses. The piezo element generates a signal that connects to the signal-conditioning electronics in Figure 2 through a coaxial cable. The circuit uses a charge amplifier.

IC₁, a versatile ICL7611 chosen for its high input impedance, low bias current,



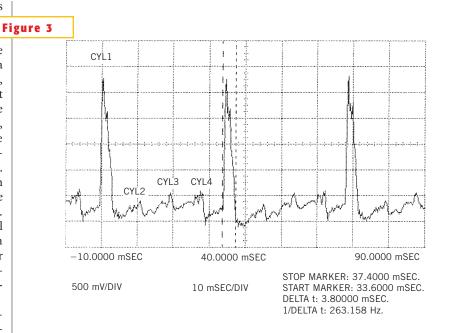
A piezoelectric sensor and an alligator clip provide an easy means of measuring the rpm of a diesel engine.



and reasonable power consumption, acts as an inverting current-to-voltage

converter. C1 integrates the highdV/dt sensor signal. R₁ ensures that the output of IC, is high in the absence of a signal. You must use high values for R₂, R₃, and R₄. The two diodes at the input protect the amplifier against overvoltage spikes. R₅ and R₆ create a virtual ground, so the circuit uses the full common-mode input range of IC₁. Figure 3 shows an oscilloscope trace of the amplifier's output. The three small peaks between the main pulses are parasitic and come from the injection pulses of the other cylinders. You can fine-tune the shape of the signal with C₁. A value near 1 nF yields a smooth signal with low amplitude; a value lower than 100 pF gives a noisy signal with narrow pulses. The value for the trace in Figure 3 is 100 pF.

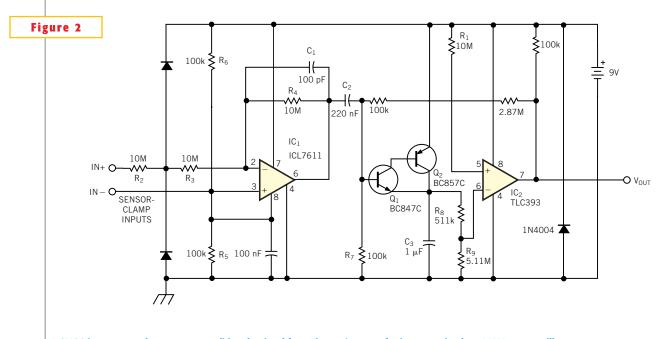
From one vehicle to another, the amplitude of the signal can vary over an approximately 2-to-1 ratio. You can't use a fixed threshold to shape the signal; either the threshold is too low, and you shape the parasitic pulses, or it's too high, and you obtain nothing. Thus, the signal-conditioning method compares the peak value to the average value: Only the main peaks are higher than the average value. C_2 and R_7 ignore the dc component of the charge amplifier's output signal, and



After conditioning, the main peaks in the sensor signal come from the cylinder under test; the secondary peaks, from the other cylinders.

transistors Q_1 and Q_2 charge C_3 to the peak value of that signal. You adjust R_8 and R_9 for a 90% ratio, which gives IC_2 , a low-power CMOS comparator, a large enough signal to shape. IC_2 delivers a logiclike signal that you can measure with a DMM (using the frequency/period range, or the rotations-per-minute range on an automotive DMM), or with an oscilloscope. (DI #2318).

> To Vote For This Design, Circle No. 397



A CMOS integrator and comparator condition the signal from Figure 1's sensor for interpretation by a DMM or an oscilloscope.

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designideas

Fast, compact routine interfaces EEPROM to μC

Grzegorz Mazur, Institute of Computer Science, Nowowiejska, Poland

HE CODE in **Listing 1** provides the interface between any MCS-51 family of μ Cs and a 24C01a/2/4/8/16 I²C EEPROM. The interface is purely software-driven, so any μ C port pins can control the EEPROM. This code is approximately two times smaller and approximately 20% faster than similar routines published by Atmel Corp (www. atmel.com). Careful coding of low-level routines and structural optimization produce the performance improvements.

The code is tuned for a -51 running at 12 MHz, but you can also use it at lower clock speeds. For higher speeds, you must adjust low-level routines by inserting "nop" instructions to match I²C-specified timings. The maximum data rate while reading memory content as 16-byte blocks is as high as 8.1 kbytes/sec. With minor modifications, you can use the routines to interface any I²C slave device to a -51 µC.

Listing 1 is available for downloading from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the "Software Center" to download the file from DI-SIG, #2329. (DI #2329).

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LISTING 1–I²C EEPROM-µC-INTERFACE ROUTINE

```
DEVADDR
              equ 0a0h ; EPROM I2C device address
scl bit p3.4
sda bit p3.5
 ; register usage
                          ; pointer to internal RAM buffer for block transfers
; r0 buf_ptr
; r1 count
; r2 addr_lo
; r3 addr_hi
                           ; byte count for block transfers
                           ; 2-byte memory address (up to 11 bits used)
                           ; used internally
; write block from RAM to EEPROM
       mov a, @r0
inc r0
acall shift_out
       jc stop
djnz rl, wblop
sjmp stop
write byte:
                           ; write single byte from ACC to EEPROM
       push acc
acall send_full_address
pop acc
jc fin
acall shift_out
cimp stream
       sjmp stop
                         ; read block from EEPROM to RAM
; 342 + 102 * nbytes
read_block:
       acall send_full_address
        jc fin
acall send_devaddr_rd
       jnc rbl
       ret
rblop:
       mov a, #0ffh
acall shift
                          ; input data from SDA and send ACK
acall shift
setb SDA
mov @r0, a
inc r0
rbl: djnz r1, rblop ; 2 + 102 * nbytes
acall shift_in_nak
mov @r0, a
inc r0
inc r0
       sjmp end_read
acall send_full_address
       jc fin
read current:
                           ; read next byte from active EEPROM page to ACC
                              224 C
       acall send_devaddr_rd
               fin
        acall shift_in_nak
end_read:
clr c
                           ; 10 C
stop:
                           ; Send STOP
; 9 C
       cir SDA
       setb SCL
```

nop nop nop nop setb SDA ; 4.7us after SCL : SCL & SDA high. ret send_full_address: ; 220 C clr acall send_devaddr ; send device address jc ; send byte address mov a, r2 sjmp soasc send_devaddr_rd: ; 112 C setb send_devaddr: ; 111 C ; Send START setb SCL jnb SCL, bbsy ; Check if bus available inb SDA, bbsy clr SDA, Dr clr SDA mov a, r3 rlc a ; min. 4.7 us after SCL high orl a, #DEVADDR clr SCL ; min. 4.0 us after SDA low , mail, will us after SDA low ; SCL & SDA low. ; send device id, 3 msbits of address and rw bit (from c) ; ; 101 C ; accil shift or soasc: acall shift_out jc stop fin: ret ; bus not available bbsy: setb c ret ; Shift out/in a byte from/to A, msb first and ACK bit from/to C. ; SCL low, SDA high on entry and exit. shift in nak: ; 96 C mov a, #Offh ; all ones - input data from SDA shift_out: ; 95 C setb c ; 9th bit - output NAK/release SDA fo shift: ; 94 C mov r4, #9 ; 8 bits + ack shlop: ; 3.5 us CLK low to data valid ; 3.5 us CLK rlc a mov SDA, c setb SCL ; move bit into C пор nop mov c, SDA SCL Cir SCL ; min. 4 us djnz r4, shlop ret ; ACK in C end



Photodetector sorts objects

Alan Erzinger, Harris Semiconductor, Palm Bay, FL

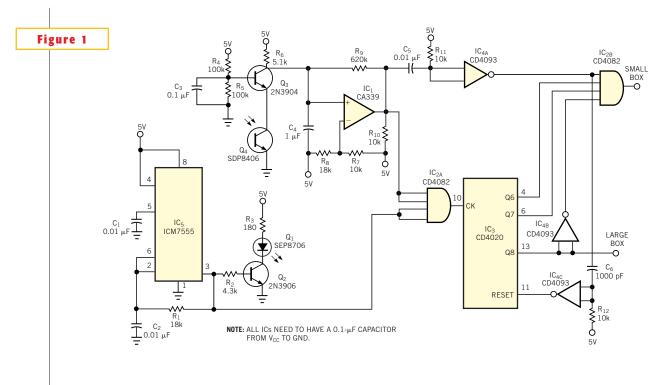
OST OBJECT-SENSING SYSTEMS have problems detecting the presence of an object. The system in Figure 1 uses an oscillator to ease detection problems and allow sorting. The oscillator reduces power dissipation in the photodiode by operating the diode at 50% duty cycle. The oscillator also enables a 50% increase in the noise-filter time constant, and it functions as a timebase to allow object sorting. The oscillator chops the photodiode's bias. The signal the photodetector receives is a square wave; thus, a filter can remove optical noise. You normally need filtering when light shines through fans onto the optical detector. When required, you can place a bandpass filter in series with Q₂'s output.

The oscillator frequency has two limits: the response time of the phototransistor and the accuracy of the objectsensing system. Q_4 and Q_3 are connected in a cascode configuration to minimize the Miller effect in Q_4 . This connection reduces the pair's optical transient response to nanoseconds, thus allowing oscillator periods of submicroseconds. Objects on a conveyor belt travel at relatively low speeds. You can calculate their expected time in front of the photodetector, t, from t=d/s, where s is the conveyor speed in feet per second and d is the object width in feet.

An object 2 in. long with a belt speed of 3.5 ft/sec blocks the detector for 47.6 msec. If the oscillator period is 250 µsec, the object blocks the detector for approximately 200 periods, so each period equates to 0.5% length accuracy. The system senses two objects-one 2 in. long and one much longer-so 0.5% accuracy is more than adequate. When the detector is unblocked, the inverting input of IC, is dominant, and it keeps the output of IC, low. The low state prevents the oscillator's output from reaching the counter (IC₃). Blocking the detector allows C_3 to charge to 5V through R_6 , and the noninverting input of IC, becomes dominant, starting the count. When the detector is unblocked, the one-shot comprising R₁₁, C₅, and IC_{4A} pulses IC_{2B} with an end-of-object pulse. The one-shot's trailing edge triggers the counter-reset one-shot comprising R_{12} , C_6 , and IC_{4C} .

C4 and R6 form a nuisance filter that rejects short optical noise. The timing is such to enable a 2-in. object to clear the detector while both Q_6 and Q_7 are high. When the end-of-object pulse coincides with Q_6 high, Q_7 high, and Q_8 low, the output of IC_{2B} indicates a 2-in. object. This situation is the only time window that can indicate a 2-in. object. If the object is longer than 2 in., Q₈ goes high, indicating a large object. When the object clears the detector, the reset one-shot resets the counter for another cycle, and Q₂ quickly discharges C4 in preparation for another cycle. With the component values shown, the system can sense and discriminate between objects as short as 2 in., separated by 0.1 in. (DI #2325).

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An oscillator circuit allows a photodetector to both count and sort objects according to size.

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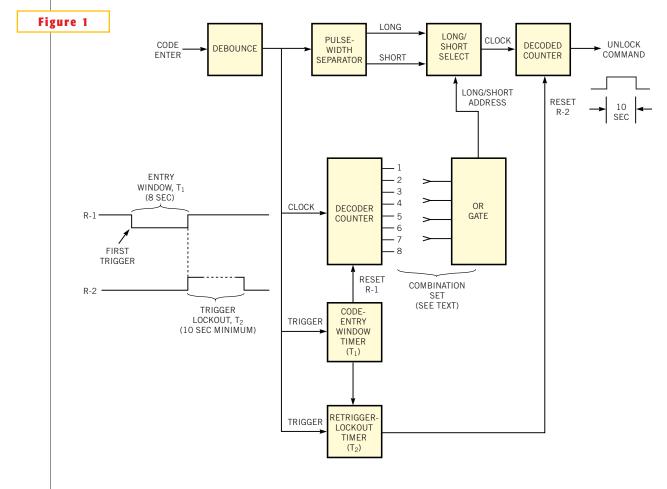
Single-button lock provides high security

Maxwell Strange, Fulton, MD

IGURE 1 IS THE BLOCK DIAGRAM OF an easily programmed, single-button combination lock. You operate the lock by using a series of short and long pulses from a momentary switch that masquerades as a doorbell button. The circuit uses inexpensive CMOS logic. The retriggerable timer, T₂, locks out entries made after the T1 code-entry window, thereby greatly enhancing security. The circuit in Figure 2 operates as follows: The Schmitt-trigger quad NAND gate, IC₁, debounces the code-entry switch and, with the aid of simple analog circuitry, produces separate outputs for activation times of less than and more than 0.3 sec. These outputs connect to the select gate, IC_5 . The initial entry also sets timer T_1 to enable the decoded decade counter, IC_4 . Each entry clocks IC_5 .

As IC_3 steps through its counts, certain of its output positions represent "short" and connect to IC_4 's inputs; unconnected lines represent "long" positions. This coding arrangement sets the combination. Short pulse positions change the address of IC_5 to select the short input pulse; otherwise, IC_5 selects the long pulse input. The short and long inputs, if present in the programmed sequence, produce an output from IC_5 . IC_6 counts the outputs and produces an unlock command only if it counts all pulses. The power-on-reset circuit ensures that no compromise of security arises under any conditions after a power outage. The timers are crucial to the high security of the system. You must enter the code within the 8-sec T_1 window. If you make a mistake, you must wait at least 10 sec for T_2 to time out before you make another attempt. If entries occur continuously and less than 10 sec apart, as an intruder might try, T_2 continuously inhibits counter IC₆.

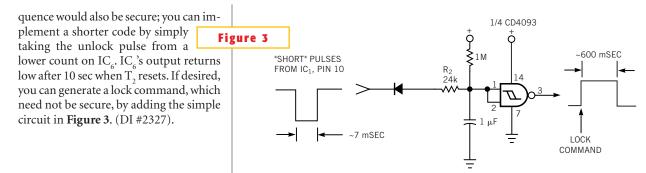
The lock proves to be reliable over several years of use. The circuit in **Figure 2** uses an eight-character combination, which you can quickly enter. A short pulse is a quick jab to the button; a long pulse is only slightly longer. A shorter se-



A handful of timers and counters configures a highly secure, single-button combination lock.

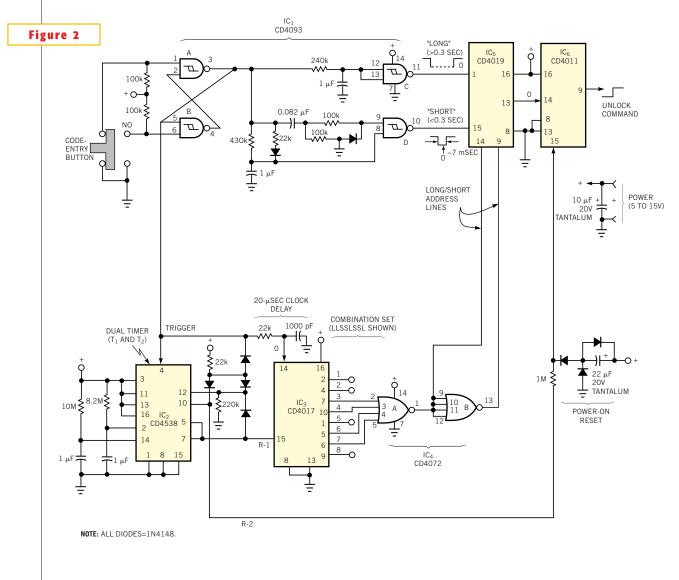
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You program your combination by hard-wiring the IC₃-IC₄ output-to-input connections, LLSSLSSL, where L and S are long and short inputs, respectively, in this example. Edited by Bill Travis and Anne Watson Swager

Model fixed-point DSP arithmetic in C

Roger Maher, SSL Ltd, Dublin, Ireland

OU CAN RUN INITIAL high-level simulations of custom numerical algorithms, such as digital filters, using floating-point numbers in an environment such as C or Matlab. Unfortunately, you won't see include fixed-point effects, such as truncation due to limited precision and register overflow, until you use a Hardware Design Language (HDL), such as Verilog or VHDL. However, a technique that models these effects in C-the function "bit_limit" in Listing 1-provides faster execution and better portability than HDLs and allows early exploration of the trade-off between bus width and performance.

Figure 1 shows a flow diagram that calculates the output $E=A/4+A\cdot B$. **Table 1** shows the effect of the chosen bus width. For example, the output of the multiplier truncates to 10 bits, and the output of the adder truncates to 9 bits. In this example, when input A=201.8 and input B=0.19, the output E=87.5; an ideal model without truncation would give 88.792.

Listing 1, the ANSI C code for the bit_limit function, shows how the code truncates. The code first converts float-ing-point numbers a_fl and b_fl to justi-

Model fixed-point DSP arithmetic in C	.125
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LED driver displays standing- wave ratio	.134
Comparator provides stable hysteresis	136

LISTING 1-FUNCTION "BIT_LIMIT" C CODE #include <stdio.h>

Jeas

```
/* Set the precision, ie. the maximum number of bits to the right of the 'binary' point */
#define PREC 8
/***********
   Function : bit limit
   Implements a precision limit on integers by regarding them as fixed point numbers with 'l' bits allowed to the left of the 'binary' point and 'r' bits to the right. If 'sgn_ext' is on then the MSB of the
   resulting truncated number is sign-extended.
int long bit_limit(
   int long 1, /* Bits left of the 'binary' point */
int long r, /* Bits right of the 'binary' point */
int long in_val /* Input Value */
   )
ł
   int long mask;
   /* Build a mask which has 1's where data is valid */ mask = (((int long)1 << (l+r)) - 1) << (PREC-r);
   /* Mask the input data */
   return mask & in_val;
ł
Function : main
   Sample code to display the effect of limited precision fixed-point
   binary arithmetic.
*****
int main(void)
   float a_fl, b_fl, e_fl;
int long A, B, C, D, E;
   /* Pick some arbitrary input values */
   a_fl = 201.8;
b_fl = 0.19;
  /* Convert a_fl and b_fl to justified integers and limit to 8 bits
  and 4 bits respectively */
A = bit_limit(8, 0, a_fl*(1<<PREC));
B = bit_limit(0, 4, b_fl*(1<<PREC));</pre>
   /* Each multiplication needs to be re-scaled */
C = bit_limit(8, 2, (A*B)>>PREC);
   /* Truncate D to 7 bits total */
   D = bit_limit(6, 1, A>>2);
   /* Truncate the output to 9 bits */
   E = bit_limit(8, 1, C+D);
   /* Re-scale to convert back to float */
   e fl = ((float)E)/(1 << PREC);
   /* Display output and full_precision output for comparison */
printf("e fl = %f\n", e fl);
   printf("e_fl(full_precision) = %f\n", a_fl/4 + a_fl*b_fl);
}
```

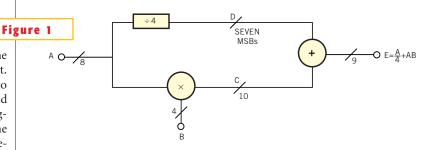


fied integers by scaling. The macro PREC sets the number of bits that the code uses to store the fractional part of the input, which are the bits to the right of the "binary" point. The bit_limit function truncates a_fl to 8 bits on the left of the binary point and to 0 bits on the right; the respective figures for b fl are 0 and 4 bits. Because the code stores the numbers as normal integers, the standard operators can perform addition and multiplication. However, the code must rescale the result of a multiplication because both operands are justified. The bus widths are set at points A, B, C, D and E; the code displays the bitlimited value of E and compares this value to the result from full-precision arithmetic.

You can handle signed arithmetic using 2's complement numbers by extending the bit_limit function to sign-extend the MSB after each truncation. You can perform rounding using the following statement:

bit_limit(8, 0, A + 0.5•(1<PREC)).

The number of bits in the "int long" data type on the simulation platform sets



A simple flow diagram implements the output E=A/4+A•B.

TABLE 1-TRUNCATION EFFECTS BASED ON BUS WIDTH

									Binary point				
Α	1	1	0	0	1	0	0	1	1	1	0	0	201
В	0	0	0	0	0	0	0	0	0	0	1	1	0.1875
C=AB	0	0	1	0	0	1	0	1	1	0	1	1	37.5
D	0	0	1	1	0	0	1	0	0	1	0	0	50
E=C+D	0	1	0	1	0	1	1	1	1	0	0	0	87.5

the major limitation of this technique. Normally, the number is 32 bits, so all numbers in the simulation, including the unscaled result of a multiplication, must be less than 2³¹. You can slightly extend this range by using "unsigned int," or you can double the range by using "int long long" when this type maps to 64 bits. **Listing 1** is available for downloading from *EDN*'s web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2328. (DI #2328)

> To Vote For This Design, Circle No. 360

Two ADC channels double sensor precision

Luke J Barker, Reinke Manufacturing Co Inc, Deshler, NE

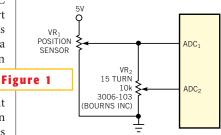
HE ACCURACY OF the onchip ADCs of numerous small and inexpensive 8bit μPs is well-suited for many applications. However, some situations benefit from just a

little more accuracy from a resistive position sensor, for example. The resistive circuit in **Figure 1** uses two ADC pins on a μ P to double the precision of a resistive position sensor. In effect, the 8-bit ADC becomes a 9-bit ADC. The resistive part of the circuit shown in **Figure 1** costs as little as \$3; the cost is higher if you use a precision potentiometer as the position sensor.

The concept behind using two \square ADC channels is simple. One ADC input takes direct measurements of the position sensor. The second ADC input measures the voltage out of a second potentiometer that is a $\frac{1}{2}$ bit behind the first input.

TABL	E	1-	AD	C	"P	HA	SI	NC] ″					
ADC ₁	0	1	1	2	2	3				253	254	254	255	255
ADC ₁	0	0	1	2	2	3				253	253	254	254	255
9-BIT Result	0	1	2	3	4	5	·	•	·	506	507	508	509	510

This scheme creates a "phasing" of the two analog-to-digital results (**Table 1**). Adding the two results produces a 9-bit answer that is limited to a value of 510.



Using two ADC pins on a μ P doubles the precision of a resistive position sensor.

To set up the circuit for operation, you will need to accurately measure V_{REF} , which is 5.000V in this case, and set ADC₁ (VR₁) to a known voltage, 3.000V in this case. Then,

adjust ADC_2 (VR₂) according to the following equation:

$$ADC_{2} = ADC_{1} - \frac{V_{REF}/255}{L 2 1}$$
$$= 3.000 - \frac{5/255}{L 2 1} = 2.990V.$$

Thus, an ADC₂=2.990V sets input-channel ADC₂ to a $^{1}/_{2}$ -bit lag. (DI #2332)

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design**ideas**

Transistor pair lowers PWM IC's start-up current

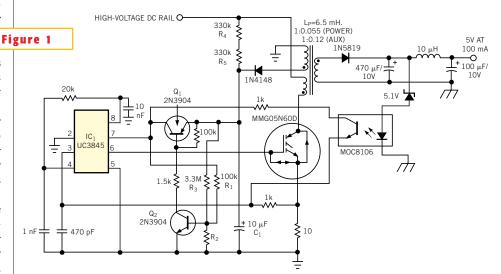
Christophe Basso, Motorola Semiconductor, Toulouse, France

N AUXILIARY WINDING usually provides power for the popular UC384X-based offline switch-mode power supplies (SMPSs). This winding feeds the main PWM controller during steady-state operation. However, the controller always needs a small start-up which current, clearly plagues the efficiency in very low-power standby SMPSs with P_{OUT}=500 mW, for example. Any wasted source power, such as for the startup network and controller supply, adds to the power drawn from the mains and significantly degrades the overall efficiency. Obtaining

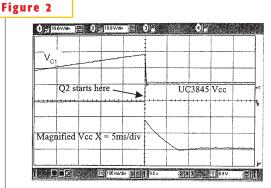
an acceptable efficiency at high line voltage represents a tough design task. Some tricks totally stop the start-up current by using a high-voltage bipolar or MOSFET (**Reference** 1). However, the addition of a high-voltage component burdens the bill-of-material cost of a small-power SMPS.

An alternative and inexpensive solution allows you to program the start-up current at any value, whatever the PWM IC (**Figure 1**). Implemented around two low-

voltage off-the-shelf bipolar transistors, Q_1 and Q_2 , the circuit brutally connects the controller to bulk capacitor C_1 when C_1 's voltage level is adequate. This level determines the C×V product that is large enough to feed the PWM IC until the steady-state operation takes over. The designer can then select any small startup current to charge the bulk capacitor in agreement with time-constant recommendations. During the charge, series pnp transistor Q_1 is locked off, which prevents any current consumption from the main controller. When the voltage reaches a defined level, Q_2 starts to pull



A pair of bipolar transistors, Q_1 and Q_2 , work with C_1 to turn any PWM controller into a low-current startup device.





 Q_1 's base to ground. Q_1 's collector voltage rises and further saturates Q_2 through the reaction resistor, R_1 . The charged bulk capacitor is now fully connected to the PWM IC, which starts to oscillate. A few cycles later, the auxiliary winding takes over, and Q_1 stays on.

The level $V_{\text{THRESHOLD}}$ at which Q_2 turns on is simply given by:

$$V_{BE}(Q_1) \bullet \frac{R_4 + R_5}{R_4}.$$

If you assume a linear charge from the start-up network, R_4+R_5 , then the time at

which Q_2 starts to conduct is equal to

$$\frac{C_1 \bullet V_{\text{THRESHOLD}}}{I_{\text{START-UP}}},$$

where

$$I_{\text{START-UP}} \approx \frac{\text{VDC}}{\text{R}_4 + \text{R}_5}$$

With the values in Figure 1, C₁ connects to the IC when its voltage reaches 17V, which occurs in less than 350 msec at VDC=350V. The circuit offers better than 50% efficiency at high-line (250VAC), drawing less than 1W for a 500-mW output power. The MMG-05N60D insulated-gate bipolar transistor (Motorola Semiconductor, http:// mot-sps.com/scg/) also contributes to the circuit's performance because of its low capacitive parasitic elements, including a 5-nC gate charge. The circuit thus minimizes commutation losses. Figure 2 shows the start-up phase of the low-power SMPS at very low line, 70V ac. (DI #2330)

Reference

1. Basso, Christophe, 'Low-cost MOS-FET quashes power resistor', *EDN*, June 9, 1994, pg 140.

> To Vote For This Design, Circle No. 362



Autozero a position-sensing detector

James Zannis, Renishaw SA, Champs-sur-Marne, France

UTOZEROING SCHEMES CAN BE NEC-ESSARY to minimize the input-offset voltages of position-sensing detectors (PSDs), particularly when you use these detectors with high dc gain. PSDs are useful optical transducers for accurately measuring displacement. In practice, their typical configuration is as a differential current-to-voltage circuit (Figure 1). The ratio of the photocurrents I,-to-I, linearly divides between the electrodes, proportional to the incident light beam. The magnitude of the photocurrents is a function of the light intensity.

Although PSDS are photodetectors, using them with high dc gain can quickly get you into trouble. Input-offset voltages can easily multiply due to the relatively low sheet resistance between pins 1 and 2, which typically ranges from 5 to 100 k Ω . Consider the following nodal equations:

$$V_{OUTB} = I_2 \cdot R_F +$$

$$\overset{\emptyset}{\underset{o}{\oplus}} - V_{OSA} \cdot \frac{R_F}{R_S} + V_{OSB} \cdot \frac{(R_S + R_F) \varnothing}{R_S} \overset{\emptyset}{\underset{fs}{\oplus}}$$

$$V_{OUTA} = I_1 \cdot R_F +$$

$$\overset{\emptyset}{\underset{c}{\oplus}} - V_{OSB} \cdot \frac{R_F}{R_S} + V_{OSA} \cdot \frac{(R_S + R_F) \varnothing}{R_S} \overset{\emptyset}{\underset{fs}{\oplus}}$$

An offset multiplication occurs because of the low intrinsic diode impedance, Re, of the PSD, and the high values of R_{r} . For normal photodetectors, R_s is very high, and, therefore, no multiplication occurs. FET-input op amps are usually the choice for photodetector circuits because they have a higher input impedance and lower current-noise density at high-impedance levels than their bipolar counterparts.

For a typical pair of FET op amps mismatched by ± 3 mV and with an R_E of 1 M Ω and sheet resistance of 20 k Ω , V_{OUTB} would be -0.303V, and V_{OUTA} would be 0.303V. For a theoretical pair of op amps mismatched by $\pm 10 \mu$ V, an R_E of 1 M Ω , and a sheet resistance of 20 k $\Omega,\,V_{_{OUTB}}$ would be -0.001V and V_{OUTA} would be 0.001V. Ultimately, it would be nice to use a low-noise, low-bias-current amplifier with a very closely matched front end. However, it is a much more difficult process to match the input FET differential pair than that of a bipolar transistor. Nevertheless, this circuit shortcoming due to the sheet resistance is also the key to its success; you can force the offset voltage to be equal.

You can accomplish this goal by sam-

pling and integrating the difference of the two input-offset voltages and forcing the positive input of Amplifier A with the result (Figure 2). The two amplifier outputs converge to the input offset voltage of Amplifier B with the difference in the two output voltages equal to the offset of amplifier C. V_{OUTA} reduces to

$$V_{OUTA} = I_1 \cdot R_F + V_{OSB} + V_{OSC}$$

and V_{OUTB} reduces to

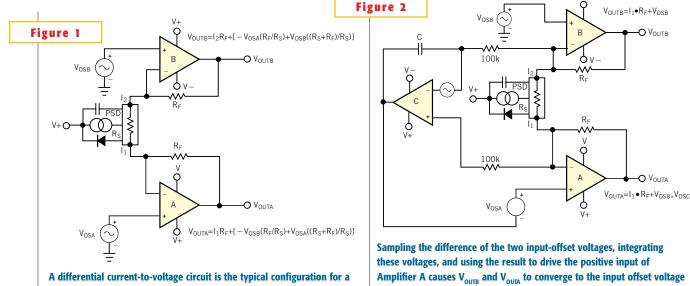
$$V_{OUTB} = I_1 \bullet R_F + V_{OSB}.$$

Note that biasing the wrong op amp causes the two outputs to diverge, and you must choose an op amp for Amplifier C on the merits of its dc specifications.

The second approach to forcing the offset voltage to be equal is to use a potentiometer to adjust one of the op amps at its offset-adjustment pins. This circuit converges or diverges in a manner similar to that depicted in Figure 2. (DI #2331)

> To Vote For This Design, CIRCLE NO. 363

> > V4



A differential current-to-voltage circuit is the typical configuration for a position-sensing detector (PSD).



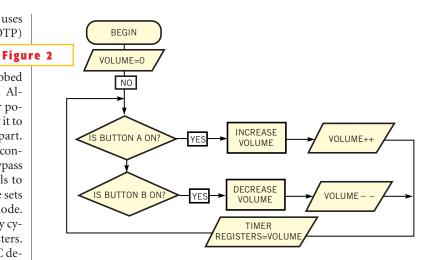


OTP μC controls Boomer amplifier

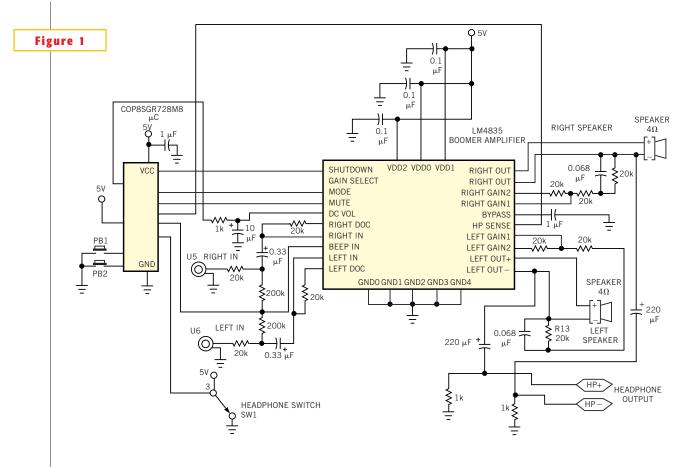
Wallace Ly, National Semiconductor Corp, Santa Clara, CA

IGURE 1 SHOWS A CIRCUIT that uses a one-time-programmable (OTP) μ C in an unusual way. A COP8SGR7 µC uses digital signals to "bit-bang" an LM4835 (dubbed "Boomer" by National) amplifier. Although the amplifier is designed for potentiometer control, you can modify it to make it a fully digitally controlled part. Figure 2 shows the flow chart for the control process. A PWM signal and a lowpass filter allow you to use digital signals to control the amplifier. The technique sets the μ C in processor-independent mode. You load the values affecting the duty cycle into the appropriate timer registers. When a control bit goes high, the µC delivers a PWM signal.

The PWM signal goes to a first-order lowpass filter. The output from the filter



Depressing the volume-control pushbuttons sets the duty cycle of the PWM signal the COP8SGR7 μC generates.



Instead of tweaking potentiometers, you can use pushbuttons and a µC to control National's Boomer amplifier IC.

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is a dc voltage, whose amplitude is proportional to the duty cycle of the PWM signal. The processor-independent mode allows the μ C to perform other duties and calculations while it generates the PWM signals. With the COP8SGR7 μ C, three PWM outputs are available; therefore, the μ C can control three amplifiers, or six channels of audio. The μ C debounces the two (volume-up and -down) pushbuttons. The controller also handles the mute, shutdown, beep, volume, and headphone functions. You can download the C code for controlling the μ C from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the files from DI-SIG, #2326. (DI #2326).

> To Vote For This Design, Circle No. 364

LED driver displays standing-wave ratio

Richard Panosh, Vista, Bolingbrook, IL

HE CIRCUIT IN Figure 1 uses an LM3914 LED driver to directly display standing-wave ratio (SWR) in a low-cost, rugged instrument. The SWR-sensing head is derived from the ARRL Antenna Handbook in an article that describes the tandem match. The forward voltage and reflected voltage $(V_{F}+V_{R})$ signal drives Pin 6 (R_{HI}) , and the $V_{F} - V_{R}$ signal drives the normal signal input at Pin 5. You can use this basic arrangement to display the ratio of two voltages in other applications. The internal circuit of the LM3914 comprises 10 voltage comparators that compare the input voltage at Pin 5 to an internal, 10step, linear-voltage-divider string between Pin 6 (R_{HI}) and Pin 4 (R_{LO}). The voltage-divider levels, V_N, are $V_N = V_{REF} \times n/10$, where n is the voltage-divider step from 1 to 10, and V_{REF} is the voltage between pins 6 and 4.

When the signal voltage on Pin 5 satisfies the equality in the following equation, the nth LED energizes in the dotmode display (with approximately 1 mV of hysteresis).

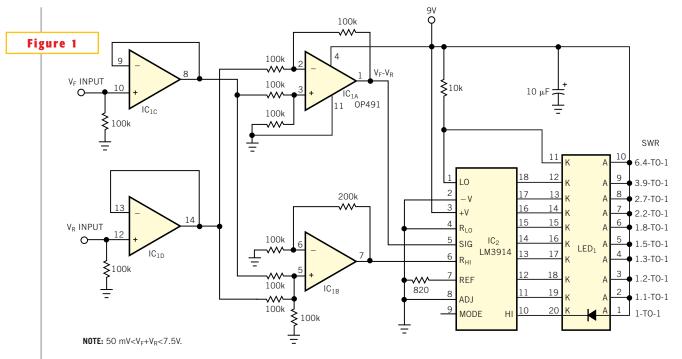
$$\frac{N}{10} \cdot V_{REF} \notin V_{PIN5} < \frac{N+1}{10} \cdot V_{REF}.$$

If you force V_{REF} to equal $V_F + V_R$ and the voltage at Pin 5 to equal $V_F - V_r$, you can arrange the terms as in the following equation.

 $\frac{10}{N} \ddagger \frac{V_{\rm F} + V_{\rm R}}{V_{\rm F} - V_{\rm R}} = \frac{V_{\rm REF}}{V_{\rm PIN5}} > \frac{10}{N+1},$

where $V_F + V_R V_F - V_R$ is the definition of the SWR. Two sections of the quad op amp, IC₁, buffer the forward and reverse voltages developed in the SWR bridge. The remaining two sections serve as a difference amplifier to produce the voltage $V_F - V_R$ and as a noninverting summing amplifier to produce the voltage $V_F + V_R$. Even though the circuit does not use the internal voltage regulator, you must properly terminate it to establish the LED current. (DI #2324).

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You can use an LED-driver IC to produce a thermometer-type indicator for the standing-wave ratio in RF systems.

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Comparator provides stable hysteresis

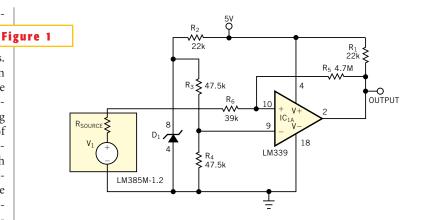
Fernando Garcia, Lucent Technologies, Brownsville, TX

NLESS A VOLTAGE-COMPARATOR CIR-CUIT is sampling an extremely clean signal, the comparator always requires some hysteresis. Traditional comparator circuits obtain the required hysteresis by using positive feedback derived from the ratio of two resistors. The voltage at the noninverting input is the superposition of a fraction of the input and output voltages, each divided by its respective resistor ratio. With an inverting comparator, the noninverting input usually connects to a voltage reference with reasonably low impedance, and you can choose the hysteresissetting resistors without concern for loading. However, for the noninverting comparator, the input voltage comes from the actual source the circuit is sampling. This source has a series impedance,

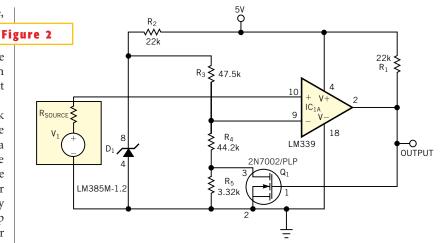
(**Figure 1**). This impedance may not be repeatable or may change value with changing circuit conditions; therefore, it may result in hysteresis errors.

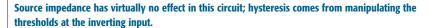
Although you can change the feedback and input resistor values to minimize the source-impedance impact, you face a practical limit on the increases, because the value of the feedback resistor that the resistor requires to maintain the proper resistor ratios can become excessively high. Traditionally, you could use an op amp configured for unity gain to buffer the high-impedance source from the comparator. However, in some applications, cost, board-area, or current-consumption constraints may preclude adding an op amp. The circuit variant in Figure 2 eliminates the source-impedance problem. The voltage source under comparison connects directly to the noninverting input. Hysteresis does not come from resistor feedback, but rather from MOSFET Q₁. If the voltage you are sampling is less than the threshold, the comparator's output is low, and Q₁ turns off.

The comparator's inverting input essentially sees a reference voltage identical to the reference voltage in **Figure 1**.









However, when the voltage exceeds the threshold, the comparator's output goes high, turning on Q_1 . The MOSFET shorts out the lower portion (R_5) of the resistor divider. This action has the net effect of lowering the reference voltage to the comparator's inverting input. The differential voltage thus increases, providing the required hysteresis. The source impedance basically sees only the comparator's input impedance. This impedance is extremely high, so the source-impedance

impact on offset is low. Most small-signal MOSFETs can work in this application, provided that the $R_{DS(ON)}$ is at least one order but preferably two orders of magnitude lower than the resistor it must shunt. This application requires a logic-level FET that turns completely on with V_{CS} =5V. (DI #2335).

To Vote For This Design, Circle No. 366



Edited by Bill Travis and Anne Watson Swager

Shift register makes a fast counter

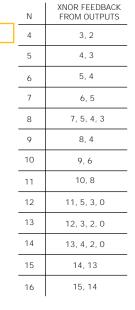
Yoram Stern, ECI Telecom, Petach-Tikva, Israel

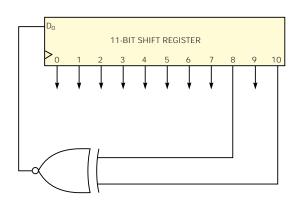
SIC designs commonly require a fast, syn-**Figure 1** chronous counter. The carry propagation is the limiting factor in a fast-counter implementation. In a binary synchronous counter, a logic function of the value of all the bits in the counter determines the value of the most significant bit in the next clock edge. When the counter is long and its frequency is high, this function evaluation can take longer than one clock cycle.

One of the methods you can use to overcome this difficulty is a linear-feedback shift-register (LFSR) technique. You can build an LFSR with an N-bit shift register with XNOR or XOR feedback from the last output, Q_N , to the serial input D_1 (**Figure 1**). An LFSR of N bits counts to 2^N-1 ; a binary counter counts to 2^N .

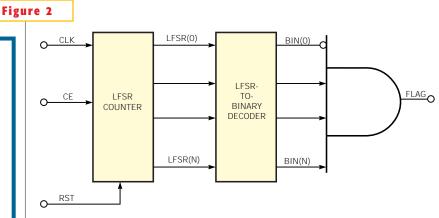
An LFSR has several advan-

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NOTE: WHEN N=4, THE COUNTER ASSERTS THE FLAG SIGNAL IN THE 14TH CLOCK (BIN="1110").

Adding a decoder after the LFSR translates the LFSR'S pseudorandom count to a regular binary count.

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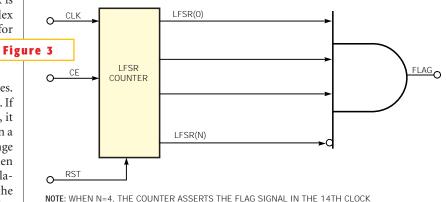
tages over a binary counter: An LFSR is much faster because the most complex logic function that needs evaluation for the next state is a four-input XOR, and LFSR logic is smaller than binary-counter logic.

An LFSR also has some disadvantages. The count of the LFSR is not intuitive. If you need a control in the 16th count, it is more intuitive to look for "10000" in a binary counter than to look for a strange "11101" in an LFSR. Furthermore, when you watch the waves on a logic simulator, you feel more relaxed when the counter is incrementing in a binary intuitive manner than a strange LFSR jump.

To overcome this disadvantage, you can use a decoder following the LFSR, which translates the LFSR pseudorandom counter to a regular binary count (Figure 2). A C program consists of VHDL code that implements the LFSRto-binary decoder (Listing 1). (You can download the program from EDN's Web site, www.ednmag.com. At the registereduser area, go into the Software Center to download the file from DI-SIG, #2345.) The additional logic for the decoder is no burden, because any logic-synthesis tool eliminates it. The silicon implementation consists of the LFSR followed by a somewhat-bizarre combination of AND gates and inverters (Figure 3).

Counters often divide fast clocks to make slower clocks or clock enables. Such clock dividers usually require a counter with a binary count because it is necessary to divide the clock by powers of 2. LFSRs are unsuitable for this application because they count by $2^{N}-1$. To circumvent this disadvantage, shorten the count sequence to get the desired modulus by synchronously resetting the LFSR counter after decoding the appropriate count. Although this scheme sacrifices the speed of the LFSR, an LFSR is still much faster than a regular binary counter.(DI #2345)

> To Vote For This Design, Circle No. 313



VOTE: WHEN N=4, THE COUNTER ASSERTS THE FLAG SIGNAL IN THE 14TH CLOCK (BIN="1110," LFSR="1000").

After logic synthesis, the decoder that follows the LFSR consists of a rather bizarre combination of AND gates and inverters.

LISTING 1–LFSR-TO-BINARY-DECODER C PROGRAM #include <stdio.h> #include <math.h> #define xnor(A, B) ((A) != (B) ? (0) : (1)) // N is the number of bits in the counter #define N 5 /********************* * main program main() short int cs_lfsr[N], ns_lfsr[N]; int cnt = 0int i, max count; max_count = (int) pow(2,N) - 2; for (i = 1; i <= N; i++) cs_lfsr[i] = 0; printf("\n case (lfsr_cnt) is"); for (cnt = 0; cnt <= max_count; cnt++) { printf ("\n when \""); for (i = 1; i <= N; i++) printf ("%d",cs_lfsr[i]); printf ("\" => cnt <= CONV_STD_LOGIC_VECTOR\(%d\, %d);", cnt, N); // calculate ns lfsr for (i = 1; i <= N; i++) switch (i) { case 1 : ns_lfsr[1] = xnor(cs_lfsr[3], cs_lfsr[5]); break default : ns_lfsr[i] = cs_lfsr[i-1]; break: 3 } // move ns_lfsr to cs_lfsr for (i = 1; i <= N; i++) cs_lfsr[i] = ns_lfsr[i]; 3 printf("\n end case;\n");

designideas

RS-232C monitor operates without a power supply

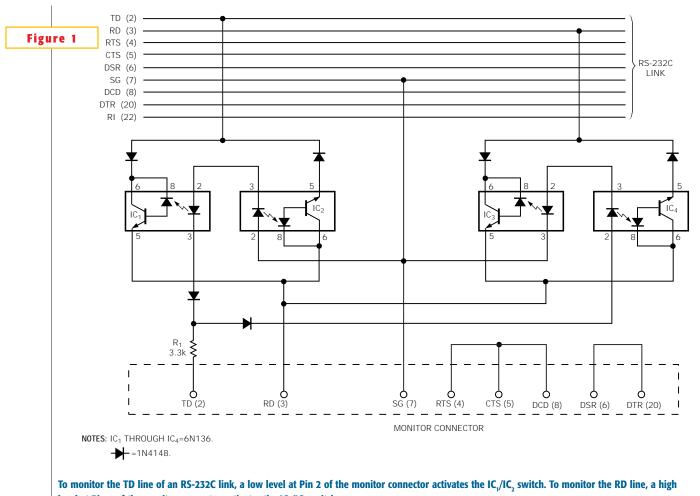
Michele Frantisek, Brno, Czech Republic

URING DEVELOPMENT WORK, YOU can use a simple circuit to monitor RS-232C receiving and transmitting data (Figure 1). The circuit consists of two bidirectional switches that each contain two antiparallel-connected optical couplers and two diodes that distribute the signal with the correct polarity to the optocouplers. The IC₁/IC₂ switch connects to the TD line of the RS-232C link, and the IC₂/IC₄ switch connects to the RD line of the link. A negative voltage or low logic level at Pin 2 of the monitor connector activates the first switch. In this case, the circuit monitors the data at the TD line. A positive voltage or high logic level at Pin 2 of the monitor connector activates the other switch to monitor the RD line. The serial connection of the optocoupler LEDs in both switches reduces the current that the circuit draws from Pin 2 of the monitor connector. R_1 limits this current to approximately 2 mA, so this circuit needs no power supply to monitor an RS-232C link.

The monitor-connector configuration is equivalent to a null modem. You can attach a μ P, for example, to monitor either the TD or the RD line of the link when the monitor device's baud rate is the same as this link. Full-duplex communication allows the circuit to monitor both TD and RD lines when the baud rate of the monitor device is greater than or equal to double the RS-232C link's baud rate.

The 6N136 optocoupler has good parameters, especially high speed and low drive current, for this circuit. Many other types of optocouplers require a lower value for R_1 , which places a greater load on the TD line of the monitor device and may cause the circuit to stop monitoring. (DI #2343)

To Vote For This Design, Circle No. 314



level at Pin 2 of the monitor connector activates the IC_3/IC_4 switch.

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Simple circuits control RC servos

Larry Korba, National Research Council, Ottawa, ON, Canada

D EVELOPERS OF ROBOTIC DEVICES sometimes need to actuate rotational elements between two positions over a range of several tens of degrees. Such motion control is particularly useful for opening doors, actuating valves, or controlling the movement of small robotic arms or legs. Two alternatives to produce this type of actuation are a solenoid and a motor attached to a gear

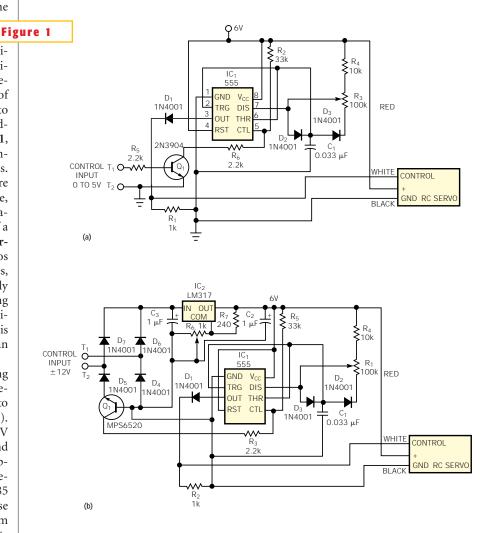
train. Solenoids require careful mechanical design to effect the conversion from linear

to rotational motion and to achieve consistent position control between two positions. Motor-based systems require careful positioning of limit switches. An alternative to these two approaches, embodied in the circuits of Figure 1, involves the use of radio-control (RC) servomechanisms. Common RC servo devices are available in a variety of size, speed, and torque specifications. The range of motion of a typical RC servo is 190 (Reference 1). Because these servos must fit into RC cars, airplanes, and boats, they are usually small-especially considering their torque. The angular position of the servomotor shaft is related to the pulse width of an input control signal.

A technique for controlling the output of an RC servo between two positions uses a 0 to 5V digital signal (**Figure 1a**). The circuit requires a 5 to 6V power source. D_2 , D_3 , R_3 , R_4 , and C_1 configure the 555 IC to operate in astable mode at a frequency of approximately 285 kHz. R_3 controls the pulse width of the output data stream over 0.3 to 2.5 msec. This setting sets the maximum counterclockwise position of the servomotor with the control input set at 0V. When the control input is at 5V, the output pulse train contains a 75- μ sec pulse. This pulse sets the servomotor at its most clockwise position. To calibrate the servo using the circuit in **Figure 1a**, you first set the control input at 5V. With this input, the shaft of the servo reaches its maximum clockwise position (which the ratio of R₂ to R₂+R₆ controls). With the

control input set at 0V, R₃ controls the rotational limit of the actuated assembly in the counterclockwise direction.

The circuit in **Figure 1b** controls the movement of an RC servo between two preset positions, using an input signal of +12 to -12V. In this case, the input control signal supplies the current that the servo and control circuit require. The bridge rectifier comprising D₁ to D₄ and



Simple circuitry uses pulse-width modulation to control an RC servomotor, using a 0 or 5V control signal (a); a self-powered version (b) uses a ±12V control input.



the base-emitter junction of Q_1 , with the aid of some filtering by C_3 , provides the input voltage for the three-terminal regulator, IC_2 . R_6 and R_7 bias the regulator to produce a 6V output, which the servomotor requires. Transistor Q_1 produces a signal of 0 or 5V, depending on the polarity of the input voltage. The circuit in **Figure 1b** supports the entry of the Carleton School Board of Ottawa (**Reference 2**) in the 1996 Canada First Robotics Competition (**Reference 3**), in which competitors developed a remotely controlled robot that plays a specialized game of basketball. The receiver unit provides control servomotors in the robot with several bipolar outputs.(DI #2338).

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Wellesley, MA, 1993.

2. Carlton School Board Warriors Web site, www.warriors.ottawa.com.

3. Canada First Web site, www. candafirst.org.

To Vote For This Design, Circle No. 315

One amplifier makes one-shot

W Dijkstra, Waalre, The Netherlands

SIMPLE CIRCUIT (Figure 1a) turns an amplifier into a one-shot. At power-on, assume that the output voltage of IC_1 is high. Then, the voltage across C_1 increases until it is greater than the voltage at the positive input of IC_1 . At this point, the output of IC_1 goes low.

A short input pulse forces the output of IC_1 to a high of 4.6V, and C_1 begins to charge. The positive input of IC_1 near the switching low of IC_1 is equal to

$$\frac{R_1}{R_1 + R_2} \cdot 4.5 = 4.1V.$$

The compliance dV_1 of the voltage across C_1 is 4.1–0.5=3.6V. The compliance of the output voltage of IC_1 (dV_2) is 4.6–0.5=4.1V.

You can transform the formula

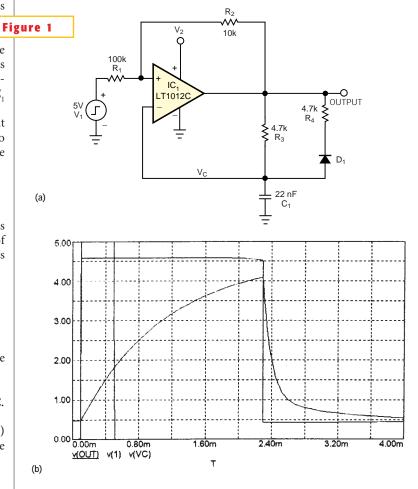
$$dV_1 = dV_2 \quad 1 - e^{\frac{-t}{R_3 \cdot C_1}}.$$

to the formula for the duration of the output pulse:

$$t = -R_3 \bullet C_1 \bullet \ln_{\pounds} 1 - \frac{dV_1}{dV_2 \ddagger} = 2.17 \text{ mSEC}$$

Spice analysis of the circuit (**Figure 1b**) shows accurate results. R_4 and D_1 ensure rapid discharging of C_1 . (DI #2333)

To Vote For This Design, Circle No. 316



A short input pulse forces of the output of IC_1 high and begins charging C_1 (a). The output goes low when V_c exceeds the voltage at the amplifier's positive input (b).

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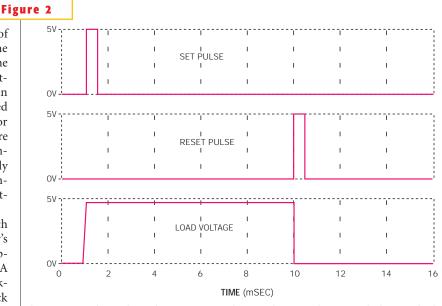


High-power latch provides 48V, 10A

Ahmed Aboyoussef, Lucent Technologies, Holmdel, NJ

ODERN CENTRAL-OFFICE telecommunications equipment has stringent reliability requirements: a bit-error rate of 10⁻¹² or better. The performance of the power supply is a significant factor in the quality of transmission. The supply voltage, which is nominally 48V but can reach 60V, must be within a designated range. It is standard practice to monitor the condition of the line voltage before applying power to the load. If the condition is satisfactory, you may apply power to the load via a switch. The highpower latching circuit in Figure 1 is suitable for such applications.

The circuit sets and resets the latch with 5V pulses. International Rectifier's (www.irf.com) IRF5210 series-pass, pchannel MOSFET (Q₃) can deliver 40A and specifies a 100V drain-source breakdown voltage. The circuit uses feedback to keep Q₂ on after setting the latch. International Rectifier bases the design on MicroSim's (www.orcad.com) PSpice; Figure 2 shows the simulation results. The circuit applies a set pulse to the gate of an IRFL4310 MOSFET (Q₁) via the R_1C_1 lowpass filter. The R_1C_1 and R_8C_2 lowpass filters provide immunity to EMI noise, which without filtering could set or reset the latch. The IRFL4310 is an nchannel, surface-mount SOT-223 MOS-FET with 100V drain-source breakdown

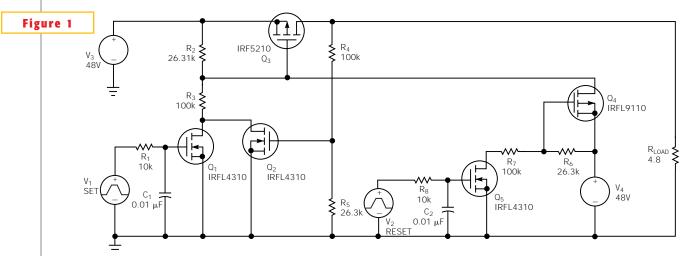


This PSpice simulation shows that narrow set and reset pulses control Figure 1's high-power latch.

voltage. With Q_1 turned on, Q_3 switches on, applying the 48V line voltage to the load.

 R_4 and R_5 provide the gate-source bias voltage to turn Q_2 on, thereby keeping Q_3 on after termination of the set pulse. A 5V pulse is applied to the gate of Q_5 via the R_8C_2 filter; this action resets the latch. Activating Q_5 enables the IRFL9110 p-channel MOSFET (Q_4) to apply 48V to the gate of Q_3 , thereby disabling Q_3 . The circuit's topology requires little pc-board real estate and takes advantage of the high drain-source breakdown voltages available in surface-mount, SOT-223 MOS-FETs. (DI #2337).

To Vote For This Design, Circle No. 317



You set and reset this compact, surface-mount high-power latch circuit by applying 5V pulses to logic-level MOSFETs.

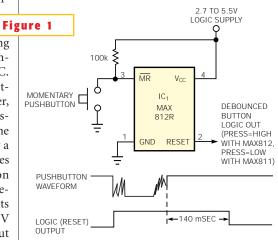
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Tiny IC debounces pushbutton switch

Len Sherman, Maxim Integrated Products, Sunnyvale, CA

HOUGH THEY'RE NOT complicated, schemes for debouncing a pushbutton switch usually entail using several logic gates. It's easy to include such circuits in an ASIC. Adding a debouncer as a lastminute design change, however, can be inconvenient. In such cases, the circuit in Figure 1 can come in handy. The circuit, using only a four-pin SO-package IC, squares up and debounces a pushbutton signal. IC, is a reset chip with a Reset output that goes high when its supply voltage drops below 2.65V or when its manual-reset input (\overline{MR}) goes low. \overline{MR} usually connects to a system-reset input, and Reset connects to a μ C, but the connections shown enable the de-



Using almost no real estate, this circuit squares up and debounces a pushbutton signal and extends it to at least 140 msec. vice to debounce any signal.

The internal one-shot provides an instant response to the first falling edge on the input and then delays any further response until 140 msec after the last rising edge. The MAX812 shown inverts the pushbutton input; a similar device (MAX811) is noninverting. The ICs also incorporate a power-on reset function that asserts the reset output when V_{cc} falls below a preset threshold and also asserts the output for 140 msec after each application of power. Selecting an R-suffix part sets this threshold at its lowest value (2.63V), preventing false outputs in the debouncer except when the supply voltage fails. (DI #2340).

> To Vote For This Design, Circle No. 318

Back-to-back FETs thwart reverse current

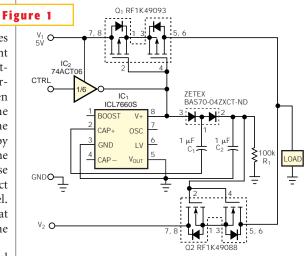
Randy Moore, Harris Semiconductor, Costa Mesa, CA

T IS SOMETIMES DESIRABLE to switch a load between power sources using MOSFETs. Problems can arise when the chosen source voltage is approximately 0.6V higher than the volt-

age of the other source. At that point, the body diode, normally reverse-biased, becomes forward-biased and allows current flow into the source of lower voltage. The MOSFET with the forward-biased body diode can then become a cosupplier, if not the only supplier, of current to the load. You can solve the problem by adding a second MOSFET of the same channel type in the reverse direction (Figure 1). You connect the MOSFETs' gates in parallel. The trade-off in the scheme is that $R_{DS(ON)}$ is twice as high as in the single-MOSFET connection.

The circuit contains two dual MOSFETs, one n-channel pair and one p-channel pair, both of

which are logic-level devices. The pchannel FETs turn on with logic 0 $(V_{GS} \approx -5V)$ on their gates. This action also starves the ICL7660S for power, be-



Adding two MOSFETs in a load/power switch eliminates reversecurrent flow between the two power supplies.

cause the IC's logic output is approximately 0V to the n-channel MOSFETs' gates. The n-channel MOSFETs, therefore, are off. Conversely, applying a logic

> 1 (5V) to the p-channel MOS-FETs' gates, the FETs turn off, because V_{GS} is approximately 0V. The ICL7660S voltage doubler now receives power and acts as a high-side driver for the n-channel MOSFETs. The 74ACT06 is more than capable of supplying the necessary current for the ICL7660S, which consumes approximately 160 μ A while providing the gate drive for the n-channel MOS-FETs. (DI #2341).

To Vote For This Design, Circle No. 319

design**ideas**

Edited by Bill Travis and Anne Watson Swager

NCO technique helps µC produce clean analog signals

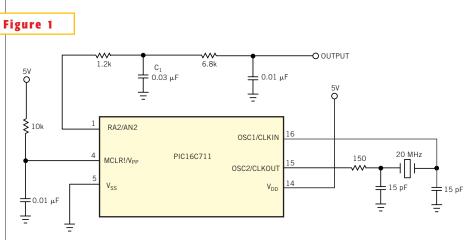
Steve Ploss, Veridian Corp, Wright Patterson AFB, OH

RECENT DESIGN IDEA described a method for producing an analog voltage from one digital output of a μ C ("Generate an analog signal with a µC," EDN, Oct 22, 1998, pg 108). The method involves generating a PWM output with a controlled duty cycle and filtering the switching waveform with a simple single-pole RC filter. Although this method provides an accurate dc output with 8 bits of resolution, it requires a filter with a low cutoff frequency to reduce the ripple to less than 1 LSB.

An alternative method doesn't have this problem. The circuit in **Figure 1** and the corresponding control program borrow a technique from direct digital synthesizers. The technique consists of a

numerically controlled oscillator (NCO) that distributes the duty cycle as evenly as possible across the main period of the output, which is 256 clocks for both the NCO and PWM approaches. **Figure 2a** and **Figure 2b** illustrate the operation of

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A numerically-controlled-oscillator (NCO) technique allows a μ C and a handful of passive components to output analog signals that, after filtering, have a ripple amplitude that is constant over changes in duty cycle.

the NCO and the PWM methods, respectively, with the duty cycle set to 10/256. **Figure 2a**'s NCO digital output has the same duty cycle as **Figure 2b**'s PWM output but distributes the duty cycle evenly across the period.

The benefit of the NCO is that the ripple amplitude after filtering is almost constant with changes in the duty cycle. In contrast, the PWM method has a ripple amplitude equal to that of the NCO approach at the lowest duty cycle, and the ripple worsens at midscale.

Figure 3 compares the expected output for each of the two methods using the same duty cycle as before, 10/256. A simple IIR filter that simulates a single-pole RC low-pass filter, performed the filtering. The time constant for this filter is 256

clocks. This **figure** shows that the NCO output has much lower ripple than the PWM output at this output duty cycle (**Figure 3a**). As the DAC value approaches midscale, which corresponds to a duty cycle of approximately 128/256, the PWM ripple gets progressively worse, but the NCO ripple improves by as much as a factor of 2 (**Figure 3b**).

The accompanying listing to **Figure 1** runs on the PIC16C711, but, because the routine doesn't use the ADC and the TMR0 interrupts, you can use it with other processor types. (You can download the program from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the file from DI-SIG, #2346.)

The DAC routine uses only two regis-

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55

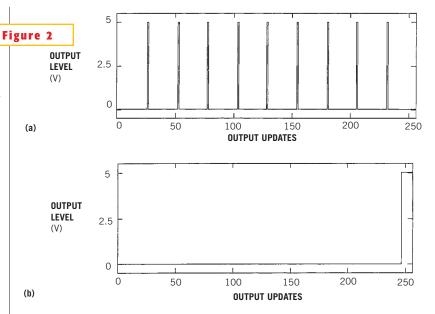


ters; the phase accumulator and the holding register form the DAC input value. Two additional registers provide sine-wave values to the DAC routine. On initialization, the phase accumulator sets to zero, and the DAC value sets to midscale (0x80). On each update, the value of the DAC register adds to the phase accumulator. When the phase accumulator rolls over-an event signaled by the setting of the carry bit-the circuit sets the output high for one update. The process then continues indefinitely. To generate a sine wave, the program counts the number of times it loops and every 32nd time it retrieves the next value from the lookup table. The table holds 16 values of a full cycle, so the period of the sine wave is 512 times the loop time, plus a small amount of time for the branch out of the loop. With a 20-MHz crystal, the loop time is approximately 3.5 µsec, and the sine-wave frequency is approximately 625 Hz.

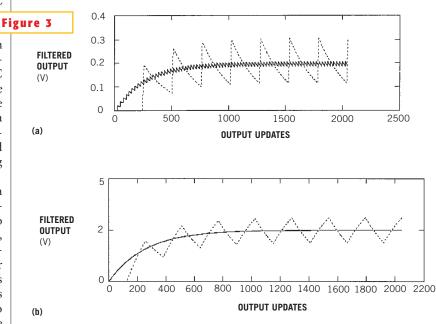
To output an analog waveform, you need only to change the value of the DAC

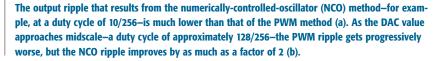
register. This change can happen at any time. The analog output almost immediately starts updating. When you use this method for your own application, remember to update the DAC output as often as possible to lower the ripple amplitude. The rate need not be precise, because you are merely setting a duty cycle—the period of which is relatively unimportant. More likely, you need to control the period of your analog waveform.

If you can afford to use a μ C with a timer interrupt, it's best to use that interrupt to determine when to change to the next DAC value. The rest of the time, you can continuously update the output. If you don't want to use the timer interrupt, you can update the DAC as part of a polling loop, as shown in this example, waiting for a loop counter to reach a predetermined value before changing the DAC value. However, you may want to make sure that the branch from the polling loop always takes the same amount of time, so that the DACvalue changes occur at a constant rate. Also, if the branch is going to take a comparatively long time, consider setting the output bit to a high-impedance state for the duration of the branch. If



The NCO digital output (a) has the same duty cycle as the PWM output (b) but distributes the duty cycle evenly across the period.





you do not take this precaution, the output will hold the last value—whether high or low—for the duration of the branch and could produce a transient on the filter output. (DI #2346)

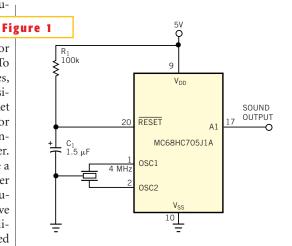
To Vote For This Design, Circle No. 402



μC generates musical sounds

Abel Raynus, Armatron International, Melrose, MA

ANY MODERN DEVICES SEND audible signals to their operators to indicate some of the predetermined conditions or states of the system under control. To avoid annoving human sensibilities, these sounds should match the musical scale. Several chips on the market provide such sound capabilities; for example, a programmable sound generator or an ISD1016 voice messager. The circuit in Figure 1 does not use a dedicated sound generator but rather generates sounds using software routines. The circuit uses an inexpensive MC68H705J1A µC and saves additional expense by eliminating the need for a sound chip. In Figure 2a, a note represents the pitch of each musical



An inexpensive μ C can provide programmable sound output without the need for expensive sound chips.

tone; **Figure 2b** shows the duration of the tone.

The first step in programming a sound-output system is choosing the type of sound signal: individual sounds or a section of a melody. As an example, consider a portion of the song Jingle Bells. Write the sequences of pitches and durations into the tables of Figure 2 and then put them into memory in addresses aMEL and aDUR (Listing 1). The addresses of these tables occupy the end of the available EPROM space. The commentaries in Listing 1 explain the structure of the subroutine MELODY. The std-jia.asm file is

Figure 2	F G												
	F E D C B A G F C C						0		0		0		
	G F C D	-0-	0		0								
	NOTE	С	D	E	F	G	A	В	С	D	E	F	G
		DO	RE	MI	FA	SOL	LA	TI	D01	RE1	MI1	FA1	SOL1
	f, Hz	264	297	330	352	396	440	495	528	594	660	704	792
	T, mSEC	3.78	3.36	3.04	2.84	2.51	2.3	2.0	1.9	1.68	1.5	1.4	1.26
	1/2T, mSEC	1.89	1.68	1.52	1.42	1.26	1.14	1.01	0.94	0.84	0.76	0.71	0.63
	NUMBER TO PUT INTO NR	189	168	152	142	126	114	101	94	84	76	71	63
	(a)												
										٦			
	NOTE SHAPE						Þ		Þ				
								_		-			
	DURATION	WHO	DLE	HALF	QUAR	FER	EIGHTH	16	БТН				
	PUT INTO DR	16	5	8	4		2		1				
	(b)									-			

A musical passage consists of pitches (a) and durations of the notes (b); you enter these values into the µ.C's pitch and duration registers.

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the standard address list of the registers and the bytes of the μ C. You can download **Listing 1** and its associated files from *EDN*'s Web site, www.ednmag.com. At the registered-user area, go into the Software Center to download the files from DI-SIG, #2336. (DI #2336).

To Vote For This Design, Circle No. 403

LISTING 1–ROUTINE FOR GENERATING MUSICAL SOUND

***		AL SOUND GE	****		rts		;end Melody Subroutine
*NOLIS				m3	incx		;go to next note
		l-jla.asm"		******	bra	m1	*****
\$INCLO. *LIST	Se StC	, j.a.asm"			*****		
*L/O P	0275			note	bset		;start a note
snd	equ	pA1			ldx	NR DI VO1	
* CONS		Fart			jsr	DLY01x	
do	equ	189T			belr	snd,prtA	
re	edn	168T			ldx	NR DLY01x	
mi	equ	1521			jsr		
m⊥ fa	equ	1421			lda	NDR	
sol	equ	126T			beq	n0 NDR	
N	equ	26T	;number of notes in the melody		dec		
ND	equ	100T	;number of each note repetition	- 0	bra	note	
aDUR	equ	ROMend-N	pitch duration table address	nO	rts		;end a note
aDUR aMEL	equ		; note pitch table address	.page		#0	
*VARIA			Prove care and cos	DLY01x	lda	#2	;delay 0.01X ms
V DALLER	ORG	RAM		rep0	decA		
NR	rmb		;note pitch register		bne	rep0	
DR	rmb		;pitch duration register		decx	DT V01	
NDR	rmb		;note duration register		bne	DLY01x	
nenx	rmb	1	,	******	rts		*****
mem1	rmb	1				#10T	
	ALIZATI			dly1s	lda	#10T mem1	;delay 1 sec
	ORG	MOR		1-1	sta		
	fcb		resistor ocs	lpl	jsr	dly01s	
	ORG	ROM	,20020002 000		dec	mem1	
init	rsp		;reset SP		bne	lp1	
	lda	#Sff	126866 DA	4101	rts	#1000	
	sta	#JII ddrA		dly01s	lda	#128T	;delay 0.1 sec
	clr	prtA		lp2	clrx		
* MATN	PROGRAM			lp3	decx	12	
main	jsr	dly1s	;delay 1 sec		bne	1p3	
	jsr	melody	start music		deca	1-0	
	jsr	dly1s	pours midio		bne	1p2	
	jsr	dly1s			rts		****
	bra	main					* * * * * * * * * * * * * * * * * * * *
.page	Dra	and 104 at 6 &		*Put ta		nto memory	
	Y SUBRO	TTTNE			org	aMEL	MT MT MT MT COT DO DE ST
MELODY			:0 -> X		fcb		, MI, MI, MI, MI, SOL, DO, RE, MI,
m1	lda	aMEL, x	;load the note pitch		fcb		, FA, FA, MI, MI, MI, MI, RE,
	sta	NR	; into NR register		fcb	RE,MI,RE	, 501
	lda	aDUR, x	; load the pitch duration		org	aDUR	
	sta	DR	; into DR register		fcb		2,4,2,2,2,2,8,
	lda	#ND	; load the number of note	******	fcb		2,2,2,1,1,2,2,2,2,4,4
	sta	NDR	; repetition into NDR reg.	******			
	sta	MOR	; save X in memory		org fdb	vectors+ init	
m2	jsr	note	; generate the note		rap	init	;set restart address
	dec	DR	, yenezade die note	.end			
	bne	m2		.nolist			
	bclr	snd, prtA	;make a pause 10ms after				
	ldx	#100T	; each note				
	jsr	DLY01x	, each note				
	ldx	DLIGIX	;reload X from memory				
	cpx	#N-1	; are there any more notes?				
	blo	m3	vare chere any more notes:				
	DTO	cm		1			

Continuity buzzer is frugal with power

Hans Krobath, EEC, Nesconset, NY

HE CONTINUITY DETECTOR IN **Figure** 1 is based on W Dijkstra's "Fleapower circuit detects short circuits" (*EDN*, July 2, 1998, pg 122). The buzzer indicator allows you to devote full attention to making the connection without having to observe an LED. The circuit also consumes less power than Dijkstra's circuit. Power comes from two AA or AAA cells, which last for a period equal to their shelf life. Current consumption is less than 2.5 mA when the circuit de-

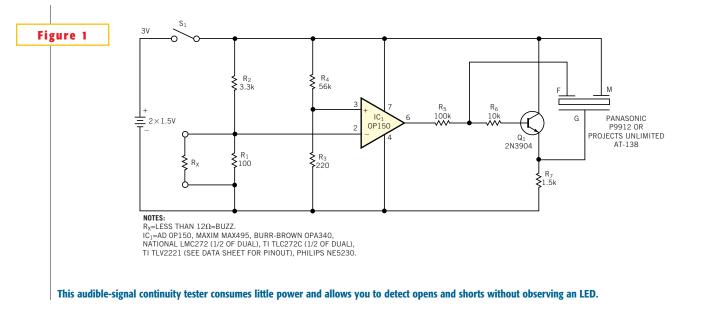


tects continuity and less than 1.7 mA for an open circuit. Open-circuit voltage is less than 100 mV, and short-circuit current is less than 1 mA. You can use a number of op amps for IC_1 , provided that the specs indicate rail-to-rail operation with a low-voltage single supply.

The piezo oscillator driver uses only 700 μ A when operating and consumes only Q₁'s leakage current when it is not operating. This type of piezo transducer is a passive, resonant-feedback type,

which provides high power efficiency and low-voltage operation. With R_x values greater than approximately 12Ω , the inverting input of the op amp is at a higher potential than that of the noninverting input. The resulting output is 0V plus the saturation voltage of the output stage. This output provides no bias current through R_5 and thus keeps Q_1 cut off. With R_x values lower than approximately 12Ω , the inverting input of the op amp has a potential lower than that of the noninverting input. The resulting output is 3V minus the saturation voltage of the output stage. The approximately 3V output biases Q_1 into the linear region. Q_1 and the piezo transducer, with their associated feedback, oscillate at their resonant frequency. Most transducers and the listed op amps operate with supply voltages as low as 2V. (DI #2350).

> To Vote For This Design, Circle No. 404



Stereo jack adds no-cost power/logic control

Gary O'Neil, IBM Microelectronics, Research Triangle Park, NC

ANY BATTERY-POWERED devices use peripherals that require only two conductors to complete their interfaces. You can use stereo phone jacks and monaural plugs to perform poweror logic-control functions in addition to completing their required I/O connections. Monaural plugs short-circuit the ring and sleeve of stereo jacks. You can place the ring connector, normally considered a redundant ground return, into service as an spst switch. A simple wireless transceiver illustrates how you can use stereo jacks for switching with monaural plugs, stereo plugs, or both (Figures 1 and 2). Using the design in Figure 1, you can connect the battery return to the ring of stereo jacks serving one or more I/O devices. The circuit in Figure 2 connects the returns of individual circuits to the ring.

With this scheme, power control be-

comes automatic with the plugging and unplugging of devices using monaural plugs, by virtue of the ring-to-sleeve short circuit. Three examples illustrate the principles of operation. In the first example, the transciever comprises a transmitter, a receiver that contains an audio amplifier, a battery supply for power, and two stereo phone jacks (J_1 and J_2) for transmitter modulation and audio output, respectively (**Figure 1**). J_1 's tip con-

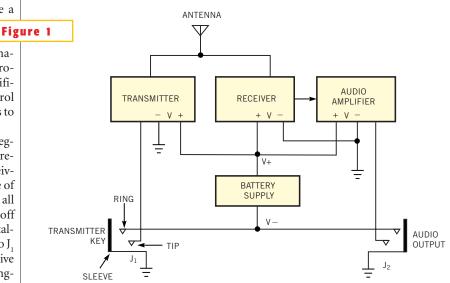


nection carries the modulation input to the transmitter. This input could be a keying line for CW (continuous modulation, for Morse code); a digital modulation interface; or an analog input, such as in a wireless microphone. The output of the audio amplifier (demodulated digital data, control tones, voice, music, or other) connects to the tip of J₂.

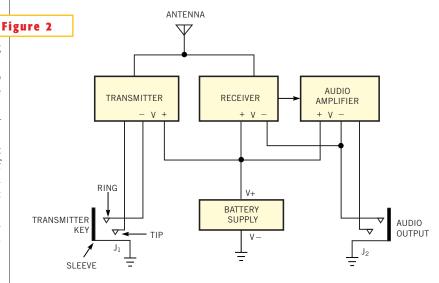
With no peripheral attached, the negative side of the battery floats, with no return to ground. Therefore, the transceiver receives no power. The negative side of the battery connects to the rings of all jacks you want to use for power-on/off control. Inserting a telegraph key, digitalmodulation device, or microphone into J. via a monaural plug connects the negative side of the battery to ground via the ringto-sleeve short circuit, and the transceiver turns on. Plugging an earphone or speaker into J, via a monaural plug completes an alternate, or redundant, ground return for the battery. Thus, inserting a plug into either jack completes the power path to all the transceiver circuits.

In another example, you can selectively isolate and enable circuits using stereo jacks to maximize power conservation. When you plug a peripheral into J₁, the circuit in Figure 2 enables only the transmitter circuit. When you plug a peripheral into J₂, the circuit enables only the receiver and audio-amplifier circuits. The return paths of the individual circuit functions float and connect to the ring of one or more stereo jacks associated with a peripheral that requires those circuit functions to operate. The battery permanently connects to the same ground reference as the sleeve of all jacks. You need both the receiver and audio amplifier to operate during the receive function; they share a common return path with the ring of J₂. You enable these circuits by inserting an appropriate peripheral (speaker or headphone) into J_2 via a monaural plug.

In the final example, you can further conserve power in specialized cases featuring remote on/off control, such as for transmitter on/off keying (**Figure 2**). You use insert a stereo plug into J_1 to remotely locate the ring/sleeve connection. The ring/sleeve path to the negative side of the







The absence of a peripheral plug breaks the ground return for either the transmitter or the receiver/audio-amplifier portion of the transceiver.

battery is incomplete until a peripheral switch or a key closes. You can define a ring/sleeve, tip/sleeve, or ring/tip/sleeve short circuit and use it to complete the desired electrical connections. In this example, the circuit consumes power only when you enable the transmitter; thus, you have maximum control of battery resources. (DI #2355).

To Vote For This Design, Circle No. 405

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S/H circuit minimizes aperture

John Guy, Maxim Integrated Products, Sunnyvale, CA

C ONVENTIONAL SAMPLE-AND-HOLD (S/H) circuits use one hold capacitor that charges during the track phase and disconnects during the hold phase. The voltage that the capacitor holds usually drives an A/D converter that operates synchronously with the S/H control signal. This approach can sometimes place excessive demands on the S/H circuit's bandwidth and settling capabil-

ities. You can improve performance by using two hold capacitors to imple-

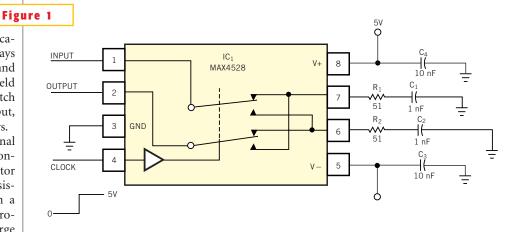
ment continuous **Fig** sampling (**Figure 1**). One capacitor or the other is always sampling the input signal, and the output is always the held value. A phase-reversal switch (IC_1) interconnects the input, output, and hold capacitors.

When the control signal (Clock) is low, the input connects to the C_2 hold capacitor via R_2 . C_2 and the on-resistance of the switch form a 160-nsec time constant, providing ample time to charge the capacitor. When Clock goes high, C_2 connects to the output via the lower switch,

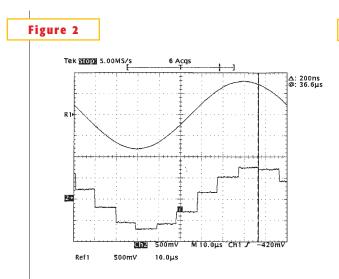
and C_1 connects to the input. Many factors affect the performance of this circuit. Droop rate on the hold voltage, for example, is a strong function of the outputload impedance. If the A/D-converter load is excessive, you should add a buffer amplifier at the output of the S/H circuit. The hold capacitors should be low-dielectric-absorption types, and the phase-reversal switch should specify low charge

injection and make-before-break timing. **Figure 2** (input and output at 100k samples/sec) and **Figure 3** (detail at 400k samples/sec) show good performance with the values shown. The high-speed transitions exhibit little overshoot or ringing. (DI #2354).

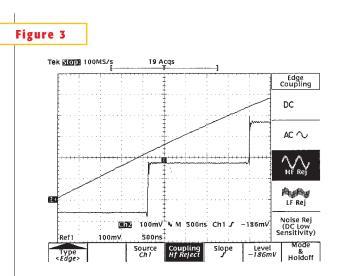
To Vote For This Design, Circle No. 406



A simple phase-reversal switch uses two hold capacitors to implement a continuous-sampling sample/hold circuit.



At a 100k-sample/sec sampling rate, the circuit in Figure 1 provides excellent hold accuracy.



The S/H circuit in Figure 1 exhibits low ringing and overshoot characteristics when sampling at 400k samples/sec.

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Edited by Bill Travis and Anne Watson Swager

Make a simple PC-based frequency meter

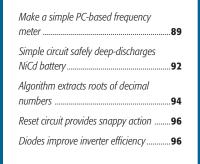
Radovan Stojanovic, University of Patras, Patras, Greece

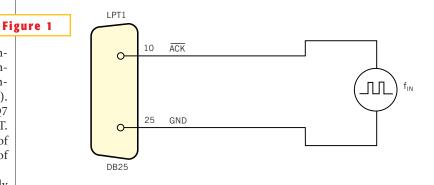
SIMPLE, LOW COST, and precision frequency meter uses only two pins of a pc parallel port (**Figure 1**). The TTL-level periodic input signal with frequency f_{IN} connects to the ACK pin of LPT1. This input produces an IRQ7 hardware interrupt on every rising edge (**Figure 2**). The software counts the number of IRQ7 interrupts in the time unit of timebase T. If this timebase is 1 sec, the frequency of the input signal equals the number of IRQ7 interrupts in 1 sec.

You can use many ways to precisely generate the timebase, T, such as using the delay() or sleep() functions in C. You can also use software calibration loops.

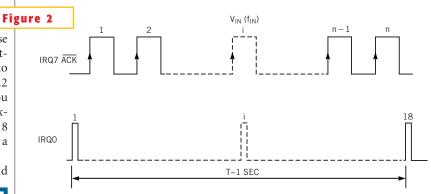
Unfortunately, these techniques are unreliable because they are based on polling. The best choice is to use a second interrupt, such as IRQ0 (software 0x1C). This interrupt is related to the internal PC timer and occurs 18.2 times/sec. For precise measurements, you can use proportional constants. For example, if your timebase equals the 18 IRQ0, you must correct the result by a factor of 18.2/18.

The software in Listing 1 is simple and









Input $f_{IN'}$ which connects to the ACK pin of LPT1, produces an IRQ7 hardware interrupt on every rising edge. The software counts the number of rising edges that occur during the timebase, T, which IRQ0 helps to generate.

interrupt-based, which allows for resident operation in an MS-DOS environment and for multitasking mode under Windows. For a timebase of 1 sec and using a 100-MHz Pentium PC, the frequency meter gives good results in the range of 10 Hz to 10 kHz with errors less than 0.26% for DOS and 0.94% for Windows (**Figure 3**). This design uses a Tektronix (www.tek.com) CFG280 function generator for reference. A faster PC should produce even better results.

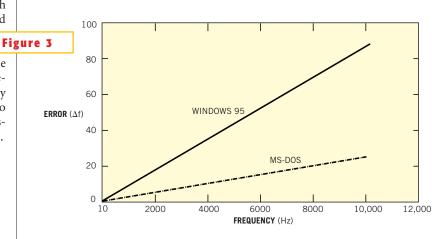
Listing 1 is written in Borland C++ compiler, and you can use the same pro-

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gram for DOS-based C compilers, such as Turbo C. Also, you can use the second parallel port LPT2, with interrupt IRQ5, to perform this same frequency-meter function. If you add one voltage-to-frequency, current-to-frequency, or temperature-to-frequency converter, the frequency meter can also perform simple, low-cost, and high-resolution measurements of analog values. (DI #2342)



To Vote For This Design, Circle No. 323 For a timebase of 1 sec and using a 100-MHz Pentium PC, the frequency meter gives good results that range from 10 Hz to 10 kHz with errors less than 0.26% for DOS and 0.94% for Windows.

LISTING 1–C++ FREQUENCY-METER PROGRAM

```
#include <stdio.h>
#include <dos.h>
#include <conio.h>
#define INTR_1 0X08 /* The clock tick interrupt */
#define INTR_2 0x0f /* IRQ7 */
#define ISR 0x20 /*interrupt service register*/
#define IMR 0x21 /*interrupt mask register*/
#define EOI 0x20 /* End-of-interrupt*/
#ifdef __cplusplus
  #define ____CPPARGS ...
#else
  #define CPPARGS
#endif
int count=0; /*time base*/
int freq=0; /*frequency*/
/*interrupt functions*/
void interrupt ( *oldbase)( CPPARGS);
void interrupt base(_CPPARGS); /*Interrupt routine for time base*/
void interrupt (*oldfrequ) (__CPPARGS);
void interrupt frequ( CPPARGS); /*Interrupt routine for frequency*/
void interrupt base(__CPPARGS)
ł
  count++; /* increase the time counter */
  outp(ISR,EOI); /*end of interrupt*/
}
void interrupt frequ(__CPPARGS)
freq++; /* increase the frequency counter */
outp(ISR,EOI); /*end of interrupt*/
}
int main(void) /*main program*/
{
```

int a; int port; int stop; float factor; factor=18.2/18; /*prop. constant for 1s*/ port=peek(0x40,8); /*find the address of the LPT1*/ /*read the Control register of the LPT1*/ a=inp(port+2); a=a|0x10; outp(port+2,a); /*enable interrupts on the pin ACK*/ outp(ISR,EOI); disable(); outp(IMR,0x20); /*Enable IRQ7 in the interrupt mask register*/ outp(ISR,EOI); oldbase = getvect(INTR_1); /* the settings of the interrupts*/ oldfrequ=getvect(INTR_2); setvect(INTR 1,base); setvect(INTR_2,frequ); enable(); while(!kbhit()) if(count>=18) /* display frequency*/ stop=freq; printf("\n F=%.2f [Hz]",stop*factor); freq=0; /*reset variables*/ count=0; ł setvect(INTR_1, oldbase); /* reset interrupts vectors*/ setvect(INTR 2,oldfrequ); return 0;



Simple circuit safely deep-discharges NiCd battery

Jim Hagerman, Science & Technology International, Honolulu, HI

ICKEL-CADMIUM (NiCd) batteries can possess an undesirable memory effect due to partial discharges. The remedy is a complete discharge before charging again. Figure Ia shows a simple circuit that performs this feat.

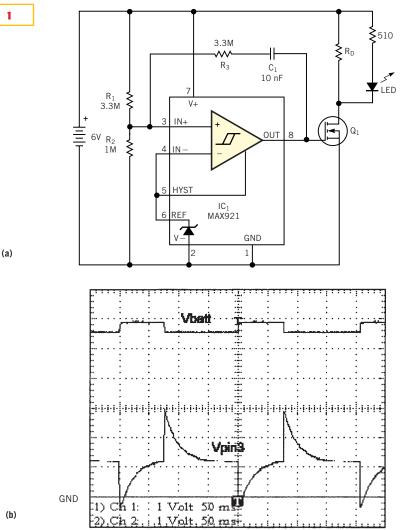
Although relatively straightforward in concept, the circuit has three redeeming features: It receives its power from the battery undergoing the discharge; after the battery is fully discharged, the current drain is only approximately 4 μ A, which is usually well below the self-discharge level of a battery alone; and an LED flashes at end-of-charge.

Ignoring LED current, R_D determines the rate at which the circuit discharges the battery, as follows:

$$I_{\text{DISCHARGE}} = \frac{V_{\text{BATTERY}}}{R_{\text{D}}}$$

A NiCd or nickel-metal-hydride (NiMH) battery has a nominal cell voltage of approximately 1.2V at midcharge and approximately 1V at end of charge. Do not discharge past the end-of-charge voltage, because you may damage the battery. The values in **Figure 1a** are for a four-cell battery. R_1 and R_2 determine the end-of-voltage limit referenced to the built-in 1.182V bandgap reference. When battery voltage is high, comparator IC₁ turns on Q₁, a power n-channel MOSFET, which discharges the battery through R_p .

When the battery reaches the end-ofcharge voltage, the circuit's behavior gets interesting. R_3 and C_1 provide positive ac feedback to ensure that the comparator fully switches and prevents the circuit from becoming a linear regulator. However, the intrinsic internal resistance of the battery also causes negative dc feedback. As the MOSFET turns off the battery terminal voltage, the comparator turns the MOSFET back on. The positive ac feedback overwhelms the negative feedback, thus ensuring switching, but only for a short time, and the circuit oscillates. The frequency is roughly



When the battery reaches the end of charge, this deep-discharge circuit (a) oscillates until the battery voltage stays below the hysteresis threshold (b).

$$\mathbf{f} = \frac{1}{2 \cdot \mathbf{p} \cdot (\mathbf{R}_3 + \mathbf{R}_1 \| \mathbf{R}_2) \cdot \mathbf{C}_1}.$$

Oscillation eventually stops when the battery voltage stays below the hysteresis threshold, which the intrinsic resistance of the battery determines. The higher the resistance, the longer the LED will flash. The circuit takes advantage of the fact that this resistance is greatest at the end of charge. When the discharge cycle stops, the LED stays off, and the only current drain is from IC_1 and the R_1/R_2 divider. Both of these values are small enough to leave the battery connected indefinitely. (DI #2348)

To Vote For This Design, Circle No. 324



Algorithm extracts roots of decimal numbers

Frank Vitaljic, Bellingham, WA

LGORITHM EXTRACTS CUBE ROOT" (EDN, Jan 15, 1998, pg 100) covers only the one-third power (cube root). In contrast, the C routine in Listing 1 calculates the Kth root $(X^{1/K})$ of positive decimal numbers X. Both K and X can vary widely. You type in X, K, and an estimate of the root; the routine then calls the calcRoot function in the software program. Upon calculating the root, the routine prints on screen the number of iterations performed and the root result X1/K. The routine raises this result to the Kth power and displays the result so you can make a comparison with the original X. The algorithm applies a Newton-Raphson approach to the equation Y=X^{1/K}. If you differentiate the equation and express it in recursive form, you obtain

ERROR = $Y(n + 1) - Y(n) = \frac{X - Y(n)^{K}}{KY(n)^{K-1}}$, FOR n = 0, 1, 2, 3K AND K = 2, 3, 4, 5K

This recursion monotonically converges toward the Kth root of the num-

TABLE 1-CUBE-ROOT MAXIMUM ERRORS	
Х	% Error
0.001	0.001
0.01	0.0005
0.1	0.0002
10	0.00005
100	0.00002
1000	0.00001

TABLE 2–CUBE-ROOT ITERATIONS

	Number	Number
	of iterations	this
X	1998 Design Idea	Design Idea
0.001	10	10
0.01	12	Eight
0.1	14	Six
10	19	Seven
100	23	11
1000	22	14

```
LISTING 1–KTH-ROOT EXTRACTION FOR DECIMAL NUMBERS
#include
                <iostream.h>
#include
                <iomanip.h>
#include
                <conio.h>
#define MIN(x,y) (((x) < (y)) ? (x) : (y)) /* min, max */
#define MAX(x,y) (((x) > (y)) ? (x) : (y)) /* values */
#define VIEWDATA(arrayname,numdata,datatype,lines,colms, \
                            colmwidth, dataform, prec, justify)
     { \
         int
                            i, j=0, k=0; ∖
                            sum=0.0, sum2=0.0; \setminus
         double
                            mean, variance; \
datamin, datamax; /* min, max data values */ \
(* array pointer */ \
          double
         datatype
                                                         /* array pointer
          datatype
                          *ptr = arrayname;
          cout.precision (prec);
                                                         /* tabulated precision
                                                         /* left or right
         cout.setf (ios::justify);
cout.setf (ios::uppercase);
          cout.setf (ios::showbase);
                                                         /* base of integers
                                                         /* clear screen
          clrscr();
              for (i=0; i < numdata; i++) { /* tabulate numdata items */ 
 if (j==0) cout << dec << i << " | "; 
 cout.width (colmwidth); 

               } (k==lines) { /* display data lines */ \
    cout << "\n"; \
    k = 0; \
    getch (); /* pause */ \
}</pre>
                  N
               if (i==1) { /* Initialize data min, max */ \setminus
                    datamin = MIN (*ptr, *(ptr-1)); \
datamax = MAX (*ptr, *(ptr-1)); \
                   /
               if (i > 1) { /* find min, max values */\
    datamin = MIN (*ptr, datamin); \
    datamax = MAX (*ptr, datamax); \
               } \
               sum += (double)(*ptr); \
sum2 += ((double)(*ptr))*((double)(*ptr)); \
ptr++; /* increment array pointer */ \
               ptr++; /* incn
/* end for() */
                                         \
             mean = sum / numdata; /* calculate data stats */ \
variance = (sum2 - sum*mean) / numdata; \
cout << "\nmin = " << datamin; \
cout << "\nmin = " << datamax; \
cout << " \nmean = " << datamax; \
cout << " \nmean = " << mean; \
cout << " variance = " << variance; \
cout.unsetf (ios::justify); \
getch (); /* pause */ \
/* end viewdata() */</pre>
     void main (void)
          double a[1000]; /* declare array of doubles */
int i; /* counter variable */
          /* generate 200 elements of doubles */
          for (i=0; i < 200; i++) a[i] = 0.333333*i-16.0;
          /* Display first 100 elements in increments of 14 lines,
3 columns each 20 spaces wide, in scientific form, 3-digit
precision, right justified. */
          VIEWDATA (a,100,double,14,3,20,scientific,3,right)
     }
```



ber. The routine terminates the iteration when

 $|Y(n+1)-Y(n)| \in ERROR = 10^{-6}.$

The error in the calculation is %ERROR $\notin \frac{\text{ERROR} \cdot 100}{\text{Y}(\text{ACTUAL})}$.

Table 1 shows cube-root errors for

numbers 0.001 to 1000. The number of iterations varies from six to 14. **Table 2** compares the number of iterations inherent in the algorithm with the number of iterations of the earlier Design Idea. For increased accuracy, you can set the maximum ERROR define to 1.0e-14 at the expense of increasing the number of iterations. You can download the C list-

ing from *EDN*'s Web site, www. ednmag.com. Click on "Search Databases/Links Page" and then enter the Software Center to download the file for Design Idea #2339. (DI #2339).

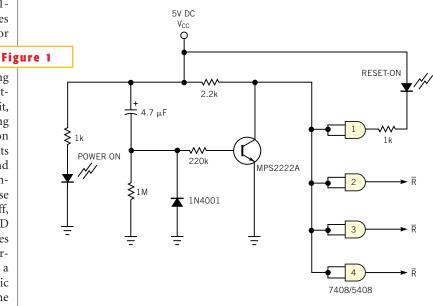
> To Vote For This Design, Circle No. 325

Reset circuit provides snappy action

Steve Kelley, Protobyte Inc, Liberty, MO

HE CIRCUIT IN Figure 1 provides a 1sec reset, using multiple AND gates for increased fanout. Intended for breadboarding or prototyping, the circuit generates a "snappy" master reset that remains active long enough to eliminate questionable startups. When you apply power to the circuit, the timing capacitor begins charging through the 1-M Ω resistor, turning on the npn transistor. The AND-gate inputs go low, generating the reset signal and turning on the reset LED. When the timing capacitor brings the transistor's base nearer to ground, the transistor turns off, and the 2.2-k Ω resistor pulls the AND gates' inputs high. The transistor isolates the capacitor from the AND gates' internal pull-up resistors and provides a smooth transition through the logic threshold. Upon removal of power, the 1N4001 diode discharges the timing capacitor. (DI #2351).

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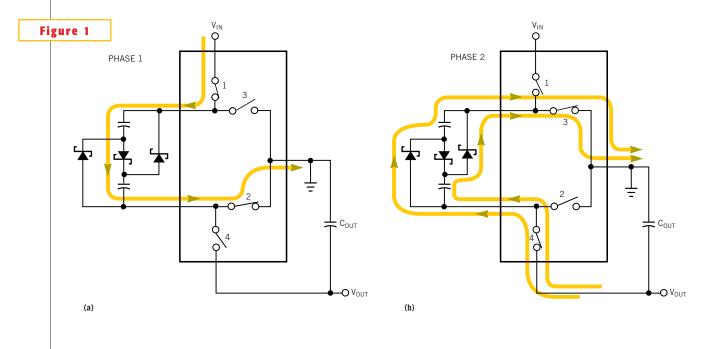


Diodes improve inverter efficiency

Jeff Witt, Linear Technology Corp, Milpitas, CA

N "SWITCHED-CAPACITOR REGULATOR PROVIDES GAIN" (EDN, March 13, 1998, pg 80) a switched-capacitor voltage inverter wired as a supply splitter steps a positive voltage down to an output voltage equal to half the supply voltage. The input current to such a circuit is one-half the output current; thus, you obtain higher efficiency and lower power loss than you would from a linear regulator performing the same function. You can obtain the same benefits while inverting the input voltage. **Figure 1** shows the principles of operation. Typical switched-capacitor inverters contain

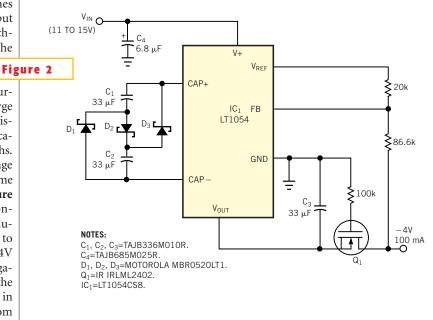




Adding a few diodes to a switched-capacitor inverter doubles the current from input to output.

four internal switches. Two switches charge a flying capacitor from the input voltage to ground; the other two switches discharge the capacitor, pulling the positive side to ground and generating a negative output voltage.

By adding three diodes to steer the current, you can use the switches to charge two capacitors in series and then discharge them in parallel to an output capacitor. Figure 1 shows the current paths. The absolute value of the output voltage equals half the input voltage minus some loss from the switches and diodes. Figure 2 shows a practical circuit, which converts 12V to -4V at 100 mA. IC, modulates the voltage drop across Switch 1 to regulate the output, maintaining -4V from an input of 11 to 15V. Many negative supplies power loads that can pull the output above ground (op-amp circuits in particular). Q1 prevents such a load from pulling IC,'s output pin above the voltage on the op amp's ground pin. Because most of IC₁'s operating current flows from its ground pin, the input current to this circuit is slightly more than half the output current. When the circuit delivers 100-mA load current, measurements



This 12V to -4V converter delivers 100-mA output current with 63-mA input current.

show that the 12V input delivers 64 mA. The circuit dissipates only 350 mW, so an all-surface-mount configuration runs cool. (DI #2352).

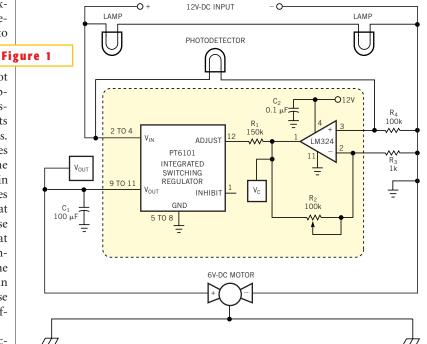
To Vote For This Design, Circle No. 327 Edited by Bill Travis and Anne Watson Swager

Switching regulator drives robot motor

Donald Comiskey, Power Trends Inc, Warrenville, IL

HE CIRCUIT IN Figure 1 shows an example of how you can use an integrated switching regulator (ISR) to efficiently vary the speed of a permanent-magnet dc motor. In this application, the rotating head of a robot senses the presence of an oncoming object (perhaps a human). If the robot senses an object, it slows the rotation of its head to closely survey the surroundings. If an object is indeed present and comes within a certain distance of the robot, the robot's head stops rotating and "looks" in the direction of the object. The robot uses a typical proximity-detection device that senses reflected light (Figure 2). It's nose contains a photodetection device that senses the light that reflects from an oncoming object. The primary source of the light is the robot's eyes, which contain two lamps. The photodetector in the nose resides in a black tube to reduce the effects of ambient light.

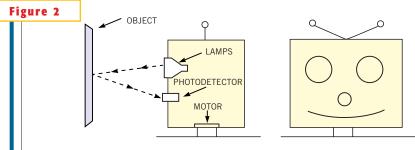
The sensed light causes a photodetection current to flow through the photodetector and R_4 , developing a voltage across R_4 (**Figure 1**). The LM324 op amp, which you configure as a noninverting amplifier with an adjustable gain of



ideas

This robotic circuit uses an integrated switching regulator as a power op amp to control the rotation of an object-seeking robot's head.

		Figure
Switching regulator drives robot motor	99	
Simple fix adds door-chime		
repeater	00	
Clock multiplier circumvents PLL 1	02	
Synthesize optimal digital-frequency dividers	04	
Voltage regulator controls scanner- lamp brightness1	08	
Simple changes improve Schmitt trigger	10	R2D2



R2D2 has lamps in his eyes to provide a light source and a photodetector in his nose to detect light reflected from an oncoming object.



 $1+R_2/R_3$, amplifies this voltage. The amplified voltage is a control voltage, V_c , which routes to the ISR's Adjust pin via R_1 . A decrease in V_c , relating to a decrease in light level, causes the ISR's output voltage and the corresponding speed of the dc motor to increase. An increase in V_c , relating to an increase in light level, causes V_{OUT} and the corresponding motor speed to decrease. A further increase in light level causes V_c to increase to a point

at which V_{OUT} becomes low enough to stop the rotation of the motor. A linear relationship exists between V_C and V_{OUT}: V_{OUT}= $-V_{C}$ +6.25V.

In the absence of light, the output voltage of the op amp saturates near 0V. The equation shows that a control voltage of 0V produces an ISR output voltage of 6.25V, causing the motor to rotate at its maximum speed. A light level that produces a 6.25V control voltage results in an ISR output voltage of 0V, causing the motor to stop rotating. Intermediate motor speeds result from control voltages between the extremes of 0 and 6.25V. You can adjust feedback resistor R₂, which sets the op-amp gain, to obtain any desired sensitivity. The PT6101 ISR in **Figure 1** is 85 to 90% efficient and supplies motor currents as high as 1A. (DI #2353).

> To Vote For This Design, Circle No. 311

Simple fix adds door-chime repeater

Dennis Eichenberg, Parma Heights, OH

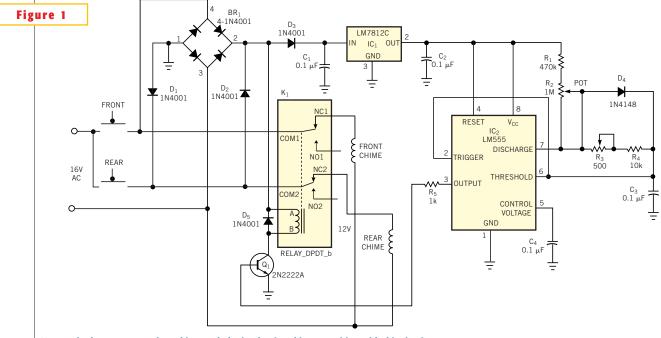
E LECTROMECHANICAL DOOR CHIMES can enhance your home, but they are vulnerable to costly repair problems. A defective pushbutton switch or a careless visitor can maintain the chime in an energized state for a prolonged period, thereby damaging the chime. The circuit in **Figure 1** prevents damage to the chime and improves the chime's effectiveness by repeating the chime strike for as long as the pushbutton remains depressed. The circuit controls both front and rear chimes. The heart of the circuit is timer IC₂, which you configure as an

astable multivibrator. The timing components, R_1 , R_2 , R_3 , and C_3 , provide the required pulse widths.

The maximum duty cycle of a typical chime is 25%. The energized time is 0.76(R_3+R_4) C_3 , which you can adjust from 7.6 msec to 0.4 sec. The de-energized time is 0.693(R_1+R_2) C_3 , which you can adjust from 0.3 to 1 sec. IC₂ drives the 12V relay, K_1 , via resistor R_5 and transistor Q_1 . D_5 is a flyback diode that protects K_1 . You must select K_1 to fit the specific chime. The coil current can be as high as 200 mA. The circuit normally uses closed

contacts so that illuminated pushbutton switches operate properly. The 16V-ac door-chime power energizes the circuit via bridge BR₁. IC₁ provides voltage regulation, and C₁ and C₂ provide filtering. Diodes D₁ and D₂ provide power from the rear-door pushbutton. D₃ isolates the filtered timer power from the relay. (DI #2349).

> To Vote For This Design, Circle No. 312



You can both protect your door chime and obtain pleasing chime repetition with this circuit.

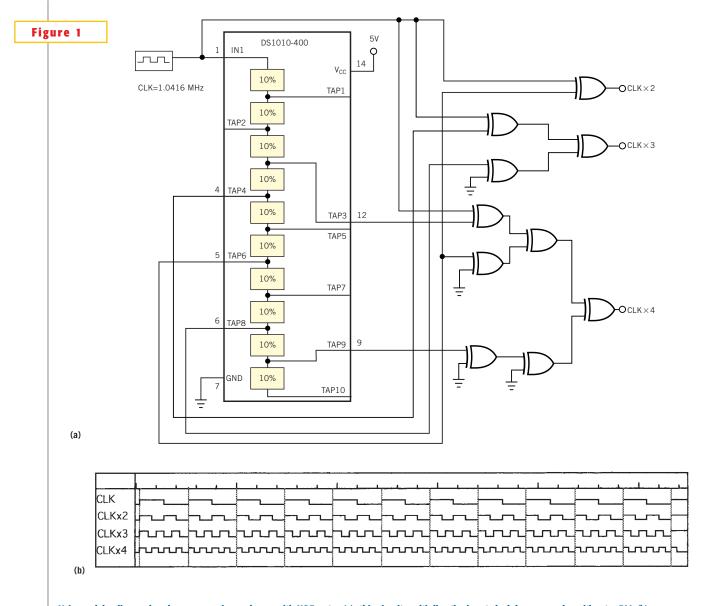


Clock multiplier circumvents PLL

Jose Carlos Cossio, Santander, Spain

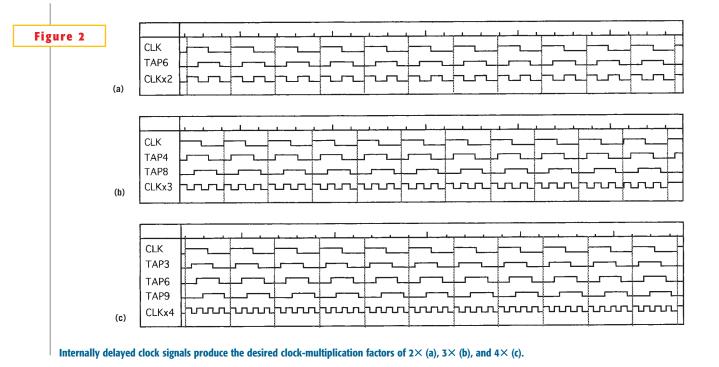
USING A STANDARD PLL CIRCUIT, such as the CMOS 4046B with some passive components, is a wellknown way to design a clock multiplier. Unfortunately, using a PLL in a digital circuit has two disadvantages: It takes a long time for the circuit to reach a stable output frequency, and the frequencydrift compensation has a complex design. An alternative clock-multiplier approach uses simple combinatorial logic and a delay line (**Figure 1**). By taking into account the propagation delays in combinatorial logic and the fact that most logic designs are edge-triggered, the circuit can multiply by 2, 3, 4, and potentially beyond. You can use this technique to increase the system clock speed and maintain a low-frequency clock for the rest of the circuit, thereby helping to reduce EMI and cost in high-speed logic designs. Also, the circuit exhibits a very fast start-up. This approach is common in modern μ P architectures that use clock-doubling techniques to achieve better performance at low costs.

In place of the silicon delay line, you could use standard CMOS logic. However, the differing propagation delays for high-to-low and low-to-high transitions



Using a delay line and a phase-comparison scheme with XOR gates (a), this circuit multiplies the input clock by 2, 3, and 4 without a PLL (b).





 $(t_{pdHL} \neq t_{pdLH})$ presents a problem. A standard delay line with fixed and known delay taps is preferable.

The circuit in **Figure 1a** uses a Dallas Semiconductor (www.dalsemi.com) DS-1010-400 delay line, which has 10 builtin fixed delays of 40 nsec, to implement a $2\times$, $3\times$, and $4\times$ clock multiplier that operates from an external 1.0416-MHz clock. This design requires XOR gates with short propagation delays, such as advanced-bipolar or fast CMOS gates with propagation delays of less than 10 nsec, so that the XOR-gate delays are negligible.

The circuit works by using the XOR gates to perform a phase comparison. These gates monitor the difference between the incoming clock signal and the delayed clock signals. First, the circuit shifts right, or delays, the signal to be multiplied: once for $2\times$, twice for $3\times$, three times for $4\times$, and so on. Then, because an XOR gate sits between the source and the delayed signals, the result of the XOR operation is the signal mul-

tiplied by 2, 3, and 4. The resultant clock signals have the same duty cycle as the incoming signal (Figure 1b). Figure 2 shows the internally delayed clock signals that are necessary to produce the $2\times$, $3\times$, and $4\times$ clocks.(DI #2344).

To Vote For This Design, Circle No. 313

Synthesize optimal digital-frequency dividers

Lindo St Angel, PrairieComm Inc, Arlington Heights, IL

OR MANY APPLICATIONS, you need to divide a reference clock into one or more subclocks to use in different parts of the system. Sometimes, this divider circuit is simple. For example, a circuit that divides by an integer number is easy to construct using a few flip-flops and assorted logic gates. However, often you must build a noninteger divider, for example, a divide by 7/8 or 512/1025. In these cases, you could use a divider and a PLL to divide the input reference by the denominator and then multiply the result by the numerator, but the circuit would become relatively complex and require analog components.

However, if your application can tolerate some clock jitter, there is another answer: the binary-rate-multiplier (BRM) circuit. This well-known circuit works by multiplexing two dividers into and out of the divide path. Unfortunately, it is sometimes difficult to find the set of design parameters that gives the least amount of jitter and the desired divider ratio. Using the following method and circuit you can easily generate optimum BRMs.

The average frequency, $\mathbf{f}_{\rm OUT}$, of the BRM output is:

$$f_{OUT} = f_{IN} \cdot \frac{(REP_1 + REP_2)}{(REP_1 \cdot DIV_1) + (REP_2 \cdot DIV_2)}, \quad (1)$$

where f_{IN} is the frequency of the input ref-



erence clock, DIV_1 is the number of times the first divider divides the input clock, DIV_2 is the number of times the second divider divides the input clock, REP_1 is the number of input clock cycles for which the first divider is active, and REP_2 is the number of input clock cycles for which the second divider is active.

Instantaneous frequency of the BRM output equals the frequency of the input clock divided by the the active divider. The BRM output jitters between these two frequencies. However, you can minimize this jitter by choosing the parameters DIV, and DIV, according to

$$DIV_1 = INT \frac{f_{IN}}{f_{OUT}},$$
 (2)

and

$$DIV_2 = DIV_1 + 1.$$
 (3)

You then need to choose values for the parameters REP_1 and REP_2 . One way to

choose these values is to transform **Equa**tion 1 into an optimization problem and finding the values of REP₁ and REP₂ that minimize the transformed equation, given your chosen values for DIV₁ and DIV₂:

$$\min Z = \frac{f_{\rm IN}}{f_{\rm OUT}} \cdot \frac{(\text{REP}_1 + \text{REP}_2)}{(\text{REP}_1 \cdot \text{DIV}_1) + (\text{REP}_2 \cdot \text{DIV}_2)} - 1.$$
(4)

The constraints on this equation are that Z is greater than or equal to zero and that REP_1 and REP_2 are integers that are greater than or equal to unity.

You can solve **Equation 4** using integer nonlinear optimization techniques. Many commercial software packages, including Microsoft Excel, solve these classes of problems. Enter **Equation 4** into Excel and use the solver from the tools menu to operate on the equation, using the above constraints. To get Z to exactly equal zero, it is important to increase the solver's precision and tolerance settings to about 10 times their default values. Also, make sure that you check your results by plugging in all values and checking that Z exactly equals zero. If it doesn't, you have to increase the solver's precision and tolerance settings.

Once you have obtained values for all the parameters, you can use them in the Verilog model to get a circuit from a logic-synthesis tool (**Listing 1**). If you don't have access to logic synthesis, the Verilog model can give you some idea of how to manually build up the circuit from gates. You can download **Listing 1** from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases/Links Page," and then enter the Software Center to download the file for Design Idea #2358. (DI #2358).

> To Vote For This Design, Circle No. 314

LISTING 1-BINARY-RATE-MULTIPLIER VERILOG

```
mcnt = 0;
// Ports:
                                                                                                                                                        ماده
//
// clkin:
// rsb:
// clkout:
                                                                                                                                                             if (rst_ment == 1'b1)
ment = 0;
                       Clock input to be divided down.
Reset, active Low input.
Binary Rate Multiplied clock signal output.
                                                                                                                                                          else
                                                                                                                                                               mont = mont + 1;
module brm (clkin, rstb, clkout);
// Change parameters below to vield the desired BRM.
                                                                                                                                                  always @(mont)
// You can do this from the module which instanciates the BRM by:
// inst brm #(div1, rep1, div2, rep2) brm;
11
// The divide ratio is equal to:
// (rep1 + rep2)/(rep1*div1 + rep2*div2)
                                                                                                                                                       endcase
// The default parameters give a 7/18 divide ratio.
                                                                                                                                             // Output Register
//
     parameter divl = 2; // Divider one
parameter repl = 3; // Number of times to repeat divider 1
parameter div2 = 3; // Divider two
parameter rep2 = 4; // Number of times to repeat divider 2
                                                                                                                                                       else
                                                                                                                                                             clkout = rst ment;
// These parameters must be chosen so that synthesis will create a
// large enough counter. The mbit parameter is chosen so that two raised
// to the power of mbit is equal to or greater than the max of (div1, div2).
// The sbit parameter is chosen so that two raised to the power
// of sbit is equal to or greater than the max of (div1*repl, div2*rep2).
//
                                                                                                                                             11
     parameter mbit = 2; // Number of bits needed for main counter parameter sbit = 4; // Number of bits needed for state counter
                                                                                                                                                             begin
                                                                                                                                                                  scnt = 0;
     input clkin, rstb;
                                                                                                                                                              state = 1'b0;
                                                                                                                                                          end
     output clkout;
                                                                                                                                                       else
if (rst_scnt == 1'bl)
     reg [(mbit - 1):0] mcnt;
reg [(sbit - 1):0] scnt;
                                                                                                                                                              begin
                                                                                                                                                                    scnt = 0;
state = ~state;
      reg clkout, state, rst_mcnt, rst_scnt;
                                                                                                                                                               end
     wire rst;
                                                                                                                                                             else
                                                                                                                                                              scnt = scnt + 1;
     assign rst = ~rstb;
                                                                                                                                             11
//
// Main Counter.
     always @(posedge clkin or posedge rst)
    if (rst == 1'b1)
                                                                                                                                                  always @(scnt)
                                                                                                                                                       case (state)
                                                                                                                                                         endcase
                                                                                                                                             endmodule
```

```
else

if (rst_mont == 1'bl)

mont = 0;

else

mont = mont + 1;

//

// Main Counter reset generation.

// This is used to switch the modulus of the Main Counter.

//

always @(mont)

case (state)

1'b0: rst_mont = (mont == (div1 - 1)) ? 1'b1 : 1'b0;

1'b1: rst_mont = (mont == (div2 - 1)) ? 1'b1 : 1'b0;

1'b1: rst_mont = (mont == (div2 - 1)) ? 1'b1 : 1'b0;

endcase

//

// Output Register

//

// State Counter and State Flag generation.

// When State Flag is Low, the BRM is using the first divide ratio,

// When State Flag is Low, the BRM is using the second divide ratio.

// When State Flag is Low, the BRM is using the second divide ratio.

// When State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// when State Flag is Ligh, the BRM is using the second divide ratio.

// always @(posedge clkin or posedge rst)

if (rst_scnt == 1'b1)

begin

scnt = 0;

state = -state;

end

else

scnt = scnt + 1;

//

State Counter reset generation.

// This is used to switch the modulus of the State Counter.

//

always @(scnt)

case (state)

1'b0: rst_scnt = (scnt == ((div1 * rep1) - 1)) ? 1'b1: 1'b0;

1'b1: rst_scnt = (scnt == ((div2 * rep2) - 1)) ? 1'b1: 1'b0;

1'b1: rst_scnt = (scnt == ((div2 * rep2) - 1)) ? 1'b1: 1'b0;

1'b1: rst_scnt = (scnt == ((div2 * rep2) - 1)) ? 1'b1: 1'b0;

// State Counter the second to the scate to the scate to the scate to to the scate to the scate to to the scate to to the scate to to the scate to the scate to to the scate to to the scate to t
```



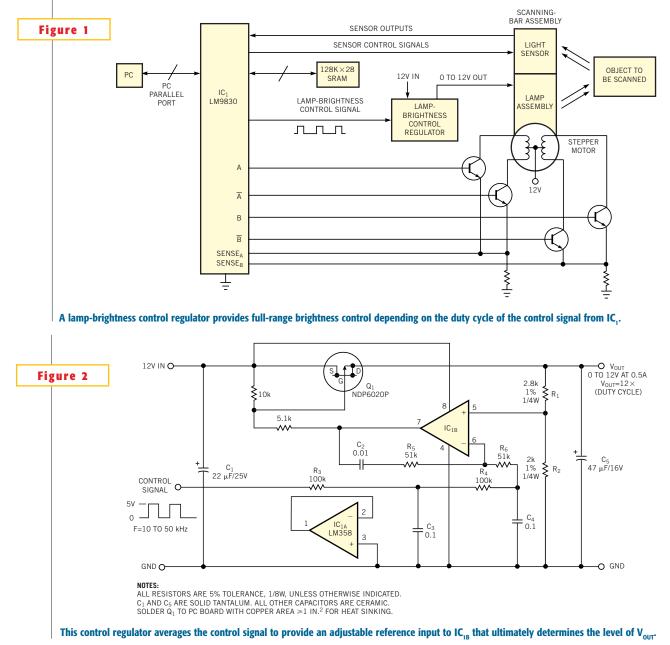
Voltage regulator controls scanner-lamp brightness

Chester Simpson, National Semiconductor, Santa Clara, CA

A MAGE-SCANNING DEVICE performs best when the scanner IC controls the brightness of the image reflected into the light sensors. The best way to control brightness is by adjusting the intensity, or light output, of the fluorescent lamp that shines light onto the scanned item. Traditionally, adjustable brightness has been economically unfeasible in most scanners because it is costly to implement a high-current voltage source that is also software-programmable. However, you can use a simple, lowcost circuit to implement full-range lamp-brightness control (**Figure 1**).

The fluorescent lamps in most low-

cost scanners operate from a fixed 12V source, which operates the lamp at maximum brightness. If you reduce the source to a lower voltage, you can adjust the brightness of the lamp to virtually any level. You can accomplish the voltage change using a circuit that takes in 12V and produces a regulated dc output volt-



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age that varies from 0 to 12V, depending on the lamp-brightness control signal coming from IC_1 's scanner IC. IC_1 sets the duty cycle of the control signal, which is a 5V pulse train.

The lamp-brightness control regulator takes in 12V and regulates this input to any voltage from 0 to 12V (**Figure 2**). Because the on-resistance of the NDP6020P FET is only approximately 50 mV, the maximum regulated output voltage the circuit provides is within approximately 25 mV of the input voltage at the typical lamp current of 0.5A.

The circuit generates a regulated output using error-amplifier IC_{1B} , the R_1/R_2 resistive divider, and an adjustable reference voltage at Pin 6 of IC_{1B} . The circuit produces this reference voltage by averaging the input control signal's squarewave pulse train. R_3 , C_3 , R_4 , and C_4 filter

the square waves into a dc voltage. The voltage across C_4 is the average value of the pulse train, which is directly proportional to the duty cycle:

$V_{C4} = 5V \cdot DUTY CYCLE.$

By adjusting the duty cycle of the 5V pulse train, you can linearly vary the reference voltage at Pin 6 of IC_{1B} from 0 to 5V. You can program a maximum of 4095 duty-cycle values for the LM9830 scanner IC, which yields 4095 brightness levels.

 IC_{1B} compares the voltage across C_4 with the voltage at the center of R_1 and R_2 , which the circuit derives from V_{OUT} . The regulating action of IC_{1B} constantly adjusts the gate-drive voltage to Q_1 , forcing V_{OUT} to a value that keeps equal the voltages at the inputs of IC_{1B} . In this way, the voltage at C_4 , which is proportional to the duty cycle of the pulse train, controls the regulated voltage, V_{OUT} . You can calculate V_{OUT} using the following equation:

$$V_{OUT} = V_{C4} \cdot \frac{R_1 + R_2}{R_2} = V_{PK}$$

DUTY CYCLE $\cdot \frac{R_1 + R_2}{R_2}$,

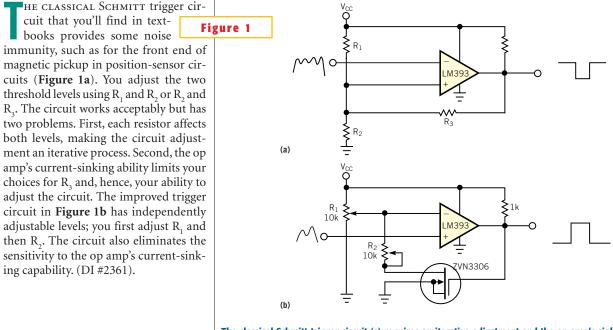
where V_{PK} is the peak amplitude of the pulse train (5V in this application) and duty cycle is the pulse on-time divided by the total period.

 R_5 , R_6 , C_1 , C_2 , and C_5 are necessary for compensation and stability. For the component values in the **figure**, the best performance occurs when the frequency of the pulse train is 10 to 50 kHz. (DI #2356).

> To Vote For This Design, Circle No. 315

Simple changes improve Schmitt trigger

Ron Patrick, ECM, Los Altos, CA



To Vote For This Design, Circle No. 316 The classical Schmitt-trigger circuit (a) requires an iterative adjustment and the op amp's sink current affects the ability to adjust the circuit. The adjustable levels of an improved circuit (b) are completely independent. Edited by Bill Travis and Anne Watson Swager

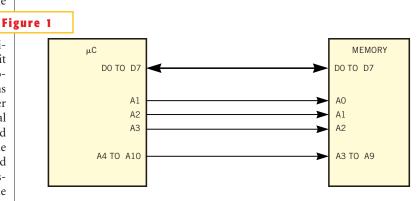
Access odd memory locations without hardware

Sorin Zarnescu, NEC Electronics, Santa Clara, CA

OME RISC CONTROLLERS, like the NEC V850 family, use an internal 32-bit architecture with an external 16-bit bus. The architecture also allows interfaces with 8-bit memories. However, with 8-bit memories, accesses to and from odd locations automatically access the higher-order byte. Thus, you would need external transceivers to access both even and odd locations. However, you can "trick" the processor and thereby save the space and cost associated with the external transceivers. Like everything else in life, the method doesn't come free-the price you pay is execution time.

The idea (Figure 1) is fairly simple: Connect the memory data bus to the least-significant bit (D0 to D7) of the μ C. Then, connect the memory-address bus to the μ C without using A0, so that the memory never sees an odd address. Thus, addressing the memory generates only even addresses. At first glance, the method might seem wasteful, because the memory occupies twice the space it needs, but with large memory spaces available (the V850 family can address as much as 16 Mbytes), the wastage should not present a problem. As an example,

Access odd memory locations without hardware
Charge indicator gauges lead-acid batteries
Use derivatives to catch RF calibration errors
μC-based circuit performs frequency multiplication 108
Kick start a crystal oscillator in Spice 110



ideas

A simple technique allows you to access odd memory locations without the need for external transceivers.

LISTING 1–SAMPLE PROGRAM TO ARRANGE STORAGE OPERATION

r2,0[r1]; 00 --> 0x100 st.b shr 8,r2 ; shift 10 into the least significant byte r2,2[r1]; 10 --> 0x101 st.b shr 8.r2 ; shift 20 into the least significant byte r2;4[r1]; 20 --> 0x102 st.b 8,r2 shr ; shift 30 into the least significant byte st.b r2,6[r1]; 30 --> 0x103

suppose register r2 contains the following data that you should store in a $1k \times 8$ memory, starting at address 0x100:

Most			Least
significant	t	sign	ificant
byte			byte
30	20	10	00
After stori resembles th	0	1 .	he memory
Address		Data	
:			
:			
0x100		00	

0x101	10
0x102	20
0x103	30
:	

Assuming (r1)=0x100, the sample program in Listing 1 arranges the storage operation. The tradeoff between extra hardware and longer execution time depends on the application's requirements. (DI #2366)

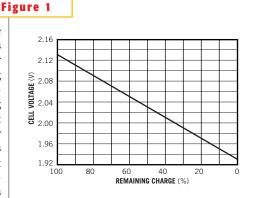
> To Vote For This Design, CIRCLE NO. 328



Charge indicator gauges lead-acid batteries

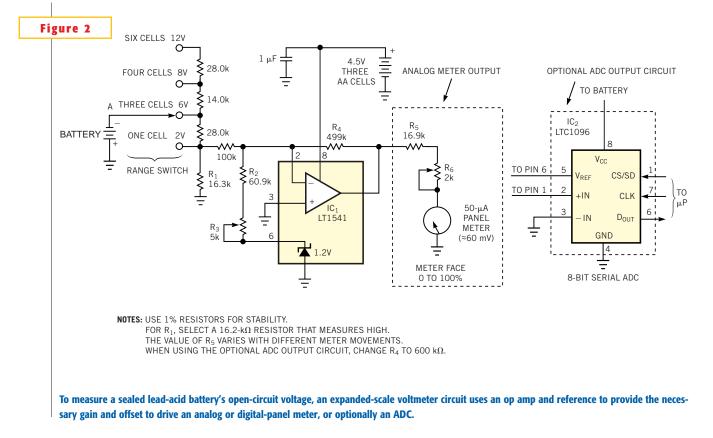
Fran Hoffart, Linear Technology Corp, Milpitas, CA

RECHARGEABLE, LTHOUGH sealed lead-acid cells are uncommon in portable applications, they are a good choice for standby applications, such as emergency lighting and burglar alarms. A key advantage to using these batteries is that you can determine the amount of remaining charge by measuring the open-circuit voltage. This technique is invalid for NiCd or NiMH cells. Figure 1 shows the relationship between the amount of remaining charge versus the opencircuit battery voltage. This curve is accurate to approximately 10%, provided that you have not charged or discharged the battery for at least 24 hours. A simple circuit measures the open-circuit voltage, such as the ex-



The curve of remaining charge versus open-circuit battery voltage for a sealed lead-acid battery is accurate to approximately 10%, if you haven't charged or discharged the battery for at least 24 hours. panded-scale voltmeter circuit in **Figure 2**, which follows the curve in **Figure 1**.

Sealed lead-acid batteries are available in several sizes, from a single D size (2.5 Ahr) to multicell rectangular battery packs. These cells can provide high output currents and years of reliable backup power. Other desirable features include relatively simple charge requirements and low self-discharge. The low self-discharge and ease of determining the remaining charge make sealed lead-acid batteries an ideal choice for flashlights and portable lighting. The low selfdischarge, which is approximately 5% per month at 25°C, means that a rechargeable flashlight using sealed lead-acid cells will still have usable





capacity of approximately 30% after one year of inactivity. NiCd and NiMH cells lose approximately 30% of their charge per month. A flashlight using NiCd cells requires a trickle charge when not in use to ensure reliable power when necessary. Without trickle charging, NiCd cells will completely discharge after three to four months of inactivity.

With the range switch in **Figure 1** in the one-cell position, the panel meter doesn't move until the input voltage exceeds 1.930V. Full scale corresponds to an input voltage of 2.130V. The op amp and reference provide the gain and offset for driving a digital panel meter, an ADC, or an analog meter with the meter scale calibrated from 0 to 100% of remaining charge. A rotary switch allows you to use the meter circuit with multicell battery packs containing one to six cells. You can measure other cell quantities by selecting the appropriate resistor divider values.

The circuit configures the op-amp section of IC_1 , which also includes an unused comparator, as an inverting gain-offive amplifier. This configuration produces a 1.000V change at the output for a 200-mV change at the input. The negative terminal of the battery connects to the op amp's inverting input resistor. To accomplish the 1.930V offset, IC_1 's internal 1.200V reference, R_2 , and R_3 generate a current that flows into the op amp's summing node (Pin 2). The op-amp out-

TABLE 1-BATTERY VOLTAGE VERSUS METER READING							
Number of cells	Nominal voltage (V)%	0%	50 %	100%			
1	2	1.93	2.03	2.13			
3	6	5.79	6.09	6.39			
4	8	7.72	8.12	8.52			
6	12	11.58	12.18	12.78			

put drives a standard 50- μ A analog panel meter with a scale from 0 to 100%. You can also use a 1V full-scale digital panel meter or an ADC (**Figure 2**). The 8-bit ADC, IC₂, uses the 1.2V reference voltage of IC₁ for the ADC reference, giving a full-scale output (8 bits) for a 1.2V input. If you use the ADC, the op amp's gain must increase from 5 to 6 to provide an output of 1.2V from the op amp for a 200-mV change at the input. To make this change, you simply increase the value of R₄ to 600 k Ω . You can also use analog meters ranging from 100 μ A to 1 mA, if you reduce the values of R₅ and R₆.

Calibrating the circuit requires an adjustable voltage source, preferably with coarse and fine voltage adjustment and a digital voltmeter. With three AA cells for power and the range switch in the one-cell position, apply a precise -2.130V to the input at point A. Connect a DVM to the op amp output (Pin 1) and adjust R₃ for a 1.000V reading on the DVM. Next, adjust R₆ for a full-scale reading, 100%, on the analog meter. Decreasing the voltage source by 100 mV to -2.030V should drop the DVM reading to 500 mV and drop the analog meter to midscale, or 50%. Dropping the voltage source an additional 100 mV to -1.930V results in a DVM reading near 0V and a corresponding meter indication of 0%. Because of minor resistor and off-set-voltage errors, the output may not exactly equal 0V, but may be a few mV positive. For this application, this value is more than adequate. Resistor values of 1% provide the best accuracy and stability, but you can use a standard 16.2-k Ω 10% resistor that measures approximately 100 Ω high for R₁. You can use **Table 1** to verify other ranges.

The circuit does not require a power switch because the op-amp section of the circuit draws extremely low quiescent current ($12 \mu A$). Battery life should equal the shelf life of the battery, which is several years. The op amp's input also includes overvoltage and reverse-voltage protection. (DI #2359)

> To Vote For This Design, Circle No. 329

Use derivatives to catch RF calibration errors

Steven C Hageman, Hewlett-Packard Co, Santa Rosa, CA

ANY RF-SYSTEM CALIBRATIONS involve checking for minimum power available or removing system offsets. One example is the checking of an RF source's output power. The system specifications may call for a minimum source power minus any cabling power loss, but a typical source may be able to provide more power than the manufacturer specifies as the minimum. To minimize the system cost, it is best to set the test-line limit to the minimum power plus a suitable instrumentation uncertainty (**Reference 1**).

This simplistic test may not catch all of the possible system problems. Loose RF connections or bad cables may result in power holes. Although these power holes may not always be deep enough to drop the power below the specified minimum test limit, no one wants to ship a system with a loose RF connection, or worse. Trained personnel may catch such a problem if they view it graphically, but this sort of test is very hard to quantify.

A better way to detect problems is to differentiate the data and place limits on the data's rate of change. This method is a surefire way to test for system problems that don't show up in the minimum-



power test. You can apply this technique to a large class of RF test and calibration issues, primarily the removal of system offsets during calibration. Many systems function properly with large offsets because calibration removes these offsets. However, the data usually has typical mismatch ripple effects over frequency, which cause the offset value to change as the frequency changes. If the offset ripple is too great or changes with frequency at a large rate, the stability of the calibration may be in jeopardy; a small change in the location of the ripple frequency may cause a large change in calibration offset data. By looking at the derivative data of the calibration, you can view the rate of change of the offset. When the rate of change reaches a certain level, the test alerts you, thereby the test is less subjective.

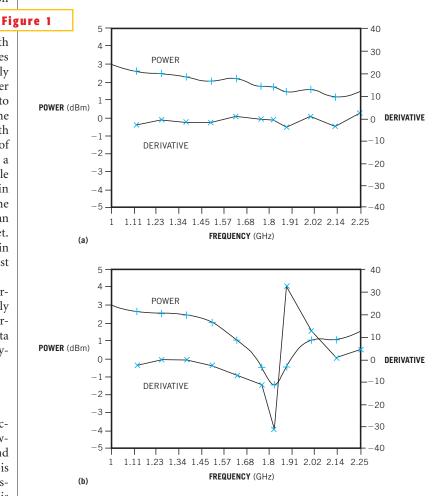
Assuming that your test is computercontrolled, you should be able to easily access the test data. You can apply the forward difference equation to the test data to find the first derivative on a point-bypoint basis:

$$F(x) = \frac{F(x + Dx) - F(x)}{Dx}$$

Figure 1a shows the results of a successful minimum-power test. The power is well above the -2-dBm limit and is well-behaved. The derivative data is also small. Figure 1b shows the same system when a connector is loose. In this case, the minimum power data is above the specification but is not well-behaved; in fact, a power hole appears. The power hole does not cause a failure in the minimum specified power, but remains a cause for concern for three reasons:

- a power hole results when a system problem in unstable with time, temperature, or shipping;
- as the loose connection moves, the null frequency may move in frequency, rendering subsequent calibrations useless;
- only a trained eye can determine from the plot that there is a failure.

You cannot determine the failure by simply looking at a pass/fail result. However, the derivative data from the power hole can generate a hard-fail indication.



In a well-behaved system (a), both the power data and its derivative are above the -2-dBm level. Tests of the same system with a loose connector (b) show that the power curve still doesn't dip below -2 dBm, but the derivative data indicates the existence of a power hole.

The derivative of the data in **Figure 1b** is 10 times the derivative data in **Figure 1a**. If you set the pass/fail criteria for the derivative data at 5 dB/ Δx , the data from **Figure 1a** easily passes, and the data from **Figure 1b** fails.

You can use a small statistical base of measurements on different systems to set a qualified, statistical three-sigma limit on the derivative data. This limit will be insensitive to offset magnitude but will show point-to-point rate of change. Using the derivative data limits and the minimum power limits together will eliminate any chance of shipping an improperly functioning system to a customer. (DI #2360)

Reference

1. Application Note AN64-1, "Fundamentals of RF and Microwave Power Measurements," Hewlett-Packard Co, Palo Alto, CA.



μC-based circuit performs frequency multiplication

Yongping Xia, Teldata Inc, Los Angeles, CA

THE TRADITIONAL FREQUENCY multiplier requires many elements: a phase comparator to detect the phase error between the input and the output signals, a lowpass filter to convert the phase error to a dc control signal, a VCO to generate the output, and a divider to set up the multiple ratio. The circuit in **Figure 1** uses a different approach to multiply frequency with a programmable multiple ratio from 1 to 7 (**Table 1**). Because the circuit is edge-triggered, the 50% output duty cycle is independent of the duty cycle of the input waveform. Test results show that the output frequency-range is

		LISTING	1–FREQUENC	CY-MULTIPLI	ER CO	DE			
.include "1	200def.inc"				ср	number,		cemp_o	;
.device ATS						half_cnt			;
					add	cnt_2,		temp_3	;
.def	cnt =r16	;				dec_1			;
.def	temp 1 =r17	;			sub	cnt_1,		cnt_2	;
.def	temp_2 =r18	,			brco				;
.def	temp 3 = $r19$				subi			\$1	;
.def	temp 4 =r20				brcs	s cnt_under	flow		
		<i>.</i>		dec_1:					
.def		;			subi			\$1	
.def	temp_6 = r22	;			brco				
.def	number =r23	;				cnt_2,		\$1	
.def	pulse =r24	;				: int_out			
.def	delay_1 =r25	;		cnt_unde.	ldi	and 1		\$1	
.def	delay_2 =r26	;			ldi	cnt_1,			
.def	cnt_1 =r27	;		int out.	Tat	cnt_2,		Ş0 .	
.def	cnt_2 =r28	;		int_out:	ldi	number,	\$0		
		;			rjmp		ΨU		
reset:		;		half cnt		100b ⁻ 1			
	rjmp init	;		harr_chc	clc				
int:		;			ror	cnt 2			
	in temp 4,	PINB ;	read input		ror	cnt 1			
	andi temp 4,	\$07 ;	-		rjmp				
	mov temp_5,	temp 4;		init:	2 1 1.12	*ouc			
	mov temp 6,	temp 4;		2012-07	ser	temp 1			
	lsl temp 5	;			out	PORTB,		temp 1	
	lsr temp 6	<i>.</i>			out	PORTD,		temp 1	
		\$0 ;			ldi			\$0	
					out			temp_1	
	cp number,	temp_4;			ldi	temp 1,		\$1	
	brne next_1				out	DDRD,		temp 1	:
	ldi temp_2,	\$1 ;			ldi	delay 1,	\$ff		;
next_1:		;			ldi	delay 2,	\$ff		,
	dec temp_2	;			ldi	temp_1,		\$40	;
	breq next_2	;			out	GIMSK,		temp_1	;
	out PORTD,	pulse ;			ldi	temp_1,		\$3	;
	inc pulse	;			out	MCUCR,		temp_1	;
next_2:		;			ldi	pulse,		\$0	
	cp number,	temp_4;			ldi	number,		\$0	;
	brlo dec cnt	;			ldi	temp_3,		\$0	
	cp number,	temp 5;			in	temp_4,		PINB	
	brlo inc cnt	- ;				temp_4,		\$07	
	sec	;			mov			temp_4	
	rol cnt 1	;			mov	temp_6,		temp_4	
	rol cnt 2	,			lsl lsr	temp_5 temp_6			
	brcc int out				IST	cemp_o			,
ent overflo		,		loop_1:					; endless loop
	ldi cnt 1,	\$ff ;		1000-11	sei				, churess roop
	ldi cnt 2,	\$ff ;				dolor 1	art 1		•
	rjmp int out	, , , , , , , , , , , , , , , , , , ,			mov	delay_1,	cnt_1		, -
ing ont.	LIND THE OUL			1 0	mov	delay_2,	cnt_2		/
inc_cnt:	add ant 2	town 2.		loop_2:			<u>^</u> 1		; delay loop
	add cnt_2,	temp_3;			subi	delay_1,	\$1		;
	breq inc_1				brcc	loop_2			;
	add cnt_1,	cnt_2 ;			subi	delay_2,	\$1		;
	brcc inc_1	;			brcc	loop_2			;
	inc cnt_2	;			cli				;
	breq cnt_overflow	;			out	PORTD,		pulse	; send output
inc_1:		;			inc	pulse			;
	inc cnt_1	;			sbrs	pulse,		\$0	;
	brne int_out	;			inc	number			;
	inc cnt_2	;				loop 1			
	breq cnt_overflow	1			- Jt.				•
	rjmp int_out	1							
dec cnt:		;							

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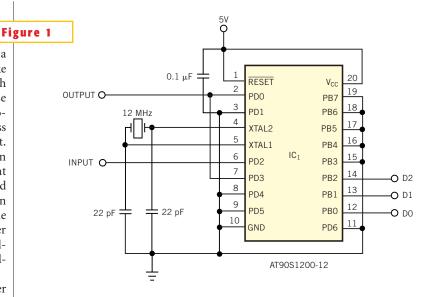


from 31 Hz to greater than 30 kHz.

The AT90S1200 is a low-cost, high-speed µC, and most instructions need only one clock cycle. With a 12-MHz clock, these instructions take 83.3 nsec. This number places the high limit on the input frequency because software performs all functions. The program in Listing 1 includes an endless loop to generate a square-wave output. The frequency of the output depends on the value of a 16-bit delay register that comprises two 8-bit registers: dly_1 and dly_2. The delay function is a countdown loop until it reaches zero. The larger the number in the delay register, the longer the delay time. The functions of the endless loop and the delay register are analogous to a VCO.

The AT90S1200 has an 8-bit counter whose input is the output signal. Because this counter is an up counter, the programmable multiple ratio loads into the counter in the 2's complement format. For instance, if the multiply ratio is four, the software loads that counter with 0xfc. Because the initial value of the counter

TABLE 1-FREQUENCY-MULTIPLIER SETTINGS					
D ₂	D ₁	D	Output frequency		
0	0	0	-		
0	0	1	x1		
0	1	0	x2		
0	1	1	х3		
1	0	0	x4		
1	0	1	х5		
1	1	0	х6		
1	1	1	х7		



A simple µC-based circuit can multiply frequency by 1 to 7.

is 0xfc, four output pulses cause the counter to overflow, which generates an interrupt. The function of this counter is analogous to the divider in a traditional frequency multiplier.

> Every rising edge of the input signal also generates an interrupt. Thus, the interrupt subroutine must identify the events that trigger the interrupts. If the input causes the interrupt, the frequency of the output is too low. If the counter trig

gers the interrupt, the output frequency is too high. In both situations, the software must adjust the value of the delay register accordingly. The interruption subroutine is analogous to a phase comparator.

Listing 1 is available for downloading from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file DI #2362.

To Vote For This Design, Circle No. 331

Kick start a crystal oscillator in Spice

Adam Chen, Cypress Semiconductor, Woodinville, WA

Starting UP OSCILLATOR CIRCUITS and getting them to maintain oscillation in a Spice simulation is difficult. Some high-frequency crystal circuits require days for the oscillation to reach steady state. Thus, most designers separate the crystal's circuit simulation from the rest of the system design. How-

LISTING 1-SPICE NETLIST						
Co	xtalin	xtalout	4pf			
Ll	xtalxi	1	9.076mH			
C1	xtalout	3	13.613f			
Rl	1	2	25			
Vsin	2	3	sin(0 0.7k 14.318Meg 0.1n 8e+6 0)			



ever, a technique that gives a "kick" to an RLC equivalent circuit solves this problem. This method makes sure the simulation starts fast and quickly reaches the steady state.

Figure 1a shows the equivalent RLC circuit of a quartz crystal. Most clock chips, such as Cypress Semiconductor's (www.cypress. com) CY227x and CY228x families, have a crystal circuit similar to **Figure 1b**. The circuit comprises the crystal, an inverter/gain block, and a feedback network.

Conventionally, Spice uses an initial condition for the RLC resonator, such as setting the inductor initial current to a certain value, to start the simulation. The

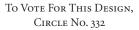
reference frequency of the most common

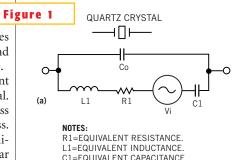
clock chips is 14.1318 MHz. The simulation takes a least a day to reach constant oscillation amplitude because high-Q resonators require long periods of time to reach a certain energy level.

The key to quickly starting this type of oscillator is giving a kick to the RLC equivalent circuit in the form of a highvoltage damped sinusoid that ultimately fades away. The frequency of this excitation is the expected frequency of the resonator. The source looks like a short circuit in the RLC circuit and does not alter any of the circuit's dc- bias conditions. **Figure 2** shows the simulation input/output waveforms, and **Figure 3** shows the excited sinusoidal voltage. The excited

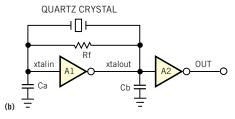
voltage is in the kV range because the voltages across L1 and C1 are in kV range when the LC tank is oscillating.

For a 14.318-MHz crystal, the equivalent circuit has Co=4 pF, C1=13.613 pF, L1=9.076 mH, and R1=25 Ω . The excited voltage source is a simple Spice sinusoidal voltage source, Vsin in **Listing 1**. The Vsin statement includes the damping factor. (DI#2357)



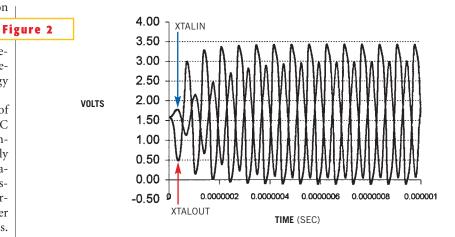


CI=EQUIVALENT CAPACITANCE. Co=INNER ELECTRODE CAPACITANCE. Vi=EXCITED SINUSOIDAL VOLTAGE SOURCE.

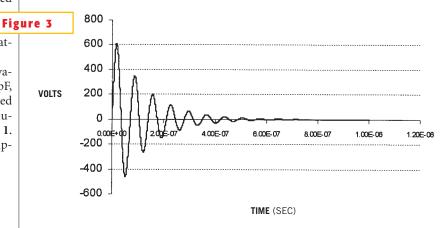


NOTES: Ca=Cb=34 pF, Rf=1M Ω . QUARTZ CRYSTAL=14.318 MHz. A1, A2 CMOS INVERTER.

The equivalent circuit of a quartz crystal (a) includes equivalent resistance, R1; inductance, L1; capacitance, C1; and inner electrode capacitance, Co. In addition to the crystal, clock chips include an inverter/gain block and a feedback network (b).







An excited voltage source in the RLC circuit ensures oscillation startup and then quickly fades away. Edited by Bill Travis and Anne Watson Swager

Missing-codes tester checks 16-bit ADC in 7 sec

ideas

Mark A Shill, Burr-Brown Corp, Tucson, AZ

s THE RESOLUTION OF ADCs increases from 12 to 16 bits and higher, the difficulty in testing the "nomissing-codes" specification grows proportionately. To fully guarantee no missing codes for a 16-bit ADC requires testing all $2^{16}-1$ possible output codes. Undertaking such a production test could add much extra cost to the ADC without a quick method for testing all codes. Fortunately, a simple approach can test the no-missing-codes specification for a 16-bit ADC—in this case, a 10-µsec ADS7805, in typically less than 7 sec (**Figure 1**).

This missing-codes tester comprises an analog ADC servo loop that you can also use to measure the integral nonlinearity and differential nonlinearity of 16-bit ADCs (**Reference 1**). The servo loop works by finding the ADC's input voltage that corresponds to the Code_i-to-Code_{i+1} output transition. The circuit uses an 18-bit DAC729, IC_1 , as a pedestal DAC to quickly set the input voltage to the ADC

Missing-codes tester checks 16-bit ADC in 7 sec11	3
Switch-mode supply draws 43-mW standby power	6
Circuit rejects ambient light11	8
V/I converter accommodates grounded load12	0
Digitally controlled potentiometer sets cutoff frequency12	2
Precision reference bans precision resistors12	4
Easy method calculates comparator trip points12	4
EDN selects 1998 Design Ideas grand-prize winners	8

under test to approximately the level corresponding to the programmed input code. The output transfer function of the pedestal DAC matches the transfer function of the ADC under test—in this case, $\pm 10V$ for the ADS7805. The DAC729 MSB bit-adjustment pins, pins 36 to 40, are open because the unadjusted DAC729's linearity is sufficient for performing only the ADC missing codes test.

The procedure successively tests each possible output code of the ADC under test by programming a PC with the desired 16-bit code, Code, Applying a 100kHz clock to pin 24 of the ADC provides for continuous operation of the ADS-7805. When the ADC completes a conversion, two 8-bit 74HC682 magnitude comparators, IC₂ and IC₃, and accompanying interface logic, IC₄ and IC₅, compare the ADC's output code to the programmed data-bus code. The signal output from IC_{4A} signifies whether the input voltage to the ADC needs to increase or decrease to achieve an ADC output equal to the programmed Code. The signal from IC4B indicates whether the output code from the ADC matches Code; a logic-low level indicates that the code was found.

Because both the $\overline{P>Q_{16}}$ and $\overline{P=Q_{16}}$ signals from IC_{4A} and IC_{4B}, respectively, can be momentarily indeterminate during the ADC conversion, the circuit latches these signals into flip-flops IC₆ and IC₇ when the conversion is complete. The clock signal for these latches is a delayed version—approximately 200 nsec—of the rising edge of the ADS7805 end-of-conversion signal, BUSY. The circuit uses the $\overline{P>Q_{16}}$ signal clocked into IC₆ to control the ramp direction of integrator op amp IC₈. The 0 to 5V output of HC-type flip-flop IC₆ directly drives the integrator

input of IC₈. R₁, R₂, and the -15V power supply shift the 0 to 5V output level to approximately -2 to +2V. C₁ filters any high-speed transients that arise from the switching action of IC₆'s output.

Op amp IC_o attenuates the integrator's output by 100 and sums the result with the output of the pedestal DAC. For the component values of IC_s's integrator stage, the maximum ramp rate at the input of the ADC is approximately 2 μ V/ μ sec, which is equivalent to 0.067 LSB per conversion. Feedback of the servo-loop circuit maintains the dc level of the integrator's output by continuously adjusting the input voltage of the ADS7805 to the level required for the $Code_i$ -to- $Code_{i+1}$ output transition. Thus, the servo-loop circuit locks in the input voltage to the ADC to maintain the Code_i-to-Code_{i+1} output transition.

The $\overline{P=Q_{16}}$ signal that the circuit clocks into flip-flop IC₇ indicates whether the programmed Code_i exists for the ADC under test. The output of IC₇ connects to an input control line, CNTL₆, on the controlling PC's I/O card. After the control program sends each new Code_i to the tester, the PC reads the state of CNTL₆. A high level on CNTL₆ indicates that Code_i exists and is not missing.

ALIGN PEDESTAL DAC WITH ADC UNDER TEST

Before starting the missing-codes test, the procedure requires alignment of the pedestal DAC's endpoints with those of the ADC under test. This alignment ensures that the pedestal DAC's output closely matches the corresponding ADC input voltage for all codes programmed to the tester. Under this condition, the voltage needed to sum with the pedestal DAC output should be only a few LSBs (referred to the ADC input), thus keeping the dc output level of the integrating op



amp, IC_{s} , close to 0V. Thus, for each Code_i setting, the integrator output never needs to slew very far from the dc level of 0V.

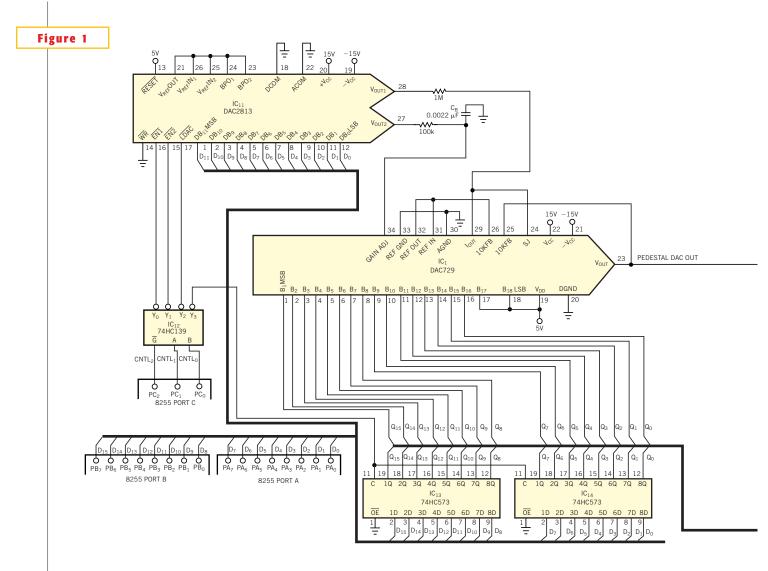
Comparators IC_{10A} and IC_{10B} form a window comparator for the output of IC₈. The window voltage is equal to 100 mV, which corresponds to approximately 3.3 LSBs, referred to the ADS7805 input. I/O control lines CNTL₄ and CNTL₅ read the outputs of IC_{10A} and IC_{10B}, respectively to determine the level of the integrator's output voltage. If CNTL₄ is high, the integrator output is more than 100 mV. If CNTL₅ is high, the integrator is less than -100 mV. If both CNTL₄ and CNTL₅ are low, the integrator output is

within the 100-mV window.

A dual, 12-bit latched DAC, IC_{11} , adjusts the pedestal DAC's endpoints. V_{OUT1} and V_{OUT2} adjust the pedestal DAC's offset and gain, respectively, to the endpoints of the ADC under test. First, the control program adjusts the DAC729's offset by programming and latching Code_i to FFFE (hex) and then counting up or down accordingly so that V_{OUT1} brings the integrator voltage within the 100-mV setting of the window comparator. Next, the program sets IC_1 's gain by programming and latching Code_i to unting up or down so that V_{OUT2} brings the integrator output to a null.

The same I/O data bus programs both the DAC2813 and the 74HC682 digital comparators. The 74HC139 decoder, IC₁₂, selects either the input Code₁ latches, IC₁₃ and IC₁₄, or the internal latches of the DAC2813. IC₁₁ has two input-latchenable pins, one for each of its output DACs. Input <u>LDAC</u> loads the DAC's input latch data into the internal latches, thus simultaneously programming both V_{OUT1} and V_{OUT2} . I/O control lines CNTL₀ and CNTL₁ select the desired latch, and CNTL₂ strobes in the data from the bus.

The listing of the Pascal program for controlling the missing-codes tester is available for downloading from *EDN*'s



An analog servo loop tests for no missing codes by finding the ADC's input voltage that corresponds to the Code, to-Code, output transition.

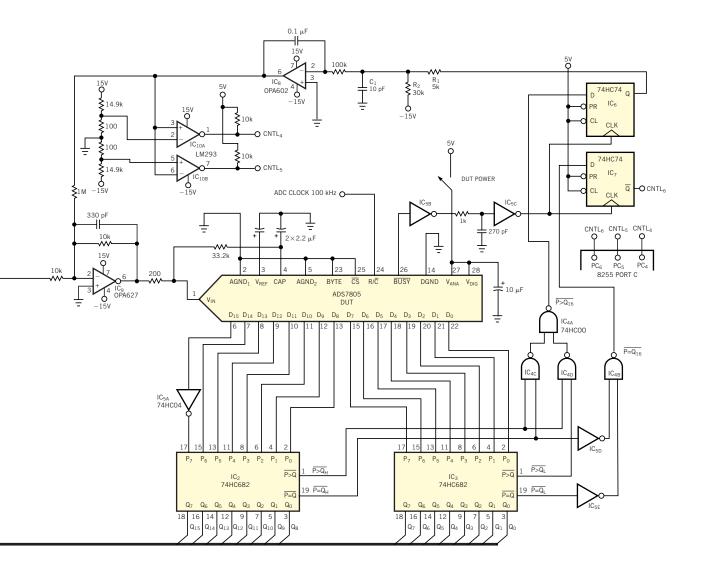
web site, www.ednmag.com. Click on "Search Databases/Links Page" and then enter the Software Center to download the file for Design Idea #2334. The section of the program that outputs codes to the data bus and reads the state of the CNTL₆ line is based on a custom I/O card built with an Intel 8255A programmable peripheral interface. The I/O routines are for reference only, and you should modify them according to the protocol used by the user's specific I/O card.

The EndPoints procedure in the listing aligns the offset and gain of the pedestal DAC to that of the ADC under test. It programs IC_{11} as necessary to null the in-

tegrator output for both offset and gain. The Detect procedure programs each Code, from 0 to 65534, to the missingcodes test board. After programming each new code, the program reads the state of the CNTL, line. If CNTL, is a logic high, indicating the programmed code exists, the Count variable is incremented. The Detect procedure loops for the given code until a minimum number of occurrences are detected, set by the variable MinCount. The variable MaxTry sets the maximum number of times that the program trys to find Code. The program loops for an appropriate delay time to ensure that measurements of the state of the line occur only once per analog-todigital conversion or, in the case of the ADS7805, approximately every 10 μ sec. For the variable MinCount set to 3 and MaxTry set to 30, the missing-codes tester can test the 10- μ sec ADS7805 for all 2¹⁶-1 codes in less than 7 sec. (DI #2334)

Reference

1. Shill, Mark A, "Servo loop speeds tests of 16-bit ADCs," *Electronic Design*, Feb 6, 1995, pg 93.





Switch-mode supply draws 43-mW standby power

Christophe Basso and François Lhermite, Motorola SPS, Toulouse, France

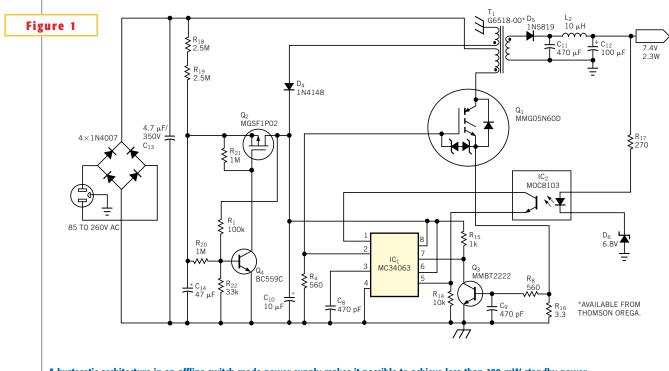
NUTCH-MODE OFFLINE SUPPLIES OFfer better efficiency than linear supplies. However, the efficiency of a switchmode power supply (SMPS) seriously degrades with light loads, and commutation losses provoke power dissipation well above 1W even with no load. A good way to build a low-standby-current SMPS is to use a hysteretic architecture, which delivers high-frequency pulses until the output passes a threshold and then no pulses until the output again drops below the threshold. The SMPS consumes little energy delivering the refreshment pulses. Figure 1 shows a circuit that uses an MC34063 controller IC and an insulated-gate bipolar-transistor (IGBT) output device.

The MC34063 operates in current

mode. Q₃ trips the IC when the voltage on sense resistor R₁₆ drops to approximately 550 mV. (I_{PEAK} =160 mA in this example.) You can adjust the peak current to compensate for the transformer's magnetorestrictive effects. Any transformer you use in an SMPS produces audible noise at a low frequency. You can either buy an expensive transformer whose construction ensures low audible noise or keep peak current low, as in Figure 1's circuit. When reducing the peak current, you need to increase either the primary inductance or the switching frequency (by varying C_{\circ}) to keep the output power constant.

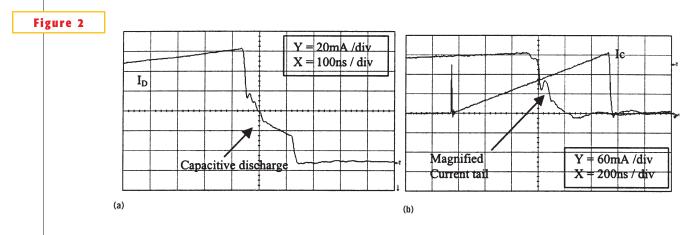
The MMG05N60D IGBT has low parasitic capacitance that degrades efficiency at low peak currents. When you open the high-voltage switch in a MOSFETbased flyback converter, the peak current does not immediately drop to zero. Depending on the amount of parasitic capacitance, the current keeps circulating while the drain voltage rises, and efficiency suffers. **Figure 2a** illustrates this wasteful behavior in a high-voltage, MOSFET-based switcher. The MMG-05N60D IGBT has low parasitic capacitance; its total gate charge at V_{GS} =10V is only 4 nC. **Figure 2b** shows the current in **Figure 1**'s circuit with zero output power.

The start-up circuit for the MC34063 uses Q_4 and Q_2 . When you apply the power main, the voltage on C_{14} starts to rise. The ratio of R_{20} and R_{22} causes Q_4 and Q_2 to remain open. The IC receives



A hysteretic architecture in an offline switch-mode power supply makes it possible to achieve less-than-100-mW standby power.





The turn-off characteristic of a lateral MOSFET (a) results in significant wasted power in a no-load condition; lower parasitic capacitance in an IGBT leads to lower dissipation during the turn-off period.

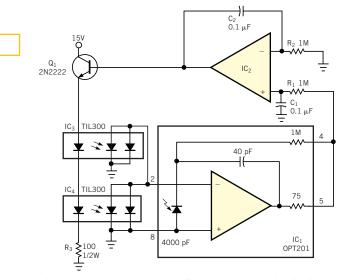
no power, and the current that flows in from C_{14} is small. When the voltage reaches a threshold, Q_4 starts to conduct and pulls Q_2 's gate toward ground. Q_2 's drain voltage rises and strengthens the conduction in Q_4 . C_{14} rapidly discharges into C_{10} , and the MC34063 oscillates. The circuit offers efficiency ranging from 59.4 to 73%. It dissipates no-load power levels of 42.5, 65, and 82.8 mW at dc input voltages of 120, 325, and 360V, respectively.(DI #2363).

> To Vote For This Design, Circle No. 416

Circuit rejects ambient light

Massimo Gottardi, IRST, Trento, Italy

N SOME APPLICATIONS, you need to detect light signals in the presence of background light whose in-**Figure 1** tensity can change by orders of magnitude. The circuit in Figure 1 uses an integrated photodiode/amplifier (OPT201) in conjunction with an integrator that drives two linear optocouplers (TIL300). The optocouplers subtract the background-light-generated current from the current the optical sensor produces. C2 integrates any dc signal present at the output of IC₁. The output of IC, drives two optocouplers, IC, and IC₄. The four photodiodes in both TIL300s connect in parallel with the diode in the OPT201 to subtract the dc component from the signal path. IC, and IC4 need 60-mA drive to produce rejection current as high as 1.5 mA. This design uses the optocoupler configura-



The two optocouplers use input-series, output-parallel connections to halve the driving current and double the output rejection current.



tion instead of a simple resistor, because the optocouplers' nonlinear characteristic allows a higher current range without substantially affecting the noise gain of the transimpedance amplifier. The total output noise in the circuit is 80 μ V rms. A 6.8-k Ω resistor can reject the same 1.5-mA dc current, but it produces 200-

μV output noise. (DI #2364).

To Vote For This Design, Circle No. 417

V/I converter accommodates grounded load

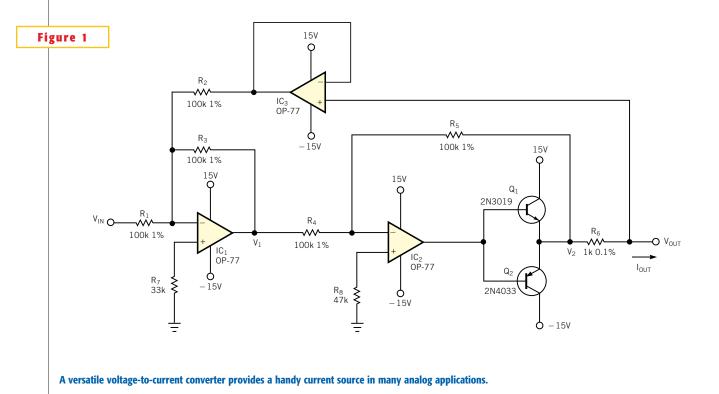
Michele Frantisek, Brno, Czech Republic

The voltage-to-current (V/I) converter in **Figure 1** uses three common op amps, two medium-power transistors, and only a few passive components. The first op amp (IC₁) inverts the sum of voltages V_{IN} and V_{OUT} to V_1 =-(V_{IN} + V_{OUT}). The second op amp (IC₂) and transistors Q_1 and Q_2 invert this voltage to produce V_{IN} + V_{OUT} . The formula for calculating the output current is thus:

$$\begin{split} I_{OUT} &= \frac{V_2 - V_{OUT}}{R_6} = \\ \frac{V_{IN} + V_{OUT} - V_{OUT}}{R_6} = \frac{V_{IN}}{R_6}. \end{split}$$

The formula shows that the value of I_{OUT} depends only on V_{IN} and R_{e} . Voltage follower IC₃ reduces to a negligible level the current from the circuit output to IC₁. The advantages of the circuit are:

- load-grounding possibility;
- simple control of I_{OUT}/V_{IN} ratio;
- high precision, linearity, stability, and bandwidth;
- wide I_{OUT} range, approximately 1 μA to I_C(max) of Q₁ and Q₂; and
- high output resistance of approximately 50 MΩ. (DI #2365). To Vote For This Design, Circle No. 418





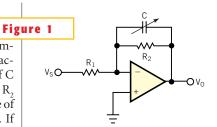
Digitally controlled potentiometer sets cutoff frequency

Chuck Wojslaw, Xicor Inc, Milpitas, CA

The TRADITIONAL METHOD of controlling the upper cutoff frequency in the basic inverting-amplifier circuit of **Figure 1** is to add capacitor C in parallel with R_2 . The value of C controls the cutoff frequency. R_1 and R_2 independently establish the magnitude of the circuit gain, which equals R_2/R_1 . If you need a variable cutoff frequency, you use a variable capacitor. However, this approach has two major problems: The circuit does not lend itself to computer control, and few variable capacitors are available with values in the nanofarad region.

The circuit in **Figure 2a** is an inverting amplifier that uses a digitally controlled potentiometer and a fixed capacitor as an input Tee network. The magnitude of the gain for this inverting circuit is also R_2/R_1 . However, in this case, R_1 , C, and the location of the wiper along the resistor array of the potentiometer establish the cutoff frequency. The upper cutoff frequency is programmable because the wiper of the potentiometer is under digital or computer control.

Several analysis approaches help determine the circuit gain as a function of frequency. One approach is to use y, or admittance, parameters. If you treat networks A and B as two ports (**Figure 2b**), the ratio of the short-circuit admittance coefficient for the input port, y_{21A}, to y_{12B}



Controlling the cutoff frequency using a traditional inverting amplifier circuit has some limitations, such as a limited selection of variable capacitors.

for the feedback port produces the following gain expression:

$$\frac{V_{O}}{V_{S}} = -\frac{y_{21A}}{y_{12B}} = -\frac{\left(\frac{R_{2}}{R_{1}}\right)\left(\frac{1}{R_{1}Ck(1-k)}\right)}{j\omega + \frac{1}{R_{1}Ck(1-k)}}.$$

In this equation, k is a number that varies from 0 to 1 and reflects the proportionate position of the wiper from one end of the potentiometer (0) to the other end (1).

The circuit's gain expression is

$$\frac{V_{O}}{V_{S}} = \frac{A_{o}\omega_{C}}{j\omega + \omega_{C}}.$$

This equation has the same form as an equation for an amplifier or lowpass filter with a gain of $-R_2/R_1$ and a cutoff frequency of

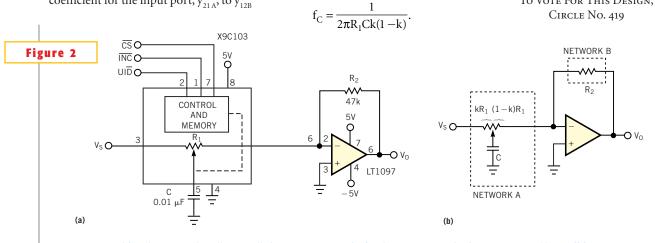
As you program the wiper from one end of the potentiometer to the other, k varies from 0 to midscale $(^{1}/_{2})$ to 1, and the cutoff frequency varies from infinite hertz to a minimum frequency and back to infinite hertz. The minimum frequency is

$$f_{C(MIN)} = \frac{4}{2\pi R_1 C}$$

For the XDCP family of digitally controlled potentiometers (Xicor Inc, www. xicor.com), k can vary from 0 to 1. The number of taps or programmable wiper positions determines the resolution. R_1 represents the R_{TOTAL} of the potentiometer. The number of taps varies from 32 to 256, and R_{TOTAL} varies from 1 k Ω to 1 M Ω , depending on the potentiometer. The potentiometer can store a wiper or cutoff-frequency setting in nonvolatile memory, which permits the circuit's cutoff frequency to return to a predetermined value on power-up.

For the circuit in **Figure 2a**, gain is 4.7, and the cutoff frequency varies from 6.4 kHz to a theoretically infinite hertz. The circuit uses a 10-k Ω potentiometer, the X9C103, which has 100 taps and a threewire interface. The circuit is useful for audio, control, and signal-processing applications. (DI #2367)

To Vote For This Design,



An inverting amplifier that uses a digitally controlled potentiometer and a fixed capacitor provides for a programmable cutoff frequency (a). You can analyze the circuit as a two-port network (b).

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Precision reference bans precision resistors

Budge Ing, Maxim Integrated Products, Sunnyvale, CA

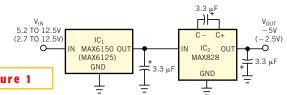
C OMBINING A SWITCHED-CAPACITOR charge pump with a precision reference yields an inverted reference from a positive power supply (**Figure 1**). Unlike the more typical combination of a positive three-terminal reference and an op-amp inverter, this circuit performs accurate inversions without the need for precision resistors and a negative supply. The compact circuit requires only three surface-mount capacitors, and the ICs occupy tiny **Figure 1**

SOT-23 packages.

The charge-pump inverter, IC_2 , delivers -5V by inverting the out-

put of a 5V precision reference, IC_1 . IC_1 has an input range of 5.2 to 12.5V. Replacing IC_1 with a 2.5V reference that accepts 2.7 to 12.5V inputs produces a – 2.5V output.

Output-voltage accuracy depends

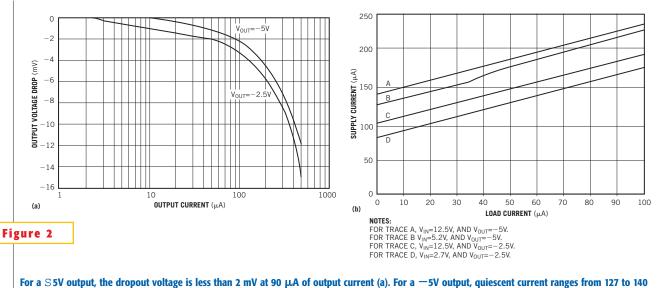


Combining a voltage reference and a charge-pump inverter forms a precision negative reference.

partly on the initial accuracy of IC₁, which in this case is 1%. To determine the overall accuracy, you must add the error from the dropout voltage, which is less than 2 mV for 90 μ A of load current (**Figure 2a**). For a – 2.5V output, the cir-

cuit draws quiescent current that ranges from 86 μ A for a 2.7V input to 105 μ A for a 12.5V input. For -5V outputs, the circuit draws 127 μ A for 5.2V inputs and 140 μ A for 12.5V inputs (**Figure 2b**). (DI #2368)

To Vote For This Design, Circle No. 420



μA.

Easy method calculates comparator trip points

Virgil Lawrence, Micro Linear, San Jose, CA

U SING MILLMAN'S THEOREM to calculate the resistor ratio reduces the time it takes to calculate the trip points on a comparator with hysteresis.

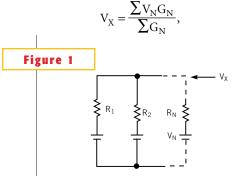
This method eliminates lengthy computations and substitutions. Using this resistor ratio, you select two resistors, assign convenient values, and then calculate the third value.

Assume an inverting comparator with an upper limit of 4V and a lower trip voltage of 1.333V. The voltage on the in-



verting input needs to reach 1.333V for the output to switch to V_{CC} . Then, for the output to return to zero, the input voltage needs to reach 4V.

Millman's Theorem states that the sum of the products of the voltages times their respective conductances divided by the sum of the conductances gives the common junction-point voltage V_x (**Figure 1**). Or,



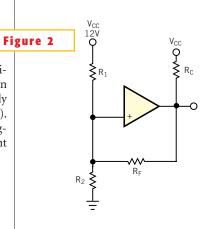
Millman's theorem states that the sum of the products of the voltages times their respective conductances divided by the sum of the conductances gives the common junction point voltage V_{x^*}

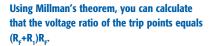
where Gt1/R.

Using Millman's Theorem, with V_{CC} at the top of R_1 and R_F (Figure 2), set up the numerator with a Millman equation. Set up the denominator with another Millman equation when the output voltage is zero (with only one voltage source in the denominator). Assume that R_C is $\mathbb{I}R_F$ and therefore negligible in the calculations. The resultant equation for the voltage ratio is:

$$V_{\text{IN(HIGH)}} = \frac{\frac{\sum V_N G_N}{\sum G_N}}{\frac{\sum V_N G_N}{\sum G_N}} = \frac{\frac{12}{R_1} + \frac{12}{R_F}}{\frac{12}{R_1}}$$
$$= \frac{R_F + R_1}{R_F} = \text{VOLTAGE RATIO}.$$

This large fraction equals the voltage ratio 4/1.333 B. First solve for R_p in terms of R_1 , and select R_1 in relation to R_p , such as R_1 tl M Ω , and R_p 500 k Ω . Then solve for R_2 . The resistance ratio always equals the voltage ratio minus one. (DI #2372)





designic des

Edited by Bill Travis and Anne Watson Swager

Controller supports differential monitor display

William Grill, Riverhead Systems, Littleton, CO

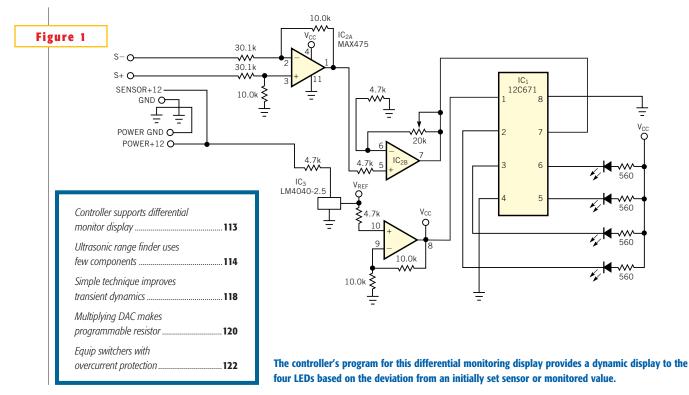
OU CAN ASSEMBLE A DIFFERENTIAL monitoring display using rail-to-rail analog hardware and a 12C671 eight-pin controller (Microchip Technology, www.microchip.com) (Figure 1). The controller, IC₁, reads the scaled analog input reference into its internal ADC at an approximately 3-msec rate. The controller's program provides a dynamic display to the four LEDs based on the deviation from an initially set sensor or monitored value. The "rolling" display moves from end to end at a rate based on the direction and magnitude of the deviation. You can download the accompanying program from EDN's Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2373.

To use the circuit, you apply the reference level and adjust the gain at Pin 7 of IC_{2R} to bring the display to an "all-lite" condition. This adjustment artificially sets the reference to half of the internal ADC's span. The absolute value of the deviation about this reference setting is scaled into eight equal steps above and below this fixed reference to the limits of the converter. For a 5V application, this results in approximately 0.31V indexes ((5/2)/8). The circuit passes the resulting index to a rate table, which sets the display update period. A second index pointer increments each time the display's update period times out. Positive deviations from the reference increment this mask pointer, and negative deviations decrement the pointer. This second pointer then indexes through a mask table, which defines the display's pattern.

The controller uses 127 bytes of code with the eight-step rate table, the relatively small display, and the related 7-byte mask sequence. A stable reference, IC_3 , reduces the display's drift over time and temperature.

Although this format is too inflexible to use for all types of monitoring, you could add filtering and span and offset adjustments to provide a more flexible deviation display. You could also implement an expanded display using a 16C710 μ C (MicroChip Technology), an external PLD, or one of several 74xx decoders. (DI #2373)

> To Vote For This Design, Circle No. 395



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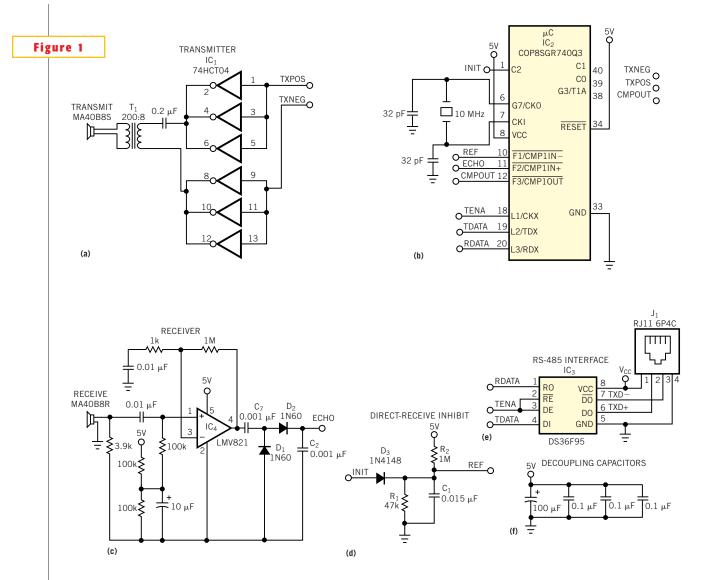


Ultrasonic range finder uses few components

Daniel R Herrington, National Semiconductor, Arlington, TX

N ULTRASONIC, OR SONAR, range finder is a common sensor in robotic systems and industrial environments. Even home and automotive uses are possible. A novel sensor design consists of a μ C, a few peripheral components, and a pair of ultrasonic transducers (**Figure 1**). The range-finder module consists of a μ C, a transmitter, a receiver, a direct-receive inhibit circuit, and an RS-485 interface. The module's usable range is approximately 4 in. to 16 ft with an accuracy of approximately ±2 in. This performance is sufficient for many industrial, automotive, and robotic uses.

Measuring distance with ultrasonic signals requires a transmitting ultrasonic transducer; a medium, such as air or water; a reflecting surface or object; a receiving ultrasonic transducer; and a time-of-flight measurement circuit. The



The range-finder module consists of five main subcircuits: a transmitter (a), a μ C (b), a receiver (c), a direct-receive inhibit circuit (d), and an RS-485 interface (e), in addition to the requisite decoupling capacitors (f).

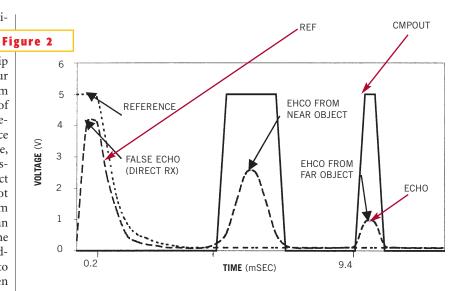
design**ideas**

speed of sound in air at 20°C is approxi-

mately 343m/sec, which translates to about 1 in. per 74 µsec. Doubling the time gives you the round-trip speed, which is 1 in. per 148 µsec. Four aspects of the system limit the maximum measurable distance: the amplitude of the sound wave, the texture of the reflecting surface, the angle of the surface with respect to the incident sound wave, and the sensitivity of the receiving transducer. The receiving transducer's direct reception of the sonar pulse-and not the echo-usually dictates the minimum measurable distance. Although you can use a discrete timer circuit to measure the time of flight, a µC can simplify the hardware design. Using a µC makes it easy to store and serialize the data and then transmit it to a PC or other master controller. The COP8SGR µC from National Semiconductor (www.national.com) includes peripheral blocks, such as timers, analog comparators, and a hardware UART. These peripherals reduce the amount of external hardware or internal software necessary to process the sensory data.

In **Figure 1**, the μ C, IC₂, waits for an "address" from a host controller over the RS-485 interface. When it receives the correct slave address, IC, begins a 250µsec pulse of 40 kHz to the ultrasonic transmitter circuit. The µC outputs a high INIT signal to charge C₁. During the transmit pulse, IC, drives audio transformer T₁ in a push-pull manner to generate about 40 to 50V p-p across the transducer. In Figure 1, the transmit and receive transducers are the matching MA40B8S and MA40B8R (MuRata, www.murata.com), respectively. At the end of the transmit pulse, the μ C brings the INIT line low again and C₁ discharges through R₁ to the level that voltage divider $R_1/(R_1+R_2)$ dictates. D_3 keeps the current from flowing back into IC,'s PORTC2 (INIT) pin.

The circuit uses the decaying voltage on the REF signal as a reference for the incoming echo (**Reference 1**). Op amp IC_4 amplifies the echo from the receive transducer. After amplification, D_1 and D_2 rectify the signal to a positive voltage. C_2 smoothes the resulting signal, and the circuit sends this preprocessed echo sig-



By comparing the ECHO and REF signals, the range-finder circuit effectively inhibits the largeamplitude receive signal at time t=0.2 msec.

nal to IC_2 's onboard analog comparator.

The CMPOUT signal feeds back into IC₂'s T1A pin to perform an input-capture operation on the result of the comparison. A positive edge on the T1A pin causes IC₂'s Timer 1 to latch the current countdown value in microseconds. Subsequent scaling reduces the 16-bit measurement in microseconds to an 8-bit value that represents distance in inches. The circuit transmits this 8-bit value back over the RS-485 interface, IC₃, to the host controller.

An assembly-code program performs all of the software processing necessary for ultrasonic distance measurement. The program is available for downloading from *EDN*'s web site, www. ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2371.

Figure 2 shows an example of the three waveforms: REF, ECHO, and CMPOUT. The comparison of the ECHO and REF signals effectively inhibits the large-amplitude signal received directly from the transmitter at time t=0.2 msec. This method allows the minimum measurable distance to be as low as approximately 4 in. This method also eliminates the need for an ADC, as well as the problems associated with defining a threshold value based on some moving average of echo samples.

You can improve the module by adding multiple-echo-detection capability, which allows a single transmitted ultrasonic pulse to recognize two or more objects at different distances (Figure 2). You can also incorporate this capability by having the program store the capture value for the first echo, at time t=5 msec, for example, and then re-enable the input-capture countdown and wait for the second capture at time t=9.4 msec, and so on. Another possible improvement is to add servo control to the circuit using one of the internal timers in mode. You can control hobby servos that you commonly find in radio-controlled toys with a 1- to 2-msec-wide positive pulse every 20 msec. In PWM mode, the μ C's timers require the loading of only a high width value and a low width value to generate this type of output signal. If you add servo control, you can use the sonar module to measure distance in a given direction. (DI #2371)

Reference

1. Ultrasonic Sensor Application Manual, MuRata Electronics North America Inc, Smyrna, GA, www.murata.com.



Simple technique improves transient dynamics

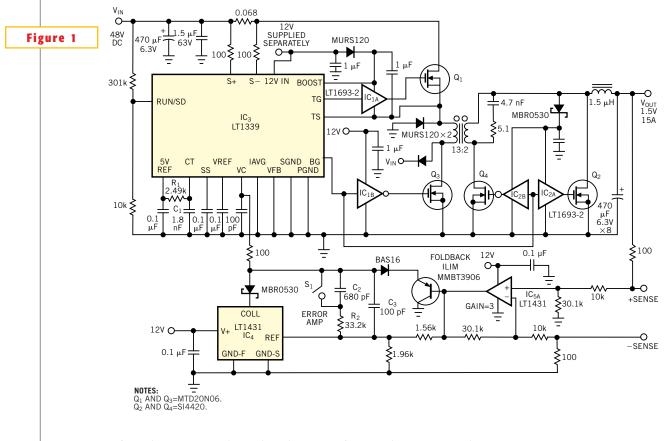
Robert Sheehan, Linear Technology Corp, Milpitas, CA

ESIGNING LOW-VOLTAGE, high-current converters with fast dynamic performance places stringent demands on a system designer. However, a simple technique reduces the peak voltage deviation and decreases the response time for a transient load step (Figure 1). This circuit converts 48V dc to 1.5V at 15A using a two-transistor forward converter with synchronous rectifiers. Q, and Q₃ are primary-side switches. Q₂ and Q_1 are the secondary-side rectifiers. IC₁ and IC₂, a pair of dual MOSFET drivers, provide the gate drive. The circuit derives the power for IC_2 by rectifying the peak secondary voltage. This feature, which allows IC, to operate with a 6V supply instead of a 12V supply, reduces gate-drive losses without any significant increase in rectifier conduction losses. IC₃, a highpower, synchronous switching-regulator controller, is at the heart of the PWM control. R_1 and C_1 set the oscillator frequency to just under 200 kHz and limit the maximum duty cycle to 50%.

 IC_4 , a programmable reference, functions as an error amplifier, overriding IC_3 's internal g_m amplifier. This design feature allows for greater control in tailoring the frequency-response characteristics and provides much greater accuracy. You can implement an added feature for output-voltage programming using the summing junction at the REF pin node. Differential amplifier IC_{5A} allows real remote sensing of the output voltage and makes it possible to produce output voltages well below the 2.5V reference of IC_4 .

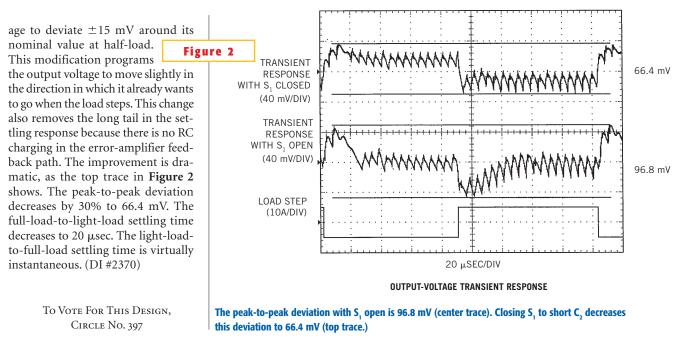
The circuit configures C_2 , R_2 , and C_3 in a classic Type 2 feedback-amplifier network. The center oscilloscope trace in **Figure 2** shows the response to a 100-nsec load step of 5 to 15A (100A/µsec). The peak-to-peak deviation is 96.8 mV with a settling time of approximately 40 µsec.

Modifying the feedback network can produce significant improvement. Shorting C_2 with S_1 limits the dc gain of the error amplifier, causing the output volt-



A two-transistor forward converter, Q_1 and Q_3 , with synchronous rectifiers Q_2 and Q_4 converts 48V dc to 1.5V at 15A.

designideas



Multiplying DAC makes programmable resistor

Albert O'Grady, Analog Devices Inc, Limerick, Ireland

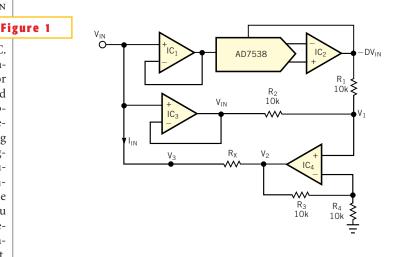
IGURE 1 SHOWS A CONFIGURATION that implements a digitally programmable resistor using a quad op amp and a multiplying DAC. The circuit is equivalent to a voltage-controlled resistor. The simulated resistor has a value that reflects the ratio of a fixed resistor (R_v) and a control voltage. Applications include generating precise resistance values for remotely controlling monostable multivibrators and configuring voltage-controlled loads in simulation circuits. The circuit provides linear control of resistance using the AD7538 14-bit multiplying DAC. You can obtain logarithmic control of the resistance by using an AD7111A logarithmic DAC as the voltage-control element.

Analysis of the circuit in **Figure 1** reveals the following:

$$V_1 = V_{IN} - \left(\frac{R_2}{R_1 + R_2}\right) (V_{IN} + DV_{IN}),$$

where D is input code to the multiplying DAC.

$$V_2 = 1 + V_1 \left(\frac{R_3}{R_3 + R_4} \right).$$



A multiplying DAC implements a linear, digitally programmable resistor.

If
$$R_1 = R_2 = R_3$$
, then
 $V_2 = V_{IN} - DV_{IN}$,
 $I_{IN} = \frac{V_{IN} - V_2}{R_X} = \frac{DV_{IN}}{R_X}$, and
 $R_{IN} = \frac{V_{IN}}{DV_{IN}/R_X} = \frac{R_X}{D}$.

The circuit in Figure 1 operates as a

voltage-controlled current source. You can adapt it for use as a basic functional block in the design of a biquad filter. In the adaptation, you modify the circuit to provide a voltage-controlled capacitor rather than a resistor. (DI #2384).



Equip switchers with overcurrent protection

Robert N Buono, Buono Consulting, Ringwood, NJ

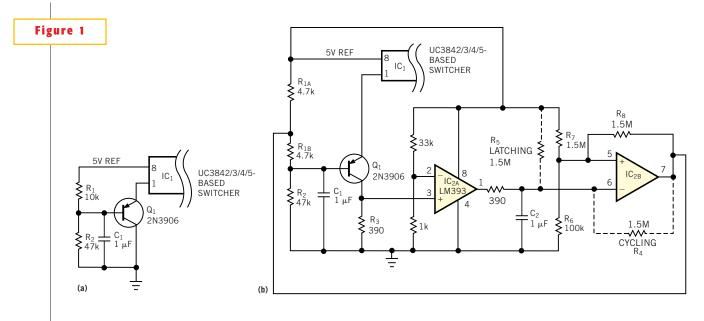
VERCURRENT PROTECTION IS USUAlly a necessary design feature of a switch-mode power supply to safeguard both the switcher and the load. Most PWM control ICs have internal overcurrent-protection circuits, and you can typically add auxiliary circuits around the IC to enhance this protection. For example, simple circuits enhance the operation of the common family of UC3842/3/4/5 (Unitrode Corp, www. unitrode.com) PWM-control ICs (Figure 1). These circuits allow the switcher to respond to an overcurrent fault condition by latching off if the overcurrent condition persists for more than some defined time interval or by cycling off and then on again at a low duty cycle until the fault clears. When the fault clears, the switcher then resumes normal operation on the next restart cycle. You can add these circuits without affecting other desirable features that the PWM IC may already include, such as soft start and maximum current-limit clamping.

In most switcher designs, operation in current limit imposes the greatest stress on the power devices. Therefore, decreasing the time that the switcher must operate in current-limit mode can enhance the reliability of the switcher. In some cases, decreasing this time may even result in reduced heat-sinking requirements for the power devices. A design that doesn't permit sustained operation in current-limit mode can have a lower average power dissipation than a design that permits a longer time in current-limit mode.

The circuits function solely by manipulating Pin 1 of the PWM IC; the schematics omit all other details of the PWM IC because the remainder of the IC's operation stays the same. In the UC384x family of control ICs, Pin 1 is the output of the internal error amplifier. The voltage at Pin 1 controls and is directly proportional to the peak current level in the main power-switching transistor. Therefore, Pin 1 is a logical place to exert control of the switching current.

The circuit in **Figure 1a** is a commonly used network that adds a slow-start feature as well as maximum current-limit clamping to the PWM- control circuit. The IC's internal error amplifier sources only a limited amount of current, typically 0.8 mA. Therefore, pnp transistor Q_1 easily clamps the voltage at Pin 1 to 0.6V higher than the voltage at its base by diverting the current from Pin 1 through its collector to ground. Thus, the voltage divider of R_1 and R_2 determines the clamping voltage at Pin 1. This voltage sets the maximum current limit of the main power-switching transistor.

A logical conclusion is that adding a capacitor, C_1 , from the base of Q_1 to ground will allow a ramp-up characteristic for the clamped voltage at Pin 1 and, therefore, will allow an analogous ramp-up characteristic for the power-switch current. This ramp-up characteristic is usually a desirable feature for initial switcher start-up because it allows the



Manipulating Pin 1 of a UC384x switcher allows you to add more overcurrent protection (a). A dual-comparator circuit allows for cycling or latching off when the switcher is in current-limit mode (b).



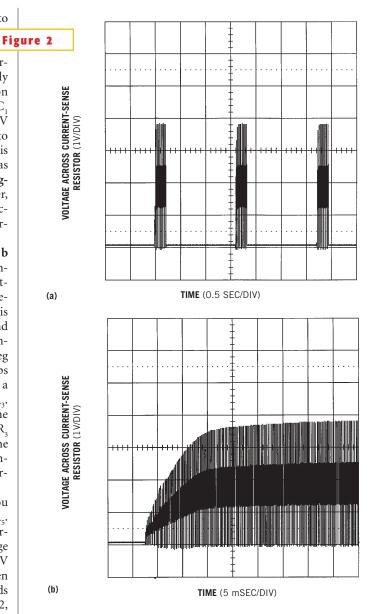
switcher's output voltage to

ramp up in a controlled manner, reducing output-voltage overshoot. The 5V REF supply in **Figure 1** is a precision voltage reference that IC₁ develops internally. This 5V REF is commonly used to power auxiliary circuits; this output delivers as much as 20 mA. The circuits in **Figure 1** are very low-power, and draw only a small fraction of that available current.

The design in Figure 1b adds a low-cost, dual-comparator circuit to the network at Pin 1. R, and C, remain the same, but this circuit splits R₁ into R_{1A} and R_{1B}. R₃ is an additional component in the collector leg of Q₁. Whenever Q₁ clamps the output of IC_1 's Pin 1, a voltage develops across R₃. This voltage indicates the onset of current limiting. R, does not interfere with the soft-start and maximumcurrent-limit clamp performance.

Cycling occurs when you install R_4 and remove R_5 . When the switcher is in current-limit mode, a voltage of approximately 400 mV develops across R_3 . When the voltage across R_3 exceeds the voltage at IC_{2A} 's Pin 2, which is approximately 150 mV, the output at IC_{2A} 's Pin 1 becomes an open-collec-

tor output and allows C_2 to charge through R_4 . The time it takes for C_2 to charge from approximately 0V to the threshold established at IC_{2B} 's Pin 5 is the "fault-delay time." During fault-delay time, the switcher remains on and in current-limit mode. IC_{2B} functions as a lowfrequency oscillator with low duty cycle. When the voltage on C_2 exceeds the voltage on IC_{2B} 's Pin 5, the open-collector output of IC_{2B} switches low. This low level pulls the base of Q_1 to ground through R_{1B} , and the voltage at Pin 1 of IC_1 clamps





to approximately 0.6V. When Pin 1 of IC_1 is less than approximately 1.1V, current through the power-switching transistor is 0A, and the switcher is off.

The resistor ratios of R_6 , R_7 , and R_8 define the duty cycle of the low-frequency oscillator. For the values shown, the duty cycle is approximately 12%; the switcher is off for 1.4 sec and on for 200 msec. Each time the switcher restarts, it does so with soft start because the output of IC_{2B} fully discharges C_1 through R_{1B} . When the circuit pulls the base of Q_1 low, collector

current continues to flow; the circuit maintains the voltage across R₃ even when the switcher is off. IC₂₈ continues to cycle until the overcurrent fault clears. When the fault clears, the circuit reestablishes the nominal output voltage of the switcher, and the voltage at IC, Pin 1 drops below the clamp level. The voltage across R₂ drops to 0V and ensures an open-collector output at IC22B's oscillator output.

Removing R_4 and adding R_5 causes the switcher to latch off and not restart, in response to current limit. You can adjust the ratios of R_6 , R_7 , and R_8 to optimize the fault-delay time. Increasing the threshold voltage at IC_{2B}'s Pin 5 increases the fault-delay time before latch-off.

Oscilloscope waveforms (**Figure 2**) show the power-switch current cycling on and off when the switcher is in current-limit mode (**Figure 2a**). A time expansion of the ramp-characteristic of the powerswitch current for each restart event shows that each restart benefits from the soft-start characteristic (**Figure 2b**).

These waveforms are the result of measuring the voltage across a current-sensing resistor; the waveforms represent the current through the main power-switching transistor switching at 50 kHz.(DI #2369)

Edited by Bill Travis and Anne Watson Swager

Control 32 DAC channels via a parallel port

Mark A Shill, Burr-Brown Corp, Tucson, AZ

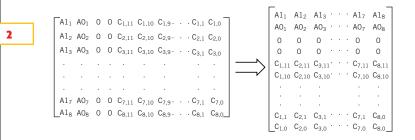
CCASIONALLY, A SYSTEM needs several digitally programmable voltage-output channels.

Figure 2

Such output channels typically provide the control for robot positioning, industrial processes, and even home automation. The circuit in **Figure** 1 (pg 94) controls 32 voltage-output channels from the parallel port of a PC. The circuit comprises eight DAC7615 quad voltage-output, serial-data programmable, 12-bit DACs. The controlling PC individually programs each of the 32 DAC channels, and all DAC outputs simultaneously update.

The parallel port's eight data-output lines provide serial data into each of the eight quad DAC7615s. The remaining four control lines of the parallel port provide the serial-data clock, input-register clock, DAC-register clock, and DAC-reset functions. Each DAC7615 has a reference high and low input, which the circuit connects to external reference voltages of 2.5V and -2.5V, respectively. Two OPA4277 quad op amps buffer the $\pm 2.5V$ DAC reference voltages. Because all of the DACs use the same $\pm 2.5V$ reference voltages, all DAC outputs track to-

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ideas

A series of eight quad-output voltage DACs provide 32 channels that you can individually program. All of the DACs simultaneously update.

gether as a function of these references. The resulting DAC output-voltage range for all 32 channels is -2.5V to +2.5V.

The circuit programs each of the eight DAC7615s by shifting in a serial 16-bit word comprising two address bits, two dummy bits, and the DAC 12-bit data word. The serial data for the $\mathrm{V}_{\mathrm{OUTA}}$ channel of each DAC7615 shifts in first, followed by the $\rm V_{OUTB}, \, V_{OUTC}, \,$ and $\rm V_{OUTD}$ channels. The DAC7615s have a doublebuffered data input, so the circuit can load the programmed data for all DAC channels into input registers without changing the previously set DAC output voltage. After each 16-bit word shifts into the corresponding DAC7615, the DAC control line **LOADREG** momentarily pulses low to latch the shifted data into each DAC's internal input register. Finally, when the circuit has programmed all DAC input registers, the signal LOAD-DACS pulses low to update the internal DAC registers and change all DAC outputs.

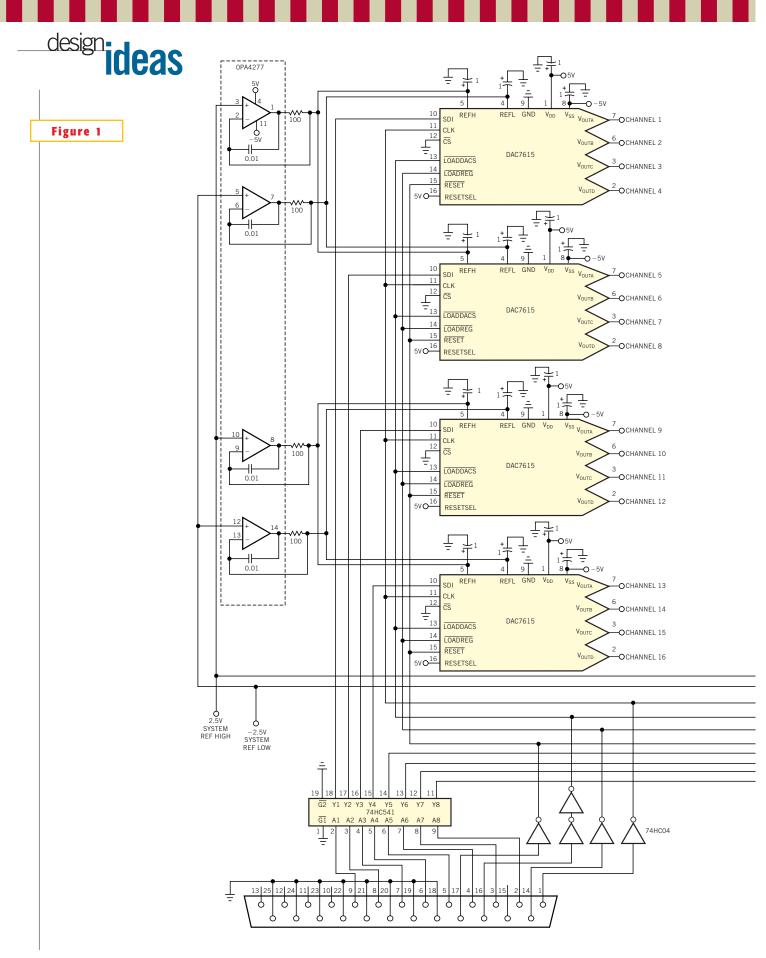
To use the parallel port for simultaneous serial data transmission to all DAC7615s, the software must first manipulate the digital output data to place it in a form that can stream out the parallel port. The controlling software transposes a group of eight 16-bit words, representing the codes to shift into each DAC7615, into a group of 16 8-bit words (**Figure 2**). The resulting vector of 16 8bit words represents the 16-bit serial data stream, which the circuit simultaneously shifts into the selected one-of-four registers of the DAC7615s. This transposition repeats four times to program all four channels of each DAC7615.

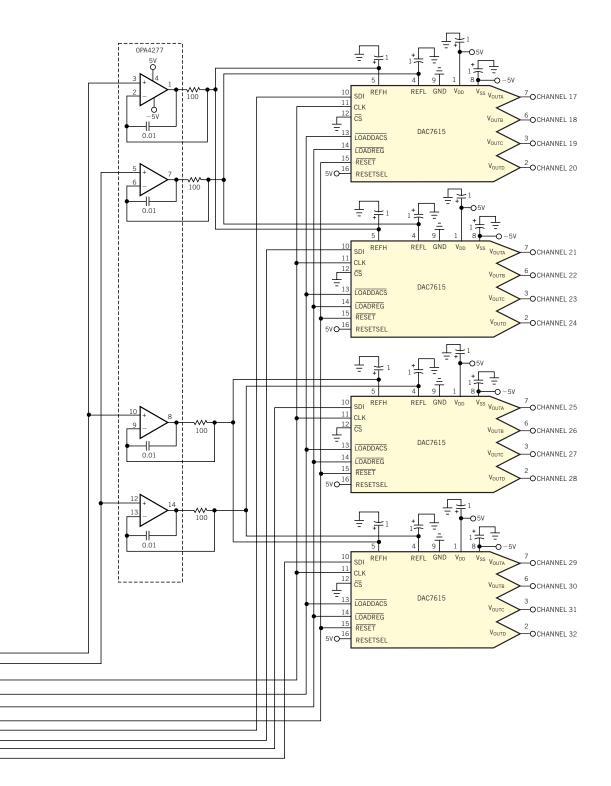
The accompanying program "Write-DAC32," which is written in Borland Turbo Pascal, accepts an array of 32 12-bit codes for programming each of the DAC channels. WriteDAC32 uses an assemblylanguage procedure to repeatedly leftshift the leading bit of each 12-bit DAC code and then reconstruct 12 8-bit words representing the stream data that the PC outputs on all eight of the parallel port's data lines. To program all 32 DAC channels, 4×16 data-clock cycles are necessary. If you daisy-chain the DACs, the number of necessary clock cycles is $4 \times 8 \times 16$. You can download the program from EDN's Web site, www. ednmag.com. Click on "Search Databases/Links Page" and then enter the Software Center to download the file from DI-SIG, #2347. (DI #2347)

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www.ednmag.com

98





NOTE: ALL CAPACITORS ARE IN MICROFARADS.

The controlling software transposes eight 16-bit words into a vector of 16 8-bit words.



Comparator has programmable limits

Michele Frantisek, Brno, Czech Republic

THE CIRCUIT IN **Figure 1** combines a dual buffered D/A converter and dual four-input comparator to configure a comparator circuit with a digitally programmable window center and width. The circuit has three outputs that sepa-

rately indicate the comparison states: within the window, over the upper limit, or below the lower limit. With the component values shown, you can program the center voltage of the window from -10.24 to +10.235V in 5-mV steps, and the width of the window from 0 to 20.47V, also in 5-mV steps. The programmed values are fully independent of each other and of the input voltage. The dual buffered DAC-8222, together with three op amps from an OP-400, generates the voltages V_x (center voltage for the LTC1040) and V_y (half the window width) from binary data stored

in the DAC's latches. Whereas DAC A of the DAC-8222 operates in a bipolar configuration, DAC B operates in unipolar mode. A μ P's address bus generates the DAC's control signals DAC-A/DAC B,

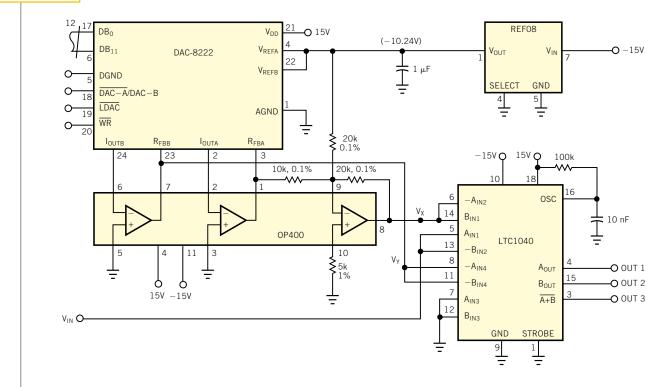
Figure 2

LDAC, and WR. The reference voltage for the V_{REFA} and V_{REFB} inputs of the DAC-8222 comes from the REF08, configured for a -10.24V output. The LTC1040 contains two sampling-mode comparators

FORM OF WINDOW	V _X	V _Y	LATCHED INPUT DATA IN DAC A	LATCHED INPUT DATA IN DAC B
1V -1V	OV	1V	1000 0000 0000 DECIMAL 2048	0001 1001 0000 DECIMAL 400
2V ov	1V	1V	0111 0011 1000 DECIMAL 1848	0001 1001 0000 DECIMAL 400
2V _4V	-1V	3V	1000 1100 1000 DECIMAL 2248	0100 1011 0000 DECIMAL 1200



Figure 1



A precision comparator uses a D/A converter to provide precise, noninteractive control of the upper and lower thresholds.



that drive the three outputs of the circuit. Output Out 1 assumes a logic-high state if the algebraic sum of the voltages at A_{IN1} , A_{IN2} , A_{IN3} , and A_{IN4} is positive, as the following equations show: $V_{IN} - V_X > 0$; therefore, $V_{IN} > V_X + V_Y$. Out 1 thus assumes a high state if V_{IN} is greater than the upper limit of the window $(V_x + V_y)$.

Similarly, Out 2 assumes a high state if the sum of voltages B_{IN1} , B_{IN2} , B_{IN3} , and B_{IN4} is positive: $V_X - V_{IN} - V_Y > 0$; therefore, $V_{IN} < V_x - V_y$. Thus, Out 2 goes high if the value of V_{IN} is lower than the bottom limit of the window $(V_x - V_y)$. Finally, Out 3 assumes a high state if both Output 1 and Output 2 are low: $V_x - V_{YY} < V_{IN} < V_x + V_y$. Thus, Output 3 goes high if the value of V_{IN} is greater than the lower limit and lower than the upper limit of the window. The RC combination at Pin 16 of the LTC1040 determines the sampling rate; in this case, approximately 1000 samples/sec. Figure 2 gives some examples of V_x and V_y and their digital equivalents stored in the DAC's latches. The circuit needs no calibration and produces maximum errors of ± 10 mV over the full range. (DI #2377)

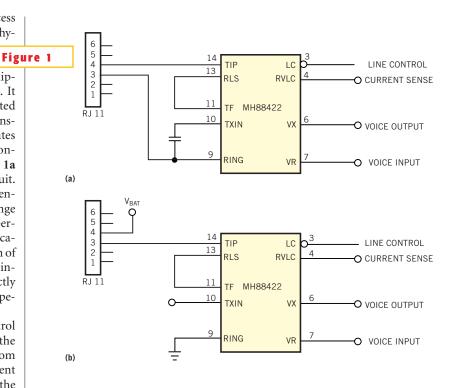
To Vote For This Design, Circle No. 347

DAA circuit emulates central-office operation

Jerzy Chrzaszcz, Warsaw University of Technology, Poland

HE MITEL MH88422 data-access arrangement (DAA), a thick-film hybrid module, contains a complete interface between duplex voice- or data-transmission equipment and an analog telephone line. It provides transformerless, optoisolated two-to-four-wire conversion with transhybrid loss cancellation and operates from a 5V supply. The DAA also consumes low on-hook power. Figure 1a gives Mitel's typical application circuit. The Tip and Ring lines connect to a central-office or private-branch-exchange line, and the interface mimics the operation of a telephone set. The modification in Figure 1b changes the function of the interface such that an ordinary single-line telephone can connect directly to such systems as a voice/touch-tone peripheral device.

In this configuration, line-control (LC) input is always active. When the telephone goes off-hook, the path from battery to ground closes. Line current flowing in the sense resistor in the MH88422 activates ring voltage/line current (RVLC), thereby signaling the off-hook state to the system controller. Analog functions are as in the original configuration; that is, you can transmit and receive signals. The modified system



A modification (b) of a DAA's recommended interface (a) provides central-office-like operation for single-line telephones.

provides no ring signal and thus can serve only incoming calls; nevertheless, the interface operates much like a central-office arrangement. (DI #2376).



Speedy logic translator uses little power

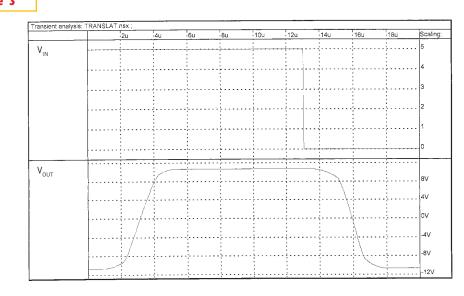
Davis Magliocco, CDPI, Scientrier, France

N HANDHELD EQUIPMENT, component count and power consumption are critical considerations. This Design Idea uses only a few transistors to configure a high-speed output

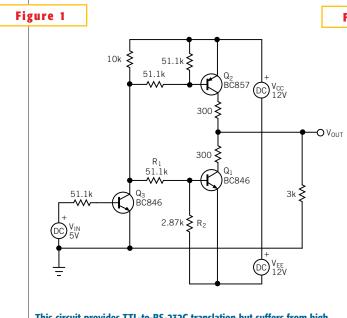
stage of an RS-232C **Figure 3** link while draining few precious milliamperes from the batteries. In general, the data to transmit comes from an IC (for example, an ADC or a μ C) connected to 5V and ground. The RS-232C protocol requires $\pm 12V$ transmission levels. You can derive the voltages directly from the RS-232C line of a computer with a simple diode circuit. You need a charge pump only in the case of a direct connection to a printer because the 12 and -12V may not be available simultaneously.

The translation from $\pm 12V$ to 0/5V of the signals coming from the RS-232C

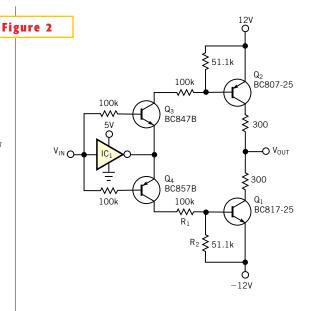
link is easy to implement with a standard Schmitt trigger, such as a CD40106 or CD4584, with protection resistors in series with the inputs. The circuit in **Figure** 1 translates in the other direction. The circuit has some shortcomings: It wastes power through R_1 and R_2 turning off Q_1 while Q_2 is on. Also, the time constants



Input-output delay and rise and fall times are all approximately 2 µsec in Figure 2's circuit.



This circuit provides TTL-to-RS-232C translation but suffers from high power consumption and dissimilar rise and fall times.



A simple logic gate cuts power drain and provides high-speed operation with symmetrical rise and fall times.



differ in turning Q_1 and Q_2 on; the output rise time can be 50% longer than the fall time. To obtain high speed and avoid transmission errors stemming from wrong bit length, you must lower all the resistor values, thereby raising power consumption.

The circuit in **Figure 2** draws current only when turning Q_1 or Q_2 on. When the

output of IC₁ is low, Q_3 is on, and the reverse-biased Q_4 is off; no current flows in R₁ and R₂. When the output of IC₁ goes high, Q_3 turns off while Q_4 turns on. Because the two branches are symmetrical, the time constants are similar, and the output exhibits similar rise and fall times (**Figure 3**). With one-tenth the power consumption of the circuit in **Figure 1**,

the circuit achieves the same transmission speed without risk of bit-length error from asymmetrical rise and fall times. (DI #2378)

> To Vote For This Design, Circle No. 349

Parallel port replaces embedded μ C

Eli Kohav and Leonid Grossman, ECI Telecom, Petah-Tikva, Israel

ANY APPLICATIONS USE an embedded processor, which has certain needs: software, RAM, ROM, board space, and others. Frequently, another host computer, usually a PC, controls the application. Using a single CPLD, you can dispense with the embedded processor and let the PC directly control your system via the PC's parallel port (**Figure 1**). The CPLD mimics the address, data, and control buses of a standard μ C, such as an 8052, so you can use standard μ C interfaces and peripherals in your system. The advantages you glean from this arrangement are:

You need no special develop-

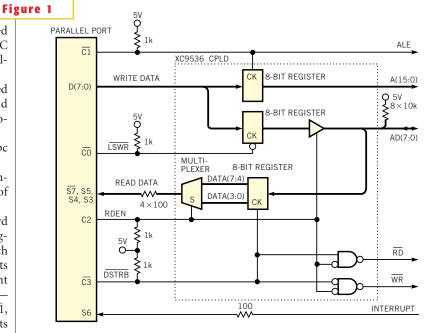
- ment software for your embedded processor. You can use standard PC software. Thus, you need not develop software for two systems.
- You can dispense with the embedded μC; its ancillary RAM, ROM, and crystal oscillator; and other components.
- You free up space on your system's pc board.
- You can benefit from the PC's computing power and its huge base of ready-made software.

The circuit in **Figure 1** uses a standard parallel-port interface, which has 12 digital outputs and five digital inputs, which you access via three successive 8-bit ports in the PC's I/O space: Data Port—eight output pins: D(7:0); the Control Port—four outputs (three inverted): $\overline{C3}$, C2, $\overline{C1}$, and $\overline{C0}$; and the Status Port—five inputs (one inverted): $\overline{S7}$, S6, S5, S4, and S3.

The design fits in a small CPLD: Xil-

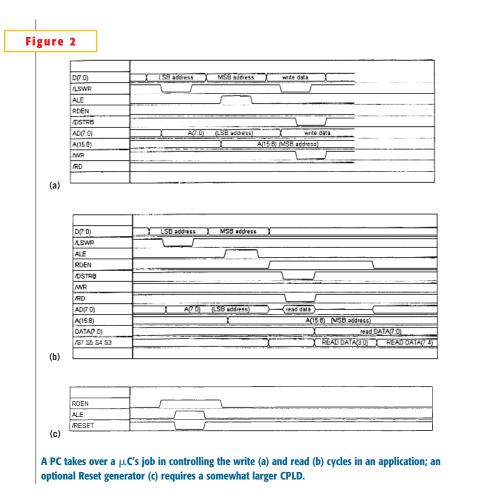
inx's XC9536. The CPLD has three internal 8-bit registers. One latches the highaddress bus—A(15:8). The other two latch the multiplexed low-address/Write data, and the Read data—AD(7:0). The PC writes address and data via the Data Port and reads data via the Status Port. Status Pin S6 provides an interrupt. The Control Port generates the control signals of the emulated processor, as well as the internal control signals of the CPLD. To implement a write cycle, the PC issues three successive bytes on the Data Port: the low-order address byte, the high-order address byte, and the data byte. The Control Port generates the needed control signals (**Figure 2a**). The system implements the read cycle by issuing the address in the same order and then reads the data byte in two cycles: low-order data nybble and high-order data nybble (**Figure 2b**).

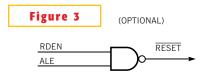
Note that, although the procedure is relatively slow, it's fast enough for most applications, because total I/O access is only a fraction of the application-soft-



A CPLD and a PC's parallel port save component count and board space by replacing an embedded processor.







You can exploit otherwise unused control signals in Figure 1's configuration to generate a Reset signal.

ware time budget. The serially connected 100 Ω resistors degrade the slew rate of the signals routed to the PC to prevent transmission-line effects on the parallel port's cable. The 1-k Ω pullup resistors connect to the open-collector signals on the Control Port. The 10-k Ω pullup resistors eliminate floating conditions on the AD(7:0) bus. This application needs no Reset signal. If your design needs one, you can generate it by using a memorymapped port or an unused combination of the control signals (**Figures 2c** and **3**). In this case, you need a larger CPLD. (DI #2374)

> To Vote For This Design, Circle No. 350

Transimpedance amp covers dc to gigahertz range

Lukasz Sliwczyński and Przemysaw Krehlik, University of Mining and Metallurgy, Kraków, Poland

TO CONVERT THE WEAK, broadband signal from a fiber-optic transmission channel into electrical form, you can use a high-impedance receiver or a transimpedance amplifier. Either method provides the desired gain and bandwidth but removes any dc and low-frequency components of the signal, because both methods require ac coupling. In a situation in which you need to also amplify the dc component, neither method is satisfactory. The feedforward compensation scheme in **Figure 1** solves the problem. The circuit exploits an ERA 5 monolithic-microwave IC (MMIC) from Mini-Circuits (Brooklyn, NY, www.minicircuits.com) as the RF amplifier. It's easier to use such an off-the-shelf part than to configure your own gigahertz-region amplifier.

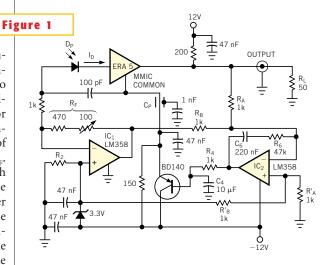
You can consider the approach in **Figure 1** as a sort of transimpedance amplifier with addition of a feedforward compensation path. The circuit processes signals from 0 Hz to the high-frequency cutoff of the MMIC (approximately 4 GHz for the ERA 5). Current from the reverse-biased photodiode, D_p , an InGaAs C 30617BQC PIN diode from EG&G Canada (www.egginc.com), enters the MMIC at 50 Ω input impedance, virtually a short circuit for the photodiode. The MMIC converts the current to a voltage, which appears on the load resistor, R_L. The MMIC exhibits an output-offset voltage of approximately 5V, referred to the MMIC's common pin. IC₂ closes a feedback path around the MMIC, thus removing any offset voltage between the MMIC and circuit ground. You could say that IC₂ substitutes for an output capacitor.



Exchanging the feedback circuit for an output capacitor provides a summing point, convenient for introducing the compensating signal. This signal comprises the current flowing into the second photodiode terminal (normally used only for polarization) and the transimpedance amplifier made up of amplifier IC₁ and resistor R_F. The signal routes next through R_{p} to the summing point at the inverting input of amplifier IC₂. Because the voltage at the summing point must be constant, any dc current from the photodiode must influence the MMIC's output voltage, to compensate the voltage at the output of amplifier IC₁. R_c and

 C_c cancel the pole resulting from the decoupling filter, R_4 - C_4 , thus guaranteeing stability.

Assuming that R_A equals R_B , R_A' equals $R_{B'}$ and the condition $RF=Z_{TO}/2$ is fulfilled, the transimpedance gain of the entire circuit is $k=-(S_pZ_{TO})/2$, where Z_{TO} is the transimpedance of the MMIC and S_p



Feedforward compensation allows you to preserve the dc and low-frequency components of fiber-optic transmissions.

is the photodiode responsivity (typically 0.85A/W at 1310 nm). You can obtain Z_{TO} from the scattering parameters of the MMIC: $Z_{TO} \approx 2s_{21}Z_{0}$, where Z_{0} is the termination resistance for the scattering matrix, usually 50 Ω . Z_{TO} for the ERA 5 MMIC is approximately 1 k Ω . If you don't fulfil the foregoing conditions, the

frequency characteristics of the circuit will not be flat in the low-frequency region.

Because you don't know the exact value of Z_{TO} , you should trim $R_{\rm F}$ for the MMIC you use. You can perform the trim using either a low-frequency spectrum analyzer or a pulse generator with an oscilloscope. With perfect compensation, the frequency response of the amplifier should be flat and should display no overshoot or undershoot. To get the best results, you must take care in designing the pc-board layout because of the circuit's high bandwidth. Especially, decouple the MMIC's common point using components as small as possible to reduce

parasitic inductance. You should accurately match resistors $R_A - R_A'$ and $R_B - R_B'$ to minimize offset voltages. (DI #2386).

To Vote For This Design, Circle No. 351

Simple scheme detects shorts

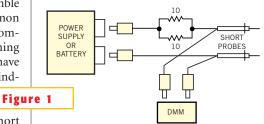
Luis Miguel Brugarolas, SIRE, Madrid, Spain

W HEN YOU MANUALLY assemble complex boards, it's common to short-circuit adjacent component or IC pins. Determining which section of the circuit you have shorted is not too difficult, but finding the precise point where

ing the precise point where the short exists can be a **Fig** formidable task, because the short

may be under a surface-mount component. The circuit in **Figure 1** eases the diagnosis. It uses off-the-shelf components, and you can build it in a few minutes. The circuit uses a

DMM set at its maximum voltagesensitivity scale (typically, 200 mV fullscale with 0.1-mV resolution). The DMM measures the voltage drop in the divider comprising the 5Ω resistor and



A do-it-yourself short-circuit detector makes it easy to find solder bridges in pc board using surface-mount components.

the cable and short-circuit resistance.

For the power source, you can use a laboratory supply or a battery cell. The low power-source voltage guarantees that no circuit damage can occur, even if you probe the wrong circuit points. For a 1V source, the circuit's transfer function is 0.5 mV/m Ω —enough sensitivity for any practical situation. The accuracy of the DMM is not important, but resolution is. The scheme is simple to use: With the circuit under test unpowered, connect the probes in any area of suspected shorted nets. Move one probe in a direction to minimize the voltage reading. Then, move the other probe to find the point that produces an absolute minimum reading. The

short circuit is most likely between the points the two probes touch. (DI #2385)

design ideas

Edited by Bill Travis and Anne Watson Swager

Synchronous oscillator converts audio, video to FM

Vasil Uzunoglu, Synchtrack, Gaithersburg, MD

■ HE SYNCHRONOUS OSCILLATOR (SO) and the coherent phase-locked synchronous oscillator (CPSO) are universal multifunctional networks that track, synchronize, and amplify as much as 80 dB; improve SNR by as much as 70 dB; and modulate AM, FM, and FSK signals. You can also use these networks as ADCs, sampling networks, and dividers that divide by rational integer numbers, such as 3/4, 5/7, and 7/8. Suitable applications include wideband spread-spectrum communications and binaryphase-shift-keying (BPSK) and **Figure 1** quadrature-phase-shift-keying (QPSK) generation. A CPSO retains all

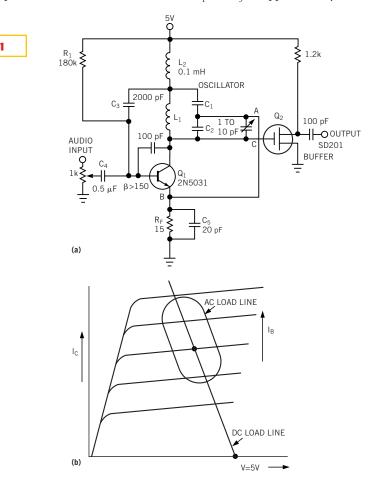
(QPSK) generation. A CPSO retains all the properties of the SO and provides zero phase error.

One SO application area is the conversion of audio and video to FM in a single process. **Figure 1a** shows a simple, one-stage SO oscillating at 94 MHz. This frequency is a good choice for testing the audio-to-FM conversion on an FM broadcast receiver. The audio or video input to this SO should not exceed -5 dBm; any signal above this level may induce amplitude modulation. C_4 's decoupling capacitor passes the audio or video to the SO and eliminates dc bias at the in-

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put. R₁ biases the SO. Because the oscillator's load is a combination of resistance, inductance, and capacitance, the load line is a combination of a straight line and an ellipse (**Figure 1b**). The linear load line indicates the dc bias, and you must locate the load line away from the nonlinear characteristics of the transistor.

 C_3 and the connection between points A and B each provide positive feedback. High positive feedback is essential to the optimum operation of the SO. The value of C_3 should range from 2000 to 5000 pF. R_F in parallel with C_5 has numerous functions. The presence of this network allows positive feedback within the SO, but looking from the input, R_F and C_5 also provide negative feedback. This negative feedback adds frequency stability. Finally, R_F and C_5 divert the input audio or video to the oscillator, not to ground. R_F and C_5 are approximately 15 Ω and 20



A single-stage synchronous oscillator converts audio or video to FM (a). The load line is a combination of a straight line and an ellipse (b).



pF, respectively, and these values depend on the β of the transistor. L₂ is an RF choke that diverts the collector feedback to the base of the transistor. You should tune the tank circuit, which comprises L₁, C₁, and C₂, to approximately 95 MHz to be within the FM broadcast band. A 2N5031 for Q₁ works well for this application because it has high gain and low noise; any other transistor with the same characteristics is suitable. A 2- or 3-in. long wire attaches to the output and acts as an antenna.

The conversion from audio or video to FM takes place in the internal base-emitter junction capacitor by its parametric action, and the changes of the junction capacitor due to audio-to-video variations modulates the oscillations to provide an audio- or video-to-FM conversion.

The SO also has high input-signal sensitivity and high noise rejection. It can detect signals as low as -100 dBm and signals with SNRs as low as -40 dB. For a PLL, these performance numbers are -25 dBm and 3 dB, respectively. The SO is frequency-stable and has low phase jitter because the tank circuit has a high Q that can reach 3×10^6 . The SO has three independent internal filters. With a 200-Hz noise-rejection filter, the SO exhibits a data bandwidth or tracking range of several megahertz. For input signals with high noise, a two-transistor cascoded SO is preferable.

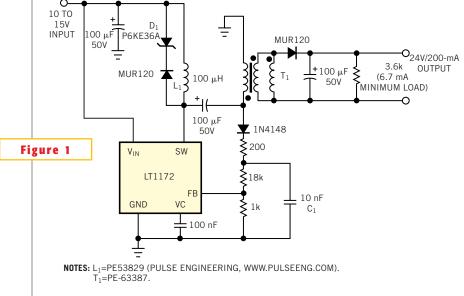
The output buffer, Q_2 , provides protection between the oscillator and the output world. However, if you want to simplify the circuit, you can remove Q_2 and its 1.2-k Ω pullup resistor and connect the 100-pF capacitor at the output directly to Point C. (DI #2379)

> To Vote For This Design, Circle No. 331

High-isolation converters use off-the-shelf magnetics

Mitchell Lee, Linear Technology Corp, Milpitas, CA

solated FLYBACK CONVERTERS usually evoke thoughts—or bitter memories—of custom transformers, slipped delivery schedules, and agency-approval problems. Off-the-shelf flyback transformers carry isolation ratings of only 300 to 500V and rarely of as much as 1 kV. Gate-drive transformers are readily available from stock with high isolation ratings and low cost, but they are wound



The second "coil" of this unusual flyback converter is not a coil but rather an off-the-shelf gatedrive transformer. This component offers 3750V rms isolation and full VDE approval. on ungapped cores, have high inductance (500 μ H to 2 mH), and quickly saturate in a normal flyback-converter circuit. Thus, high isolation calls for an abnormal flyback converter (**Figure 1**).

Based on the uncoupled SEPIC (single-ended primary-inductance-converter) topology, the converter operates from a 12V battery-backed input supply and outputs 24V at 200 mA. The key feature is the second "coil," which is not a coil but rather an off-the-shelf gate-drive transformer, T₁. This component offers 3750V rms isolation and full VDE approval; it functions flawlessly in SEPIC service. The output is completely isolated from the input.

The converter derives feedback from the primary winding through D_1 . The transformer winding is 1-to-1. C_1 peak detects a voltage roughly equal to the output. A minimum load of 3.6 k Ω prevents the output from rising uncontrollably at zero load (**Figure 1**). (DI #2380)



Autoranging circuit simplifies hardware and software

Dana Romero, Phonex, Midvale, UT

NATURAL APPROACH TO autoranging is to use an inverting op amp and switch in one of N feedback resistors at a time for a gain of $A=-R_F/R_o$ (**Figure 1**). However, the inverting configuration suffers from low input impedance of $Z_{IN}=R_o$ because the negative input is at virtual ground. Also, another inverter is necessary to provide positive voltage ranges because of positive signals at the input.

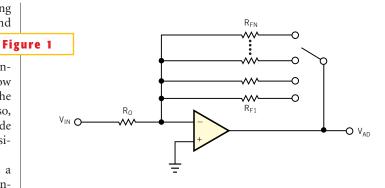
An alternative approach is to use a noninverting op amp that has a high input impedance and a gain equation of $A=1+R_F/R_O$ (Figure 2). This circuit augments the typical 0 to 5V input range of a μ C with ranges of 0 to 1V and 0 to 10V. The circuit in Figure 2 uses a 68HC16 μ C, but the results generally apply to any μ C with an ADC. The unusual

arrangement of circuit components provides three input ranges that use only a single op amp, two spdt relays, and resistors with standard values. Also, the circuit simplifies the autoranging software because after K_2 switches, the status of K_1 is irrelevant.

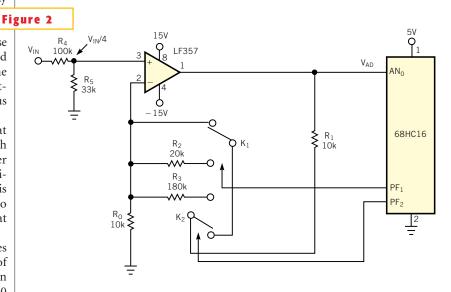
With the relays in the positions that **Figure 2** indicates, R_F equals R_1 , which in turn equals R_0 . Thus, the amplifier gain is 2. Combined with the voltage divider of R_4/R_5 , the overall circuit gain is 1/2, which is the gain necessary for a 0 to 10V input at V_{IN} to provide 0 to 5V at V_{AD} .

 V_{AD} . When K_1 switches, R_F becomes $R_2+R_1=2R_0+R_0=3R_0$ for a gain of $1+3R_0/R_0=4$. Dividing by 4 gives an overall gain of 1, which is suitable for a 0 to 5V range at V_{IN} . At this point, it becomes obvious why the voltage divider sits before the amplifier: With V_{IN} near 5V, multiplying by 4 would saturate the op amp.

When K_2 switches, the position of K_1 is irrelevant, and R_F equals $R_3+R_1=18R_0+R_0=19R_0$. Thus, $A=1+19R_0/R_0=20$. Now, the overall gain is 20/4=5, or exactly the value necessary for a V_{1N} range of



A single noninverting op amp, two spdt relays, and standard-value resistors can produce a 0 to 5V output from input ranges of 0 to 10V, 0 to 5V, and 0 to 1V.



An obvious autoranging circuit suffers from low input impedance and needs an inverter to produce positive output-voltage ranges.

0 to 1V to produce an output of 0 to 5V.

Although the gain calculation works out exactly with standard 5% resistor values, for greater accuracy, you can switch the resistors to the nearest 1% values. Or, even better, sort through a batch of 5% resistors and use a good multimeter to find resistors that are within 1% of nominal. (DI #2381)



Simple technique speeds Microstrip breadboarding

Steve Hageman, Hewlett-Packard Co, Santa Rosa, CA

S UPERGLUE AND SOME THIN, sheared pieces of Teflon copper-clad material are all you need to easily produce Microstrip-type structures for breadboarding high-frequency analog or RF circuits. By gluing properly sheared widths of copper-material to the pc-board material, you can build an RF-circuit prototype in less than one-tenth of the time it takes to carve and clean a Microstrip on the top surface of a prototype pc board. Also, this method allows you to easily move or add Microstrip lines as prototyping progresses.

High-frequency prototyping of analog circuits demands that you build everything on a ground plane to limit the inductance in the ground returns. Furthermore, RF-circuit design demands that all interconnections be 50Ω transmission lines, or 75Ω transmission lines if you are a TV type. The most common way to make a 50Ω transmission line on a pc board is to use a Microstrip structure. A Microstrip transmission line is a trace on the top of the board, and the ground return is the backside copper of

the board. This type of structure is easy to make when you are laying out a board for production, but it presents formidable problems when you are prototyping. For one thing, it is inconvenient to use the backside of the prototype pc board as the ground plane. For every node that must connect to ground, you must drill a via through the board to reach the ground. Also, making the Microstrip line requires that you use a razor or power tool to carve out the top-side copper. This technique is messy and error-prone, especially if you are building the circuit piece by piece.

The sheared-copper method exhibits the necessary 50Ω -impedance characteristics and eliminates the groundplane-attachment problems for the other components. The key is to get your hands on a 0.026-in.-thick Teflon pcboard material called RT/duroid 5870 (Rogers Corp, www.rogers-corp.com). This material has a relative dielectric constant (e_r) of about 2.33. Using any electrical-engineering text, you can find equations that state that for an e_r of 2.33, the width-to-height ratio of a Microstrip structure is about 3.3 to 1 for a 50 Ω impedance. So, when using 0.026-in.-thick pc-board material, you should shear the



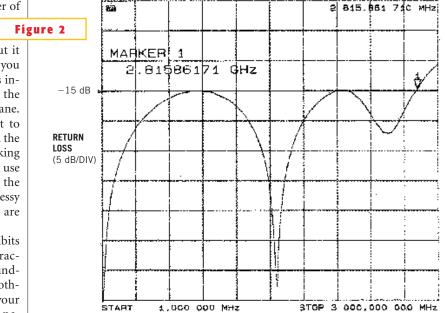
Figure 1 RT/duroid material on top of normal FR4 pc-board material makes a very quick Microstrip structure. Make sure that the line lies flat and is firmly glued in place against the board to maximize the return loss

of the line.

RT/duroid board in approximately 0.086-in.-wide strips.

You can attach the strips to the copperclad prototype board using dabs of cyanoacrylate, or instant, adhesive along the length of the strips to form the Microstrip structure. The RT/duroid material is soft and makes it easy to place and bend the strips as necessary; it exhibits an excellent 50 Ω match to around 3 GHz or higher. Also, you can easily cut the resulting Microstrip structure to allow for placement of series-matching or passivelumped elements for dc decoupling. This method also makes it easy to place parallel components and to place components from the Microstrip line to the ground plane; you simply solder from the top of the Microstrip line to the adjacent ground plane without drilling vias.

For measurement purposes, the photo in **Figure 1** shows two Microstrip lines on a prototype pc board. You glue the upper line to the prototype board to form a straight transmission line. The lower



A return-loss (S11) measurement of the bent Microstrip-line in Figure 1 exhibits an excellent match->-15 dB or VSWR<1.4 to 1-to nearly 3 GHz.



line, which easily bends around corners, is bent 90°. Measurements of the bent line show that the return loss of the line exceeds 15 dB to almost 3 GHz and that the straight Microstrip line has a better than 20-dB return loss all the way to 3 GHz (**Figure 2**).

Alternative methods of breadboarding yield poorer results. The use of common

wire-wrap wire placed above a ground plane yields an impedance of about 100Ω and is usable only to the 100-MHz region for short lengths. The use of miniature coax is not only time consuming, but the shield pigtails at the ends of the coax, which are necessary to access the center conductor, add enough inductance to cause power holes of 5 to 10 dB in the range of 100 MHz to 3 GHz. Also, both of these methods preclude the easy attachment of components anywhere along the transmission line. (DI #2382)

> To Vote For This Design, Circle No. 334

Comparator has independent trip voltages

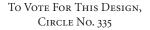
Gregory Billiard, Fike Corp, Blue Springs, MO

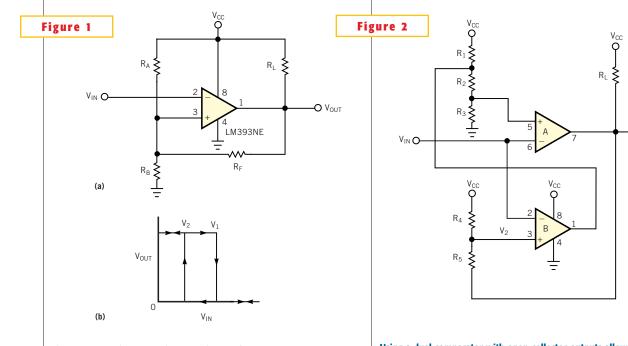
Figure 1). Unfortunately, using three resistors to set the upper and lower trip voltages creates a dependence between the two trip voltages: It's impossible to set one voltage without affecting the other. However, you can achieve the same output-voltage response with two independent trip voltages by using a comparator with an open-collector output, such as the LM393 or LM339. In **Figure 2**, the resistor divider of R_1 , R_2 , and R_3 determines the upper trip voltage, V_1 . R_4

and $\rm R_{_5}$ determine the lower trip voltage, $\rm V_{_7}.$

When V_{IN} is between 0 and V_1 , V_{OUT} is high and prohibits any current flowing through R_4 and R_5 , which sets V_2 to V_{CC} and thus keeps the output of Comparator B high. When the output of Comparator B is high, $V_1 = V_{CC} \times R_3/(R_1 + R_2 + R_3)$. When V_{IN} exceeds V_1 , V_{OUT} goes low, to 0.7V, allowing current to flow through the resistor divider. V_2 then changes from V_{CC} to 0.7V+ $V_{CC}R_5/(R_4 + R_5)$. On this change, the output of Comparator B also goes low, bringing V_1 to $0.7 \times R_3/(R_2 + R_3)$. V_1 is now lower than
$$\begin{split} & V_{\rm IN}, \text{so } V_{\rm OUT} \text{ goes low. } V_{\rm OUT} \text{ stays low until } V_{\rm IN} \text{ drops below } V_2. \text{ When } V_{\rm IN} \text{ drops below } V_2, V_{\rm OUT} \text{ goes high again; } V_2 = V_{\rm CC}; \\ & \text{and } R_1, R_2, \text{ and } R_3 \text{ set } V_1. \end{split}$$

You can easily set either trip voltage without affecting the other. However, V_1 must be greater than V_2 or both trip voltages will be equal to V_1 . A disadvantage of this circuit is that it requires two comparators, but comparators usually come in dual packages. (DI #2383)





Three resistors determine the trip voltages of an inverting comparator (a) with hysteresis (b), but the trip voltages are not independent.



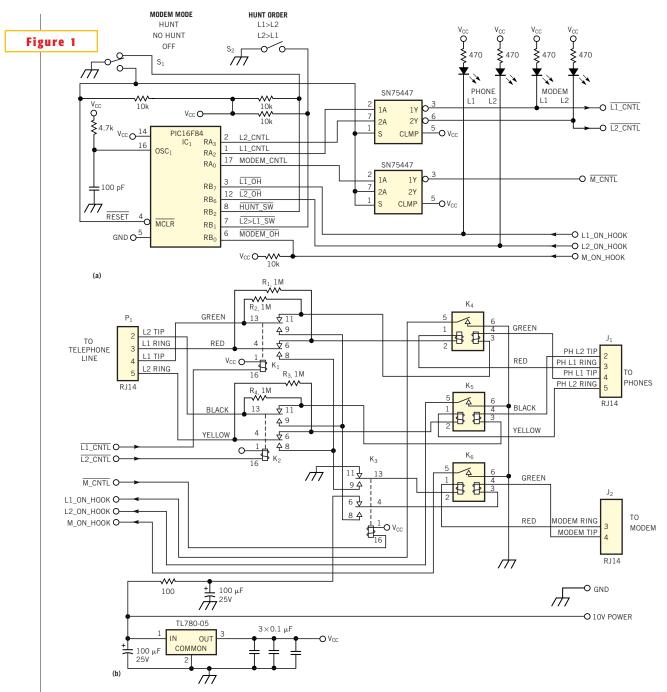
O VOUT



Modem-access adapter reduces interference

Thomas Schmidt, Schmidt Consulting, Milford, NH

HE MODEM-ACCESS ADAPTER (MAA) in **Figure 1** has features that reduce problems when modems and phones share the same line. The design also overcomes the shortcomings of modem interference protectors. The design eliminates mutual interference between phones and modems, is compatible with the line-usage indicators on multiline



A low-cost μ C with flash memory controls the connection of phone lines L1 and L2 to the modem (a). Electromechanical relays switch the phone lines while providing an isolated data path (b).



phones, can search for an idle phone line in multiline installations, draws minimum power, and requires no changes to a PC modem's hardware or software.

Most residential PC users connect to the Internet using a dial-up modem. In most cases, the modem and voice calls must share one phone line. This sharing presents a problem because you can't use the modem and the phone at the same time; picking up an extension disconnects the modem. Many sites have more than one phone line. A computer has a better chance of connecting to a phone line if it can search multiple lines to find one that is idle.

Vendors of modem interference protectors claim the devices eliminate interference between extension phones and computer modems. The devices function by monitoring the voltage between the phone line's tip and ring leads. When all phones are on their hooks, this voltage is typically >48V. Picking up a phone closes the tip-and-ring circuit, which drops the voltage to approximately 7V. The protector monitors the line voltage. When the voltage drops below a certain threshold, the protector disconnects the phones that are connected to it. This action prevents an active phone from interference when you pick up an extension.

Unfortunately, these protectors have two serious shortcomings. First, the device needs to be in series with the phones and modems it is protecting, which requires one device per phone. When you use the device in this manner, you cannot use more than one extension at a time. This situation prevents you from placing a call on hold and picking it up on another extension. Second, you can split the wiring into two circuits: one for phones and one for the modem. This split wiring minimizes the number of protectors you need and allows multiple extensions to pick up the same call. Unfortunately, regardless of how you wire the protectors, the voltage drop across the protector confuses the line-busy indicators on most multiline phones. Multiline

phones no longer indicate when a line is in use.

The MAA in **Figure 1** does not suffer from these problems. You must connect the MAA in series between the telephone-company central office and the phones and modem the adapter is protecting. The most convenient location for the MAA is in proximity to the phonecompany network's interface demarcation point. Simply disconnect the inside phone wiring from the demarcation point and plug this wiring into the MAA. Then run a dedicated phone line between the MAA and computer modem.

The MAA consists of control (**Figure 1a**) and data-path (**Figure 1b**) subsystems. Phone lines source high voltages and are balanced with respect to ground. The design uses electromechanical relays to switch the phone lines while providing an isolated control path.

The heart of the control circuit is IC_1 , a PIC16F84 (Microchip Technology, www.microchip.com) low-cost RISC μ C with flash memory. Flash memory makes this part ideal for development. The MAA program is approximately 100 words long. The accompanying source code is available for downloading from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2389.

When the modem is idle, relay K_3 supplies power to the modem local loop (**Figure 1b**). When the modem goes "off hook" to place a call, relay K_6 senses current flow and wakes the CPU. The CPU reads the state of the hunt-order switch, S_2 , which is a physical switch that allows the user to select the phone-line search order.

Relay K_4 monitors Line 1 (L1), and K_5 monitors Line 2 (L2). When a phone is off hook, loop current causes the appropriate line-sense relay contact to close. The CPU uses this information to determine if the line is in use. Assuming the hunt-order switch is in the search-L1-before-L2 position, the CPU reads the state of L1. If L1 is idle, the CPU energizes K₁

using the L1_CNTL signal. Energizing K_1 disconnects the extension phones from L1 and routes L1 to the normally open contacts on K_3 . Then the CPU energizes K_3 , which connects the modem to L1.

If L1 is busy, the CPU reads the modem-mode switch. If the setting of S_1 enables the hunt mode, the CPU checks the other line for availability. If L2 is idle, the CPU energizes K_2 using the L2_CNTL signal. Energizing K_2 disconnects the extension phones from L2 and routes L2 to the contacts on K_3 . The CPU then energizes K_3 to connect the modem to L2. If both lines are busy, the modem never gets a dial tone and eventually disconnects.

The telephone central office typically disconnects the phone line for a short time at the beginning of the dial tone. After the circuit establishes the connection, the CPU enters a long delay loop. During this time, the CPU ignores changes in the state of the line. At the end of the delay, the CPU checks to see if the line is in the expected condition. If it is, the CPU goes back to sleep. If it is not, the CPU processes the new state.

When the modem hangs up, relay K_6 deenergizes, which also wakes the CPU. When the CPU detects hang-up, it tears down the modem connection and returns the lines to their default state for voice.

The bleeder resistors R_1 through R_4 discharge the phone capacitance and impress the line voltage on all of the extension phones to ensure that the telephonebusy indicators function normally. Relays K_4 through K_6 (Teltone, www.teltone. com) are specially designed to monitor telephone loop current.

The MAA device connects directly to the phone line and therefore must meet FCC CFR 47 Part 68 for protection of the public switched telephone network. Residential devices must meet FCC CFR 47 Part 15 Class B for limitation on unintended radiation. (DI #2389)

Edited by Bill Travis and Anne Watson Swager

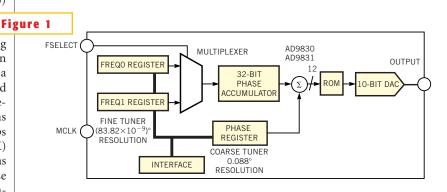
Scheme extends DDS phase-shift resolution

Mary McCarthy, Analog Devices Inc, Limerick, Ireland

IRECT-DIGITAL-SYNTHESIS (DDS) devices find wide use in instrumentation and communications applications. Rather than using a baseband converter to modulate data in a communications system, you can use a DDS device. Such a device has onboard phase registers that accommodate phaseshift keying (PSK). In communications applications, the phase shifting is in steps of 45° ($\pi/4$ differential-quadrature PSK) or 90° (quadrature PSK). The device has enough resolution to generate these phase shifts. In instrumentation applications, the required phase shifts vary, depending on the system under development. Some applications require extremely accurate phase shifts. The phase registers in a DDS device are typically 12 bits wide, resulting in a phase resolution of 360°/4096, or 0.088°. However, by using the frequency register as in Figure 1 to perform the phase-shifting, you can increase the phase-shifting resolution to 32 bits.

If the DDS device has two frequency registers, you can use one to generate the output signal and the other to generate the phase shifts. By using the frequency register to perform phase-shifting, the

120
122
126
128



ideas

By using both the phase and frequency registers in a DDS device, you can increase the phase-shifting resolution from 12 to 32 bits.

phase-shifting resolution becomes $360^{\circ}/2^{N}$, where N is the resolution of the frequency register. Many DSS devices have 32-bit-wide frequency registers. You can therefore phase-shift the output signal with a resolution of $(83.82 \times 10^{-9})^{\circ}$. For example, if register FREQ0 contains the output-frequency value, then you can set FREQ1 to FREQ0+Q, thus phase-shifting the output signal by Q. Under normal conditions, FREQ0 supplies the phase accumulator of the DDS device. During phase-shifting, you select FREQ1 for one MCLK cycle, resulting in phase shifting the output signal by Q.

You can phase-shift the output signal by 0 to 360° . However, the frequency registers should not contain a value equal to or greater than 180° . Thus, to perform phase shifts greater than 180° , you must use the phase register along with the frequency register. You can set the phase register to 180° while using the frequency register to obtain the fine phase-shift resolution. The phase register and FREQ1 register serve as coarse and fine tuners, respectively. You use both registers in unison to perform the phase shift. For example, for Q phase shift in the output signal, PHASE+FREQ1=Q+FREQ0. You set PHASE to 180° and FREQ1 to Q+FREQ0- 180° .

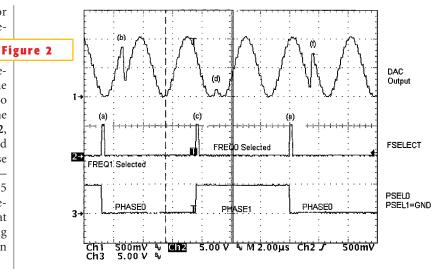
A DDS device has associated pipeline delays. When you select a frequency or phase register, a pipeline delay exists before you see a change at the DAC's output. In some devices, the latency from the phase register to the DAC's output is different from the latency from the frequency register to the DAC's output. With such devices, an intermediate phase shift occurs because the phase shift from either the FREQ1 or PHASE register occurs before the phase shift from the other register. In other DDS devices, such as the AD9830 and AD9831, the latency from the frequency and phase registers to the DAC's output is the same. Therefore, no intermediate phase shift occurs. The plot in Figure 2 shows the performance of the circuit in Figure 1, using the AD9830/9831 DDS device.

The master clock to the DDS device runs at 5 MHz. The device generates a 312.5-kHz output signal. The phase shift of the output signal is 270° at points b, d, and f in the plot. Because the PHASE register in the DDS device comes after



the numerically controlled oscillator (NCO), you must keep this register selected until the next phase shift takes place. The FREQ1 register comes before the NCO, so you need to select it for only one MCLK signal. The AD9830/9831 has four phase registers, so you can use two of them to perform the phase-shifting. For the plot in Figure 2, PHASE0 and PHASE1 are the selected registers. At Point b, the output phase shift is 270° PHASE0's setting is 2048-180°, whereas FREQ1's setting is 1.5625 MHz (equivalent to 312.5 kHz+90°). Selection of FREQ1 and PHASE0 occurs at Point a, with FREQ1's selection lasting one MCLK cycle, and PHASE0's selection a continuous one.

At b, the phase and frequency values have propagated through the DDS device, causing an output phase shift of 180+90=270°. At c, FREQ1's selection lasts one MCLK cycle, and PHASE1 becomes selected, with a value of zero. PHASE1 causes an output phase shift of



Points b and c show the output waveform shifting in phase by 270°.

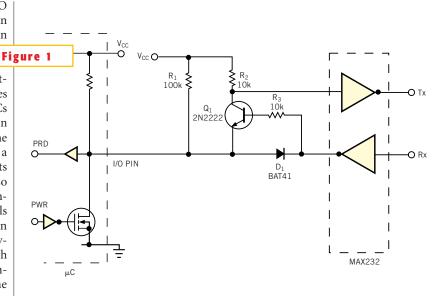
 -180° (PHASE1-PHASE0=0-180°). At d, the output signal's phase shift is $-180+90=-90=+270^{\circ}$. At e, FREQ1 becomes selected for one MCLK cycle while PHASE0 is again selected. This selection produces an output (f) phase shift of 180+90=270°. (DI #2387).

To Vote For This Design, Circle No. 339

Single μ C pin makes half-duplex RS-232C

By Marin Ossman, University of Applied Sciences, Aachen, Germany

N MANY μ C designs, nearly all the I/O pins are occupied. If only one I/O pin is available, the circuit in Figure 1 can help you implement a serial RS-232C interface. For many purposes, half-duplex operation using a software-driven RS-232C interface provides a good communications link. Many µCs have open-drain I/O pins, as shown on the left of the figure. In the idle state, the RS-232C lines Rx and Tx both assume a negative voltage; their TTL counterparts assume a high level. The I/O pin is also at a high level, and neither D₁ nor Q₁ conduct. If a mark signal on the Rx line pulls the Rx line high, D, conducts, the I/O pin goes low, and the µC reads this low level. Because the base of Q_1 is negative with respect to its emitter, Q1 does not conduct and Tx does not retransmit the mark level. If the µC wants to transmit a mark, it pulls the I/O pin low (by setting power to low).







Now the emitter of Q_1 is at ground level, and the high level on the Rx interface output supplies base current to Q_1 via R_3 . Q_1 conducts, and the RS-232C Tx driver input goes low. The MAX232 driver transmits a high-level mark signal. In this way, Q_1 and D_1 simply provide a route from Rx to the I/O pin when the circuit receives characters without echoing them, and the μ C itself also transmits characters. R₁ is necessary only if no internal pullup resistor is available. You can use this type of circuit for service purposes in many designs, such as to connect a PC to a pin of a μ C. At startup, the μ C sends a short message to the PC. Then, the PC sends initialization or debugging parameters to the μ C. During normal operation, the μ C reports its actions to the PC by transmitting the appropriate data. If the circuit has a pin with edgetriggered interrupt capability, you can even implement interrupt-driven I/O. (DI #2397).

> To Vote For This Design, Circle No. 340

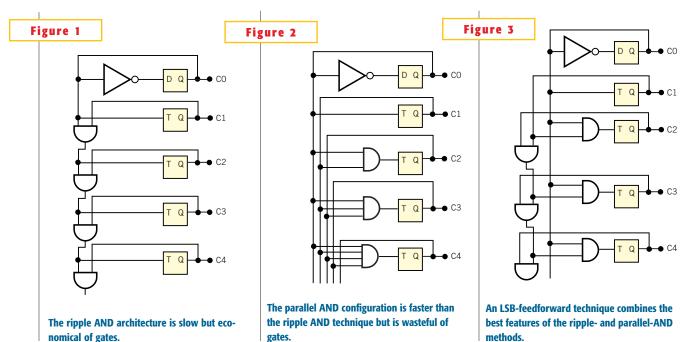
Binary counter uses LSB feedforward

Robert Carter, Siemens PLC, Congleton, Cheshire, UK

TYPICAL SYNCHRONOUS BINARY counter contains a series of flipflops, each of which changes state when all least significant bits (LSBs) are logic 1. This repeated AND function is the Achilles' heel of the binary counter. A designer has two choices: Use a ripple AND function (**Figure 1**), or a parallel AND function (**Figure 2**). The ripple AND function is slow, but the parallel AND function is hugely wasteful of gates and places a large fan-out burden on the LSBs of the counter. Note that, in typical CMOS gate-array technology, AND gates

with more than four inputs are made up of combinations of gates. The configuration in **Figure 3** combines the best features of both approaches.

The key to combining the two methods is to recognize that an AND function, *not* including the LSB of the counter, has two whole clock cycles to complete and then simply bring in the LSB in parallel with a further two-input AND gate. The approach in **Figure 3** is generally beneficial when the counter is wider than 6 bits. This application is for a 32-bit error counter using 2-µm CMOS or a 140Mbps plesiochronous-digital-hierarchy test set. You can extend the technique (to more than 15 bits or so) to propagate the LSBs in parallel; this extension would give the ripple path four clock cycles to settle. The downside of this method is that next-state errors would occur if you needed a resettable counter, though you can usually design out the requirement for such a counter at the system level. (DI #2388)





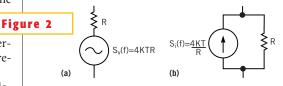
Simple logic reduces EMI

Eugene Palatnik, BCI International, Waukesha, WI

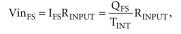
current-input ADC whose primary use is measuring low-level signals from photodetectors can also measure a range of voltages using the circuit in **Figure 1**. The main component is a dual-input current-integrating ADC, IC₁. IC₂ and IC₃ provide the

buffered 4.096V reference for IC₁. The **figure** does not include a μ C, which typically oversees the digital control and data retrieval.

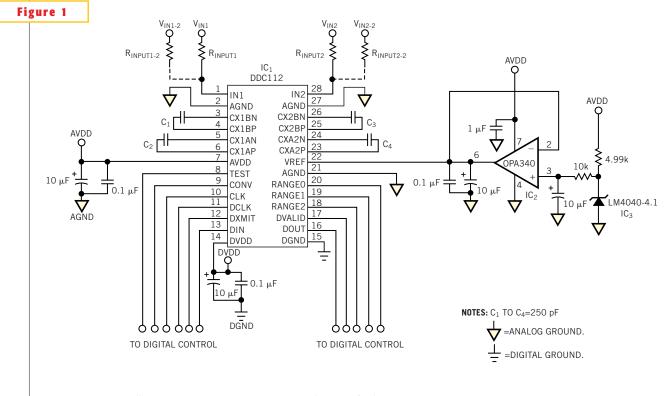
When you use IC₁ with photodetectors, this ADC integrates the currents at input pins 1 and 28 for a user-controlled integration period, T_{INT} , IC₁ then digitizes the output voltages of the integrators into 20bit digital words that are ready for retrieval over the serial interface. The only modifications necessary to enable IC_1 to measure voltages are resistors in series with the inputs. IC_1 's integrators hold the input at a virtual ground, so the applied voltages produce currents through the resistors, which by Ohm's law equal V_{IN}/R_{INPUT} . The full-scale voltage input for the circuit in **Figure 1** is



The spectral density of the voltage noise, $S_v(f)$, is proportional to the value of resistance (a), but the spectral density of the current noise, $S_i(f)$, is inversely proportional to the value of resistance (b).



where I_{FS} is the full-scale input current; Q_{FS} is the full-scale range of IC₁ in coulombs, set by pins RANGE₀ to RANGE₂; and T_{INT} is the user-controlled integration period. R_{INPUT} 's value should be large, preferably greater than 10 M Ω . Avoid using resistors with poor voltage co-



Series input resistors allow a current-input ADC to measure a wide range of voltages.

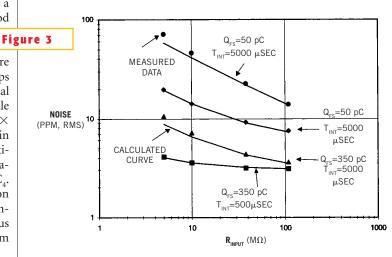


efficients and excess noise. Caddock Electronics Inc (www.caddock.com) offers a variety of high-value resistors with good performance.

Eight full-scale ranges are available in IC₁. Seven of these ranges are internal ranges of 50 to 350 pC in steps of 50 pC. The eighth range uses external capacitors C_1 to C_4 to establish a full-scale range approximately of 0.96× $V_{REF} \times C_{EXT}$. For the 250-pF capacitors in Figure 1, this external range is approximately 866 pC. Surface-mount COG capacitors are a good choice for C_1 to C_4 . The CONV Pin of IC, sets the integration time. In a typical configuration, the minimum integration period for continuous operation is 500 µsec, and the maximum period is 1 sec.

The circuit exhibits a number of useful features. First, the dynamic range of the circuit is large: IC1 outputs 20-bit words. Adjusting $Q_{\rm FS}$ and $T_{\rm INT}$ provides additional dynamic range. The circuit can measure voltages that span more than seven orders of magnitude using a fixed value of R_{INPUT}. Second, the virtual ground at IC₁'s inputs allows you to place additional resistors in parallel, such as $R_{INPUT1-2}$ and $R_{INPUT2-2}$, to measure the sum of the applied voltages. And, because IC, is a dual-input ADC, the circuit can simultaneously make two independent voltage measurements. Finally, the largevalue resistors in series with IC,'s inputs allow the circuit to measure large voltages. For example, if $R_{INPUT} = 100 \text{ M}\Omega$, then a voltage of 100V produces only a 1µA current, which IC, can easily measure. When using large voltages, make sure that the resistors are rated to handle the voltages and that the pc-board layout provides the proper spacing for insulating the high-voltage lines.

At first glance, you might think that the large resistors in series with IC_1 's inputs contribute a lot of thermal noise. Fortunately, the noise that these resistors produce is usually low and decreases as the resistor values increase. To see why this surprising behavior occurs, consider two identical noise models of a resistor (**Figure 2**). The model in **Figure 2a** is probably more familiar and shows the



This plot of noise performance versus R_{INPUT} for different values of T_{INT} and Q_{FS} includes both measured and calculated results.

resistor modeled as a voltage source in series with a noiseless resistor. The spectral density of the voltage noise, S₁(f), is proportional to the value of resistance. The Thevenin-equivalent model in Figure 2b comprises a current source in parallel with a noiseless resistor. In this case, the spectral density of the current noise, $S_i(f)$, is inversely proportional to the value of resistance. The bigger the resistance, the smaller the current noise. IC, measures current. The current-noise contribution of the resistor is important, so bigger resistors reduce the noise. Also, the thermal noise power is independent of resistance. (For a detailed explanation of the physics behind thermal and other noise phenomenon, see Reference 1.)

You can use the following expression to calculate the rms thermal noise, where V_{FS} is the integrator's full-scale voltage, not the input signal's full-scale voltage, V_{inFS} in the previous equation:

NOISE(ppm) =
$$10^6 \frac{\overline{v}}{V_{FS}}$$
 =
 $10^6 \frac{\sqrt{\frac{2KT}{R}}T_{INT}}{Q_{FS}}.$

You must add this thermal noise to IC₁'s inherent noise to calculate the total rms noise. **Figure 3** shows noise performance versus R_{INPUT} for values of T_{INT} and Q_{FS} . The **figure** includes measurement points for comparison with the calculated noise performance.

IC₁'s inputs have very high input impedances and can be susceptible to noise pickup unless you use care in laying out the circuit. Try to keep R_{INPUT} as close to the inputs as possible to minimize the length of the input traces. Also, shield the input leads and IC₁ with grounds wherever possible. If noise pickup is still a problem, adjusting the integration period can notch out specific frequencies. For example, setting the integration period to 16.666 msec places a notch in the frequency response at 60 Hz. (DI #2392)

Reference

1. Van der Ziel, Aldert, *Noise in Solid State Devices and Circuits*, John Wiley and Sons, 1986.



Emergency strobe flasher generates 250V

Robert Sheehan, Linear Technology Corp, Milpitas, Corp

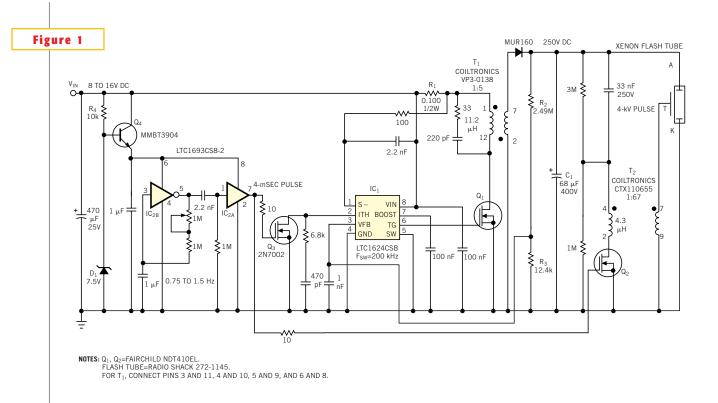
IGURE 1 SHOWS A COMPLETE circuit for an emergency lamp that operates from a 12V automotive battery. The xenon flash tube requires a 250V-dc anode voltage and a 4-kV trigger pulse. To generate the 250V dc, IC₁, a switching regulator controller, and \dot{T}_1 , a standard Versa-PAC transformer, operate in the discontinuous-flyback mode. With this configuration, circuit efficiency is typically 75 to 80%. R1 and IC1's internalsense-threshold voltage limit the peak primary current to 1.6A. The R₂/R₃ divider and IC₁'s internal 1.25V reference at the VFB Pin determine the maximumvoltage setpoint. To generate the 4-kV trigger pulse, a standard cold-cathodefluorescent-lamp (CCFL) backlight

transformer, T_2 , operates in the forward mode. IC₂, a dual MOSFET driver, functions as a 1-Hz oscillator and a one-shot for the trigger pulse for Q₂. Additionally, Q₃ blanks out the operation of the 250V supply during this time. This feature is important because the circuit must reduce the flash tube's anode current to a low level, allowing the tube to reset and wait for the next cycle. Otherwise, the Xenon flash tube may burn out.

The selected flash tube has a maximum flash energy of 4W/sec (joules) and a maximum frequency of 60 flashes/min. Using a $68-\mu$ F capacitor for C_1 , the available flash energy, 1/2CV², is 2 joules, and a flash frequency greater than 1 Hz is possible.

If input voltages below 8V are desirable—for example, when you use a 6V lantern battery—it is important to limit the flash frequency to less than 1 Hz. This limit allows sufficient time for C_1 to charge. The peak primary current, converter switching frequency, and transformer primary inductance determine the charge time: t=($^{1}/_2$ CV²)/($^{1}/_2$ LI²f). You can omit Q₄, D₁, and R₄ and use V_{IN} to power IC, (DI #2393)

To Vote For This Design, Circle No. 343



A complete circuit for an emergency lamp operates from a 12V automotive battery and generates a 250V-dc anode voltage and a 4-kV trigger pulse for the Xenon flash tube.



3.3V lithium-cell supply requires one inductor

Matt Schindler and Jay Scolio, Maxim Integrated Products, Sunnyvale, CA

BECAUSE OF THE GROWING popularity of lithium-ion (Li-ion) batteries and 3.3V power supplies, portable-equipment designers must often create a 3.3V supply that a single Li-ion cell can power. The fact that the output of a Li-ion battery ranges above and below 3.3V during its discharge cycle complicates the design.

This situation calls for a buck/boost converter, which can perform both stepup and step-down conversions. This requirement is not new; for years, portableequipment designers have faced the similar problem of deriving 5V from the output of four NiCd cells.

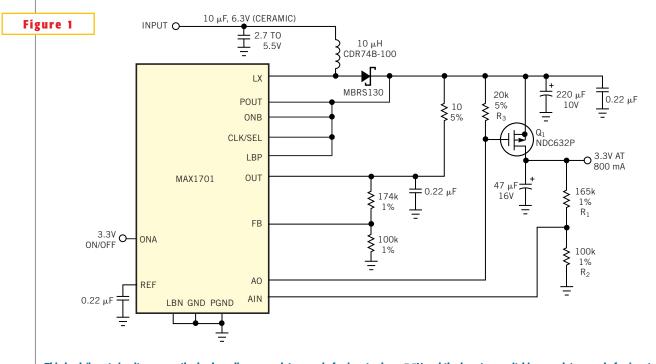
Using a flyback converter is tempting, but the size and expense of a transformer and the extra noise that this converter type creates prompt the search for an alternative. For example, the single-ended primary-inductance converter (SEPIC) is quieter, but this converter's buck/boost circuit has a maximum limited efficiency of 85%. This converter also requires either a transformer or two inductors in place of the single inductor that most dc/dc converters require.

You might overlook an alternative approach because the converter uses a linear regulator and takes an efficiency hit when you fully charge the Li-ion battery to about 4.2V (**Figure 1**). Nevertheless, this approach offers a longer battery life than the other two buck/boost circuits . For a large portion of the Li-ion battery's discharge cycle, battery voltage is within a range that allows the converter to exhibit excellent efficiency.

The operation of the circuit is straightforward. When the input voltage is above 3.3V, the IC stops switching. A linear regulator comprising Q_1 , R_1 , R_2 , R_3 , and an op amp internal to the IC step down the input voltage to 3.3V. When the input is below 3.3V, the IC operates as a step-up switching regulator and boosts the output to 3.3V. For this condition, the MOS- FET is fully on, offering a virtual short from drain to source.

Efficiency is a function of the input voltage and the output current. As expected, the efficiency is a minimum of approximately 78.5% for a peak battery voltage of 4.2V. However, with a 3.6V input and an output current of less than 500 mA, the efficiency is above 89%. This behavior is significant because the output of a Li-ion cell is nearly 3.6V for most of its discharge cycle. For inputs of 3.3 to 3.6V and the same output-current conditions, the efficiency is even higher. Efficiency is also in the same range when the IC operates as a step-up switching converter, which it does for battery voltages below 3.3V. The efficiency gradually decreases as the output current exceeds 500 mA.(DI #2390)

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This buck/boost circuit assumes the buck, or linear-regulator, mode for inputs above 3.3V and the boost, or switching-regulator, mode for inputs below 3.3V.

128 EDN | AUGUST 5, 1999

Edited by Bill Travis and Anne Watson Swager

Circuit monitors quad supply for PCI systems

Roger Zemke, Linear Technology Corp, Milpitas, CA

ANY MODERN SYSTEMS operate with multiple power supplies that must meet tight tolerances to accommodate high-end μ Ps and peripherals. For instance, PCI applications may use as many as four supplies: 5V, 3.3V, and ± 12 V. The circuit in **Figure 1** can monitor all these voltages for an undervoltage condition and can also monitor the three positive voltages for an overvoltage condition. The LTC1536 has a built-in ability to monitor the 3.3 and 5V

levels and one adjustable level for undervoltage conditions. The adjustable input of the IC monitors the 12V supply. The LTC1536 also acts as the logic input for the open-drain outputs of the LTC1444 quad comparator.

ideas

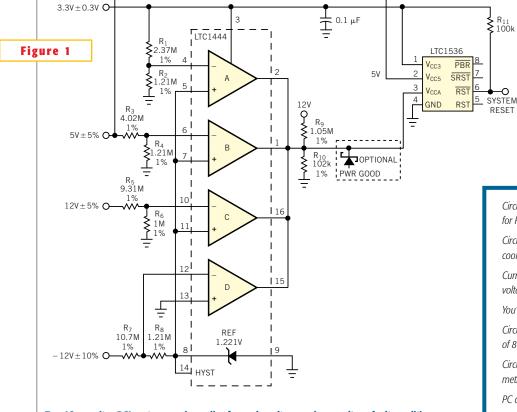
Comparators A, B, and C of the LTC1444, along with resistors R_1 through R_6 , monitor the 3.3, 5, and 12V positive supplies, respectively, for an overvoltage condition. The nominal overvoltage trip points are 3.61, 5.28, and 12.6V. Com-

parator D, aided by resistors R_7 and R_8 , monitors the -12V supply for an undervoltage condition. The nominal trip point for the -12V supply is 10.8V. The open-drain outputs of all the comparators, tied together, connect to the adjustable input of the LTC1536. The resistor divider comprising R_9 and R_{10} provides a pull-up function for the opendrain outputs. The divider also sets up the 12V undervoltage trip point, which is nominally 11.3V. A Schottky diode tied

to the LTC1536's adjustable input can provide another logic input, such as a Power-Good signal. If any undervoltage or overvoltage fault conditions occur, the LTC-1536 issues a reset until 200 msec after the fault condition goes away. (DI #2403).

To Vote For This Design, Circle No. 411

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Two ICs monitor PCI-system quad supplies for undervoltage and overvoltage fault conditions.



Circuit controls multiple thermoelectric coolers

By Frank Effenberger, Bellcore, Morristown, NJ

PTOELECTRONIC AND OTHER COMponents sometimes use a thermoelectric cooler and a thermistor for temperature control. A typical thermoelectric cooler has 1A maximum current and 1Ω impedance. These parameters make simple series-pass drive circuits inefficient, given the typical available supply voltages (5, 12, or 15V). Often, several thermoelectric coolers exist in a single circuit (for example, a multiple-wavelength optical transmitter). In this case, you can obtain improved efficiency by using the circuit in Figure 1. This circuit has three devices to cool, so it contains three coolers and three thermistors. On the sensor side, each thermistor connects to a standard proportional-integral-differential op-amp or µP-based-controller circuit. Each controller produces a command voltage that is proportional to the current its respective cooler requires.

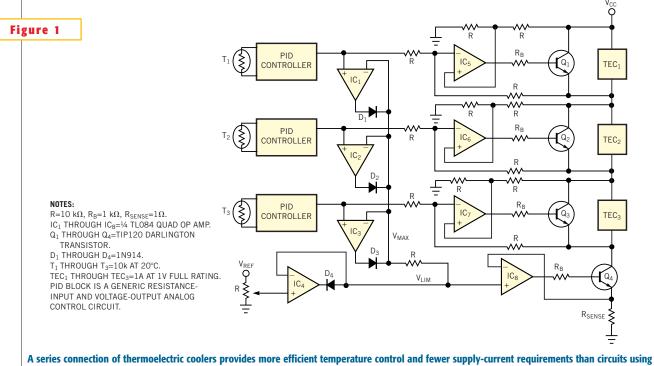
The command voltages drive precision rectifier circuits (op amps IC_1 to IC_3) that generate the maximum control V_{MAX} . Op

amp IC_4 limits V_{MAX} , thus allowing you to control the maximum current delivered to the coolers. This limited output, V_{LIM}, is the input to the main transistordriver amplifier, IC₈. V_{11M} commands the main transistor to pass a current corresponding to the largest demand, subject to the limit constraint. The thermoelectric coolers connect in series, and this chain receives its current via the main series-pass transistor Q4. IC8 drives this transistor such that the voltage drop across $R_{_{\rm SENSE}}$ equals $V_{_{\rm LIM}}$. You choose $R_{_{\rm SENSE}}$ to equal the impedance of one cooler. The coolers have shunt transistors $(Q_1 \text{ through } Q_2)$ that divert any excess current around the individual coolers. The shunt transistors receive their drive from op amps IC₅ through IC₇, which are connected as difference amplifiers. The op amps drive the shunt transistors such that the voltage across each thermoelectric cooler equals the command voltage for that cooler.

Because the sense resistance equals that

of the coolers, the current passing through each cooler assumes the correct value. The actual values of the differenceamplifier resistors, R, and the transistorbase resistors depend on the type of op amps and transistors you select. In most cases, the desired cooler currents have an average value, $\mathbf{I}_{\mathrm{MEAN}}$, and a maximum value, I_{MAX}, that are almost equal. If you cool N coolers using separate circuits, the supply needs to deliver $N \times I_{MFAN}A$. Using the series-connected circuit, the supply current reduces to just I_{MEAN}. Even in the case in which you an optimize the supply voltage for either circuit, the power dissipation for the series-connected circuit is lower because it drops a smaller fraction of the supply voltage through the series-pass transistor. (DI #2395).

> To Vote For This Design, Circle No. 412



individual cooler controllers.



Current-input ADC measures voltages

Jim Todsen, Burr-Brown Corp, Tuscon, AZ

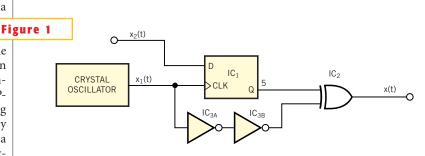
PRACTICAL REALIZATION of a spread-spectrum technique lowers a μ P's clock-related EMI by approximately 4 dB without the drawbacks associated with modulation (**Figure 1**). The spread-spectrum technique is a popular method to reduce μ P-clock-related EMI (**Reference 1**). Using this method, the μ P's clock frequency constantly shifts around and creates a moving target for quasipeak EMI detection. Although this method dramatically reduces measured EMI, it has a few drawbacks.

The first drawback is an unpredictable clock frequency. Peripheral devices that

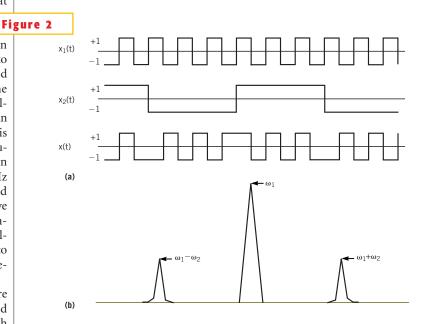
share the same clock with the µP and rely on a stable clock frequency might suffer. One example is an ADC that relies on direct µP control to define the sampling time. The second drawback is the periodic nature of the frequency shift. The technique essentially modulates the clock frequency with an approximately 50-kHz frequency. This frequency is slightly higher than the audio band to prevent audio "hum." In some systems, however, this 50-kHz modulation frequency may be in band with data-acquisition or other sensitive analog circuitry. Under these circumstances, separate nonmodulated digitalcontrol and clock signals are necessary to prevent demodulation of 50-kHz frequency and to prevent analog noise.

Consider the product of two square signals with unity amplitude, $x_1(t)$ and $x_2(t)$, where $x_1(t)$ is a square signal with frequency ω_1 and $x_2(t)$ is a square signal with frequency ω_2 in radians (**Figure 2a**). The Fourier transforms of square waves $x_1(t)$ and $x_2(t)$ are:

$$\mathbf{x}_{1}(t) = \frac{4}{\pi} \begin{bmatrix} \sin(\omega_{1}) + \frac{\sin(3\omega_{1})}{3} + \\ \frac{\sin(5\omega_{1})}{5} + \cdots \end{bmatrix}, \text{ and }$$







Multiplying $x_1(t)$ by $x_2(t)$ produces x(t) (a). In the frequency domain, the multiplication causes the original main frequency component, ω_1 , to split into two equal components (b).

$$x_{2}(t) = \frac{4}{\pi} \left[\frac{\sin(\omega_{2}) + \frac{\sin(3\omega_{2})}{3}}{\frac{\sin(5\omega_{2})}{5} + \cdots} \right].$$

The Fourier transform of the product of x,t and x,t is:

$$\begin{aligned} \mathbf{x}(t) &= \mathbf{x}_1(t)\mathbf{x}_2(t) = \\ & \frac{4}{\pi} \left[\frac{\sin(\omega_1)\sin(\omega_2) + \frac{\sin(3\omega_1)\sin(\omega_2)}{3} + }{\cdots + \frac{\sin(3\omega_2)\sin(\omega_1)}{3} + \cdots} \right]. \end{aligned}$$

You can limit the series to the first term

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for simplification:

$$\begin{aligned} \mathbf{x}(t) &= \frac{4}{\pi} \sin(\omega_1) \sin(\omega_2) = \\ &\frac{4}{\pi} \bigg[\frac{1}{2} \cos(\omega_1 - \omega_2) - \frac{1}{2} \cos(\omega_1 - \omega_2) \bigg]. \end{aligned}$$

If ω_1 is the frequency of the crystal oscillator and ω_2 is the result of the frequency division of ω_1 by 128, for example, then you can rewrite the previous equation as follows:

$$\mathbf{x}(t) = \frac{4}{\pi} \sin(\omega_1) \sin\left(\frac{\omega_1}{128}\right) = \frac{4}{\pi} \left[\frac{1}{2} \cos\left(\omega_1 - \frac{\omega_1}{128}\right) - \frac{1}{2} \cos\left(\omega_1 + \frac{\omega_1}{128}\right)\right].$$

In other words, the frequency peak of $x_1(t)$ multiplied by $x_1(t)/128$ splits into two frequency peaks separated by $2 \times \omega_1/128$. Each peak has half of the energy of the original ω_1 peak. **Figure 2b** shows a Matlab-generated spectrum of $x_1(t)$ and x(t).

Multiplying the nth harmonic of the original $x_1(t)$ signal by x_2t splits the nth harmonic into two major frequency components with frequencies $n \times \omega_1 + \omega_1/128$ and $n \times \omega_1 - \omega_1/128$. (These product

terms are the most significant.) If $x_2(t)$ is purely sinusoidal and the frequency analyzer has an unlimited narrow frequency bandwidth, the initial $x_1(t)$ nth harmonic splits into two frequency spikes. Each of these spikes is approximately 6 dB μ V, or two times, lower than the initial frequency spike. In practice, you can obtain a 4-dB μ V reduction. In many cases, this reduction is a lifesaver because it helps the circuit pass an EMI test, particularly when bulky ferrites on each cable turn your portable electronic device into a boat anchor.

Figure 1's circuit realizes this technique using a few simple logic gates. You can obtain $x_{2}(t)$ from the μP timer or the counter by dividing $x_1(t)$ by any number—in this example, 128. Flip-flop IC, locks $x_{2}(t)$ to the crystal oscillator's phase. The XOR gate, IC,, is the key element. Algebraic multiplication of signals $x_1(t)$ and $x_{2}(t)$ in **Figure 2a** is equivalent to the XOR function of $x_1(t)$ and $x_2(t)$ when they are "logic" signals. IC_{3A} and IC_{3B} compensate for IC₁'s propagation delay. The output of IC, routes directly to the clock input of the µP. The resulting signal x(t) experiences two phase shifts over one period of $x_{a}(t)$ (Figure 2a). The first

shift of 180° occurs during $x_2(t)$'s transient from logic 0 to logic 1; the second shift of -180° occurs during the transient from logic 1 to logic 0.

From the μ P's perspective, the clock signal loses one full period of $x_1(t)$ over one full period of $x_2(t)$. In this example, if you program the μ P's internal timer to 127 cycles, the clock counts 128 cycles of the original crystal frequency.

If you use this technique, you can easily predict the μ P's clock behavior. For example, sampling with every period of $x_2(t)$ introduces no noise into the ADC's reading. The frequency content of the digital clock and other digital signals contains no low frequencies, such as 50 kHz, so the digital clock does not cause any noise in the analog sections. (DI #2391)

Reference

1. Bolger, Steve, and Samer Omar Darwish, "Use spread-spectrum techniques to reduce EMI," *EDN*, May 21, 1998, pg 141.

> To Vote For This Design, Circle No. 413

You've got mail

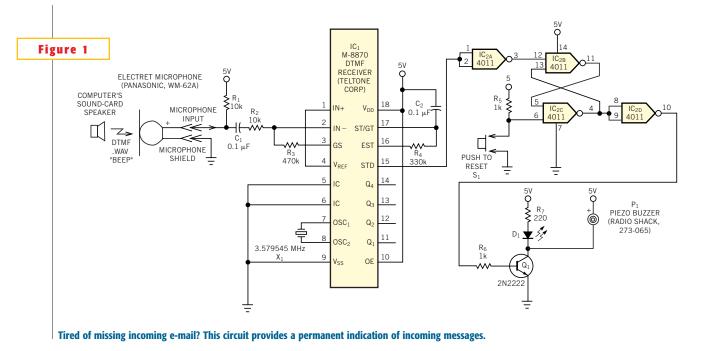
by Gary Kath and Craig Bishop, Scotch Plains, NJ

ANY E-MAIL PROGRAMS provide a "beep" or a pop-up message box signaling the user that a new e-mail message has arrived. If the you are too far from the computer to hear the audible signal or if the monitor is turned off, then you miss the new-mail audible and visual signals. The simple circuit in **Figure 1** (see pg 136) latches on an LED and an audio sounder when an appropriate new audible e-mail signal occurs. The method replaces the normal e-mail sound.wav file with a .wav file of any valid recorded dual-tone multifrequency (DTMF) sound. The circuit listens for the DTMF

tone and latches on LED D_1 and the piezoelectric buzzer, P_1 . R_1 biases the microphone's FET, and C_1 couples the audio to the M-8870 DTMF-receiver, I C_1 (Teltone Corp, www.teltone.com). I C_1 integrates both bandsplit-filter and decoder functions into an 18-pin DIP.

Resistors R_2 and R_3 configure the onchip differential amplifier for a gain of 47. The 3.579545-MHz crystal, X_1 , provides a precise clock generator for IC₁'s digitalcounting decoding circuitry. R_4 and C_2 provide an RC guard time to place accept and reject limits on tone duration. IC₁'s STD output switches to logic high for the duration of any valid DTMF tone. The NAND gate, IC_{2A} , inverts this logic signal and then directs it to a latch configured with NAND gates IC_{2B} and IC_{2C} . Pushbutton switch S_1 resets the latch. IC_{2D} buffers and inverts the latch's output and drives a 2N2222 transistor, Q_1 , thereby turning on the LED and the piezo buzzer. The circuit latches for any valid DTMF tone. You can add additional circuitry to use the M-8870's 4-bit binary outputs, Q_1 to Q_4 if you need to discriminate between DTMF tones. (DI #2399).





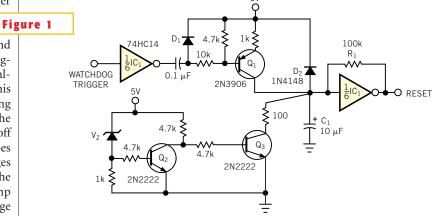
Circuit provides brownout control of 80C31

By N Kannan, Mediatronix, Pappanamcode, India

N THE RESET and watchdog-timer circuit in **Figure 1**, IC_1 is a 74HC14 Schmitt-trigger inverter that, with R_1 and C_1 , acts as an astable oscillator. The circuit provides an active-high reset for an 80C31 μ C. The watchdog trigger (WDT) consists of watchdog-trigger pulses from a port line. At poweron, the voltage on C_1 is 0V, and re-

set=1. As C_1 charges, reset goes low, and the μC generates watchdog-trigger signals. These ac-coupled pulses periodically turn on Q_1 and charge C_1 to V_{CC} . This action prevents C_1 from discharging through R_1 when reset is low. If the watchdog-trigger pulses stop, Q_1 turns off and C_1 discharges through R_1 , reset goes high, resetting the μC . Now, C_1 charges through R_1 , and reset goes low after the reset period. D_1 prevents charge-pump action, and D_2 provides a fast discharge path for C_1 when the supply goes down. The Q_2 - Q_3 combination acts as a lowvoltage reset circuit. When V_{CC} decreases to less than approximately 4.5V, Q_2 turns off and Q_3 turns on, discharging C_1 ; reset then goes high. The circuit works with voltages as low as 1.5V. During power-up and -down, hysteresis of the inverter pro-

vides a clean reset signal. (DI #2400).







Circuit emulates mechanical metronome

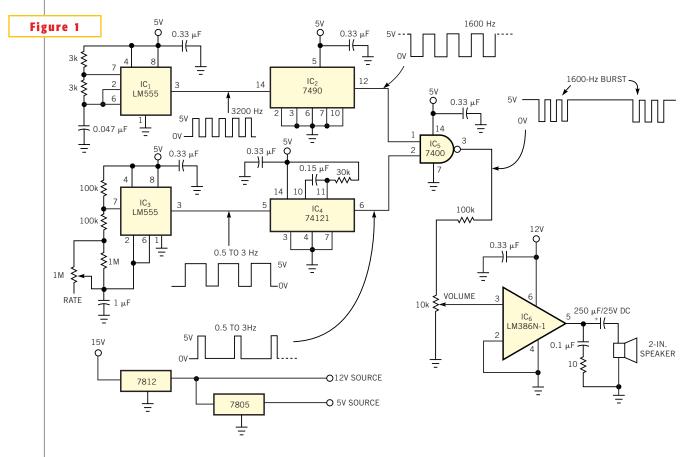
Jim Kocsis, Allied Aerospace, South Bend, IN

HE CIRCUIT IN Figure 1 produces timing signals with a sound like that of a mechanical metronome. IC, is a 555 timer that oscillates at approximately 3200 Hz. The two 3-k Ω resistors and the 0.047-µF capacitor set the frequency. IC, divides the frequency of IC,'s output by 2. IC, produces a square wave with an exact 50% duty cycle. The frequency of the output of IC, determines the sound of each beat. A higher frequency yields a sharper sound, like beating on a small drum; a lower frequency produces a deeper sound, like beating on a large drum. You can adjust the sound by changing the values of the 3-k Ω resistors or the 0.047-µF capacitor. The square wave from IC, is always present on Pin 1

of IC₅. IC₃ is a low-frequency oscillator that runs from approximately 0.5 to 3 Hz. This oscillator determines the rate or speed of the beat. The two 100-k Ω resistors, the 1-M Ω potentiometer/resistor pair, and the 1- μ F capacitor determine the oscillator frequency.

For every rising edge from IC₃, the IC₄ one-shot produces one low-to-high-tolow output pulse. The 30-k Ω resistor and the 0.15- μ F capacitor determine the length of IC₄'s output pulse. This pulse is approximately 2 msec long with the values shown. The output from IC₄ allows three to four pulses from IC₂ to pass through to the output of IC₅. When IC₅'s Pin 2 is high, the pulses from IC₂ appear at IC₅'s Pin 3; when Pin 2 is low, no pulses appear at Pin 3. From IC_5 's Pin 3, the series of pulses routes to the volume control and then to the power audio amplifier. All the circuitry except IC_6 uses a 5V supply. IC_6 needs a 12V supply to drive the speaker loud enough to hear over the sound of an instrument. If you want a visual indication of the beat, you can connect an npn transistor, with a 470 Ω series base resistor, to IC_4 's Pin 6. An LED in series with a 470 Ω resistor from the collector to 5V produces the visual indication. (DI #2404).

> To Vote For This Design, Circle No. 416



Sounding just like an old-fashioned metronome, this circuit sets the cadence for your music practice.



PC controls light dimmer

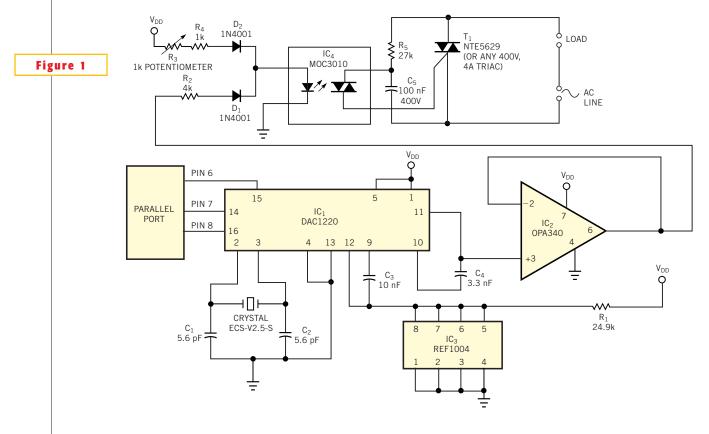
Afshin Mellati, Burr-Brown Corp, Tucson, AZ

SING THE SIMPLE circuit in Figure 1, you can control the light intensity in your room or work area from your PC. The heart of the circuit is a low-power D/A converter that converts digital words from a computer's parallel port to analog-voltage signals. To isolate the dc low-voltage part of the circuit from the high-voltage part, the circuit uses an optoisolator, which prevents any direct electrical connection between the two sections. The optoisolator triggers triac T₁ which behaves like a switch. In each power cycle, T₁ switches on, the ac supply voltage connects to the load (lamps), and current starts flowing in the triac. At the end of a half-period, when the current drops to zero, T, turns off and awaits another trigger in the opposite direction. This additional trigger occurs in the second half-period of the power cycle. A lower triggering voltage makes T_1 conduct at an earlier point in and stay on for a larger fraction of the cycle. The larger fraction corresponds with transferring more power to the lamp, resulting in a higher intensity.

The output voltage of the D/A converter sets the triggering point. The DAC, after one stage of buffering, provides enough current to drive the optoisolator. IC₃ generates a 2.5V reference; the crystal oscillator and capacitors C₁ through C₄ set the DAC's timing characteristics. The DAC1220 (Burr-Brown Corp, www.burr-brown.com) connects to the parallel port with three wires for serial transfer of the digital codes. The Pascal program of **Listing 1** (pg 142) reads the PC's keyboard; when you press Q or W,

the routine increments or decrements a digital code and sends it to the DAC. The DAC then controls the lamp's intensity. Upon power-up, the DAC receives a digital code of zero, which corresponds to a 2.5V output (the reference voltage). You then adjust potentiometer R₃ such that the lamp is half on. Using the keyboard, you can change the light intensity to the desired level. The dc part of the circuit consumes only approximately 5 mA. Listing 1 is available for downloading from EDN's Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea 2401. (DI #2401).

> To Vote For This Design, Circle No. 417



Set your computer area's lighting intensity from the comfort of your swivel chair, using keyboard commands. A simple Pascal routine and some lowcost components do the trick.

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	LISTING 1–PC-CONTR	OLLED LIGHT DIMMER		
Program proj1; uses CRT,Strings;		else PORT[wraddr]:= ibte OR 16; {set sdin=1} ibte:=PORT[wraddr]; PORT[wraddr]:= ibte AND 191; {set scik=0}		
procedure writedata(dwor var wraddr,readdr,strbaddr	•	end; end;		
F	^word; byte;	{*************************************		
to20,to28,num,data	: longint;	var inpkey : char;		
begin pPrintPort := Ptr(\$40,\$08); wraddr := pPrintPort^;		num,num1 : longint; label start; begin num := 0;		
to20:=\$100000; to28:=\$10000000; num:=to20*\$40 + dword;		start: inpkey := readkey; if inpkey = 'q' then begin		
for n:= 1 to 32 do	lize to cs=0, scik=0, sdin=1}	if (num+\$1000)>\$7fff0 then num:=\$7fff0 else num:=num+\$1000; end:		
begin ibte:=PORT[wraddr]; PORT[wraddr]:= ibte 0 num:=num*2:	PR 64; {set scik=1}	if inpkey = 'w' then begin if (num-\$1000)<-\$7fff0 then num:=-\$7fff0		
bit:=0; if num >= to28 then		else num:=num-\$1000; end; if instant = tal then exift		
begin bit:=1; num:=num-to28:		if inpkey = 'x' then exit; if num<0 then num1:=\$fffff+num else num1:=num;		
num:=num-to20; end; ibte:=PORT[wraddr]:		writedata(num1); goto start		
	raddr]:= ibte AND 239 {set sdin=0}	end.		

Edited by Bill Travis and Anne Watson Swager

DDS device provides amplitude modulation

Mary McCarthy, Analog Devices, Limerick, Ireland

ANY APPLICATIONS REQUIRE an analog output to assume different amplitudes, but many direct-digital-synthesis (DDS) devices do not accommodate amplitude variations. Test equipment uses DDS devices to generate signals of different frequencies. However, the amplitude of these signals often must be variable, too. In communication systems, such as base stations, it is essential that the system does not deliver sig-

nals until data is ready to transmit. Between transmissions, the amplitude of the DDS-device output must decrease to near zero. In addition, many applications require AM. Some DDS devices have onboard amplitude registers that allow you to vary the magnitude of the analog output. However, you can also use DDS devices that do not have AM registers (**Figure 1**). The method involves varying the onboard DAC's current.

The onboard DAC for many DDS devices is a current-source type. The reference current to the DAC is a function of the reference voltage, V_{REF} , and an external resistor, which you normally tie from

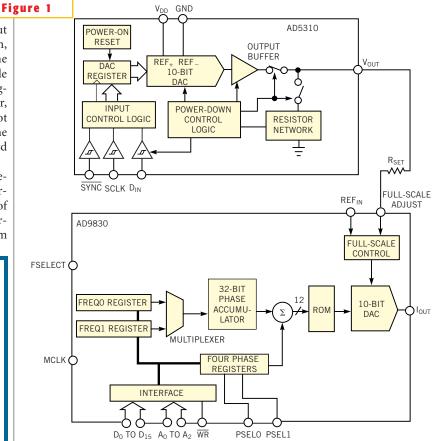
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the DAC to ground. The reference current is V_{REF}/R_{SET}. The full-scale current from the DAC is a multiple of the reference current; the multiple is a function of the size of the transistors in the DAC. For example, the full-scale current of an AD9830 is $16 \times V_{REF}/R_{SET}$. If you do not tie R_{SET} to ground but tie it instead to some varying voltage, V, the full-scale current is $16 \times (V_{REF} - V)/R_{SET}$. Varying V

^{gn}ideas

varies the full-scale current and, therefore, the voltage output from the DDS device. You can provide the varying voltage by using a voltage-output DAC.

In **Figure 1**, an AD5310 provides a variable voltage to the AD9830. With the DAC output at 0V, the DDS device has maximum full-scale current. Increasing the voltage output from the AD5310 reduces the full-scale current of the AD-

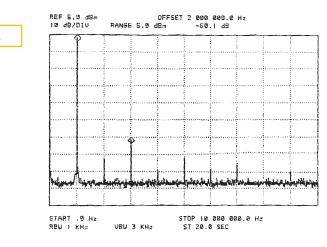


By using a voltage-output DAC, you can obtain amplitude modulation in a DDS device that does not provide for variable output voltages.



9830. The AD9830 uses a 1-k Ω R_{SFT} and a nominal V_{REF} of 1.21V, yielding **Figure 2** a 19.36-mA full-scale current. Figure 2 shows the output spectrum of the DDS device with this full-scale current. The master clock to the DDS device runs at 50 MHz, and the DDS device produces a 1-MHz output signal. The spuriousfree dynamic range (SFDR) is typically 60 dB. Loading code 223 into the DAC generates a 1.089V output voltage. This voltage results in 1.936-mA full-scale current (reduced by a factor of 10) from the AD9830. With this full-scale current and the same clock and frequency conditions as above, the SFDR remains unchanged.

The AD5310 is a 10-bit DAC with integral nonlinearity of ± 2 LSB. It is suitable for use with the AD9830 in test equipment or for amplitude-ramping applications. If you need high-resolution amplitude modulation of the DDS device's output, you need a more accurate



The spurious-free dynamic range for the amplitude-modulation system is 60 dB.

DAC. The AD8300, for example, is a 12bit DAC with integral nonlinearity of ± 2 LSB, representing a fourfold improvement over the AD5310. The increased accuracy makes this DAC more suitable for systems in which you need finer control over the amplitude variations. Both DACs have a serial interface, so you need only three connections to talk to the DAC. (DI #2396).

To Vote For This Design, Circle No. 336

Charge pump converts V_{IN} to $\pm V_{OUT}$

Ioan Ciasci, Rei Data, Cluj-Napoca, Romania

CHARGE-PUMP IC's ability to pro-₽ duce both V_{IN} and $-V_{IN}$ outputs allows the circuit in **Figure 1** +VOUT1 -Ø 1N5818 C Figure 1 to generate separate positive and negative outputs from a single input volt- V_{IN1} FC V_{DD} age, regardless of the input-voltage poø larity. For example, the circuit allows an C1+ SHDN IC_1 RS-232C interface to generate a dual sup-MAX860 2.2 μF GND $| \rangle$ ply for low-power data-acquisition sys-- V_{OUT1} C1 -OUT tems (if you use TxD as V_{IN}, and you lim--Ø D₂ 1N4148 it $\rm V_{\scriptscriptstyle IN}$ to the $\pm 6\rm V$ maximum that $\rm IC_{\scriptscriptstyle 1}$ can 4.7 μF accommodate). Consider a positive V_{IN}: R₁ 22k ş The positive V_{OUT} appears via D_1 and supplies power to the IC via Pin 8. D, and ł R₁ pull Pin 7 high, which is a condition D_3 (along with other connections) for set-1N5818 ting the chip in its inverter mode. As a re-



quency of 6 kHz (13 kHz for the MAX861) with Pin 1 unconnected and at its maximum frequency of 130 kHz (250 kHz for the MAX861) with Pin 1 connected to Pin 5. To reduce the voltage drops associated with D_1 and D_3 , you can

replace the two Schottky diodes with MOSFETs. (DI #2402).

To Vote For This Design, Circle No. 337

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sult, the circuit produces $-V_{OUT}$ at Pin 5.

along with the Pin-5-to-Pin-6 connec-

tion, is a condition for setting the chip to

its doubler mode. Thus, doubling $-V_{IN}$

produces V_{OUT} at Pin 8. The MAX860 (or

MAX861) operates at its minimum fre-

For a negative V_{IN} , $-V_{OUT}$ appears via D_a . D_a and R_a pull Pin 7 to ground, which,



Electronic SPDT controls two PCs

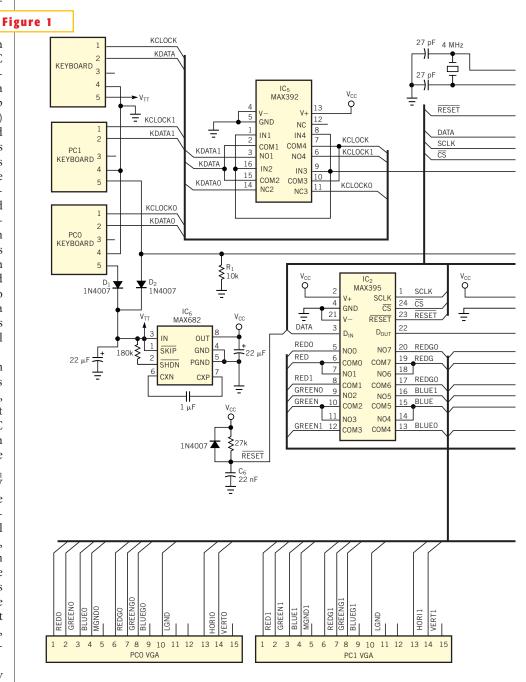
Luis Angulo, Barakaldo, Spain

THE CIRCUIT IN **Figure 1** is a switch that allows you to use one VGA monitor, one mouse, and one keyboard with two PCs. The switch has four pushbuttons. One switches the mon-

itor between the two PCs, a second switches the mouse, a third switches the keyboard, and a fourth connects all the devices to the PC that's inactive at the moment. The active portion of the circuit uses a PIC16F84 µC, IC₁, from Microchip Technology (www.microchip.com) and MAX395 (IC₂, IC₃, and IC₄) and MAX392 (IC₅) electronic switches from Maxim Integrated Systems (www.maxim.com). The μ C is the core of the system; with a simple program, it checks the pushbuttons and selects the proper switches to implement the desired connection. You can download the program from EDN's Web site, www.ednmag.com. Click on "Search Databases/Links Page" and then enter the Software Center to download the file for Design Idea #2375. The µC also drives three LEDs that indicate the PC each peripheral device connects to.

The circuit derives its power from the keyboard connector. If both PCs are initially off, and one switches on, the circuit connects all devices to that one. R, detects the switched-on PC and communicates the switched-on status to the RB2 input of IC₁. The circuit receives its power through D, and D₂. These diodes decrease the 5V supply by approximately 0.7V. The MAX682 step-up regulator, IC₆, restores the 5V for the more critical parts of the circuit. The MAX238, IC₂, provides TTL-to-RS-232C conversion and vice versa for the serial ports. The program initializes the μ C's registers and connects the devices to one of the computers, depending on the level at the RB2 input. It then executes a loop, which ends when you press a pushbutton.

The system detects the newly pressed key and changes the corresponding bit or bits of a register, PC_SEL (PC Select) in the μ C (**Table 1**). The routine then changes the signals, if necessary, to the MAX392, IC₅, for the keyboard selection, and issues a group of bits to configure the MAX395s for the monitor and mouse control. Finally, be-

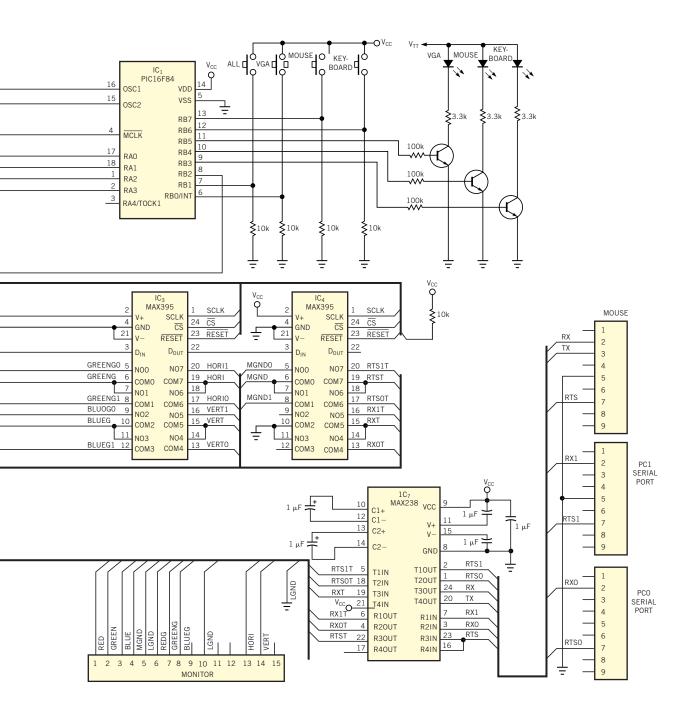


An electronic switch allows you to use a single monitor, mouse, and keyboard to control two PCs.

TABLE 1-	PC_SEL REGIS	STER					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mouse	Keyboard						Monitor

fore returning to the main program loop, the software updates the LEDs, which in-

dicate which PC each device connects to. (DI #2375).





GMR sensors manage batteries

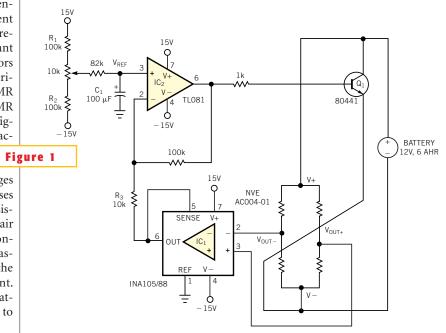
D Ramirez and J Pelegri, University of Valencia, Spain

THE PAST FEW decades have seen remarkable progress in magnetic-sensor technology. Early and current sensors exploit the Hall effect; more recent devices use an effect called giant magnetoresistance (GMR). GMR sensors use semiconductor processing of materials such as indium-antimony. The GMR sensor in **Figure 1** comprises four GMR resistors in a Wheatstone-bridge configuration. Two arms of the bridge have active resistors; the other two resis-

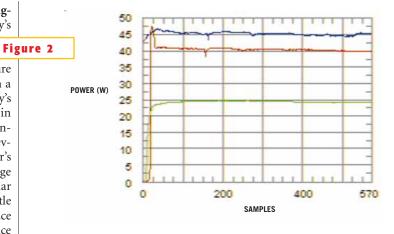
Fi tors are shielded against magnetic fields. When a magnetic field impinges on the sensor, the GMR effect decreases the resistance of the active pair of resistors, and the values of the shielded pair remain constant. GMR-based semiconductors are suitable for current measurement because they respond to the magnetic field rising from the current. However, in this application, the Wheatstone-bridge topology allows you to measure and control power.

All you need to do is connect the power pins of the GMR sensor to the voltage terminal, V+, and place the cable or trace the battery current traverses near the sensor. The output voltage of the bridge then relates to the power, which is the product of V+ and the current. The circuit in Figure 1 provides a way to check a battery's condition. Measuring a battery's voltage is not the best way to check its condition; it's better to measure the power that the battery delivers in a discharge process to evaluate the battery's energy capacity and life. The circuit in Figure 1 discharges a battery in a constant-power mode. You can select the level of discharge power. The GMR sensor's output signal is related to the discharge power. The power stage uses a bipolar Darlington transistor, which draws little power from its op-amp driver. You place the GMR sensor over the pc-board trace that connects the Darlington's emitter to ground.

Using the GMR sensor in a negativefeedback closed loop, the circuit controls the battery discharge in constant-power







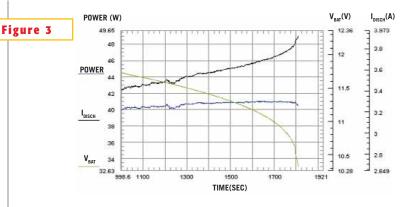


mode. The difference amplifier (IC_1) converts the sensor's differential output signal to a unipolar signal; the op amp,

IC₂, supplies the appropriate loop gain and compares the difference-amplifier output with the externally selected ref-



erence voltage. IC₂ provides the base current for the Darlington transistor, which discharges the battery at a constant-power rate. **Figure 2** shows profiles of the constant-power battery discharge. **Figure 3** shows current, voltage, and power profiles of the constant-power discharge process. When the battery voltage decreases, the current discharge increases, and the power remains constant. (DI #2394).



To Vote For This Design, Circle No. 339

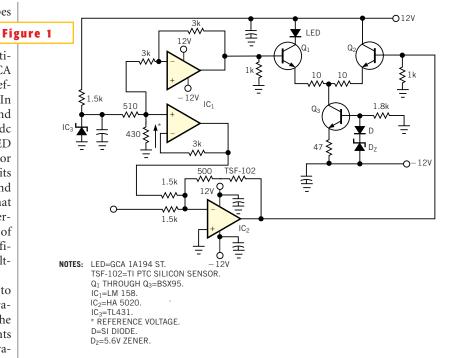


Driver thermally compensates LED

Andrzej Wolczko, University of Mining and Metallurgy, Krakow, Poland

PTICAL POWER OF popular types of LEDs decreases with temperature. Optical-power measurements into a typical multimode fiber at 62.5/125 µm for a GCA 1A194 LED indicate a temperature coefficient of approximately -0.4%/°C. In bipolar analog drivers for short- and medium-distance fiber links with a dc component, you frequently place an LED in the collector of a differential pair. For zero-input signals, the LED emits half its maximum power (zero reference), and the bipolar input signal modulates that power from zero to maximum. Temperature changes cause decreased power of zero reference and decreased slope efficiency of optical power versus input voltage.

The circuit in **Figure 1** allows you to compensate for both of these temperature-dependent problems, using only the TSF-102 sensor from Texas Instruments (www.ti.com). The device is a temperature-dependent positive-temperaturecoefficient resistor with a linear temperature coefficient of approximately $0.7\%/^{\circ}$ C at 25°C. For the circuit in **Figure 1**, you must thermally couple the sensor with the LED. IC₂ is a summing amplifier for the input voltage and the reference voltage from IC₃. The gain is



A positive-temperature-coefficient sensor and a closed-loop amplifier circuit allow a LED to deliver constant optical power over temperature.

-1 and increases with temperature. The temperature-independent $-V_{REF}$ drives the base of transistor Q₂. The thermally stable current source, Q₃, via the differential pair Q₁-Q₃, supplies the LED. Note

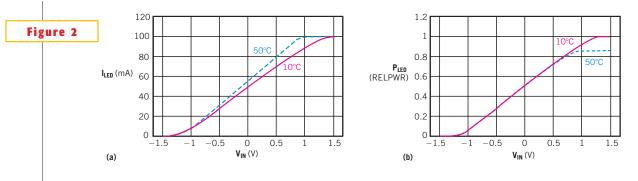
that you should mount Q_3 , D, and D_2 on a common heat sink.

With V_{IN} =0V, temperature changes unbalance the Q_1 - Q_2 pair, such that the optical power remains constant. Empir-



ical measurements show that the compensation is optimal with V_{REF} =1.1V. IC₂ amplifies the input signal by a temperature-dependent factor. You obtain matching of the temperature coefficient of the sensor to the coefficient of the LED by inserting the additional 500 Ω resistor in the feedback loop of IC₂. Figure 2 shows the LED current (Figure 2a) and the optical power (Figure 2b) in the fiber-versus-input voltage for 10 and 50° C. The circuit provides an approximate tenfold decrease in the thermal coefficient. The improvement comes at the cost of a limited input-signal range for linear operation. The circuit has a bandwidth of 0 Hz to more than 10 MHz. (DI #2398).

> To Vote For This Design, Circle No. 340



Using the circuit in Figure 1, an LED uses temperature-dependent operating current (a) to produce nearly constant optical power (b) at 10 and 50°C.

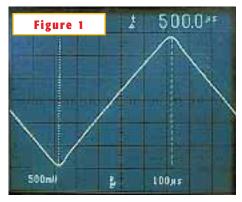
Program turns PC sound card into a function generator

David Sherman, David Sherman Engineering Co, Everett, WA

OU CAN USE a low-cost PC sound card as an analog-function generator by controlling the PC with the program "SoundArb." The program generates standard waveforms, noise, and arbitrary waveforms. The program reads arbitrary waveforms from simple ASCII text files consisting of whitespace-separated numbers. You can use a program such as Mathcad to create such files. SoundArb provides common triggering modes, such as continuous, one-shot, burst, and toggled. An on-screen "button" serves as the trigger input. The program's user interface is a dialogue-box-style controlpanel window. (You can download the self-extracting installation program from EDN's Web site, www.ednmag. com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2409.)

The main advantages of using a

sound card as a standard and arbitrary waveform generator is its low cost and ready availability. The typical 16-bit resolution is better than many arbitrarywaveform generators, the output drive capability is generally good, and you can't



Using a cheap sound card, the SoundArb program produces a 1-kHz triangle wave. Limited high-frequency bandwidth produces the rounding at the points of the triangle wave. beat the price: as low as \$10.

The disadvantages include poor waveform quality, including distortion, noise, and ringing; ac-coupled output only; limited triggering modes, including no external trigger; imprecise amplitude ad-

justment; and the possibility of interruptions in the waveform due to other system demands. All in all, the quality of the generated waveforms depends directly on the quality of the sound card, and the cheapest cards generate the worst waveforms. An oscilloscope photo (**Figure 1**) shows a 1kHz triangle wave such as those generated by cheap sound cards. The photo shows rounding of the points of the triangle wave due to limited highfrequency bandwidth.

SoundArb is a 32-bit application that runs under 32-bit Windows. The program communicates with the sound card through the Windows multimedia application-program-



ming interface, so it should work with most sound cards. SoundArb places relatively light demands on the system, so a fast CPU and large amounts of memory are usually unnecessary. Long arbitrary waveforms may require more memory. Low-cost sound cards rely on the computer's main memory for waveform storage, which means that, if the system is slow or busy, the waveform may be interrupted. The sound card must support the pulse-code-modulation, audio-wave format; must have 16 bits of resolution; and must have a maximum sample rate of at least 44.1 kHz. Although standard sample rates are 10.25, 20.5, and 44.1 kHz, many sound cards support any integer sample rate within a much wider range. Such a card is a more versatile function generator than one that supports only the standard sample rates.

The resolution and full-scale range of the amplitude adjustment depend on the

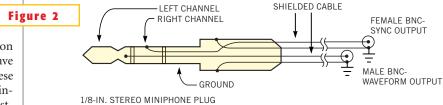
design of the sound card. Unfortunately, no way exists to set the amplitude to a known voltage other than by observing the waveform on an oscilloscope. Many sound cards have relatively few amplitude levels, and these levels do not necessarily follow either linear or logarithmic curves. One card tested provided 16 amplitude steps, including "zero." The remaining 15 steps followed a two-part piecewise-logarithmic curve.

If you have a stereo sound card, SoundArb allows you to use the "right" channel as a "sync" output to mark the start of the analog waveform. Note that a sound card reproduces only audio frequencies. Most provide no dc-coupled output. The output bandwidth typically approximates the 20 Hz to 20 kHz audio band. A good first test of your sound card is to generate square waves of various frequencies and lengths while monitoring the output with an oscilloscope. Low-frequency square waves may show a pronounced droop due to an ac-coupled output, and ringing on the edges may be severe. The amplitude and frequency of the ringing may depend more on the sample rate than on the waveform repetition rate. Much of this depends upon the analog-to-digital-conversion technique that the sound card uses. Take the

time to familiarize yourself with the analog limitations of your sound card before relying upon it for important work. For more information on this, search the online help index for the keyword "Distortion."

To use the sound card for electronic testing, you probably need to make an adapter cable (Figure 2). A convenient way to make the cable is to obtain two male BNC-to-cable connectors, a stereo miniphone plug, and a short shielded wire. Because of the low frequencies involved, you need no coaxial cable. You then connect your normal BNC-to-cliplead test cables to the male BNCs. Alternatively, you can make a longer cable by terminating the right channel in a female BNC, which you can connect to the sync input of your oscilloscope. You can terminate the left channel in an alligator clip or a minigrabber. If you don't use the

Grounding may be less than optimum because no good way exists to connect the PC's ground to the ground of the device under test. If glitches from the sync line are a problem, you may be able to disconnect that line's shield from its BNC shell, assuming that the waveform line's shield remains connected to its BNC's shell. If necessary, you can break a bad ground loop by isolating, or floating, the PC and its monitor from the power-line ground. You cannot use a "cheater" plug because it defeats the safety aspects of grounding and can allow the PC chassis and peripherals to become hot. To isolate the PC from the power line and its ground, use a medical-grade isolation transformer that includes a Faraday shield between the primary and secondary windings. This transformer often reduces interference from noisy power lines and may reduce conducted EMI, es-



A convenient adapter cable comprises two male BNC-to-cable connectors, a stereo miniphone plug, and a short length of shielded wire.

right-channel sync output, you can get by with one BNC and one piece of cable because the program supports only "rightchannel-sync" mode. The tip of the miniphone plug carries the left-channel signal, the first ring carries the rightchannel signal, and the main ring provides the ground. Separate shielded cables, rather than a shielded twisted pair, between each BNC and the phone plug are recommended because with the twisted pair the sync pulse edges capacitively couple into the waveform and cause glitches. As an alternative to using a miniphone plug, most sound cards have an internal waveform output comprising a pin header on the card. Some cards also have jumpers that you can use to select between "line out" and "speaker out," the difference being the output impedance or voltage.

pecially if used with an RF-line-filter block.

Never float the PC or any other test equipment as a way to connect the ground to a high voltage, for example, to connect an oscilloscope probe across a current-sensing resistor in a hot ac power line. Doing so could kill you, and you could destroy expensive test equipment whose power supply was not designed for a ground-to-neutral voltage of more than 30V. If you need to connect test equipment to a high voltage, use optical or magnetic isolation in the signal wires, not in the equipment's power supply. Small, modular isolation amplifiers with low distortion are readily available at reasonable prices.(DI #2409)



Li-ion battery charger adapts to different chemistries

Fran Hoffart, Linear Technology Corp, Milpitas, CA

Rechargeable LITHIUM-ION (Lion) cells require a precise charging voltage for maximum performance. The battery chemistry, of which there are many, determines the optimum charge voltage. Two of the more common charging voltages are $4.1V\pm50$ mV and $4.2V\pm50$ mV per cell.

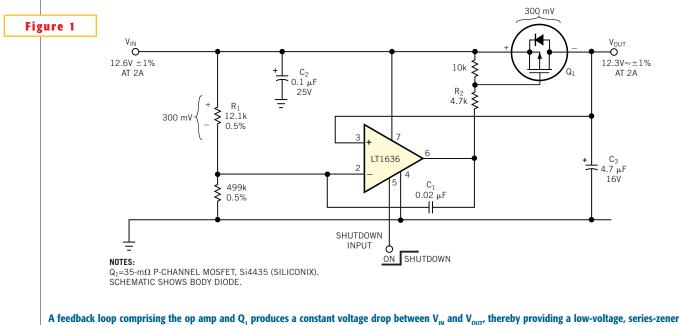
Consider the following situation: You have thousands of three-cell Li-ion battery chargers with an output voltage of $12.6V\pm1\%$. However, because of a battery-chemistry change, your chargers now need $12.3V\pm1\%$. The 12.6V output is well-regulated and has current limiting, but the voltage is 300 mV too high, and you cannot easily adjust it.

The circuit in **Figure 1** can solve this problem by providing a constant 300mV drop between V_{IN} and V_{OUT} at currents as high as 3A. The accuracy of the 300-mV drop is nearly as good as the accuracy of the input voltage, which in this case is approximately 1%. This circuit requires an input voltage that is fixed, regulated, and preferably current-limited. A precision voltage divider across the regulated input derives the 300 mV necessary for the circuit to operate, thus eliminating the need for an external voltage reference. The circuit also includes a logic-level low-quiescent-current shutdown. In shutdown, the series MOSFET, Q_1 , is off, and the total circuit current drops to approximately 8 μ A.

The circuit operates by developing a 300-mV reference voltage across R_1 and applying this voltage to the inverting input of the op amp. The noninverting input connects to the output side of the p-channel MOSFET. The resultant feedback loop forces the voltage across Q_1 to equal the voltage across R_1 , which is 300 mV. In normal operation, the voltage drop across R_1 and Q_1 are equal in value but opposite in polarity, thus forcing the voltage between the two op-amp inputs to be 0V. C_1 provides stability, and

 C_2 and C_3 bypass the supply.

Although this circuit was intended to solve a Li-ion-charger problem, you can use the circuit for any application that needs to drop a constant voltage. Changing the appropriate resistor values allows the circuit to accommodate other input voltages or voltage drops. The voltage drop across R₁ determines the voltage drop between V_{IN} and V_{OUT} . For low input voltages of 5V, reduce R_2 to 470 Ω to ensure adequate gate drive for Q_1 . Q_1 has a low R_{DS(ON)} and comes in an SO-8 surface-mount package. Allow a minimum of 1 sq in. of pc-board copper around the eight leads for heat sinking. Higher voltage drops require additional copper area. For even higher power levels or higher currents, select a MOSFET in a TO-220 package and mount it to an appropriate heat sink. (DI #2408)



type of function.



Edited by Bill Travis and Anne Watson Suager

Current-sense amplifier precisely measures low side

John Ursoleo, Silicon Mountain Design, Colorado Springs, CO

Several INTEGRATED HIGH-side current-sense amplifiers, such as the MAX4172 (Maxim Integrated Products, maxim-ic.com), make it easy to measure the current from a positive power supply. With a couple of resistors, these devices provide a groundreferenced voltage output that is proportional to the delivered current (Figure 1a).

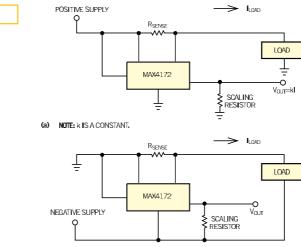
Unfortunately, no equivalent devices implement a true low-side current sense for negative supplies. You can use the high-side devices to measure current from negative supplies, but this approach has drawbacks. The sense resistor must be in the load's ground lead, which effectively floats the load off ground by the sense resistor voltage, and the output voltage, V_{OUP} , is referred to the negative supply and not to ground (**Figure 1b**). Both of these characteristics are undesirable.

The circuit in **Figure 2** implements a true low-side, precision current-sense amplifier that provides a ground-referenced voltage proportional to the

negative supply current and that **Fi** does not float the load off ground. This circuit is similar to the circuit in the

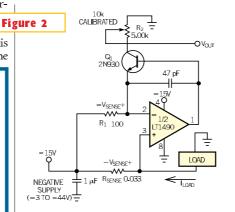


www.ednmag.com



(b) NOTE: LOAD IS NOT GROUNDED, AND $V_{\rm OUT}$ IS REFERRED TO THE NEGATIVE SUPPLY.

High-side current-sense amplifier ICs, such as the MAX4172, make it easy to measure positivepower-supply current (a). Although you can also use these devices to measure current from negative supplies (b), the resultant circuit has undesirable characteristics.



A true low-side, precision current-sense amplifier provides a ground-referenced voltage that is proportional to the negative supply current and does not float the load off ground. MAX4172 but is reconfigured for a negative supply. When current flows through the load, a proportional voltage, V_{SENSE} develops across the current-sense resistor $R_{\text{SENSE}} V_{\text{SENSE}} = I_{\text{LOAD}} R_{\text{SENSE}}$. To stay balanced, the op amp raises its output until V_{SENSE} also appears across R₁. The current through R₁ equals V_{SENSE}/R_1 , which is identical to the current through R₂, which scales V_{OUT} . The equation for V_{OUT} is then as follows:

$$V_{OUT} = -\frac{V_{SENSE}}{R_1} \bullet R_2 =$$
$$I_{LOAD} \bullet R_{SENSE} \bullet \frac{R_2}{R_1}.$$

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To minimize the effects of the op amp's offset voltage, the voltage developed across the sense resistor should be larger than this offset value. The circuit in Figure 2 develops a 0 to -5V output for load currents of 0 to 3A and is accurate to about 1%.

You must adhere to the following component restrictions: The op amp needs to have an input common-mode range that includes the negative rail. The op-amp output needs to be a rail-to-rail type, Q_1 should have a high beta at low currents to minimize errors due to base current. Keep R_1 small so that op-amp bias currents are insignificant. For greater accuracy, you can replace Q_1 with an enhancement-mode n-channel MOSFET to eliminate base-current errors; however, operation as low as 3V is then unlikely. You can also replace the op amp with a lower offset device at the expense of high-voltage operation to -44V. (DI #2410)

> To Vote For This Design, Circle No. 433

Connect a modem to a Basic Stamp

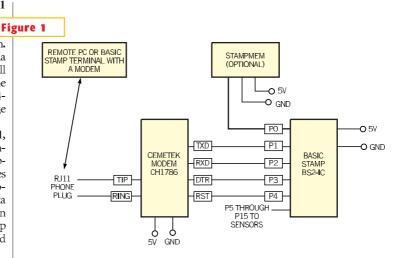
Ken Gracey, Parallax Inc, Rocklin, CA

THE 2400-BPS MODEM in Figure 1 makes it easy to connect a Basic Stamp (Parallax Inc, www. parallaxinc.com) to a telephone modem. Using this circuit, you can call home via your PC and find out if the house is still there. The Basic Stamp2, BS2-IC, has the necessary programming space, and a 64kbyte StampMEM memory-storage board enhances site data collection.

In the setup configuration of **Figure 1**, the Basic Stamp can read data from sensors and store the result on the Stamp-MEM board. When the modem receives a call, the Basic Stamp reads the Stamp-MEM board and transfers the stored data directly to the modem, which in turn sends it to the remote PC or Basic Stamp terminal that has a modem interface and standard communication software.

Simple software code performs data movement to and from the modern. The software collects sensor data and places the modem in an auto-answer mode for a short time and loops back to collect more data. When a remote terminal sends a phone call, the looping stops, and the Basic Stamp answers the phone call by requesting the terminal to type "start." After receiving the typed input from the remote terminal, the Basic Stamp reads the StampMEM data-storage board and transfers the entire stored data to the remote terminal. (You can download the program from EDN's Web site, www. ednmag.com. Click on "Search Databas-

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The 2400-bps modern allows you to connect a modern to a Basic Stamp.

es" and then enter the Software Center to download the file for Design Idea#2411.)

After data transfer is complete, the Basic Stamp hangs up the phone call, returns to collecting sensor data, and awaits another phone call. The software communications between the Basic Stamp, modem, and memory data storage are through the "serin" and "serout" commands. This approach allows the Basic Stamp to use just a few I/O pins, leaving at least 11 pins for the sensors' data input. The program includes no sensor inputs; doing so would complicate the software. The StampMEM memory data storage is unnecessary if you intend to retain the data within the available memory on the Basic Stamp. You can easily connect many data-storage devices and EEPROM chips to the circuit. Sensor and data-storage-device software codes are available for free on the Parallax Web site. (DI #2411)

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Bias supply provides short-circuit protection

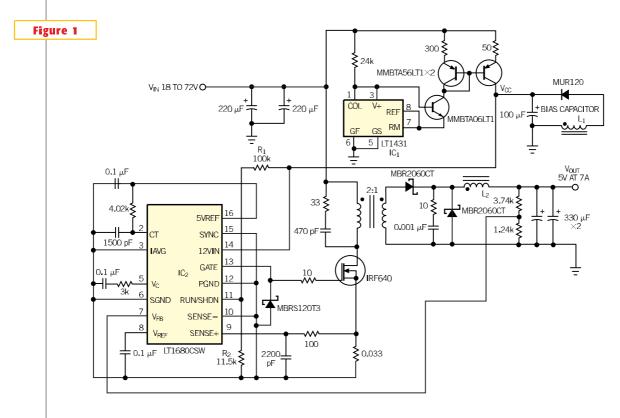
Dave Kim, Linear Technology Corp, Milpitas, CA

OST POWER-SUPPLY DESIGNS require protection from a short-circuit fault condition. One of the methods of short-circuit protection is cycling, or the "hiccup-mode" method. This method is an effective way of controlling a short-circuit fault condition while minimizing power loss in the circuit. **Figure 1** shows a trickle-charged bias supply that uses an LT1431 programmable reference, IC₁, to start an LT1680 high-power dc/dc step-up controller, IC₂, which operates here in a forward-converter topology. This circuit is useful for applications with wide inputvoltage ranges, such as telecommunication applications with input ranges of 18 to 72V.

IC₂'s undervoltage-lockout (UVLO) hysteresis, which you can adjust using the R_1/R_2 voltage divider at the RUN/SHDN pin, sets the short-circuit cycling. An overwinding, L₁, on L₂'s output inductor provides a V_{CC} of 12V. When a short-circuit fault at the output drags V_{CC} down to IC₂'s UVLO threshold, IC₂ shuts down, and a constant bias current starts to charge the bias supply capacitor. IC₁ controls the scaled current mirror that generates a constant current and continually adjusts itself to keep the input of the current mirror at 3 mA. When this constant current charges the bias capacitor to the level of IC₂'s turn-on threshold (approximately 12V), IC₂ wakes up. You can calculate the turn-on delay using the following equation:

 $\frac{T_{\text{TURN-ONDELAY}} = }{\frac{C_{\text{BIAS}} \times V_{\text{TURN-ON THRESHOLD}}}{I_{\text{CHARGE}}}.$

With a constant charging current of 3 mA, the turn-on delay for the circuit is



A programmable reference, IC,, and a bias-capacitor network control the on/off cycling of IC,'s step-up controller during a short-circuit fault condition.

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approximately 400 msec. You can produce shorter turn-on delays by reducing the value of the bias capacitor or increasing the bias current. If you increase the bias current, you must scale the transistors according to their power-dissipation ratings.

Figure 2a shows the bias-capacitor voltage and the output of the forwardconverter voltage during turn-on. When the bias capacitor charges to the turn-on threshold voltage of 12V set by IC₂, the output turns on and the bias capacitor's voltage dips to 11.5V, which is the level that the overwinding sets. Figure 2b shows the bias capacitor and output voltage in cycling mode during a short-circuit fault. IC1 sets the constant current, which charges the bias capacitor to the turn-on threshold, and IC2 starts up. However, the overwinding generates no voltage because of the short at the output. And because IC_2 's quiescent current is greater than the charge current, the bias capacitor discharges. Discharging the bias capacitor to less than the UVLO threshold shuts down IC2. This charging and discharging cycle repeats until you remove the fault.

You can calculate the restart time using the following equation, where V_{RUN} equals the turn-on threshold set by RUN/SHDN:

$$\frac{T_{\text{RESTART}} =}{\frac{C_{\text{BIAS}} \times (V_{\text{RUN}} - V_{\text{UVIO}})}{I_{\text{CHARGE}}}},$$

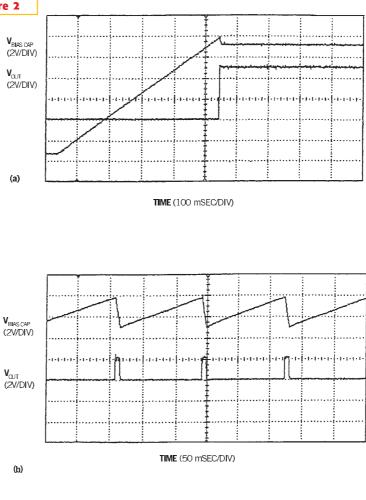
When implementing a cycling type of short-circuit protection, a constraint is on the maximum capacitive load for which the power supply starts. The capacitive load depends on the short-circuit current and the threshold voltage at which the overwinding back-feeds the bias supply. The output rise time of the LT1680 must be less than the holdup time that the hysteresis and the bias capacitor provide.

You can calculate the start-up time using:

$$\frac{I_{OUTPUT RISE} =}{C_{OUT} \times V_{THRESHOLD}},$$
$$\frac{I_{SHORT} - I_{LOAD}}{I_{SHORT} - I_{LOAD}},$$

where

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The output turns on when the bias capacitor reaches 12V (a). During a short-circuit fault, the bias capacitor continually charges and discharges until you remove the fault (b).

$$\frac{V_{\text{THRESHOLD}} = }{\frac{V_{\text{ULVO}} \times V_{\text{OUT}}}{V_{\text{CC}}}}.$$

where I_{RUN} is the current necessary to start up IC₂. The start-up time must be less than the hold-up time for the power supply to start. (DI #2414)

You can calculate the hold-up time using:

$$\frac{T_{\text{HOLDUP}} = }{\frac{C_{\text{BIAS}} \times (V_{\text{RUN}} - V_{\text{UVLO}})}{I_{\text{RUN}}}},$$

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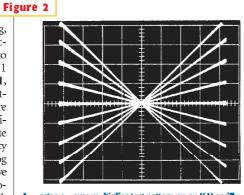
design**ideas**

Analog multiplier works over large frequency range

Hubert Houtman, Consultant, Blaine, WA

SCHOTTKY-DIODE DOUBLE-balanced mixers are common elements in analog and digital telecommuni cations circuits that operate

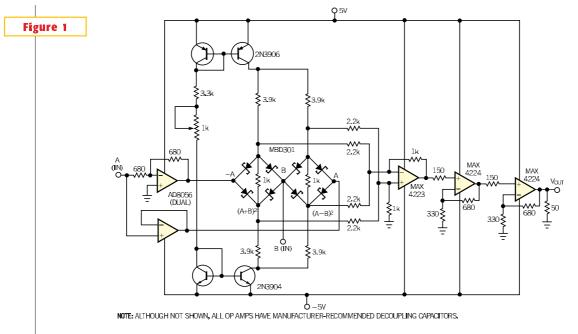
at radio and microwave frequencies. Transistor analog multipliers, such as log-antilog, MOS, and variable-transconductance types, are usually limited to frequencies of much less than 1 GHz. In the circuit in Figure 1, an MBD301 hot-carrier Schottky-diode bridge forms the core of a four-quadrant analog multiplier and, therefore, can operate over a much larger frequency range than can transistor analog multipliers. This highly sensitive double-balanced modulator provides a high-quality output with low spurious-response level. Using the proper high-frequency circuit and IC techniques, you can use this type of circuit for digital and analog communications, radar, product detection, AGC circuits, and phase de-



A quarter-squares multiplier test pattern on an X-Y oscilloscope illustrates good linearity and balanced behavior in all four quadrants. (Horizontal = Input A at 10 mV/div; vertical = V_{our} at 20 mV/div.)

tectors in the radio and microwave bands.

Like many double-balanced mixers and analog multipliers, this circuit has an amplifier, the MAX4223, for the IF. This differential amplifier is the only essential amplifier in the circuit; the MAX4224s are two 10-dB amplifier stages. If you use a balun transformer with a center-tap-grounded secondary in place of the dual AD8056, inputs A and B can be radio or microwave frequencies. With the input amplifiers shown, however, the frequency range for Input A is limited to about 100 MHz. You can use fast transistor amplifiers for the input and the output amplifiers to achieve system bandwidths greater than 1 GHz. You can also use a fast buffer amplifier-such as the MAX4405, which has a 75 Ω output-at Input B for improved port isolation.



An MBD301 hot-carrier Schottky-diode bridge forms the core of a four-quadrant analog multiplier that performs continuous computations of the product of arbitrary input signals A and B.

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This four-quadrant analog multiplier is a quarter-squares multiplier based on the identity:

 $(A+B)^{2}-(A-B)^{2}=4AB.$

The MAX4223 differential amplifier, which has a 1-GHz bandwidth, registers $(A+B)^2$ from the left bridge while subtracting $(A-B)^2$ from the right bridge to form the product:

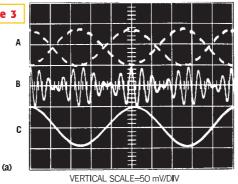
V_{OUT}=AB/K,

where the constant, K, is 12 mV. You can add the carrier at the differential amplifier's input for amplitude modulation as necessary.

The differential output across the $1-k\Omega$ resistor of each diode bridge is a precisely symmetric, even function of the voltage across it: A+B for the left bridge and A-B for the right bridge. Consequently, the bridge's V_{OUT} contains only even terms of the combined Taylor series due to the four diode currents. The constant terms cancel out because the MAX4223 subtracts the bridge outputs, so the dominant term is the square term. Higher order even terms do not contribute, provided that inputs A and B stay at less than approximately 150 mV. For large inputs, each bridge behaves as a full-wave rectifier; the diodes become forward-biased with resistance smaller than the 1-k Ω load, and the parabolic branches ultimately degenerate into straight lines that the load resistor dominates. Therefore, the multiplier is unusable with such large inputs.

The circuit includes a balanced, double current-mirror network that supplies the diode bridge with four bias currents. A single 1-k Ω potentiometer controls the current, and four 3.9-k Ω resistors accurately distribute equal, balanced currents to the two bridges while preventing crosstalk between the bridges. These four resistors also isolate the diode bridges from the transistors, thereby improving system bandwidth.

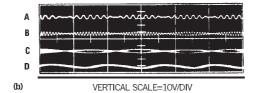
Without this bias-current network, the bridge requires an approximately 5-M Ω load resistor for parabolic behavior. This value precludes this design's use in highfrequency circuits because the currents are extremely small and the time constants are very long when you connect the bridge to an amplifier input of a few



HORIZONTAL SCALE=100 mSEC/DIV

TRACE | DESCRIPTION

A	MULTIPLIER OUTPUT WITH A 12-mV, 20-kHz SQUARE-WAVE CARRIER AT INPUT B
В	MULTIPLIER OUTPUT WITH A 12-mV, 20-kHz SINE-WAVE CARRIER AT INPUT B
C	2-kHz SINE-WAVE-MODULATION SIGNAL AT INPUT A



TRACE	HORIZONTAL SCALE	DESCRIPTION
A	500 NSEC/DIV	MULTIPLIER OUTPUT WITH A 10-MHz SIGNAL AT INPUT B
В	500 NSEC/DIV	MULTIPLIER OUTPUT WITH A 25-MHz SIGNAL AT INPUT B
C	500 NSEC/DIV	MULTIPLIER OUTPUT WITH A 120-MHz SIGNAL AT INPUT B
D	5 NSEC/DIV	TRACE C WITH AN EXPANDED TIME SCALE

NOTE:

INPUT A IS A 600-kHz SINE-WAVE-MODULATION SIGNAL.

Example multiplier outputs include a double-sideband suppressed-carrier with a 20-kHz square-wave carrier at Input B (a) and outputs with input frequencies as large as 120 MHz (b).

picofarads. With the 1-k Ω load for the bridge and no bias network, the bridge output has a pronounced flat bottom around the origin. Fortunately, with the bias current of 1.08 mA in each 3.9-k Ω resistor, the Schottky diodes become forward-biased into partial conduction with 340 mV for each path, and the bridge yields an accurate and symmetric square-law output with a low source resistance.

You can use one such bridge with the differential amplifier as a fast squarer for frequency-doubling and square-law detection, for example. With slightly more current, you can make the load resistor as little as 50Ω .

The multiplier test pattern in Figure 2 results from a 5kHz sine wave on both Input A and the horizontal input and a 20-kHz square wave from a 100Ω source set at 0-, 6-, 12-, 18-, and 24-mV amplitude levels at Input B. Over this range of inputs, this multiple exposure shows that the analog multiplier exhibits linear behavior with errors of less than 1% of full scale. In Figure 3a, Trace A shows a double-sideband, suppressed-carrier output resulting from a -28 dBm, 20-kHz square-wave carrier, and Trace B results from a 20kHz sine-wave carrier. Trace C shows the 2-kHz modulation signal on Input A. Figure 3b shows double-sideband suppressed-carrier output signals at Input B frequencies of 10 MHz (Trace A), 25 MHz (Trace B), and 120 MHz (Trace C) using a 600-kHz sine-wave modulator at Input A. Trace D shows that same signal as Trace C but at 5 nsec/division, to show that the rise time of the multiplier in this breadboard version is just a few nanoseconds. (DI #2413)

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design**ideas**

5V logic pulser is battery-powered

W Stephen Woodward, University of North Carolina, Chapel Hill, NC

BATTERY-POWERED, PUSHBUTTONtriggered TTL/CMOS-compatible source of debounced 5V logic pulses is a simple but handy piece of test equipment to have in any tool kit (Figure 1). The circuit's battery-powered operation complicates what would otherwise be a trivial exercise in switch-bounce and timing-circuit design. The convenient use of battery power simultaneously imposes two requirements: near-zero quiescent-current draw and input-variation-tolerant voltage regulation. A nearzero quiescent-current draw minimizes the likelihood that you will encounter a dead battery when you need to use the logic pulser, and input-variation-tolerant voltage regulation accommodates the inevitable voltage droop as the battery ages and traverses its service-life curve from fresh to flat.

Of course, the unglamorous on/off switch is a traditional and serviceable way to fulfill the first requirement. Unfortunately, the effectiveness of an on/off switch depends directly, and regrettably, on whether you remember to use it. Neglecting proper and timely operation of on/off switches may result in battery damage. Thus, a key feature of the logic pulser in **Figure 1** is a satisfactory battery life without dependence upon a separate, manual on/off switch.

The trick to this design feature is the use of a single NO spst momentary-contact pushbutton switch to control both the trigger logic and the voltage regulator. In the quiescent state, S_1 is open, which leaves the ground-reference pin of the 78L05 regulator floating and causes the regulator's output voltage to saturate about 1V less than the input voltage from the battery. The circuit applies the resulting 7 to 8V to the V_{DD} pin of the 74C04 and, via R₅, to the debounce timeout circuit comprising R_{φ} , R_1 , and C_1 .

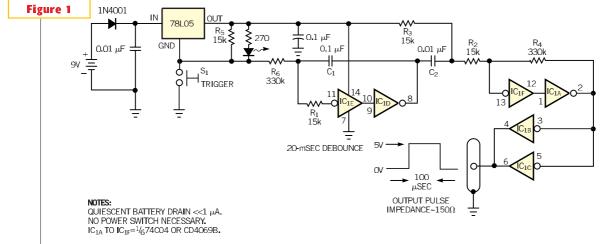
In this state, the 74C04 typically consumes less than 1 μ A and is the only power demand on the battery. The regulator is floating and consumes no power, despite its normally multimilliamp quiescent current. This low power implies a battery-life expectancy that is limited only by the self-discharge characteristics, or shelf life, of the battery. This expectancy is typically 10 years for alkaline and much longer for lithium. Meanwhile, the fact that the circuit applies V_{DD} to the output gates of IC1B and IC1C while the steady state of timing circuit R, R, R₄, and C₂ applies a logic 1 to the inputs of these gates ensures a solid low-impedance logic low at the pulser's output.

When you push the trigger button, the

sequence of events begins with the grounding of the regulator's reference pin and the consequent regulation—in-dependent of battery voltage—of the 74C04's V_{DD} to 5V. Simultaneously, grounding one end of R_6 starts the discharge of C_2 . The resulting approximate 20-msec delay provides adequate time for reliable debounce of the pushbutton, thus preventing the possibility of spurious multiple pulses in response to a single button press.

When $I\dot{C}_{1E}$'s input ramps to the approximate 2.5V CMOS logic threshold, the positive feedback around the IC_{1E} - IC_{1D} pair via C_1 causes the circuit to present a clean logic transition to the C_2/R_3 differentiator. The R, R, and C_2 network combines with the $I\dot{C}_{1F}$ - IC_{1A} regenerative pair to convert the resulting edge into a single, pristine, 100-usec pulse. The parallel IC_{1B} - IC_{1C} pair then inverts and buffers this pulse to the output. Following the pulse, the circuit output remains low until you release the pushbutton, which readies the trigger circuit for another cycle. (DI #2412)

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PC and DACs generate two simple analog outputs

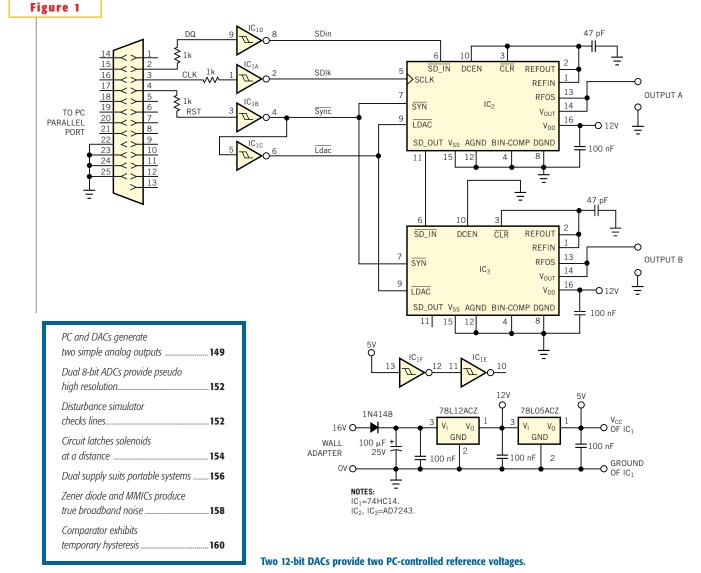
ideas

Jim Terrade, Clermont-Ferrand, France

The SIMPLE AND INEXPENSIVE circuit in **Figure 1** generates two PC-controlled analog reference voltages. You supply a wall-adapter supply and a

parallel connector, and the circuit is ready to run. The circuit uses two 12-bit AD7243 DACs, which require only one supply voltage. These converters also include internal references, minimizing the number of external components.

Simple software uses the parallel port to communicate with the converters. The



www.ednmag.com



two converters connect in series with a connection of their Sync and Ldac inputs. This arrangement makes it possible for only three wires to drive **F** the circuit.

The value of N can range from 0 to 4095 because the converters are 12 bits. The converters' internal reference voltages are fixed at 5V. To calculate the number N to enter, you can use the equation $N=V\times(4095/5)$, where V is the output voltage. For example, if $V_{\rm B}$ needs to be 4V and $V_{\rm A}$ needs to be 30 mV, Nb= $4.000\times(4095/5)=3276$ (\$CCC), and Na= $0.030\times(4095/5)=49$ (\$31).

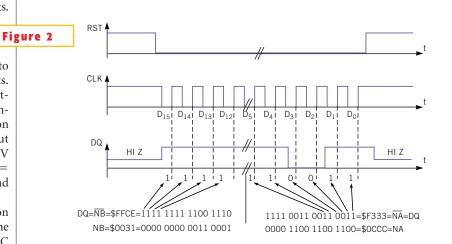
Figure 2 shows how the transmission occurs. DQ is the 2's complement of the real numbers, Nb and Na, that the PC sends to the converters. The PC sends inverted data because of the presence of the inverting 74HC14 trigger, IC₁. RST goes low first to enable the converters. CLK must also go low because the data input is active only on the positive edge of the clock signal; the converter reads data bits only when CLK goes from a low to high level. The transmission starts when the PC sends a 16-bit word-four zeros and then the 12-bit word-for the second converter, IC₂, MSB first. Next, the PC sends the 16-bit word for the first converter, IC2, MSB first. Niwm RST and CLK can go high, and the transmission stops.

If more than two converters are necessary, you connect the Sync and Ldac signals to the other converters and connect the $\overline{\text{SD}_{-}\text{IN}}$ input to the $\overline{\text{SD}_{-}\text{OUT}}$ output of IC₃. Make sure that the first word the PC sends is the one for the new converter.

Because the 74HC14 is an inverter, you have to consider the following relations—and follow all data-sheet instructions for the AD7243—before reading the C program that drives the converters:

- RST=Ldac=Sync=Sync
- $CLK = \overline{Sclk}$
- DQ=Sdin

Listing 1 shows the structure of the standard C program, which you can download from *EDN*'s Web site, www. ednmag.com. Click on "Search Databas-



Transmission begins after RST and CLK go low. Then, the PC sends the 16-bit words for Converter B and then for Converter A.

LISTING 1–STANDARD C PROGRAM Main loop : Read numbers to be sent : Na, Nb Set RST=1 Send data for Nb /* call sub-routine */ /* call sub-routine */ Send data for Na Reset RST=0 End Sub-routine (Send word N) : Set Numbit=15 MSB first /* Numbit is the rank of the actual bit */ /* 16 bits : 16 times */ do : CLK=0 If Numbit=1 then DQ=0 then DQ=1 If Numbit=0 wait CLK=1 (write 1 bit) wait Numbit=Numbit-1 while Numbit # 0 end of sub-routine

es" and then enter the Software Center to download the file for Design Idea #2407. (DI #2407)

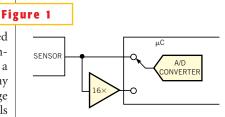


Dual 8-bit ADCs provide pseudo high resolution

Douglas Butler, Imetrix Inc, Cataumet, MA

ANY INEXPENSIVE μCs now come with several 8-bit A/D-converter channels. However, many high-dynamic-range sensors need more than 8 bits of resolution. The simple technique in **Figure 1** provides a pseudo-high-resolution result for any application that has a mixture of large low-resolution signals and small signals near zero.

For example, the turning-rate sensor of a robot autopilot operates in two realms: Either the robot is rapidly turning to a new heading, or it is trying to travel a straight line. When the robot is turning, the least significant bits (LSBs) are meaningless because they change too fast for the system to track them. When the robot is trying to travel a straight line, the LSBs are important, but the most significant bits (MSBs) are all zero.



For a sensor-output signal that is a mixture of large low-resolution signals and small signals near zero, you can use two ADC channels to achieve a pseudo-high-resolution result.

By using two 8-bit ADC channels for the same signal, the technique in **Figure** 1 can accommodate both conditions. One channel, which the controller uses for fast motion, reads the input directly and adds four 0 LSBs for a 12-bit result. The second channel reads the signal amplified by 16 with four 0 MSBs. The amplification gives this channel the resolution necessary for small-error signals while the robot is traveling a nearly straight line.

The controller first reads the second channel and checks for overflow. If no overflow occurs, the result is the reading plus four zeros for the MSB. If an overflow occurs, the controller discards this first reading and proceeds to read the first channel.

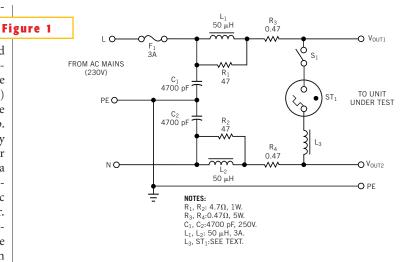
The controller can perform amplifieroffset correction any time the signal is in the small-signal realm by reading both channels, shifting 4 bits, and subtracting. In most cases, this correction is unnecessary. (DI #2415)

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Disturbance simulator checks lines

Peter Guettler, APS Software Engineering, Cologne, Germany

HE SIMPLE LINE-DISTURBANCE simulator in Figure 1 helps you check the immunity of linepowered devices to line disturbances and noise; you can build the device from leftover parts found in a junk drawer. The key elements are a ballast inductor (L_{2}) and a slightly modified glow-discharge starter (ST₁) from a fluorescent lamp. Starters for fluorescent lamps usually contain a glow-discharge tube together with a noise-suppression capacitor in a small housing. You must remove the capacitor for this application. Electronic starters are unsuitable for this simulator. Operation of the circuit is straightforward: When S₁ closes, the glow-discharge starter switches on and off at a random rate. The abrupt current variations



You can create dirty power lines for testing by using this simple circuit.



through L_3 induce noise at the output terminals, V_{OUT1} and V_{OUT2} . L_1, L_2, C_1, C_2 , and R_1 through R_4 form

 L_1, L_2, C_1, C_2 , and R_1 through R_4 form a decoupling filter to keep noise from flowing back into the ac mains. L_1 and L_2 must have a 3A current rating. You can wind them yourself, with 40 turns of 1mm-diameter magnet wire wound on a ferrite rod of 10-mm diameter and 50mm length. R_1 and R_2 are 47 Ω , 5W wirewound types. You mount all parts in a shielded enclosure. This simple circuit does not replace accurate, calibrated test equipment, but it provides a handy tool for a quick check during development. (DI #2423)

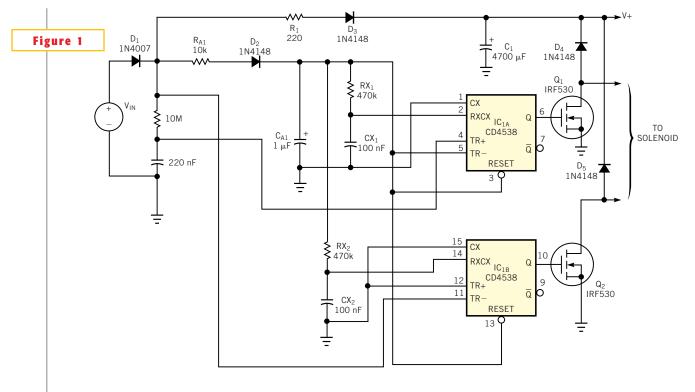
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Circuit latches solenoids at a distance

J Pelegri and D Ramirez, University of Valencia, Spain

HE CIRCUIT IN **Figure 1** controls lowcost, latching solenoid valves over long distances. For example, it can control one valve 1 km away using two wires and a 12V supply. The circuit provides 700 mA at 12V for the 20 msec necessary for latching a solenoid valve. The CD4538 monostable multivibrator provides an output-pulse width of 100 μsec to 1 sec. The IC consumes 5-nA standby current. The RX₁CX₁ and RX₂CX₂ network determines the output-pulse duration and accuracy. When the voltage on C_{A1} reaches 6V, an input trigger occurs, monostable IC_{1A} delivers an output pulse to Q_1 's gate, and Q_1 sinks the current needed to open the latching solenoid valve. When the voltage on C_{A1} drops be-

low 6V, monostable IC_{1B} turns on Q₂, and Q₂ sinks the current needed to close the latching solenoid valve. C_1 provides power to the solenoid valve. (DI #2426)



This circuit can drive a latching solenoid valve over a 1-km distance.

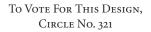


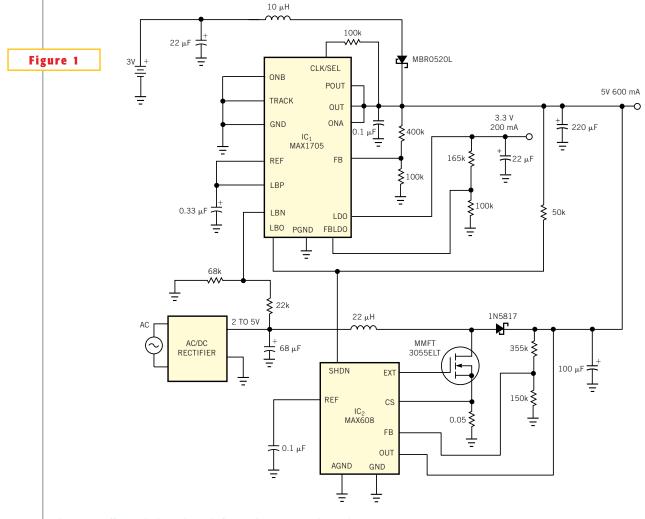
Dual supply suits portable systems

Budge Ing, Maxim Integrated Products, Sunnyvale, CA

THE PRIMARY CONCERN with power management in portable equipment is to prolong battery life by eliminating unnecessary energy consumption. The dual-output power supply in **Figure** I meets this objective and maintains regulated 5 and 3.3V outputs as long as the battery or ac-wall-cube voltage or both are present. The circuit draws battery power only when the ac source is absent. Switch-over between the battery and the wall cube requires no user intervention, and the circuit imposes no extra diodes or MOSFETs in the battery path. The switch-mode regulators deliver as much as 600 mA at 5V, and the linear regulator supplies as much as 200 mA at 3.3V. IC₁, which contains a switch-mode regulator and a linear regulator, has separate internal on/off controls that enable its linear regulator to remain on (powered by IC₂'s output) when its switch-mode regulator is off.

IC₂ is a switch-mode dc/dc converter that boosts the unregulated 2 to 5V wallcube output to a regulated 5.1V level. Note that the wall cube's output variation would produce excessive power dissipation in a linear regulator. IC₁'s POUT terminal, which can deliver 300 mA at 95% efficiency, provides a regulated 5V output. Thus, when IC₂ is producing 5.1V, IC₁'s feedback tells it to stop switching and wait. IC₁ goes into idle mode, drawing less than 1 μ A of quiescent current, and waits for its output to drop below the setpoint. Similarly, a comparator in IC₁ (LBN/LBO) tells IC₁ to shut down whenever the ac supply goes off. This shutdown prevents a flow of reverse current through IC₂. (DI #2427)





This energy-efficient dual supply works from either an ac supply or a battery.

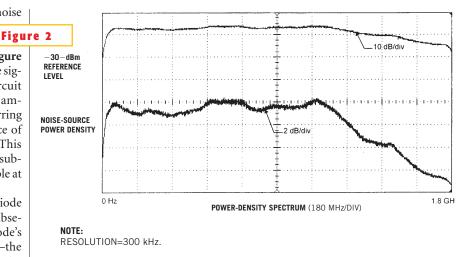


Zener diode and MMICs produce true broadband noise

Lukasz Sliwczynski, University of Mining and Metallurgy, Institute of Electronics, Krakow, Poland

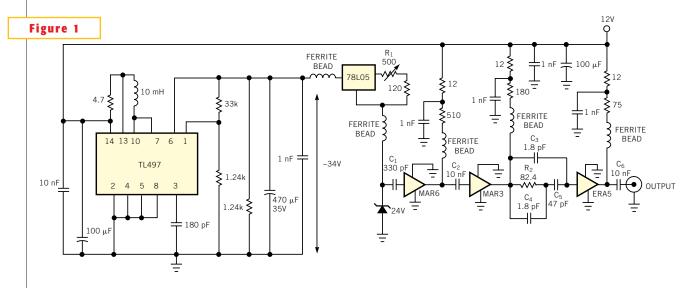
BROADBAND SOURCE OF white noise can be useful for measuring and testing communications equipment. The source in **Figure** 1 is simple and produces a large noise signal at its output terminals. The circuit comprises a zener diode and a few amplifying stages. The breakdown occurring in the zener diode is the true source of broadband noise in this design. This process is truly broadband because a substantial amount of noise is measurable at frequencies higher than 2 GHz.

The circuit ac-couples the zener diode into the first amplifier stage, and subsequent stages build up the zener diode's tiny noise voltage. The amplifiers—the MAR6, MAR3, and ERA5 (Mini-Circuits, www.minicircuits.com)—are monolithic-microwave ICs (MMICs). The total voltage gain of approximately 58 dB is high enough to produce an output voltage of approximately 224 mV rms at the 50 Ω terminating load, which is equivalent to approximately 0 dBm. Each amplifier in the chain has a compression point 1 dB higher than that of



A power-density spectrum of the noise source shows a flat spectrum with an accuracy of ± 1 dB from 20 MHz to 1 GHz.

the previous amplifier. Good amplifier linearity is important to ensure that the output signal has a Gaussian probabilitydensity function. The 1-dB compression point for the last amplifier in the chain is more than 18 dBm to ensure that the amplifier operates in the linear mode. From observations and measurements, it appears that the noise level of the avalanche-type breakdown diodes prevails over the noise based on the tunnel effect, and this noise level increases with the zener voltage of the diode. The frequency spectrum of the noise signal



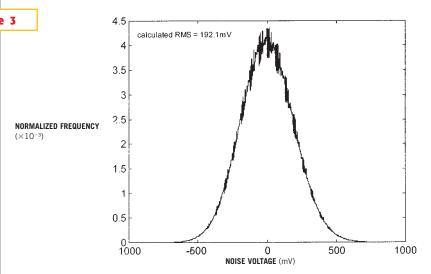
A 24V zener diode and a series of MMIC amplifiers create a broadband noise source.

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design**ideas**

is independent of the zener diode's voltage value, although a higher breakdown voltage typically means lower bandwidth. Using a zener diode with a 24V breakdown voltage for the circuit in **Figure 1** allows the design to produce a 10-dB-greater output signal than a design that uses a 9.1V zener diode.

A switching regulator, the TL497, and associated components provide the supply voltage for the zener diode; a 12V source supplies power for the rest of the circuitry. An additional linear regulator, the 78L05, supplies current to the zener diode. Changing the value of the current through the zener diode by trimming R, allows you to obtain a flat frequency spectrum from the source. You can increase the current to some value to find an optimum point for which the noise spectrum is flat and the noise level is as high as possible. For this design, the optimum current is approximately 21 mA. Increasing the current beyond this optimum point is not recommended because further increases cause a decrease of the output signal. Figure 2 is a plot of the noise-power-density spectrum, measured with a spectrum analyzer. In the frequency range of 20 MHz to approximately 1 GHz, the spectrum is flat with an accuracy of ± 1 dB, and the 3-dB bandwidth is approximately 10 MHz to 1.35 GHz. The probability-density function measured for 107 samples has the well-known Gaussian shape (Figure 3).



The probability-density function has a Gaussian shape, and the calculated rms value is 192.1 mV.

The calculated rms value from the histogram differs slightly from the powermeasurement value; this difference stems from the limited bandwidth of the sampling gate used to acquire the samples.

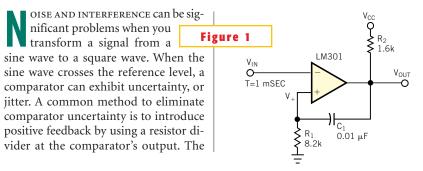
To achieve a flat power-density spectrum of the noise in the low-frequency region, some spectrum whitening is necessary because of the existence of 1/f-type noise. This circuit achieves the necessary frequency shape of the amplifier gain using properly chosen values of coupling capacitors between amplifier stages— C_1 , C_2 , and C_6 —and by using a correcting network before the last stage— C_3 , C_4 , C_5 , and R₂. The values of all frequency-shaping components were chosen experimentally while observing the power-density spectrum on the analyzer screen.

To obtain good performance from the circuit, you must obey all RF design rules. In particular, keep the pins of the zener diode as short as possible and locate all decoupling capacitors near the MMIC amplifiers. Screening the entire circuit is also recommended. (DI #2406)

> To Vote For This Design, Circle No. 322

Comparator exhibits temporary hysteresis

Victor Axenenko, CSRI, St Petersburg, Russia



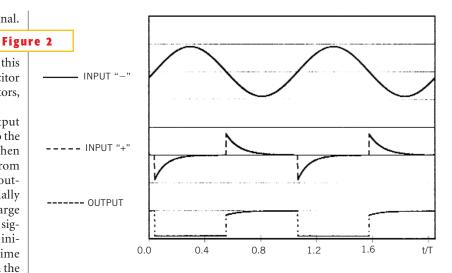
drawback of this method is that the resulting hysteresis produces an offset that's a function of the state of the comparator. With an asymmetric output, the offset of the comparator's input is also asymmetric. The result is asymmetry in

Replacing a resistor by a capacitor eliminates asymmetry by providing "temporary hysteresis."



the desired rectangular output signal. You can eliminate this drawback by creating a "temporaryhysteresis" characteristic. You create this characteristic by substituting a capacitor for one of the positive-feedback resistors, as in **Figure 1**.

When the comparator's output switches, the voltage step transfers to the noninverting input through C₁. When the comparator's output switches from a high level, V_{H} , to a low level, V_{I} , its output transistor saturates. C1, initially charged to V_H, begins to discharge through R₁. The noninverting-input signal, V₁, rises exponentially from its initial value $(V_H - V_L)$ to 0V with a time constant $T_1 = R_1 \cdot C_1$ (Figure 2). When the comparator's output switches from V₁ to V_{H} , its output transistor switches off. C_{L} charges through R₁ and R₂ and creates a voltage step $V_{+} = (V_{CC} - V_{L}) \cdot R_{1} / (R_{1} + R_{2})$ at the noninverting input. V₊ then decreases exponentially with the time constant $T_2 = (R_1 + R_2) \cdot C_1$. Note that the hysteresis is present only in the time intervals defining the time constants, T,



The feedback capacitor in Figure 1 provides a step voltage to the noninverting input each time the comparator switches.

and T_2 . Note also that upon termination of transients, the signal V₊ on the comparator's noninverting input in both cases is equal to 0V (if $T_1 < 0.1T$ and $T_2 < 0.1T$, where T is the input signal's period). For maximum symmetry, you should select $R_1 >> R_2$. (DI #2425)

Edited by Bill Travis and Anne Watson Swager

Controller IC halves switcher's standby power

Christophe Basso, On Semiconductor, Toulouse, France

The QUEST FOR LOW standby power is a challenge for switch-mode-powersupply (SMPS) designers. You can split the definition of "standby" into two facets. In "no-load" standby, such as in a fully charged battery, output-power demand is nonexistent. In "light-load" standby, such as in a TV set awaiting a remote-control command, internal circuitry has turned off most of the powerhungry blocks, but some μC activity still takes place. The design in **Figure 1** covers both standby facets with a simple solution. **Figure 1a** depicts the way you could achieve the regulation using a classic op-

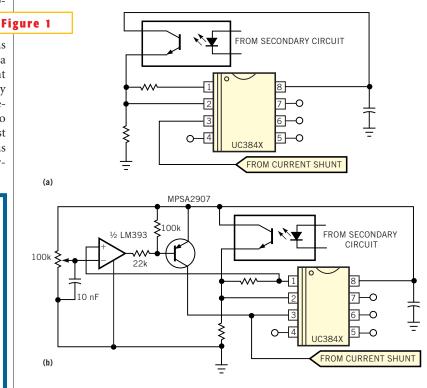
toisolated supply that uses a member of the UC384X family. When the output load decreases, the LED bias raises Pin 2 (the FB pin) and demands a lower peak current. At no load or light load, the PWM IC tries to reduce the duty cycle as much as possible. Unfortunately, high-frequency limitations lead to compromised performance at the lowest duty cycles, and the circuit can waste as much as 1.5W with a 30W SMPS operating at no load.

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One possible solution uses a hysteretic regulator but, as you can imagine, the high peak currents switched in the audible range make the design of a quiet, medium-power SMPS a difficult task. An elegant solution would combine the best of both worlds: normal high-frequency operation in current mode and burstmode operation when the output-power demand diminishes. **Figure 1b** shows how to apply the method to your UC384X-based design by simply adding a low-cost comparator. In nominal-pow-

ideas

er operation, the voltage on Pin 1 is higher than the level imposed by the 100-k Ω potentiometer's wiper, and the UC384X operates in its normal mode. When the load disappears, the voltage on Pin 1 drops to reduce the primary peak-current setpoint. If you adjust the potentiometer for a given peak level, the only way to further reduce the power is to stop the output pulses. The comparator, deriving its power from the UC384X's internal reference, biases the pnp transistor and brings the current-sense pin to the



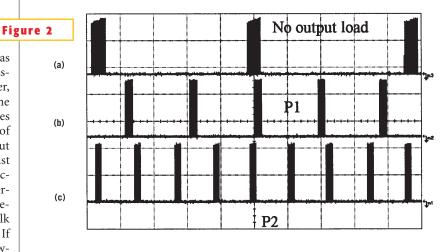
The classic arrangement in (a) reduces no-load standby power; the addition of a comparator (b) cuts the standby power by 50%.

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level at Pin 8. This action blocks the output pulses, and the circuit delivers no power.

The output voltage decreases, and, as soon as the error amplifier's level crosses the level at the potentiometer's wiper, the pulses reappear for another time packet. In other words, the circuit goes into burst mode. Thanks to the lack of hysteresis in the comparator, the output ripple is minimal. However, you must prevent the UC384X from entering hiccup mode during the burst-mode operation to preserve good transient response. Increasing the power-rail bulk capacitor can prevent hiccup mode. If the circuit enters hiccup mode, the power consumption further decreases but to the detriment of the transient response. Figure 2 shows how the circuit behaves at different load conditions. By adjusting the level at the comparator's inverting input, you have the flexibility to make the supply enter burst mode at a peak value at which no acoustic noise results. You can also select the output level at which



Burst-mode pulses reflect a no-load condition (a) and different light-load conditions (b and c).

the circuit enters burst mode: a no- or light-load condition. With a typical 12V, 30W flyback supply using a UC3843, measurements reveal an input power of 1.35W at no load (V_{IN} =100V ac; $R_{STARTUP}$ =100 k Ω). Adding the compara-

tor reduces the input power to 770 mW. (DI #2436)

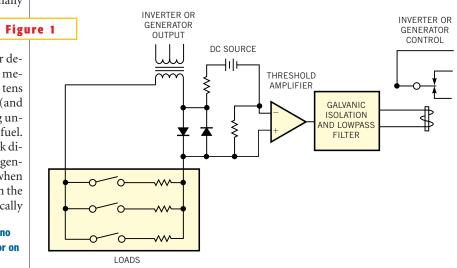
To Vote For This Design, Circle No. 494

Load detector controls power sources

Giovanni Romeo, Instituto Nazionale de Geofisica, Rome, Italy

MERGENCY GENERATORS normally operate when the main power source fails. Inverters run continuously (and expensively) even when no load-power demand exists. Even unloaded, a medium-sized inverter consumes some tens of watts just to keep its fan running (and to make noise). A generator running under no-load conditions just wastes fuel. The simple scheme in **Figure 1**'s block diagram controls your power source (generator or inverter), switching it off when no load exists and turning it on when the load needs power. The device is basically

Why waste generator power when there's no load? This simple circuit turns the generator on only when a load demands power.

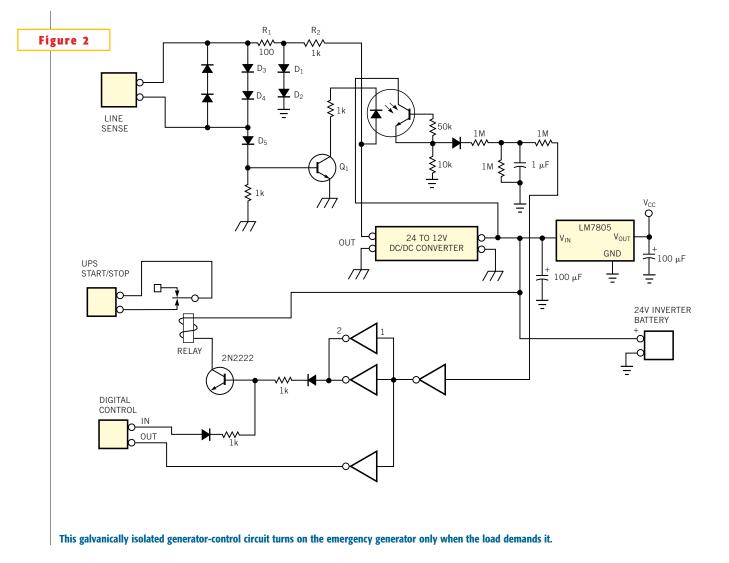




an ohmmeter that monitors the generator resistance of the generator or inverter output. Usually, the output comes from a motor coil or a transformer winding having low resistance. The circuit in **Figure 1** can detect any load whose resistance is lower than 15 k Ω . When no load exists, the voltage at the amplifier input (the generator's voltage minus the diode-junction voltage) does not exceed the threshold, so the relay does not engage.

When one or more loads connect to the circuit, the voltage at the amplifier input exceeds the threshold, actuating the relay and starting the generator or inverter. When the ac load current flows through the circuit, it keeps the relay engaged. When the load disconnects, the relay disengages. In operating a generator, you should wire the system to start the generator when no line power exists *and* when the load requires power. **Figure 2** shows a complete schematic. In the no-load case, the voltage source (R_1 , R_2 , D_1 , and D_2) cannot forward-bias Q_1 's base-emitter junction, because of the voltage drop across D_3 , D_4 , and D_5 . The junction becomes forward-biased when a load connects to the inverter, and the load cur-

rent flows through the output coil (inverter or generator transformer). The high-voltage section of the circuit is galvanically isolated via the dc/dc converter and the optocoupler. An RC lowpass filter delays the relay's actuation; it takes approximately 1 sec for the relay to engage after connecting the load and 2 sec to disengage after disconnecting the load. (DI #2435)



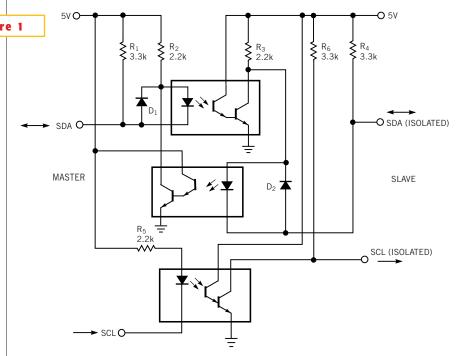


Two-wire interface has galvanic isolation

Minh-Tam Nguyen and Martin Baumbach, Maxim Integrated Products, Munich, Germany

NLIKE THE FOUR-WIRE SPI, QSPI, and Microwire data-in-**Figure 1** terface standards, I²C and SBBus buses require only two wires for data transmission, because they send and receive over the same wire. The circuit in Figure 1 provides galvanic isolation for the two-wire interface. A small transformer and a MAX253 transformer driver (not shown) derive an isolated 5V rail from the master-side 5V rail. The data rate and isolation-barrier voltage in your application guide the selection of the transformer and optocoupler. The circuit in Figure 1 uses a Hewlett-Packard 6N138 optocoupler. For more information on component suppliers, see the MAX253 and MAX845 data sheets. The scheme assumes a μP or μC for the master device, and the currentsink limitation of the processor's SDA terminal dictates that the optocoupler's minimum on-state current be less than 3 mA. Even so, the optocoupler's 300% current-transfer ratio (CTR) is adequate to ensure proper operation in this circuit.

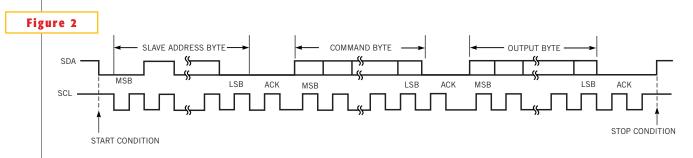
The slave side should host an I²Ccompatible device, such as the MAX517 8-bit DAC or the MAX127 data-acquisition system. The master-side SDA and SCL signals are high when the bus is not in use. The I²C Start condition is typically a high-to-low transition on SDA while SCL remains low (**Figure 2**). With SDA low, current through R_2 and the optocoupler's input causes the opto output to produce a signal of approximately 0.4V



A handful of components provides an isolation barrier for the two wires of an I²C transmission interface.

(sum of the opto output and the forwardbiased Schottky diode, D₂). Pull-up resistors R₁, R₄, and R₆ are necessary for I²C compatibility. After the master addresses the slave as described, the addressed slave responds with a low-level acknowledge bit. The bidirectional SDA line allows data transfer in both directions, but the unidirectional SCL line needs only to conduct signals from master to slave. Data transmission ends with the Stop condition, in which SDA typically makes a low-to-high transition while SCL is high. (DI #2438)

> To Vote For This Design, Circle No. 496



This diagram shows the I²C timing protocol for the MAX517 D/A converter.

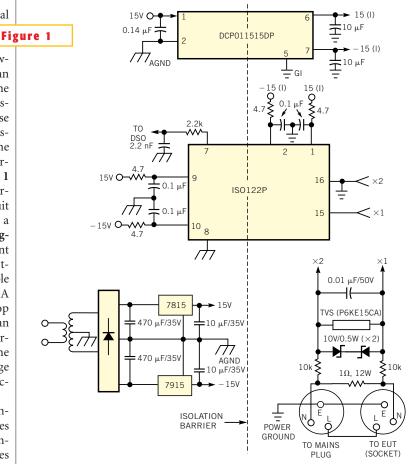


Measure power-on current transients on ac line

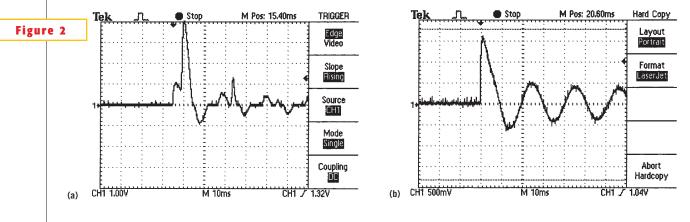
N Kannan, Mediatronix, Trivandrum, India

OR ANY ELECTRONIC OR electrical system, you usually determine the ac-line fuse rating based on the steady-state current. However, the power-on current surge is an important parameter in determining the fuse's I²t rating. The I²t rating is a measure of the energy required to blow a fuse in pulsed conditions. Also, in many cases, you may find it of value to know the shape of the current surge and its harmonic content. The circuit in Figure 1 can help you capture the power-on current transients in a system. The circuit costs less than \$25 to build. You need a DSO to capture the waveforms. In Figure 1, the neutral line of the equipment under test contains a 1Ω , 12W currentsense resistor. The resistor should be able to handle10A surge current and 3A steady-state current. The voltage drop across the sense resistor drives an ISO122P isolation amplifier (Burr-Brown, www.burr-brown.com). The zener diode and the transient-voltage suppressor provide overvoltage protection.

A DCP011515DP isolated dc/dc converter (also Burr-Brown) generates $\pm 15V$ isolated supplies to power the input side of the ISO122P. Both devices provide more than a 1000V rms isolation capability. A local supply powers the in-







A highly capacitive power supply causes a 4A current surge (a) in the power line; an incandescent bulb produces a 1.5A spike (b).



put of the dc/dc converter and the output side of the ISO122P. The filtered output of the ISO122P provides the input to a DSO. You use transient-capture mode in the DSO to capture the power-on current surge. **Figure 2** shows the waveforms for:

- A system with a 10,000-µF transformer/bridge-capacitor filter (Figure 2a). Steady-state rms current is approximately 0.13A at 220V rms.
- An incandescent lamp (Figure 2b). From the waveforms, you can determine the surge's shape, width, and peak value. You can then use this information to determine the proper I²t rating for the system fuse. Figure 2a shows a current surge of 4A peak, although the steady-state current is only 0.13A. The heavy surge arises because of the large-value capacitor filter and also from

core-saturation effects. **Figure 2b** shows a turn-on surge of approximately 1.5A for the 60W, 220V incandescent bulb. Warning: Hazardous voltages are present in the mains-side circuitry. (DI #2428).

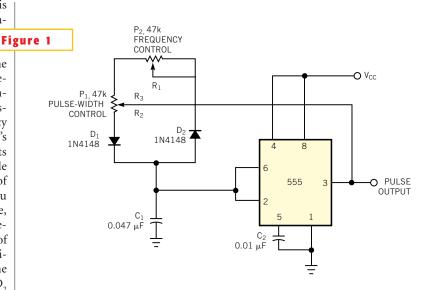
To Vote For This Design, Circle No. 497

Generator has independent pulse width, frequency

Darvinder Oberoi, CEDTI, Jammy, India

COMMON CIRCUIT in electronics is the square-wave, astable multivibrator (one-shot), which is useful for various purposes, such as timing circuits and audible alarms. The most common way to generate the desired square wave is to use the inexpensive 555 timer. The need sometimes arises for a square wave with fixed frequency but variable pulse width or vice versa. It's difficult to satisfy these requirements with a conventional 555-based astable circuit. Figure 1 shows a modification of the basic 555-based astable circuit. You can use the circuit to generate stable, variable-pulse-width or variable-frequency signals, which are independent of each other by means of individual dedicated controls. The Pin 3 output of the 555 charges and discharges C₁. D₁ and D₂ provide individual paths for the charging and discharging operations, respectively. The two timing potentiometers, P, and P₂, control the RC₁ time constant during the charging and discharging cycles.

When Pin 3 of the 555 is high, the capacitor charges through R_2 (a component of P_1 , whose value depends on the wiper position). When C_1 charges to two-thirds V_{CC} , Pin 3 goes low, and C_1 discharges through the combination of D_2 , P_2 (resistance R_1), and P_1 (resistance R_3). When



You can independently and noninteractively control pulse width and frequency by adjusting two potentiometers.

the voltage across C_1 reaches one-third V_{CC} , the Pin 3 output again switches high. The process of alternately charging and discharging C_1 continues; the result is an output with a desired pulse width and frequency. Because the forward resistance of the diodes is negligible, the pulse width equates to $R_2C_1\log(2)$. The pulse period (reciprocal of frequency) is $0.693(R_1 + R_2 + R_3)C_1$. Thus, the pulse width is independent of P₂'s wiper position, and the frequency is independent of P₁'s wiper position. (DI #2444)



Customized potentiometers aid amplifier design

Chuck Wojslaw, Xicor Inc, Milpitas, CA

HE CIRCUIT IN **Figure 1** is a model of an amplifier circuit whose cutoff frequency and gain are functions of the values of variable resistors. A first-order, RC lowpass filter establishes the cutoff frequency, and a traditional noninverting op-amp circuit determines the gain. You can add variability and programmability if you use digitally controlled potentiometers to implement the variable resistors. The circuit in Figure 2 shows the implementation of the frequency and gain controls. The potentiometer, R, forms a pseudo-tee network; along with capacitor C, the potentiometer establishes the upper cutoff frequency f_c . Potentiometer R_2 is

Trequency I_c . Potentiometer R_2 is a three-terminal device that establishes the voltage gain, G_0 . The voltage gain for the circuit is:

$$\frac{V_0}{V_S} = \frac{G_0 \omega_C}{j\omega + \omega_C}.$$

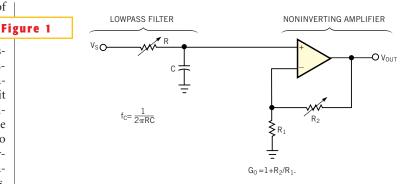
G₀ is the programmable closed-loop passband gain:

$$G_0 = \frac{R_1 + R_2}{R_1 + k_2 R_2}$$
, and $0 \le k_2 \le 1$,

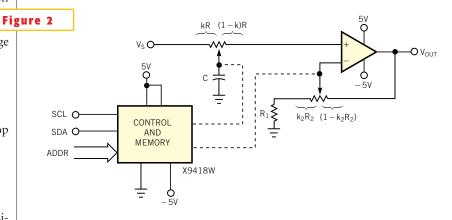
where k_2 reflects the proportionate position of the wiper from one end of the potentiometer (0) to the other end (1). The gain is programmable from 1 to $(R_1+R_2)/R_1$. The fixed resistor, R_1 , limits the circuit's maximum voltage gain, a limitation usually necessary for accuracy and bandwidth purposes. The upper cutoff frequency f_C is a function of the input RC network:

$$f_{\rm C} = \frac{\omega_{\rm C}}{2\pi} = \frac{1}{2\pi(k_1 R)C}$$
, and $0 \le k_1 \le 1$.

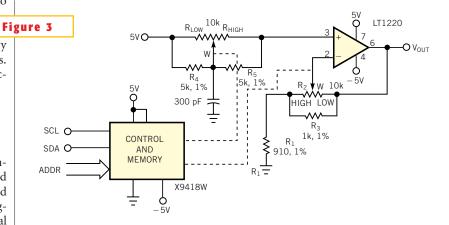
where k_{12} like k_{22} reflects the proportionate position of the wiper from one end of the potentiometer (0) to the other end (1). The dual versions of the XDCP digital potentiometers use the same serial bus with different addresses for the individual potentiometers.











You can use the same serial bus to control both the gain and the cutoff-frequency potentiometers in an amplifier circuit.



For high-frequency amplifiers, the 10k Ω end-to-end resistance of the X9418 creates time constants limiting the bandwidth of the circuit. You can reduce the effective end-to-end resistance of the potentiometers by using two techniques shown in the high-frequency amplifier circuit in **Figure 3**. If you connect the wiper of the potentiometer to a high impedance, shunting R_{TOTAL} directly with an external resistor reduces the effective end-to-end resistance. Resistor R_3 changes the effective end-to-end resistance of potentiometer R_2 from 10 to 0.909 k Ω . If you do not connect the wiper of the potentiometer to a high impedance, you can reduce the effective end-to-end resistance by adding external, equal-value resistors, R_4 and R_5 , from the wiper to the high and low terminals. This technique, however, creates a potentiometer whose taper is pseudolinear and whose end-to-end resistance varies with

wiper position by approximately 20%. The gain of the amplifier circuit in **Figure 3** is programmable from 1 to 2, and the cutoff frequency is programmable from 130 kHz to more than 1 MHz. (DI #2437)

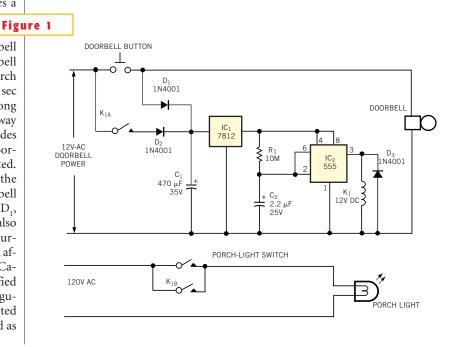
To Vote For This Design, Circle No. 499

Ring your bell; light your light

Dennis Eichenberg, Parma Heights, OH

HE CIRCUIT IN Figure 1 provides a simple and inexpensive way to provide illumination for a dark doorway. Pressing the doorbell button momentarily rings the doorbell and turns on the porch light. The porch light remains on for approximately 25 sec and then turns off. This interval is long enough for a person to find his or her way when it's dark. The system also provides security in that anyone pressing the doorbell button is automatically illuminated. The circuit receives its power from the doorbell system. Pressing the doorbell button provides voltage to diode D₁, which acts as a half-wave rectifier. D, also acts as a blocking diode to prevent current from flowing back to the doorbell after you release the doorbell button. Capacitor C₁ filters the half-wave-rectified voltage, and voltage regulator IC, regulates the filtered voltage. The regulated voltage supplies timer IC₂, configured as a monostable multivibrator.

Relay K_1 activates when you press the doorbell button. It remains activated until IC₂ times out, according to the expression t=1·1R₁C₂. Diode D₃ is a flyback diode to protect IC₂ from the inductive spike K₁ generates when it becomes deactivated. Normally open relay contact K_{1A} continues to power the circuit via



Scared of the dark? Use this circuit to turn on your porch light when you ring the doorbell.

diode D_2 after you release the doorbell button. K_{1B} connects in parallel with the porch-light switch to power the porch light by means of the new circuit. You must size the relay contacts to accommodate the current requirements of the porch light. (DI #2433)

To Vote For This Design, Circle No. 500

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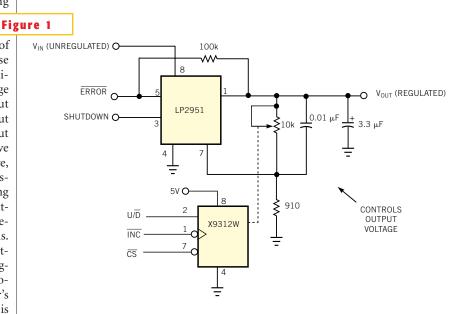
Edited by Bill Travis and Anne Watson Swager

Voltage regulator goes digital

Chuck Wojslaw, Xicor Inc, Milpitas, CA

OWER CONSUMPTION AND failing batteries are key issues in battery-operated applications. Features in the new generation of series voltage regulators address these concerns. For example, National Semiconductor's LP2951 micropower voltage regulator provides a logic-level output signal indicating a low regulated output voltage; the IC also has a logic-level input to shut down the regulator to conserve power. These signals are digital; therefore, they are compatible with µP-based systems. But what about the programming or controlling the regulator's output voltage? A mechanical potentiometer or selected resistors are not elegant solutions. You can complete the so-called computerization or digitizing of the voltage regulator by using a digitally controlled potentiometer to program the regulator's output voltage. The circuit in Figure 1 is a wide-range, computer-controlled voltage regulator with a nominal output voltage that varies from 1.235 to 14.8V. The regulator uses a Xicor XDCP X9312W digitally controlled potentiometer that,

Voltage regulator goes digital	. 167
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Resistor implements half-duplex RS-232 with echo	172
Circuit monitors ac-power loss	172
RF transmitter uses AMI encoding	174
High-voltage regulator is 100% surface-mountable	178



A digital potentiometer adds programmability to an ordinary series voltage regulator.

with its 100 steps, can program the regulator with a resolution of 0.136V per step. The output voltage is $1.235V(1 + kR/910\Omega)$, where k is a number from 0 to 1 and reflects the proportionate position of the wiper from one end of the pot (0) to the other end (1). R is the end-to-end resistance of the potentiometer.

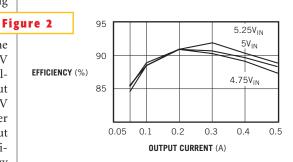
The XDCP's programming uses a three-wire bus. The potentiometer is configured as a two-terminal variable resistor. The regulator's Error output signal warns of a low output voltage; you can use it as a power-on reset. The logic-compatible Shutdown input signal allows you to switch the regulator on and off to conserve power. These signals, along with those you require to program the XDCP, typically connect to the I/O port or the μ P or μ C. The potentiometer adds variability to the regulator circuit; its digital controls, which are attached to a computer-controlled bus, provide programmability. For example, an automated closed-loop calibration procedure to program the regulator saves manufacturing test time. You can use the circuit as a bias supply; a voltage reference; or a programmable, high-output-current voltage source in test-and-measurement applications. (DI #2442).



Supply converts 5V to -48V

Kurk Mathews, Linear Technology Corp, Milpitas, CA

S THE DEMAND for networking equipment grows, the need arises for a -48V supply that can power telecommunication lines. The circuit in Figure 1 delivers 24W at -48V from a 5V input. One of the biggest challenges in this design is choosing the input voltage. Although high-current, 5V sources are commonly available, lower input voltages generally mean high input currents with accompanying low efficiency. With a relatively simple topology and a 5V input source, the circuit in Figure 1 delivers greater than 85% efficiency (**Figure 2**). T₁ stores energy during the on-state time of Q₁. Energy transfers to two stacked 24V outputs to create -48V. C₁ charges to a dc value equal to the 24V



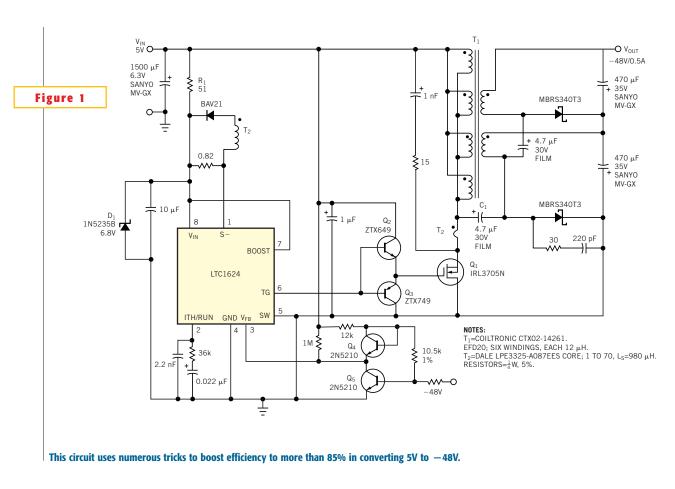
The circuit in Figure 1 delivers greater than 85% efficiency under all conditions and greater than 90% for much of its output-current range.

input voltage while clamping T₁'s leakage-inductance spike and providing a path for input current during Q₁'s off-state time. This operation results in continuous input current and thus reduces capacitor ripple-current requirements

The reduced input ripple current, which is characteristic of this topology, demands sensing of the switch current rather than the input current. In this case, T_2 senses the switch current, eliminating 400 mW of resistor loss without using excessive board

space (7×8 mm). Other additions im-

prove the circuit's efficiency and per-





formance. The LTC1624's Boost pin normally provides the internal output driver (the TG pin) with a 5.6V regulated supply, but TG produces only 4.2V with a 5V input. Bypassing the internal regulator by connecting the Boost and V_{IN} pins increases Q_1 's gate voltage, resulting in a gain of more than 3.2% in overall efficiency. R_1 and D_1 keep the Boost pin below its 7.8V rating in the event of an input overvoltage condition. The addition of Q_2 and Q_3 provides an additional 5.5% of efficiency by speeding transitions and increasing gate voltage from 5 to 5.3V. This voltage peaking results from excess emitter current as Q_2 turns off after charging Q_1 's gate capacitance. Q_4 and Q_5 translate the -48V output to the 1.2V that the feedback pin (V_{FB}) requires to regulate the output voltage. The LTC1624's switching frequency decreases with output voltage, thereby reducing input current during output short-circuit conditions. (DI #2440).

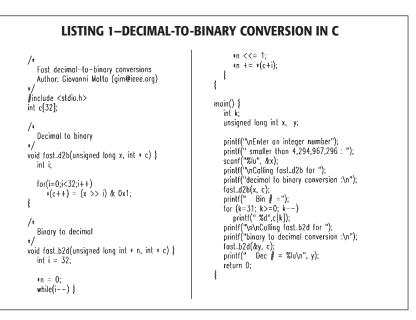
To Vote For This Design, Circle No. 451

C routine speeds decimal-to-binary conversion

Giovanni Motta, Brandeis University, Waltham, MA

PREVIOUS DESIGN IDEA ("Program provides integer-to-binary conversion," *EDN*, March 2, 1998, pg 110) describes a C/C++ function that provides integer-to-binary conversion. The function, named cintbin/classicC, implements a conversion in a straightforward way that defines decimal and binary numbers in terms of powers. Although this function can be useful for testing or educational purposes, its low efficiency precludes its use in embedded or other fast applications. The main source of inefficiency is the use of the pow C function, which requires linking the math library. By carefully rewriting the function and by directly accessing the binary representation of the integers in C, you can speed the conversion by as much as 58 times. The rewrite also results in more compact code, because linking the math library is unnecessary. Listing 1 shows a simple calling program and two functions, fast d2b and fast b2d, that implement conversion between decimal and binary integer representations.

In fast_d2b, the main loop is a for loop, in which the variable, i, accesses the array, c, sequentially, from 0 to 31. At each iteration, x, the number to convert, rightshifts by i positions (the >> operator), and the routine extracts its least significant bit by masking x with the constant 1 (the & operator). The routine finally assigns the result to the ith term of the vector c. The symmetric fast_b2d function converts a binary number to its decimal



equivalent. The function performs the conversion through a sequence of left shifts and sums. To compare the performance of fast d2b with

the function classicC, we ran several tests on two platforms, both running Unixlike OSs. We used the GNU C compiler (gcc) with and without turning on "aggressive optimization" (the O3 flag). **Table 1** shows the time to convert the first 100 million integers. The Unix time command produces the running-time figure. Fast_d2b is 20 to 58 times faster

TABLE 1-	SECONDS TO	CONVERT 100	MILLION IN	TEGERS
	Irix (SGI Indy R5000)		Linux (PIII/500)	
	gcc	gcc-03	gcc	gcc-03
fast_d2b	476	160	80	28
classicC	9377	8542	2206	1672

than classicC. You can download **Listing** 1 from *EDN*'s Web site. At the registereduser area, go into the Software Center and download the file from DI-SIG #2444. (DI #2443).

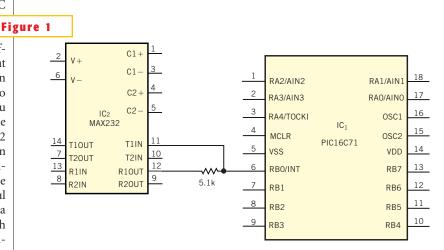


Resistor implements half-duplex RS-232 with echo

Matt Bennett, Austin, TX

PREVIOUS DESIGN IDEA ("Single µC pin makes half-duplex RS-**2**32," *EDN*, Aug 5, 1999, pg 118) presented a way to implement halfduplex RS-232 communications without echo. Sometimes, an echo is desirable in a µC application. You can obtain the echo by using a single resistor (Figure 1). You insert a 5.1-k Ω resistor between the transmit and receive pins on the RS-232 driver (such as a MAX232). The I/O pin on the μ C (RB0 on 14-bit PIC μ Cs) connects directly to the transmit gate on the RS-232 driver. This technique is useful for implementing a user interface on a Microchip PIC for applications in which you communicate to the PIC via a terminal or a terminal-emulation program. Full duplex is unnecessary with a user interface based on user-issued commands and μC responses, when the μC generates no spontaneous data that would mask the user-issued commands. The character echo is useful in determining whether the device is powered up and the RS-232 receiver is active, but an echo alone does not tell you whether the µC is active; the µC must send data.

When the μC is in receive mode, it makes the input pin a high-impedance



The addition of a single resistor provides an echo in RS-232 half-duplex communications.

input. All RS-232 data sent to the μ C is immediately retransmitted via the resistor that connects the receiver to the transmitter. Because the input has high impedance, the μ C is essentially just monitoring the traffic on the RS-232 line. When the μ C must send serial information, the μ C converts its I/O pin to a lowimpedance driver. Anything now sent to the μ C shunts to ground or V_{CC} (depending on the μ C's output state) through the resistor and the μ C's driver. The μ C ignores data sent to it. The μ C now directly sends data down the serial line. The μ C must immediately change the serial line back to high-impedance mode after transmitting or risk data loss. (DI #2445).

> To Vote For This Design, Circle No. 453

Circuit monitors ac-power loss

Dennis Eichenberg, Parma Heights, OH

THE CIRCUIT IN Figure 1 provides a simple, nonvolatile means of monitoring critical ac-power failures. Monitoring the power is important in such systems as heating and refrigeration, in which damage can occur if the ac power goes down for an extended period. The circuit in Figure 1 requires little power from the ac-power system. The quiescent battery current of approximately 5 μ A

provides long battery life in this application. The optocoupler consists of a neon lamp and a photocell. When the ac-power system is active, the neon lamp lights via current-limiting resistor R_1 . A neon lamp is ideal for this application because of its low power drain. The resistance of the photocell in the optocoupler is low when the cell is illuminated and high when it's unilluminated. R_2 serves as a current-limiting resistor for the photocell.

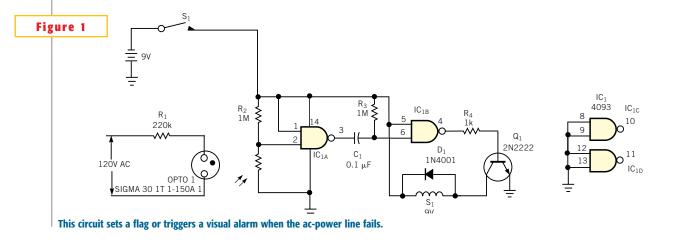
 IC_{1A} of the quad two-input NANDgate Schmitt trigger serves as a buffer for the optocoupler. The output of IC_{1A} is normally high when the ac power is present and goes low when a power failure occurs. IC_{1B} is configured as a negativeedge-triggered, half-monostable multivibrator. It produces a positive pulse with



a width of approximately $0.8R_3C_1$, or approximately 0.8 sec, whenever the ac power goes down. The output pulse drives transistor Q_1 via the current-limiting resistor, R_4 , to activate solenoid S_1 .

 D_1 is a flyback diode to protect Q_1 from the inductive spike S_1 generates when it becomes deactivated. You can use S_1 to trigger a flag or to provide a similar visual alarm. The flag remains in position until you manually reset it to prepare the circuit for the next power failure. (DI #2446).

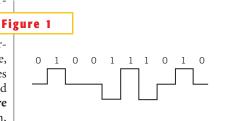
To Vote For This Design, Circle No. 454



RF transmitter uses AMI encoding

Paul Sofianos, Motorola, Tempe, AZ

LTHOUGH ALTERNATE-MARK-inversion (AMI) encoding is wellsuited for direct-conversion FM transmission, designers often overlook the technique. AMI, a three-phase, synchronous-encoding technique, uses bipolar pulses to represent logic ones and no signal to represent logic zeros (Figure 1). Direct-conversion FM transmission, in which data directly modulates a carrier, is also known as frequency-shift-keying (FSK) modulation. For higher frequency transmissions, a PLL usually synthesizes the carrier from a crystal reference. This type of RF transmission requires the dc voltage of the modulating signal to be 0V; otherwise, the PLL tends to "track out" the transmitted data. FSK transmission usually uses the familiar Manchester-encoding method. However,



AMI encoding uses a pulse of either polarity to denote a logic one and a 0V level to denote a logic zero.

Manchester encoding requires twice the bandwidth of AMI encoding and usually requires the addition of preamble and postamble bits to allow the receiver to determine the center of the data bit for decoding. AMI suffers from none of these disadvantages; however, it has a drawback: A long string of zeros produces no transitions in the data stream. To address this drawback, high-density bipolar 3 (HDB3) encoding is available.

The circuit in **Figure 2** shows a 16channel, AMI-encoded RF transmitter for data rates as high as 28.8 kbps. The circuit operates in the unlicensed (FCC Part 15) 902- to 928-MHz industrial, scientific, and medical (ISM) band and is reliable for open-field distances as long as 1000 ft. You can easily modify it to sustain higher or lower data rates. IC₁, IC₂, R₁, and R₂ perform the AMI encoding. IC_{1A}, a simple D flip-flop, controls the high-impedance state on Pin 13 of IC₂. IC_{1B} alternates the data presented to IC₂ whenever the previous data is a logic one. This data has a slight delay to avoid



glitches in the output waveform. R_1 and R_2 set the high-impedance voltage to $1/2V_{CC}$. R_2 adjusts the peak deviation of the transmitted RF signal from IC₃, nominally set at 50 kHz. C_1 and R_2 constitute a lowpass filter with corner frequency set to attenuate the data at frequencies above the third harmonic.

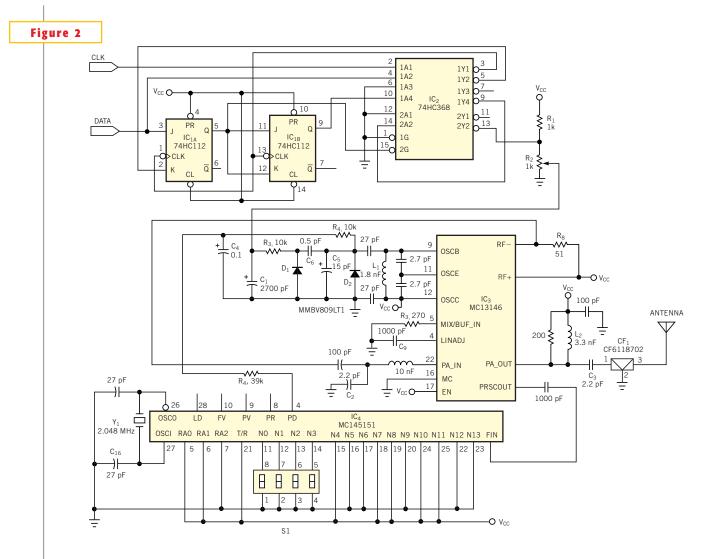
 IC_3 is a low-power, integrated RF transmitter (Motorola, www.motorola. com) targeting ISM applications. Its voltage-controlled oscillator is a parallel-resonant Colpitts type. The varactor diode, D_1 , controls the modulation, and D_2 sets the center frequency. The modulation, D_1 , is set to approximately 60 kHz/V, and the frequency adjustment, D_2 , is set to 7

MHz/V. The mixer of the IC serves as a buffer; you can adjust R_3 for desired output power. C_2/L_1 and C_3/L_2 conjugately match the source-to-load impedances. These values can vary, depending on the parasitics of your layout. CF_1 (TDK Corp, www.tdk.com) provides final filtering of the output before transmission. IC₄ synthesizes the desired carrier frequency. The IC internally divides by 512 the frequency that crystal Y_1 establishes. With Pin 16 of IC₃ tied low, the synthesized frequency is $f_{OUT}=(2.048 \text{ MHz}/512)\cdot65\cdot\text{N}$, where N represents the digital value present on the N bus of IC₄.

As illustrated, N can vary from 3472 to 3487, yielding 16 discrete output chan-

nels from 902.72 to 906.62 MHz in 260kHz steps. R_4 and C_4 form a lowpass filter with corner frequency set to a value substantially lower than the internal reference frequency of the synthesizer or the data stream, whichever is lower. As with any RF design, you should give careful consideration to parts placement and shielding. You should also apply generous decoupling. If desired, you can hold Pin 17 of IC₃ at logic zero for low-power-disabled operation. (DI #2429).

> To Vote For This Design, Circle No. 455



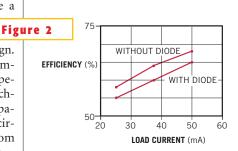
AMI provides an attractive alternative to Manchester encoding for direct-conversion FM transmission.



High-voltage regulator is 100%-surface-mountable

Tom Gross, Linear Technology Corp, Milpitas, CA

T CAN BE DIFFICULT to generate a high-voltage supply from a medium-voltage input, especially if you need a surface-mount design. It is difficult to find surface-mount components with the necessary specs, especially the transformer and power switches. High-voltage surface-mount capacitors can also be hard to locate. The circuit in Figure 1 generates 100V from 25V. The circuit is a typical flyback regulator that uses a couple of well-established circuit techniques to handle the high voltage. The first technique is to insert an n-channel MOSFET (Si4480) in series with IC₁'s internal power transistor. The cascoded FET stands off the large switch voltage that arises when the switch turns off. The large switch voltage represents the input voltage summed with the reflected output voltage of the transformer's primary. Using the cascode FET not only increases the effective switchvoltage capability, but also eliminates the

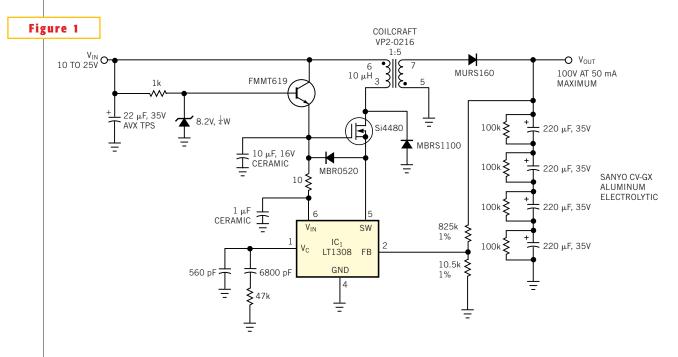


Bootstrapping the IC switch voltage to the input in the circuit of Figure 1 improves efficiency by about 3%.

need for a snubber circuit across the primary of the transformer.

Of course, the FET actively turns on when the source goes low. But simply using the input voltage to supply the gate voltage doesn't work, because the maximum input voltage (25V) exceeds the maximum $\pm 20V$ limit of the MOSFET's gate-to-source voltage. Therefore, the cir-

cuit uses an emitter follower to supply a constant voltage to the gate of the MOS-FET. A 1-k Ω resistor delivers bias current to an 8.2V zener diode at the base of the npn transistor and provides base current to the npn. This arrangement sets the npn's emitter and the FET gate connected to it at 7.5V-more than enough voltage for a logic-level FET. The input to IC, also connects to the emitter through an RC filter. A convenient feature of this circuit is that the IC switch voltage feeds back through the diode to the input (bootstrapping). This connection allows for a small boost in efficiency, negating the loss of efficiency from using a cascoding FET and the emitter-follower circuit. Figure 2 shows the efficiency of the regulator with and without the bootstrapped diode at different load currents. (DI #2439).



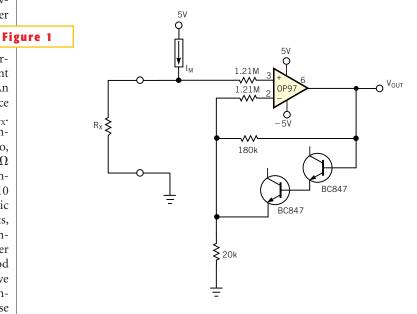
This bootstrapped high-voltage regulator uses all surface-mount components.

Edited by Bill Travis and Anne Watson Swager

Scheme cancels amplifier error

David Magliocco, CDPI, Scientrier, France

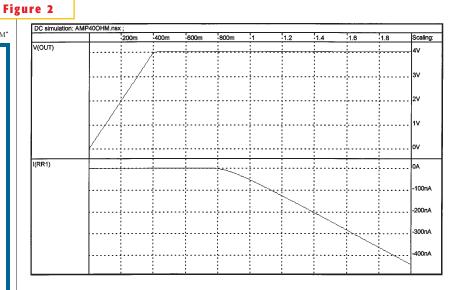
HE CIRCUIT IN Figure 1, using a lowoffset amplifier, is a basic ohmmeter circuit common in multimeters, except for the addition of the two diode-connected transistors. A current source supplies a selectable current ranging from 100 nA to 1 mA to RX. An A/D converter with a 400-mV reference voltage reads the voltage drop across R_v. Manufacturers of handheld DMMs limit I_{M} to 1 mA to save battery power. So, to measure resistance lower than 40Ω with 10-m Ω resolution, you need to amplify the voltage drop across R_x by 10 times to fully use the ADC's dynamic range. For high-precision measurements, you need a low-offset, high-input-impedance amplifier. The moderate-power OP97 from Analog Devices is a good choice. Because the OP97's inputs have back-to-back diode protection, differential input voltages greater than 1V cause current to flow through the diodes, causing measurement errors. For example, errors can occur when you try to measure a high value of R_{y} , say a fe



ideas



w megohms, with a wrong value of N_X , say a \Box	
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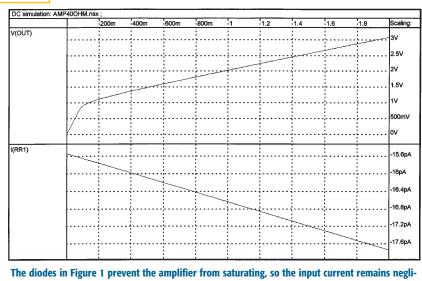
Without the diodes in Figure 1, the amplifier saturates, and current flows in the differential inputs.

www.ednmag.com



Not all the measurement current goes to R_x, so the converted value is inaccurate. Figure 3

Figure 2 shows V_{OUT} and the current that goes into the noninverting input of the OP97 (without the diode-connected transistors), configured for a gain of 10, for input voltages as high as 2V. For V_{IN} greater than 1V, the leakage current becomes non-negligible in comparison with the lowest values of I_M. A simple way to limit the leakage current is to limit the gain of the amplifier for high input voltages. To prevent the differential input voltage from exceeding 1V, you can reduce the gain by limiting the voltage across the feedback resistor. When that voltage reaches approximately 0.8V, for example for $I_M R_x \simeq 10$ mV, the two diode-connected transistors start to conduct and limit the gain. Transistors are better than signal diodes because they have lower leakage current at low voltages. Low leakage current is critical in avoiding additional errors when reading the output of the OP97. Figure 3 shows V_{OUT} and the current that enters the non-



gible with respect to I_M.

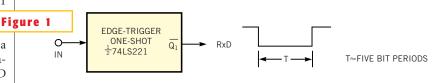
inverting input of the OP97 for input voltages as high as 2V in the circuit of **Figure 1**. The leakage remains low in

comparison with I_M. (DI #2447) To Vote For This Design, Circle No. 301

Serial port provides interrupts for 8031 μC

N Kannan, Mediatronix Ltd, Trivandrum, India

OU CAN USE THE RXD PIN of an 8031 μC for external interrupts (Figure 1). You program the serial port to receive in Mode 2 with a baud rate either ¹/₃₂ or ¹/₆₄ of the oscillator frequency, depending on the SMOD bit in the PCON register. In serial mode, the start bit should be a zero, and the stop bit should be a one for a valid reception. The µC generates the interrupt upon reception of a low start bit, nine data bits, and a high stop bit; the interrupt occurs at the end of reception. The one-shot multivibrator in Figure 1 provides a low pulse (the start bit) to the RxD input with a width greater than one bit period; for example, four periods. The bit period depends on the baud rate. Whenever an external signal edge-triggers the one-shot,





the 8031 enters serial-reception mode and generates an interrupt after 10 bit periods. The only disadvantage of the method is that at least 10 bit periods should occur between interrupts. Also, you should use the μ C's ISR pin to reinitialize the controller for the next interrupt. If you can't guarantee the minimum period between interrupts, then you can use a dual 74LS221 one-shot multivibrator. You can use the rising edge at $\overline{Q_1}$ to trigger a second one-shot and then use the output of the second to clear the first one-shot. This action forces $\overline{Q_1}$ to a high state for five to six bit periods to ensure a high stop bit. (DI #2441)



ADC-to-PC interface transfers data in nibbles

DS Oberoi, Jammu, India

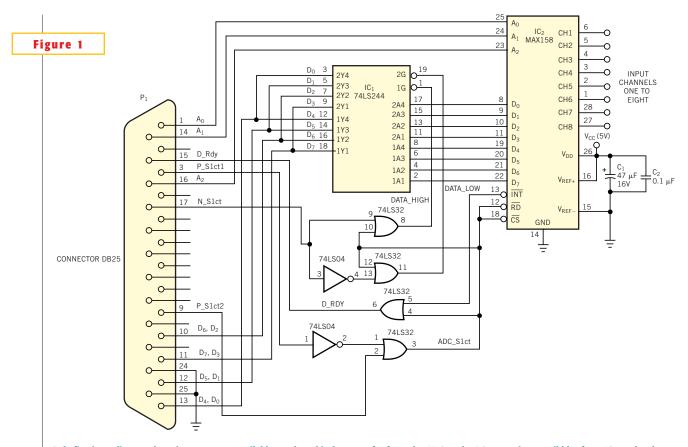
THE CIRCUIT IN Figure 1 uses a Centronics printer port to interface an eight-channel, 8-bit ADC to a PC. The circuit cuts the cost of addressing and decoder circuitry and saves one expansion slot for interfacing. The design uses three of the subport's various signals as control signals for channel selection, handshaking, and data transfer to the MAX158 ADC. These signals are programmable by means of a bit position in the control word of the respective port.

Two signals, P_Slct1 and P_Slct2, when high and low, respectively, select the MAX158 ADC. This arrangement overcomes any accidental-selection problem, which can happen when you use a single select bit. A falling edge at the RD and CS pins of the MAX158 initiates a conversion, and the read operation latches the multiplexer address inputs, A_0 through A_2 , for the channel selection. The level at the INT pin of IC₂ indicates the status of the conversion process. A low level at INT indicates that conversion process is over and that the converted digital data is available. The INT pin interfaces to the port through the D_Rdy signal. The corresponding software repeatedly samples this line to check its status. When D_Rdy is low, the PC reads the converted digital data through IC₄.

Only five input lines to the printer port are available, so the 8-bit data transfer occurs in two nibbles from IC₁. The higher or lower nibble is available when IC₁'s Pin 1 or Pin 19 is low, respectively. Under the control of the N_Slct signal, only one of these pins is low at once. The software then combines two nibbles to complete 1 byte of data. The circuit uses the fifth input bit, which is the D_Rdy signal, to check the conversion status of IC₂.

 V_{REF} + and bypass capacitors C_1 and C_2 connect to a 5V input supply, which results in a full 0-to-5V conversion. A 7805 regulator (not shown) generates V_{CC} .

The accompanying C program works satisfactorily and can scan all the channels one after the other and print the converted data on the screen. You can download the program from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2448. (DI #2448)



Only five input lines to the printer port are available, so the 8-bit data transfer from the ADC to the PC occurs in two nibbles from IC₁, under the control of the N_Slct signal from the PC.



Matched offsets put signals into ADC's range

Michael Petersen, Iowa State University, Ames, IA

THE CIRCUIT IN Figure 1 measures a voltage that is negative with respect to the system's ground point. The constraint is that the a single supply powers the ADC, and its ground point is fixed relative to the measured voltage. A simple current source and matched resistor set provide the necessary offset to bring the voltage within the ADC's common-mode range.

This circuit was designed for measuring the current from a set of power trackers on the Iowa State University Solar Car, the PrISUm Phoenix. The power trackers provide impedance matching between the solar array and the main electrical bus on the car. Because the current shunt for the power trackers is on the low side and the ground reference point is on the electrical-system side of the shunt, the voltage is normally negative with respect to the system ground.

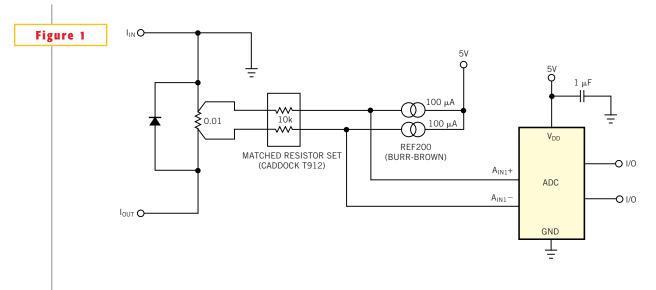
The current to be measured flows through the 0.01Ω shunt. Because the voltage is negative with respect to the system ground, you must add an offset to place the signal within the common-mode range of the ADC. The REF200

matched current sources and the 10-k Ω matched resistors create this offset. This scheme provides a positive offset of approximately 1V with a reasonable temperature coefficient. Because the ADC measures a differential voltage, the exact offset is unimportant as long as both legs have the same offset and remain matched. For this application, 1V is an adequate offset because the maximum current expected to flow through the shunt is only 10A, which equates to a maximum differential voltage of only 0.1V. You can easily modify this offset for other current-and-shunt-resistor combinations by selecting different resistor values for the matched resistor pair. Take care not to make the resistance values too high because high values may cause settling-time errors on the ADC's input.

Suitable ADCs for this circuit are the AD7705 (Analog Devices) and the ADS121x (Burr-Brown Corp). These ADCs provide system-calibration capabilities that let you easily correct for slight mismatches in the current sources and resistors. The system-gain- and systemoffset-correction features enable the circuit to maintain accuracy even in the presence of these mismatches. To adjust for offset, apply zero current and instruct the ADC to perform the system-offset calibration. To perform gain calibration, apply a current that corresponds to full scale and instruct the ADC to perform the system-gain calibration. You can obtain these calibration values, store them in the μ C, and then send them to the ADC upon subsequent power-ups, eliminating the need for calibration on every power-up.

The diode across the current shunt passes any high-current transients when you apply the power source. In the original design, this feature was necessary to pass the high-current surge that charged the power tracker's output capacitors when the power trackers switch into the system. Without the diodes, this surge destroyed the current shunt. Depending on the application and the size of the current shunt, these diodes may be unnecessary. (DI #2450)

To Vote For This Design, Circle No. 304



A simple current source and a matched resistor set provide the necessary offset to bring the voltage within the ADC's common-mode range.

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Amplifier compensates piezoelectric-rate gyros

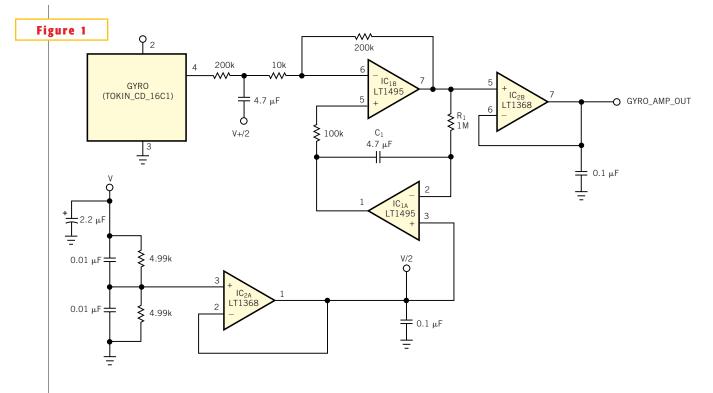
Jim Mahoney, Linear Technology Corp, Milpitas, CA

ow-power, low-cost ceramic piezoelectric rate gyros are available, but they lack the low-temperaturecoefficient characteristics of their quartz counterparts. However, you can use a servo amplifier to remove the dc level shift due to temperature-related drift effects (Figure 1). The original application of these small, rugged gyros was for damping video-camcorder jitter, but these devices suit many other applications, including camera-platform stabilization, radio-controlled-airplane- and helicopter-rate-damping-control assistance, remotely piloted vehicles, and computermouse motion sensors.

By setting the time constant of the servo loop in **Figure 1**, the circuit responds at an appropriate low frequency for the system under control. The time constant you use for the servo loop depends on the dynamics of this system, but 10 to 50 times the lowest frequency of interest is a good starting point. The dc-level drift occurs at a slow rate and hence appears to be a valid response. However, the rategyro amplifier also passes some frequencies above the set frequency. (The corner frequency of the highpass filter depends on what the circuit is controlling.)

Amplifier IC_{1A} and its servo-driver stage, IC_{1B} , comprise a low-power op amp. The servo controlling the dc level ac-couples, or highpass-filters, the gyro's output by forcing the output of IC_{1A} to swing around V÷2. The lowest frequency that the circuit passes is a function of the C_1/R_1 time constant. The maximum value of R_1 depends on the minimum input bias current of the op amp, which is 250 pA for the LT1495. If space permits, C_1 should be a good low-leakage type, such as polystyrene, Teflon, or polypropylene. A Mylar capacitor compromises the integrator's performance.

The gyro and its amplifier can be some distance from the main processing circuit, and cable capacitance can cause many op amps to oscillate. However, the LT1368, IC_{2B} , at the output can drive cable capacitance without stability problems. The LT1368, IC_{2A} , also serves to drive a filter capacitor to provide a lownoise $^{1}/_{2}V$ reference point for the LT1495 servo driver. (DI #2453)



Servo amplifier IC_{1A} removes the dc level shift due to temperature-related drift effects of a piezoelectric-rate gyro.



Digital camera subs as a scope camera

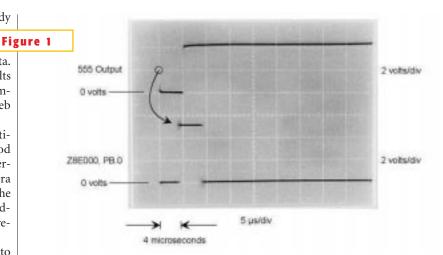
Allen Moore, Redmond, WA

A DIGITAL CAMERA can be a handy substitute for an oscilloscope camera for older scopes that cannot output hard copy or digital data. A digital camera provides instant results and allows you to easily enhance the image and then add it to reports or Web pages.

If the scope has an illuminated graticule, turn up the illumination. A tripod is useful for repeated shots but is otherwise unnecessary. Position the camera and adjust the camera's zoom so that the oscilloscope screen fills the picture. Adjust lighting and position to minimize reflections.

After you take the picture, transfer it to a PC. You can then use an image-editing program to crop, rotate, and otherwise enhance the photo as necessary. To add annotations, such as text and arrows, to the image, you can import the image into a drawing program, although some image-editing programs offer this capability as well. You can then print the final image, insert it in a document, or add it to a Web page.

For output to monochrome devices, such as a black-and-while printer, it can be advantageous to first convert the color image to monochrome and then re-



If you use an old oscilloscope lacking hard-copy- or digital-output capability, you can use a digital camera to capture, save, and annotate the oscilloscope image

verse the result: Change the white to black and the black to white. This procedure results in sharp, dark lines for the oscilloscope traces against a light-gray background. Some digital cameras have a monochrome mode.

The image in **Figure 1** illustrates the results of this procedure in capturing a timing measurement using a Sony Mavica MVC-FD7 camera set to mono-chrome mode. After image capture, the

next step is cropping the resulting JPEG image using Microsoft Photo Editor 3.0 and then applying a reverse effect to swap the black and white tones. Finally, importing the image to Micrografx Windows Draw 6.0 allows you to add annotations, such as in the **figure**. (DI #2452)

To Vote For This Design, Circle No. 306

MOSFET pair makes simple SPDT switch

Howard Chen, Vishay Siliconix, Santa Clara, CA

WW ITH AN N-AND P-CHANNEL MOS-FET, you can easily implement a single-pole double-throw (SPDT) switch to isolate part of a circuit and power it from a secondary supply for standby operation while the rest of the circuit is off (**Figure 1**). By using a complementary pair, you can use a single control input for the MOSFETS. An Si4501DY MOSFET in this topology exhibits less than a 0.1V drop at 5A for the main element and contains both MOS-FETs in an SO-8 package.

When the 2N7002 or similar control MOSFET ties the gates together and pulls them to ground, the p-channel MOSFET is on. Pulling the gates above the supply rail by turning the 2N7002 off results in turning the n-channel MOSFET on. Pulling the gate of the p-channel MOS-FET above the source potential has no effect; the MOSFET remains off with low leakage.

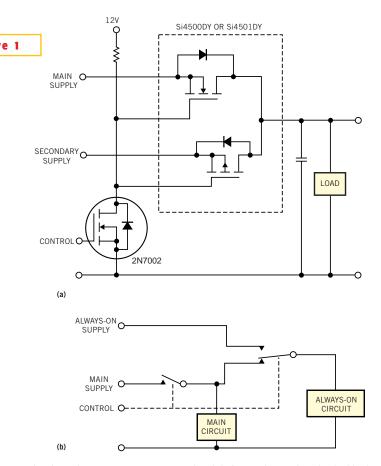
The resultant switch is a break-beforemake configuration, which is necessary to ensure that the secondary, or alwayson, supply never has to power the whole



circuit. However, due to the fast switching of the MOSFETs, extra capacitance beyond normal design rules is probably unnecessary to maintain the operating voltage.

The arrangement of the n-channel device in the circuit ensures that the internal diode does not conduct while the subcircuit is isolated. In this direction, the n-channel MOSFET also provides a fail-safe path for the circuit's power through the diode. The forward voltage of the p-channel MOSFET's diode blocks any current from "back-feeding" the secondary supply, assuming that the two supplies are close in voltage.

An example of an application for this circuit is the Advanced Configuration and Power Interface in desktop computers providing instant-on and low power consumption in standby. The main power supply is a high-power switching power supply, and the secondary supply is a 60-Hz transformer with linear regulation. (DI #2451)



To Vote For This Design, Circle No. 307 An n- and p-channel MOSFET pair comprises a break-before-make, single-pole, double-throw switch (a). The switch isolates part of a circuit and powers it from a secondary supply during standby operation when the rest of the circuit is off (b).

Motor controller operates without tachometer feedback

Bruce Trump, Burr-Brown Corp, Tucson, AZ

SPEED CONTROLLERS have long exploited the reverse-EMF characteristics of dc motors to control their speed. These linear driver circuits use power op amps to create a negative resistance drive to the motor that counteracts the voltage drop in the motor's series resistance (**Reference 1**). The circuit in **Figure 1** shows an implementation of this type of speed control using a PWM drive, which reduces power dissipation in the drive circuitry. Control voltage V_{IN} sets the speed, and IC₁, Q₁, and R₃ convert V_{IN} to a 0- to 200µA current. The current source controls the duty cycle of the PWM driver, IC₂, at Pin 3. D₁, D₂, and R₅ prevent the circuit from pulling the control input too low, which can cause an inversion in the control loop.

Motor current flows through the internal switching transistor in IC_2 out the common terminal and through the current-sense resistor, R_s . The circuit filters and scales the voltage across the sense resistor to provide positive feedback to the input circuitry through R_2 . With the proper amount of positive feedback, an increase in motor load increases motor current, which increases duty-cycle drive to maintain constant speed.

The equation of speed balance is

$$I_{M}(R_{M} + R_{S}) = I_{M}R_{S}\left(\frac{R_{1}}{R_{1} + R_{2}}\right)\left(\frac{V + R_{3} \times 200 \,\mu\text{A}}{R_{3} \times 200 \,\mu\text{A}}\right).$$

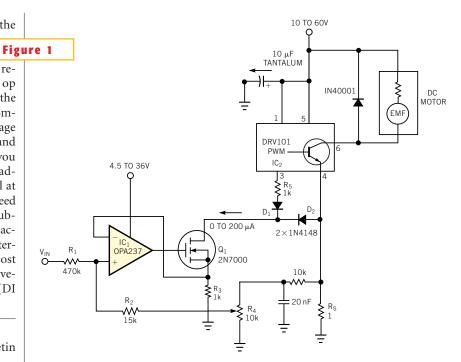


This model neglects losses in the switching circuitry of IC2. Depending on supply voltage, such losses may significantly affect the required feedback. Unlike the power op amp implementation of the scheme, the absolute supply voltage affects this compensated PWM controller. The voltage lost in switching is not truly resistive and can be tricky to model. In practice, you can optimize the speed control by adjusting the positive feedback control at R₄. With proper adjustment, motor speed remains relatively constant with substantial changes in load. Although less accurate than true closed-loop tachometerfeedback controllers, this low-cost technique provides a dramatic improvement over simple voltage drive. (DI #2449)

Reference

1. Burr-Brown Applications Bulletin AB-152

To Vote For This Design, Circle No. 308



Positive feedback derived from current-sense resistor R_s increases the duty-cycle drive from PWM controller IC, to compensate motor speed with varying loads.

Edited by Bill Travis and Anne Watson Swager

Cascade ABCD two-port networks

Bert Erickson, Thomson Consumer Electronics, Fayetteville, NY

ELEPHONE SUBSCRIBER LINES have become a topic of intense interest for organizations attempting to transmit Internet signals on telephone lines. Basic loop standards exist, and tables of twisted-pair primary constants extending to 20 MHz are in the literature. Asymmetric digital-subscriber lines (ADSLs) are now available for high-speed Internet service. The telephone industry has always used two-port networks in the form of ABCD matrices to cascade sections of telephone cable. These configurations allow you to join the sections by matrix multiplication. However, because the elements in the matrices are complex numbers and several sections make up a chain, you need to organize the process of matrix multiplication. A short computer program performs this task (Listing 1). You enter the number of matrices in the chain and then enter the real and imaginary parts for each A, B, C, and D element. The product then appears on the screen.

The two-port matrix equation with

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the ABDC parameters has the following format:

^{Ign}ideas

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & C \\ B & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \xrightarrow{I_1} \underbrace{V_1}_{C} \xrightarrow{A & B} \underbrace{V_2}_{C} .$$

where

CLS

$$A = \frac{V_1}{V_2} \Big|_{I_2 = 0} \quad B = \frac{V_2}{I_2} \Big|_{V_2 = 0} C = \frac{I_1}{V_2} \Big|_{I_2 = 0} D = \frac{I_2}{I_2} \Big|_{V_2 = 0}$$

A represents the open-circuit transfer function, B represents the short-circuit transfer impedance, C represents the open-circuit transfer admittance, and D represents the short-circuit current ratio. You can find the ABCD matrix for a ladder network composed of RLC elements by slicing the network into series and shunt matrices. You then multiply the product of the first two by the third, and the progression continues with additional subscripts identifying the components. In the final product, the elements A, B, C, and D-with all their component symbols-may become quite cumbersome. To avoid these complicated expressions in the matrix for the ladder network, don't use them. Rather, enter the numerical values for the series and shunt components along with the necessary 0,0s and 1,0s. You can use this concept for any network comprising passive components that you can separate into isolated twoport sections. You can also use the method to predict the degradation a bridged tap produces in a telephone cable.

The progression of entering values for cascaded networks is normally from left to right, or from source to load with the

LISTING 1–CASCADING TWO-PORT NETWORKS PRINT SPC(8); : INPUT "Enter number of 2X2 matrices, n => 2

```
 \begin{array}{l} \text{DIM } a(n \ - \ 1) \ , \ b(n \ - \ 1) \ , \ c(n \ - \ 1) \ , \ d(n \ - \ 1) \\ \text{DIM } e(n \ - \ 1) \ , \ f(n \ - \ 1) \ , \ f(n \ - \ 1) \ , \ h(n \ - \ 1) \ , \ t(7) \\ \text{FOR } j \ = \ 0 \ \text{TO } n \ - \ 1 \end{array} 
PRINT SPC(8); "For matrix number
                                                                                                                                           "; j + 1
PRINT SPC(16); : INPUT "Enter A and E "; a(j), e(j)
PRINT SPC(16); : INPUT "Enter B and F "; b(j), f(j)
PRINT SPC(16); : INPUT "Enter C and G "; c(j), g(j)
PRINT SPC(16); : INPUT "Enter D and H "; d(j), h(j)
NEXT j
GOSUB 1
END
 1 FOR j = 1 TO n - 1
      For j = 1 to n - 1

t(0) = a(j - 1) * a(j) - a(j - 1) * a(j) + b(j - 1)

t(1) = a(j - 1) * a(j) + a(j - 1) * a(j) + b(j - 1)

t(2) = a(j - 1) * b(j) - a(j - 1) * f(j) + b(j - 1)

t(3) = a(j - 1) * f(j) + a(j - 1) * b(j) + b(j - 1)

t(4) = c(j - 1) * a(j) - g(j - 1) * a(j) + d(j - 1)
                                                                                                                                                                                                 c(j)
                                                                                                                                                                                                                          £(j
                                                                                                                                                                                                 g(j) + f(j - 1)
d(j) - f(j - 1)
                                                                                                                                                                                                                                                               c(j)
                                                                                                                                                                                                                                                               h(j)
                                                                                                                                                                                         \begin{array}{c} a_{(j)} - f_{(j-1)} + f_{(j)} \\ * h_{(j)} + f_{(j-1)} * d_{(j)} \\ * c_{(j)} - f_{(j-1)} * g_{(j)} \\ * g_{(j)} + h_{(j-1)} * c_{(j)} \\ * d_{(j)} - h_{(j-1)} * h_{(j)} \end{array}
      \begin{aligned} t(4) &= o(j-1) * a(j) - g(j-1) * e(j) + a(j-1) \\ t(5) &= c(j-1) * b(j) + g(j-1) * a(j) + d(j-1) \\ t(6) &= o(j-1) * b(j) - g(j-1) * f(j) + d(j-1) \\ t(7) &= c(j-1) * f(j) + g(j-1) * b(j) + d(j-1) \\ a(j) &= t(0) : b(j) = t(2) : c(j) = t(4) : d(j) = t(6) \\ e(j) &= t(1) : f(j) = t(3) : g(j) = t(5) : b(j) = t(7) \\ maximum contained (15) + t(0) + t(1) + t(2) + t(3) \end{aligned}
                                                                                                                                                                                                                                        - 1)
                                                                                                                                                                                                                 + h(j
                                                                                                                                                                                                 h(j)
       PRINT : PRINT SPC(16); t(0); t(1), t(2); t(3)
PRINT SPC(16); t(4); t(5), t(6); t(7)
       NEXT 1
       RETURN
```



current pointing toward the load. If you reverse the progression, the direction of the current is usually reversed, and the location of elements A and D is reversed to conform to the reciprocity theorem. The matrices for a single series component and a single shunt component are as follows:

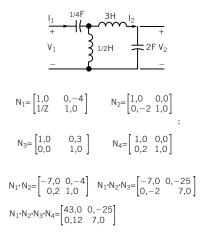
$$\xrightarrow{Z} \begin{bmatrix} 1,0 & Z \\ 0,0 & 1,0 \end{bmatrix} Z \begin{bmatrix} 1,0 & 0,0 \\ 1/Z & 1,0 \end{bmatrix}$$

You can use these simple matrices to represent RLC components, transformers, and bridged taps in telephone cables. However, for a telephone cable, you must consider the reflected wave. Thus, you must express the A, B, C, D elements by the following hyperbolic functions:

 $\begin{array}{l} A = \cosh(\gamma d), \\ B = Z_0 \sinh(\gamma d), \\ C = (1/Z_0) \sinh(\gamma d), \text{ and } \\ D = \cosh(\gamma d). \end{array}$

where the propagation constant $\gamma = \alpha + \beta$, d is the electrical length of the cable, and Z_0 is the characteristic impedance. In the United States, the nominal

value for Z_0 is 100V, which is also the specified value for the source and load impedance. Because γ is a complex number, A, B, C, and D are also complex numbers, or the polar equivalent thereof. These numbers are not difficult to calculate; however, the parameters depend on the application (**references 1** and **2**). The following example shows how to enter the data and read the results:



Within the solid bars, N₁ through N₄ show the entered data for the compo-

nents. The bottom line shows the matrix product as it appears on the screen. For this network, the matrix elements are A=43+j0, B=0-j25, C=0+j12, and D=7+j0. The open-circuit voltage ratio is $V_1/V_2=A=43$. The open-circuit transfer admittance I1/V2=C=0+j12. The input impedance is $Z_{IN}=A/C=0-j$ (43/12). Listing 1 uses easy-to-read and-compile QuickBasic. You can download this listing from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2455. (DI #2455)

References

1. Rauschmayer, Dennis, *ADSL/VDSL Principles*, MacMillan Technical Publishing, 1999.

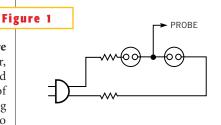
2. Chen, Walter, *DLS: Simulation Techniques and Standards Development of Digital Subscriber Line Systems*, MacMillan Technical Publishing, 1998.

> To Vote For This Design, Circle No. 426

Simple tester checks Christmas-tree lights

William Dias, Brown & Sharpe, North Kingstown, RI

HY IS IT THAT YOU always test 48 bulbs before you find the bad one in a 50light string? The simple circuit in Figure 1 allows you to divide and conquer, greatly reducing the time it takes to find the bad bulb. The circuit uses a pair of NE2 neon bulbs with current-limiting resistors. You can use a pair of Radio Shack 272-1100 bulb-resistor sets. It's convenient to house the tester in a clear piece of plastic tubing, with the probe tip emerging from one end and a light-duty power cord emerging from the other end. You place the bulbs in the tube such that one is close to the probe tip and the other is near the power cord, so it's easy to re-



A simple probe set cuts the time you spend troubleshooting a series-string light set.

member which bulb lit last. The probe tip connects to common point between the neon bulbs. It consists of thin spring wire with all but the last ¹/₄ in. insulated. You use the bare tip to make contact with the crimp connectors in the base of the bulbs.

Series-string Christmas-tree lights come in two types. The first type is the continuous-series string (**Figure 2a**). In this configuration, one wire from the plug goes from bulb to bulb until it reaches the last bulb. A return wire bypasses all the bulbs and returns to the plug. The second type is the alternatingseries string (**Figure 2b**). In this connection, one wire from the plug goes to the first bulb, and the other wire from the plug goes to the second bulb. The connections then alternate through the string. To troubleshoot a defective continuous series string:



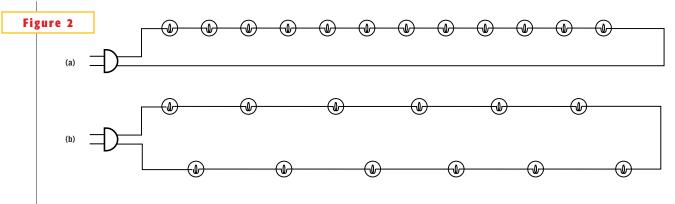
- Plug in both the tester and the bulb set.
- Insert the tip of the tester's probe into the wire hole in the base of the first bulb. One of the neon bulbs should light; remember which one.
- Move halfway down the set and insert the probe again. If the same neon bulb lights, then the problem is in the second half of the set. If the other neon bulb lights, then the problem is in the first half of the set. Either way, you are testing 25 of the 50 bulbs without breaking into a sweat.
- If the original neon bulb lights, move halfway down the remaining

part of the set and try again. If the other neon bulb lights, you must move back halfway to the last bulb you tested and try again. This process should allow you to find a bad bulb in a set of 50 in only seven steps. You know you have the bad bulb when inserting the probe tip into one side of the bulb lights one neon bulb and placing the tip in the other side lights the other neon bulb.

To troubleshoot a defective set with many bad bulbs, use the same process as above. At some point, you will reach the dead spot between two or more bad bulbs. When you reach this point, neither neon lamp will light. Back up, just as if the other neon bulb had lit. You know you have a bad bulb if the probe lights when you plug it into one side and nothing lights when you plug it into the other side. Replace this bulb and start over.

To troubleshoot an alternating-series string, you must work in pairs. Test the first bulb, and one neon bulb lights. Test the second bulb, and the other neon bulb lights. Now move down the set an even number of lights and test the next pair of lights. When you pass the bad bulb, the same neon lamp lights for both seriesstring bulbs. (DI #2457).

> To Vote For This Design, Circle No. 427



Series-string light sets come in two flavors: a continuous-series string (a) and an alternating-series string (b).

Power meter uses low-cost multiplier

Jeff Kotowski and Alan Johnston, National Semiconductor, Grass Valley, CA

A power-METER CIRCUIT typically requires either an analog or a digital multiplying circuit. These circuits can be complex, finicky, or expensive. A simpler way to achieve the multiplication first converts the current to a duty cycle proportional to the current. You can use this duty cycle to gate the input voltage; the gating effectively provides a multiplication function. A lowpass filter then provides an output voltage proportional to power. The method sounds convoluted, but the implementation is simple. **Figure 1** shows the complete power-meter circuit. The National Semiconductor LM3812M-7.0 IC senses current and delivers a duty cycle proportional to the current. The current relates to the dutycycle output as follows:

$I = 22 \bullet (DUTY _ CYCLE - 0.5).$

The desired output is a voltage equal to

the input power divided by 10. The divide-by-10 operation keeps the voltage within a manageable range. The output is, then:

$$V_{OUT} = V_{IN} \bullet I/10 = 2.2 \bullet$$

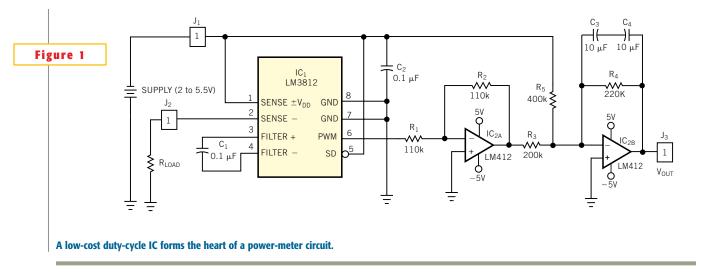
$$\begin{bmatrix} DUTY_CYCLE \bullet V_{IN} - \frac{1}{2} \bullet V_{IN} \end{bmatrix}$$

To subtract the $\frac{1}{2}V_{IN}$ term in the equation, the first op amp inverts the power signal. The second op amp adds in the



offset and again inverts the signal. Capacitors C_1 and C_2 provide filtering. These capacitors connect back-to-back to achieve nonpolar operation. Tests with input currents of -7 to +7A and with a source voltage of 2 to 5.25V showed better than 3% accuracy over the range of 0 to 25W. (DI # 2458)

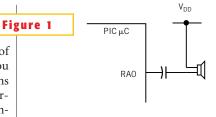
To Vote For This Design, Circle No. 428



Add music to your next project

Rodger Richey, Microchip Technology Inc, Chandler, AZ

DDING MUSIC TO YOUR next design is as simple as using one I/O pin to drive the speaker and approximately 150 words of program memory to play the music. You can store the musical notes and durations internally in program memory or externally in a serial EEPROM. Frequently, implementing musical playback requires an external processor with memory or a specialized melody device. Both cases can bring increased cost and can limit the number of songs you can play back. The approach described here uses a Microchip Technology midrange PIC µC with a free 8-bit timer resource. Two implementations are possible. The one presented here uses internal program memory to store the musical notes. This method allows as many as 127 notes per song. The other technique is to use an ex-



You need only one I/O pin and a capacitor to generate music with a PIC mC.

ternal serial EEPROM to store the notes.

The first important point to consider is that the musical playback is completely interrupt-driven. Therefore, the main application can run in the foreground and can accept interrupts as necessary from the musical playback. Timer0 controls the playback; you can find it on any of the midrange PIC μ Cs—from the eight-pin PIC12C671 to the 68-pin PIC16C924. This timer is a generic 8-bit timer with an 8-bit prescaler. You can download the assembly code from EDN's Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2556. The code is designed to run a PIC µC at 4 MHz. You can accommodate other frequencies by changing defines in the code. At 4 MHz, you use a 1-to-8 prescaler to provide the correct frequencies for the notes to play. Again, you can modify the prescale value to suit the desired operating frequency by changing the value in the Option register. One I/O pin provides the musical notes to the speaker. Figure 1 shows the simple connections. You can modify the source code and hardware to drive the speaker differentially using two I/O pins.

Toggling an I/O pin at twice the fre-



quency of the desired note generates each note. This technique creates softwarebased pulse-width modulation with a 50% duty cycle and a tone at the desired frequency. At each Timer0 interrupt, the routine reloads TMR0 with the number of ticks for the desired frequency. You use the following formula to calculate the number of ticks for each note:

TICKS(Freqx)= [256-((CLOCK/4/PRESCALER/ Freqx/2)-1)]

Using CLOCK=4MHz, PRESCALER =8, and Freqx5523, the calculated number of ticks for an A tone is 137. The number of ticks required is actually 118, but by subtracting this number from 256 in the formula, you can get the value to load into TMR0. A table designated Notes in the source code lists only seven notes, but it's easy to add more. You can determine the duration of each note by counting the number of Timer0 inter-

rupts. Because the timer interrupt period differs for every note, the number of Timer0 interrupts differs for every note. A table called Durations in the source code contains the note duration for the corresponding note in the Notes table. On each Timer0 interrupt, the Notes value loads into TMR0 and the note duration decrements. At the end of each note, a pause of $\frac{1}{64}$ occurs to emphasize the note you are playing. The routine creates the pause by not toggling the output pin during the pause interrupts. Again, each note requires a different number of interrupts to generate a pause of a set duration. To simplify the pause generation, the program subtracts the number of interrupts required for a pause from each note duration. The routine creates the pause by setting the timer such that the pause occurs from one timer interrupt. If the clock frequency is such that you cannot create the pause with one interrupt, you can alter the value STOP_LENGTH in the source code. The program loads the next note to play after the pause interrupt. A 0 in the Notes and Durations tables in the source code denotes the end of the song. At this point, the program plays the song again.

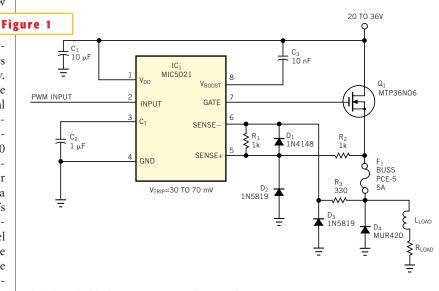
Using internal memory to store the notes and durations has some limitations. Without some extra table-handling code, tables are limited to 255 elements and must start on a 256-byte boundary. Because the duration values are 16 bits long, the number of notes the PIC μ C can play is 127. Depending on the size of program memory, you can place many songs in 256-byte blocks and play them individually. By using two more I/O pins (SCL and SDA), the PIC μ C can interface to an external serial EEPROM and play any number of notes up to the maximum memory size divided by 3. A 24LC01B from Microchip Technology can hold 341 notes plus corresponding durations. (DI #2456)

To Vote For This Design, Circle No. 429

PWM circuit uses fuse to sense current

Eugene Kaplounovski, Nautilus International, Burnaby, BC, Canada

IGH EFFICIENCY AND, hence, low loss is a usual design goal for a PWM circuit. Figure 1 shows one of several channels of lowloss PWM control for hydraulic valves used in heavy industrial machinery. These valves usually have dc resistance of approximately 12Ω and substantial inductive reactance. The operating voltage is 24V, and the PWM circuit usually operates at frequencies of 50 to 500 Hz to prevent valve sticking. To minimize on-resistance losses in the power MOSFET, the circuit uses a Motorola MTP36N06, even though that device's current-handling capacity greatly exceeds the load requirements. A Micrel MIC5021 high-side driver provides gate control; its high slew rate minimizes the MOSFET's switching losses. To implement the overload-protection feature in

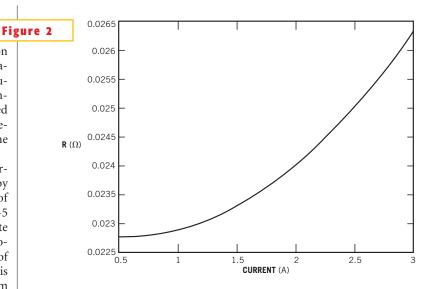


A fuse does double duty as a protection device and a current-sensing resistor.



the gate driver, a low-resistance current-sensing resistor is necessary. Safety requirements and common sense mandate protection against catastrophic component failure. Unfortunately, the resistance of the fuse contributes to circuit losses. The combined losses in the fuse and current-sensing resistor are comparable with those in the rest of the circuit.

You can sometimes replace the current-sensing resistor by the fuse, thereby eliminating one of the two sources of loss. The dc resistance of a Buss PCE-5 5A fuse is 20 to 30 m Ω , which is quite close to the value that the overload-protection circuit requires. The trip point of the MIC5021 overcurrent comparator is nominally 50 mV, but it may vary from 30 to 70 mV. Such wide tolerance makes setting a precise trip point with a precision resistor impossible. Another of the fuse's benefits is its positive temperature coefficient of resistance. The comparator's trip differential voltage also has a positive temperature coefficient. These two temperature coefficients track somewhat, offering some temperature compensation. Figure 2 plots the fuse-resistance behavior. The curve is an approximated mean value of resistance versus current. Data for the graph uses 10 sam-



Self-heating causes a positive temperature coefficient of resistance in the fuse in Figure 1.

ples of the fuse and a second-order polynomial function using Matlab software. According to Micrel's data sheet, the trip point is a linear function of the ambient temperature.

 R_2 and R_3 , along with D_2 and D_3 , provide protection against negative inductive-kick spikes at the comparator's inputs. Adding R_1 allows adjustment of the current trip point. D_1 does not conduct during normal operation but protects the

comparator from excessive differential voltage if the fuse fails. R_2 and R_3 limit the load current under this condition to a low and safe level. Disconnecting the fuse during experimentation leads to immediate shutdown, with only short (several-microsecond) pulses at the output. C_2 determines the time between the circuit's attempts to restart. (DI #2459)

To Vote For This Design, Circle No. 430

Bias supply accepts high inputs

Robert Sheehan, Linear Technology Corp, Milpitas, CA

HEN YOU DESIGN dc/dc converters, it is often necessary to generate a bias supply to operate the control circuitry from the raw input voltage. Many methods are available for configuring the bias supply, each with its own benefits and shortcomings. Some methods use a "trickle-charge" start-up circuit, with a back-feed winding to provide power under normal operating conditions. With a low parts count and cycling short-circuit protection (if leakage inductance to the back-feed winding doesn't cause cycling to stop), this configuration is widely used in the power-supply industry. However, the configuration suf-

fers from a long turn-on time and a limit on the capacitive load into which the converter starts up. Another popular approach uses a transistor-based pass regulator, often in conjunction with an overwinding to keep power dissipation low in normal run conditions. Although this method can provide a fast start-up, it generally exhibits high power dissipation during an output short circuit. Attempts to gate this type of circuit can be messy and complicated. A buck regulator overcomes the disadvantages but can be complex and costly. The circuit in Figure 1 uses IC,, an LT1431 shunt regulator, lowcost transistors, and an off-the-shelf in-

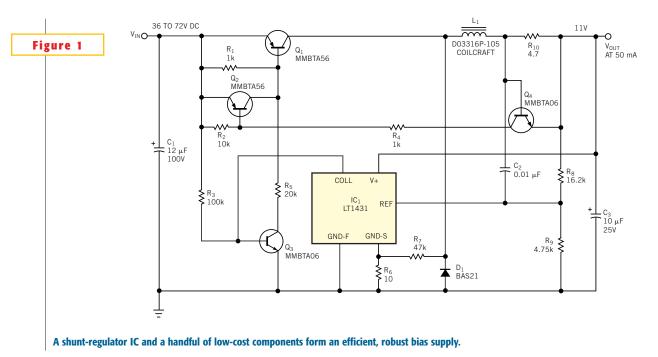
ductor to form a high-voltage converter for use as a bias supply.

The circuit needs no bleeder resistors or tertiary winding. The selection of Q_1 and Q_3 limits the maximum input voltage to 80V in the circuit as shown. The circuit operates as a hysteretic regulator, also called a ripple regulator, relaxation oscillator, or bang-bang controller. Positive feedback comes from R_6 and R_7 ; negative feedback comes from C_2 , R_8 , and R_9 . With a 48V input, inductor current is discontinuous, and the switching frequency is 50 kHz. Efficiency is typically 74% with a 48V input and a 50-mA load, an acceptable figure for bias-sup-



ply power. Q_2 and Q_4 provide short-circuit protection; thus, the design is robust. Short-circuit current is typically

120 mA. You can repeatedly hot-plug the circuit with no adverse effects. (DI #2454) To Vote For This Design, Circle No. 431



Method provides simple error-rate generator

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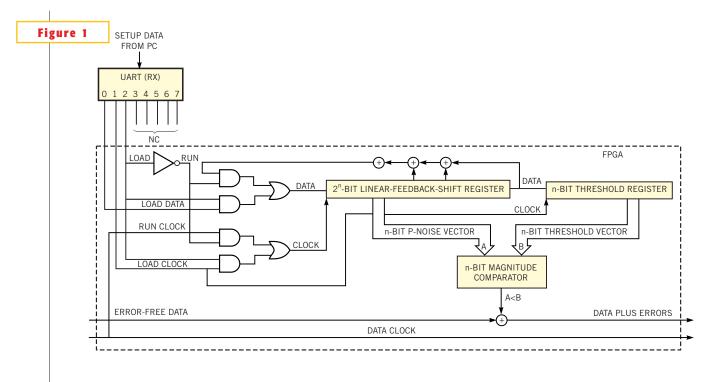
ESTING THE PERFORMANCE OF a system being fed random errors can be tricky; it is not easy to add an accurate, low-level bit-error rate to a data stream. The technique shown in Figure 1 (page 121) uses a PC, some simple software, and a few external components or an FPGA. The PC computes an n-bit threshold from the chosen bit-error rate, which then downloads to the FPGA. Using a magnitude comparator, the FPGA compares the threshold with the contents of the linear-feedback-shift register (LF-SR), which clocks at the same rate as the data stream. If the LFSR's contents are lower in magnitude than the threshold, an error occurs. If they are greater than or equal to the threshold, no error occurs. Thus, if you need 50% errors, you set the threshold to 1000...0; if you need 25% errors, you set the threshold to 0100...0, and so on. The PC translates from rates expressed as, for example, 1 in 10⁴, to such a threshold. The n-bit threshold should be long enough to achieve the desired accuracy. The LFSR must be longer than the threshold to minimize the effects of the LFSR's not generating the all-zeros state. Making the LFSR twice the length of the threshold vector is satisfactory. It is also necessary to randomize the starting point of the LFSR. You can do this by downloading random digits from the PC at the same time the threshold downloads.

You use the serial data port and a UART to control the FPGA and load data into it, by choosing one of the UART's output bits to set the Run/Load mode and two other output bits to drive the Data and Clock lines. You then write routines to translate loading information into sequences of asynchronous characters. Other methods are obviously available. Building the UART into the FPGA design is another clear improvement. If the threshold register is 32 bits long, the LFSR should be 64 bits long. You should choose the taps to give a sequence length of $2^{64}-1$. In other words, the choice should be in accordance with a primitive polynomial. **Reference 1** gives a useful list of taps that yield a maximal length sequence. One choice (chosen at random) requires three taps located at stages 2, 19, and 25 (**Figure 1**). The speed of operation depends on the capabilities of the FPGA. With modern FPGAs and a little care in the design, rates in the hundreds of megahertz are possible. (DI #2460)

Reference

1. Schneier, Bruce, *Applied Cryptography, Second Edition*, John Wiley, pg 408.





Using a PC and an FPGA, you can generate any percentage of random errors in a data stream.